0.18µm PHASE / FREQUENCY DETECTOR AND CHARGE PUMP DESIGN FOR DIGITAL VIDEO BROADCASTING FOR HANDHELD’S PHASE-LOCKED-LOOP SYSTEMS

THESIS

Presented in Partial Fulfillment of the Requirements for
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BY

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* * * * *

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ABSTRACT

A Phase/Frequency Detector and Charge Pump design is proposed in this paper. The design is used to be implemented for a frequency synthesizer for digital video broadcasting for hand held devices. The schematic designs of the circuits are implemented using TSMC 0.18µm CMOS technology. Two phase/frequency detector are proposed in this paper to show the effect of the dead zone on the performance of the frequency synthesizer. The main propose of these two PFD is to reach a low power consumption and small dead zone which was achieved by the second design where the current consumption is 3.4µA and the dead zone is 20ps. Next this paper will cover the design of a conventional charge pump which uses two 500µA switched current sources to charge up and down a capacitance load. At the end this paper will shows the simulation result of the PFD/CP system in typical situation and also the simulation result using Monte carol method to check the performance of the circuit in nontypical situation like different temperature or supply voltage variation.
Dedicated to my family
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CHAPTER 1

INTRODUCTION

Recently, plenty of researches have been conducted on mobile technologies. Most of these researches concern developing handheld devices to be able contain more capabilities and perform more functions. The main concern of the new technologies development is to have low power consumption and small size devices. Recent development that a lot of research has been conducted on is the digital video broadcasting for handheld devices. This new technology aims to enable handheld device such as cell phones to receive digital video signals and process them and display TV channels on the device screen. DBV-H frequency synthesizer architecture has been introduced in this paper with the design of the first two blocks of this architecture Phase/Frequency Detector and Charge Pump using TSMC 0.18μm CMOS technology which will allow the design to consume less power since the supply voltage will be 1.8v and occupy less PCB area [3, 4, 5, 6, 7, 8].

Before start talking about the blocks design, this chapter will give a brief idea about DVB-H system and the frequency synthesizer our lab developing for this system.

1.1 DVB-H systems:

DVB-H stands for digital video broadcasting for handheld devices. it is originally derived from DVB-T with some additions that allowed this new technology to be suitable
for handheld devices that depends on a limited power supply. The main idea of DVB-H is to efficiently allow multimedia services to be delivered to handheld devices over digital broadcasting networks. The word efficiently here refers to the system ability to consume low power since it targets handheld devices have limitations on power supply and varying transmission conditions due to mobility [10].

DVB-H operating frequency in US is between 1.67 and 1.675GHz, while for the European operating frequency is between 470 and 867MHz. Since DVB-H originally derived from DVB-T, it has all its standards with some new additions to make it suitable for handheld devices. One of these additions is the time slicing technique [9]. The main idea of using time slicing in DVB is to minimize the power consumption of the device that uses DVB-H [11]. In time slicing burst of data transmit in a time slot then for the rest of the time period there will be no data transmission as shown in figure 1.1. This scenario will help the handheld device to switch on the components when it receiving a data burst and switch them off during the rest of the time frame conserving power.
1.2 Frequency Synthesizer:

Frequency synthesizer plays a major role in the field of communication. The main job of frequency synthesizer is to create a set of frequencies that is a multiple of a reference frequency. The way the frequency synthesizer operates is as follow, it compares the phase and frequency of two inputs signals and produces an error signal that will produce a control voltage; this control voltage will be applied to a voltage controlled oscillator (VCO) which will produce and output frequency. The output frequency from the VCO will be fed through a frequency divider and the output of the frequency divider will be one of the two signals that have been compared. The other signal that has been compared is a reference frequency signal which will be produced using a crystal oscillator.

![Diagram of Frequency Synthesizer](image)

Figure 1.2: Frequency Synthesizer

As long as there is a phase or frequency error between the reference signal and the divider signal, the output frequency from the VCO will keep increasing or decreasing
until this error is zero. Once both reference frequency and the output frequency of the divider have no phase or frequency error we get a lock situation where both reference and divider signal has the same phase and frequency.

Frequency synthesizer has two designs:

1- Integer-N frequency synthesizer.

2- Fractional-N frequency synthesizer.

1.2.1 Integer-N frequency Synthesizer:

In this synthesizer, the output frequency of the VCO will be a multiple of integer N of the reference frequency. From figure 1.2 we can conclude that:

\[ f_o = N \times f_r \quad (1) \]

In this case the frequency divider will divide the output signal of the VCO by N to get back to the reference frequency [1].

1.2.2 Fractional-N frequency synthesizer:

We saw that in the Integer-N Frequency synthesizer is that the output frequency of the VCO is always an integer multiple of the reference frequency, which means the resolution frequency equal to the reference frequency [2]. In case of fine resolution is needed, a lower reference frequency will be needed, or we can get an output frequency from the VCO that equal to a multiple of integer plus fraction of the reference frequency. In fractional-N synthesizer the output frequency of the VCO is not only an integer multiple of the reference frequency, but also a fractional part will be add to this integer to increase the resolution of the synthesizer without reducing the reference frequency. In this case we can get:

\[ f_o = (N + A/Q) \times f_r \quad (2) \]
Since the divider can only divide by an integer, to obtain a fractional ratio, the divider will divide by \( N+1 \) for A reference periods and by \( N \) for Q-A reference periods, and the average division ratio for the whole periods will be \( A/Q \) as indicated in equation (2) [2]. By this method we can get a fractional divider from an integer divider that will increase the resolution of the frequency synthesizer.

1.2.3 Proposed frequency synthesizer for DVB-H system:

Figure 1.3 shows the system diagram of the proposed frequency synthesizer our lab working on.

![Diagram](image)

**Figure 1.3: Proposed frequency synthesizer system diagram**

This frequency synthesizer will be designed for cell phone uses. The first two blocks of this system are Phase/Frequency detector (PFD) and Charge Pump (CP). The job of these two blocks is to measure the phase and frequency error between the divider signal and the reference signal and produce an output voltage that will control the output frequency signal of the VCO. The design and testing of these two blocks will be covered in details in the next chapter. The next block will be the loop filter. This block will help
the system to stable in a short time which will help to increase the frequency synthesizer speed to reach a lock. The main part of the system is the VCO, as we can see from the figure the output frequencies of the VCO will be able to cover both UHF band (470-867 MHz) and L-Band (1.65-2.5 GHz). The last two blocks will be the multi-modulus fractional-N divider, which has two division ratios N=2 and N+1=3 that will enable the system to produce a large frequency range between 400 MHz and 2.5 GHz. The other block is the ΣΔ Quantizer, which shapes the fractional noise quantization out of the PLL band. The reference frequency of the system CLKREF= 40MHz with channel bandwidth equal to 35 KHz.

The next chapters will cover the design and testing of the Phase/Frequency Detector and Charge Pump and the simulation of the combined system PFD/CP.
CHAPTER 2

PHASE AND FREQUENCY DETECTORS AND CHARGE PUMP

2.1 Phase Frequency Detector:

Phase frequency detector is one of the important parts in PLL circuits. PFD (Phase Frequency Detector) is a circuit that measures the phase and frequency difference between two signals, i.e. the signal that comes from the VCO and the reference signal. PFD has two outputs UP and DOWN which are signaled according to the phase and frequency difference of the input signals. Fig. 2.1 shows a PFD with its inputs and outputs.

![Figure 2.1: Phase Frequency Detector](image)

Figure 2.1: Phase Frequency Detector
The output signals of the PFD are fed to the charge pump. The output voltage of the charge pump controls the output frequency of the VCO, so with a change happens at the input of the CP the output voltage will change which will change the output frequency of the VCO [3]. In this case the sensitivity of the phase and frequency difference detection of the PFD is very crucial. Sensitivity of the PFD means the smallest difference the PFD can detect and produce UP or DOWN signals that will affect the charge pump, this lead to the conclusion that the higher the sensitivity the better the PFD. One of the disadvantages that PFD suffers is dead-zone. Dead-zone is a small difference in the phase of the inputs that a PFD will not be able to detect. Dead zone is due to the delay time of the logic components and rest of the feedback path of the flip flops.

Figure 2.2, shows a detailed design for PFD with input/output signals transaction. A simple design of PFD consists of two D flip flops and AND gate. As the figure shows the D input of the flip-flops is connected to VDD and the input signals (CLKREF, CLKVCO) are applied to the clock input. When one of the clocks change to high, this flip-flop will charged and change its output to high. The AND gate is for preventing both flip-flop to be high at the same time. As we can see the inputs of the AND gate are the both Up and DOWN signal from both flip-flops, and the output of the AND gate is connected to the reset input of the flip-flops. As soon as both outputs (UP, DOWN) are high the AND gate will generate a high signal that will reset both flip-flops avoiding the situation of both high at the same time. The signal transaction in figure 3.2 gives an example of CLKREF leading CLKVCO.
From the transaction, once CLKREF goes high it will charge the flip-flop and resulting in changing UP signal to high. when CLKVCO becomes high it will result in changing DOWN signal to high, this will lead to have both output at high which will let the AND gate to signal the reset output and reset both flip-flops driving both outputs to low. Since CLKREF is leading in figure 2.2, we can notice that only UP signal is signaling when CLKREF change to high. in case CLKVCO is leading the opposite is true, which means DOWN signal will be high when CLKVCO change to high.
2.2 Dead Zone:

As we mentioned before, dead-zone is due to small phase error. When the phase difference between PFD’s input signals, the output signals of the PFD will not be proportional to this error [4]. The reason of this problem is the delay time of the internal components of the flip-flop and the reset time that need s the AND gate to reset both flip-flops [3]. Figure 2.3 illustrates the dead zone problem. When the two clocks are very close to each other (small phase error), due to the delay time the reset delay, the output signals UP and DOWN will not be able to charge and no output will signal leading to losing this small difference.

![Figure 2.3: Dead Zone](Image)

Figure 2.4 illustrates the output voltage of the charge pump vs. the phase error measured by the PDF. Figure 2.4a illustrates the relation in no dead zone PDFs, while figure 2.4b illustrates the relation in the presence of a dead zone. We can see that in a dead zone PFDs the relation become nonlinear around zero. This is due to inability to
detect the phase error in this region. Plenty of solution has been done for this problem some of them reduce the delay time in the internal components of the PFDs, other solution eliminate the reset path by implementing new reset techniques that will not create a delay and produce a high speed PFDs.

Figure 2.4: Phase Error vs. Output Voltage
(a) No Dead Zone (b) Dead Zone

2.3 Proposed PFD Design and Simulation:

In the PFD design I worked on two designs using two different circuits topology. The first design is the traditional PFD architecture.

2.3.1 Type 1 PFD (Traditional PFD architecture):

The design consists of two flip-flops and a NOR gate to provide a reset path when both outputs go high at the same time as shown in figure 2.2.. Due to the reset path this design suffers from large dead zone. Figure 2.5 illustrates the system diagram of the first design which we will call type I PFD. As we can see from the figure, this design has two
D flip-flops and NAND gate. The schematic design of the D flip-flop is shown in figure 2.6 [6]. The schematic design of the circuit has been done using TSMC 0.18µm technology with 1.8v as a supply voltage.

Figure 2.5: Block Diagram of Traditional PFD architecture
The D flip-flop circuit operates as follow. When both CLK and RST are low, node 1 will be connected to VDD through M1, M6. At the raising edge CLK, the node 2 will be connected to ground through M3, M4. Since node 1 is connected to VDD that will turn off M2 keeping node 2 from charging high. as RST signal charges up, node 1 will be connected to the ground through M5, which will lead to pull up node 2 and it will become high due to switching M2 on. Transistor M1 job is to prevent a short circuit in the M0, M1amd M5 path. When CLK is low and RST is high a large current will low this path so M1 is placed there to prevent this current and lower the power consumption of the D flip-
Since we are getting flipped value of Q, an inverter has been added at the end of the circuit to flip the value and get a correct value of Q. Both flip-flops have the same design, one of them will control the UP output of the PDF and the other will control the DOWN output. The direct output from node 2 of both flip-flop are connected to a NOR gate, and the output go this NOR gate will be connected to the RST input of the flip-flops to enable reset when both output go high at the same time. Figure 2.7 shows a schematic design of the NOR gate.

![Figure 2.7: CMOS NOR gate](image)

Due to the NOR reset path, the time needed to charge the NOR gate and reset both flip-flops will be added to the reset delay time in the internal components of the flip-flops and produce a large dead zone. Figure 2.8 illustrates the large dead zone for this design. We can see that the NOR gate needs around 80 Pico seconds to charge up and be able to reset both flip-flops, and because of this delay both outputs will be high at the
same time, therefore they will switch on both transistors in the charge pump preventing it from charging the output up or down according to this phase error.

Figure 2.8: Dead Zone caused by NOR reset delay

Figure 2.9 shows a longer simulation done on type 1 PFD. The input CLK frequency is 40 MHz with CLKOUT leading CLKREF by 2ns; this will result in having UP signal as we can see from the graph. This PFD were able to operate at much higher frequency, but for our PLL design 40 MHz is the highest frequency the PFD will operate at. The power consumption of the type 1 PFD is 66.9 µW @ 40 MHz which is a high value and that is due to the reset signal that consumes some power to charge up and reset both flip-flops.
Figure 2.9: simulation of the Type I PFD with 2ns delay

Because of the high power consumption and the large dead zone of type I PFD, some modification has been done with that design that reduced the power consumption to 9.81 µW @ 40 MHz and the size of the dead zone to 40 Pico second. The modification on type I PFD has enabled us to remove the reset path and reduce the delay time that causing the dead zone problem. As shown in figure 2.10 the D flip-flop schematic design has few changes from the original type 1 PFD, this changes allowed getting ride of the reste path and applying the CLK signal immediately to the RST input for each flip-flop to reset them as soon as both flip-flops have high output at the same time. The modified D flip-flop in figure 2.10 operates exactly like type 1 PDF [6]. Figure 2.11 shows the modified PFD.
Figure 2.10: Modified D flip-flop

Figure 2.11: Modified Type 1 PFD
The simulation of the modified type 1 PFD (figures 2.12 and 2.13) shows that the dead zone of this design is just 40 ps, which makes it a better candidate for our system than the traditional type 1 PFD, beside the lower power consumption make this design more suitable for cell phones that use a limited power supply. Figure 2.13 shows that at 40 ps the Down signal become low enough that it will not switch on the pull down transistor in the charge pump.

Figure 2.12: Modified Type 1 PFD simulation at 40 MHz and no phase error
Smaller dead zone and lower power consumption PFD is achievable, this lead us to the type 2 PFD that will introduce in the next section.

2.3.2 Type II PFD:

To be able to achieve a higher speed PFD than the one we just discuss, another design is being proposed in this section. This design eliminates the reset path, which will lead to a smaller time delay. To be able to detect the phase error and has a fast reset, this design depends on detecting the raising and falling edge of the input signals to do the job.
Figure 2.14: Schematic design of Type 2 PDF.

Figure 2.14 shows the schematic design of the Type II PFD. As we can see instead of having feedback reset path, both CLK signals will reset both outputs as soon as they are high at the same time [3]. This circuit operates as follow, when CLKOUT raises both node 1 and 2 will become low. As CLKREF goes up node 2 changed from low to high, same as when CLKOUT charges to high node 1 changed from low to high. The other components in the design are NAND gate and inverter [3].

Figure 2.15 and figure 2.26 show the simulation result of this PFD. we can see from figure 2.15 that the dead zone of this design is only 15ps which is 0.0012π in radian
which is almost zero dead zone. The power consumption of this design is only 6.228µW @ 40MHz.

Figure 2.15: Dead zone in Type 2 PFD

Figure 2.16 shows a simulation of this PFD at 40MHz and CLKOUT leading CLKREF by 750ps; this will result in having a UP signal as shown in the figure, while the DOWN signal will be low all the time.
Figure 2.16: Type 2 PFD Simulation with 750ps (45 degree) phase error

With these results, Type 2 PFD is the best candidate for our PLL design since it has low power consumption and almost zero dead zone. Next, I will cover the charge pump design.

### 2.2 Charge Pump:

Charge pump is the circuit that translates the UP and DOWN signals from the PFD to control voltage that will control the VCO. As shown in figure 2.17, charge pump consist of two switched current sources driving a capacitance load [7]. Charge pump is switched on and off by the PFD output signals UP and DOWN. This will result in three control states for the charge pump shown in Table 2.1.
Table 2.1: Three state of the Charge Pump

<table>
<thead>
<tr>
<th>UP</th>
<th>DOWN</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>IB deposit current in CL raising Vo</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>IB sink current from CL reducing Vo</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>Both switches are off and no Vo changes</td>
</tr>
</tbody>
</table>

2.2.1 Proposed Charge Pump:

Figure 2.18 shows the schematic design of the charge pump. The design consists of two switched current sources that provide 500\(\mu\)A each and a 10pF load capacitor for the simulation purpose. When the up signal is high transistor M11 will switch on allowing current to flow through and charging the load capacitor up. On the other hand, when DOWN in high transistor M12 is on and it will discharge the load capacitor. The power consumption of this design according to the operating state is shown in table 2.2.
Figure 2.18: Schematic design of the purposed charge pump

<table>
<thead>
<tr>
<th>UP</th>
<th>DOWN</th>
<th>Power Consumption</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>0.91mW</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>-0.912mW</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>-200nW</td>
</tr>
</tbody>
</table>

Table 2.2: Power consumption of the charge pump
2.2.3 CP Simulation Result:

Figure 2.19 and 2.20 show the simulation result of charging-up and charging-down. The frequency of this simulation is 500 MHz with 1.8v supply voltage.

Figure 2.19: CP Charging-up

Figure 2.20: CP Charging-down
CHAPTER 3

PFD/CP SIMULATION RESULTS

3.1 Simulation setup and result:

This chapter will cover all the simulation result of the type 2 PFD and the charge pump. The complete system is shown in figure 3.1. The output of the PFD is connected to the input switched of the charge pump, and the capacitance load of the charge pump is 10pF. The operating frequency of this simulation is 40MHz with 1.8v as supply voltage.

Figure 3.1: PFD/CP system test pinch
Figure 3.2 shows the simulation result of the full system when CLKOUT leading that of CLKREF by 750ps, which resulting triggering the UP signal in PFD and that will switch the UP transistor in the CP charging up the load capacitor.

![Figure 3.2: PFD/CP simulation with 750ps (45 degree) phase error](image)

Figure 3.3 shows the noise simulation of the system. The figure contains the output noise and the phase noise of the system. The output noise of the system is -165dB and the Phase noise is -132dBc/Hz. The main contributor of the noise is the charge pump; since it uses a high current the charge pump introduces high noise for the system. CP in general consider as the most power consumption and noise producer in PLL system.
3.2 Dead Zone compassion:

This section shows the performance of the system using Type I PFD and Type II PFD. Both simulations were done using 40MHz operating frequency with 1.8v supply voltage.

Figure 3.4 shows the comparison between the dead zone sizes between both PFDs. We can see from figure 3.4a that the dead zone of the Type I PFD is 40ps, while from figure 3.4b the dead zone size of Type II PFD is 20ps, which is 50% less than the Type I PFD.
Figure 3.4: Dead Zone size of (a) Type I and (b) Type II PFDs

3.3 Monte Carlo Simulation:

This section shows the results of the Monte Carlo simulation. Monte Carlo simulation involves process and mismatching between transistors and other components in the design, beside it consider the effect of temperature on the performance of the system.

Figure 3.5 shows the result of simulating the system in 40MHz with no phase error. We can see from the result that the system maintains its performance as designed for most of the iterations except few where it starts to charge down. The problem here is that because of the mismatch the output current from the PFD becomes high enough to be able to switch on the charge pump transistors allowing them to pass current through them.
Figure 3.5: Monte Carlo simulation for PFD/CP

Figure 3.6 shows the deviation of the current usage of the system. We can see that the current in all iteration stay in the premises of 1.2 mA.
Figure 3.6: Monte Carlo Simulation result of the current usage
APPENDIX A

DESIGN PROCESS OF THE D-LATCH

FOR TYPE I PFD
In this section I will cover the design process of the D-latch used in the design of the Type I PFD.

Starting from the current consumption budget of the D-latch which is 40µA for our proposed frequency synthesizer, I divided this value between the three branches of the D-latch. Each branch will have 40/3 = 13.3µA flowing through it.

![Figure A.1: D-latch of the Type I PFD](image)

Using the value of this current I calculate the width of each transistor for each branch. The length of all these transistors is 180nm, so by changing the width of each transistor I can control the current value that flows through it. Since all transistors operate in the active region, the equations I used to determine each transistor width were:

\[
I_n = \mu_n \cdot C_{ox} \cdot (W/L) \cdot (V_{gs} - V_{tn})^2 \quad \text{for NMOS} \quad (3)
\]

\[
I_p = \mu_p \cdot C_{ox} \cdot (W/L) \cdot (V_{gs} - V_{tp})^2 \quad \text{for PMOS} \quad (4)
\]
From the simulation software (Cadence) I got the values of $V_{gs}$ for NMOS and PMOS and plugged them in equation (3) and (4) respectively.

The same design process was applied to design the modified D-Latch for the modified Type I PFD and Type II PFD to get the width of the transistor that used in these designs.
LIST OF REFERENCES


