EFFICIENT RADIO FREQUENCY POWER AMPLIFIERS FOR WIRELESS COMMUNICATIONS

DISSERTATION

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By

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* * * * *

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ABSTRACT

With the rapid growth of personal wireless communication systems, there has been increasing demand for radio frequency (RF) power amplifiers (PAs) to be power-efficient so as to extend terminal’s battery/talk time and achieve low form-factor in mobile, as well as reduce the cooling and electrical power cost in base stations.

This dissertation primarily addresses three types of promising high efficiency PAs namely class E, class F and Doherty amplifier. The traditional designs of switching mode class E PAs have been relying on a priori classical design equations, which are challenged by non-ideal issues such as the finite RF choke inductance and limited Q factor of load network. Altogether this could make the analysis of class E PAs enormously complex and lead to analytically intractable situation. In this work, the design of class E pHEMT PA is based on the ADS load-pull simulations, which permits an iterative search for the nominal impedance values that maximize efficiency and output power under various working conditions of the active transistor. Simulation results also help to investigate the principle of class E PA’s non-linear operation.

An important contribution of this dissertation is the proposed multi-harmonic real-time active load-pull (RT-ALP) based on the large signal network analyzer (LSNA), for designing high efficiency class F PAs. It bypasses the large-signal PA transistor models
needed by simulations, which are often custom-made with limited accuracy. Conventional experimental load-pull systems with passive tuners are typically time-consuming when sweeping a large area of the Smith chart. Moreover the attainable reflection coefficient magnitude is limited by the passive tuner losses. Active load-pull (ALP) systems relying on the closed-loop architecture improve the reflection coefficient range, but are subject to potential stability problems. In addition, the time needed for finding the optimal load for each harmonic for non-linear PA design, still remains significant as both the amplitude and phase must be swept under computer control.

For the proposed RT-ALP technique, the applied real-time tunings at second and third harmonic frequencies enable to quickly synthesize a wide range of harmonic load reflection coefficients without stability issue due to open-loop structure. Fast acquisition of reliable large-signal data is available to generate the RF dynamic loadlines, PAE and power contour plots for guiding the design of non-linear power amplifiers. Using this RT-ALP system, GaN device is chosen to explore the impact of the multi-harmonic loading conditions on non-linear class F PA, demonstrating a power added efficiency of 81% at 2 GHz by tuning up to the third harmonic. A pHEMT PA is designed and constructed with matching networks based on the optimal impedances predicted by the RT-ALP technique. Its measurement result of 68.5% PAE at 2 GHz has a good agreement (3% difference) with the RT-ALP prediction, further demonstrating the efficacy and reliability of the proposed multi-harmonic RT-ALP for the interactive design of power efficient PAs.

Doherty amplifier is known to be another promising high-efficiency PA solution but there is a need to reduce circuitry size for integration and improve linearity for emerging high data rate wireless standards such as WiMAX. The design of integrated Doherty PAs
in low-cost CMOS processes, however, still remains challenging and this is aggravated by the decreasing supply and breakdown voltage, as well as the substrate coupling losses in the scaling-down deep submicron CMOS processes.

This dissertation presents an integrated CMOS Doherty PA at 3.5 GHz WiMAX band, using the standard 0.18μm TSMC CMOS process. To address the issues of low breakdown voltage, cascode transistors are chosen to help achieve high efficiency. Lumped matching components are used to replace the quarter-wave transmission line for circuitry miniature. The design is implemented with the novel GSML methodology for reliable parasitics control and passes all the DRC and LVS checks. Furthermore compact integrated diode linearizers are utilized and demonstrate linearity improvement up to 5.75 dBC for the Doherty PA, which achieves a peak output power of 24.5 dBm and power added efficiency as high as 43% at 3.5 GHz.
Dedicated to my dear parents and family...
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**FIELDS OF STUDY**

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CHAPTER 1

INTRODUCTION

1.1 The Significance of Efficient RF Power Amplifiers

During last decade the phenomenal growth of personal wireless communications has made remarkable impacts to modern life. Nowadays billions of people use mobile cellular phones to communicate everyday with the coverage penetrating to massive areas around the whole world [1.1] [1.2]. Wireless data networking infrastructures are widely being deployed into public zones to offer wireless computing and internet services [1.3] [1.4] through laptops. Accordingly the revolution of communications has also been pushing the evolution of wireless systems and innovation of the internal radio frequency (RF) circuits, including the RF power amplifier (PA).

RF power amplifier is a circuit for converting DC supply power into a significant amount of RF output power [1.5] [1.6]. As a critical module in the transmit chain, it is typically the final stage of a wireless transmitter to drive the antenna. The modulated RF signal is amplified by the PA to a nominal power level and then sent through antenna to radiate for propagation.
RF power amplifiers are usually the most power-hungry building blocks [1.7] in the transceivers (i.e. transmitter plus receiver) of wireless mobile terminals. For instance cellular handsets PA can consume more than 70% of the DC battery power during transmit period [1.8]. There is increasing demand for highly efficient RF power amplifiers to meet the ever-growing need for power saving, compact and low cost solutions.

Indeed the higher the DC to RF conversion efficiency, the less amount of electrical charge is drawn from the battery for PA to transmit the same amount of RF power. That helps to considerably prolong the battery operation time to satisfy end users.

High-efficiency RF PA also reduces the portion of battery power transformed into heat. The result is less stress for the active transistors inside PA and more importantly decreasing heat sink metal and its associated cost. It is worth noting that the dimension of wireless mobile terminals has been shrinking for user convenience in recent years as demonstrated in the handset example in Fig. 1.1. The state-of-the-art form factor for

![Fig. 1.1 Evolution of cellular handsets: dimensions shrinking down.](Adapted from [1.2], courtesy of Microwave Journal)
handset PA modules has decreased to $5 \times 5$ mm$^2$. A good thermal dissipation performance benefited from high-efficiency PA is definitely an important factor to continue this downward trend. Moreover emerging popular features (e.g. MP3, camera, GPS and FM radio) are being progressively added to new generation of mobile terminals. However they inevitably bring additional power consumption and burden the battery. High-efficiency power amplifiers are able to save more power during transmit and leave some margin in the power management budget for these new features. Likewise for cellular base stations, high efficiency PA is the key as well to save operation supply power, lower down cooling cost and alleviate problems due to thermal stress on active devices.

1.2 Choices of Efficient Power Amplifiers

The ways of pursuing RF power amplifiers with high efficiency, are related to the modulation schemes of communication systems. Mainly there are two existing categories of modulation schemes for personal wireless applications: constant-envelope modulation and non-constant envelope modulation.

The constant-envelope modulation schemes have been widely accepted by systems such as Globe System for Mobile Communications (GSM), Bluetooth and RFID. Linearity requirements of a PA are less stringent due to the usage of constant-envelope signals, e.g. GMSK (in GSM). In such a case, a non-linear PA with high efficiency can be considered: it maintains the modulated information while efficiently utilizing the limited battery power resource. In contrast to a linear PA (e.g. class A PA), where output signal amplitude presumably to be linearly controlled by the input signal amplitude,
non-linear PA’s output signal is controlled by the phase and frequency information of its modulated input signal.

With its active transistor working as on-off switch, class E [1.9] power amplifier is a type of nonlinear PA capable of achieving high efficiency at RF frequency. In a class E PA, the transistor’s current and voltage waveforms are shaped by the parallel capacitance and load network to minimize the overlap, resulting in less power dissipation of the transistor itself and boosting up the efficiency of the amplifier. For optimal operation the drain voltage decreases to zero and has zero slope just as the transistor turns on. Hence the loss from drain capacitance discharge is avoided as well leading the theoretical drain efficiency to be 100%.

Class F [1.5] power amplifier is another type of promising non-linear PA for realizing high efficiency. It requires harmonic terminations in the transistor output network to shape the device’s drain voltage and current waveform, insuring the condition in which the transistor’s current and voltage do not become high simultaneously. Theoretically the ideal waveforms of drain voltage and current are non-overlapping square wave and half sinusoidal wave respectively, achieving 100% as maximum efficiency. It is important to note that highly non-linear class E or class F power amplifiers are feasible for linear amplification of non-constant envelope modulated signals, with the aid of special techniques such as envelope elimination and restoration (EER) [1.6] as explained in Chapter 2.

On the other hand, the non-constant envelope modulation applies to growing wireless systems such as wideband Code Division Multiple Access (WCDMA) and Worldwide Interoperability for Microwave Access (WiMAX). The used shaped-pulse modulations
(e.g. QAM, QPSK) or multiple carriers (OFDM) allow high data rate but occupy wider spectrum bandwidth and need highly linear components, particularly power amplifiers to transmit RF signals with time-varying envelope and phase. In such case a linear PA (typically controlled current sources) is required to lower the inter-modulation and adjacent channel interference of amplified signals. Oftentimes it operates at back-off for adequate linearity. Staying away from its peak input/output power in most of the time, however, wastes the supplied DC bias power designed for the maximum output capability and causes low PA efficiency.

Up to now various techniques, such as Doherty amplifier and dynamic bias [1.5], have been proposed for improving efficiency of linear PAs. The former technique utilizes the load-pulling effect between two PAs and the latter one brings in dynamically controlled bias circuitry according to input power level. The key idea behind is to only supply the RF PA with just sufficient DC power depending on the input signal’s fluctuating envelope. Details of these two techniques will be described in Chapter 2.

1.3 Motivation and Objectives

Traditional designs of class E power amplifiers have been relying on a priori classical design equations. Designers often have to face non-ideal and practical issues such as finite RF choke inductance, the limited Q factor of load network and transistor’s voltage dependent drain capacitance, etc. All these complicated conditions together could make the analysis of class E operation enormously complex and lead to analytically intractable situation [1.10].
One objective of this work is to design a class E pHEMT power amplifier based on the load-pull simulations, which permit iterative search for the nominal impedance values that maximize efficiency and output power. Simulation results will also help to reveal the principle of class E PA’s non-linear operation.

Designing a non-linear class E or F PA with load-pull simulation is often challenged by the availability of custom-made large-signal transistor model and its accuracy. Conventional passive or active load-pull [1.11] investigates the optimal load conditions with the power transistor under real-world environment, but it is a time-consuming process especially in non-linear PA design where both the amplitude and phase must be swept for each harmonic to find optimal terminations.

A main goal of this dissertation is to propose a multi-harmonic real-time active load-pull (RT-ALP) for designing high efficiency power amplifiers such as class F. This technique bypasses the limit of transistor model in simulations. It is also able to explore the complete Smith chart avoiding the losses of mechanical tuners as in passive load-pull. With the applied multi-harmonic real-time tunings, the RT-ALP is expected to enable fast sweepings of impedances at both fundamental (f₀) and harmonic (2f₀, 3f₀) frequencies, so as to quickly determine the optimal load terminations and shorten the PA design cycle.

Doherty amplifier is known to be a promising high-efficiency PA solution as noted in previous section. It has been accepted by base station PA designs but needs circuitry size adaptation for integrated implementations. Meanwhile the emerging standards of personal wireless connectivity (e.g. WiMAX) call for battery-efficient power amplifiers in low-cost technology such as CMOS. However, the designs of fully integrated PA in CMOS still remain challenging, which is aggravated by the reduced supply voltage due to
scaling-down feature and on-chip passive losses due to the lossy substrate in deep submicron CMOS processes.

The third objective of this dissertation is to design an integrated CMOS Doherty PA at 3.5 GHz WiMAX band, using the standard 0.18 μm TSMC CMOS process. A Doherty configuration with cascode transistors is chosen to achieve high efficiency overcoming the issues of low breakdown and supply voltage. Lumped matching components will replace the quarter-wave transmission line for circuitry miniature. Furthermore the added integrated diode linearizer needs to demonstrate linearity improvement for the Doherty PA.

1.4 Dissertation Organization

The rest of this dissertation is organized as follows. In Chapter 2 a brief overview of RF power amplifiers is presented. The classification of RF PAs is introduced with emphasis on the high-efficiency class E and class F. The conventional load-pulls for PA design are discussed. PA efficiency enhancement and linearization techniques are explained as well. Chapter 3 focuses on the design of a pHEMT class E PA at 2.4GHz, with the aid of ADS load-pull simulations to find the nominal load impedances that maximize PA efficiency or output power. The principle of class E PA’s non-linear operation and non-ideal practical design issues are also investigated. In Chapter 4, a multi-harmonic real-time active load-pull (RT-ALP) system based on the large signal network analyzer (LSNA) is proposed for the design of non-linear RF power amplifiers (PA). The real-time tuning approach is described here for quick searching of the optimal
impedances not only at the fundamental but higher harmonic frequencies with a supportive theory provided. The RT-ALP technique is demonstrated on a class F GaN HEMT device with high PA efficiency achieved. A prototype PA with pHEMT is designed and constructed as well. Its measurement results are presented further verifying reliability of the multi-harmonic RT-ALP. In Chapter 5, the challenges of designing RF power amplifiers in low-cost CMOS technology are addressed. A CMOS Doherty PA design using standard 0.18 μm TSMC process is proposed for the 3.5 GHz WiMAX band. Simulation results and final layout are presented. The novel Doherty configuration with both cascode transistors and integrated diode linearizers achieves high efficiency and output power with improved linearity. Chapter 6 concludes this dissertation with a summary of the results obtained.
CHAPTER 2

BACKGROUND OF RF POWER AMPLIFIERS

2.1 Power Amplifier Classes of Operation

A power amplifier’s efficiency is influenced by its classes of operation, which generally include class A, B, AB, C, D, E and F. The conventional class A, B, AB and C belong to the basic category while class D, E and F engage with more complex concepts.

As shown in Fig. 2.1, the basic PA configuration consists of power transistor, RF choke (L₁), DC block (C₁), output filter and the load. DC power supply, gate (or base)

![Conceptual schematic for class A, B, AB and C PA.](image)

Fig. 2.1 Conceptual schematic for class A, B, AB and C PA.
bias and RF input drive are also provided to the PA.

The major factor to differentiate class A, B, AB and C is the conduction angle ($\theta$) of a RF transistor’s drain (or collector) current. For class A, the quiescent gate bias is set large enough above threshold voltage, so that the drain current remains greater than zero during any signal period at the PA’s working frequency. As can be seen in Fig. 2.2(a), conduction angle of a class A is $2\pi$. The PA transistor completely operates in the active region and acts as a current source controlled by the input signal drive [2.1] [2.2]. The resulting ideal drain voltage and drain current are both sinusoidal, intrinsically with absence of harmonics and considered as “pure linear”. In general the RF output power is defined by:

$$P_{out} = \left(\frac{V_{om}}{\sqrt{2}}\right)^2 \frac{\pi}{R} = \frac{(V_{om})^2}{2R}$$

where $V_{om}$ represents the amplitude of drain voltage waveform at fundamental frequency ($f_0$) and $R$ for load resistance. With full voltage swing, $V_{om}$ is permitted to reach the supply voltage $V_{dd}$ as maximum (knee voltage neglected), which corresponds to the highest output power ($P_{out,max} = 0.5V_{dd}^2/R$) for class A PA.

The two common DC-to-RF efficiency metrics for class A (and other classes) PAs are drain efficiency ($\eta$) and power added efficiency (PAE):

$$\eta = \frac{P_{out}}{P_{DC}} \quad (2.2) \quad \text{PAE} = \frac{P_{out} - P_m}{P_{DC}} \quad (2.3)$$

where $P_m$ represent the RF input drive power and $P_{DC}$ for consumed DC supply power. The maximum drain efficiency of an ideal class A PA turns out to be 50%.

As for class B, the PA transistor is biased right at the threshold point, which means
the transistor only active during half of a signal period. It leads the conduction angle to be \( \pi \) and the drain current to be half-sinewave as illustrated in Fig. 2.2(b).

Fig. 2.2 Ideal voltage and current waveforms for (a) Class A \((\theta = 2\pi)\) (b) Class B \((\theta = \pi)\) (c) Class C \((0 < \theta < \pi)\).

With the bias reducing below the threshold voltage, the transistor only generates drain current during a smaller fraction of one signal period, reducing the generated output power. At the same time, \( \theta \) becomes less than \( \pi \) and the PA operates as class C (Fig. 2.2
The intermediate bias condition between class A and class B namely class AB makes $\theta$ to be between $\pi$ and $2\pi$. For class AB the drain efficiency ($\eta$) can be formulated as a function of the conduction angle [2.2]:

$$\eta = \frac{\theta - \sin \theta}{4\sin(\frac{\theta}{2}) - 2\theta \cos(\frac{\theta}{2})} \tag{2.4}$$

Class B can be used in a push-pull topology to combine two drain-currents together forming a fully sinusoidal wave. Class AB is a typical compromise to offer efficiency higher than the “pure linear” class A, but with some tolerable PA non-linearities [2.2]. In terms of efficiency comparison (Table 2.1), class C provides higher efficiency than class A, B and AB. In fact $\eta$ rises toward 100 percent as the conduction angle approaching zero, however, the amount of output power drops down to zero for $\theta = 0$ as well. So a realistic $\theta$ for class C is to set around $150^\circ$ rather than around zero degree [2.1]. In practice the maximum efficiency in Table 2.1 will be degraded by the transistor parasitics, knee voltage and load reactance.

<table>
<thead>
<tr>
<th>PA Classes</th>
<th>A</th>
<th>B</th>
<th>AB</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conduction Angle ($\theta$)</td>
<td>$2\pi$</td>
<td>$\pi$</td>
<td>$\pi-2\pi$</td>
<td>$0 \sim \pi$</td>
</tr>
<tr>
<td>Maximum Drain Efficiency (%)</td>
<td>50</td>
<td>78.5</td>
<td>50-78.5</td>
<td>100</td>
</tr>
<tr>
<td>Output Power Capability</td>
<td>large</td>
<td>medium</td>
<td>medium</td>
<td>low</td>
</tr>
</tbody>
</table>

Table 2.1 Efficiency comparison of class A, B, AB and C.

Note that filters are usually used to suppress the harmonics originated from the non-sinusoidal drain currents of class AB, B or C, so as to create the sinusoidal output voltage. For instance the ideal shunt $L_0-C_0$ tank in Fig. 2.1 stands for the output filter shorting.
harmonics to ground. The resistive load (R) is often transformed from the 50 Ohm reference impedance by the Output Matching Network (OMN). Typically the output filter is incorporated into the OMN for circuit simplicity.

Class D is a switching-mode PA with two transistor switches driven 180 degree out-of-phase and one series resonator at the load. Its ideal drain voltage and current are non-overlapping square wave and half sinusoidal wave respectively, similar to class F and capable of reaching 100% for maximum $\eta$. However, class D has not been popular at RF frequencies because of the substantial loss from the output capacitance at high switching speed. Reported work achieved operation at 0.9 GHz [2.3], but so far class D PAs still stay as the mainstream of low frequency audio application such as Hi-Fi audio.

Class E is a switching-mode non-linear PA capable of achieving 100% drain efficiency at the peak output power (an advantage over class C). Class F is another type of non-linear PA involved with substantial harmonic tunings with maximum efficiency up to 100% as well. The common attribute of class E and class F is minimizing the overlap between a PA transistor’s drain voltage and current to suppress the power consumption of the transistor itself and boost up the PA efficiency. Details of class E and F are provided in next section.

2.2 High Efficiency Class E and Class F PA

2.2.1 Class E PA

The concept of class E power amplifier was proposed by Sokal [2.4]. As shown in Fig. 2.3, the class E PA consists of an active transistor in switching operation and a passive load network. The load network has a series resonant circuit and a capacitor
in parallel with the transistor. The drain (collector) voltage waveform is determined by the switching action and the transient response of the load network. This results in Fig. 2.4 a switching voltage that drops to zero and has zero slope just as the transistor switch turns on, i.e., zero-voltage-switching (ZVS). So the switching loss related to drain (collector) capacitance discharge is removed and there is no overlapping between drain voltage and drain current, ideally achieving a 100 percent drain efficiency.
Table 2.2 lists the reported results of class E PAs, implemented in different semiconductor technologies, such as CMOS, GaAs FET, pHEMT and GaAs HBT processes. Class E PAs possess advantages such as circuit simplicity and controllable output [2.13], however, it requires the active transistor to endure high peak voltage up to 3.56 V_{dd}, which is particularly not favorable to the deep submicron CMOS process with low breakdown voltage. Further analysis and equation derivations of class E PA will be given in the following Chapter 3 and Appendix A.

### 2.2.2 Class F PA

The class F power amplifier is another type of high efficiency non-linear PA. It requires harmonic terminations in the transistor output network to shape the drain (collector) voltage waveform. Typically only odd harmonics exist in the drain (collector) voltage to approximate a square wave; only even harmonics exist in the drain (collector) current to approximate a half sinusoidal wave. The overlap between drain voltage and

<table>
<thead>
<tr>
<th>Ref. #</th>
<th>Class</th>
<th>Technology</th>
<th>Frequency</th>
<th>Pout</th>
<th>PAE</th>
<th>Gain</th>
</tr>
</thead>
<tbody>
<tr>
<td>[2.5]</td>
<td>E</td>
<td>pHEMT</td>
<td>10.6 GHz</td>
<td>24dBm</td>
<td>63%</td>
<td>10 dB</td>
</tr>
<tr>
<td>[2.6]</td>
<td>E</td>
<td>pHEMT</td>
<td>3.25 GHz</td>
<td>23 dBm</td>
<td>70%</td>
<td>NA</td>
</tr>
<tr>
<td>[2.7]</td>
<td>E</td>
<td>GaAs HBT</td>
<td>0.8 GHz</td>
<td>21.3 dBm</td>
<td>74%</td>
<td>13 dB</td>
</tr>
<tr>
<td>[2.8]</td>
<td>E (2stages)</td>
<td>GaAs HBT</td>
<td>1.95 GHz</td>
<td>27 dBm</td>
<td>62.5%</td>
<td>22 dB</td>
</tr>
<tr>
<td>[2.9]</td>
<td>E</td>
<td>GaAs FET</td>
<td>0.5 GHz</td>
<td>27.4 dBm</td>
<td>80%</td>
<td>15.3 dB</td>
</tr>
<tr>
<td>[2.10]</td>
<td>E</td>
<td>GaAs FET</td>
<td>5 GHz</td>
<td>27.9 dBm</td>
<td>72%</td>
<td>9.8 dB</td>
</tr>
<tr>
<td>[2.11]</td>
<td>E</td>
<td>0.25μm CMOS</td>
<td>0.9 GHz</td>
<td>29.5 dBm</td>
<td>41%</td>
<td>NA</td>
</tr>
<tr>
<td>[2.12]</td>
<td>E (2stages)</td>
<td>0.18μm CMOS</td>
<td>2.4 GHz</td>
<td>21.3 dBm</td>
<td>55%</td>
<td>14.3 dB</td>
</tr>
</tbody>
</table>

Table 2.2 Class E PAs implemented in different technologies.
current is reduced, thus minimizing transistor’s own power consumption to enhance the DC-to-RF efficiency of the whole PA [2.14]. The schematic of a basic Class F power amplifier is shown in Fig. 2.5.

![Fig. 2.5 Basic class F power amplifier schematic.](image)

A parallel LC tank, $L_0 - C_0$, is resonant at fundamental frequency $f_0$. Ideally this tank shows infinite impedance (open) at fundamental and zero impedance (short) at harmonic ($nf_0$, $n \geq 2$) frequencies, so as to keep the output voltage a sinusoidal. Due to the quarter-wavelength transmission line’s property of impedance inversion, the transistor’s drain node observes various impedance values corresponding to different frequencies. At $f_0$, the impedance seen by the drain node can be set to the desired value.

At odd harmonics, the $L_0 - C_0$ tank is a short so that the drain sees an open impedance. At even harmonics, the quarter-wave transmission line is equivalent to a half-wavelength transmission line, presenting the drain node a short. The required impedance condition is summarized below, where $Z_1$ is the characteristic impedance of the $\lambda/4$ transmission line:

$$Z_{in}(nf_0) = \begin{cases} Z_1^2 / R & @ f_0 \quad (n = 1) \\ \text{open} & @ \text{odd harmonics} \quad (n = 3, 5...) \\ \text{short} & @ \text{even harmonics} \quad (n = 2, 4...) \end{cases}$$
Since all the even harmonics are shorted, they do not contribute to the drain voltage waveform. All the odd harmonics see open impedance at the drain node, so ideally the drain voltage presents as a square wave. The only current component that flows into the quarter-wave transmission line is at the fundamental frequency. Due to the gate biased at threshold voltage point, the PA transistor conducts current only during half of a signal period. In this ideal case drain voltage and drain current do not overlap to each other as illustrated in Fig. 2.6.

![Ideal class F power amplifier drain voltage and drain Current.](image)

The quarter-wave transmission line in Fig. 2.5 is often replaced with lumped LC tanks for integrated implementation. A series of LC tanks are used as lumped approximation to replace the transmission line. For instance, using one LC tank tuned to the third harmonic enhances the maximum drain efficiency to about 88%; adding LC resonators tuned to the fifth (Fig. 2.7) and seventh harmonics can improve the efficiency bound to 92% and 94% correspondingly [2.15]. However, obtaining the perfect waveforms in Fig. 2.6 demands infinite number \( (3f_0, 5f_0, 7f_0, \ldots) \) of cascaded LC tanks and
a flawless high Q (quality factor) $L_0-C_0$ resonator tuned at $f_0$. Due to the limited Q of LC tanks,

![Fig. 2.7 Alternative class F PA topology (tuned up to 5$f_0$).]

more power loss can be generated than expected and reduces the PA efficiency far from unity, as indicated by the reported class F PAs in Table 2.3. Note that the LC tank’s quality factor issue is a drawback for implementing Class F PAs in CMOS process, in which inductors have intrinsic coupling with substrate resulting $Q$ rarely higher than 10.

Compared with Class E PAs, Class F power amplifiers normally employ more harmonic resonators to shape waveform but put less stress on active transistors [2.16]. The maximum drain voltage swing for Class E and Class F are $3.56V_{dd}$ and $2V_{dd}$ respectively.

<table>
<thead>
<tr>
<th>Ref. #</th>
<th>Class</th>
<th>Technology</th>
<th>Frequency</th>
<th>Pout</th>
<th>PAE</th>
<th>Gain</th>
</tr>
</thead>
<tbody>
<tr>
<td>[2.16]</td>
<td>F</td>
<td>0.2 μm CMOS</td>
<td>0.90</td>
<td>31.76</td>
<td>43.00%</td>
<td>NA</td>
</tr>
<tr>
<td>[2.17]</td>
<td>F</td>
<td>0.6 μm CMOS</td>
<td>1.90</td>
<td>22.50</td>
<td>42.00%</td>
<td>10.50</td>
</tr>
<tr>
<td>[2.18]</td>
<td>F</td>
<td>pHEMT</td>
<td>14.00</td>
<td>26.50</td>
<td>57.60%</td>
<td>10.50</td>
</tr>
<tr>
<td>[2.19]</td>
<td>F</td>
<td>pHEMT</td>
<td>0.90</td>
<td>22.00</td>
<td>71.40%</td>
<td>14.00</td>
</tr>
<tr>
<td>[2.20]</td>
<td>F</td>
<td>GaAs FET</td>
<td>2.55</td>
<td>24.40</td>
<td>63.00%</td>
<td>NA</td>
</tr>
<tr>
<td>[2.21]</td>
<td>F</td>
<td>GaAs FET</td>
<td>1.60</td>
<td>28.14</td>
<td>76.70%</td>
<td>10.14</td>
</tr>
</tbody>
</table>
2.3 Load-pull Technique for PA Designs

For designs of power amplifiers, one key issue is to find a suitable load impedance to be presented to the transistor for optimal performance such as high efficiency and output power. Due to non-ideal effects, including transistor parasitics, finite RF choke inductance and bias networks, classical design equations only give rough estimate and can not predict well for the realistic large-signal operation of RF PA device [2.1] [2.2].

The load-pull technique essentially characterizes a device’s key performance parameters as a function of numerous varied load impedances. The data of the key parameters (e.g. output power, efficiency and gain) are plotted on a Smith chart as contours, which directly helps finding out the optimal load for the selected tradeoff to build up the complete PA matching networks.

One low-cost way of using load-pull is to utilize the “virtual impedance tuner” embedded in the circuit simulator of commercial EDA tools, as in the Advanced Design System (ADS). This load-pull simulation utilizes the fast computation power of EDA, but it depends on the accuracy and availability of large-signal transistor model [2.22]. Additional cost may be added to get customized models if special working conditions like bias or source power are requested for the transistor.

On the other hand, the experimental load-pull systems [2.1] [2.2] bypass the need of transistor models and incorporate the effects of transistor’s package parasitic (drain inductance). It can supply precise transistor data under various load conditions to improve PA design. An experimental load-pull system conventionally consists of a test fixture or on-wafer probes with bias modules, power meter, and more importantly the
precision mechanical tuners (Fig. 2.8) with good repeatability. The active transistor’s performance data are acquired while the mechanical tuner varies its impedances. However, mechanical tuners are driven by motors that normally move very slowly from one impedance setting to another, resulting to a time-consuming process when covering a large area of Smith chart. Besides, the associated losses of a mechanical tuner prevent it to reach the edge of Smith chart, limiting the range of achievable reflection coefficients.

The Active Load-pull (ALP) system avoids the shortcoming of lossy mechanical tuners. It introduces a properly amplified and phase-shifted external signal coupled to the transistor output port. By adjusting the amplitude and phase of the injected signal, a larger range of reflection coefficients can be synthesized at the output of the test device [2.23] [2.24]. This external signal can be either generated from an additional RF signal source (open loop), or from a feedback loop (close loop) added at the transistor output. The ALP technique is able to cover the edge of the Smith chart, but still can be time-consuming if extensive area of the Smith chart needs to be swept to make design decisions.

For the designs of high-efficiency PA (e.g. class F), the impedances at both the fundamental ($f_0$) and harmonic frequencies (e.g. $2f_0$, $3f_0$) need to be decided for optimal
PAE. That process requires considerable amount of time either using the conventional load-pull or even ALP.

In this work the proposed multi-harmonic real-time active load-pull (RT-ALP) noticeably reduces the time cost of high-efficiency PA designs. It provides fast real-time tunings [2.25] not only at \( f_0 \) but also at harmonics of \( 2f_0 \) and \( 3f_0 \). The complete Smith chart including its unity edge, where the optimal harmonic impedances of a class F PA generally located, is readily covered with the open-loop setting. In addition, the RT-ALP system is based on the unique large signal network analyzer capability of measuring both amplitude and phase of RF signals. It enables the acquisition of transistor’s time-domain RF voltage/current and dynamic loadlines, which are critical for minimizing the power consumption of transistor itself so as to improve PA efficiency. The resulting PA transistor’s power and efficiency metrics under actual working conditions directly steer the design decisions. Details of the proposed RT-ALP system are elaborated in Chapter 4.
2.4 Techniques for PA Efficiency Enhancement

2.4.1 Envelope Elimination and Restoration (EER)

As illustrated in Fig. 2.9, the EER system [2.2] generally consists of four major components: highly non-linear RF PA (e.g. class E or class F), envelope detector, limiter and amplitude modulator. It amplifies the non-constant envelope RF input by processing it as separate amplitude-modulated and phase-modulated signals. Ideally the phase characteristic of the input signal is preserved by the limiter and drives the RF PA with reduced voltage swing to minimize the chance of AM-PM distortion. The amplitude modulation information is extracted by the envelope detector and then passes through the amplitude modulator, which controls the DC supply voltage of the final RF PA to restore the envelope information back to the phase-modulated carrier creating an amplified replica of the input signal.
The EER technique allows a non-linear PA to amplify non-constant envelope RF signals with high efficiency and reasonable linearity [2.1] [2.26]. The average efficiencies reported can reach 3 to 5 times than those of linear amplifiers in L-band [2.27]. Since the linearity depends upon the modulator instead of RF-power transistors, the modulator needs to accurately track the envelope variation with fast speed because it is the only reliant signal holding the envelope information, which controls the amplitude of final RF PA output. The efficiency of this modulator is required to be high as well for good overall PA efficiency. The challenges of EER are the envelope bandwidth and phase alignment of the two signal paths. The envelope bandwidth of the modulator typically must be at least twice the RF channel bandwidth [2.1], making EER applicable to system such as North American digital cellular (NADC) [2.28]. In recent implementations, the amplitude and phase modulated signals have been generated by FPGA or DSP to extend the envelope bandwidth up to 5MHz [2.29] [2.30] for CDMA applications.

**2.4.2 Dynamic Bias**

The goal of this dynamic bias technique, also called adaptive bias [2.15], is to adjust the quiescent DC bias of the PA transistor according to its input/output drive voltage level so that the PA only provides sufficient enough DC bias power for amplification maintaining averagely high efficiency. Dynamic current bias (DCB) and dynamic voltage bias (DVB) are the two parallel methods which can be also combined together [2.31] [2.32] [2.33].
A typical DCB implementation is to vary the base/collector bias conditions of PA transistors, with the bias currents proportional to the PA’s input signal envelope as demonstrated in [2.34] for class A amplifiers.

For the case of DVB, one particular example is the “Variable Power Supply” or “Envelope Tracking (ET)” system, which borrows the concept from EER. Similar to EER, the envelope tracking system utilizes the same idea of providing dynamically adjusted drain supply voltage ($V_{dd}$) along with the detected signal envelope. However its architecture substitutes the non-linear PA and limiter in EER (Fig. 2.9) with an inherently linear RF PA and a delay line respectively. Without exploiting the non-linear PA, the ET technique tends to achieve lower efficiency but better linearity compared with EER.

To improve the overall PA efficiency, ET systems often make use of high-efficiency (>65%) and small-size dc-dc converters [2.35] [2.36] as a counterpart of the modulators in EER. PA input to help improve linearity as well. Advanced implementations of ET harness the processing power of DSP [2.37] [2.38] to control PA parameters (e.g. bias point) and add intended distortions into the PA input signal to enhance linearity. The drawbacks of DCB/DVB include the degradation of gain flatness due to the bias change and finite frequency response of the DC-DC converter that limits the PA’s operation bandwidth. The substantial complexity in the DSP domain also requires expertise beyond common RF designs.
2.4.3 Doherty Amplifier

This technique was initially introduced by W. H. Doherty for PA efficiency enhancement in the early age of broadcast transmission [2.39]. Its conventional configuration (Fig. 2.10) essentially consists of the main (carrier) amplifier PA1 and auxiliary (peaking) amplifier PA2. The RF input signal is divided to feed the inputs of PA1 and PA2 separately. The ideal quarter-wave transformation line (λ/4) functions as an impedance inverter, while the compensation line adjusts the electrical delay for in-phase power combination at the final output port (RFout).

The operation of Doherty amplifier which has been well discussed in the previous literature [2.2] [2.40], is basically divided in 3 different regions determined by its input power: low power, medium power and peak power. When the input signal is below the designed threshold, typically a quarter of the peak power (or half of peak amplitude), the Doherty amplifier is in the low power region. Since the input power is not large enough
to turn on the peaking amplifier, only the carrier amplifier functions to provide output power. With PA2 presenting a near infinite impedance to the carrier amplifier, the impedance seen at the output of PA1 is:

\[
Z_1 = \frac{(Z_T)^2}{Z_{in}} = \frac{(Z_T)^2}{Z_L} = \frac{(R)^2}{R/2} = 2R
\]

where \(R\) is the optimum load resistance determined by Eq. (2.1) under full voltage swing. The \(\lambda/4\) line’s characteristic impedance \((Z_T)\) and load \((Z_L)\) are set to be \(R\) and \(R/2\) respectively. In this region the drain efficiency is proportional to its output power, reaching to 78.5% as maximum for the classical Doherty configuration (class B).

The Doherty amplifier will enter into the medium power region as the input signal’s amplitude keeps increasing further beyond the threshold. Now the peaking amplifier PA2 begins turning on and contributes to the total output power. The increasing current \(I_2\) supplied by PA2 generates a so called load-pulling effect [2.2], which raises the effective impedance value for \(Z_{in}\). Hence the output of PA1 is presented with a decreasing impedance due to the \(\lambda/4\) impedance inverter. As a consequence the carrier amplifier is capable of delivering output power proportional to the increasing input power, while still remaining in saturation and maintaining its peak efficiency to keep the overall efficiency high at backoff. At the peak output power, both PA1 and PA2 see the optimum \(R\) at their outputs because of the load-pulling effects. Correspondingly PA1 and PA2 delivers equal amount of power to the final output.

Indeed the load-pulling effect from the peaking amplifier is not perfect mainly due to the finite device output impedance [2.41]. In practice the peaking amplifier (class B or C) also produce distortions that degrade the linearity performance. Moreover, the class C
amplifier is known to have lower gain than the class-A/AB amplifier when using the same size of device. For the case of equal input power division, the transistor size of peaking amplifier needs to be larger than that of the carrier PA for compensating for the gain difference.

Recent research interests have been focused on its non-linearities and miniature IC realization of RF Doherty amplifiers. The work reported in [2.42] and [2.43] reveals the possibility of utilizing the linearization schemes such as feedforward or predistortion in junction with the high-efficiency Doherty PA technique. Non-linear power amplifiers, e.g. class F amplifiers, can also be implemented in feedforward Doherty configuration to further boost up efficiency [2.44]. Using DSP control to dynamically adjust the gate bias of peaking amplifier [2.45] has been demonstrated to improve linearity for CDMA at 840 MHz.

Already recognized by the base station PA designers, the Doherty amplifier is indeed a very promising solution for mobile handsets/terminals as well, due to its less complex configuration compared with other efficiency enhancement techniques [2.42]. Even though the transmission lines in conventional Doherty configuration may occupy large circuitry area, it is feasible to replace them with active phase shifter [2.46] or LC lumped elements [2.47] [2.48] to shrink geometry for integrated implementation.

The details of the proposed CMOS Doherty power amplifier design are presented in Chapter 5.
2.4.4 Linear Amplification using Non-linear Components (LINC)

Often referred to as “outphasing PA”, the LINC technique was exploited by AM-broadcast transmitters and came to microwave applications in the 1970s [2.1] [2.49]. It utilizes two highly non-linear PAs (PA1 and PA2) to achieve linear amplification with high efficiency. As can be seen in Fig. 2.11, the RF input signal with time-varying amplitude and phase is converted into two constant envelope signals by a signal separator.

The idea of this conversion derives from the following arithmetic identity:

\[
\cos(x) + \cos(y) = 2 \cos\left(\frac{x+y}{2}\right) \cos\left(\frac{x-y}{2}\right)
\]  

(2.7)

Formulated with \(A(t)\) and \(\alpha(t)\) for amplitude and phase modulation respectively, the RF input \(V_{in}(t)\) is converted to \(V_1(t)\) and \(V_2(t)\) that have phase difference of \(2\beta(t)\):

\[
V_{in}(t) = A(t) \cos(\omega t + \alpha(t)) \\
V_1(t) = \cos(\omega t + \alpha(t) + \beta(t)) \\
V_2(t) = \cos(\omega t + \alpha(t) - \beta(t))
\]

(2.8)  

(2.9)  

(2.10)

where \(\beta(t)\) is determined by the \(A(t)\), the envelope of input RF signal:

\[
\beta(t) = \arccos(A(t))
\]

(2.11)

Fig. 2.11 Linear amplification using non-linear components (LINC) system diagram.
Driven by the constant envelope signals with different time-varying phase ($V_1(t)$ and $V_2(t)$), the efficient PA1 and PA2 having identical gain ($G$) amplify and combine the two signal paths for the final output $V_{out}(t)$, which replicate the original amplitude and phase modulation:

$$V_{out}(t) = G[V_1(t) + V_2(t)]$$

$$= 2GA(t)\cos(\omega t + \alpha(t)) \quad (2.12)$$

The practical designs are not as straightforward as the simple equations. First a complicated signal separation is critical to translate the envelope modulation of input to the corresponding phase modulation $V_1(t)$ and $V_2(t)$. In addition the combiner needs to have low loss and good isolation between its two input ports to avoid mutual coupling before the two signal paths combine [2.50][2.51]. LINC is also sensitive to component drift due to factors such as aging and temperature changes, which may affect signal separator’s performance and shift the gains of PA1 and PA2 to be not identical. Nevertheless reported results have demonstrated LINC’s application to CDMA [2.52] and capability of handling signals with high peak-to-average ratio (10 dB) up to 52.1% for PA efficiency [2.50].
2.5 Techniques for PA Linearization

The following subsections focus on two of the major linearization techniques, feedforward and predistortion [2.1].

2.5.1 Feedforward

![Feedforward linearization system diagram](image)

Fig. 2.12 Feedforward linearization system diagram.

The feedforward technique can be dated back to the patent by Black [2.53]. As shown in Fig. 2.12, the feedforward system includes a RF PA and another error amplifier utilized for canceling non-linearities. With splitter the RF input signal ($V_{\text{in}}$) is directed into two paths. One goes through the main RF PA for amplification and generates a non-linear output, containing the desired signal with unwanted distorted products due to inter-modulation (IMD). This non-linear amplified signal is coupled and attenuated with factor of $1/A_v$ and then sent to 180-degree combiner. The other path is designed to present a non-distorted version of signal after the delay line A. Then the subtraction occurs and ideally the only left signal is the RF PA’s unwanted distortion component, which is amplified by the small signal error amplifier. This error amplifier is assumed to produce
no additional distortion and its amplified result is sent to combine with the delayed (delay line B) version of RF PA’s output. Ideally the non-linearities in this RF PA’s output are cancelled by the error amplifier’s output, so that the merged final signal ($V_{out}$) is a highly linear amplification result of $V_{in}$.

The feedforward technique overcomes stability issues due to its open-loop structure. It also offers a finite bandwidth available from the delay lines. However, the error amplifier is required to be low power and provide very linear amplification. In addition, the matching between the two paths is so critical. The two delay lines, A and B, have to accurately match the latency of the RF PA and error amplifier respectively to avoid poor cancellation that brings phase distortion. The considerable losses of the combiners and delay lines also need to be taken into account for the power budget. With these prices feedforward typically improves distortions more than 20 dB [2.1] [2.54] [2.55]. It is capable of linearizing highly non-linear PA for example class-F as reported in [2.44].

2.5.2 Predistortion

The basic concept of a predistortion technique (Fig. 2.13) is to add a nonlinear element preceding to the RF PA of interest, so that the combined transfer characteristic becomes linear [2.1][2.2]. The linear relationship between system input and output is normally formed by subtracting the additional expansive transfer function from the original PA compression transfer function. The typical improvement for IMD3 is over 10 dB.

RF/Analog predistortion [2.56] [2.57] belongs to the traditional category for predistortion technique. Either a RF or analog device, such as the active cuber [2.58]
circuit, is built before the PA input to generate the desired non-linear correction signals which are inverse to the PA’s distortion characteristics. Without the error amplifier, it typically has less power consumption than a feedforward PA. It also offers better stability and bandwidth than feedback technique due to its open-loop structure. However the gain and flatness of the predistorter will also limit the performance of the linearized PA.

Digital predistortion has been extensively reported in recent years [2.59] [2.60]. The rapidly increasing power of digital signal processing (DSP) has provided a chance to digitally correct the non-linearities produced by PA transistors. As shown in Fig. 2.14, predistortion can happen in digital baseband with the look-up-table (LUT) storing envelope and phase compensation [2.61], prior to the DAC and upconversion which generates the PA’s input signal. Having demonstrated capabilities to linearize PAs in narrowband systems, digital predistortion also shows potentials to wideband application [2.62].
To achieve good linearity a critical assumption for most digital predistortion is the sufficiently well characterized PA model without memory effects [2.63]. In reality, however, process variations and memory effects due to self-heating/bias circuit indeed change the PA’s transfer function and cause the IMD products to be asymmetric. Consequently an adaptive algorithm is necessary requiring substantial processing and storage of LUT to adjust the amplitude and phase compensation for optimization [2.64][2.65]. Nevertheless digital predistorter with DSP hardware has potential of readily integrating into cellular handsets, which usually has less stringent linearity requirement than base stations.
CHAPTER 3

ANALYSIS AND DESIGN OF HIGH-EFFICIENCY CLASS E PA

3.1 Introduction

As noted in Chapter 2, class E power amplifiers are non-linear and operated in switching-mode. The theoretical maximum drain efficiency of 100% is acquired by eliminating the overlap between transistor’s drain voltage and current. In practice however the ideal switching operation of class E RF PAs are challenged due to multiple factors.

In this chapter, the principle of class E PAs and assumptions for ideal switching operation are first investigated, followed by the discussion of a 2.4 GHz class E PA design with pHEMT transistor. Extensive load-pull simulations in Advanced Design System (ADS) are used to facilitate this design.

3.2 Analysis of Class E Power Amplifier

The schematic of an ideal class E power amplifier is repeated in Fig. 3.1. It includes a transistor whose operation approximates an on/off switch S, showing infinite “off” impedance and zero “on” impedance in ideal case. For a Field Effect Transistor (FET),
the off status corresponds to cutoff region and the on status corresponds to triode region. Ideally no power is dissipated in the transistor except at the switching transients.

![Ideal class E power amplifier schematic.](image)

Behaving like a constant DC current source, the RF choke inductor $L_1$ connects the switch to supply voltage ($V_{dd}$). The switching transistor ($S$ in Fig. 3.1) contains a parasitic drain to source capacitance $C_i$, which combines with the external capacitance $C_2$ to form $C_p$ in parallel with the switch. Consisting of the inductor $L_0$ and capacitor $C_o$, the series resonant circuit is tuned to the input signal frequency. The reactance ensures a proper phase shift between the output voltage and drain voltage is established. The load resistance is $R$, which could result from the impedance transformation of standard 50 Ohm load.

To alleviate the analytical complexity, early works were based on the following assumptions [3.1] [3.2] [3.3]:

A. Inductance of RF choke is high so that it only allows DC current going through.

B. $Q_e$ of series resonant circuit is infinite or high enough so that output voltage only
has fundamental frequency component.

C. Loss of the switch is negligible: the transistor has zero voltage when switch is on, zero on-resistance and infinite off-resistance. Inevitable transition times between on and off status are minimized.

D. The total shunt capacitance is linear, i.e., independent of the drain voltage.

Fig. 3.2 Ideal voltage and current waveforms of class E power amplifier.

Fig. 3.2 shows the ideal waveforms for a class E PA. Driven by the gate input signal, the switch is turned on and off periodically at the input signal frequency. During the ON time interval, the switch is turned on and the voltage across it is zero. During the OFF time interval, the switch is turned off and the current going through it is zero. Meanwhile the current from DC supply begins to charge the capacitance $C_p$. This means that the
switch voltage will rise as $C_p$ is being charged. When the ON cycle comes again, any charge still stored on the capacitance $C_p$ will discharge through the switch to ground, generating a potential loss of power. To avoid this drain discharge loss, the circuit can be designed so that the drain-to-source voltage across transistor switch decreases to zero and has a zero slope (circled part in Fig. 3.2) before switch-on time arrives.

If a 50% switching duty cycle is assumed, the design equations for optimum class E PA are reproduced below:

\[
C_p = \frac{0.1837}{\omega R} \quad (3.1) \\
P_{\text{out}} = \frac{(V_{dd} - V_{\text{knee}})^2}{1.7337R} = \frac{V_{\text{eff}}^2}{1.7337R} \quad (3.2)
\]

\[
R = \frac{0.577(V_{\text{eff}})^2}{P_{\text{out}}} \quad (3.3) \\
X = 1.152R \quad (3.4)
\]

Normally the pre-determined output power level and supply voltage will control the optimal value of the load resistance. The total parallel capacitance $C_p$ is dependent on the operation frequency and load resistance. For BJT transistors the knee voltage $V_{\text{knee}}$ in Eq.(3.2) becomes saturation voltage $V_{CE(Sat)}$. The required fundamental and harmonic impedance are [3.4]:

\[
Z_{in}(n f_0) = \begin{cases} 
R + jX = R(1 + j1.152) & \text{at } f_0 \\
\text{open} & \text{at others (} n = 2,3,4,\ldots \)
\end{cases} \quad (3.5)
\]

To evaluate the PA performance, the following definitions of Power Added Efficiency (PAE) and Drain Efficiency (DE) are used:

\[
PAE = \frac{P_{\text{out}} - P_{\text{in}}}{P_{dc}} \quad (3.6) \quad \text{and} \quad \eta = \frac{P_{\text{out}}}{P_{dc}} \quad (3.7)
\]
With the aforementioned assumptions and ideal lossless conditions, no power is
dissipated either in the transistor switch or other components. Hence all the DC supply
power is transformed to RF output power and the theoretical maximum drain efficiency is
100%. Re-derivations of the analytical equations for class E switching amplifiers are
provided in Appendix A for validation of the counterpart in [3.3].

To improve designs of class E PAs, a number of publications dealt with different
aspects of non-ideal effects of class E power amplifiers. A real switch implemented with
a transistor always has some resistive loss, which means that during the switch-on time
the transistor inevitably sustains some small amount of voltage while carrying a current.
Derivations presented in [3.5] [3.6] [3.7] attempted to analyze effect of finite switching-
on resistance with a resistor model inserting in the switch path. Yoo [3.8] derived an
equation demonstrating the degradation effect of on-resistance on drain efficiency, where
\( r_{on} \) represents the on-resistance of the transistor switch.

\[
\eta = \frac{1}{1 + 1.4 (r_{on} / R)}
\]  
(3.8)

For practical implementation a RF choke inductor has finite inductance. To include
this effect, there were also discussions [3.9] [3.10] [3.11] about replacing the ideal RF
choke (infinite inductance) with a finite DC feed inductance in the analysis for class E
PA. Early analysis works as well assume an infinite quality factor \( Q_L \) in the output
network used for the design equation derivations. However, the value of \( Q_L \) at RF
frequency is often limited by realization, especially in the situation of integrated passive
elements. Also it is often desirable to use low quality factor value to obtain wider
operating frequency bandwidth, in spite of the fact that the output current accordingly
have more harmonic components. The dependence of class E power amplifier performance on the value of $Q_L$ has been analyzed in [3.12] [3.13].

At RF operating frequencies, the shunt capacitance in the typical class E amplifier configuration is dominated by the switching transistor’s nonlinear parasitic capacitance [3.14], which is voltage dependent and leads to the required component values being different from the values resulting with constant capacitor. Nonlinear output capacitance models were introduced [3.15] [3.16] to aid calculating the actual optimal class E PA component values. Equivalent shunt capacitance concept was proposed to model the nonlinear capacitance for satisfying class E amplifier’s optimum conditions.

### 3.3 Class E PA Circuit Design with ADS Load-pull

The classical class E design equations in previous section are based on assumptions that are not realistic enough for practical designs at RF frequencies. Although analytical design methods considering non-ideal effects have been studied as referred in section 3.2, they either result in very complicated design equations or rely on numerical method to obtain meaningful solution. Those analytical methods unavoidably still incorporate some of the original ideal assumptions, to keep away from the analytically intractable situation [3.4], i.e., reduce the complexity of derivations. Consequently more tuning cycles, however, are needed to reach the desired circuit performance during tests. Additional tuning circuits may also degrade the efficiency of the power amplifier.

To overcome the difficulties met by the analytical methods, the load-pull (LP) simulation can be considered to improve the practical designs of class E power amplifier, especially for RF frequencies where parasitic parameters may dominate performance.
As described in Chapter 2, the load-pull simulation looks for optimum load impedance values that maximize the power amplifier’s performance, such as power added efficiency (PAE) and output power (Pout). Because the typically used small-signal S-parameters and static IV curves are only applicable for small-signal levels, load-pull simulation utilizes large-signal device model to predict the device’s behavior as a power amplifier. The load-pull simulation calculates PAE or Pout for different load conditions to generate contours on Smith chart so as to find the best targeted load impedance.

Practical circuits can exhibit a number of deviations from the idealized class E operation, such as finite switching transient time and finite DC feed inductance, etc. So the realistic impedance values for achieving optimal performance are different from the idealized Eq.(3.5). With the aid of load-pull simulation in ADS, it is possible to find realistic load impedance conditions that provide maximized PAE and Pout performance.

3.4 Class E PA Design Details and Simulation Results in ADS

The design of a class E power amplifier targeted for Bluetooth application at 2.4 GHz is presented here. A pHEMT device, ATF-54143, is considered because of its low knee voltage compared with GaAs FET and high switching speed capability. As indicated in Eq.(3.2), the low knee voltage is beneficial for maintaining high output power and efficiency. With the advantage of single-polarity power supply configuration, ATF-54143 has 20dBm P1dB compression point, which is suitable for the power class 1 level of Bluetooth standard.

Load-pull simulations are executed in the ADS utilizing its embedded tuner function. The principle is to run the harmonic balance simulation to calculate PAE and Pout, while
ADS load tuner simultaneously sweeping Smith chart to get the optimal impedance points. The ADS tuner is set to sweep the fundamental load impedances ($Z_{load}$) stored in a one-port component that saves $S_{11}$ (reflection coefficient) data. The sweeping algorithm selects a center point with radius for a circle on the Smith chart. Then the number of impedance points desired to sweep within this circle are assigned. For each impedance point swept, the harmonic balance simulator calculates resulting PAE and Pout. The optimal load impedance can be found eventually by adjusting the positions of circles.

Fig. 3.3 Harmonic termination network (HTN) in class E PA.

Besides the load tuner in ADS, another key in this design is the Harmonic Termination Network (HTN) as in Fig. 3.3, which is a substitute for the ideal series LC resonator ($L_0-C_0$). HTN terminates the targeted harmonics and transforms the optimal fundamental load impedance to the drain node of transistor.

The designed HTN topology is as demonstrated in Fig. 3.4. It consists of a set of transmission lines and open stubs to short harmonics at frequencies of $2f_0$, $3f_0$ and $4f_0$. The open stub for terminating the highest harmonic frequency ($4f_0$) is positioned closest to the drain node. The stubs for controlling lower harmonics are positioned further from
the drain to allow for terminating harmonics with the shortest circuit dimension.

The open stub $l_4$ is of 90° electrical length at the fourth harmonic, so a short circuit presents at the point A in Fig. 3.4. Since $l_4$ is also 90° long at the fourth harmonic, this short circuit at point A is transformed to an open at drain node. This open impedance condition presented at the fourth harmonic is not affected by other lines and stubs [3.17]. Similarly, open stubs $l_3$ and $l_2$ are 90° long at the third and second harmonics respectively; they create a short circuit at points B and C correspondingly. The transmission lines $l_A$, $l_B$ and $l_C$ cooperatively function with stubs $l_3$ and $l_2$ to present open impedance condition for drain node at third and second harmonics. The whole HTN circuit is implemented in ADS using microstrip lines using Duroid 5880 substrate, which has dielectric constant of

Fig. 3.5 ADS layout of the HTN implemented with microstrip lines.
2.2 and substrate thickness of 31mil. The generated HTN layout is illustrated in Fig. 3.5.

The load-pull simulations are executed by setting the center of sweeping circle at (-0.2+j0.1) and radius of 0.8 in Smith chart. Based on the input power of 10 dBm, the resulting efficiency and output power contours are shown in Fig. 3.6. The maximum achievable PAE is 59.88\% and corresponding output power (Pout) is 19.7 dBm. The optimal impedance points corresponding to the highest PAE and highest Pout (20.67 dBm) are close to each other in the Smith chart.

![PAE and Pout contours from load-pull simulations.](image)

From the PAE contour in Fig. 3.6 a normalized load impedance point (0.351+j0.396), corresponding to maximum PAE, is chosen for in depth harmonic balance simulations with the input excitation power of 10 dBm. Fig. 3.7 shows the current of transistor (switch) itself ($i_{SW}$), the current going through the paralleled capacitor ($i_{CAP}$) and the total current, which is the sum of $i_{SW}$ and $i_{CAP}$. 

---

Fig. 3.6 PAE and Pout contours from load-pull simulations.

From the PAE contour in Fig. 3.6 a normalized load impedance point (0.351+j0.396), corresponding to maximum PAE, is chosen for in depth harmonic balance simulations with the input excitation power of 10 dBm. Fig. 3.7 shows the current of transistor (switch) itself ($i_{SW}$), the current going through the paralleled capacitor ($i_{CAP}$) and the total current, which is the sum of $i_{SW}$ and $i_{CAP}$. 

---

Fig. 3.7 Current in SW and CAP.
In Fig. 3.8 the critical drain voltage \( v_{DS} = v_{SW} \) and drain current \( i_{DS} = i_{SW} \) are displayed. Apparently the slope of the drain voltage is steeper when it rises than it falls back to zero. Although the drain voltage is nonzero after the switch current rises, the overlap between the drain voltage and current is still small so as to achieve the high PAE. Voltage amplification is observed from Fig. 3.9 that shows the load voltage and input voltage of the PA. The sinusoidal load current after suppression of harmonics is also shown in Fig. 3.9.

Fig. 3.9 Load current, load voltage and input voltage.
The simulated dynamic loadline in IV plane is plotted in Fig. 3.10 to show the trajectory of both drain current and voltage. Its background is the DC IV characteristic curves of ATF-54143. For the loadline of case A, the current value only includes the drain current that flows through the transistor switch. It demonstrates the transition between the triode region (ON) and cutoff region (OFF). The loadline of case B include the current of both transistor itself and the parallel capacitor ($C_p$). It shows the charging and discharging effects of the parallel capacitor.

Other than using the nominal input power level of 10dBm, harmonic balance simulations with a power sweep from 6dBm to 12dBm are also carried with results summarized in Table 3.1 and Table 3.2.

<table>
<thead>
<tr>
<th>RF Input Power (dBm)</th>
<th>RF Output Power (dBm)</th>
<th>Power Gain (dB)</th>
<th>PAE (%)</th>
<th>Total DC Power Consumption (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>6.00</td>
<td>15.94</td>
<td>9.94</td>
<td>41.95</td>
<td>0.08</td>
</tr>
<tr>
<td>8.00</td>
<td>18.41</td>
<td>10.41</td>
<td>54.19</td>
<td>0.12</td>
</tr>
<tr>
<td>10.00</td>
<td>19.73</td>
<td>9.73</td>
<td>59.34</td>
<td>0.14</td>
</tr>
<tr>
<td>12.00</td>
<td>20.44</td>
<td>8.44</td>
<td>59.05</td>
<td>0.16</td>
</tr>
</tbody>
</table>

Table 3.1 Summary of harmonic balance simulation with power sweep.

<table>
<thead>
<tr>
<th>Input RF Power (dBm)</th>
<th>$f_0=2.4$GHz Power (dBm)</th>
<th>$2f_0=4.8$GHz Power (dBc)</th>
<th>$3f_0=7.2$GHz Power (dBc)</th>
<th>$4f_0=9.6$GHz Power (dBc)</th>
<th>$5f_0=12$GHz Power (dBc)</th>
</tr>
</thead>
<tbody>
<tr>
<td>6.00</td>
<td>15.94</td>
<td>-71.30</td>
<td>-78.03</td>
<td>-75.18</td>
<td>-33.86</td>
</tr>
<tr>
<td>8.00</td>
<td>18.41</td>
<td>-73.05</td>
<td>-74.93</td>
<td>-71.40</td>
<td>-31.98</td>
</tr>
<tr>
<td>10.00</td>
<td>19.73</td>
<td>-75.01</td>
<td>-66.53</td>
<td>-70.91</td>
<td>-36.86</td>
</tr>
<tr>
<td>12.00</td>
<td>20.44</td>
<td>-75.96</td>
<td>-64.42</td>
<td>-76.64</td>
<td>-26.22</td>
</tr>
</tbody>
</table>

Table 3.2 Output spectrum from the fundamental to the fifth harmonic ($f_0$ to $5f_0$).

The PAE obtained at 10 dBm input power is higher than others. Compared with the output power at the fundamental frequency (2.4 GHz), the second, third and fourth
harmonic contents are lower than -66 dBc due to the function of the harmonic termination network in design.

Fig. 3.11 Dynamic loadline with power sweep. Fig. 3.12 Transistor instantaneous power.

Fig. 3.11 shows the dynamic loadline corresponding to different input power without affected by the $C_p$. With different power excitation, the instantaneous power consumption of the transistor itself is displayed in Fig. 3.12. The positive and negative parts cancel to each other to reduce the transistor’s average power consumption.

Fig. 3.13 HTN impedance variations vs. harmonic frequency ($f_0$ to $4f_0$). Fig. 3.14 Pout and PAE vs. supply voltage.
Fig.3.13 shows $S_{11}$ simulation results of the harmonic termination network. At the fundamental frequency (2.4 GHz) the $S_{11}$ of HTN does not change the optimum impedance value (0.351+j0.396) for maximizing PAE. At the harmonic frequencies ($2f_0, 3f_0, 4f_0$) the HTN is able to provide highly reactive impedances, which are often considered as the practical methods of satisfying the load impedance conditions of the class E PAs. As can be seen in Fig. 3.14, the output power can be controlled via adjusting the DC supply voltage ($V_{dd}$). The PAE is able to maintain between 57.5% and 59.3% even though the supply voltage changes from 2 to 3 V. This verifies an advantage [3.18] of the class E power amplifier that is in sharp contrast to conventional power amplifiers, which typically achieve optimum efficiency only at the maximum output power. The relatively constant efficiency of class E PAs will generally lead to substantial power saving.
CHAPTER 4

REAL-TIME ACTIVE LOAD-PULL OF THE 2ND & 3RD HARMONICS
FOR DESIGN OF NON-LINEAR POWER AMPLIFIERS

4.1 Introduction

Nowadays the availability of high efficiency RF power amplifier (PA) is a critical factor for wireless mobile devices to extend battery operation time as well as reduce the heat sink form factor and weight. Likewise base stations also demand high efficiency PAs to save supply power consumption and cooling cost. Non-linear power amplifiers, such as class F [4.1] [4.2], are potential solutions due to the theoretically non-overlapping device current and voltage waveforms that minimize the power dissipation of the transistor itself.

As described in Chapter 2, the experimental load-pull technique is a good empirical approach to look for optimum load impedance values that maximize the power amplifier’s performance, e.g. efficiency or output power. However, classical load-pull systems with passive tuners are typically time-consuming when sweeping a large area of the Smith chart. Moreover the attainable reflection coefficient magnitude is limited by the passive tuner losses. Active load-pull (ALP) systems relying on the closed-loop architecture [4.3] [4.4] improve the reflection coefficient range, but are subject to
potential stability problems. The open-loop ALP system in [4.5] overcomes the stability issue and the reflection coefficient is calculated from the measured incident and reflected waves. The time needed for finding the optimal load terminations in non-linear PA designs, however, remains significant as both the amplitude and phase must be swept for each harmonic under computer control.

A versatile real-time multi-harmonic active load-pull (RT-ALP) system based on the large signal network analyzer (LSNA) is developed for the design of class F RF power amplifiers (PA). The real-time concept previously used for fundamental-impedance tuning in [4.6] is extended here to the real-time impedance tunings at not only fundamental frequency but also higher harmonics (2f₀, 3f₀). The real-time open-loop technique used enables to efficiently synthesize a wide range of fundamental and harmonic load conditions without stability issues. A supportive theory is proposed with derived equations.

This multi-harmonic RT-ALP technique is applied to an on-wafer GaN HEMT device with a very high PAE of 80.96% demonstrated at 2 GHz. A complete pHEMT PA is designed based on the comprehensive RT-ALP data and implemented with microstrip networks for optimal match, achieving a maximum PAE of 75% for 18.6 dBm output power at 2GHz.
4.2 Real-time Multi-harmonic Active Load-pull System

4.2.1 Real-time Tuning

Real-time tuning at the n-th harmonic utilizes one CW tone $a_2(n\omega_0 + \Delta\omega)$, which is injected at the device output and has a frequency offset $\Delta\omega$ (Fig. 4.1 and Fig. 4.2) from the targeted n-th harmonic frequency, so that the phase of the harmonic load reflection coefficient is continuously swept in a single LSNA measurement (e.g., 10ms). The power level of this CW tone $\left|a_2(n\omega_0 + \Delta\omega)\right|^2$ is then in turns stepped under computer control to vary the radius of the reflection coefficient loci as well, and produce a large set of harmonic reflective load coefficients with amplitude smaller or larger than unity mapping the extended Smith chart.

In a more advanced real-time tuning scheme both the amplitude and phase could be continuously swept. This could be realized by injecting a two-tone excitation, $a_2(n\omega_0 + \Delta\omega)$ and $a_2(n\omega_0 + \Delta\omega + \delta\omega)$, at the device output. The amplitude would be swept with the beat frequency $\delta\omega \ll \Delta\omega$ and the phase with the frequency $\Delta\omega$ like in the single tone case. The work presented here focuses on real-time tuning realized by injecting of a single CW tone.

Fig. 4.1 Frequency domain demonstration of RT-ALP signal injection ($a_2(n\omega_0 + \Delta\omega)$) at the transistor’s output. Note $a_2$ is the incident wave at the output port.
4.2.2 RT-ALP Measurement System Description

The real-time multi-harmonic active load-pull system implemented with the LSNA is depicted in Fig. 4.2. The LSNA is able to measure both amplitude and phase of RF spectrum components in frequency domain, while displaying time domain current and voltage waveforms for large signal excitation. With its wideband measurement ability (up to 40 GHz), LSNA is ideal for inspecting transistor’s multi-harmonic non-linear behavior for instance in class F PA.

In Fig. 4.2, Port 1 is used for the gate and port 2 for the drain of the Device Under Test (DUT). Two external bias tees and DC power supplies set the quiescent operating point of the DUT. The voltage probes and current sensors detect the time variations of the device bias voltage/current, which are displayed on the oscilloscope. A group-delay
calibration procedure was developed to synchronize the RF envelope measured by the LSNA with the time-dependence of the acquired bias current signal (with period $\Delta \omega$).

For this study the ESG source generates the fundamental 2GHz signal used to excite the DUT input. The two harmonic sources (PSG and Anritsu) inject the $(2\omega_0 + \Delta \omega, 3\omega_0 + \Delta \omega)$ signals in the real-time tuning case (i.e. swept phase measurement), or generate $(2\omega_0, 3\omega_0)$ in the constant phase measurement case. The 10MHz reference signals of all the signal sources are tied together for phase synchronization.

The diplexer provides a path for the injected second and third harmonic signals to reach the transistor output while maintaining good impedance match (50 Ohm) at fundamental frequency for LSNA’s port 2.

The LSNA directly acquires the incident and reflected waves in the frequency domain at the de-embedded calibration planes (Fig. 4.2). A two-tier calibration is used to adjust the LSNA calibration as the tuner impedance is varied. The LSNA is operated in the modulation mode to deal with the modulation effects brought about by $\Delta \omega$. The used modulation frequency ($\Delta f = 2\pi \Delta \omega$) is 200 kHz with the resolution BW as 95.37 Hz.

![Graph](image)

Fig. 4.3 Example of swept dynamic loadlines acquired by the RT-ALP technique.
For the practical design of class F power amplifiers, the real-time feature of this system can reduce the time required for exhaustive search for optimal harmonic conditions, as well as enable the acquisition of RF dynamic loadlines as shown in Fig. 4.3. Without exhibiting any oscillation problem, the active open-loop approach allows the emulated harmonic load to reach the edge of the Smith chart, where the optimal harmonic terminations are generally positioned.

4.3 Supportive Theory

4.3.1 Time Domain Reconstruction

The time domain incident waveform \(a_{i,\text{total}}(t)\) at port \(i\) can be reconstructed from the frequency domain complex incident waves \(a_i(n\omega_0 + p\Delta\omega)\) acquired by the LSNA using:

\[
a_{i,\text{total}}(t) = \text{Re}[A_i(t)] = \sum_{n=1}^{N} \sum_{p=-SSB}^{SSB} \text{Re}[a_i(n\omega_0 + p\Delta\omega)e^{j(n\omega_0 + p\Delta\omega)t}] \tag{4.1}
\]

where \(i=1\) or \(2\) is the port index, \(n\) the number of harmonic and \(p\) the single side band (SSB) tones around the center tone. The reflected wave \(b_{i,\text{total}}(t)\) can be similarly calculated. The time domain RF voltage and current are then given by LSNA:

\[
v_i(t) = a_{i,\text{total}}(t) + b_{i,\text{total}}(t) \tag{4.2}
\]

\[
i_i(t) = [a_{i,\text{total}}(t) - b_{i,\text{total}}(t)]/50 \tag{4.3}
\]

4.3.2 Extraction of Reflection Coefficient and Output Power in Swept Phase Measurement

For the \(n\)-th harmonic frequency, the swept phase measurement introduces a CW tone with frequency offset \(\Delta\omega\). So the incident and reflected complex wave around \(n\omega_0\) at the DUT output port can be approximated by the following two dominant tones:
\[ A_{2,n}(t) = a_z(n\omega_0)e^{j\omega_0 t} + a_z(n\omega_0 + \Delta\omega)e^{j(n\omega_0 + \Delta\omega)t} \]  \hspace{1cm} (4.4)

\[ B_{2,n}(t) = b_z(n\omega_0)e^{j\omega_0 t} + b_z(n\omega_0 + \Delta\omega)e^{j(n\omega_0 + \Delta\omega)t} \]  \hspace{1cm} (4.5)

Within a narrow time interval \([t, t + T]\) with \(T = 1/(2\pi\omega_0)\), one can use the least square fit method to represent the above two main tones with a single tone:

\[ a_{2,n}(t) = \text{Re}[A_{2,n}(t)] = C_{a,n} \cos(n\omega_0 t) - S_{a,n} \sin(n\omega_0 t) \]  \hspace{1cm} (4.6)

\[ b_{2,n}(t) = \text{Re}[B_{2,n}(t)] = C_{b,n} \cos(n\omega_0 t) - S_{b,n} \sin(n\omega_0 t) \]  \hspace{1cm} (4.7)

where the coefficients \(C_{a,n}, S_{a,n}, C_{b,n}\) and \(S_{b,n}\) are \textit{time dependent} since they are extracted in the interval \([t, t + T]\).

Because the modulation frequency \(\Delta\omega\) is small compared to the RF frequency, the above estimation is reasonable. Then the reflection coefficient at the n-th harmonic \((n\omega_0)\) can be extracted to be:

\[ \Gamma_{L}(n\omega_0, t) = \left( \frac{C^2_{a,n}(t) + S^2_{a,n}(t)}{C^2_{b,n}(t) + S^2_{b,n}(t)} \right)^{1/2} e^{j[\phi_{a,n}(t) - \phi_{a,n}(t)]} \]  \hspace{1cm} (4.8)

where \(\phi_{a,n} = \angle(C_{a,n} + jS_{a,n})\) and \(\phi_{b,n} = \angle(C_{b,n} + jS_{b,n})\). The extracted \(\Gamma_{L}(n\omega_0, t)\) is time dependent for the swept phase measurement due to the time interval dependence.

As derived in Appendix B, the more direct method for extracting \(\Gamma_{L}(n\omega_0, t)\) is based on device output port’s signal flow graph, which leads to the following equation:

\[ \Gamma_{L}(n\omega_0, t) = \frac{A_{2,n}(t)}{B_{2,n}(t)} \]

\[ = \Gamma_{L_0} + \frac{(1 - \Gamma_{L_0}\Gamma'_{\omega_0})}{\Gamma'_{\omega_0}[1 + e^{-j\Delta\omega}b_z(n\omega_0)/b_z(n\omega_0 + \Delta\omega)]} \]  \hspace{1cm} (4.9)

where \(\Gamma'_{\omega_0} = b_z(n\omega_0 + \Delta\omega)/a_z(n\omega_0 + \Delta\omega)\), and \(\Gamma_{L_0} = a_z(n\omega_0)/b_z(n\omega_0)\).
In fact the extracted $\Gamma_L(n\omega_0,t)$ from Eq. (4.8) and (4.9) match quasi perfectly and Eq. (4.9) will be preferred for the simplicity of its calculation.

A third method more realistic than the previous ones, extracts $\Gamma_L(n\omega_0,t)$ by accounting for all the sidebands tones with $p$ ranging from $-SSB$ to $SSB$:

$$\Gamma_L(n\omega_0,t) = \frac{\sum_{p=-SSB}^{SSB} a_z(n\omega_0 + p\Delta\omega)e^{ip\omega t}}{\sum_{p=-SSB}^{SSB} b_z(n\omega_0 + p\Delta\omega)e^{ip\omega t}}$$  \hspace{1cm} (4.10)

At low injection power $|a_z(n\omega_0 + \Delta\omega)|^2$ limiting the $\Gamma_L(n\omega_0,t)$ calculation to the two dominant tones like in Eq. (4.8) or (4.9), is a good approximation of Eq. (4.10) and will result in smooth circular $\Gamma_L(n\omega_0,t)$ loci.

The total RF output power including all the harmonics at port 2 is determined by:

$$P_{out,total} = \sum_{n=1}^{N} P_{out}(n\omega_0,t)$$

where

$$P_{out}(n\omega_0,t) = \frac{1}{2} \sum_{p=-SSB}^{SSB} \sum_{q=-SSB}^{SSB} \left\{ |a_z(n\omega_0 + p\Delta\omega)\times i_z^*(n\omega_0 + q\Delta\omega)e^{ip\omega t}|^2 \right\}$$  \hspace{1cm} (4.11)

Considering only the RF fundamental output power, $P_{out}(\omega_0,t)$, the following equation defines the PAE used in the subsequent measurements:

$$PAE = \frac{P_{out}(t) - P_{out}(t)}{P_{DC}} = \frac{P_{out}(\omega_0,t) - P_{out}(\omega_0,t)}{P_{DC}}$$  \hspace{1cm} (4.12)

The input power, $P_{in}(t)$, which is calculated using a similar method to Eq. (4.11), considers the modulation effects brought about by the swept phase measurement.
4.4 Multi-harmonic RT-ALP Experimental Results of A GaN PA

In this part of the study, the DUT is an on-wafer GaN HEMT investigated for class F operation at 2GHz. The LSNA is used to acquire frequency domain data up to the fourth harmonic (N=4) each with 99 tones (SSB = 49). The quiescent DC bias of the GaN HEMT device is $V_{GS} = -2.77V$, $V_{DS} = 4.25V$, and $I_{DS} = 1.7mA$.

Before we pursue the real-time 2nd and 3rd harmonic tuning, it is desirable to run the real-time ALP measurement at the fundamental frequency, so that an optimal load at $\omega_0$ is found to form the basis for subsequent harmonic tuning.

4.4.1 Fundamental Real-time Active Load-pull

In this measurement the ESG source provides the 2GHz fundamental $\omega_0$ signal and the PSG source injects the $\omega_0 + \Delta \omega$ signal to the DUT output.

As shown in Fig. 4.4, both the phase and magnitude of the load reflection coefficient

Fig. 4.4 Loci of $\Gamma_L(\omega_0,t)$ obtained from the $(\omega_0+\Delta\omega)$ real-time swept phase measurements using Eq. (4.9) (solid line) and Eq. (4.10) (dashed line).
are well swept in the Smith chart. The density of the $\Gamma_L(\omega_0, t)$ loci can be controlled by varying the power level at the offset frequency $\omega_0 + \Delta \omega$. The outer $\Gamma_L(\omega_0, t)$ circles are generated by the larger injected power at $\omega_0 + \Delta \omega$.

The dashed line represents the extracted $\Gamma_L(\omega_0, t)$ loci obtained when accounting for all sideband tones (center tone plus all SSB tones). The solid line corresponds to the $\Gamma_L(\omega_0, t)$ loci obtained when considering only the two dominant tones $(\omega_0, \omega_0 + \Delta \omega)$. As expected, the latter one (based on Eq. (4.9)) is a good approximation to the former (Eq. (4.10)) at low power levels. For accuracy the followed contour plots (e.g., PAE) will be based on $\Gamma_L(\omega_0, t)$ produced by Eq. (4.10).

The output power contour plot in Fig. 4.5 is generated using the database of RF output power $P_{out}(\omega_0, t)$ determined by Eq. (4.11) versus the extracted reflection coefficient $\Gamma_L(\omega_0, t)$.

Fig. 4.5 Output power contour obtained from the $(\omega_0+\Delta \omega)$ real-time swept phase measurements.
In Fig. 4.6 the PAE contour is also generated on the Smith chart plane of $\Gamma_{\omega_0}(\omega_0, t)$. For computing the PAE, the total DC power dissipation is estimated using a least square fit method to remove the effect of the scope discretization noise in the small variation of the DUT’s DC drain current and voltage. Good candidate impedances in Fig.4.6, such as the case Z marked by a black dot, can be selected for achieving high PAE while keeping a large output power.

Some areas with PAE higher than the case Z (80%) are observed in Fig. 4.6. However when referring to Fig. 4.7, one can identify those termination impedances to be potentially unstable because the corresponding magnitude of $\Gamma_{\omega_0}(\omega_0)$ is greater than one, indicating a negative input impedance which could lead to potentially unstable operation.
Fig. 4.7 $|\Gamma_{in}(\omega_0)|$ contour obtained from the $(\omega_0+\Delta\omega)$ real-time swept phase measurements.

Only the candidates with positive input impedances are investigated in this study. So three typical cases (X, Y, Z) are selected from the PAE contour plot in Fig. 4.6 for comparison as shown in Table 4.1.

For each of these three cases, the PAE and output power data extracted from the real-time swept phase measurement correlates to the results obtained from the constant phase measurement. Note that in the constant phase measurement the ESG source injects the 2GHz fundamental signal at the drain output without any frequency offset.

<table>
<thead>
<tr>
<th>$\Gamma_{L}(\omega_0)$</th>
<th>PAE (%)</th>
<th>Output Power (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Swept Phase</td>
<td>Constant Phase</td>
</tr>
<tr>
<td>Case X: 0°</td>
<td>47.9</td>
<td>49.1</td>
</tr>
<tr>
<td>Case Y: 0.2°</td>
<td>55.4</td>
<td>57.6</td>
</tr>
<tr>
<td>Case Z: 0.53°</td>
<td>80.0</td>
<td>70.6</td>
</tr>
</tbody>
</table>

Table 4.1 Comparison of three typical cases in Fig. 4.6: case X, Y, Z.
One can observe in Table 4.1 the difference brought about by memory effects in real-time tunings. In the case Z, higher PAE is extracted from the swept phase measurement than that obtained from the constant phase measurement, due to the large swept power at \((\omega_0 + \Delta\omega)\). For case X or case Y, the PAE difference is less between the swept and constant phase measurement because smaller power at \((\omega_0 + \Delta\omega)\) is applied.

Due to the high PAE (70.6 %) and stability consideration, the load reflection coefficient of the case Z is chosen as the optimum. The other two cases (X and Y) will be used latter for comparison.

### 4.4.2 Second Harmonic Real-time Active Load-pull

As described in previous sections, the second harmonic real-time tuning uses the PSG source for injecting \((2\omega_0 + \Delta\omega)\) at the DUT output, whereas the ESG source still provides the 2GHz \((\omega_0)\) excitation at the DUT input.

![Loci of \(\Gamma_L(2\omega_0, t)\) obtained from the \((2\omega_0+\Delta\omega)\) real-time swept phase measurements using Eq. (4.9) (solid line) and Eq. (4.10) (dashed line).](image)

Fig. 4.8 Loci of \(\Gamma_L(2\omega_0, t)\) obtained from the \((2\omega_0+\Delta\omega)\) real-time swept phase measurements using Eq. (4.9) (solid line) and Eq. (4.10) (dashed line).
Based on the previously selected optimal load (case Z) at $\omega_h$, the second harmonic real-time ALP measurement generates the loci of extracted second harmonic reflection coefficients in Fig. 4.8.

Both PAE and output power contours are shown in Fig. 4.9 and Fig. 4.10. In agreement with the prediction of class F PA design theory, the realistic second harmonic termination with the highest PAE (case A) is closed to the SHORT and almost reaches the edge of the Smith chart. This high PAE is verified from the constant phase measurement to be 72.03%. Its corresponding output power is 57.7mW and the gain is 16.93 dB.

Fig. 4.9  PAE contour plot in the $\Gamma_L(2\omega_0)$ plane, obtained from the $(2\omega_0+\Delta\omega)$ real-time swept phase measurements.
Fig. 4.10 Output power contour plot in the $\Gamma_L(2\omega_0)$ plane obtained from the $(2\omega_0+\Delta\omega)$ real-time swept phase measurements.

<table>
<thead>
<tr>
<th>$\Gamma_L(\omega_0)$</th>
<th>PAE (%)</th>
<th>Output Power (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Swept Phase</td>
<td>Constant Phase</td>
</tr>
<tr>
<td>Case A: $0.985 \angle -156^\circ$</td>
<td>74.95</td>
<td>72.03</td>
</tr>
<tr>
<td>Case B: $0.976 \angle -180^\circ$</td>
<td>74.18</td>
<td>71.82</td>
</tr>
<tr>
<td>Case C: 0</td>
<td>67.13</td>
<td>66.47</td>
</tr>
</tbody>
</table>

Table 4.2 Comparison of three typical cases in Fig. 4.9: case A, B, C.

In Table 4.2 three typical cases (A, B, C) are picked out from the PAE contours in Fig. 4.9 for comparison. For the constant phase measurement the PSG source injects simply a $2\omega_0$ signal to the DUT output. In each of these three cases, both the PAE and output power results calculated from the real-time swept phase measurement are consistent with those from the constant phase measurement. The degradations of PAE and output power from the swept phase to constant phase measurement are much less than those in Table 4.1. This fact indicates that the memory effect brought about by the
200 KHz frequency is prominent only at the fundamental frequency rather than in the second harmonic.

The performance improvement achieved from controlling the second harmonic termination is further revealed in Table 4.3, which shows the results from different combinations of fundamental and second harmonic load conditions.

<table>
<thead>
<tr>
<th>Loadline</th>
<th>$\Gamma_L(\omega_0)$</th>
<th>$\Gamma_L(2\omega_0)$</th>
<th>PAE (%)</th>
<th>Output Power (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case L1</td>
<td>$0.53 \angle 19.3^\circ$</td>
<td>$0.985 \angle -156^\circ$</td>
<td>72.03</td>
<td>57.7</td>
</tr>
<tr>
<td>Case L2</td>
<td>$0.2 \angle 0^\circ$</td>
<td>$0.99 \angle 126^\circ$</td>
<td>65.69</td>
<td>88.9</td>
</tr>
<tr>
<td>Case L3</td>
<td>$0$</td>
<td>$0.98 \angle 156^\circ$</td>
<td>58.12</td>
<td>96.5</td>
</tr>
<tr>
<td>Case L4</td>
<td>$0$</td>
<td>$0$</td>
<td>51.31</td>
<td>76.8</td>
</tr>
</tbody>
</table>

Table 4.3 Comparison of the four cases of loadline in Fig. 4.11. Note: the case L1 is same as the case A in Table 4.2.

Due to the trade-off between the PAE and output power, a designer can choose the combination satisfying the design requirement, with either an emphasis on high PAE (case L1), high output power (case L3) or a compromise between the two (case L2).

Fig. 4.11 RF loadline comparison for the four typical cases in Table 4.3.
The associated RF loadlines in Fig. 4.11 clearly show the trade-off between the PAE and output power. For the case L1, PAE is high due to the high drain voltage swing and the low average drain current, which reduces the DC power consumption. The case L3 has larger drain current swing and obtains higher output power consequently.

Fig. 4.12 DUT drain current and voltage of the four cases in Table 4.3.

Fig. 4.13 Instantaneous product of DUT drain current times drain voltage.

Fig. 4.12 shows the drain voltage and current for each of the cases in Table 4.3. Obviously the overlap between the time-domain drain voltage and current waveform is minimized for the case L1, leading to the highest 72.03% PAE in Table 4.3. The
instantaneous power dissipation of the transistor itself is displayed in Fig. 4.13, which is also consistent with the PAE results in Table 4.3.

4.4.3 Third Harmonic Real-time Active Load-pull

The third harmonic real-time ALP measurement utilizes the optimized load conditions acquired from the previous real-time ALP tests at the fundamental and second harmonic. The ESG source gives the 2GHz \( \omega_0 \) excitation at the DUT input. The second harmonic \( 2\omega_0 \) and the third harmonic with frequency offset \( (3\omega_0 + \Delta \omega) \) are injected by the two harmonic sources to the DUT output. The load tuner is properly adjusted to the optimal position.

Based on the optimal case A in Table 4.2, the third harmonic swept phase measurement generates the extracted \( \Gamma_L(3\omega_0,t) \), covering the whole Smith chart in Fig. 4.14. With the Smith chart mapped, we can construct the PAE (Fig. 4.15) and output

![Fig. 4.14 Loci of \( \Gamma_L(3\omega_0,t) \) obtained from the \( (3\omega_0 + \Delta \omega) \) real-time swept phase measurements using Eq. (4.9) (solid line) and Eq. (4.10) (dashed line).](image)
power (Fig. 4.16) contour plots based on the third harmonic reflection coefficient plane using the same method described before for the fundamental and second harmonic.

Fig. 4.15 PAE contour plot in the $\Gamma_L(3\omega_0)$ plane obtained from the $(3\omega_0+\Delta\omega)$ real-time swept phase measurements.

Fig. 4.16 Output power contour plot in the $\Gamma_L(3\omega_0)$ plane obtained from the $(3\omega_0+\Delta\omega)$ real-time swept phase measurements.
In Fig. 4.15 the high PAE (around 80%) contour lines are mainly distributed around the rightmost part of the smith chart. From this contour, the optimum for class F is selected to be case W with $\Gamma_L(3\omega_0)$ of $0.97 \angle 17.3^\circ$, which is close to the edge of Smith chart and achieves higher efficiency than the OPEN impedance does.

The resulting constant phase measurement of case W leads PAE to be 80.96%, which improves by 8.9% the result for case A (best PAE for the second harmonic tuning). Its corresponding output power and gain are 65mW and 16.33dB respectively.

The design choice for case W is consistent with the class F PA theory, which demands that the optimal third harmonic termination be an open, or in practice a highly reactive load.

4.5 A Complete pHEMT PA Design with Multi-harmonic RT-ALP Technique

The proposed multi-harmonic RT-ALP has demonstrated its capability of facilitating high efficiency PA designs, by achieving a PAE of 80% for a GaN device. This section will describe a complete PA design with a pHEMT transistor (ATF-54143) using the RT-ALP technique to reach PAE as high as 75% at 2GHz.

The RT-ALP system in Fig. 4.2 is slightly adapted to realize a connectorized setup: cables are added to replace the two probes to fit in the connectorized pHEMT board, which hosts the packaged ATF-54143 transistor and bias. For the class F operation, the quiescent DC bias is around its threshold voltage ($V_{DS} = 3.0V$, $V_{GS}= 0.31V$). In this study the LSNA acquired spectral data up to the 4th harmonic each with 99 tones (SSB = 49). The fundamental frequency is 2 GHz and modulation frequency $\Delta f$ is 200 kHz.
With the RT-ALP first run at $f_0=2$ GHz at input power of 6.5 dBm, the optimal load at fundamental frequency is selected as $\Gamma_L(\omega_0, t) = -0.2$ to form the basis for the further RT-ALP tunings at $2f_0$ and $3f_0$.

Fig. 4.17 illustrates the extracted $\Gamma_L(2\omega_0, t)$ result from the 2\textsuperscript{nd} harmonic RT-ALP data at 4 GHz. The dashed line loci are obtained when accounting for all sideband tones.

![Fig. 4.17 Loci of $\Gamma_L(2\omega_0, t)$ obtained from the $(2\omega_0+\Delta\omega)$ real-time swept phase measurements by accounting for the two dominant tones (solid line) or all the sideband tones (dashed line) with Eq. (4.10). Each circle is measured in 10 ms.](image)

Fig. 4.17 Loci of $\Gamma_L(2\omega_0, t)$ obtained from the $(2\omega_0+\Delta\omega)$ real-time swept phase measurements by accounting for the two dominant tones (solid line) or all the sideband tones (dashed line) with Eq. (4.10). Each circle is measured in 10 ms.

![Fig. 4.18 PAE contour plot in the $\Gamma_L(2\omega_0)$ plane, obtained from the $(2\omega_0+\Delta\omega)$ real-time swept phase measurements (based on dashed line contour in Fig. 4.17).](image)

Fig. 4.18 PAE contour plot in the $\Gamma_L(2\omega_0)$ plane, obtained from the $(2\omega_0+\Delta\omega)$ real-time swept phase measurements (based on dashed line contour in Fig. 4.17).
based on Eq. (4.10), while the solid line loci are obtained only considering the two dominant tones. At low power levels the latter one is a good approximation to the former as expected.

The critical PAE contour for design decision is shown in Fig. 4.18. As can be seen, the realistic 2\textsuperscript{nd} harmonic impedance for class F with the highest PAE (case A) is different from the ideal SHORT and almost reaches the edge of the Smith chart. This high PAE is verified from the constant phase measurement to be 71.92\% with an output power of 60.8 mW.

Table 4.4 lists the three typical cases (A, B, C) of the PAE contours in Fig. 4.18 selected for comparison. In each case both the PAE and output power results from the RT-ALP are consistent with those from the constant phase measurement. The small difference indicates the device’s memory effect is small for the 200 kHz modulation frequency used in RT-ALP.

With the RT-ALP tuning at 3f_0, it was found out that the performance improvement from controlling the 3\textsuperscript{rd} harmonic is almost insignificant for this particular device. The resulting optimal load terminations for the output matching are then determined as:

\[
\Gamma_L(\omega_0, t) = -0.2, \quad \Gamma_L(2\omega_0, t) = 0.6 + j0.7, \quad \Gamma_L(3\omega_0, t) = 0.30 - j0.85.
\]

<table>
<thead>
<tr>
<th>\Gamma_L(2\omega_0)</th>
<th>PAE (%)</th>
<th>Output Power (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Swept Phase</td>
<td>Constant Phase</td>
</tr>
<tr>
<td>Case A (optimal 0.6+j0.7)</td>
<td>77.04</td>
<td>71.92</td>
</tr>
<tr>
<td>Case B (short)</td>
<td>62.70</td>
<td>63.48</td>
</tr>
<tr>
<td>Case C (50 Ohm)</td>
<td>60.44</td>
<td>61.90</td>
</tr>
</tbody>
</table>

Table 4.4 Comparison of three typical cases in Fig. 4.18: case A, B, C.
Note: The transistor’s input power remains as 6.5 dBm at 2 GHz.
The PA output matching network is designed to implement the optimal reflection coefficients predicted by RT-ALP. The S-parameter of output matching at \( f_0 \), \( 2f_0 \) and \( 3f_0 \) frequencies are shown in Fig. 4.19 (a). The layout is realized with microstrip substrate of Rogers 5880 Duroid \((\varepsilon_r=2.2, H=31\text{mil})\) using two open stubs (Fig. 4.19 (b)). The source matching network is a conjugate match of the input impedance for transistor.

Fig. 4.19 Output matching network to supply the optimal reflection coefficients predicted by RT-ALP: (a) \( S_{11} \) at \( f_0 \), \( 2f_0 \) and \( 3f_0 \) frequency (marker 1, 2 and 3 respectively) (b) layout (left end to transistor and right end to 50 \( \Omega \)).
Fig. 4.20 Simplified schematic of the designed pHEMT PA.

Fig. 4.20 illustrates the fabricated pHEMT power amplifier, with the measurement reference planes still de-embedded to the transistor’s gate and drain ports. The red loadline in Fig. 4.21 is acquired from the final constant phase measurement of the completed pHEMT PA board. The single optimal swept loadline (green) is shown with a group (blue) of swept RF load lines in its background. Indeed the measured final red loadline (constant phase) matches well to the green optimal one (swept phase), which is from the predicted optimal impedance condition (case A in Table 4.4).

Fig. 4.21 RF load lines of the transistor for swept phase (blue) with the optimal one (green) and the final constant phase load line(red).
Note that the overlap is small between the time-domain drain voltage and current waveform (Fig. 4.22(a)). It leads to the instantaneous power dissipation of the transistor itself shown in Fig. 4.22(b) balancing each other with the positive and negative areas, which is consistent with the high PAE result.

Under the input power of 6.5 dBm at 2 GHz, the PA achieves PAE of 68.5% with 64.1 mW fundamental output power and 15.9 dB gain. The PAE and Pout results are very close to the findings in Table 4.4, revealing the reliability of the RT-ALP design methodology.

Fig. 4.22 Waveforms of (a) drain voltage and current of the transistor (b) Instantaneous product of drain voltage times drain current.
From the power sweeping measurement result in Fig. 4.23, we can observe a PAE of 68.5% with 18 dBm output power and around 16 dB gain at 2 GHz. Below the 1dB compression point, this PA achieves a PAE up to 74.6% with 18.6 dBm output power.

4.6 Summary

A novel multi-harmonic real-time active load-pull technique with supportive theory is proposed, so as to efficiently explore the impact of the harmonic loading conditions on class F PA designs. It eliminates the need of harmonic tuners and has fast tuning capability to cover the entire Smith chart, at both the fundamental ($f_0$) and harmonic (2$f_0$ and 3$f_0$) frequencies.

A wide range of harmonic load reflection coefficients can be properly synthesized, permitting the fast acquisition of reliable large-signal data that generates the RF dynamic loadlines, PAE and power contour plots for guiding the designs of non-linear class F PAs.
With the RT-ALP technique, a GaN device demonstrates a power added efficiency of 80.96% at 2 GHz by tuning up to the third harmonic. A pHEMT PA is designed and fabricated with matching networks based on the optimal impedances predicted by the RT-ALP technique. The measurement result of 68.5% PAE at 2 GHz is a good agreement (around 3% difference) with the RT-ALP prediction.

This work demonstrates the efficacy and reliability of the proposed multi-harmonic real-time tuning for the interactive design of power efficient PAs.
CHAPTER 5

A 3.5 GHz CMOS DOHERTY POWER AMPLIFIER WITH INTEGRATED DIODE LINEARIZER TARGETED FOR POTENTIAL WiMAX APPLICATION

5.1 Introduction

In recent years integrated CMOS RF frond-end circuit designs have drawn enormous research efforts, particularly driven by the consumer mobile markets. Highly integrated CMOS transceivers comprising of LNA, VCO and mixer [5.1][5.2][5.3] have been successfully implemented to satisfy the strong need of low cost and small form-factor, which are indeed the core initiatives of the appealing system-on-chip (SOC) solution [5.4][5.5]. The challenges of designing fully integrated RF CMOS PA on the same die of transceiver, however, escalate as the state-of-the-art deep-submicron processes scale down remarkably under “Moore’s Law” trend.

With the shrinking minimum feature size, the CMOS processes achieve faster operation speed and already reach cutoff frequency higher than 40 GHz (e.g. 90 nm process) [5.5] encouraging for RFIC designs. Unfortunately another effect of scale-down is the resulting lower breakdown voltage and higher knee voltage [5.6], which significantly reduce the voltage swing headroom at the device output (drain) node,
causing transistors easier to be stressed or damaged. This reduced voltage swing range also requires PA transistors to drive small load impedance under rated power, asking for a matching network with large transformation ratio. Furthermore the low resistivity of substrate layer in standard CMOS technology causes RF couplings, which brings losses for PA, introduces more parasitics to designs and may generate unwanted influence (e.g. LO pulling to VCO) to other on the same CMOS die. The issue of substrate loss also leads to low quality-factor (Q) of on-chip passive particularly the planar spiral inductors. With higher cost process the improved Q can reach larger than 10 using top thick metal option for inductors. The lack of precise large-signal CMOS RF models also affects the accuracy of simulations in PA designs.

On the other hand, emerging standards for personal wireless connectivity impose stringent requirements on RF power amplifiers. Worldwide Interoperability for Microwave Access (WiMAX) is an uprising wireless communication standard (IEEE 802.16) for defining the broadband wireless access over a wide metropolitan area [5.7] [5.8]. It uses orthogonal frequency division multiplexing (OFDM) to offer high-speed data rate and strong immunity to multi-path fading and narrow-band interference. Due to the OFDM modulation, its resulting signal has a large crest factor that demands PAs to be highly linear.

In addition power amplifiers used in WiMAX handsets or CPE (Customer Premises Equipment) need to have high efficiency to save battery power. However, the linearity specifications are often achieved by backing off the output power of PAs, causing a large reduction in efficiency. Because the PA is the most power consuming block in a WiMAX TX/RX chain, the efficiency of power amplifiers become a critical design issue as it
strongly affects the battery operation time as well as determines the space/weight used for heat sinking.

Conventional techniques for PA efficiency enhancement include envelope elimination and restoration (EER), dynamic bias and Doherty PA [5.9] [5.10]. The major limits of EER are its circuit complexity and narrow-bandwidth [5.11]. Dynamic bias often needs additional DC-DC converter and requires complexity and resources from the digital signal processing (DSP) domain for effectively controlling the bias voltage [5.12] [5.13]. For the mobile handset/CPE, the Doherty PA is the most promising solution [5.14] due to its easy configuration and wide-bandwidth. However, the normal Doherty PA is limited by the linearity degradation from its peaking amplifier’s class C operation and carrier amplifier’s deep class AB operation. A compact Doherty PA [5.15] [5.16] also requires miniature implementation of the quarter-wave transmission line and input power division section.

This chapter presents a novel CMOS Doherty PA design for WiMAX at 3.5 GHz using standard 0.18μm TSMC process. A Doherty configuration with cascode transistors is adopted to achieve high efficiency and output power. Lumped matching components are utilized to replace the quarter-wave transmission line to reduce circuitry size. In this work the integrated diode linearizer [5.17] is first demonstrated with the cascode transistors for improving the linearity of Doherty PA. The proposed power amplifier provides a maximum output power of 24.5 dBm and power added efficiency (PAE) as high as 43% at 3.5 GHz operation frequency. At 1-dB compression point this PA exhibits around 23.5 dBm of output power with 36.1% PAE. The third order inter-modulation (IMD3) comparison obtained from two-tone test reveals the linearity improvement from
the diode linearizer. Layout implemented with the novel GSML methodology [5.18] and corner simulations results are also included.

5.2 Doherty PA Design and Implementation

5.2.1 Doherty PA with Integrated Diode Linearizer

![Fig. 5.1 Typical Doherty PA configuration.](image)

The conventional circuit configuration of a Doherty PA is repeated in Fig. 5.1. It consists of the carrier amplifier (PA1), peaking amplifier (PA2), quarter-wave (λ/4) transmission line, phase delay line and input divider. In practice PA1 and PA2 are typically biased as class AB and C respectively to balance the linearity and efficiency performance. In the low power mode, mainly the PA1 generates output power; in the medium and high power mode both PA1 and PA2 are operational, combining their power efficiently using the load modulation [5.14] and maintaining high efficiency within the power back-off range. However, the λ/4 line critical for the active load modulation effect does increase the circuit dimension. The whole Doherty PA’s linearity is also degraded...
due to the class C operation of the peaking amplifier (and carrier amplifier’s deep class AB operation).

Fig. 5.2 Proposed schematic of the CMOS Doherty PA with diode linearizers.

Fig. 5.2 shows the new CMOS Doherty PA design proposed. Both the carrier (NMOS $M_1 - M_2$) and peaking (NMOS $M_3 - M_4$) amplifier are configured with cascode thick oxide transistor to reduce the risk of oxide breakdown, allowing the use of larger supply voltage (3.3 V) helpful to achieve higher output power and better reverse isolation.

A diode connected NMOS transistor ($M_5$ or $M_6$) with bias resistors ($R_1$ - $R_2$ or $R_3$ - $R_4$) is tied to the gate of common source transistor ($M_1$ or $M_3$). Thus $R_1$ - $R_2$ - $M_5$ and $R_3$ - $R_4$ - $M_6$ implement a gate biasing circuit with linearization function for the carrier and peaking amplifier respectively. The linearization works by maintaining the gate bias voltage at the desired levels despite of the increasing input power [5.17]. The gate DC bias levels of $M_1$
and $M_3$ are prevented from dropping with the aid of the forward biased diodes of transistor $M_5$ and $M_6$ respectively.

For a compact realization, the $L$-$C$ lumped elements ($L_T$, $C_{T1}$, $C_{T2}$) forming a low-pass network are used to replace the quarter-wave transmission line. The corresponding approximation of inductance and capacitance are determined respectively by the two equations below, where $f_0$ is the operation frequency and $Z_T$ represents the characteristic impedance of the $\lambda/4$ transmission line:

$$L_T = \frac{Z_T}{2\pi f_0}$$  \hspace{1cm} (5.1)

$$C_{T1} = C_{T2} = \frac{1}{2\pi f_0 Z_T}$$  \hspace{1cm} (5.2)

The input matching networks of PA1 ($L_1$, $C_1$) and PA2 ($L_2$, $C_2$) are designed for matching to 100 Ohm for equal power split from the 50 Ohm input port. The PA1’s output matching network ($L_3$, $L_T$, $C_{T1}$, $C_{T2}$, $C_3$) insures an optimum resistance (around 13 Ohm) presented at the transistor drain node of the carrier amplifier. The output matching network of PA2 ($L_4$, $C_4$, $L_5$, $L_6$) is designed such that PA2 contributes RF signal amplification for input power entering into the medium level; in the low power mode operation it also provides PA1 with a high impedance at the power combining junction ($RF_{out}$ node) to avoid power leakage.

A short segment of off-chip phase compensation line is introduced to remove the bulky input Wilkinson power divider or hybrid coupler, saving space for small profile implementation. This compensation line works with the high-pass network ($L_4$, $C_4$, $C_5$)
network to synchronize the phase of carrier and peaking amplifier paths to get optimal merged power at the output port.

### 5.2.2 Ground Shielded Microstrip Line (GSML) Methodology

The Ground Shielded Microstrip Line (GSML) methodology [5.18] is a good approach to reduce the substrate coupling and accurately predict the parasitic effects (e.g. inductance and capacitance) from distributed interconnects.

![Cross section of a multi-metal-layer CMOS process.](image)

Fig. 5.3 Cross section of a multi-metal-layer CMOS process.

Fig. 5.3 displays the cross section of a multi metal layer process to demonstrate the GSML principle. CMOS process such as TSMC 0.18 μm technology consists of a few metal layers inter-spaced by SiO₂ dielectric layers as simplified in Fig. 5.3. If the
presence of the intermediate metal layers is neglected, the top-layer metal trace can be approximately considered as microstrip line. The bottom layer metal is grounded and acts as the ground plane. Then the middle SiO₂ layers are the dielectric layers for microstrip line. The thickness of this dielectric layer is around $6.5 \, \mu m$ for TSMC $0.18 \, \mu m$ process.

Once the above GSML approximation has been made, the layout design is carried out in such a way so that most of the inter device connections are made through the top layer interconnects. The other metal layers are kept to a minimum. The bottom metal layer is filled in densely and grounded to reduce substrate coupling and predict parasitics. Correspondingly the simulator is able to simulate the parasitics brought by transmission line interconnects. These GSML features can be seen in the next section.

### 5.2.3 Doherty PA Layout Implementation

![Fig. 5.4 Simplified transistor cell schematic with GSML methodology. Transmission lines are used to model the interconnections.](image)
The aforementioned GSML methodology is utilized to build the transistor cell and surrounding interconnects as shown in Fig. 5.4. In fact most of the inter device connections are made through the top metal layer and other metal layers are kept to a minimum. The bottom metal layer is filled in densely and grounded. In the absence of intermediate layers, the top-layer metal trace can be approximately considered a microstrip line. The bottom layer metal is grounded and acts as the ground plane. If the intermediate metal layers are absent, the dielectric $\text{SiO}_2$ layers between the top and bottom level metals acts as the dielectric layer of a micro-strip line.

In the transistor cell we can see the transmission line widths change from $2W_1$ to $W_1$ at the gate side, while varying from $W_2$ to $2W_2$ at the drain side. This feeding structure (corporate tree) improves the synchronization of traveling RF signal when they reach different transistor cells. Therefore it also improves the matching at the PA input and output.

The proposed complete PA layout is shown in Fig. 5.5. It passes DRC & LVS check in the Calibre tool of Mentor Graphics. In this design, transistor gate and drain lines are placed on high metal level (Metal 6). A large ground plane is introduced on the lower metal level (Metal 1) to both shield RF signal traces from the substrate coupling and implement transmission lines permitting the realization of interconnects with predictable parasitic values.

Multi-finger ($n=16$) structure is employed for the transistor unit cell to reduce the gate resistance. Multiple unit cells ($m=14$) are connected in parallel to form a transistor with large effective gate width, while using the optimum width of each unit cell which
provides the best high-frequency performance. For each unit cell, the source and bulk nodes are tied together to reduce body effect, which may cause threshold voltage variations. The deep N-well (DNW) option of the each TSMC RF NMOS transistor is chosen for better isolation from the substrate and improved RF performance [5.19].

To minimize the unwanted ground inductance (cause gain degradation) at the source
terminals of both the carrier and peaking PA stages, each stage adopts eight bondpads for
down-bonding connections to present a small inductance around 0.2 nH. To avoid the
substrate loss of on-chip low Q inductors, the matching inductors are implemented with
bondwire inductance simulated with bondwire models in Advanced Design System
(ADS). In addition, on-chip Metal-Insulator-Metal (MIM) decoupling capacitors are
added at the gate nodes of both M2 and M4 transistors to filter out AC ripples from the
imperfect DC power supplies. Dummy metals are also added around corners to satisfy the
metal density requirements.

5.3 Simulation Results

This section summarizes the results of harmonic balance simulations with the TSMC
design kit. As seen in Fig. 5.6, the proposed amplifier provides 11.9 dB of Gain,
maximum output power of 24.5 dBm and power added efficiency (PAE) as high as
42.73% at 3.5 GHz operation frequency. The 1-dB compression point of the Doherty PA

![Graph](image)

Fig. 5.6 Pout, Gain and PAE versus the input power at 3.5 GHz.

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Fig. 5.7 Comparison of IMD3: with and without linearizer.

is extended from that of a single carrier/peaking amplifier, exhibiting around 23.5 dBm of output power, while achieving 36.1% of PAE.

Fig. 5.7 displays the third order inter-modulation (IMD3) comparison obtained from the two-tone test (10 MHz spacing centered at 3.5 GHz), to demonstrate the linearity improvement brought about by using the diode linearizer. As expected, the circuit with

| m3 | freq=3.485GHz | Pout dBm=-32.776 |
| m1 | freq=3.495GHz | Pout dBm=10.147 |
| m2 | freq=3.505GHz | Pout dBm=9.777  |
| m4 | freq=3.515GHz | Pout dBm=-32.692 |

Fig. 5.8 Example of two-tone test spectrum for IMD3.
the diode linearizer achieves better overall IMD3 performance than that without the linearizer. In most of the power level range, the IMD3 improvement is about 1.1 dBC. For input power (Pin) from 2.5 to 7 dBm, the improvement of IMD3 is significant reaching 5.75 dBC.

Fig. 5.8 demonstrates an example of output spectrum in two tone test for calculating IMD3. The IMD3 level of upper side band and lower side band are slightly different as expected.

To account for the statistical CMOS process variations that affect physical parameters such as the threshold voltage, channel length and width, it is necessary to run corner simulations for evaluating their impact. Fig. 5.9 to 5.11 show the simulation results for Gain, Pout and PAE with typical, fast and slow process corner parameters respectively.

![Gain simulation at corner parameters.](image)

In Fig. 5.9 a drop in the gain is observed at slow process parameter, while it increases 1.8 dB reaching 13.7 dB for fast corner as expected. With the input power getting higher
than 10 dBm, the gain of fast corner reduces more dramatically than the case of the typical and slow corners.

Fig. 5.10 Output power simulation at corner parameters.

In Fig. 5.10, the P1dB output power of typical corner (23.3 dBm) is in between the P1dB compression point of the fast (23.6 dBm) and slow (22.3 dBm) corners. For fast corner the output power rising slope gets to decline earlier than the typical or slow corner does, consistent with the gain result in Fig. 5.9. Displayed in Fig. 11, the PAE of slow

Fig. 5.11 PAE simulation at corner parameters.
corner exhibits degradation in the medium power range, while still achieving up to 40% efficiency when input power is high enough. Overall the PAE at maximum output power is around 6% higher than the PAE at P1dB. The key results of corner simulations are summarized accordingly in the following Table 5.1.

<table>
<thead>
<tr>
<th>Corner</th>
<th>Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Gain (dB)</td>
</tr>
<tr>
<td>Typical</td>
<td>11.9</td>
</tr>
<tr>
<td>Fast</td>
<td>13.7</td>
</tr>
<tr>
<td>Slow</td>
<td>9.4</td>
</tr>
</tbody>
</table>

Table 5.1 Summary of corner simulations.

Fig. 5.12 Simulated Pout, Gain and PAE versus supply voltage variation for input power of 12 dBm at 3.5 GHz.
As revealed in Fig. 5.12, the performance of the PA is also simulated as a function of the DC supply voltage (Vdd) with ±10 percent variation. The output power and gain are observed to be proportional to the supply voltage variation while the PAE drops slightly with Vdd increasing, which is consistent with the tradeoff between PAE and gain.

![Figure 5.13](image)

**Fig. 5.13** Simulated Pout, Gain and PAE versus frequency for input power of 12 dBm.

In Fig. 5.13 the PA performance is also simulated as a function of operation frequency. Note that the gain remains almost flat over the band from 3.3 to 3.6 GHz. The output power has around 1dB variation within the band. Due to the difference in DC power consumption, the PAE varies from 30% at 3.6 GHz to 37.5% at 3.45 GHz. For the nominal 3.5 GHz the proposed PA achieves around 36%.
5.4 Summary

In this work, a novel integrated Doherty power amplifier in 0.18 μm CMOS process has been demonstrated. The advantages of this designed CMOS Doherty PA are summarized:

A) Integrated diode linearizer for linearity improvement of cascode Doherty PA at 3.5 GHz WiMAX frequency band.

B) Layout implementation with GSML methodology.

C) High efficiency at the extended high P1dB.

D) Replacement of quarter-wave transmission with lumped elements.

E) Removal of bulky power divider or hybrid coupler at PA input.

<table>
<thead>
<tr>
<th>Reference Number</th>
<th>Freq (GHz)</th>
<th>Semiconductor Process</th>
<th>Vdd (V)</th>
<th>P1dB (dBm)</th>
<th>Gain (dB)</th>
<th>PAE @ P1dB</th>
</tr>
</thead>
<tbody>
<tr>
<td>[5.20]</td>
<td>1.75</td>
<td>0.5 μm CMOS</td>
<td>3.3</td>
<td>24</td>
<td>23.9</td>
<td>29%</td>
</tr>
<tr>
<td>[5.21]</td>
<td>2.4</td>
<td>0.35 μm CMOS</td>
<td>1</td>
<td>18</td>
<td>NA</td>
<td>33%</td>
</tr>
<tr>
<td>[5.22]</td>
<td>5</td>
<td>0.18 μm CMOS</td>
<td>1.8</td>
<td>19.2</td>
<td>7.1</td>
<td>18%</td>
</tr>
<tr>
<td>[5.23]</td>
<td>1.9</td>
<td>0.18 μm CMOS</td>
<td>3.3</td>
<td>23</td>
<td>16</td>
<td>23%</td>
</tr>
<tr>
<td>[5.24]</td>
<td>2.4</td>
<td>0.18 μm CMOS</td>
<td>3.3</td>
<td>8</td>
<td>11</td>
<td>25%</td>
</tr>
<tr>
<td>This work</td>
<td>3.5</td>
<td>0.18 μm CMOS</td>
<td>3.3</td>
<td>23.5</td>
<td>12</td>
<td>36%</td>
</tr>
</tbody>
</table>

Table 5.2 Comparison with previously reported CMOS power amplifiers.

ADS harmonic balance and corner simulations were utilized to evaluate the PA performance and robustness. The integrated diode linearizer improves the IMD3 performance by up to nearly 6 dB. PA layout was implemented using the GSML
methodology for reliable parasitics control and passed all the DRC and LVS checks. The performance parameters of this work are compared with previous reported results of CMOS power amplifiers. Among all the reported work in Table 5.2, the proposed Doherty configuration with cascode transistors achieves good P1dB (23.5 dBm) at high operation frequency (3.5 GHz) with the highest PAE (36%).
CHAPTER 6

CONCLUSIONS

In this dissertation, the switching mode class E non-linear PA is first investigated. Analysis and design equations based on the classical assumptions are given. The ideal drain voltage and current waveforms are shaped to be non-overlapping to maximize PA efficiency. To overcome the non-ideal factors such as finite RF choke inductance, load-pull simulations are utilized in this work to improve the design of a pHEMT class E PA. Simulation results show the contours of PA efficiency and output power to find the nominal load impedances that achieve high efficiency. Transistor voltage and current waveforms are studied with the instantaneous RF loadlines simulated as well. The designed class E PA is able to maintain PAE between 57.5% and 59.3% even though the supply voltage changes from 2 to 3 V.

One focus of this dissertation is the novel multi-harmonic real-time active load-pull for high efficiency non-linear PA designs. This multi-harmonic RT-ALP system is proposed with a supporting theory and successfully implemented based on the large signal network analyzer. The real-time tunings at second and third harmonic frequencies enable to quickly synthesize a wide range of harmonic load reflection coefficients.
without stability issue due to the open-loop structure. Fast acquisition of reliable large-signal data is available to generate the RF dynamic loadlines, PAE and power contour plots for guiding the design of non-linear power amplifiers. With this RT-ALP technique, a GaN device is chosen to explore the impact of the multi-harmonic loading conditions on non-linear class F PA, demonstrating a power added efficiency of 81% at 2 GHz by tuning up to the third harmonic. Furthermore, a pHEMT PA is designed and constructed with matching networks based on the optimal impedances predicted by the RT-ALP technique. The measurement result of 68.5% PAE at 2 GHz is in good agreement (around 3% difference) with the RT-ALP prediction, demonstrating the efficacy and reliability of the proposed multi-harmonic RT-ALP for the interactive design of power efficient PAs.

In this work, a novel integrated Doherty power amplifier in 0.18 μm CMOS process has been designed for the 3.5 GHz WiMAX. The Doherty configuration with cascode transistors help to achieve high efficiency and output power. Lumped LC components are used to replace the bulky quarter-wave transmission line for miniaturization purpose. Integrated diode linearizers are added at the transistor gates to improve the linearity of Doherty PA. Layout is implemented with the novel GSML methodology [12] for reliable parasitics control and passes all the DRC and LVS checks. The simulation results show a maximum output power of 24.5 dBm and power added efficiency (PAE) as high as 43% at 3.5 GHz. This CMOS Doherty PA exhibits around 23.5 dBm of output power at P1dB with 36.1% PAE achieved. Two-tone tests for IMD3 reveal the linearity improvement from the diode linearizers. To the author’s knowledge, this is the first work of CMOS Doherty PA with integrated diode linearizer targeting at the potential WiMAX band of 3.5 GHz.
APPENDIX A

EQUATION RE-DERIVATION FOR SIMPLIFIED CLASS E PA ANALYSIS

The following equations are derived to study the Cripps’ simplified theory of class E amplifier [1.6] as well as investigate its switching mode operation. Corrections are found out about for the published equations in [1.6] and the re-derived equations match well to corresponding plots for clarifications.

The configuration of a basic class E power amplifier is shown in the Fig. A.1. The transistor approximates an on/off switch S, showing infinite “off” impedance and zero “on” impedance in ideal case. The switch S is in parallel with the capacitor \( C_p \). Behaving like a constant current source, the RF choke inductor \( L_1 \) connects the switch to supply voltage \( (V_{dc}) \). Consisting of the inductor \( L_s \) and capacitor \( C_s \), the series resonant circuit is tuned to the input signal frequency. \( R_L \) is the load resistance that could result from the impedance transformation of standard 50 Ohm load.

The Q-factor of the resonator is assumed to be high enough, so that only a sinusoidal wave of current flows on the \( L_s - C_s - R \) branch. The RF choke inductor \( L_1 \) ensures no
current variation exists on the $I_{dc}$ branch. Then one can get the following current equation for $i(\theta)$, the combined total current from the switch (S) and capacitor ($C_p$),

$$i(\theta) = I_{ef} \sin \theta + I_{dc} \quad (\theta = \omega t)$$

(A.1)

where the $I_{dc}$ is the value of DC current component and $I_{ef}$ is the amplitude of the current sine-wave. The values of $I_{dc}$ and $I_{ef}$ are to be determined in the latter part.

As shown in Fig. A.2, the current waveform of $i(\theta)$ can be separated into two parts, $i_{sw}(\theta)$ and $i_c(\theta)$. They are the transistor switch current and capacitor current respectively. When the switch is off, $i(\theta)$ flows entirely into the capacitor ($C_p$) and generates $i_c(\theta)$. When the switch is on, $i(\theta)$ only flows through the switch (S) and generates $i_{sw}(\theta)$. 

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Fig. A.2 Class E power amplifier voltage and current waveforms.

From the Fig. A.2 one can observe the switch turns off at $\theta = \alpha$ and turns on at $\theta = \beta$. The capacitor voltage $v_c(\theta)$ is the integral result of the current $i_c(\theta)$ going through $C_p$.

\[ i_c(\theta) = I_{dc} + I_{rf} \sin \theta \quad \alpha < \theta < \beta \]  
\[ = 0 \quad \beta - 2\pi < \theta < \alpha \]  

\[ v_c(\theta) = \frac{1}{\alpha C_p} \int_{\beta - 2\pi}^{\theta} i_c(\theta) d\theta \]  

(A.2)  

(A.3)
Two values, $\beta$ and $\gamma$, label the zero crossing points of the capacitor current $i_c(\theta)$ in Fig. A.2. To determine value of $\beta$ for latter analysis, one can get

$$I_{dc} + I_{rf} \sin \theta = 0$$  \hspace{1cm} (A.4)

or

$$\sin \beta = -\frac{I_{dc}}{I_{rf}} \quad (\frac{3}{2} \pi < \beta < 2\pi)$$  \hspace{1cm} (A.5)

To find the relation between $I_{rf}$ and $I_{dc}$, one can use the property that the capacitor $C_p$ has zero mean DC current over an entire RF cycle:

$$I_{dc} = \frac{1}{2\pi} \int_{\pi - 2\pi}^{\alpha} (I_{dc} + I_{rf} \sin(\theta))d\theta$$  \hspace{1cm} (A.6)

After rearranging the integration result, one can get

$$\frac{I_{dc}}{I_{rf}} = \frac{\cos \beta - \cos \alpha}{\beta - \alpha}$$  \hspace{1cm} (A.7)

utilizing (A.5) and (A.7) together, one can get

$$\sin \beta = \frac{\cos \beta - \cos \alpha}{\alpha - \beta}$$  \hspace{1cm} (A.8)

Apparently the peak value for current $i(\theta)$ is

$$I_{pk} = I_{rf} + I_{dc}$$  \hspace{1cm} (A.9)

assigning a ratio $\tau$

$$\tau = \frac{I_{dc}}{I_{rf}} = -\sin \beta$$  \hspace{1cm} (A.10)

then one can get

$$I_{dc} = \frac{I_{pk}}{1 + \frac{1}{\tau}}$$  \hspace{1cm} (A.11)
and \[ I_{rf} = \frac{I_{pk}}{1 + \tau} \quad (A.12) \]

Now the voltage of capacitor \( C_p \) can be determined as followings.

\[
v_c(\theta) = \frac{1}{\pi C_p} \int_\alpha^{\beta} \left[ I_{dc} + I_{rf} \sin \theta \right] d\theta \quad \alpha < \theta < \beta
\]

\[ = 0 \quad \beta - 2\pi < \theta < \alpha \quad (A.13)\]

\[
v_c(\theta) = \frac{1}{\pi C_p} \left[ I_{dc} (\theta - \alpha) + I_{rf} (\cos \alpha - \cos \theta) \right] \quad \alpha < \theta < \beta
\]

\[ = 0 \quad \beta - 2\pi < \theta < \alpha \quad (A.14)\]

The mean DC component of the capacitor voltage \( v_c(\theta) \) is determined by the following integral:

\[
V_{dc} = \frac{1}{2\pi} \int_\alpha^{\beta} v_c(\theta) d\theta
\]

\[ = \frac{1}{2\pi \pi C_p} \int_\alpha^{\beta} \left[ I_{dc} (\theta - \alpha) + I_{rf} \cos \alpha - I_{rf} \cos \theta \right] d\theta
\]

\[ = \frac{1}{2\pi \pi C_p} \left[ (\beta - \alpha) (I_{rf} \cos \alpha - I_{dc} \alpha) + \frac{1}{2} I_{dc} (\beta^2 - \alpha^2) - I_{rf} (\sin \beta - \sin \alpha) \right] \quad (A.15)\]

From (A.10) one can get

\[ I_{dc} = -I_{rf} \sin \beta \quad (A.16)\]

Substituting (A.16) to (A.15) one can get

\[
\frac{2\pi \pi C_p}{I_{rf}} V_{dc} = (\cos \alpha + \alpha \sin \beta) (\beta - \alpha) - \frac{1}{2} \sin \beta (\beta^2 - \alpha^2) - (\sin \beta - \sin \alpha)
\]

\[ = (\beta - \alpha) \cos \alpha + ((\alpha - \beta) \sin \beta) [\alpha - \frac{1}{2} (\beta + \alpha)] - \sin \beta + \sin \alpha
\]

\[ = \frac{1}{2} (\beta - \alpha)(\cos \beta + \cos \alpha) + \sin \alpha - \sin \beta \quad (A.17)\]
Therefore, the final expression for the capacitor \( (C_p) \) DC component voltage \( (V_{dc}) \) is

\[
V_{dc} = \frac{1}{\omega C_p} I_{pk} v_{dc}(\alpha)
\]

(A.18)

\[
v_{dc}(\alpha) = \frac{I_{rf}}{2 \pi I_{pk}} \left[ \frac{1}{2} (\beta - \alpha)(\cos \beta + \cos \alpha) + \sin \alpha - \sin \beta \right]
\]

(A.19)

where \( v_{dc}(\alpha) \) is the normalized function of a certain conduction angle \( \alpha \) for unity \( I_{pk} \).

The in-phase fundamental component \( (V_{ci}) \) of the capacitor (and transistor switch) voltage is used to calculate the RF load resistor. \( V_{ci} \) is basically determined by the following integral:

\[
V_{ci} = \frac{1}{\pi} \int_{\alpha}^{\beta} v_c(\theta) \sin \theta d\theta
\]

\[
= \frac{1}{\pi \omega C_p} \int_{\alpha}^{\beta} \left[ I_{dc}(\theta - \alpha) + I_{rf} \cos \alpha - I_{rf} \cos \theta \right] \sin \theta d\theta
\]

\[
= -\frac{1}{\pi \omega C_p} \int_{\alpha}^{\beta} \left[ I_{dc}(\theta - \alpha) + I_{rf} \cos \alpha - I_{rf} \cos \theta \right] d \cos \theta
\]

(A.20)

\[
\pi \omega C_p V_{ci} = \int_{\alpha}^{\beta} \left[ I_{dc}(\theta - \alpha) \cos \theta + I_{rf} (\cos \alpha - \cos \theta) \cos \theta \right] \sin \theta d\theta
\]

\[
= \left[ I_{dc}(\beta - \alpha) \cos \beta + I_{rf} (\cos \alpha - \cos \beta) \cos \beta \right] + \left[ I_{dc} \sin \theta \right]_{\alpha}^{\beta} + \left[ I_{rf} \sin \theta \cos \theta \right]_{\alpha}^{\beta}
\]

\[
= \left[ I_{dc}(\beta - \alpha) \cos \beta + I_{rf} (\cos \alpha - \cos \beta) \cos \beta \right] + \left[ I_{dc} \sin \beta - \sin \alpha \right] + \frac{1}{2} I_{rf} (\sin \theta)^2_{\alpha}
\]

\[
= I_{dc} [\cos \beta(\alpha - \beta) + \sin \beta - \sin \alpha] + I_{rf} [(\cos \beta - \cos \alpha) \cos \beta - \frac{1}{2} (\sin \beta)^2 + \frac{1}{2} I_{rf} (\sin \alpha)^2]
\]

\[
= -I_{rf} \sin \beta(\alpha \cos \beta - \beta \cos \beta + \sin \beta - \sin \alpha] + I_{rf} [\frac{1}{2} (\cos \beta - \cos \alpha)(\cos \beta - \cos \alpha)]
\]

\[
= -I_{rf} \sin \beta(\alpha \cos \beta - \beta \cos \beta + \sin \beta - \sin \alpha] + \frac{I_{rf}}{2} \sin \beta(\alpha - \beta)(\cos \beta - \cos \alpha)
\]

\[
= \frac{I_{rf}}{2} \sin \beta((\beta - \alpha)(\cos \beta + \cos \alpha) + 2 \sin \alpha - 2 \sin \beta)
\]

(A.21)
Therefore, the final expression for \( V_{ci} \) is

\[
V_{ci} = \frac{1}{\omega C_p} I_{pk} v_{ci}(\alpha)
\]  
(A.22)

\[
v_{ci}(\alpha) = \frac{I_{rf}}{\pi I_{pk}} \sin \beta \left[ \frac{1}{2} (\beta - \alpha)(\cos \beta + \cos \alpha) + \sin \alpha - \sin \beta \right]
\]  
(A.23)

From equation (A.17) and (A.21), one can easily find the relation between \( V_{ci} \) and \( V_{dc} \) as below:

\[
\frac{V_{ci}}{V_{dc}} = 2 \sin \beta
\]  
(A.24)

In [1.6] the intermediate equations Eq. (6.26) and (6.27) are inconsistent. Using either equation (6.26) or (6.27), one can not obtain the \( V_{ci} \) curve as shown in the Fig. 6.12 of that book. With the corrected final equations (A.22) and (A.23) for \( V_{ci} \), one can successfully generates the \( V_{ci} \) curve as shown in Fig. A.3, which is identical to the class E analysis plot in [1.6].

Similarly, the quadrature voltage component \( (V_{cq}) \) for the capacitor voltage is

\[
V_{cq} = \frac{1}{\pi} \int_{\alpha}^{\beta} v_c(\theta) \cos \theta d\theta
\]

\[
= \frac{1}{\pi \omega C_p} \int_{\alpha}^{\beta} [I_{dc}(\theta - \alpha) + I_{rf} \cos \alpha - I_{rf} \cos \theta] d\sin \theta
\]  
(A.25)

\[
\pi \omega C_p V_{cq} = \left[ I_{dc}(\theta - \alpha) \sin \theta + I_{rf} (\cos \alpha - \cos \theta) \sin \theta \right]_{\alpha}^{\beta} - \int_{\alpha}^{\beta} [I_{dc} + I_{rf} \sin \theta] \sin \theta d\theta
\]

\[
= \left[ I_{dc}(\beta - \alpha) \sin \beta + I_{rf} (\cos \alpha - \cos \beta) \sin \beta \right] - \left[ I_{dc} \cos \theta \right]_{\alpha}^{\beta} + \int_{\alpha}^{\beta} \frac{1}{2} I_{rf} (1 - \cos 2\theta) d\theta
\]

\[
= I_{dc} [(\beta - \alpha) \sin \beta + \cos \beta - \cos \alpha]
\]

\[
+ \frac{I_{rf}}{4} [4 \sin \beta (\cos \alpha - \cos \beta) + 2\alpha - 2\beta + \sin 2\beta - \sin 2\alpha]
\]  
(A.26)
\[ V_{cq} = \frac{1}{\omega C_p} I_{pk} \nu_{cq}(\alpha) \]  

\[ \nu_{cq}(\alpha) = \frac{I_{rf}}{\pi I_{pk}} \{-\sin \beta(\beta - \alpha) \sin \beta + \cos \beta - \cos \alpha \} + \frac{1}{4} [4 \sin \beta(\cos \alpha - \cos \beta) + 2\alpha - 2\beta + \sin 2\beta - \sin 2\alpha] \]  

From equations of (A.12), (A.19), (A.23) and (A.28), one can generate plots for \( I_{rf}(\alpha) \), \( v_{dc}(\alpha) \), \( v_{ci}(\alpha) \) and \( v_{cq}(\alpha) \) versus conduction angle \( \alpha \). Unity \( I_{pk} \) is used for generating the result as shown in Fig.A.3, which is identical to the Fig.6.12 in [1.6].

![Graph](image)

**Fig. A.3 Normalized voltage and current coefficients versus conduction angle.**

From the result in Fig. A.3, on can get the values of \( I_{rf} \), \( v_{dc} \), \( v_{ci} \) and \( v_{cq} \) for the conduction angle of 110 degrees. The list below verifies the values shown in the example.
of [1.6] (p. 171). Accordingly the resulting detailed circuit component parameters are also correct in that example.

<table>
<thead>
<tr>
<th>$v_{dc}$</th>
<th>$v_{ci}$</th>
<th>$v_{cq}$</th>
<th>$I_{rf}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.30</td>
<td>0.19</td>
<td>0.385</td>
<td>0.76</td>
</tr>
</tbody>
</table>
APPENDIX B

TWO TONE MODEL FOR EXTRACTION OF HARMONIC REFLECTION COEFFICIENTS

![Signal Flow Graph](image)

(a) Fig. B.1 Signal flow graph of DUT port 2 for deriving Eq. (4.9) for RT-ALP.

The signal flow graphs in Fig. B.1 model the DUT at port 2 in the swept phase measurement. Fig. B.1(a) and B.1(b) are the signal flow graphs at \( n_0 \) and \( (n_0 + \Delta) \)
respectively. The symbol \( a_2 \) and \( b_2 \) are the incident and reflective waves at the port 2 of the DUT. The \( a_{2,T} \) and \( b_{2,T} \) are the incident and reflective waves at the port 2 of the load tuner. The \( b_{\text{out}} \) and \( \Gamma_{\text{out}} \) represent respectively the n-th harmonic \((n\omega_0)\) injected signal and the effective impedance at the device output; \( b_{\text{ALP}} \) and \( \Gamma_{\text{ALP}} = 0 \) represent respectively the \((n\omega_0 + \Delta \omega)\) signal and source impedance injected by the matched external signal source in the swept phase measurement.

Applying the Mason’s rule, one can calculate the complex wave \( A_{2,n}(t) \) and \( B_{2,n}(t) \) in the two tone case by summing the two excitation tones in the signal flow graph:

\[
A_{2,n}(t) = a_2(n\omega_0) e^{i(n\omega_0)t} + a_2(n\omega_0 + \Delta \omega) e^{i((n\omega_0 + \Delta \omega)t)}
\]

\[
= \frac{b_{\text{out}} S_{11,T}^{\omega}}{1 - \Gamma_{\text{out}} S_{11,T}^{\omega}} e^{i(n\omega_0)t} + \frac{b_{\text{ALP}} S_{12,T}^{\omega}}{1 - \Gamma_{\text{ALP}} S_{11,T}^{\omega}} e^{i((n\omega_0 + \Delta \omega)t)} \tag{B.1}
\]

\[
B_{2,n}(t) = b_2(n\omega_0) e^{i(n\omega_0)t} + b_2(n\omega_0 + \Delta \omega) e^{i((n\omega_0 + \Delta \omega)t)}
\]

\[
= \frac{b_{\text{out}} S_{11,T}^{\omega}}{1 - \Gamma_{\text{out}} S_{11,T}^{\omega}} e^{i(n\omega_0)t} + \frac{b_{\text{ALP}} S_{12,T}^{\omega}}{1 - \Gamma_{\text{ALP}} S_{11,T}^{\omega}} e^{i((n\omega_0 + \Delta \omega)t)} \tag{B.2}
\]

where \( S_{ij,T} = S_{ij,T}(n\omega_0) \) and \( S_{ij,T}^{\omega} = S_{ij,T}(n\omega_0 + \Delta \omega) \) stand for the S parameters of the load tuner. \( \Gamma_{\text{out}} \) and \( \Gamma_{\text{out}}^{\omega} \) represent the effective impedance at the device output for \( n\omega_0 \) and \((n\omega_0 + \Delta \omega)\) respectively:

\[
\Gamma_{\text{out}} = \frac{b_2(n\omega_0)}{a_2(n\omega_0)} \quad \text{and} \quad \Gamma_{\text{out}}^{\omega} = \frac{b_2(n\omega_0 + \Delta \omega)}{a_2(n\omega_0 + \Delta \omega)}
\]
Equation (B.1) can be written as:

\[ A_{2,n}(t) = S_{1,T} B_{2,n}(t) + \frac{b_{ALP} S_{12,T}'}{1-\Gamma_{\text{out}} S_{11,T}'} e^{i(\nu_0 + \Delta \omega) t} (1 - S_{11,T} \Gamma_{\text{out}}') \]

It results that the ratio between \( A_{2,n}(t) \) and \( B_{2,n}(t) \) is:

\[
\frac{A_{2,n}(t)}{B_{2,n}(t)} = S_{11,T} + \frac{b_{ALP} S_{12,T}'}{1-\Gamma_{\text{out}} S_{11,T}'} e^{i(\nu_0 + \Delta \omega) t} \frac{1}{1-\Gamma_{\text{out}} S_{11,T}'} + \frac{b_{ALP} S_{12,T}'}{1-\Gamma_{\text{out}} S_{11,T}'} e^{i(\nu_0 + \Delta \omega) t}
\]

with

\[
R = \frac{(1-\Gamma_{\text{out}} S_{11,T}) b_{ALP} S_{12,T}'}{b_{\text{out}} (1-\Gamma_{\text{out}} S_{11,T}')} = \frac{b_2(\nu_0 + \Delta \omega)}{b_2(\nu_0)}
\]

\[ A_{2,n}(t) = S_{11,T} + \frac{1}{(1-\Gamma_{\text{out}} S_{11,T}) R} + \frac{\Gamma_{\text{out}}'}{1-\Gamma_{\text{out}} S_{11,T}'}
\]

Finally using the above expression for \( R \) we get the following Eq. (B.3) same as Eq.(4.9):

\[
\Gamma_L(\nu_0, t) = \frac{A_{2,n}(t)}{B_{2,n}(t)} = \frac{(1-\Gamma_{\text{out}} \Gamma_{\text{out}}')}{\Gamma_{\text{out}}[1+e^{-j\Delta\omega t} b_2(\nu_0 + \Delta \omega)/b_2(\nu_0 + \Delta \omega)]}
\]

with \( \Gamma_{\text{out}} = b_2(\nu_0 + \Delta \omega)/a_2(\nu_0 + \Delta \omega) \) and \( \Gamma_{L0} = S_{11,T} = a_2(\nu_0)/b_2(\nu_0) \).
APPENDIX C

PHOTOS OF THE PROPOSED MULTI-HARMONIC REAL-TIME ACTIVE LOAD-PULL SYSTEM

Fig. C.1 Proposed multi-harmonic real-time active load-pull (RT-ALP) system.
Fig. C.2 Zoom-in view of the on-wafer probe station and GaN wafer.
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