UNIVERSITY OF CINCINNATI

OCTOBER 9 , 20 03

I, PRERNA D. PATEL,
**hereby submit this as part of the requirements for the
degree of:**

MASTER OF SCIENCE

in:

COMPUTER ENGINEERING

It is entitled:

DESIGN OF A PIXEL SCALE OPTICAL POWER METER

SUITABLE FOR INCORPORATION IN A MULTI-TECHNOLOGY

FPGA

Approved by:

DR. FRED BEYETTE, JR.

DR. KAREN TOMKO

DR. DAVID KLOTZKIN

Design of a Pixel Scale Optical Power Meter Suitable for Incorporation in a Multi-Technology FPGA

A thesis submitted to the

Division of Graduate Studies and Research
of the University of Cincinnati

in partial fulfillment of the
requirements for the degree of

MASTER OF SCIENCE

in the Department of Electrical & Computer Engineering and Computer Science
of the College of Engineering

September 2003

By

Prerna Patel

B.S., (ECECS), University of Cincinnati,
Cincinnati, Ohio, 2001

Thesis Advisor and Committee Chair: Dr. Fred R. Beyette Jr.

Design of a Pixel Scale Optical Power Meter Suitable for Incorporation in a Multi-Technology FPGA

Prerna Patel

ABSTRACT

Over the years, FPGA devices have proven to be a valuable tool for engineers that allows faster development time and greater design flexibility. While current FPGA devices excel at facilitating the implementation of digital designs, they do not yet bring these same benefits to systems containing non-traditional multi-technology features such as optoelectronics, MEMS, and microwave devices. The goal of the MT-FPGA project is to take steps to bring the advantages of FPGA to these types of systems. One component identified for use within an MT-FPGA is an optical power meter system. This paper outlines the details of a pixel scale optical power meter that has been designed for use with the MT-FPGA project. The first part of this paper discusses the motivation behind the design of the MTB and outlines the project goals and constraints. Afterwards, the subject turns to the circuit design choices and other implementation details. Finally, the simulation and testing results are presented and analyzed.

ACKNOWLEDGEMENTS

To begin with, I would like to mention my deep appreciation for the supportive environment that Dr. Beyette and all of the members of the PSDL group have provided throughout my graduate school experience. Without the cooperation and assistance of my colleagues and the guidance of Dr. Beyette, this project would not have been possible. I would like to specifically thank the members of the MT-FPGA group Prosenjit Mal, Christopher Hawk, and Kavita Toshniwal.

Furthermore, I would like to express my gratitude to Dr. Klotzkin and Dr. Tomko for serving on my thesis advisory committee.

In addition, I would like to thank Prashant Bhadri who on more occasion than one helped the group get out of a tough situation. Not to be forgotten, I would like to thank Arvind Chockhani for his assistance with LabView. Also, for their respective contributions, I would like to express thanks to Vipul Patel, Hemant Sampath, Chris Isbell, John Phillips, Roger Kirschner and Rob Montjoy.

Table of Contents

Chapter 1 : INTRODUCTION	1
Section 1.1: Motivation.....	1
Section 1.2: MT-FPGA.....	6
Section 1.3: The MTB.....	9
Section 1.3: The MTB.....	10
Chapter 2 : Design Methodology.....	12
Section 2.1: Overall System Specifications	12
Section 2.2: Photodetectors.....	14
Section 2.3: Photoreceiver Sub System	16
Section 2.4: Analog to Digital Converter Alternatives	17
Section 2.5: Timing Considerations S/H	18
Chapter 3 : CIRCUIT DESIGN, LAYOUT AND SIMULATIONS.....	19
Section 3.1: Photodetector	19
Section 3.2: Photoreceiver (Variable Gain Amplifier)[12].....	22
Section 3.2.1: Simulation of VGA.....	24
Section 3.3: Unity Gain Buffer[21]	25
Section 3.4: Sample and Hold.....	27
Section 3.4.1 Sample and Hold Simulations.....	29
Section 3.5: Comparators [12]	30
Section 3.5.1: Comparator Simulations	33
Section 3.6: Analog to Digital Converter	34

Section 3.7: Entire Layout	38
Section 3.7.1: Simulation of System.....	40
Chapter 4 : TEST PLAN AND RESULTS.....	45
Section 4.1: Test Plan	45
Section 4.2: Electrical Test Results	47
Section 4.3: Optical Test Results	56
Chapter 5 : CONCLUSIONS.....	64
Section 5.1 Summary	64
Section 5.2 Discussion	64
Section 5.3 Future Work	65

Table of Figures

Figure 1-1: The basic layout of the components of the MT-FPGA.....	6
Figure 2-1: MTB connection with MTLC.	14
Figure 3-2 : Layout of photodetector.	21
Figure 3-3 : Circuit diagram of photoreceiver (VGA).....	22
Figure 3-4 : Layout of VGA.	23
Figure 3-5 : Effect of adjusting gain control of the VGA.....	25
Figure 3-6 : Circuit diagram for unity buffer.....	26
Figure 3-7 : Layout of unity buffer.	26
Figure 3-8 : Circuit diagram of sample and hold (capacitor not shown).	28
Figure 3-9 : Layout of sample and hold.....	29

Figure 3-10 : Transient Response ADC input.....	30
Figure 3-11 : Zoomed view of Figure 3-10	30
Figure 3-12 : Circuit diagram of comparator 1.....	31
Figure 3-13 : Circuit diagram of comparator 2.....	32
Figure 3-14 : Layout of comparator 1.....	32
Figure 3-15 : Layout of comparator 2.....	32
Figure 3-16 : DC response of comparator 1 at $V_+ = 1.65$ V.	33
Figure 3-17 : DC response of comparator 2 at $V_+ = 472$ mV.	33
Figure 3-18 : ADC block diagram.	35
Figure 3-19 : Gate level diagram of decoder.	36
Figure 3-20 : Layout diagram of ADC.	37
Figure 3-21 : Floorplan of optical power meter MTB.	39
Figure 3-22 : Output of Flash ADC at lowest gain.....	41
Figure 3-23 : Output of Flash ADC at mid gain.....	41
Figure 3-24 : Output of Flash ADC at high gain.	42
Figure 3-25 : DC response at end of each stage.....	43
Figure 3-26 : Overlay of amplified signal as it passes from the output of VGA through S/H to ADC.....	44
Figure 4-1: Block diagram of the test structure.	46
Figure 4-2: Electrical testing bench setup.....	47
Figure 4-3: Electrical test results for VGA.	49
Figure 4-4: Electrical test result for ADC output for lowest gain setting	51
Figure 4-5: Electric test results for ADC out for mid gain level.	52

Figure 4-6: Electrical test results for ADC out for high gain level.....	53
Figure 4-7: Electrical test results on system behavior for low current input.	54
Figure 4-8: Electrical test result on system behavior at each stage for lowest gain level.	55
Figure 4-9: Optical setup diagram.	57
Figure 4-10: Optical power characterization when testing photodetector.	58
Figure 4-11: Current output of photodetector.	59
Figure 4-12: Optical power characterization when testing MTB 1 (entire system).	60
Figure 4-13: Photoreceiver behavior for optical testing.	60
Figure 4-14: Optical test result for ADC out for low gain setting.	61
Figure 4-15: Optical test results of ADC out for high gain setting.....	62
Figure 4-16: Complete view of system measurements at a low gain setting.....	63

Table of Tables

Table 3-1: Gain and resolution at each comparator reference point.	34
Table 3-2: Layout sizes of selected components	39
Table 4-1: Bias conditions and power consumption at selected test point.	48
Table 4-2: Biasing points for each gain control setting.	50

Chapter 1 : INTRODUCTION

Section 1.1: Motivation

While advances continue to be made in VLSI technology with regards to traditional digital and analog circuit integration, large efforts are currently underway to explore the integration of new types of features. Examples of these include optoelectronic circuitry and MEMS devices [6, 7, 16]. Presently, it is not certain exactly what different kinds of components will be significant in future technologies, but some components appear likely to find widespread use.

In the area of optoelectronics, one of the component that often appears is the optical power meter. Optical power meters consist of a series of components that combine to sense and quantify the light incident on the detector structure. The primary components required by such a system are a photodetector, photoreceiver, and ADC. Photodetectors are integrated components capable of generating an output current when in the presence of a light source. Since this current is often too small to find useful application, photodetectors are often coupled with photoreceiver amplifiers that boost the signal to levels suitable for transport or further modification. The final component, an ADC, samples the magnitude of the resulting analog signal and assigns it to a representative digital value.

The entire system forms a gateway for information to travel from the optical domain into the digital domain, and is a significant element in many systems [1]. With any such system element that finds repeated application, it is often desirable to include such a design in a reconfigurable device. Through the design and development of an optical power meter suitable for integration within a new class of reconfigurable chips

known as multi-technology field programmable gate arrays (MT-FPGAs) a versatile device can be created that has the ability to fulfill a multitude of roles . MT-FPGAs have been created in an attempt to bring all the benefits of reconfigurable architectures into systems that contain advanced integrated components such as mixed-signal, optoelectronic or MEMS components [8]. Reconfigurable architectures are valuable because of their flexibility. Field Programmable Gate Arrays (FPGAs), Programmable Logic Arrays (PLAs), Programmable Logic Devices (PLDs), and Field Programmable Analog Arrays (FPAAs) are all recognized classes of devices that provide engineers with basic system building blocks that can be programmed in such a way to suit the needs for a wide variety of applications. Because a single flexible device can potentially implement a whole range of functions, it is possible for the users of these types of devices to create rapid circuit design prototypes on a single chip without having to go through the long process of creating a custom fabricated chip. Additionally, the same hardware can be reused over and over to test out different design choices. All of this flexibility results in a much quicker and cheaper way to experiment with and arrive at successful system designs. It is also possible for an existing piece of hardware containing the reconfigurable device to be modified after production to fulfill a new role. Other applications might even seek to continually modify themselves as a way to evolve and adapt to new situations [3].

Up till now, there has been a gap where applications requiring sophisticated components that can not be implement using the digital or simple analog circuitry must require the developer to create a custom design to accomplish the their goals. However, it is intended for MT-FPGAs to act as a programmable hardware resource that allows

engineers to think about developing such systems in a programmable fashion just like with traditional FPGAs. When deciding on the building blocks that will be available within the MT-FPGA, it has been concluded that the chip should offer the all the functionality of the regular FPGA such as programmable digital look up tables and interconnections. Additionally, these new devices should provide the user with a library of multi technology building blocks that extend the potential capabilities of the system and provide interfaces between the new integrated domains and the digital processing elements.

The limitation for what types of multi technology blocks might be included is constrained only by the capabilities of the process technology used for the design fabrications and our ability to prevent components from interfering with each other. For our design, the MT-FPGA was fabricated on a .35um process technology by way of the MOSIS foundry service [9]. In this technology we are able to create optoelectronic structures such as photodetectors which can be integrated into the Multi-Technology Blocks (MTBs) of the MT-FPGA. The MTB considered in this discussion is intended to function as an optical power meter that can operate independently or as part of an array of sensors within the MT-FPGA's programmable architecture. When present as part of programmable architecture this MTB is a building block that can help tie together optical signals with any electrical system that can be fabricated within the MT-FPGA. In this way it is possible to use the MT-FPGA containing pixel scale optical power meter MTBs as a general purpose optical gateway where optical signals can be collected and converted into digital data and transformed in intelligent ways to compensate for signal losses in the optical paths, help extract useful information, assist in reducing noise, or any other useful

signal transformations. MT-FPGA devices could potentially devote varying amounts of processing power to each optical pixel, either choosing to perform large amounts of processing on each optical signal path while leaving less amounts of free logic to perform general purpose logic functions or taking the opposite approach, devoting few resources to the optical signals and instead creating a more complex system controller.

Some possible applications for this type of hardware would include systems where it is necessary to sense optical data and process it within a single integrated chip system. One area where this might be useful is in biochip applications where an integrated silicon device could analyze the optical signature of biological liquids to detect the presents of tagged chemicals [20]. In certain circumstances, it might be desirable to create these types of biochip systems that can be inserted into living tissues. In these cases it would be necessary for the entire system to be small as possible, and therefore, a single chip detector and processing device would be highly desirable. A device such as the MT-FPGA might offer such a single chip solution and therefore a good candidate of this class of applications. In general, all image processing applications where overall system size or cost is a critical factor in where it is not necessary to have large number of pixels are suitable for implementation with MT-FPGA.

It is clear that providing functionality of the MT-FPGA has a potential to being useful device that will allow engineers to more efficiently integrate mixed technology capabilities into their system. There are some limitations because of the requirements that lead to nontraditional technology will have to be integrated on the same wafer as a the programmable logic. Because of this many high speed cutting edge applications of optoelectronics or MEMS which requires highly customized fabrication techniques will

not benefit from such a device as the MT-FPGA. Instead designer will be able to try out various signal processing arrangements and take advantage of the locality of having signal processing capabilities adjacent to the optoelectronic or other technology components.

Section 1.2: MT-FPGA

Much like any field programmable device, the MT-FPGA offers an architecture composed of basic functional blocks which are connected together by a structure of programmable interconnections. The MT-FPGA, as a new class of reconfigurable programmable devices, must provide a platform for a wide variety of mixed technology components as well as provide for programmable interconnections and IO capabilities to distribute the signals generated by these multi-technology blocks. Figure 1-1 details the overall structure of the MT-FPGA.

Figure 1-1: The basic layout of the components of the MT-FPGA.

An array of multi-technology logic clusters (MTLCs) provides the device with its processing power. Each logic cluster is capable of performing basic digital logic

functions as well as any capabilities provided by the MTB block at its center. The MT-FPGA project team envisions a library of different MTB each giving the device new powers. Before fabrication time, a set of MTBs would be selected and inserted into the available space. Depending on if the choice of MTB was a broad or narrow selection the

Figure 1-2: A more detailed look at a MTLC.

MT-FPGA could trade off general flexibility for a more specifically tailored purpose based on the need.

Figure 1-2 shows the basic structure of a single multi-technology logic cluster (MTLC). Inside each MTLC, there are several digital look-up tables, an internal bus with programmable connections, and a space for a multi-technology block. Within the central space, there are connections to handle digital and analog signals for input and output of the various multi-technology cells that could occupy the MTB space.

The array of logic clusters rests within a framework of flexible programmable routing channels that are responsible for all the communication between the MTLCs as well as transporting signals to and from the chip's external pins. The interconnect structure of the MT-FPGA is comprised of digital and analog signal path ways. The

analog pathways feature special shielding on all sides and are always kept some distance away from digital signal paths. Wherever there is an intersection between a horizontal and a vertical routing channels the signal pathways pass through programmable switchblocks. When programmed, the switchblocks (SB) define the electrical connections between all the routing channels at an intersection. Around the peripheral of the chip the switch blocks also connect to I/O blocks which have the responsibility of bringing signals to and from the pad frame and configuring the pad's input and output drivers.

The programmability and re-configurability of the MT-FPGA is accomplished by using SRAM cells to handle all of the device's memory, and then arranging the SRAM in an array of select and data control lines. These control lines are accessible through two shift registers. The shift registers serially control the selection and loading of data into the MT-FPGA.

Figure 1-3 illustrates the physical layout of a MT-FPGA design as seen from the MAGIC layout editor.

Figure 1-3: Magic layout of an MT-FPGA.

Section 1.3: The MTB

While research continues to extend the range of what types of things can be accomplished solely through optical computing, it is still the case that most present and near term applications of integrated optics rely on both conventional electronic circuits and optics [7]. As long as it is necessary to continue to interface optics and electronics, components that are capable of interfacing between the two types of computing will remain an important part of many systems.

Figure 1-4: The top level diagram of the MTB.

Beyond simply detecting the presence of a light signal, the optical power meter attempts to quantify the power within the light source and provide a digital representation of the signal. On the top level, the optical power meter consists of a photodetector, photoreceiver, and ADC module. Additionally, buffers and a sample and hold circuit are added to maintain signal driving strength and integrity at the nodes between the major components.

Figure 1-4 is a schematic showing how optical light enters into the system and passes through the series of components until it is converted into a multiple-bit digital signal. The Gain Control and V-bias signals are useful signals that greatly increase the

flexibility of the optical power meter. It is well known that the semiconductor parameters of a fabricated run of chips can vary by significant amounts at different points on a wafer or even a single device. Because of this each optical power meter will be slightly different and will require a different bias point and have differing gain characteristics. By allowing the bias and gain control to be set by an outside source, it is possible to make adjustments for process variations so that components performing differently from each other can all be configured to behave in roughly the same way. All that is required is for the chips to be characterized after fabrication, and based on the results, the control signals of two MTB are adjusted until the bias point and range are brought into alignment. Furthermore, the MT-FPGA logic could possibly make intelligent decisions to alter the power meter performance based on other factors (i.e. temperature change, differences in light sources, feedback from and auto-calibration routine). By configuring the architecture of the MT-FPGA into an appropriate control system and including the proper MTB components many possibilities are imaginable.

Chapter 2 : Design Methodology

Section 2.1: Overall System Specifications

To construct a good optical power meter MTB, it is a good idea to outline the overall specifications of the system, and consider the advantages and disadvantages of various design choices. At the highest level, an optical power meter detects a light source and produces output telling the amount of power in the light source. Also, it is important to consider outside constraints that limit the design choices in ways that will affect the overall decision making process. In the case of the MT-FPGA, the goal is to develop a programmable multi-technology device that is manufactured in a commonly available and inexpensive technology. If it can be proven that useful systems can be developed on a general purpose technology, it is much more likely that others will choose to adopt and build on the research. As a result, from the start it has been determined that the MTB design will be implemented on a .35 micron CMOS process with 2 poly layers and 4 metal layers. It is also important to note that the process is n-well only, and elements requiring a p-doped bulk contact are built directly into the silicon substrate. The four metal layers are needed because one characteristic of FPGA type devices is that they require large amounts of extra routing to handle all the programmable switches and the extensive interconnection networks. For the purposes of the MTB, probably the more important feature is the two different poly layers. Since there are two poly layers, it is possible to create poly-poly capacitor structures which are useful in analog circuitry. Another feature of the fabrication process that has some effect on the design choices for the MTB is the requirement that the entire chip use less than 7 mm^2 of silicon area. This

small area limits the size of the MTB. In this case, the overall area was set at 200 x 200 microns of floor space.

In addition to the constraints caused by the device technology and fabrication, other factors also influence the design choices that have been made. In the area of optics, it is important to take into account the types of light sources that are used, and the range of power that can be expected so that these sources can be measurable by the optical power meter MTB.

One last important set of considerations is the impact of the existing MTLC architecture. Since the MTB is just one component out of a library of multi-technology devices, it is necessary that the MTB must interface with a digital and analog routing resources provided to it by the MTLC internal bus. A simplified view of the MTLC internal routing is shown in Figure 2-1. According to the documentation concerning the MTLC [8, 17], all of the communication between the MTB and the MTLC must be done using bits 9 to 12 of the MTLC internal routing bus. These four bit lines are capable of transporting both analog and digital signals between the MT-FPGA routing channels and the MTB area. The rest of internal bus signals are reserved for the programmable logic blocks (PLB) as well as other global signals. Considering these facts, the design of the MTB optical power meter should be able to perform its intended function utilizing these available communication pathways.

Figure 2-1: MTB connection with MTLC.

Section 2.2: Photodetectors

The next phase of the planning for the optical power meter involves a more detailed look at each of the essential components of the MTB system. Because the photodetector is the first component along the data flow path of the optical power meter, it is probably a good idea to choose a design for the photodetector and analyze the expected performance of the design before proceeding to the rest of the system's components. All silicon photodetectors operate based on the photoelectric effect of the substrate material. The photoelectric effect is the name for the property of material to produce electron hole pairs of free charge when light photons are absorbed. These free carriers normally drift in random directions through out the substrate. However, when the free carriers passed through area where there is an electric field, forces in the field caused

the motion of the carriers to be changed so that they generate electric currents in the direction of the electric field.

In integrated device it is possible to create an electric field by creating a diode junction and applying reverse bias voltage across the junction. There are different choices for the junction that can be used to create a photodetector. Since the process technology has been decided on as 0.35 micron CMOS process the two junctions available for creating a photodetector are the N-well to P-substrate junctions, and the P-diffusion to N-well junction.

In general, a CMOS process is not ideal for producing high quality photodetectors. Because light has a long absorption depth in silicon and because the available junction for creating the photodetector are all fixed at depths much shallower than where the bulk of the photons are absorbed, only a small percentage of the incident light is actually absorbed within the detector's electric field. The rest of the light is instead absorbed deep within the silicon substrate causing a slow response time for the photodetector. This slow response time is known as "long tails" [4]. The reason for the long tail is that the random motion of the electron hole pairs created deep within the substrate continue to add current to the output as some of them eventually migrate into the electric field.

Fortunately the P-diffusion to N-well photodetector has a nice feature that helps to deal with the decreasing the numbers of carriers allowed to migrate back into main output current. Beneath the primary junction of the photodetector the N-well to P-substrate junction conveniently acts as a screen for these extra carriers. This gives the P-diffusion to N-well photodetector an advantage in terms of response time over the simpler N-well and P-substrate photodetector. On the other hand, because the electric field of the P-

diffusion to N-well photodetector is shallower and therefore even further from the ideal absorption depth, this type photodetector will have less responsivity.

Previous work in the area of the photodetector provides a good foundation of data supporting these ideas [5]. In our case we do not require the higher responsivity of the N-well to P-substrate because we intend to operate the circuit with a large amount of optical power and it should not be difficult to amplify the resulting current to the voltage levels needed. Therefore, based on its response time, the P-diffusion to N-well photodetector is a good design for this system. Assuming the responsivity predicted by Woodward and Krishnamoorthy [4], it is expected that the photodetector will have a responsivity of .01 A/W for a 16.54 μm X 16.54 μm structure.

Section 2.3: Photoreceiver Sub System

The discussion of the performance of the photodetector and the range of optical power for which the meter has been designated to measure indicates the amount of current that can be expected to be generated. This amount of current if taken directly would make it very difficult for the ADC to resolving the signal into the many different power levels. Therefore, if we take the approach of first amplifying the signal it would be possible to provide the ADC with an input signal that varies by a much greater magnitude. This is helpful because the accuracy of the ADC depends upon the range of the input signal. The highest possible range for this system is 3.3 V which is the difference between Vdd and Gnd. As a result, it is good to shoot for a photoreceiver design that can amplify output of the photodetector so that the signal varies between 0 V and 3.3 V. Based on this information, it is possible to know the overall gain that we would like for the amplifier.

One of the overall goals for the MT-FPGA is to provide a flexible test bed that can be used to create systems capable of working in variety of ways and in as many potential working environments as possible. Following from this, it makes sense that the optical power meter should also be flexible and able to operate over whole a range of potential input currents. In this respect, the important thing to do is to try to produce an MTB with an adjustable gain setting so that the photoreciever can work for different ranges of current generated by the photodetector. This has the added benefit of creating some margin for error concerning the estimation of the photodetector current around which the amplification system has been based. According to this reasoning, a variable gain amplifier design is an appropriate choice for the photoreceiver. Furthermore, the degree of variability should be as high as possible so long as the amplifier can be reliably held stable at a particular gain setting.

Section 2.4: Analog to Digital Converter Alternatives

Because the system architecture limits of the number of the output bit lines in the MTLC we have to create a 4-bit Analog to Digital converter which converts the amplified signal from VGA to 4-bit digital output. The digital output can than connect directly to the internal bus of the MTLC. For our purposes we would like to choose an ADC design with small circuit size, high speed and good resolution. Considering that an ADC will be only 4-bits, a flash ADC seems an ideal choice in all of these areas. Flash ADCs are constructed by creating a set of comparators and different voltage reference points against which the input signal is compared in parallel. The outputs of these comparators are than sent to a decoder that is used to generate four output bits.

Section 2.5: Timing Considerations S/H

Up to this point, we have not taken into account all of the transient effects that the system must account for during its actual operation. In reality the signal at the output of the photoreceiver will be constantly varying with time. At the same time the operation of the ADC requires a finite amount of time. If we allow the ADC input to constantly change as the calculation of the output is being performed, this can cause problems with the accuracy of the final output digital value. To fix this problem it is usual to introduce a sample and hold circuit before the ADC to provide the ADC with a more stable signal from which to produce an output signal.

Chapter 3 : CIRCUIT DESIGN, LAYOUT AND SIMULATIONS

Section 3.1: Photodetector

After coming to the conclusion that the p-diffusion to n-well photodetector would be the best option for the implementation of the optical power meter's light sensing component, the next step was to begin planning the physical layout and construction.

Figure 3-1: Cross section of the p-diffusion to n-well photodetector.

Figure 3-1 is a cross-sectional view of the device showing the important junctions and contacts, and Figure 3-2 gives a picture of the physical layout as seen from the MAGIC layout editor. The layout of the photodetector has a rectangular floorplan on account of the desire to keep the overall system in roughly a 1 by 1 aspect ratio. The n-well region forms the base of the photodetector and has dimensions of 147 μm x 84.4 μm .

Surrounding the n-well structure, a narrow n-diffusion contact ring forms a connection to the n-well and enables it to be connected to the detector bias voltage. Because of the fact that it was already present, it was decided that it would be most efficient from an area standpoint to fix the bias voltage to the VDD value of 3.3V. With this biasing method, it is no longer necessary to have an extra voltage source or worry about the routing that would have been required to connect it to the photodetector. For the purpose of protecting against any noise that might be injected through the substrate, a ring of grounded substrate contacts lie just outside the n-well detector base. Because of the low levels of the detector current, this is especially important since even low levels of noise superimposed on a small signal will greatly impact the signal to noise ratio. Finally, the detector's active terminal is made up of sixteen interdigitated fingers in the p-diffusion layer. The interdigitated design is a nice feature that helps to maximize the overall responsivity by increasing the volume of the electric field. Since the p-diffusion regions of the photodetector are 3-dimensional they will create electric fields on 3 sides, this extra area can potentially create more current. The spacing between the p-diffusion fingers has been set to 7 microns. A center strap ties all the fingers together and connects the active terminal to the input of the photoreciever.

Figure 3-2 : Layout of photodetector.

transistor. Because the amplifier's input is connected to both a p-mos transistor to pull the signal up and a n-mos transistor to pull the signal down it is known as a push-pull amplifier or in digital circuits just an inverter.

The feedback transistor can be thought of as a variable gain resistor with the resistance controlled by its gate voltage. Since the gain control mechanism operates on the first stage only, it is possible to adjust the overall gain of the amplifier over a wide range. The second stage of the circuit is a wide-swing differential amplifier [12]. This amplifier effectively contains two differential amplifiers, one featuring a P-channel differential pair and one featuring a N-channel differential pair. The presence of two differential amplifiers increases the common mode range of the amplifier helping to increase its flexibility. Both differential amplifiers use diode connected transistors as a load.

Figure 3-4 : Layout of VGA.

The current flowing through the negative leg of each differential pair is detected by current mirror circuits and the mirrored current is then directed into the node at the drain of the positive leg of each differential pair. This causes the current generated within both the differential pairs to flow together through the load transistors on each of the differential pair's positive legs. The output of the amplifier is generated by comparing both of the shared currents at the two output driver transistors. By appropriately sizing the widths of key transistors, it is possible to construct this amplifier design so that the gain is constant regardless of whether both differential amplifiers are operating or just one. The physical layout of the VGA design is given in Figure 3-4. This compact design includes grounded guard ring shielding.

Section 3.2.1: Simulation of VGA

All the circuit design work was done using NCSU cadence design kit [10]. Using the spectre circuit analysis tool provided within the cadence design kit, simulations were performed on both the schematic and the extracted views of all of the circuits. For the VGA we were able to see the range of variability of a correctly biased circuit. Figure 3-5 shows an output of a parametric sweep of various gain control settings for the VGA. It is clear that as the gain control voltage is decreased the gain of the amplifier continues to increase. Measurements of the gain indicate that at the minimum gain control setting the gain equals 30M V/A and for high gain control setting the gain equals 18.75K V/A.

Figure 3-5 : Effect of adjusting gain control of the VGA.

Section 3.3: Unity Gain Buffer[21]

Figure 3-6 illustrates the circuit diagram of a simple unity gain buffer design that was used to help preserve the output of the variable gain amplifier as it passes to the ADC. The circuit features two stages. The first is a N-channel differential amplifier. Instead of creating a full current source design, the source of the differential pair is instead connected to a NMOS transistor with the gate tied directly to VDD. This was done to save layout area. In this case, the differential pair features a current source load to improve the overall first stage performance. The rest of the circuit for the unity gain buffer consists of a output driver stage that adds driving capability and stability. Figure 3-7 show an image of the buffer layout.

Section 3.4: Sample and Hold

It is important to remember the sample and hold circuit because it plays an important role in helping the optical power meter produce accurate measurements. The significance of the sample and hold circuit lies in that it provides the ADC with a snapshot of the constantly changing VGA output and works to prevent the captured voltage level from decaying over the time period that the ADC requires to produce an output. The sample and hold circuit is responsible for tracking the VGA output. There should be very little discrepancy between the internal node of the sampling circuit and the output of the VGA when the circuit is in sampling mode. Also, it is desirable that the sampling mechanism does not place too much load on the receiver amplifier. Once the circuit enters the hold mode, the circuit then works to prevent the signal from drooping while the ADC operates.

Flash ADCs operate in a parallel fashion and are fast. Therefore, in this case, the hold time can be fairly short. For such a design, it makes sense to use a simple switch and capacitor for implementing the circuit. Figure 3-8 shows the design of the sample and hold circuit minus the storage capacitance. The switch is just a transmission gate consisting of an NMOS and a PMOS transistor in parallel. Since the transmission gate also requires the inverse of its control signal, an inverter is also present. The transmission gate is important because the output of the VGA should pass through accurately across the entire VDD to GND voltage range. In the sampling mode the transmission gate will be open and the signal from the output of the VGA passes through and charges a capacitor. The capacitor adds a load to the VGA so from this perspective it is important to keep it fairly small. At the time of measurement, the sampling switch is closed,

trapping the voltage level across the capacitor, therefore holding it to a fixed value for a time while the ADC senses it and performs its conversion to a digital output.

The complete layout of the sample and hold circuit is shown in Figure 3-9. Again, we have included a grounded guard ring structure surrounding the design to help keep out unwanted noise.

Figure 3-8 : Circuit diagram of sample and hold (capacitor not shown).

Figure 3-9 : Layout of sample and hold.

Section 3.4.1 Sample and Hold Simulations

The performance of the sample and hold circuit is best characterized using the transient analysis as we switch the control signal on and off. Figure 3-10 and Figure 3-11 shows the two views of the simulation outputs. Figure 3-10 shows entire behavior and Figure 3-11 shows the zoomed in view of the circuit behavior. From the simulations, only a small amount of the error has been introduced into the system by the sample and hold, and little to no drooping of the signal is observable.

Figure 3-10 : Transient Response ADC input

Figure 3-11 : Zoomed view of Figure 3-10

Section 3.5: Comparators [12]

Essentially a subcomponent of the ADC design, the comparators required a lot of careful circuit design work to achieve a good high resolution design. The comparator design has three important stages that combine to produce a device that can distinguish small differences in its input terminals. Figure 3-12 and Figure 3-13 show two slightly different versions of a basic comparator design. The three stages are a input pre-amplifier, a decision stage, and a output post-amplifier. The pre-amplifier stage is once again a differential amplifier with diode connected load transistors. The current flowing through the loads are sensed and mirrored along two pathways at the output of the first stage. The next stage is the decision circuit stage. The decision circuit accepts the current outputs from the preamplifier and uses them to force a decision at the gate-drain cross coupled nodes. The cross coupled configurations create a positive feed back mechanism that allows even small differences in the currents to quickly switch the

outputs when one input becomes stronger relative to the other. The final stage of the comparator circuit is a self-biasing output driver. The output driver accepts the differential input voltage output from the decision circuit and produces single voltage output capable of driving power without loading the previous stages of the comparator.

In this design, two extra inverter output stages have been added to increase performance. The two separate designs are included because the ADC design requires comparators that work at a full range of comparison reference points. Since the input preamplifier shuts off when its inputs fall below their common mode range, a second comparator layout was created that takes advantage of a preamplifier with opposite channel polarity to allow comparisons at the remaining voltage reference points. Figure 3-14 and Figure 3-15 show the final layout of the comparator designs.

Figure 3-12 : Circuit diagram of comparator 1.

Figure 3-13 : Circuit diagram of comparator 2.

Figure 3-14 : Layout of comparator 1.

Figure 3-15 : Layout of comparator 2.

Section 3.5.1: Comparator Simulations

For the comparator, we have performed number of the simulations to get a good idea of the performance that device should display. The main characteristic that we are concerned with for the comparator is the resolution between two signals of the comparator. Since the resolution depends on the magnitude of the voltage reference the most important value to consider is the worse case gain out of all of the various reference points in the design. Figure 3-16 and Figure 3-17 shows the comparator gain at two different voltage reference points. Overall the worse case gain is that the reference point 470 mV with the value of 8.38 KV/V. Table 3-1 shows the voltage gain and the resolution at each of the reference points.

Figure 3-16 : DC response of comparator 1 at $V_+ = 1.65$ V.

Figure 3-17 : DC response of comparator 2 at $V_+ = 472$ mV.

Voltage Reference Points (V)	Resolution (V)	Gain (V/V)
2.829574468	2.16763u	1.21631M
2.66106383	2.03485u	1.2955M
2.492553191	2.00465u	1.31356M
2.324042553	2.03001u	1.30236M
2.155531915	1.99261u	1.3232M
1.987021277	1.9863u	1.32767M
1.818510638	1.97783u	1.33337M
1.65	2.00139u	1.31757M
1.481489362	1.95917u	1.34593M
1.312978723	1.94943u	1.35252M
1.144468085	1.93874u	1.36012M
0.975957447	1.90864u	1.38146M
0.807446809	271.875u	9.69468K
0.63893617	293.906u	8.97123K
0.470425532	341.595u	8.38124K

Table 3-1: Gain and resolution at each comparator reference point.

Section 3.6: Analog to Digital Converter

The Flash style analog to digital converter is known as the fastest converter design available because of the fact that all of the conversions take place in parallel. The completed ADC circuit uses 2^N-1 of the comparators described in Section 3.5 where N = the number of bits of resolution, in this case four. Figure 3-18, shows the ADC block design. Also, there are 2^N resistors arranged into a string that have the purpose of generating each of the 2^N-1 reference voltages. The lowest three comparators utilize the alternate comparator circuit design because of the low level of the reference point. After the resistor string and comparators, have been put into place, the outputs of the comparators are set up so that the all of the comparators with a reference point greater than the input signal will output a digital 1 value and all of the comparators with a reference point less than the input voltage have output of 0. At this point there are total of 2^N-1 comparators outputs. To convert this to a four bit output, a decoder is needed. The decoder stage is shown in Figure 3-19. The decoder consists of two levels of NAND

gates that detect adjacent comparators with differing output values. Figure 3-20 shows the entire layout of the four bit Flash ADC.

Figure 3-18 : ADC block diagram.

Figure 3-19 : Gate level diagram of decoder.

Figure 3-20 : Layout diagram of ADC.

Section 3.7: Entire Layout

The last step in putting everything together involves connecting all the components into one layout. The complete diagram of the entire MTB is shown in Figure 3-21. To begin with, the p-diffusion terminal of the photodetector is connected to the input of the first stage of the VGA. In the VGA, the photocurrent is converted to an appropriate voltage level for the ADC. While the negative terminal of the differential amplifier is connected to the first stage output, the positive input is connected to a user controllable bias voltage. Successful operation of the power meter system would therefore involve two steps to adjust the two photoreceiver control settings. First, the user would have to adjust the first stage gain control input until the desired amplifier gain is reached. After this has been completed the user could then adjust the V-bias signal to adjust the point where the ADC will overflow. The overall effect of these adjustments is that the linear range of operation of the photoreceiver circuit can be adjusted. The low end range of operation is always set to 0, while the high end is scalable by adjusting V-bias and the gain control voltage. Following the VGA, comes the sample and hold circuit surrounded by two unity gain buffers. Finally, the last component is the ADC. In order for a functional system to be integrated into the MT-FPGA, the four outputs of the ADC must be stored into an output register, which can then be sent two bits at a time through output muxes to two digital outputs. In total, the entire system has two analog inputs, one digital input and two digital outputs. Additionally, the system clock is needed to take care of triggering. The current fabrication of the MT-FPGA does not include a testable MTB formatted in this way. Instead the tested model sends its outputs directly to the chip's output pins.

Figure 3-21 : Floorplan of optical power meter MTB.

	X (um)	Y (um)	Area (um^2)	Aspect Ratio
VGA	41.2	16.9	696.28	2.43786982
UNITY	40.6	18.5	751.1	2.19459459
S/H	11.6	10.4	120.64	1.11538462
Comp3	33.4	12.6	420.84	2.65079365
Comp4	35.4	12.6	446.04	2.80952381
ADC	85.7	200.2	17157.14	0.42807193
Entire	192.3	201.8	38806.14	0.95292369

Table 3-2: Layout sizes of selected components

Section 3.7.1: Simulation of System

After completing the design of the MTB, simulation of the entire system was able to show some convincing results that help supported that the system was working properly. For the purposes of the full system simulation, the optical power input was replaced by a voltage controlled current source such that the responsivity of the photodiode is equal to the gain of the VCCS. Also, the photodiode PN junction was modeled with technology appropriate data. Extracted views of the rest of the component's layouts were then combined into one complete model of the system. After a complete circuit schematic was laid out, a simple sweep of the simulated input optical power produced a number of interesting waveforms. These waveforms demonstrated the operation of the ADC as well as the entire system. Figure 3-22 shows the ADC output at the VGA's lowest gain setting. Each waveform gives the output of a single bit of the ADC. When all four are taken together, the signals represent the digital value that corresponds to each possible input optical power. Figure 3-23 and Figure 3-24 illustrate two additional gain settings and give some idea the effectiveness of the gain control adjustment.

Figure 3-22 : Output of Flash ADC at lowest gain.

Figure 3-23 : Output of Flash ADC at mid gain.

Figure 3-24 : Output of Flash ADC at high gain.

Taking a look at a few more figures, Figure 3-25 and Figure 3-26 are included to show the way which the VGA out signal passes through the various stages and eventually reaches the ADC input. It is clear to see that the signal integrity and linearity behave well at all four internal stages.

Figure 3-25 : DC response at end of each stage.

Figure 3-26 : Overlay of amplified signal as it passes from the output of VGA through S/H to ADC.

Chapter 4 : TEST PLAN AND RESULTS

Section 4.1: Test Plan

Prior to fabrication a test plan was developed for evaluating the performance of the optical power meter MTB unit. Overall, there were three MTBs integrated into the MT-FPGA that was fabricated. The first two MTBs are controllable directly through the chip's pins while the third was to be accessible through the MT-FPGA routing channels and programmable circuitry. Because of errors made during layout, this third MTB was not available for programming and was therefore untestable by any means and will not be discussed further. In total, the testing process involved two modes of testing. The remaining two MTB systems share a set of pin connections that are multiplexed using the TEST pin to select between the two test modes. In the first mode, special test features allow the post-photodetector circuitry to be tested purely by electrical methods. During this electrical testing a modified MTB circuit was used to directly inject a current into the VGA. The test features making this possible are visible in Figure 4-1. The TEST pin is used to select between a mode where the direct output of the photodetector is sent to an output pin and another mode where the pin can be used to drive the VGA. Additionally the TEST pin directs the proper MTB's output signals to the pins. Section 4.2 contains a discussion of the electrical testing performed. After finishing the electrical portion of the test plan the chip was then moved onto the optical test bench where further testing was done to demonstrate the functionality of the complete system. Section 4.3 outlines the optical testing procedure and presents all the important data that was collected.

Figure 4-1: Block diagram of the test structure.

Section 4.2: Electrical Test Results

The first step done in the electrical testing was to choose an appropriate test setup for evaluating the MTB performance and collecting the important data to support that it is working well. The test setup for the electrical testing required a multitude of instruments. A HPE3631A Triple Output supply was used to supply the VDD, Vbias and Vgain signals to the device under test. A pattern generator was used to input the Control Signal timing needed to operate the Sample and Hold for the MTB. The current input for the VGA was created using a Keithley 220 current source. Lastly, a Hewlett-Packard 34401A multimeter monitored some of the selected internal nodes, and the four digital outputs were collected using a National Instruments DAQ card. A LabView program helped assist the acquisition of data by coordinating the current source, multimeter, and DAQ card. The complete electrical test setup is shown in Figure 4-2.

Figure 4-2: Electrical testing bench setup.

After the electrical testing setup was put into place, the first step was to perform an initial analysis over a range of chips to get a feel for the effects of process variation on the overall performance of the optical power meter system and to select a good sample set to be used for more intensive testing later. Each of the chips were first biased such that at zero current input the ADC output became zero and at 160uA input current the output just transitions to 1111. Table 4-1 summarizes the biasing conditions and power consumption for each of the seven chips tested.

	Vbias(V)	Vgain(V)	I power Supply(A)	Power(mW)
Chip 1	1.188	3.01	0.08	264
Chip 2	1.185	3.08	0.08	264
Chip 3	1.197	3.11	0.07	231
Chip 4	1.199	3.04	0.08	264
Chip 5	1.185	3.02	0.07	231
Chip 6	1.19	3.05	0.07	231
Chip 7	1.212	3.08	0.07	231

Table 4-1: Bias conditions and power consumption at selected test point.

Based on the results from the broad characterization, chip 7 was selected for further characterization. Figure 4-3 shows the characterization of the VGA over a range of gain control settings. The graph shows the multimeter measurements recorded through the Vmonitor pin connection which records the voltage at the output of the VGA. Table 4-2 contains a record of the points at which each trace was calibrated.

Figure 4-3: Electrical test results for VGA.

Current (uA)	Biased_Current	Vgain
10	9.375	2.12
20	18.75	2.36
30	28.125	2.46
40	37.5	2.56
50	46.875	2.63
60	56.25	2.7
70	65.625	2.75
80	75	0.8
90	84.375	2.84
100	93.75	2.89
110	103.125	2.92
120	112.5	2.96
130	121.875	3
140	131.25	3.03
150	140.625	3.05
160	150	3.08

Table 4-2: Biasing points for each gain control setting.

The final digital output of the ADC when driven by a current input is also observable. Similar to the characterization of the VGA, the output of the ADC was also measured at a variety of gain settings. Figure 4-4, Figure 4-5, and Figure 4-6 show the ADC digital output a low, medium, and high gain setting. Additional testing showing the point where the noise in the system begins to become more apparent by causing more uncertainty in the ADC output is shown in Figure 4-7 where in input current is biased at a 7uA point. Finally, Figure 4-8 tries to capture the best case linearity of the system as seen at the lowest specified gain control settings.

Figure 4-4: Electrical test result for ADC output for lowest gain setting.

Figure 4-5: Electric test results for ADC out for mid gain level.

Figure 4-6: Electrical test results for ADC out for high gain level.

Figure 4-7: Electrical test results on system behavior for low current input.

Figure 4-8: Electrical test result on system behavior at each stage for lowest gain level.

Section 4.3: Optical Test Results

The final testing stage for the optical power meter MTB required the characterization of the photodetector and demonstration of the full system operation in optical mode. The optical testing required much difficulty in aligning a precise free space optical test setup so that it focuses a 852nm laser diode beam on to the detector structure. Figure 4-9 illustrates the optical test bench layout. To begin with, the laser diode beam is directed through a planar-convex lens to prevent beam divergence and then sent into a beam splitter. The beam splitter divides the light into two paths for the purpose of providing an accessible measurement point so that the light can be measured and delivered to the photodetector simultaneously. One of the divided paths continues on into a fiber coupling assembly that allows precise control for positioning the cleaved fiber tip directly over the focal point of the light as it passes through a focal lens. After being coupled into the fiber, the light then travels through a second fiber mounting assembly used to direct the fiber tip onto a precise spot on the exposed surface of the fabricated MT-FPGA device under test. The chip is also mounted on its own assembly that features fine grained motion control. In addition to the optical equipment, all of the same electrical equipment is again used to control the device and monitor its performance.

Before any actual testing was performed the first step involved creating a laser and test setup characterization to capture the relationships between the laser driving current and the optical power actually delivered to various points in the optical test bench set up. Figure 4-10 shows the characterization data for 4 key test points. The characterization of the test set up makes it possible to estimate the optical power actually delivered to the photodetector as the chip is being tested.

Figure 4-9: Optical setup diagram.

Figure 4-10: Optical power characterization when testing photodetector.

The first optical test performed on the MTB was the characterization of the photodiode. Figure 4-11 shows the relationship between optical power delivered to the detector and the current response measured directly from the detector through the chip's pins. The measurement indicated that the photodetector has a responsivity of .002 A/W.

Figure 4-11: Current output of photodetector.

Following the photodetector characterization, the optical setup was readjusted to focus the light onto the correct MTB so that the entire system could be tested. Because of the disturbance to the test setup that this involved, the next step was to immediately perform another characterization of the laser and the test bench. Figure 4-12 shows the rerun of the characterization. After the characterization, the full system optical testing was conducted, and the results are shown. Figure 4-13 details the VGA output behavior when driven directly by the photodetector. The multiple traces indicate a progression of varying gain settings. Figure 4-14 and Figure 4-15 show the final system output at two different gain settings, and Figure 4-16 shows all the measured outputs of MTB system at a low gain setting.

Figure 4-12: Optical power characterization when testing MTB 1 (entire system).

Figure 4-13: Photoreceiver behavior for optical testing.

Figure 4-14: Optical test result for ADC out for low gain setting.

Figure 4-15: Optical test results of ADC out for high gain setting.

Figure 4-16: Complete view of system measurements at a low gain setting.

Chapter 5 : CONCLUSIONS

Section 5.1 Summary

During the course of this work, an integrated optical power meter system has undergone the full range of a development cycle. Starting from the specification to design a system capable of detecting and quantifying optical signals has been created. The design goals included creating a flexible and accurate power meter that would fit in a small layout area. After fabrication in a 0.35 micron CMOS process, the device was then tested in the Photonic Systems Development Lab. Together the Vbias and Vgain control signals have shown to be useful in adjusting the system to compensate for process variation and setting it up to distinguish between different ranges of optical power. The demonstrated range of operation suggests that the MTB design is most reliable when the input range is biased for input ranges that overflow for optical powers greater than 5mW. The attenuation in the optical setup limited the tested power delivered to the system to 17mW, and the system worked well when biased up to this point. Measurements of the photoreceiver responsivity at .002 A/W tell that the p-diffusion to n-well structure is generating significantly less current than expected. The electrical testing done on the chip shows that the photoreceiver works well for input currents up to 160uA.

Section 5.2 Discussion

One of the biggest limitations of the system as it is now is the very low responsivity of the photodetector structure. The p-diffusion to n-well structure typically sacrifices responsivity for speed, but previous work suggests that more responsivity should be expected from this detector structure. Going back to the photodetector layout,

it is probable that at least part of this problem is caused by the large amount of metal that lies on top of the p-diffusion contacts within the photodetector. As it is nearly all of the p-diffusion region is covered by metal intended to carry the current away from the detector. This oversight is likely the cause for such a low responsivity. Another factor that currently limits the performance of the design is the increased system sensitivity to noise at high gain settings. The extra control signals each introduce a source of external noise that make it more difficult for the system to operate with a high resolution. These difficulties will limit the range of applications for the MTB unless they can be successfully be redesigned. As it stands, the optical power meter MTB works well in the middle of the range for which it was designed, and should continue to work well in higher ranges if such large optical power values can be directed into the photodetector. One regret is that it was not possible to test the power meter in the configuration where the inputs and outputs connect through the routing of the MTLC's internal bus. As a result, any issues that might relate to this configuration have not been resolved, and no signal post processing could be performed.

Section 5.3 Future Work

The most important issue to be resolved is the modification of the photodetector so that it will produce more current for the photoreceiver. This extra current will directly affect the overall system resolution. Additionally, it might be a good idea to somehow create the analog V_{bias} and V_{gain} control signals as near as possible to the VGA so that noise on these signals can be minimized. This could be done by creating a second MTB that supplies these voltages.

References

1. P. Patel, P. Mal, F. R. Beyette Jr., "*Design of a Pixel Scale Optical Power Meter Suitable for Incorporation in a Multi-Technology FPGA.*" proceedings of 48th SPIE meeting at San Diego 2003.
2. W. Carter, K. Duong, R.H. Freeman, H. Hsieh, J.Y. Ja, J.E. Mahoney, L.T. Ngo, and S.L. Sze, "A user programmable reconfigurable gate array," in proc. Custom Integrated Circuits Conf., May 1986, pp. 233-235.
3. P. Marchal, "*Field-Programmable Gate Arrays.*" Communications of the ACM, vol. 42 no. 4, pp. 57-59. April 1999.
4. T.K. Woodward and A.V. Krishnamoorthy. "1 Gbit/s Integrated Optical Detectors and Receivers in Commercial CMOS Technologies." IEEE Journal of Selected Topics in Quantum Electronics, Vol 5(2), Mar/Apr 1999. pp. 146-156.
5. P. Bhadri, P. Mal, S. Konanki, F. R. Beyette, Jr., "*Characterization and performance evaluation of CMOS photodetectors implemented in optoelectronic circuits,*" in the Proceedings of the 45th IEEE Midwest Symposium on Circuits and Systems, vol. II, pp. 659-662, Tulsa OK, August 2002.
6. P. Mal, J.F. Cantin and F. R. Beyette, Jr., "*Design and demonstration of an optical field programmable gate array,*" in the proceedings of SPIE, vol. 4535, pp. 238-246, August 2001.
7. J. Van Campenhout, H. Van Marck, J. Depreitere, and J.Dambre, "*Optoelectronic FPGA's*", IEEE J. Select. Top. In Quant. Elect., Vol. 5, No. 2, pp. 306-315, March/April 1999.

8. P. Mal, F. R. Beyette, Jr., "*Development of an FPGA for multi-technology application,*" in the Proceedings of the 45th IEEE Midwest Symposium on Circuits and Systems, vol. III, pp. 172-175, Tulsa OK, August 2002.
9. MOSIS Web page at <http://www.mosis.org>
10. Cadence Design Kit Web page at <http://www.cadence.ncsu.edu>
11. P. Mal, J.F. Cantin and F. R. Beyette, Jr., "*Programmable photoreceiver module for incorporation in an optical field programmable gate array,*" in the proceedings of SPIE, vol.4534, pp. 138-147, August 2001.
12. R. J. Baker, H.W. Li, D. E. Boyce, "CMOS circuit design, layout, and simulation", IEEE press prod., New Jersey, 1998.
13. B. Razavi, "Design of Analog CMOS Integrated Circuits," McGraw-Hill., New York, 2001.
14. F. Beyette, P. Stanko, S. Feld, P. Mitkas, C. Wilmsen, K. Geib, and K. Choquette, "Demonstration and Performance of a CMOS/VCSEL Based Recirculating Sorter," Optical Engineering, vol. 37, no. 1, pp. 312-319, January 1998.
15. P. Mal, J.F. Cantin and F. R. Beyette, Jr., "*Design and demonstration of a Configurable Architecture for Smart Pixel Research,*" in the Proceedings of the 44th IEEE Midwest Symposium on Circuits and Systems, pp. 405-408, Dayton OH, August 2001.
16. S. Sherif, S. Griebel, A. Au, D. Hui, T. Szymanski, and H. Hinton, "*Field-programmable smart-pixel arrays: design VLSI implementation, and applications.*" *Applied Optics*, Vol. 38, No. 5, pp. 838-846, February 1999.

17. P. Mal, C. Hawk, K. Toshniwal, F. Beyette, "*Design and Demonstration of a multi-technology FPGA for photonic information processing.*" Accepted for oral presentation for 48th SPIE annual meeting at San Diego 2003.
18. A. Moscovici, "High Speed A/D Converters: Understanding Data Converters Through Spice," Kluwer Academic Publishers, Boston, 2001.
19. W. Sansen, J. H. Hijsing, and R. J. van de Plassche, "Analog Circuit Design: MOST RF Circuits, Sigma-Delta Converters and Translinear Circuits," Kluwer Academic Publishers, Boston, 1996.
20. Z. Zhao, et al. "An integrated biochip design and fabrication", *Proceedings of the SPIE - The International Society for Optical Engineering*. v. 4936, 2002, p. 321.
21. Allen, P. E., Holdberg, D. R., "CMOS Analog Circuit Design", New York, NY, Oxford University Press., 2002.