UNIVERSITY OF CINCINNATI

DATE: Oct. 25th, 2002

I, Hang Li,
hereby submit this as part of the requirements for
the degree of:

Master of Science

in:

Electrical Engineering

It is entitled:

Design Of A 32 By 32 Bit Read Head Device

For Page-Oriented Optical Memory

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Design of a 32 by 32 bit Read Head Device for Page-Oriented Optical Memory

A thesis submitted to the

Division of Graduate Studies and Research
of the University of Cincinnati

in partial fulfillment of the
requirements for the degree of

MASTER OF SCIENCE

in the Department of Electrical & Computer Engineering and Computer Science
of the College of Engineering

December 2002

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DESIGN OF A 32 BY 32 BIT READ HEAD DEVICE FOR PAGE-ORIENTED OPTICAL MEMORY

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Abstract

Extremely large capacity is needed in the next decade for the application of optical storage memory. To achieve higher data transfer rates page-oriented optical memories have been suggested as replacements for current bit-serial memories in large-capacity memory systems. Although many research endeavors have been concentrated on the development of page-oriented memory, a practical optical storage system also depends on the demonstration of optical read head technologies that are capable of reading and processing data in page-oriented fashion. This thesis explores the possibility for implementing a device to interface an ultra-high density optical storage media with an existing electronic computing hardware.

The page-oriented data read capability of a next generation read-head device is demonstrated using current CMOS technology, which is compatible with other electronic circuitry. The circuit was designed and fabricated using a conventional CMOS process. A CMOS based photodetector, which is an unconventional photonic device, was integrated monolithically onto each individual pixel on the chip, as well as the CMOS photoreceiver circuit and other control units. A 2-D pixel array was presented to realize the page-read mode. Test results verify our design of the high sensitivity photoreceiver circuit and high system throughput of the pixel array structure. The final system implementation is expected to serve as the front-end in a page-oriented optical memory system.

In the first part of the thesis, a brief introduction to the motivation and background of this project is given. A literature review is presented with an emphasis placed on the design of high performance photoreceivers. The second part of the thesis describes the design, simulation and analysis of the proposed read-head device. Individual components and the whole system are characterized and simulation results shown. While the final system is designed for implementation in a $0.35\mu\text{m}$ CMOS technology, fabrication costs limited the project to implementation of a test chip in $1.5\mu\text{m}$ CMOS technology. Finally, the performance evaluation of the fabricated test chip is presented.

ACKNOWLEDGEMENTS

First and at the very outset, I'd like to express my deep gratitude to Dr. Beyette for his mentoring and guidance on this project, as well as on other academic and life issues critical to my future study.

Great thanks for Dr. Boyd, Dr. Ferendeci and Dr. Harold Carter of reviewing my thesis and serving as my thesis committee member.

Deep appreciations toward Arvind Chokhani and Sathya Vageeshwar for their invaluable discussions on receiver design and Jianjing for his help on the system test. I would also like to thank my colleagues and seniors in our PSDL group, Prashant Bhadri, Prosenjit Mal, Kuntao Ye, Shankar Raman, Dominic Dsouza, Evan Jones and Arunansu Pattanayak, for their great minds from which I benefit most throughout my study here.

Last, but not the least, I would convey my gratitude and love to my parents in China. Without their sustained encouragements and supports, my achievements would not be possible.

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Chapter 1

Introduction

1.1 Motivation of this project

Since the invention of lasers in the 1960s, optical storage has been a hot research area. High performance optical memory systems have been well proposed and developed for high storage density and fast access time. Therefore, it is obvious to expect optical memories as a solution for applications requiring high storage capacity, such as relational databases and image processing. It is estimated that [1], over the next decade, optical storage requirements are expected to reach terabyte (10^{12}) level for personal users and the petabyte (10^{15}) level for database and knowledge base applications. In order to meet these needs, it has been suggested that future optical storage system will provide page-oriented memory (POM) access, which transcends the limitation of bit-serial method used to access the conventional optical memories. The 2-D data format provides the parallel access to an entire page at a time, which yields greater throughput than the bit-serial format, and thus offers an excellent system speed performance.

While the optical storage community has focused on the ability of next generation optical storage media to produce page-oriented optical output, the development of a practical optical storage system also depends on the demonstration of optical read-head technologies that are capable of reading and processing data in a page-oriented fashion. Previous research has been focused on the design of processing circuits for the POM, such as filtering circuit [2] or data decoding and error detection and correction circuit [3]. Little has been explored to implement a practical system for the POM using a state-of –

the-art technology. Given the fact that the illumination power from current POM is at a pretty low level, i.e. order of μWs [4], one should pay careful attention when designing such a system. For example, it is a big challenge to design the photoreceiver circuit whose threshold power is at such low level, while maintaining a high data transfer rate. Noise and power consumptions are also big issues when designing such a large and sensitive system. This thesis focuses on the design, implementation and test of a practical read-head device capable of reading one page optical data simultaneously from the page-oriented optical storage memory.

1.2 Design challenges, constraints and requirements

The goal of this project is to demonstrate the page-oriented data read capabilities of the next generation read-head device. In order to be compatible with the current electronic logic circuitry, the device should be implemented through a conventional CMOS based process. However, the inclusion of photonic devices distinguishes this Photonic VLSI technology from a conventional CMOS chip. A CMOS based photodetector will be integrated monolithically with a CMOS photoreceiver circuit, to form an individual pixel. A 2-D pixel array will be presented to realize page-oriented read capabilities. Some control circuitry will also be added to bridge the gap between the page-oriented data and word-oriented bus architecture in conventional computers. The system operation is described in Figure 1.1. Since the read-head device will integrate all necessary optoelectronic components, analog amplifiers and digital logic components, including photodetector, photoreceiver, data manipulation logic, into one single COMS chip, it is therefore based on a mixed-signal VLSI technology.

Figure 1.1 System overview of the read- head device

Several issues confront the realization of CMOS based page-oriented read-head device. First, Si based CMOS photodetector have an inherent tradeoff between speed and responsivity. In order to achieve high input data bandwidth, the optical responsivity of the detector must be sacrificed. Second, in the photoreceiver design, there is also a universal tradeoff between speed and sensitivity: the circuit will only operate at a high data rate at the cost of high input optical power levels. Unfortunately, the optical power per bit from a POM is extremely low. This fact places a challenge on the design of high sensitivity receiver circuits that maintain high operation speed. Another critical issue is how to interface the page-mode data with the current word-oriented data bus system. Control logic must be designed carefully to assure the reliability and uniformity of the circuit operation. Further, the pixel should be compact enough to be readily integrated

into an array. This need pushes the designer to reduce the complexity of individual pixels. Finally, scalability of the design is also required to increase the page size. These design factors are intertwined and must be examined with respect to each other during the design process.

With further analysis, compromises between different circuit requirements can be made, and the final design objective will be clear. First, high data transfer rate necessitates high responsivity from CMOS based photodetectors and receiver circuits. Low power output from a POM seems to aggravate this problem. However, the page-read mode of the read-head device tends to alleviate the requirement on receiver speed. For example, the read-head will read a page of data simultaneously, and the system bus is word-oriented, therefore the responsive speed for the receiver circuit is downgraded by the *page to bus size ratio*. Currently, the system bus speed has reached 133MHz in commercial computers. Therefore, for a 32 by 32 photoreceiver array, the minimum responsive speed is $133\text{MHz} \div \{(32 \times 32) \div 32\} = 4.16\text{MHz}$. Based upon above analysis, the technical objectives for this research are listed below:

- Design a CMOS based photodetector, whose responsive speed is fast enough to match the receiver circuit speed.
- Examine the constraints of CMOS technology on the implementation of high sensitivity photoreceiver circuits. Design the CMOS compatible receiver circuit operating above the minimum speed required by the read-head device (4MHz as described above).
- Design the data control logic and realize individual pixel into layout level. The control logic should be designed to work under 100MHz system bus speed.

- Evaluate the pixel performance through simulation.
- Implement layout of the whole photoreceiver array. The size of the array to be implemented in the test chip depends on the complexity of individual pixel, as well as the maximum chip area offered by fabrication brokers.
- Evaluate the test chip, and compare to simulation results to determine the individual pixel and whole system performance in comparison to the expected design specification range.
- Make conclusions and suggest future improvements to the design.

1.3 Expected contributions of this research

This research project should provide a practical interface between page-oriented optical memory and electronic host computer. The design is targeting an implementation of 32 by 32 photoreceiver array, which is compatible with current 32-bit computer systems. Therefore, it can be readily combined with other circuits serving as the front-end in page-oriented memory applications, such as database filter [2] or smart photodetectors arrays for data error-detection and correction [3]. In addition, the research will also give an insightful evaluation on the use of CMOS technology in the realization of page-oriented read-head devices.

1.4 Thesis overview

The rest of this thesis has been organized into four chapters. Sections below give a brief overview on each chapter.

Chapter 2: In this chapter, background information for this research is provided, and related literature is reviewed. A brief introduction is given to the development of page-oriented optical memory (POM). The two optical components: photodetector and photoreceiver circuit are discussed according to their performance and design tradeoffs. The requirements of scaling in the read-head design are also analyzed, along with the advantage of our design to current approach used for interfacing to POMs.

Chapter 3: This chapter talks about the design issues on the system. Detailed design methodology has been introduced with SPICE simulation results to verify our expectation. The system has been divided into individual components: detector, photoreceiver circuit, pixel, and control unit. For each section, we talk in a fixed format: First, the design objective on the component; second, detailed description on the design and simulation analysis and modeling parameters. By default, our design is implemented under $0.35\mu\text{m}$ CMOS technology. However, for the popularity of the free-fabrication for educational purpose provided by MOSIS, our test chip will be processed under $1.5\mu\text{m}$ technology. The scaling issues and results in our design are also compared and discussed. Finally the whole system implementation of 32×32 read head chip in $0.35\mu\text{m}$ technology is presented, with emphasis on layout design techniques to optimize power and area consumption. Test chip layout is also illustrated, which is an 8×8 array in $1.5\mu\text{m}$ technology.

Chapter 4: This chapter deals with the performance evaluation of an 8×8 array test chip implemented using AMI 1.5μm CMOS technology. The test setup is described, followed by test results of individual component (detector, receiver, control) and the entire system. Discrepancies between simulation and test results are also presented and possible reasons are analyzed. Finally, characterization of the chip in terms of power consumption and throughput is presented.

Chapter 5: This chapter includes the summarization and suggestion to future work to be carried out in the area of page-oriented read-head devices.

Chapter 2

Background and Literature review to the research

In this chapter, background knowledge on this project is introduced. Related research has also been reviewed. This includes the concepts of page-oriented optical memory, design issues on CMOS based photodetector and photoreceiver circuit, and read-head design scalability issues. The design objectives are analyzed at the end of this chapter.

2.1 Page-oriented optical memory

Optical storage technology is one of the primary applications developed since the invention of laser in 1960s. The sustaining interest in optical memories is well explained by their potential for high-density storage. Optical memories can store as much as 8×10^{12} bits/cm³ [5]. Therefore, it is reasonable to say that optical memories are a promising solution for applications requiring ultra high volume storage. Driven by the exploding requirements on capacity, page-oriented optical memories (POM) have been developed.

POM provides parallel access to large blocks of optical data in a two-dimensional (2-D) format. Current POM technologies include planar and volume holographic storage [24][25], spectral hole burning techniques [26], and two-photon three-dimensional memories [27]. In order to illustrate the process to generate, as well as read from the POM, we take the prevailing volume holographic storage memory as an example.

The volume holographic memory (VHM) utilizes holographic recording technology to store binary data onto a 3-dimensional optical material. Unlike conventional holography, VHM records light scattered from a special binary object called spatial light modulator (SLM). Different patterns of “1” and “0” can be modulated by the SLM in a 2-dimensional format. A typical page of binary data on a SLM might contain 1024×1024 bits and the size of each bit cell could be 15-20 microns. [6] When recording the VHM, a 2-D page-format binary data transferred from CPU is projected on the SLM. Miniature openings on the SLM serve as shutters whose open or close state represents “1” or “0” in the binary data domain. A laser beam will pass through the SLM, interfere with a reference beam at a certain angle, and form the corresponding hologram of the binary page-format data on the VHM. Another page will be recorded onto the same VHM at a different reference beam angle. This technology is the so-called “angle-multiplexing”. During the reading process of VHM, a reference beam at exactly the same angle as the one that was used to record a page is used to read the page. This beam will interact with all holograms on VHM, but only the angle-matched page will be reflected and an output light will be generated corresponding to that of the binary data page. This phenomenon is explained by the Bragg effect, which also indicates the low diffraction efficiency for the unwanted pages due to the angle mismatch between reading and recording beams. The optical output from the POM is focused onto an array of photodetectors-receivers that converts it to a page of digital signals. Then the binary data page is reconstructed and transferred back to the CPU. A different page can be read independently at a different reference beam angle.

POM excels in high data-rate performance for two reasons. First, nonmechanical optical addressing leads to extremely fast access time. The POM almost instantaneously

reconstructs the optical data page at the speed of light. Second, the 2-D data format provides parallel access to an entire page at a time, instead of reading one bit data per time in conventional CD-ROMs. In the current SLM size up to 10^6 bits, the data transfer rate will be on the order of 10 GB/s [12]. Therefore the system speed of the read-head device is only limited by other peripheral components, such as the SLM, align elements, photodetector array, output data bus, etc.

In addition to those sophisticated optical components required for recording and detecting in POM systems, electronic circuits are also needed to format and channel the reconstructed page data, and to interface with an electronic host computer. The detection of the optical data page will generate analog signals, ex. photo current, that be thresholded to produce digital outputs. The output data should be reformatted to produce a word-oriented data stream compatible with current computer architectures. These tasks outline the work required in developing a read-head device for a practical POM storage system.

Charge-coupled device (CCD) arrays are used widely in current POM systems to perform optical to electrical (OE) conversion and data transfer. Although CCD arrays can read optical data in parallel, the serial output nature impedes them from high data-rate transfer. Typical CCD speed ranges from 100kHz to 1MHz. High speed CCD array requires small pixels ($<10\mu\text{m}$) to obtain low-capacitance and multiple-parallel readout channels. However, the SLMs in recording POM are limited to a size of $15\mu\text{m}$ [7], which makes CCD array unrealistic to be aligned to the recording media. Further, the quantum efficiency of most CCDs' decreases sharply at longer wavelengths, and many even have no sensitivity beyond 700 nm, impacting the choice of recording material and laser. In

order to compensate for the above problems, in this project we present a 2-D photoreceiver array with one CMOS based photodetector integrated monolithically together onto each pixel. The detector window can be varied by choosing appropriate detector structures, and the quantum efficiency in wavelength spectrum is also ideal for silicon CMOS photodetectors. A detailed introduction will be given in the following sections on previous research results of CMOS based photodetectors and photoreceiver circuits. Although the system throughput can be increased from the proposed solution, one shortcoming is foreseeable which is the relatively huge area consumption for the implementation of a large photoreceiver array.

2.2 CMOS and OEIC

Over the past decades, people have witnessed the powerful performance that the integrated circuit has achieved and the endless quest to integrate more functionality of electronic systems onto a single chip. CMOS technology has gained the greatest success in this regard. This is a direct result of the advantages associated with a CMOS process, which include mature technology, resourceful design tools, low price, scalable nature, etc.

In a CMOS process, both NMOS and PMOS transistor are fabricated on the same substrate. For example, in an n-well process, the N type diffusion region is provided in the P type substrate which hosts PMOS device. Alternatively, NMOS is formed in the P substrate region. The gate oxide, poly-silicon gate and source-drain contact metal are shared between PMOS and NMOS transistors, but the source and drain implant region must be done separately. Different transistors are isolated by field oxide on the same substrate. When connecting these devices, the source regions of the NMOS and PMOS transistor are connected to ground and V_{dd} respectively. P-substrate contacts are tied to

ground while N-well contacts are biased to V_{dd} . In this way, body effect introduced by source to bulk potential can be eliminated.

One of the advantages of a CMOS device compared to NMOS circuits is that its digital output value can reach to either V_{dd} or ground. This large voltage swing between different logic values leads to a large operation margin for digital circuit. Another important virtue of CMOS technology is its low power dissipation. Either the PMOS or NMOS device is turned off during the circuit static state, yielding almost no static power consumption. The dissipation will only occur at the short transition period when circuit switches between logic states. However, the CMOS circuit suffers from a lethal property, namely latch up. Simply speaking, it is a condition in which the parasitic bipolar transistor existing between CMOS devices enters a conducting state. This occurs when the two transistor are far apart and will cause excessive power consumption, and even logic failure. Separation of PMOS and NMOS device can solve the latch up problem. Another solution is to put N-well and P-substrate contacts as close as possible to decrease the parasitic resistance value associated with the latch up circuit. The speed of CMOS circuit is not as fast as NMOS implementation because of the introduced low mobility PMOS transistors.

Recently there is a trend to integrate other components on the same chip with electronic circuits [22]. Hybrid VLSI-optoelectronics (OEIC) exploit the respective strengths of optics and electronics for the production of optical information processing systems of high performance. These devices combine the massive parallelism offered by optical interconnections with powerful processing capabilities of CMOS electronic circuits. The integration of light emitters, detectors and SLMs have been demonstrated, which refers to

a great amount of applications in optical communications. A prospective research arena has emerged in the applications of optically interconnected CMOS chips. For our research purposes, we explore the potential of current OEIC technology in the application of interfacing the page-oriented optical storage memories with electronic host computers. This chip enjoys a multi-technology mixed-signal feature of CMOS chip since it is responsible for processing optical, analog, and digital signals at the same time.

2.3 Photodetectors

2.3.1 Introduction to photodetectors

Photodetectors are semiconductor devices that receive incoming light signal and convert it into an electronic representation. Several parameters characterize the performance of the photodetectors:

- Responsivity: The current generated by unit power incident light. (unit: A/W)
- Spectral Response: the absolute responsivity as a function of the wavelength.
- Quantum efficiency: the percentage of the photons detected compared to the total photons received.
- Noise Equivalent Power: the radiant power that produces a signal equal to the noise signal from the detector. The noise may result from background irradiation or non-optical generated electron-hole pairs in depletion region of the detector.
- Response Time: “Rise time” is the time difference between the 10% point and the 90% point of the peak amplitude output on the leading edge of the pulse. “Fall time” is measured between the 90% point and the 10% point of the trailing edge of the pulse waveform. The time measured between the 50% value of peak current

and the 50% peak power of incident light on the surface of the detector is called the “Delay time”. These figures determine the operating frequency of the detector.

- Dark current: The current obtained when the detector is biased at normal condition without illumination.

The basic merit metrics evaluated by a good photodetector include high sensitivity and responsivity at a desired wavelength, low noise, fast response, insensitivity to thermal changes, compatibility with fiber dimensions, etc. PIN diode and avalanche photodiode [23] are two basic types of photodetector. Semiconductor p-n junctions are used widely for photon detection. The main physical mechanisms involved in junction photodetection are illustrated in Fig 2.1.

Fig 2.1 Operation of a P-N junction photodiode

The junction is reverse biased, and photon is absorbed to stimulate an electron to the conduction band, leaving a hole in the valence band. Electron-hole pairs created by the absorption process will eventually recombine with one another if no electric field is presented. Only those carriers generated in the region of high electric field or close enough for them to diffuse into it have an opportunity to be collected as photocurrent.

Consequently two factors contribute to photocurrent: diffusive transport and field-aided transport. In contrast with the field-aided transport, the diffusion-based component will have a much slower time-response associated with it. Photodetectors are important in optical communication systems operated in near-infrared region (0.8-1.6 μm). In our application, we attempt to use CMOS based photodetector as image capture device instead of the conventional CCD approach. The laser wavelength for recording/retrieving optical data spans from 500nm-700nm for current technology. However, since our test facility can only provide controllable laser source at 850nm, a high responsivity design in this near-infrared region is desired. In addition, the detector should be compact in size and easy to be integrated with other electronic circuits.

Different materials are used according to different requirements on the detector performance. For example, in the 800nm-900nm range, GaAs MSM detectors are used for very high speed OEIC receivers, while in 1.0 μm -1.65 μm range, Ge is used because it has a higher absorption coefficient and good sensitivity. Although Si detectors are slow in response compared to their direct-bandgap counterparts, such as GaAs, AlGaAs, the gradual onset of absorption coefficient of Si makes it ideal for detection for wide range of wavelength in the vicinity of its bandgap. This is due to its indirect-bandgap nature. With the $E_g=1.1\text{eV}$, Si can sensitize light in a spectrum from 0.6 μm to 1.2 μm .

2.3.2 Si Technology for photodetector

Different technologies suffer tradeoffs in the design of integrated photodetectors. The two prevailing technologies currently available nowadays are Bipolar/BiCMOS and CMOS.

As mentioned previously, CMOS technology enjoys a good reputation for low power consumption and high integrating capability. Bipolar devices, on the other hand, provide high switching and I/O speed due to large driving current generated from them. In order to take the advantages of both technologies', BiCMOS process has been introduced to improve the speed in CMOS and reduce the power dissipation in bipolar circuits. BiCMOS differs from conventional CMOS technology by the use of the retrograde doping introduced for the collector region in CMOS devices. As shown in Fig 2.2, an N^+ buried layer can be achieved by either high-energy ion-implantation or epitaxy. The N collector contact will be trenched through the N-well region in conventional CMOS process and made ohmic contact with the N^+ buried layer. Base (P) and emitter (N) region will also be realized in N-well region. The most disadvantage of BiCMOS technology is the process complexity, which leads to a great cost increase over original CMOS circuit.

Fig 2.2 Illustration of BiCMOS process

Extensive research has been conducted in the area of high performance Si photodetector development. For example, in Hartman's et al. work [8], a silicon bipolar detector is implemented by several steps of process modifications. A P-I-N detector between the substrate and the emitter contact is realized and the responsivity is 0.5A/W at 820nm with operation speed of 250MHz. In another example, Wieland et al. [19] designed a detector implemented between the base and collector layers in the bipolar devices without special process step. The detector responsivity is limited to 0.045A/W at 850nm, but a speed up to 5GB/s can be reached. These examples present the tradeoff embedded in the implementation of Si detector- that of responsivity for speed. This tradeoff is further exemplified in CMOS technology. In the conventional CMOS process, a detector can be realized by the parasitic P-N junction between n-well and p-substrate. A responsivity of 0.3A/W at 850nm can be easily achieved. But the responsive speed is not optimized because of the diffusive carriers created in the bulk region. Several solutions are introduced in order to improve the speed. As described in [20], a low doped substrate material is grown during the process in order to have the surface electric-field penetrate deep enough to extract excessive photo-generated carriers. While in [21], a novel concept of amplifying the spatial gradient in carrier concentration is introduced to compensate for the slow response problem. However, these attempts all require additional treatment on conventional CMOS process, which will increase the production cost. It is obvious to conclude that, a much more optimized process will certainly facilitate the design of high performance Si detectors. In contrast with an integrated detector along with other electronics on the same chip, the performance must be sacrificed due to the already-established process procedures. In our read-head design, we use an unmodified detector design to be compatible with low cost CMOS technology.

2.3.3 CMOS based photodetector

There are four types of CMOS compatible photodetector structures [10], as shown in Fig 2.3: a) N-well to P-substrate photodiode, b) P⁺-diffusion to N-well photodiode, c) P⁺-diffusion to N-well and N-well to P-substrate photodetector, and d) BJT phototransistor. While the first three structures use the parasitic P-N junction fabricated during CMOS process, the last one is implemented using a P⁺ diffusion in an N-well to form the emitter and base region and the P-substrate (which is grounded in the n-well CMOS process) acts as the lightly doped collector region. During operation, the photodiode is reversed biased to receive light in the junction region. And the phototransistor is biased in a floating base configuration by applying a positive potential to the emitter with current generated at the floating base region.

Fig 2.3 Four CMOS based photodetectors [10]

I-V characteristics, transient analysis, spectral responsivity have been made on each structure. Generally speaking, the phototransistor possesses a good responsivity while

suffers a bad responsive speed. On the other hand, photodiode shows a good transient characteristic but a poor responsivity. The combined diode structure in Fig 2.3(c) can improve the responsivity to some extent. While other techniques can also be included to further enhance such detector's performance.

In our design, we explore the fastest speed ever achieved to read the POM. Therefore, P-diff to N-well structure is selected. The rise and fall time is extremely fast, i.e. less than 0.1ns, corresponding to a large signal response over 1GHz. The operation wavelength is designed for near infrared region (600-800nm) for the recording and reading laser at this region. Typical responsivity value ranges from 0.02-0.04A/W. Techniques to improve the responsivity will be introduced and detailed design will be shown in Chapter 3.

2.4 Photoreceiver circuit

Photoreceiver circuit senses the optically induced current and converts it to a voltage level for subsequent electrical processing. In operation, the receiver circuit is integrated with a photodetector to receive the photo-generated current signal. Different detector-receiver schemes have been widely demonstrated, such as PIN-FET, APD-FET, III-V OEIC receiver [23]. In our design, the CMOS based receiver circuit will be designed and integrated with CMOS photodetector. The design involves current source, amplifier and decision circuit, etc., which are the main components of any analog circuit. The performance of a receiver circuit can be evaluated by the following characteristics.

- **Data Rate:** the amount of data bits transferred by receiver per second. Normally non return to zero (NRZ) code is used for the receiver circuit operation.

- Bit Error Rate: the probability of error bit caused by receiver circuit when converting large amount of data. This feature depicts the anti-noise capability of receiver.
- Sensitivity: the minimum power level for thresholding receiver circuit.

In our POM application, all photoreceivers in the array should operate concurrently to achieve parallel data acquisition. Several concerns are associated with the optimization in the receiver design. First, optical energy per bit at the receiver input is extremely low due to the well-known $1/M^2$ drop in diffraction efficiency of the read-out beam, where M is the number of pages VHM stores [12]. This requires that the detector and receiver circuit be sensitive to low optical power if a large number of pages are to be stored. Unfortunately however, there is generally a tradeoff between input power and switching speed in CMOS photoreceiver circuits. Therefore, careful consideration must be given to the design of the photoreceiver so that the speed of this circuit does not limit the throughput of POMs. Second, because the receiver will be replicated on a large array structure, layout area and power consumption must be minimized. Finally, since the receiver performs the thresholding of the optical signal, it is desirable that this component be tolerant to noise due to the fluctuations in optical intensity during the reading from POMs.

While CMOS based photoreceivers for optical communications and smart pixel applications have been shown to provide both high data rates and low BER, the minimum optical power requirements for them are significantly higher than those expected for POM systems. As a matter of fact, implicit in the demonstration of high data rates ($>1\text{Gb/s}$) and low BER (10^{-10}) is the fact that these performance metrics are only

achieved at input power levels orders of magnitude larger than the output power from POMs. This tradeoff between sensitivity and data rate presents significant challenges to the design of photoreceiver circuits.

Two photoreceiver designs are reviewed which are conducive to our research. In Woodward and Krishnamoorthy's work [11], 3 cascading push and pull amplifiers are presented to perform thresholding. The detector used is P-diffusion to N-well CMOS compatible with an active area of $16.54\mu\text{m} \times 16.54\mu\text{m}$ and dark current of 1nA. The responsivity ranges from 0.01-0.04A/W at increased biased voltages. The output and input of the first push-pull amplifier is coordinated by a PMOS transistor, forming a simple transimpedance stage. The transimpedance of the first stage can be adjusted by changing the gate voltage of the PMOS transistor. There is an active load NMOS transistor placed between the second and third push-pull amplifier to adjust the gain and switching point of these threshold stages. The interaction between the additional PMOS and NMOS transistor to the push-pull amplifiers is key to the receiver circuit operation. The circuit is implemented under $0.35\mu\text{m}$ technology and tested with 850nm lasers. At a given data rate, V_{tune} was adjusted for optimum performance. The V_{dd} ranges from 1.8V to 3.3V during operation while the best sensitivity was obtained at a supply bias of 2.3V. A BER of 10^{-9} is obtained at an average optical input power of -6.3dBm (0.234mW). The sensitivity of the receiver improves at lower data rates, with a BER of 10^{-9} requiring an average input power of -8.6dBm (0.138mW) at 622Mb/s and -14dBm (0.04mW) at 155Mb/s. The most attractive feature of this receiver is its high operation speed due to the simplicity and compact size. At the same time, we notice that the sensitivity for this circuit is relatively low, i.e. 40 μw over 100Mb/s data rate. This level is not suitable for

the application of reading POMs. However there is a trend towards high sensitivity when decrease the data rate, providing possible modification to this circuit to meet our demands.

Tang et al. demonstrated another design [1], which is aiming for achieving high sensitivity. The circuit consists of a bipolar junction phototransistor, a three-stage current amplification circuit, an active load transistor and an adjustable reference comparator. The circuit was implemented using a $1.2\mu\text{m}$ CMOS process. The base contact of the phototransistor is floating to receive incoming light. The photogenerated current is amplified by three current gain stages and is mirrored through a unity gain NMOS mirror. Then it passes an active load NMOS transistor yielding a voltage level that is dropped from the V_{dd} supply (5V). This voltage is fed into one of the input of the adjustable threshold comparator circuit. The comparator compares the optical converted voltage signal with user defined reference voltage and produces the logic value based on comparison results. By varying the reference voltage the optical power threshold changes. Test results show a sensitivity of 0.5nW (-63dBm) is achieved at a reference voltage of 3.2V . Although ultra-sensitivity was realized, this circuit suffers from an extremely slow speed, which makes it less than ideal for interfacing to POMs. This problem arises from the low responsive nature of phototransistor and current mirrors. The diffusive current in phototransistor leads to a very slow turn-off speed, while the switching of current signals in current mirrors is not as fast as voltage signals, making the frequency response worse. The speed of this circuit under simulation is only 300 KHz , not enough for our need in POM application (the minimum receiver speed is $3\text{-}4\text{MHz}$ as described before). Improvements can be conceived to increase the speed, such as to replace the BJT phototransistor with a faster P-N junction diode. However, the responsivity of the photodiode is often two orders of magnitude lower than that of the phototransistor: the

transistor used in above circuit possesses a responsivity of 20A/W, while the most common p-diff to n-well diode's responsivity is only 0.04A/W. Therefore at the same threshold current value, the optical threshold power to the photodiode circuit is much higher than that for the phototransistor, affecting the sensitivity to a great extent. Some gain stages (current mirrors) should be added to the circuit to maintain the performance, which will inevitably introduce more time delay between stages. So it is obvious that we ought to convert the current signal at the earliest stage in order to achieve better time response characteristic for the receiver circuit.

Based upon above two photoreceiver circuits, our research is focused on the realization of high sensitivity circuit operating at MHz levels. With reference to the second circuit, the basic goal is to use the fastest p-n junction diode and design the circuit working at a threshold power level comparable to POM requirement.

2.5 CMOS scalability issues on the read-head design

One of the great advantages of CMOS technology is its design scalability. One can easily shrink the circuit to a smaller feature size. The smaller dimensions on transistors will enhance the circuit performance in many ways. First, the circuit area will be reduced to a great extent. Therefore high yield will be expected in a certain area of silicon real estate. More functional circuits can be added on chip in a fixed area too. Second, the parasitic capacitance during CMOS process will be smaller, which will increase the circuit speed and decrease the dynamic power consumption. The power consumption can be further decreased by scaling the value of power supply V_{dd} . All these features provide us a good reason to scale our design in this project. Most important however, in the volume holography page-oriented memories, a larger page size is desired to maximize optical

power for each pixel [12]. If the retrieval time of the system is fixed, the data transfer rate can also be increased by larger page size. Therefore it is necessary to explore the scalability of the read-head design so that the capacity and system throughput can be maximized. In this project, the design is initially implemented in 0.35 μm technology. The shrinking of our design to smaller technology will generate a larger array. Several critical issues are associated with the scalability of the design as follows.

- Pixel size and complexity constraint.

The scalability of the read-head design depends on the size of individual pixel. Smaller pixel size apparently will generate larger page size in a fixed chip area. The size can be measured by the area of individual pixel. According to Semiconductor Industry Association (SIA) roadmap, the maximum chip area is estimated to 4cm² for 0.35 μm processes. Therefore, this limitation gives the upper bound for the single chip scalability.

- Dynamic power consumption constraint.

There is current going through CMOS logic gates during their transition between logic states. This current leads to dynamic power consumption. In addition, current is also required to charge and discharge the output capacitive loads, which is another great contribution. Power estimation shows a skyrocketing value for a big photoreceiver array. Smaller feature size design and V_{dd} value will decrease the power consumption when scaling. Given the maximum power dissipation value by SIA roadmap, ex. 70W for 0.35 μm technology, the limitation of power consumption on the read-head page size can be calculated as long as we know the individual pixel's power dissipation level.

- Optical power budget constraint.

Low optical power budget is required in POM read-head design. The low input power value will affect the responsive speed of the photoreceiver circuit, which in turn decreases the system throughput. Following the analysis of Schaffer et al. [12], for typical POM values of 50mW illumination power, assuming the power is distributed evenly among all pixels and half of the pixels are “1”s, the available power per pixel

is $P_{pixel} = \frac{\eta P_{in}}{0.5 N_p}$, where η is the value of diffraction efficiency from VHMs. With an

addressing time of τ , by the definition of the switch energy for the photoreceiver circuit

$E = P_{pixel} \tau$, the number of pixels in one page $N_p = \frac{2\eta P_{in} t}{E}$. The relationship between

page size and switching energy for the receiver circuit at a fixed addressing time therefore can be derived. From this relationship we can determine the ideal page size is 10^3 for $\tau=10\mu s$, $\eta=10^{-4}$. This value is far smaller than those limited by chip area and power consumption, which makes the optical power the primary factor affecting read-head scalability.

Based upon analysis, we design a 32×32 (1024) receiver array in accordance with the page size limited by optical power budget described above. The switching energy of the receiver in this range is 30-50 fJ. This design is also compatible with current 32-bit computer hardware. The system bus speed is targeting at 100MHz. Detailed analysis on circuit scalability and optimized page size will be made in Chapter 3.

Chapter 3

Individual Components and System Design

This chapter talks about the individual components and system design of the read-head device. The topics are in sequence of photodetector, photoreceiver circuit, control unit, pixel, array and final chip implementation. Design objectives and methodology are introduced along with simulation results. With the exceptions of detector and receiver circuit, all components are designed, by default, for 0.35 μm implementation. The detector and receiver circuit are initially designed in 1.5 μm technology and then scaled down to 0.35 μm technology. Changes of simulation results are presented, along with the modification to the circuit requested to maintain the same desired performance as that in 1.5 μm implementation.

3.1 Photodetector

3.1.1 Design Objective

While the photodetector is the only optical component in the system, it must be implemented in a way that is compatible with CMOS technology. As described in Chapter 2, four CMOS compatible device structures are possible. A tradeoff between responsivity and speed is inherent in the design of CMOS based photodetectors. For our design purposes, we expect detector speed not to significantly limit system performance. Therefore, the fastest structure, P-diffusion to N-well diode, is chosen in our design.

3.1.2 Device structure and circuit implementation

Fig 3.1 P-diffusion to N-well structure [10]

As shown in Fig 3.1, this structure uses the P-diffusion to N-well junction as the active region to detect the incoming photons. During operation, the N-well contacts are connected to positive potential, giving a reversed bias between the P-N junction. The P-substrate is biased to ground, which is in consistent with CMOS device operation. The generated current flows out of P⁺ contacts. Therefore, the contacts should be connected to the receiver circuit such that the photo-generated current flows appropriately in receiver input amplifier stage.

Simulation has been performed by 2-D device simulation software Medici [10]. Results show a low photo response at $\lambda=853\text{nm}$ (Fig 3.2). This is due to the limited carriers generated in the shallow P-diffusion region. Incoming light is mostly absorbed in the P bulk region instead of the P-diffusion regions at surface. So the current flow from P⁺ contacts is very small, leading to low detector responsivity. However, the transient response is very fast. From Fig 3.3 we can see that the rise and fall time of this detector is

less than 0.1ns, corresponding to operating speed in the GHz regime. The extremely fast speed is due to the electric-field aided transport of carriers. After being stimulated, photo-generated carriers will immediately be swept out of junction due to the short active region dimension. The reverse biased N-well to P-substrate diode acts as a screening terminal which impedes carriers generated in substrate from being injected into P^+ terminals. Therefore, almost no diffusion current contributes to the total current from P-diffusion region, causing the transit time very fast.

Fig 3.2 Responsivity characteristic of P-diff to N-well detector [10]

Fig 3.3 Transient characteristic of P-diff to N-well detector [10]

In order to improve the responsivity, we introduce an interdigitated P^+ diffusion network to increase the active region. It is observed that the photo current increases linearly with the increase in the number of fingers in the network. Another important factor to the design is the spacing between adjacent fingers. From Fig 3.4 we can see that the photo current is slightly higher before the finger spacing is close to the depletion region of the p-n junction and decreases until $4\mu\text{m}$ and increases again until $7\mu\text{m}$. The overlapped depletion region is actually a waste of silicon active area. The current is almost constant from that point where two fingers are completely separated from each other. Hence we can achieve optimum photocurrent by having the fingers spaced $7\mu\text{m}$ apart from each other.

Fig 3.4 Photocurrent vs. Finger spacing [10]

3.1.3 Detector Layout Design

The detector layout is shown in Fig 3.5. It is in shape of rectangular. P⁺ substrate contacts surround the N-well active region serving as the guard rings. They are tied to ground to isolate the highly sensitive optical component from nearby electronic circuits. 3 fingers are made in the N-well region. The area of the active region is confined by other circuits' area in the pixel design which will be discussed later in this chapter. All P⁺ terminals are connected together to be fed into the following receiver circuit. Considering the low current output from the detector region, the metal wire connecting the detector and receiver is made wide enough to decrease the resistance of the metal lines. The spacing between P⁺ fingers is set to 7μm and the width of the P⁺ fingers is governed by specific

process design rule (In $1.5\mu\text{m}$, $W=3\lambda=2.4\mu\text{m}$). The final size of the detector window is $30\mu\text{m}\times 30\mu\text{m}$.

Fig 3.5 Detector Layout

3.1.4 Design Scalability

Since the above analysis is based upon the $1.5\mu\text{m}$ technology, scaling down to $0.35\mu\text{m}$ implementation may cause performance changes of the detector. The actual window size will be scaled down to $6\mu\text{m}\times 6\mu\text{m}$ for a $0.2\mu\text{m}$ feature size process. One may expect a decreased responsivity due to reduced active region. However, the doping level will increase in $0.35\mu\text{m}$ technology because of the condensed device dimensions. This will help compensate for the small active area. The optimum finger spacing should not be affected too much when scaling down because the same scaling ratio on width and length of the design. Based upon the assumption that the detector area is large enough for carrier collections, the responsivity in $0.35\mu\text{m}$ implementation is expected to be larger than that in $1.5\mu\text{m}$'s. From chapter 2 we know the typical responsivity value for P-diffusion to N-

well structure is 0.02-0.04A/W. This range will be used during the following receiver circuit simulation.

3.2 Photoreceiver Circuit

3.2.1 Design Objective

Low cost, high reliability and high performance photoreceivers are essential for application in long-haul optical communication and photonic information processing systems. CMOS based photoreceiver circuits provide an alternative way to solutions based on III-V materials. While it benefits from low cost and mature technology, CMOS technology faces many design challenges in the implementation of high performance monolithically integrated CMOS photoreceivers. As to our design requirements, the photoreceiver comprises the most sensitive electronics of the CMOS chip due to high gain and bandwidth requirements. However, the tradeoff between sensitivity and speed suggests that the two characteristics should be balanced during the design in order to achieve our design goals.

There are a couple of guidelines in our design. First, as mentioned in section 1.2, the parallel reading nature of the read-head will compromise the speed requirement on the photoreceiver. Because our design targets at 100MHz system bus speed, the minimum operation speed for a 32×32 array will be 100MHz/32=3.125MHz. Second, low optical power coming from the POM will limit the page size of the receiver array to 10^3 pixels. The switching energy for receiver in this range is 30-50fJ as discussed in section 2.5. By introduction of effective switching energy [12] $E_{\text{eff}}=R \times P_{\text{thres}} \times \tau$, where $R=0.04\text{A/W}$ is the

detector responsivity of our design, and $\tau=1/3.125\text{MHz}=0.32\mu\text{s}$ is the accessing time with respect to receiver speed, the required threshold power is $2\text{-}4\mu\text{W}$. Considering the uneven power distribution in the real optical system, threshold power less than $1\mu\text{W}$ are desired. The threshold current for the receiver turns out to be around 40nA . Consequently, our objective is targeting a receiver circuit that amplifies small input photocurrent around 40nA to logic-levels of 0V and 5V (or 3.3V in $0.35\mu\text{m}$), while at the same time operates at $3\text{-}4\text{ MHz}$. In addition, the circuit area should be minimized so that larger array can be generated in a fixed area. The design is first introduced in $1.5\mu\text{m}$ implementation, followed by scaling down analysis of the circuit and final design in $0.35\mu\text{m}$ technology.

3.2.2 Design methodology and circuit diagram

Our design idea is based on the circuit [11] described in section 2.4. In that circuit, the operation speed is extremely fast, i.e. 1GHz , but requires a relative large optical signal ($0.2\text{-}0.3\text{mW}$). Therefore, by introducing some amplification stages, the circuit speed can be tailored to our need. The final schematic of the design meeting our requirements is illustrated in Fig 3.6. As can be seen, the photoreceiver consists of three primary stages: The photodiode and transimpedance preamplifier comprise the first stage. The photodiode provides current input signal. A push-and-pull amplifier serves as the transimpedance amplifier with a P-MOS transistor connected between the input and output to give the feedback mechanism. The feedback resistance can be adjusted by changing the gate voltage (V_{TUNE}) of M3. For a $V_{\text{dd}}=5\text{V}$ system, the gate voltage of the feedback transistor is 2.5V for operation at $1\mu\text{W}$ power level.

After the transimpedance stage the second stage which is comprised of a differential amplifier followed by 2 common source amplifiers. The purpose of this stage is to produce a single-ended output whose voltage swing is sufficient to switch the subsequent buffer stages between digital values (0V, 5V). Since the second stage is the last linear stage in the circuit, the bandwidth of the receiver is primarily determined by the transimpedance stage and differential gain stage. The differential stage is simply an actively loaded CMOS differential amplifier, with NMOS loads and PMOS input transistors. The current source for the differential amplifier is simply a PMOS transistor biased in saturation region. It replaces the normal current source for its simplicity. Although the current value is not stable, simulation result shows that it is still in the tolerable range for correct operation. The size of M10 and M12 are designed such that the two cascaded common source amplifiers can swing the voltage to the switching point of the buffer inverters.

The buffer inverters make up the final stage of amplification in the design which pushes the output voltage to logic levels. Two inverters are needed in order to have the correct logic value. By insuring that the buffer input voltages swing spans around the inverter switching threshold region, we can guarantee that the receiver output does not stick to Vdd or ground values.

3.2.3 Simulation results

3.2.3.1 Photodetector model during simulation

Fig 3.7 Simple photodetector model including the photocurrent source and shunt capacitance

Due to the lack of CAD tools, we can not simulate the receiver circuit performance with detector attached. Therefore it is necessary to illustrate the detector model we used before we present the simulation results. As illustrated in Fig 3.7, the simple model of the photodiode consists of two parts: the shunt capacitance C_{pd} , which is the P-N junction capacitance C_j combined with the receiver circuit input capacitance C_{in} ; and the photon generated current fed into the circuit I_{pd} . Because of the simple nature of the device, the photocurrent can be represented as a simple constant current source. In later simulations, a voltage-dependent (voltage is treated as the light power source) current source is used to model the photocurrent whose gain is equivalent to detector's responsivity value.

Since the shunt capacitance C_{pd} serves as the input capacitance of the receiver circuit, it will limit the receiver speed. Rough estimation to the value of the capacitance is needed

when doing AC analysis. The simulation results as the input capacitance value is varied are presented in section 3.2.3.3.

3.2.3.2 DC Performance

According to our design methodology, the DC response requires the circuit toggle the output logic value from 0V to 5V at a current input around 40nA. As shown in Fig 3.8, different locations in the circuit are examined as we sweep the input photocurrent through its threshold range. A recent BSIM model is used (T21M from MOSIS February Runs). The sizing of M2 and M4 is key to the operation of the circuit, which determines the first stage transimpedance gain and second stage current source value. At the transimpedance stage, the L/W ratio of transistor M2 is designed such that it will transfer the input current value near threshold range (40nA) to an equivalent voltage swing of 1mV (node A), yielding a transimpedance of 25K Ω . The gate voltage of M3 is adjustable to modify the transimpedance value. However, in order to avoid the inconvenience of introducing extra bias circuit, we set it to Vdd. The differential stage then amplifies this voltage swing to over 900mV (node B). One input of the PMOS pair is connected to ground for the same purpose of circuit succinctness. The current source value used in the differential gain stage is 70 μ A. This value is critical to the circuit performance. The normal current mirror is replaced by M4 in the final design to minimize the area consumption. The width of M4 is adjusted such that the current flowing through it resembles that in the normal current mirror structure. Simulation shows the swing of current flowing through M4 is from 69 μ A to 71 μ A.

Fig 3.8 Photoreceiver DC Response, including the (A) Transimpedance output, (B) differential gain stage output, (C) first common source amplifier output, (D) second common source amplifier output, (E) voltage swing of the first buffer inverter, as a function of input photocurrent

Although the current is not constant, the swing is sufficiently small to allow correct operation of the circuit. It should be noted that this scheme yields a 11% saving in pixel area compared to the normal design. The following common source amplifiers finally increase the voltage to $\sim 2.5\text{V}$ (at 40nA threshold) which is sufficient to adequately switch the buffer inverters. The gate lengths of all transistors are the same ($5\mu\text{m}$) except for M2. The overall gain of the stages is roughly $4.5 \times 10^7 \Omega$.

Different models are used in the dc simulation to evaluate the design robustness across process variations. The threshold current varies from 10nA to 50nA . Furthermore, Monte Carlo simulation of the dc response over varying SPICE model parameters suggests that the 40nA threshold range is achievable.

Fig 3.9 shows the threshold power simulation for the receiver circuit. A voltage controlled current source (VCCS) is used in place of the constant current source. The controlling voltage source acts as the input power source. As we vary the gain of VCCS from 0.02 to 0.04, which is the typical range of responsivity of the detector, the threshold will shift left. However, the $1\mu\text{W}$ power is enough to toggle the receiver circuit in all cases. Note in Fig 3.9 that the x-axis is in units of μV . This is due to the fact that a voltage source is used to model the optical signal illuminating the detector. In a real device, the x-axis units μV would map to μW .

*Fig 3.9 Photoreceiver Threshold Power Simulation
Note x-axis units μV maps to μW in a read device*

Fig 3.10 illustrates the Monte Carlo simulation of the process variation effects on circuit performance. Most recent fabrication parameters are observed and several important parameters are analyzed [15]. The analysis sweeps parameter values that are chosen based on statistical variations. Results show two primary factors contribute most to the performance, which are maximum carrier drift velocity, V_{MAX} , and zero-biased threshold voltage, V_{TO} . However simulations reveal that the variation of threshold power will not exceed $1\mu\text{W}$ limit, which makes the parameters effect negligible.

(a)

(b)

Fig 3.10 Monte Carlo simulation of a parameter uniform distribution with 50% relative variation on (a) VMAX, maximum carrier drift velocity (m/s) and (b) VTO, zero-bias threshold voltage(V) in a 50 runs iteration period.
 $R=0.04A/W$. Note x-axis units μV maps to mW in a read device

3.2.3.3 AC Performance

Another important characteristic of the receiver performance is the AC response as a function of input detector shunt capacitance. The input capacitance includes the capacitance from the P-diff to N-well detector and capacitance at the input node of the photoreceiver. Hand calculation shows a value of 160fF according to the model we used. We performed simulation of the design over different models as we varied the capacitance between 200fF and 1pf. The ac response is measured at node D, which is the output of the second common source amplifier. As Fig 3.11 shows, at low frequency range, the response is independent of input capacitance. The 3db decade bandwidth of the photoreceiver is 200 KHz. This value is far less than the 3-4MHz requirement. Better performance is expected when implemented in a smaller feature size, such as in 0.35 μ m technology.

Fig 3.11 Simulated Photoreceiver AC response

3.2.3.4 Transient Analysis

Fig 3.12 Simulated Photoreceiver transient response

Finally we simulated the transient response of the photoreceiver. The frequency of the input light power source is 50 KHz, i.e. 100Kb/s NRZ rate, switching between 0 μ w and 1 μ w. Rise and fall time of the input signal are equal to 100ns.

Fig 3.12 illustrates a good receiver response. The delay time of T_{PLH} and T_{PHL} measured from this figure is 2.15 μ s and 1.92 μ s respectively. The corresponding frequency response is 245.7 KHz. Although this circuit suffers from poor speed, the rise and fall time is pretty fast, 0.2 μ s altogether. It should be noted that in this simulation, no load capacitance is added at the output of the receiver. While this is not a completely accurate representation, the load capacitance is expected to be small since the receiver circuit will be connected to a digital circuit in the pixel, i.e. D-latch and Tri-state buffer. The output

capacitance is the sum of the node capacitance of the buffer inverter in the receiver circuit and the input gate capacitance of the D-latch, which is in order of aF (10^{-15}F), which is ignorable to the transient response.

3.2.3.5 Power and Temperature Analysis

Power analysis is also simulated. The input pattern is the same as that in transient response analysis. Results show a minimum of $375\mu\text{W}$ and a maximum of $415\mu\text{W}$ during operation. The power dissipation comes from the static current generated by the feedback and gain stages in the receiver design. The circuit performance is simulated under environment temperature of 27°C , 57°C , and 97°C . No variation is observed both on DC and transient response. Therefore, it is safe to say the circuit is immune to temperature changes in the reasonable working range.

3.2.4 Scaling down the design

3.2.4.1 Performance difference

In order to achieve better transient response, we shrink our previous design in $1.5\mu\text{m}$ to $0.35\mu\text{m}$. Different simulations are performed to observe the effect of process variation on the performance of the receiver circuit. The W/L ratios of all transistors are kept the same and different model file is used according to each process. Table 3.1 shows the results.

Process	l (mm)	Threshold Current (nA)	Speed(MHz) ($f=1/T_{PLH}+T_{PHL}$)
AMI 1.5	0.8	40	0.24
AMI 0.8	0.5	85	1.07
AMI 0.5	0.25	150	10
TSMC 0.35	0.2	155	33.3

Table 3.1 Process variations on the photoreceiver circuit performance

Although the device current density doesn't change significantly from one foundry to another, the scaled-down devices require less gate drive ($V_g - V_t$). Therefore, device transconductance and reference current change slightly at constant-current density with scaling, while device capacitance decreases. This is the reason for the performance difference between different processes. As we can read from the table, as circuit shrinks, the sensitivity is decreased (threshold current increases), while the response speed will be increased. Hence in smaller feature size design, transistor sizes should be redesigned to compensate for the reduced threshold current.

3.2.4.2 Redesign of the receiver circuit

We change the size of M2 and M4 in order to compensate for the slightly changed bias condition introduced by 0.35 μ m technology. The L/W ratio of M2 is changed from 3 in 1.5 μ m technology to 6 in 0.35 μ m, while the W/L ratio of M4 is modified from 2 to 1.8.

The corresponding current source value is $103\mu\text{A}$. DC simulation shows the photoreceiver toggles at a threshold current of 45nA , almost the same in $1.5\mu\text{m}$ technology. The layout is shown in Fig 3.13. Total area of the circuit is $924\mu\text{m}^2$.

Fig 3.13 0.35 μm Photoreceiver Circuit Layout

*Fig 3.14 0.35 μm Photoreceiver Threshold power simulation
Note x-axis units μV maps to μW in a read device*

In Fig 3.14, we vary the responsivity of the detector from 0.02A/W to 0.04A/W just as we did in the case of 1.5 μ m technology. The threshold power is 1.8 μ W at the lowest responsivity value (0.02A/W), which is still in the range of our requirement (2-4 μ W).

Fig 3.15 0.35 μ m Photoreceiver AC response simulation

The same method is used in 0.35 μ m receiver AC analysis. As shown in Fig 3.15, the input capacitance varies from 200fF to 1000fF, and the 3-db bandwidth is 40MHz for the worst case (1pF). The results demonstrate that the photoreceiver AC performance is not limited by input capacitance in our desired working range.

As shown in Fig 3.16, the transient analysis is performed again. The input light power source switches between 0 μ W and 1 μ W at a frequency of 1MHz. Detector responsivity is set to 0.04A/W. Rise and fall time are both 1ns. The T_{PLH} and T_{PHL} measured are 0.15 μ s

and $0.01\mu\text{s}$ respectively, referring to a maximum response of 6.25MHz . Much faster speed is also observed of 14.3MHz and 25MHz at responsivity of 0.06A/W and 0.08A/W . This fact implies that the circuit speed can be well increased if a higher responsivity detector structure is utilized. However, the receiver circuit speed will finally be limited by control unit design which will be discussed later in section 3.6.2. The speed is adjusted to 2MHz eventually to be consistent with the 33-clock cycle provided by control unit in system array design. The static current from the receiver circuit is measured to be $120\mu\text{A}$. Power analysis shows a corresponding power consumption of $360\mu\text{W}$.

Fig 3.16 0.35 μm Photoreceiver Transient response simulation at $R=0.04\text{A/W}$

3.3 System Overview

The entire photoreceiver array design will first be described before we introduce the design of the control unit and individual pixel. For our initial objective, a 32×32 photoreceiver array will be realized to read the page-mode data from POMs. As a brief summarization of previous topics, the photoreceiver is implemented by $0.35\mu\text{m}$ technology to meet the minimum speed requirement for the receiver array while the system data-bus speed is targeting at 100MHz. Hence all circuits, from now on, are designed for $0.35\mu\text{m}$ technology, and the feature size we used in the technical file is $0.2\mu\text{m}$. One important function of the array is to bridge the gap between page-mode optical data and word-oriented bus structure. Further, due to the long addressing time of optical pages, i.e. order of μs , a pipeline scheme should also be introduced to enhance the system throughput. In other words, the array is required to process the current page of data and read the next page of data simultaneously.

Fig 3.17 Block Diagram of the system design

As shown in Fig 3.17, an array of 32 by 32 pixels is laid out to form the photoreceiver array. As illustrated later, an $ENAi_j$ ($i=0-31, j=0-31$) and a CLK_{ij} ($i=0-31, j=0-31$) are two ports for each pixel, which are the tri-state buffer enable signal and D latch clock signal, respectively. All pixel's CLK_{ij} ports are tied together as one node CLK_Pixel . And all $ENAi_j$ ports of the pixels in one row in the pixel array are joined together as $ENAi$ ($i=0-31$). The 33-bit shifter register (SR) acts like the control logic. There are two input signals for the SR: "CLK" to be fed in as the system clock, as well as the data bus clock, and "Reset" to initiate or reset the system operation. 32-bit output signals from the SR, C1 to C32, are connected with the $ENAi$ ($i=0-31$) of each row. The 33rd bit output of the register C0 is connected with CLK_Pixel to generate the clock signal for all pixels in the array. The output of each pixel in one column is connected together to the data bus. After system resetting, the SR will relay the selection signal ("1") from C0 to C32. At the first clock cycle, C0 is effective, and all pixels are clocked and the optical data from the POM is latched into each pixel. Then during the following 32 clock cycles, each row's $ENAi$ signal will take effect and transfer the valid word-oriented data to the system bus. At the same time, the system reads in the next page of data. The SR will repeat the signal sequence thereafter to transfer the next page of data. The disadvantage of this pipeline structure is the waste of one clock cycle to store the page-mode data. However, as page size and clock speed increase, this effect becomes less significance. In addition, the SR receives out-chip "Halt" signal to suspend the operation. Another "Stop" signal will also be provided for CPU to bypass the reading during the "C0" effective cycle, which is the data storage period. Detailed design will be presented in the following section.

3.4 Control Unit

The shift register is implemented by a string of 33 cascading flip-flops (FF). Shown in Fig 3.18, the output of the last FF in the string is connected to the input of the first FF to give a closed loop structure. The first FF in the string is different from others, which is pre-set to “1” instead of being pre-reset to “0” as in others. This will guarantee the effective signal (“1”) passing through the flip-flop string from the first clock cycle after system resets. A buffer stage is followed by the last flip-flop to drive the long metal line connecting the output of the 33rd FF with the input of the 1st FF. Control signals C0 to C31 are taken from the output of 2nd to 33rd FF. C32 is generated by “anding” the first FF’s output with “reset” signal. In this way, the pre-set “1” will be cancelled by “reset” signal (“0” effective) before system operation starts. Some delay mechanism is introduced before “reset” signal feeds into the AND gate to eliminate the glitches of C32 after system starts. The delay is simply realized by means of long gate length buffer inverters. In order to yield the “Stop” signal, Boolean equation is derived from K-map in Table 3.2. The function then is implemented by 3-input AND gate. Delay stage is again added for the purpose of glitch elimination. The external system clock signal “CLK” will first pass through a tri-state buffer before it is fed into synchronized FF string. When control signal “Halt” is effective (“0”), the buffer will impede the clock signal to go through, therefore suspend the system operation. The operation will resume after “Halt” is cancelled. Standard cells are used in the layout implementation. Specifications and circuit diagram of the logic gates are listed in Appendix 1.

Fig 3.18 Block Diagram of Control Unit

C0,Halt Reset	00	01	11	10
0	0	0	0	0
1	0	1	0	0

Table 3.2 Derivation of “Stop” signal. “Stop”= “Reset”·”Halt”·” $\overline{C0}$ ”

Fig 3.19 is the IRSIM simulation result of normal control unit operation. The circuit is implemented in 0.35 μ m technology, and the clock period is 10ns, i.e. 100MHz. The same “reset” and “CLK” signals are used in SPICE simulation as shown in Fig 3.20(a). Because of the complexity of the circuit, the rise and fall time of the system clock signal should be set to 0.1ns to get the correct simulation results from SPICE. Fig 3.20(b) is the response without considering the loading effect to the output of the control unit. However, since C0-C32 will be connected to long metal lines in the array, especially for C0, whose output load will be all “CLK” inputs from the pixels in the array, rough estimation to those load values are made and fed back to the control circuit simulation. Table 3.3 lists the critical timing parameters. From this table, we can tell that for C1 to C32, the loading effect (300fF) on signal delay is not significant. However, for C0 of a capacitive load up to 5pF, the output signal will be distorted as shown in Fig 3.21. Appropriate buffer stages should be introduced to alleviate loading effect on C0. Experiment shows that two standard 4X buffers are needed for enhancing signal C0’s responsive speed. The whole control unit area is 6397 $\lambda \times 109\lambda$. Average power consumption measured during operation is 74mW.

Fig 3.19 IRSIM simulation of the control unit operation.

Fig 3.20(a) Reset and CLK signal for control unit. $T=10\text{ns}$, $t_{\text{rise}}=t_{\text{fall}}=0.1\text{ns}$

Fig 3.20(b) “Stop”, “C0”, “C1”, “C2”, “C3” response without “Halt”. No capacitive loads are considered.

Load Capacitance (fF)	Rise Time (ns)	Fall Time (ns)	T _{PLH} (ns)	T _{PHL} (ns)	Duty Cycle “1” %
0	0.6	0.44	0.61	0.53	94.5
300	1.52	0.87	0.98	0.76	81.4
5000 (Buffered)	4.58	2.26	1.96	1.56	53.8

Table 3.3 Timing parameters from loading effects

Fig 3.21 C0 response without buffer (middle) and with buffer (bottom)

3.5 Individual Pixel

3.5.1 Block Diagram

The individual pixel serves as the basic element in the entire read-head system, which will be replicated to form the array structure. Its main functions are to convert the optical data from POM, save the data into the array, reconstruct the page format data into word-oriented ones, and queue them to be sent to the external data bus. Since a huge amount of

pixels (1024) will be presented in the array, the total power consumption is a critical concern. To minimize the power dissipation in transistor and layout level becomes the primary objective in the pixel and array design.

As described in Fig 3.22, the pixel contains photodetector, and photoreceiver circuit, which have been discussed in previous sections. In addition, it also has a D-latch and a tri-state buffer. The D-latch performs like a memory unit, which will latch the converted data. All “CLK” signal in the D-latches in the array will be tied together and receive the effective high signal from the control unit. Therefore the whole page of data will be stored at the same clock cycle and waits to be transferred to external bus at the following clock cycles by tri-state buffers. The “ENA” port of the tri-state buffer accepts effective high signal also from the control unit. The whole pixels in one row in the array will then be selected at one clock cycle and the word-oriented data will be sent to external data bus. “Reset” function is also needed for latches and tri-state buffers to clear the bus and array data storage before operation starts.

Fig 3.22 Block Diagram of the individual pixel design

3.5.2 Transistor and layout level design

Static CMOS logic is used in the digital part of the pixel design for its low power consumption and stable performance. In the layout design, the sizes of all transistors, except the one at tri-state buffer output stage, are minimized to reduce the dynamic current during switching. The output transistors in the tri-state buffer are sized relatively large to increase the charge/discharge time of the large capacitive load from the long wires of the data bus. The “Reset” function is implemented by ANDing the “Reset” signal with the output signal in D-latch and tri-state buffer. Although delay will be introduced into these additional stages, simulation results show they are in the tolerable range according to our design specification and won’t affect the overall performance.

Fig 3.23 (a) and (b) illustrate the details of the gate level design of the D-latch and tri-state buffer. Fig 3.24 shows the layout design of the digital part in the pixel. The whole area is measured as $107\lambda \times 139\lambda$. It is integrated with previous detector and receiver circuit layout to form the individual pixel in shape of square.

Fig 3.23 (a), (b) Gate level design of D latch and Tri-state buffer

*Fig 3.24 Layout of the digital part in the pixel.
Transistors in circle area are output buffers*

3.5.3 Simulation result

Rough estimation of the load capacitive value at the output of the pixel “O”, as well as the input capacitances of “ENA” and “CLK” signal lines of the 32×32 array, should be made before we simulate the function of the digital section on the pixel. By layout parameter extraction in 0.35μm implementation, the wire capacitances of “O”, “ENA” and “CLK” signals in the array are 127.1fF, 112.9fF and 117.5fF respectively. Taken into account the input gate capacitance in each pixel and vertical line’s capacitance connecting with control unit output, the final output capacitance values of the “O” and “ENA” are estimated to be 300fF. The value of “CLK” will be much larger, i.e. 5pF, because all “CLK” ports in the array are connected together. The values of “CLK” and “ENA” are fed into the control unit circuit netlist to calculate the rise and fall time of these signals as shown in Table 3.3. Then the timing parameters are added arbitrarily

along with the output capacitance value at “O” in the SPICE file to simulate the operation of the digital part. Table 3.4 shows the timing parameters used in the digital simulation.

Signal	Load Capacitance (fF)	Rise Time (ns)	Fall Time (ns)	Pulse Width (ns)
“CLK” (with buffer stage)	5000	4.58	2.26	5.38
“ENA” (Loading to 300fF)	300	1.52	0.87	8.14
“O” (Loading to 300fF)	300	2.61	1.71	N/A

Table 3.4 Timing parameters in digital section simulation

Fig 3.25 shows the correct response of the output “O” on the pixel at a bus capacitive load of 300fF. The rise and fall time are well within the pulse width of the “ENA” signal. So no data conflict will happen between adjacent “ENA” signals, which means the output buffer transistors are sufficient enough to switch signals during operation.

Fig 3.25 Simulation results of the digital part in pixel design. The pixel is loaded to a capacitive value of 300fF. Input data value is set arbitrarily at the input of D-latch. Rise and fall time of the response are 2.61ns and 1.71ns respectively.

3.5.4 Pixel layout design and simulation

In the entire pixel simulation, a 4MHz pulse light power source is fed into the photoreceiver circuit. Fig 3.26(a) shows the circuit response at detector's responsivity $R=0.04A/W$ and threshold power $1\mu W$. Fig 3.26(b) illustrates the following digital circuit response to the transition of converted optical data from “0” to “1”. From this picture we can tell, that the transition time of the signal fed into digital section is comparable to the pulse width of “ENA” signal generated by control unit. In addition, all

Fig 3.26(a) Photoreceiver response to 4MHz input light source @ $W_{thre}=1\mu W$, $R=0.04A/W$

Fig 3.26(b) Expanded view of the pixel response towards the optical data transition. Signals sequence (from above to bottom): CLK, ENA, output from receiver, “O” data signal on the bus. Load to “O” is 300fF.

optical data are saved at the first clock cycle of the control unit output, at which the transition has been over. Therefore, the data integrity and accuracy are guaranteed. Noticing that the photoreceiver operation speed is a little bit faster than the required minimum frequency, i.e. 4MHz, the transition of the optical data will actually appear earlier than the last word “ENA” signal in the previous page, which makes sure that next page of data are recorded correctly into the array.

Component	Height (l)	Width(l)	Area(l²)
Receiver	107	216	23112
Digital	107	139	14873
Detector	100	80	8000
Active Area (P ⁺)	72	41	2952
Pixel (without power rails)	204	209	42636
Pixel (with power rails)	324	328	106272

Table 3.5 Specification about the pixel design

Table 3.5 lists the physical layout dimensions for all components of the individual pixel design. The entire layout of an individual pixel is shown in Fig 3.27. Simulation result reveals an average current of 400 μ A during operation. Approximately 280 μ A of the total current comes from the digital section, with the rest of the static current from analog receiver circuit. Since the feature size of 0.35 μ m technology is relatively small, i.e. $\lambda=0.2\mu\text{m}$, the power rails (VDD, GND) have to be sized wide enough to handle the current of all pixels in one row/column according to our array structure.

Fig 3.27 Pixel Layout with power rails

The width of the rails is determined by the electron migration limit of the CMOS process, i.e. $1\text{mA}/\mu\text{m}$ for the metal wires to handle the current flowing through it. Hence, a width of 80λ ($16\mu\text{m}$) is selected to carry the current sum up to 32 pixels at a maximum current limit of $500\mu\text{A}/\text{pixel}$. In order to prevent the substrate noise from the digital circuit, guard rings is surrounded by the photodetector and receiver circuit to isolate them from current injection by adjacent large swing digital circuits.

From Table 3.5, the individual pixel area implemented by 0.35 μm technology is approximately 4250 μm^2 . The average power consumption of the pixel is 400 $\mu\text{A} \times 3.3\text{V} = 1.32\text{mW}$. According to Semiconductor Industry Association roadmap [18], the maximum constraints of area and power consumption are 4 cm^2 and 70W for 0.35 μm technology. Therefore, the page size limits of our photoreceiver array in terms of area and power consideration are 9.4×10^4 and 5.3×10^4 respectively. Although the array can be made larger, it will ultimately be limited by the optical power budget as analyzed in section 2.5.

3.6 Photoreceiver Array and entire system design

3.6.1 Layout Issues

Based upon the individual pixel design, the 32 $\times$ 32 photoreceiver array is laid out in 2-D format. Each row of the array will serve as the word format reader as described in section 3.3, while all pixels' outputs in one column are connected together to external data bus. During operation, the receiver array receives input light signals and outputs converted data word by word at each clock cycle. The system clock signal out-of-chip feeds into the control unit and generates "ENA" signal for reading each word in the array at one clock cycle. In our 0.35 μm implementation, the clock speed is 100MHz.

Fig 3.28 Partial overview of the pixels in the array

The partial layout detail about the array is shown in Fig 3.28. A couple of issues need to be mentioned during the array layout design. First, the huge power consumption of the array requires a strong current handling capability of the power rails. Nearly 70% of the total current comes from the digital logic in the pixel, with the rest taken by analog circuit. In order to distribute current flow evenly in the array, analog VDD and digital VDD are separated from each other, and the analog VDD and digital VDD between 2 adjacent columns are connected together. In this way, the current flowing through the

vertical VDD rails will be the combination of two adjacent columns instead of one, and the switching probability and turn on frequency of the pixel can be reduced among a larger pixel group. In addition, the GND rails of all pixels in one row are common. The vertical-VDD horizontal-GND structure will further alleviate current burden on rails further by serving a larger number of pixels (1 row + 1 column). Second, the data output signal of each pixel runs vertically through the pixel area. In this way, the length of output data lines will be decreased significantly, which reduces the loading effect on pixel's output buffer. What's more, the entire array area will be decreased as much of 50% as that if we route the data-bus line around the pixel. However, since the energetic data line will run over the highly sensitive, low voltage swing analog receiver circuit, noise caused by the frequently switching data lines should be avoided. As shown in the figure, Metal 3 is used as data line while grounded Metal 2 is inserted between it and the underlying analog signal line M1. Therefore, the analog circuit will be isolated by digital signal to be immune from disturbance. Finally, "reset", "CLK", and "ENAi" ($i=0-31$) signal lines run above each pixel row to be connected to corresponding input nodes from control unit.

3.6.2 Simulation

Fig 3.29 (a) and (b) shows the IRSIM simulation results of the array performance. Since we can not designate current signal in IRSIM command file, the simulation is just the operation of the digital part of the array. We assign data value arbitrarily to receiver output node (out) on each pixel. In this way we assume that the converted optical data is already available and finishes transition before next working cycle begins. Reliable

operation is observed under 100 MHz clock frequency. 3.29 (a) is the operation with “Halt”=1. The input data pattern set to each column in the array is 517A5C97 (01010001011110100101110010010111) which is randomly generated and won’t change during the whole operation. Therefore, the output of each bus will recycle the same word. This is the exact test method discussed in chapter 4, because we can not provide dynamic optical page changes. During the cycle of storing the next page of data, the bus output will keep the previous data value, while the “Stop” signal is generated to inform CPU not to read the unwanted data. 3.29 (b) shows the operation with “Halt” effective (“0”). When system is in “Halt” mode, the bus output keeps unchanged until “Halt” signal is removed. Five probe data buses: B0, B1, B15, B30, B31 are observed. Simulation results prove the correct layout routing and connection.

Fig 3.29 (a) IRSIM simulation of the array, with “Halt”=1. Circled area is transition period between two consecutive pages

Fig 3.29 (b) IRSIM simulation of the array, with “Halt”=0. Squared area is the operation when system “Halts”

It is impossible to simulate such a huge system by SPICE. From the results in section 3.5.4, the performance of individual pixel has been verified. In Fig 3.30, we combine the control unit with one column of pixel to simulate the system operation. Simulation results are less accurate since we change SPICE tolerable error parameters to force the program to converge. However, desired performance can still be observed for the reading of two adjacent pixels as depicted in Fig 3.30.

Fig 3.30(a) two adjacent pixel photoreceiver response to a 2MHz light power source @ $R=0.04A/W$ and $P_{threshold}=1\mu W$, and (b) Bus output of the system. Signals are: C0, C1, C2, Bus0 and CLK. Area within black lines is the same time range in two plots.

From Fig 3.30 (b) we can see, that the bus output changes from “0” to “1” during the first operation cycle, which is the reading of “0” and “1” in pixel 1 and pixel 2 in the first page case. For the next cycle, its value changes again from “1” to “0”, which is the reading of “1” and “0” in pixel 1 and pixel 2 in the next page case. In this simulation, control unit is only integrated with one column of pixels in the array. Larger circuit simulation is beyond SPICE capability. Another thing that needs to be mentioned is the modification of photoreceiver speed. In section 3.2.4.2 we’ve seen the speed is 6.25MHz at $R=0.04A/W$. However, if receiver works under this speed, the stable data period, i.e. $1/6.25MHz=0.16\mu s$, is shorter than the 33 clock cycle provided by control unit, which is $1/(100MHz/33)=0.33\mu s$. This apparently will ruin the normal reading sequence of the array. So the receiver speed needs to be decreased to be within the array working cycle. Taken into account the loading effect by final layout design, the speed is adjusted to 2MHz as shown in Fig 3.30(a).

3.6.3 Entire system layout

Fig 3.31 is the entire system layout. The main area is $9408\lambda \times 9808\lambda$, i.e. $3.7mm^2$. Due to the undecided fabrication process, the pad-frame has not been incorporated into the main chip design. The power rails are not connected together because of the huge power consumption from the photoreceiver array. It is suggested that several power pads are needed in the pad-frame design to accommodate the rail to rail current flow. From above discussion, we see a total current value of $400\mu A \times 32 \times 32 = 0.4A$ from the array and 22.4mA from the control unit, i.e. 0.422A. In a SCN4M_SUBM.20 process, for example, the wide power pad has metal wire of 334λ wide, i.e. $67\mu m$. Considering

electronmigration of $1\text{mA}/\mu\text{m}$ is safe for the metal wires, the number of power VDD pads needed is 7 ($422/67=6.29$).

Fig 3.31 Entire 32×32 system layout

3.7 System implementation in $1.5\mu\text{m}$ technology

Because the available free fabrication run to us is AMI $1.5\mu\text{m}$ CMOS technology, we implement the read-head device in such a manner to test the functionality of our design. However, a few changes appear when we migrate our design from $0.35\mu\text{m}$ to $1.5\mu\text{m}$ technology, as illustrated in previous sections. First, and the most important, the photoreceiver speed will decrease below our requirement. However, due to test equipment incapability, we can not provide dynamic optical page input in our simulation,

ex. 2MHz. Therefore, the 1.5 μ m photoreceiver array is still good for a static system test. Second, the 100MHz clock speed in 1.5 μ m circuit can not be guaranteed. Therefore, the test on the implemented chip is just a function test on array operation. Exact feature test is expected only when we implement the circuit in its original 0.35 μ m design scheme. The design methodology strictly follows the ones in previous sections. Comparisons are made and listed in Table 3.6. The maximum area provided by MOSIS free fabrication run is 2.2mm $\times$ 2.2mm. According to our design specification, the final array size is 8 $\times$ 8. Control unit is also modified accordingly to 9-bit shift register in the new design. The 40-pin MOSIS digital pad-frame is used, and the entire chip layout is shown in Fig 3.32.

Fig 3.32 8 $\times$ 8 array implemented by 1.5 μ m technology

Fig 3.33(a) IRSIM system simulation with padframe. “Halt”=1.

Fig 3.33(b) 8×8 array implemented by 1.5μm technology, “Halt”=0.

In order to enhance the chip’s testability, different parts of the array are laid out separately, such as photodetector, receiver circuit, control unit, individual pixel. Direct pin observation is not welcomed here for avoiding the loading effect introduced by I/O pads on the sensitive circuit elements. Therefore, for the chip space taken by test structure, the final array size is made to 4×8. The final test chip layout is illustrated in Fig 3.34. And IRSIM simulation results are in Fig 3.33(a), (b). The chip operation speed

is estimated to be less than 20MHz. The long start time for bus output data, which is the unstable state in Fig 3.33, maybe due to the loading effects of I/O pads associated with the circuit. The final test chip layout is shown in Fig 3.34. Test results and performance evaluation on the chip are discussed in the Chapter 4.

	32×32 Array in 0.35mm	8×8 Array in 1.5mm
Pixel Output Load	300fF	600fF
Pixel Area	4250 μm^2	41600 μm^2
Detector Window Size	118 μm^2	944 μm^2
Pixel Average Power Consumption	1.32mW	7.25mW
Control Unit “ENA” load	300fF	600fF
Control Unit “CLK” load	5pF	2pF
Buffered rise&fall time for “ENA”	1.52ns+0.87ns	1.96ns+1.09ns
Buffered rise&fall time for “CLK”	4.58ns+2.26ns	4.53ns+2.33ns
Control Unit Average Power Consumption	74mW	45mW
Minimum Power rails size needed for one column/row	16 μm (80 λ)	16 μm (20 λ)
Maximum clock speed evaluated by IRSIM simulation	150 MHz	20 MHz

Table 3.6 Specification comparisons between 2 designed chips

Fig 3.34 Test Chip Layout. Circled pads are analog ones for photodetector and receiver testing

Chapter 4

System Test and Performance Evaluation

In this chapter, individual components and system tests are reported. The test chip layout shown in Figure 3.34, was implemented using AMI ABN 1.5 μ m process. The discrepancies between simulation and test results are presented and possible reasons creating the difference are analyzed. The whole system performance is verified and evaluated in terms of power consumption, system throughput, etc. Since this is just a function test on our design, detailed feature test of the read-head device is expected when the chip is implemented in 0.35 μ m process.

4.1 Experiment plan and test bench setup

The test of the chip is divided by five phases: First, the I/O test for the pad-frame, which is realized by pin to pin test through built-in inverters. Second, the electrical test on receivers. Third, the digital test on pixel logic and control unit. Fourth, the optical test on photodetectors and entire photoreceiver circuit. Finally, the array test to validate the system performance. The test is embarked in sequence as described above in order to optimize the efficiency of the whole test procedure.

The test setup for electrical parts is relatively easy, giving certain inputs by different sources and observe output results by instruments such as multimeter and logic analyzer. However, the test-bench for optical test is much more complicated due to the requirement on the input light power onto a certain area on the chip. As illustrated in Fig 4.1, the

configuration for the optical test consists of four parts: The controllable laser diode (LD) which gives the adjustable light power source in near infrared range ($\lambda=853\text{nm}$), the fiber (FB) which transmits light signal onto the chip, the device under test (DUT) which is the chip attached to a three-axial motion controller to adjust the appropriate position of photodetector on the chip for the incoming light from the fiber, and the multimeter (MM) which reads output signal, ex. photo-generated current, from the detector. There is also an optical power meter (OPM) positioned at different locations, measuring power values for the calculation of responsivity of the photodetectors and threshold power for the photoreceivers. The LD, OPM and MM are coordinated by LABVIEW programs through GPIB bus, which can facilitate the control and data collection.

As shown in Fig 4.1, a cubicle splitter (CS) is used to attenuate the light from the LD source. Power values at different locations, as shown in the figure, are observed and plotted. The result is illustrated in Fig 4.2. From this picture we can see, the power values are pretty linear to the driven laser current, which is ideal for the sweep test on photoreceiver threshold power when we sweep the light power through the threshold range.

Fig 4.1 Optical Test-bench Setup [28]

Fig 4.2 Optical Power Distribution of the testbench

The power at location 4 is the input power to the photodetector. Therefore we can refer to P4 curve in Fig 4.1 during the optical test to determine the illumination power to the chip, without disturbing the alignment of the fiber-chip system. Since our receiver circuit is designed for high sensitivity, low power range, i.e. less than $1\mu\text{W}$, is to our interest. The linearity in this range is not as ideal as that in high power range. Therefore, an optical attenuator is used to transfer high optical power range to the desired range. What's more, intentionally misalignment of the fiber-coupler is also introduced to attenuate the power further. Coupling efficiency is also calculated by the ratio of P4 to P2. The average coupling efficiency at high power level (50mA-200mA) is 37%. The fiber used in the test-bench is multimode fiber with core diameter of $100\mu\text{m}$.

4.2 Photodetector Testing

The photodetector in our design is P-diffusion to N-well CMOS compatible, which is in shape of rectangular. Since the light spot coming from the fiber core is round, a fill factor of the power transmitted onto the photodetector should be taken into consideration. The active area for the CMOS photodetector is $30\mu\text{m}\times 30\mu\text{m}$, while the core diameter of the multimode fiber is $100\mu\text{m}$. Therefore, at an optimized position where light spot covers the whole area of the active region of the detector, assuming an even power distribution from the light spot, the power transmission coefficient (fill factor) should be around 36%. After exact alignment of the fiber to the detector, LD is swept from 0mA to 200mA. Power at each measuring point is determined by multiplying the corresponding value in P4 power curve in Fig 4.2 with the fill factor. Photodetectors at different chips are

measured respectively and average photon generated current values are recorded. The photodetector response curve is plotted in Fig 4.3.

From this figure we can tell a pretty linear response of this kind of CMOS photodetector. The average responsivity at 853nm illumination light is calculated as 0.0411A/W. With a fill factor of 36%, the actually responsivity can be reached to 0.114A/W. This value is well above our expected value, i.e. 0.02-0.04A/W. However, it is below the 0.3A/W value for silicon photodetector operating at near infrared range. Higher responsivity is also estimated in shorter visible wavelength range (400nm-600nm). From the result we can conclude that responsivity of 0.04A/W is reasonable and achievable when the detector design is downsized to 0.35 μ m technology.

Fig 4.3 Photodetector Responsivity Characteristic

4.3 Photoreceiver Circuit Testing

The receiver test is comprised by two steps. First, a constant current source was fed into the test pin for the photoreceiver circuit on-chip without photodetector attached. The current source behaves like the photo-generated current. The receiver toggles from 0V to 5V at around 80nA. Then the entire receiver circuit (with photodetector) is aligned to receive light input from the fiber. The output characteristics are shown below in scale of light power. Fill factor is also taken into account when plotting.

Fig 4.4 Photoreceiver Output Characteristic

From Fig 4.4 we can tell a threshold power of 770nW is achieved for the photoreceiver. Related to the photodetector responsivity of 0.114A/W we measured, the threshold current is 88nA, which is in well accordance with 80nA value in the first step.

Fig 4.5 Simulation of photoreceiver circuit threshold power

The process model in Appendix 2 is fed back to threshold power simulation of the receiver circuit, and result is shown in Fig 4.5. Compared to test result, the threshold power is 500nW, 35% less than the test value. The difference may due to the inaccuracy of power estimation during test phase. However, it is close enough to say that the photoreceiver circuit threshold power is well under 1 μ W level. As concluded in chapter 3, the responsivity of detector implemented in 0.35 μ m technology is expected to be higher than its 1.5 μ m counterpart. Therefore, it is safe now to say that the sensitivity of photoreceiver circuit in our design meets the need for reading POMs.

Transient test on receiver circuit is not applicable because of the insufficient test equipment in our lab. A dynamic light power source is needed in the future to test the photoreceiver responsive speed.

4.4 Digital Part Testing

The test on the digital part includes individual pixel test and control unit test.

As described in chapter 3, the digital part in the pixel design consists of the D latch and tri-state buffer. The cells are fully custom designed to fit into individual pixel area. The test is pretty straightforward: give digital inputs (0V or 5V) and measure the output voltage values. Table 4.1 lists the test results that are consistent with expectations. From the table we can see, when “ENA” signal is high, the output will transfer the data stored in D latch; when ‘ENA’ is low, the output will be set to 0.

Reset	ENA	CLK	IN	OUT
0	X	X	X	0
1	1	1	0	0
1	1	1	1	1
1	1	0	0/1	0/1
1	0	X	X	0

Table 4.1 Digital Outputs of the pixel test

The control unit is tested by Agilent Logic Analyzer. The sample rate is 4ns. Due to the availability of pins, we only observe three outputs of the control unit: C0, C4 and C8. Fig 4.6 shows the normal operation. We can see exactly 9-clock working cycle and alternative effective signal’s relay between all outputs during the working cycle. Fig 4.7

demonstrates the operation when “Halt” signal is effective, i.e. “0”, which stops the control outputs. These results are obtained at a clock frequency of 2MHz, at which the waveform can be observed by oscilloscope.

Fig 4.6 Control Unit test with “Halt”=1

Fig 4.7 Control Unit test with “Halt”=0

4.5 Array (System) Test

This test is designed to validate the operation of 4×8 photoreceiver array. Some input pattern should be generated and aligned accurately onto the array area. The test system to realize our requirement is shown in Fig 4.8. In that figure, a slide with black and transparent dots is used to give a certain input pattern. It is placed in front of a headlight. The output power of the light is large enough to turn on all the photoreceiver circuits in the array. A beam narrower comprised by 2 convex lenses is fixed in the middle of the transparency and the array (chip), so that the image on the slide will be projected onto the array area. Since the pixel size on chip is approximately $200\mu\text{m} \times 200\mu\text{m}$, and the individual shadow element area on slide is $2\text{mm} \times 2\text{mm}$, the ratio of $f1/f2$ is adjusted around 10 in order to give a precise projection. Carefully alignment is made to transfer the input pattern onto the chip as accurate as possible. During the operation, “Reset” signal (“0”) is first applied to clear the entire photoreceiver array. Bus (B4-B7) will start to output data after “Reset” is cancelled.

Fig 4.8 Array operation test setup

Due to the inaccuracy of the pattern source projection, the outcome of the array shows error bits during application, especially when the masking bits are distributed randomly. This may due to the imperfect alignment of the system. Since our receiver circuit is extremely sensitive, cross-talk issue between adjacent pixels is another possible expectation. The array responses to different input patterns are shown below. From Fig4.9-4.14 we can see the bus output is repeated every 9 clock cycles. This is because the input pattern doesn't change during working cycles. It is impossible for us to change the patterns at rate of 9 clock cycles for the lack of test equipments. Static-page power consumption under each pattern is also measured as shown in the caption of each picture. From those values we can see greater power dissipation at complex input patterns (pattern 5 and 6). This may caused by high switching activities at those patterns. Fig 4.15 is the operation when "Halt" signal is applied. Array works reliably at clock speed up to 2MHz. This value is derived at the condition of long cables connecting the chip under test with the testing meters. Hence large capacitive and inductive values are presented to affect the timing response. Faster operation speed is expected in actual chip operation.

*Fig 4.10 Array operation at input pattern 2
All transparent bits “1” for B4-B7
P=65mW*

*Fig 4.11 Array operation at input pattern 3
Transparent bits for B4&B5= “1”, dark bits for B6&B7= ”0”
P=45mW*

Fig 4.12 Array operation at input pattern 4
Cluster dark bits for B6&B7
B4=11111111 B5=11111111
B6=11110000 B7=11110000
P=50mW

Fig 4.13 Array operation at input pattern 5
Cluster dark bits distributed orderly
B4=11110000 B5=01111000
B6=00111100 B7=00011110
P=200mW
Error bits are circled in the plot

Fig 4.14 Array operation at input pattern 6

Random dark bits

B4=11011110 B5=11011011

B6=10101111 B7=01101101

P=215mW

Error bits are circled in the plot

Fig 4.15 Array operation at input pattern 5 when “Halt”=1 is applied.

4.6 System Evaluation

Based upon test and simulation results, evaluations are made for our designed 32×32 bit read-head device implemented by 0.35μm technology.

According to previous test results, optical power to toggle the receiver circuit in 1.5μm implementation is 770nW. The responsivity of P-diff to N-well detector measured is 0.114A/W. According to simulation results in Chapter 3, approximately the same threshold power is expected at responsivity of 0.04A/W when shrinking the feature size to 0.35μm. For the final system design in section 3.6.2, the receiver operates at 2MHz at threshold power of 1μW and detector responsivity of 0.04A/W. The corresponding addressing time for POM system $\tau=0.5\mu s$. As described in Chapter 2, the Switching Energy for the receiver circuit $E_s=R \times P_{thres} \times \tau=0.04A/W \times 1\mu W \times 0.5\mu s=20fJ$. This value is within the range (30-50fJ) limiting the read-head page size to 10^3 . Considering the effective 32 out of 33 data output cycles, the throughput of the read-head is $2MHz \times 1024b \times 32/33=1.93Gbps$. If faster bus speed is realized, the throughput can be enhanced to 6.06Gbps at our maximum photoreceiver speed of 6.25MHz. Given sufficient optical power, higher throughput can be achieved by increasing the number of array blocks. The design is possible by having wide output bus and high performance output driven pads. Referring to chip area and power dissipation constraints on the page size in our design, the system throughput are 91.15Gbps and 51.4Gbps respectively in applications where optical power will not limit the page size. The optical power budget for this 32×32 read-head is 1.24mW at photoreceiver threshold power of 1μW. Reading from Table 3.6, the rough power estimation of the read-head is $1.32mW \times 1024 + 74mW = 1.4W$.

Chapter 5

Conclusions and Discussions

In this chapter, summarizations about what have been achieved are made, along with discussions and future work towards this project.

5.1 Conclusions

This thesis has described the design, simulation, test and performance evaluation of a 32×32 photoreceiver array as the read-head device for page-oriented optical memory. The proposed design is practical and applicable to serve as the front-end of POM related applications. High sensitivity and high throughput are two characteristics of this read-head design. It can be readily integrated with other electronics circuit, such as filter or error correction circuits, to realize high performance optical reading system for future POMs. Based on previous chapters, conclusions on this piece of work are presented as follows:

- Read-head requirements and constraints necessary to optimize the POM advantages of data transfer rate and access time are considered and analyzed. For the typical POM system, Volume Holographic Memory, the low diffraction efficiency will limit our CMOS based photoreceiver array design to a size of 10^3 .
- We designed a photoreceiver model circuit to meet the requirements of our read-head design. In our $0.35\mu\text{m}$ implementation, the receiver threshold power is $1\mu\text{W}$ at maximum speed of 6.25MHz . These specifications are within the 10^3 pixels limitation by optical power. The final array throughput is 1.93Gbps . Higher

values are estimated, i.e. 51.4Gbps, 91.15Gbps, if sufficient optical power is obtained from page-oriented optical memories. The total power consumption is estimated to be above 1W.

- A model chip is implemented by MOSIS 1.5 μ m technology. An array size of 4 $\times$ 8 is tested. Functional test results show that the receiver threshold power is 770nW at detector responsivity of 0.11A/W. Page mode reading is realized at static optical input patterns. Dynamic test should be made to complete the demonstration of array operation.

The comparisons between simulated and tested results are summarized in Table 5.1.

	0.35mm Chip	1.5mm Chip	Test Chip
Array Size	32 $\times$ 32	8 $\times$ 8	4 $\times$ 8
Detector Responsivity	>0.04A/W	0.02-0.04A/W	0.11A/W
Photoreceiver Threshold Power	1.8 μ W(@0.02A/W)	1 μ W(@0.02A/W)	770nW(@0.11A/W)
Photoreceiver Speed	6.25MHz	250KHz	N/A
System Bus Speed	100MHz	20MHz	2MHz
System Throughput	2Gb/s	16Mb/s	N/A

Table 5.1 Comparisons between expected and tested values

5.2 Discussions and Future Work

The throughput of our read-head design will ultimately be constrained by system data-bus speed and width. Given enough optical power, we can increase the array size and data bus width. In a larger array design, the data-bus speed will be augmented facilitated by an advanced process technique, such as $0.18\mu\text{m}$ CMOS process. The control unit should be redesigned to be compatible with the bus speed as well as the array size.

Timing analysis on receiver and detector is desired in the future to prove our simulation results. The $0.35\mu\text{m}$ 32×32 read-head chip is also expected to be processed to give us detailed test results on system performance. The optimization of the current design in circuit or logic level is needed in order to reduce power dissipation of the photoreceiver array.

Finally, we suffer the great inconvenience of simulating the system without the inclusion of optical components. This fact arises from the lack of CAD tools nowadays in the design area of hybrid multi-technology VLSI circuits. Therefore, it is essential to have design tools developed in the future for our design of this Photonic VLSI based read-head device.

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Appendix 1. STANDARD CELLS USED IN CONTROL UNIT DESIGN (LAYOUT & CIRCUIT DIAGRAM)

1. INV100: Normal Inverter

2. INV104: (4X Buffer)

3. NANF211: (2-input AND Gate)

4. INV311: (3-input AND Gate)

5. BUFF121: (Tri-State Buffer)

6. DFRF301: (D Flip-flop with Reset Function)

7. DFBF311: (D Flip-flop with Set Function)

Appendix 2. MOSIS PARAMETRIC TEST RESULTS

RUN: T24P

VENDOR: AMI

TECHNOLOGY: SCN15

FEATURE SIZE: 1.6 microns

TRANSISTOR PARAMETERS	W/L	N-CHAN	P-CHAN	UNITS
MINIMUM	4.0/1.6			
Vth		0.57	-0.99	volts
SHORT	20.0/1.6			
Idss		170	-62	uA/um
Vth		0.54	-0.94	volts
Vpt		10.0	-10.0	volts
WIDE	20.0/1.6			
Ids0		< 2.5	< 2.5	pA/um
LARGE	50/50			
Vth		0.57	-0.90	volts
Vjbkd		16.6	-14.3	volts
Ijlk		<50.0	<50.0	pA
Gamma		0.57	0.48	V^0.5
K' (Uo*Cox/2)		36.4	-12.0	uA/V^2
Low-field Mobility		651.46	214.77	cm^2/V*s

POLY2 TRANSISTORS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	4.8/3.2			
Vth		0.86	-1.16	volts
SHORT	9.6/3.2			
Vth		0.84	-1.12	volts
LARGE	28.8/28.8			
Vth		0.85	-1.09	volts
K' (Uo*Cox/2)		22.8	-7.2	uA/V^2

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	volts

BIPOLAR PARAMETERS	W/L	NPN	UNITS
2X1	2X1		
Beta	120		
V_early		54.5	volts
Vce,sat		0.2	volts
2X2	2X2		
Beta	120		
V_early		54.7	volts
Vce,sat		---	volts
2X4	2X4		
Beta	120		

V_early		54.7	volts
2X8	2X8		
Beta	121		
V_early		54.5	volts
Vce,sat		0.0	volts
BVceo		12.1	volts
BVcbo		28.8	volts
BVebo		7.7	volts

PROCESS PARAMETERS N+ACTV P+ACTV POLY POLY2 PBASE MTL1
MTL2 UNITS

Sheet Resistance	52.9	78.0	23.3	21.4	1960.3	0.05	0.03	ohms/sq
Contact Resistance	54.6	40.4	27.6	14.7		0.05		ohms
Gate Oxide Thickness	309	angstrom						

PROCESS PARAMETERS N_WELL UNITS

Sheet Resistance	1614	ohms/sq
Contact Resistance		ohms

CAPACITANCE PARAMETERS N+ACTV P+ACTV POLY POLY2 M1 M2
N_WELL UNITS

Area (substrate)	272	297	37	24	14	58	aF/um^2
Area (N+active)	1118	724	49	24			aF/um^2
Area (P+active)	1101	715					aF/um^2
Area (poly)	584	44	21				aF/um^2
Area (poly2)	45						aF/um^2
Area (metal1)	35						aF/um^2
Fringe (substrate)	127	177	32	37			aF/um
Fringe (poly)	59	44					aF/um
Fringe (metal1)	56						aF/um
Overlap (N+active)	179						aF/um
Overlap (P+active)	223						aF/um

CIRCUIT PARAMETERS

Vinv	1.0	1.78	volts
Vinv	1.5	2.07	volts
Vol (100 uA)	2.0	0.30	volts
Voh (100 uA)	2.0	4.51	volts
Vinv	2.0	2.27	volts
Gain	2.0	-17.45	
Ring Oscillator Freq.			
DIV64 (31-stg,5.0V)	33.24		MHz

T24P SPICE LEVEL3 PARAMETERS
* DATE: Jun 14/02
* LOT: T24P WAF: 6502

```

* DIE: N_Area_Fring      DEV: N3740/10
* Temp= 27
.MODEL CMOSN NMOS (                      LEVEL = 3
+ TOX  = 3.09E-8      NSUB  = 1E17      GAMMA = 0.6847386
+ PHI  = 0.7          VTO   = 0.5803213  DELTA = 0.751823
+ UO   = 660.0708269  ETA   = 9.997723E-4 THETA = 0.0711395
+ KP   = 7.245549E-5   VMAX  = 1.39058E5   KAPPA = 1
+ RSH  = 0.0469771    NFS   = 5.348556E11  TPG   = 1
+ XJ   = 3E-7         LD    = 0           WD   = 6.226945E-7
+ CGDO  = 1.79E-10    CGSO  = 1.79E-10    CGBO  = 1E-10
+ CJ    = 2.777248E-4  PB    = 0.7351857   MJ    = 0.5
+ CJSW  = 1.521337E-10 MJSW  = 0.05      )
* DATE: Jun 14/02
* LOT: T24P             WAF: 6502
* DIE: P_Area_Fring     DEV: P3740/10
* Temp= 27
.MODEL CMOSP PMOS (                      LEVEL = 3
+ TOX  = 3.09E-8      NSUB  = 1E17      GAMMA = 0.4991546
+ PHI  = 0.7          VTO   = -0.9112926  DELTA = 0.3513965
+ UO   = 106.1137976  ETA   = 2.800317E-3  THETA = 0.1295214
+ KP   = 2.391166E-5   VMAX  = 7.528076E4   KAPPA = 12.027453
+ RSH  = 37.852073    NFS   = 6.381792E11  TPG   = -1
+ XJ   = 2E-7         LD    = 1E-14        WD   = 9.502512E-7
+ CGDO  = 2.23E-10    CGSO  = 2.23E-10    CGBO  = 1E-10
+ CJ    = 2.727731E-4  PB    = 0.5300272   MJ    = 0.3239429
+ CJSW  = 3.721974E-10 MJSW  = 0.05      )
*

```

T24P SPICE BSIM3 VERSION 3.1 PARAMETERS

SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8

* DATE: Jun 14/02

* LOT: T24P WAF: 6502

* Temperature_parameters=Default

```
.MODEL CMOSN NMOS (                                LEVEL = 49
+VERSION = 3.1      TNOM  = 27      TOX   = 3.09E-8
+XJ   = 3E-7      NCH   = 7.5E16    VTH0  = 0.5384269
+K1   = 0.9047341  K2    = -0.0763166 K3   = 6.5210487
+K3B  = -2.3943298 W0    = 9.742914E-7 NLX  = 1.366362E-7
+DVT0W = 0        DVT1W = 0        DVT2W = 0
+DVT0  = 0.4490922 DVT1  = 0.3492005 DVT2  = -0.5
+U0   = 680.069603 UA    = 1.783144E-9 UB   = 1.68733E-18
+UC   = 4.48515E-11 VSAT  = 1.111807E5  A0   = 0.6117492
+AGS  = 0.1342138  B0    = 2.110777E-6 B1    = 5E-6
+KETA  = -8.827804E-3 A1   = 0        A2   = 1
+RDSW  = 3E3      PRWG  = -0.0186524 PRWB  = -9.622805E-3
+WR    = 1        WINT  = 6.90805E-7 LINT  = 1.023081E-7
+XL    = 0        XW    = 0        DWG   = -2.63673E-8
+DWB   = 3.757925E-8 VOFF  = -0.0850101 NFACTOR = 0.6718121
+CIT   = 0        CDSC  = 2.773385E-6 CDSCD = 0
+CDSCB = 2.593176E-5 ETA0  = 0.2224474 ETAB  = -0.1272268
+DSUB  = 0.7750765 PCLM  = 1.1286255 PDIBLC1 = 6.523298E-3
+PDIBLC2 = 3.710531E-3 PDIBLCB = -0.1    DROUT  = 0.0568465
+PSCBE1 = 2.501184E9 PSCBE2 = 5.732034E-10 PVAG  = 1.186702E-5
+DELTA = 0.01     RSH   = 52.9     MOBMOD = 1
+PRT   = 0        UTE   = -1.5     KT1   = -0.11
+KT1L  = 0        KT2   = 0.022    UA1   = 4.31E-9
+UB1   = -7.61E-18 UC1   = -5.6E-11 AT    = 3.3E4
+WL    = 0        WLN   = 1        WW    = 0
+WWN   = 1        WWL   = 0        LL    = 0
+LLN   = 1        LW    = 0        LWN   = 1
+LWL   = 0        CAPMOD = 2        XPART  = 0.5
+CGDO  = 1.79E-10 CGSO  = 1.79E-10 CGBO  = 1E-10
+CJ    = 2.707244E-4 PB   = 0.99    MJ    = 0.5644076
+CJSW  = 1.618906E-10 PBSW = 0.99    MJSW  = 0.1
+CJSWG = 6.4E-11   PBSWG = 0.99    MJSWG = 0.1
+CF    = 0        )
```

*

```
.MODEL CMOSP PMOS (                                LEVEL = 49
+VERSION = 3.1      TNOM  = 27      TOX   = 3.09E-8
+XJ   = 3E-7      NCH   = 2.4E16    VTH0  = -0.8476404
+K1   = 0.4513608  K2    = 2.379699E-5 K3   = 13.3278347
+K3B  = -2.2238332 W0    = 9.577236E-7 NLX  = 1E-6
+DVT0W = 0        DVT1W = 0        DVT2W = 0
+DVT0  = 0.9279152 DVT1  = 0.5820483 DVT2  = -0.1010777
```

```

+U0   = 236.8923827  UA   = 3.833306E-9  UB   = 1.487688E-21
+UC   = -1.08562E-10 VSAT = 1.411134E5   A0   = 0.8275501
+AGS  = 0.2147628   B0   = 2.093493E-6  B1   = 5E-6
+KETA = -3.37057E-3  A1   = 0           A2   = 0.364
+RDSW = 3E3         PRWG = 0.263341   PRWB = -0.2596674
+WR   = 1          WINT = 7.565065E-7  LINT = 1.215187E-9
+XL   = 0          XW   = 0           DWG  = -2.13917E-8
+DWB  = 3.857544E-8 VOFF = -0.0877184  NFACTOR = 0.2508342
+CIT  = 0          CDSC = 2.924806E-5  CDSCD = 1.497572E-4
+CDSCB = 1.091488E-4 ETA0 = 0.18903   ETAB = 5.276505E-3
+DSUB = 0.2873     PCLM = 2.8513297  PDIBLC1 = 9.977891E-3
+PDIBLC2 = 1E-3    PDIBLCB = -1E-3    DROUT = 7.25933E-3
+PSCBE1 = 3.350848E9 PSCBE2 = 5.017246E-10 PVAG = 15
+DELTA = 0.01      RSH  = 78         MOBMOD = 1
+PRT  = 0          UTE  = -1.5        KT1  = -0.11
+KT1L = 0          KT2  = 0.022       UA1  = 4.31E-9
+UB1  = -7.61E-18  UC1  = -5.6E-11    AT   = 3.3E4
+WL   = 0          WLN  = 1          WW   = 0
+WWN  = 1          WWL  = 0          LL   = 0
+LLN  = 1          LW   = 0          LWN  = 1
+LWL  = 0          CAPMOD = 2         XPART = 0.5
+CGDO = 2.23E-10   CGSO = 2.23E-10   CGBO = 1E-10
+CJ   = 2.745265E-4 PB   = 0.4450305  MJ   = 0.3021705
+CJSW = 3.852905E-10 PBSW = 0.99      MJSW = 0.1
+CJSWG = 3.9E-11   PBSWG = 0.99      MJSWG = 0.1
+CF   = 0          )
*
```