A Thesis

entitled

Design and Fabrication of a Micro-Machined Free-Floating Membrane on a Flexible Substrate

by

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Submitted to the Graduate Faculty as partial fulfillment of the requirements for the
Master of Science Degree in Electrical Engineering

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August 2010

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A MEMS device might function perfectly well in the controlled environment in which it was created. However, the device can be a real viable product only after it has been packaged with proven performance in a package. As such, the assembly yield of a MEMS package is often a challenging target to meet. This thesis is focused on the design and fabrication of a free-floating membrane on a flexible substrate to enable easy and cost effective packaging of MEMS devices. The advantages of this configuration are twofold. First, MEMS devices are fabricated on the flexible film while it is still bonded to the Si substrate, which provides mechanical support. Secondly, a grid pattern of membranes is surrounded by Si support structures, thus allowing the flexible circuit to be held flat by vacuum during various processing steps.

Since standard MEMS fabrication processes are designed for rigid substrates, several process modifications were required to handle flexible substrates. The adaptation of each fabrication process has been documented. Furthermore, detailed information regarding the selection of compatible materials, as well as incompatibilities that were encountered, has been presented to aid future researchers in developing flexible MEMS processes.

To the four pillars of my life: God, my parents, and my fiancé. Without you, my life would fall apart. I might not know where the life's road will take me, but walking with you through this journey has given me strength.

Sneha, you are everything for me, without your love and understanding I would not have been able to make it.

Mom, you have given me so much, thanks for your faith in me, and for teaching me that I should never surrender.

Dad, you always told me to "reach for the stars." I think I got my first one. Thanks for inspiring my love for technology.

We made it...

Acknowledgements

I would like to thank everyone who has helped me along the way - Dr. Devabhaktuni for providing me an opportunity to conduct my master's research under him and for his guidance and immense support over the course of it - you have been a great mentor; Dr. Christopher Melkonian for giving me an opportunity to work at Midwest MicroDevices (MMD), serving on my thesis committee, and his valuable suggestions; the engineering and production staff at MMD. I would also like to extend special thanks to my uncle Jatin Udeshi for everything he has helped me with; the Kaw family for their support; my roommates for all the memorable times; and lastly, my family.

I would also like to thank the Electrical Engineering and Computer Science (EECS) Department at the University of Toledo for the financial support in the form of Graduate Assistantship.

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List of Abbreviations

ARDE.....	Aspect Ratio Dependent Etch
CHF ₃	Trifluoromethane
CMOS.....	Complementary Metal Oxide Semiconductor
Cr.....	Chromium
CVD.....	Chemical Vapor Deposition
DRIE.....	Deep Reactive Ion Etching
E-Beam.....	Electron Beam
HF.....	Hydrofluoric Acid
IC.....	Integrated Circuit
Inductively Coupled Power.....	ICP
KOH.....	Potassium Hydroxide
LCP.....	Liquid Crystal Polymer
MEMS.....	Microelectromechanical Systems
Ni.....	Nickel
O ₂	Oxygen
PDMS.....	Polydimethylsiloxane
Research & Development.....	R&D
RF.....	Radiofrequency
RIE.....	Reactive Ion Etching
S1813.....	Shipley 1813
S1827.....	Shipley 1827
Si.....	Silicon
Si ₃ N ₄	Silicon Nitride
SiO ₂	Silicon Dioxide
STS.....	Surface Technology Systems
TMAH.....	Tetra Methyl Ammonium Hydroxide
TSV.....	Through Silicon Via
XeF ₂	Xenon Difluoride

Chapter 1

Introduction

Microelectromechanical systems (MEMS) are devices which convert physical phenomena, such as pressure, acceleration, sound, or light, into electrical signals. Every MEMS device interacts with the world in a different way, and demands custom or at least semi-custom packaging solutions. System-in-package techniques attempt to form an entire microsystem—which could include a microprocessor, communications components, actuators and sensors—within a single package. However, packaging of a MEMS device is totally different from packaging an integrated circuit (IC). MEMS devices are categorically different from ICs despite sharing some fundamental processing technologies. Packaging is the biggest challenge for commercializing most MEMS devices [1].

1.1 Motivation

1.1.1 Need for a Robust Packaging Technique for MEMS Devices

Package, in electronics, is the “material added around a component or integrated circuit to allow it to be handled without damage and incorporated into a circuit [2].” Packaging is a critical part of any electronic system, including MEMS. MEMS have

adopted a lot of the IC fabrication techniques with an exception of its packaging technology. The reason being that unlike ICs, MEMS devices often have mechanical components in addition to the electrical components. Thus a MEMS package not only has to protect the device mechanically and electrically but also allow the microstructures to interact with the environment to enable measurement of the desired physical/chemical parameters [3]. Due to this, there is no standard MEMS packaging technology and every MEMS package must be custom designed to optimize the devices performance [3-5].

A MEMS device might function as desired in the controlled environment in which it was created. However, the device can be a real viable product only after it has been packaged with proven performance in a package. MEMS devices include delicate movable structures which are easily damaged through fabrication and assembly processes. For example, the packaging stress can distort the sensitivity and the performance of the MEMS devices. As such, the assembly yield of a MEMS package is often a challenging target to meet.

The packaging requirements of MEMS devices are complex because the devices need to interact with the physical phenomenon and yet the devices need to be protected from the environment. As such, exotic package structures with specialized assembly techniques and unique packaging materials are employed. Packaging is usually responsible for anywhere between 60 to 85 percent of the cost of a MEMS device. Thus, there exists a need for a low cost packaging solution with robust assembly for MEMS devices.

1.1.2 Need for Devices on Flexible Substrates

Flexible substrates facilitate the production of conformal electronics, enabling foldable systems on a chip, made of sensors, electronics and actuators. These systems have a large potential of applications as electronic fabrics, smart tags and conformal sensors in the fields of defense, medicine, industrial monitoring and testing.

For numerous applications, it is essential to obtain the real-time 2-D profiling of certain physical parameters such as temperature, force, pressure or shear stress on a 3-D object. If the surface of the object is flat, this profiling can be achieved by using a monolithic MEMS device with a large amount of sensors [6]. However, it becomes a lot more difficult if the surface is non-planar. It has been a goal to develop a flexible MEMS technology (with integrated MEMS devices) that can be easily taped or glued on non-planar surfaces. Retrospectively, Barth et al. [7], in 1985 reported the first version of this idea with a one dimensional flexible Si-diode temperature sensor array in which a polyimide strip was the flexible material connecting Si islands formed by isotropic HNA etching.

The use of flexible substrates for the manufacture of electronic devices is growing rapidly. Flexible substrates are particularly advantageous where rapid, low-cost manufacturing is desirable. Particularly attractive is the possibility of using continuous fabrication techniques with rolls of flexible substrate. However, the difficulties in obtaining suitable flexible substrates and manufacturing/batch-fabrication techniques are formidable [8].

1.2 Research Objectives

The objective of this research is twofold - to develop a novel process to fabricate MEMS devices on flexible substrates and to design a free-floating membrane structure for robust and cost-effective packaging of the devices on flexible substrates. Fabricating the monolithically integrated devices on flexible substrates requires the development of new MEMS processes.

1.2.1 Research and Development (R&D) Leading to a New Technique for Permanently Bonding Flexible Films to Si Substrates

Various temporary bonding techniques have been reported in literature. Polydimethylsiloxane (PDMS), a bonding material that is inert, heat resistant, non-toxic and non-flammable has been investigated in order to make the bonding process suitable for most of the MEMS devices and allow its use in a numerous industries/applications. PDMS has been used, both as a temporary as well as a permanent bonding material. Other potential bonding materials including SU-8 resist, photoresist, polymeric compounds etc, which have been used for bonding [9-10] have also been investigated.

1.2.2 R&D of an Etching Technique for the Si Substrate

Based on its ability to create deep steep-sided holes and trenches in wafers, with aspect ratios of 20:1 or higher, Deep Reactive Ion Etching (DRIE) was chosen as one of the potential techniques to be used for etching Si substrates. However, DRIE is prone to feature size dependent etch rates, which may lead to non-uniform etch depths and some

branching [11-12]. To avoid such issues, a generic recipe for the DRIE of Si has been developed and demonstrated.

1.2.3 R&D of an Etching Technique for the PDMS Bonding Layer

Etching the bonding layer is of paramount significance to achieve a free-floating membrane. An etching technique has been designed and demonstrated for the bonding material, that is, PDMS. Etching methods including $O_2/SF_6/CF_4$ plasma etching, reactive-ion etching, and wet-chemical etching have all been investigated for the specific application at hand [13-14].

1.2.4 Investigation on the Need for Etch-Stop Layer(s)

It could be difficult to achieve uniform etching using DRIE. As well, other potential etching techniques, both for Si and the bonding layer have similar problems, and an etch stop layer is required to protect the flexible film against etchants. Therefore, etch-stop layer(s) have been employed to attain highly selective and uniform etch. Candidate etch stop layers include silicon dioxide (SiO_2) and silicon nitride (Si_3N_4) [15-16]. A flow diagram depicting the research objectives is shown in Fig. 1.1.

Fig 1.1 Illustration of the research objectives of the proposed research

1.3 Structure of the Thesis

Chapter 2 provides an overview of the theory surrounding the principal topics covered in this thesis, as well as a survey of relevant literature. Chapter 3 develops a novel method for fabrication of MEMS devices on flexible substrates. The method is validated against the traditional fabrication processes and a significant improvement in the production yield and reduction in the cost of production is observed. Information on material compatibility and a detailed justification of the choice of specific materials and processes is also provided with a view that it would serve as a starting point for future research. Chapter 4 develops a technique to achieve a free-floating MEMS-based device

suitable for RF energy detection, and includes the modification of each fabrication process step required to handle the flexible materials. Conclusions and future work are documented in Chapter 5.

Chapter 2

Review of MEMS on Flexible Substrates

As mentioned earlier, MEMS devices are essentially integrated circuits with moving parts. For example, in order to produce a freely moving mechanical structure, a temporary supporting layer is used during fabrication as shown in Fig. 2.1(a). This layer is commonly referred to as a sacrificial layer since it is removed as the final step of a MEMS fabrication process as shown in Fig. 2.1(b).

Fig 2.1. Typical MEMS device (a) fabricated using sacrificial layer as a temporary support and (b) after releasing the device.

Conventional MEMS fabrication processes are designed to produce devices on rigid substrates such as Si, glass and alumina. Fabricating MEMS devices on flexible substrates poses a significant challenge since the flexible substrate should remain flat

during all the processing steps involved. Also, the presence of organic materials (e.g. that used for bonding) limits the process temperature range. The first generation devices on flexible substrates were made on prefabricated sheets of polyimide using a Si wafer as carrier during the fabrication [17]. However during processing, the polyimide substrate could not be kept planar on the Si due to the formation of bubbles and the difference in thermal coefficients of expansion between the polyimide and the subsequent layers. The next generation of detectors was made by using spin-on polyimide layers (such as PI5878G from HD Microsystems), which were subsequently cured to form the flexible substrate. Again, Si wafers were used as a carrier. The completed devices were then peeled off the carrier to obtain the flexible detectors arrays [18]. However, the de-bonding/peeling of the polyimide from the Si substrate (to extract/recover the devices) posed several challenges like curling of the polyimide layer, damage to the fabricated devices due to curling/handling, and increased cost and time for packaging the device(s).

Several creative approaches to fabricating MEMS devices on flexible substrates have been reported in the literature. Section 2.1 documents several published processes in which the MEMS devices are mechanically supported by rigid islands of Si and the published MEMS processes for flexible substrates that are temporarily bonded to a rigid carrier for mechanical support.

2.1 Background d

2.1.1 MEMS Devices Supported by Rigid Si Islands

Figure 2.2 shows a process used to produce a MEMS conformal array of pressure sensors on a flexible substrate [19]. MEMS devices are fabricated on the top side of the

Si wafer. Silicon nitride is coated on the front-side of the wafer and is used as a mask to selectively protect back-side of the wafer. Back-side etching is carried out using potassium hydroxide (KOH) or tetra methyl ammonium hydroxide (TMAH) and then Reactive Ion Etching (RIE). To achieve almost vertical side walls using RIE, the wafer is etched using wet etching techniques until a thickness of less than 100 μm is achieved. Following the back-side etch, aluminum is evaporated and patterned onto the top side of the wafer. The aluminum layer acts as an etch stop layer when the silicon islands are formed. A 3-4 μm polyimide layer is spin-coated, cured and patterned to cover the aluminum etch stop areas. The contacts used to connect the MEMS devices are exposed by etching the silicon nitride protective layer. A second layer of aluminum, used for the interconnections, is deposited and patterned. A second layer of polyimide is then spin-coated, cured and patterned to cover the flexible network of interconnections.

Fig 2.2. Conformal MEMS Sensor Array [19]

On the back-side of the wafer, aluminum is deposited and patterned to form a mask. RIE etching using SF_6 is used to completely etch the remaining Si and silicon nitride between the islands. Removing the silicon nitride is extremely critical since it is brittle and could crack when the substrate bends. The final 10 μm layer of polyimide is spin-coated and cured on the back side of the wafer to completely encapsulate the Si islands.

According to [19], the peel-off force of the polyimide from Si is 0.23g/mm which is weak. Fully encapsulating the islands greatly increases the maximum tensile force (to about 3.57kg/mm).

The thickness of the Si islands is less than 100 μ m, and allows for minimum island dimensions of 100 μ m x 100 μ m, and a minimum spacing of 50 μ m between the islands. Since the wafers are fragile, the individual array of devices must be kept sufficiently small so that it will survive the fabrication process. The size of the array of devices is 1cm by 3cm. The Si islands are 450 μ m by 550 μ m and 75 μ m thick. Figure 2.3 illustrates the effect of using different etching techniques on the geometry of the Si islands, as shown in [19]. Figure 2.3 (a) shows a cross-section of the Si islands formed using HNA, an aggressive wet etching technique using a mixture of Hydrofluoric acid, Nitric Acid and Acetic Acid. The HNA etch is isotropic, resulting in the island tapering to a very thin edge that is extremely fragile. Figure 2.3 (b) shows a more robust geometry formed by anisotropic wet etching (TMAH or KOH). Figure 2.3 (c) illustrates the use of a combination of anisotropic wet etching and RIE to yield a geometry that ensures minimum thickness at the island edges. Of all the three examples, the geometry of Fig. 2.3 (c) is the most robust.

Fig 2.3. Various etch methods to produce Si islands [19].

This technique, though viable, includes a number of processing steps requiring precision and control. Also, a combination of wet and dry etching techniques, for the through wafer etch, demands for increased processing time. The above technique poses following challenges

- Increased cost of production
- Low yield due to the fragile nature of the etch stop layers
- Increased time for processing

Figure 2.4 illustrates a process that is capable of producing an array of solid Si probes with interconnects, which are later integrated onto a flexible substrate. The detailed process is outlined in [20]. The starting material is an oxide coated Si wafer. Polyimide is spin coated over the wafer to form a flexible substrate. However, metal wires (Cr and Ni) are patterned over the oxide before spin coating and curing polyimide to enable easy removal of the flexible substrates after fabrication. The Si wafer is then etched to form the probes. A combination of isotropic and anisotropic etching (eg. dry etching using XeF_2 and DRIE) is used for this purpose. The final step is to coat the devices with a spin on polyimide for insulation and to prevent the probes from detaching from the substrate.

The challenge in this technique is the combination of isotropic and anisotropic etching (highly selective) required to form the Si probes. Also, spin coating the polyimide layer may result in the formation of a non-uniform polyimide film, thus making device fabrication extremely difficult.

Fig 2.4. Si Probe Array [20]

The technique outlined in [21] uses boron doped Si as the flexible substrate, instead of polyimide. The heavily doped Si in addition to being inherently flexible, also acts as an etch stop for KOH wet etching [21]. The device has thick regions of undoped Si as rigid islands, connected together with the flexible doped Si (as shown in Fig. 2.5). The first step in the process is to define the islands with deep boron diffusion. The flexible interconnect region is defined by a shallow boron diffusion. Defining the geometry using diffusion regions leads to rounded structures, which are more robust as they do not contain sharp corners that crack easily [21].

Fig 2.5. Flexible circuit process using boron diffusion [21]

To make the wafer impervious to KOH etching, a plating base of evaporated Cr, followed by Au, is deposited on the top side of the wafer. Then a protective layer of nickel is electroplated over the top side of the wafer. The nickel protects the top of the wafer, and the silicon nitride protects the Si islands. As mentioned, the boron diffusion acts as an etch stop layer, defining the final thickness of the flexible substrate. After completing the KOH etch step, the nickel and gold plating base are stripped to give just the interconnected Si islands.

The lack of adhesion between the Si substrate and most of the flexible substrates makes this technique limited to be used only with a boron doped Si film, unless a bonding layer is used otherwise. The etching of the flexible substrates may not always be viable, since it may lead to significant impact on the flexibility, performance and other characteristics of the flexible film.

2.1.2 Flexible Substrates Temporarily Supported During MEMS Fabrication

Another technique of fabricating devices on flexible substrates is to use a Si wafer to temporarily support the structure during fabrication. Figure 2.6 shows a device fabricated using similar techniques outlined in [21] and [22]. Silicon nitride is first deposited onto the Si wafer. The flexible substrate is built up by spin-coating and curing multiple layers of polyimide onto the wafer, until the desired thickness is achieved. The silicon nitride layer over the polyimide serves dual purpose and acts both as a passivation layer and an adhesion layer for the devices. The MEMS device is fabricated on the supported flexible substrate, following the deposition of silicon nitride. After the device fabrication is

complete, the final step is to release the flexible substrate from the Si wafer. However, this technique is specific for devices that employ silicon nitride as a layer between the flexible substrate and the devices. Also, as stated previously, the silicon nitride layer is brittle and may crack during bending the flexible substrate, thus damaging the fabricated devices.

Fig 2.6. MEMS on flexible substrates created on a temporary rigid wafer support [22-23]

Another prominent technique is to fabricate MEMS phase shifters on liquid crystal polymer (LCP) substrates [24-25]. These devices address the flexibility issue by either temporarily bonding the material to a smooth rigid carrier using adhesives or by permanently attaching the LCP to a support using a thermal bonder. The unprocessed substrate, having 5-10 μm surface roughness, is not sufficiently smooth for MEMS device fabrication. Two planarization methods can be used to mitigate roughness issues: spin-coating and curing polyimide over the rough LCP surface [24], and/or mechanical polishing using alumina slurry [24-25]. As shown in Fig. 2.8, electrostatically actuated

MEMS cantilevers were fabricated using gold for the metal structure, and PECVD silicon nitride as a pull-down electrode insulator. Photoresist was used as a sacrificial layer, which was wet released in the final process steps, before drying the devices using a supercritical dryer. Use high temperatures, however, leads to hard-curing the photoresist, thus making it difficult to de-bond the flexible substrate/ remove the photoresist.

Fig 2.7. MEMS devices fabricated on LCP substrates [24-25]

In [26], MEMS tactile sensor devices were fabricated on LCP substrates. RIE Oxygen plasma was used to etch bulk substrate material at a rate of $0.22\text{-}0.27\mu\text{m}/\text{min}$. The researchers either directly laminated the LCP material to a rigid carrier or used photoresist as an adhesive. The MEMS sensors were fabricated on LCP with a NiCr strain gauge overlapping thick and thin substrate regions to form the transducer as shown in Fig. 2.9. The first step is to pattern the strain gauge, followed by etching the back side of the LCP substrate using an Al etch mask and RIE oxygen plasma. The final steps are to pattern the gold traces and form a polyimide bump on the top.

Fig 2.8. MEMS tactile sensor devices on LCP substrate [26]

In [27-28], a novel MEMS process fabricates inverted MEMS devices on a Si wafer, which are then transferred to a flexible FR-4 substrate. Before fabricating devices, a silicon nitride layer, used as the pull-down electrode insulator, is first deposited on the Si wafer. The next step is to fabricate the MEMS devices, which are cantilever structures that use silicon dioxide as a sacrificial layer. After fabricating the inverted MEMS devices, the Si wafer is flipped over and attached to the FR-4 substrate with an epoxy based film using a wafer bonder. The final stage of the process is to eliminate the Si wafer to leave the correctly oriented MEMS devices on the new substrate. Most of the Si wafer is removed by grinding, and the last 100 μm are etched using KOH. The newly exposed silicon nitride layer, used as an etch stop layer, is removed using RIE. The final process step is to release the MEMS devices using HF.

All the techniques listed in section 2.1 have been used successfully for packaging of MEMS devices. However, most of these packaging techniques are device specific and are suitable only for certain processing equipment. Also, because of the high processing cost

involved, the more robust techniques become unsuitable for use in a manufacturing environment.

2.2 Other Materials Used for Packaging

There are several commonly used materials when packaging a MEMS device. Fluorocarbon (polytetrafluoro-ethylene) is the most well-known packaging material for MEMS. It has desirable electrical characteristics, but poor adhesion and mechanical characteristics. Epoxy has good mechanical properties yet maintains poor ion and moisture barriers. When cured, epoxy shrinks, the mechanical, electrical, and thermal properties change. Acrylic packaging offers good electrical properties: is hard, rigid and tough, has little shrinkage during cure but has poor solvent resistance. Parylene can use chemical vapor deposition (CVD) to deposit thin, uniform pinhole-free films. It has good electrical properties, low permeability to moisture and gases and poor adhesion. Polyimide has both good mechanical and electrical properties. It is stable over a wide range of temperatures and is commonly used in microelectronics. Glass requires matching of thermal expansion coefficients and offers high strength, especially in compression. Glass, unfortunately, is also affected by stress concentrations due to surface imperfections. Ceramic packaging is inert and brittle with low fracture toughness. It offers good electrical properties and is an excellent moisture barrier. Ceramic requires high temperatures for sealing and is typically biocompatible. Metal packaging is lightweight; and some metals, like titanium, have excellent corrosion resistance. Metal, of course, offers good mechanical properties as well.

As described previously, MEMS devices have been used in various areas including biological, aviation, mechanical, automotive, and medicine. Finding the right packaging partner can significantly impact the success or failure of a MEMS product. Packaging partners not only need to integrate packaging with the MEMS design, but also need to test the MEMS devices and address additional aspects of assembly, i.e., calibration.

Chapter 3

Preliminary Experiments

3.1 Introduction

Numerous significant challenges exist in developing a process for fabrication of MEMS devices on flexible substrates (e.g. the process of photolithography requires substrates to remain flat for spin-coating, hot plate baking, alignment and exposure, the high process temperature of e-beam evaporations, need for organic adhesives etc). Furthermore, since MEMS devices have moving mechanical structures, they are prone to distortion when bending the substrate. This chapter documents the development of a novel process to fabricate MEMS devices on flexible substrates.

The first step in the fabrication process is to chemically clean the Si substrates in piranha (1:9 H_2O_2 : H_2SO_4) at 125°C for 10 minutes followed by a clean in hydrofluoric acid (HF) for 30 seconds. The advantages of this are twofold. First, use of clean substrates avoids the possibility of any contamination in the processing steps. The second benefit arises since the cleaning with HF makes the substrates hydrophobic, thus improving the adhesion between the substrate and the bonding layer.

Since standard MEMS fabrication processes are designed to produce devices on rigid substrates such as Si, glass or alumina, several process modifications were required to handle flexible materials. Section 3.3 documents the adaptation of each fabrication process step to handle flexible substrates.

A number of combinations of process and materials are available for fabrication of MEMS devices on flexible substrates. However, only a limited number of combinations are viable for each device due to compatibility issues between processes, materials and chemicals used for the specific device. In many cases, incompatibilities may be avoided by consulting with data from manufacturers, and from exceptional references such as [29] and [30]. In developing a novel process, however, data is not always available, and the initial experiments were carried out based on trial and error methods. Sections 3.2 and 3.4 document the selection of compatible materials and also highlight incompatibilities that were encountered to aid future researchers in developing MEMS processes. Section 3.5 documents the newly developed process which has been used to successfully fabricate working MEMS devices on flexible substrates. Appendix A provides detailed recipe for each step of the process of Section 3.5.

3.2 Choice of Flexible Substrate

The extensive combination of properties, which are required to obtain satisfactory MEMS devices using flexible substrates, makes it difficult to choose a suitable flexible substrate for any application/device. Some of the requirements include - the flexible dielectric substrate should be suitable for bonding, should be dimensionally stable and have long-term thermal stability. In addition, the flexible dielectric material should be

cost-effective, have high mechanical strength and be suitable for soldering. High tear strength, low cold flow, and low water absorption are some of the other critical requirements. Other required properties are high fire resistivity, good punch ability and availability in continuous rolls.

Most important of all are its electrical properties. It should have good insulator properties such as high resistance and low dissipative losses, and high breakdown voltage. Although many such materials have been proposed and used, improvements in some or all of the properties described above is highly desirable. The choice of flexible substrates available for use in electronics is thus very limited. Some of the popular flexible substrates used are Kapton, Teflon, PDMS, etc. Much background material on flexible circuitry is given in an article by J. M. Rausch in *Electronic Packaging and Production* (1975).

Several different options were considered when selecting a flexible substrate material. The candidate materials that can handle the process temperatures and chemical resistance requirements are Dupont Pyralux AP [31], Rogers ULTRALAM 3850 LCP [32], and Dupont Kapton. However, the surfaces of Dupont Pyralux AP and LCP are too rough for MEMS device fabrication without some form of planarization [33]. DuPont Kapton was selected as a flexible substrate material based on its unique combination of electrical, thermal, chemical and mechanical properties over a wide range of industrial environments and applications [34]. It has been used for temperatures as high as 400°C. Kapton also has a smooth surface with better than 100nm flatness [35].

3.3 Process Adaption for Flexible Substrates

Standard MEMS processes and fabrication equipment are designed to fabricate devices on rigid substrates such as Si, glass or alumina. The design of the processing equipments poses a major problem for the fabrication of devices on flexible substrates. The most common method of processing flexible substrates is by means of temporary bonding to a rigid wafer that acts as a carrier. This method, however, is only feasible under limited conditions since the adhesive material peel strength may change significantly when cycled through high temperatures and conditions encountered during processes like sputtering, e-beam evaporation, PECVD, etc.

Photolithography processes like spin coating, alignment and exposure, and hot plate baking require the substrate to be flat. Additionally, the hot plate baking requires an intimate thermal contact between the substrate and the vacuum hot plate to ensure adequate heat flow through the substrate to the photoresist. This requires the bonding of flexible substrates using a thermally conductive bonding material. Also, the flexible substrate would have to be bonded and held extremely flat through all the processing steps. Care should also be taken to ensure that the edges of the flexible substrate are secured properly, since an air gap could lead to various problems (e.g. misalignment in photolithography) for different processing steps. If the flexible substrate is secured to a rigid wafer using a double-sided adhesive layer covering the entire area, the photolithography process is almost identical to the rigid wafer version. The only required modification could be in the photoresist baking time and temperatures, depending on the thermal contact between the wafer and the flexible substrate.

Experiments were carried out using both, 1 mil and 2 mil DuPont Kapton film rolls. Dow Corning Sylgard 184 PDMS was used to bond the entire back side of a flexible substrate to a rigid Si wafer. This bonding method ensured intimate thermal contact between the flexible substrate and Si wafer - a requirement for adequately baking the photoresist during photolithography processing. Since it was not possible to use the temporary bond between the flexible substrates to rigid carriers for all processes, creative workarounds were later developed for each specific process. The process specific adaptations are later described in Chapter 4.

3.4 Section of Metals

Metals were deposited using electron beam (e-beam) evaporation. Several metals including aluminum, copper, gold, silver, chromium, titanium, and platinum were deposited and tested for compatibility. In practice, it was found that aluminum and silver have excellent adhesion properties and did not require an intermediary adhesion layer to first be deposited on the substrate. Gold, however, required adhesion layers of chromium or titanium to prevent the metal from peeling away from the substrate.

Initially, silver appeared to be a good choice for MEMS device fabrication, provided the application did not require DC contact switching which would be affected by oxidation. In addition to excellent conductivity, the processing is straightforward since silver was found to adhere readily to Kapton with no adhesion layer. Unfortunately, silver oxidation presented issues that were more serious than increased contact resistance. However, silver is the best choice for a temporary layer that may be removed before starting MEMS device fabrication.

Gold is an excellent material for producing MEMS DC contact switches, since its electrical properties are not affected by rapid oxidation experienced by many other conductors. In addition to its high cost, however, gold presents significant processing challenges. As discussed previously, an adhesion layer is required between the substrate and gold. Chromium and titanium were both used as adhesion layers to enable gold to successfully adhere to Kapton.

Aluminum was found to have excellent adhesion to Kapton without the need for an adhesion layer. The result is a straightforward process that produces reliable MEMS devices. The significant drawbacks of using aluminum are its low conductivity as well as the resistance of aluminum oxide.

3.5 Fabrication of Devices Using a Temporary Bond

The experiments described in this section were conducted before designing the free-floating membrane structure. This set of experiments was done in order to conclusively establish that this technique can be used to fabricate MEMS devices on flexible substrates using traditional processing equipment. These experiments were done on a trial and error basis. Considering the limitations of the scope of this research, the best workable solutions were selected.

3.5.1 Bonding Principle

The most practical method for fabrication of devices on flexible substrates is to have a solid polyimide sheet that can be temporarily adhered to a Si carrier wafer, such that it can be separated at the end of fabrication. This fabrication process can be accomplished

with conventional Si processing equipment and is relatively simple. Figure 3.1 shows a temporary adhesion method that employs the principle which causes stiction - the adhesion of contacting surfaces due to surface forces in wet released MEMS devices. A small drop of DI water is first placed on a rigid wafer, followed by the flexible substrate as shown in Fig. 3.1(a). The wafer is then heated, causing the water to evaporate. As the water volume decreases, the flexible substrate is pulled down by surface tension until it contacts the rigid substrate, as shown in Fig. 3.1(b). Although this method was used successfully during a couple of initial process development stages, the substrate did not hold during the spin-coating process. Additionally, the flexible substrate released from the Si substrate, as soon as it was immersed in the liquid developer.

3.5.2 Material Used for Bonding

PDMS is the most widely used Si-based organic polymer, and is particularly known for its unusual rheological (or flow) properties. It is optically clear, and, in general, is considered to be inert, non-toxic and non-flammable. PDMS has temporary adhesive properties which are described in [36]. It has been used for temporary adhesion in [37 – 39].

Based on the properties and its compatibility with other materials, PDMS was chosen as the candidate bonding material to bond the flexible substrate to the rigid Si carrier. Though the aim is to ultimately peel-off the Kapton film after the processing, care should be taken to avoid any potential defects in the film or the PDMS layer, since it could lead to de-bonding of the Kapton film in middle of processing.

(a)

(b)

Fig. 3.1 Flexible substrate held to rigid wafer by (a) placing a small drop of DI water between the substrate and carrier and (b) heating substrate such that the surface tension pulls the substrates together as the water evaporates.

3.5.3 Temporary Bonding Technique

For this process, an ordinary, rigid, single-side polished Si wafer is used as a temporary carrier. The fabrication begins with preparing the PDMS (Sylgard 184 elastomer, Dow corning) mixture. The PDMS precursor is mixed with its curing agent in a ratio of 10:1 by weight. Subsequently, the mixture solution is gently stirred and then degassed in vacuum for about 45 to 60 minutes in order to remove air bubbles. This is followed by the PDMS liquid precursor spin coating.

Generally, the shear forces at the outside edges of the wafer are different than those at the center. Since PDMS is a non-Newtonian fluid, the different shear forces affect the uniformity of the final coating. Also, the spin speed and spin time are accommodated to unique needs depending on the substrate size, shape and coating mass as well as the desired film thickness and uniformity required.

Specifically, adequate PDMS precursor is dispensed onto the center of Si carrier. Then the spin starts with the determined spin speed leading to the liquid precursor wetting out on the entire surface and throwing the gross excess coating. The coating was done at a 10 second spread at 500 rpm and different spin speeds – 2000, 3000, 4000, and 5000 rpm for 30 sec were tried to obtain the best coat. It was observed that the best results were achieved with a spin speed of 3000 rpm for 30 seconds, as seen in Table 3.1. The spin coating is followed by a cure for 60 min at 100°C to reduce thermal cycling due to the thermal expansion difference between the Si carrier and PDMS interlayer.

Table 3-1 PDMS coating at different spin speeds

Spread Spin	Speed	Observations
10 sec @ 500 rpm	30 sec @ 2000 rpm	Coating not uniform. Striations appear.
10 sec @ 500 rpm	30 sec @ 3000 rpm	Best overall quality. Smooth coating i.e. no obvious striations appear.
10 sec @ 500 rpm	30 sec @ 4000 rpm	Small striations appear.
10 sec @ 500 rpm	30 sec @ 5000 rpm	Bubbles appear.

This approach attains about 20-25 μ m thick membrane with a relatively uniform film thickness. Experimenting with the spin speeds will produce the widest range of results in final coating thickness. The variation of thickness depending on the spin speed is shown in Fig 3.2. The coated PDMS layer is then cured at 100°C for 60 minutes [39]. It should be noted that the cured PDMS surface is originally hydrophobic. Therefore, prior to bonding with the Kapton film, the PDMS membrane and the Kapton film are treated with oxygen plasma for 120s at an RF power of 400 W under the pressure of 200mT. This step

is essential to turning the PDMS surface hydrophilic to allow the bonding of the Kapton film with necessary adhesion and guarantee a smooth and uniform bond [14].

Fig. 3.2 Graph showing thickness of PDMS versus spin speed

Fig. 3.3 Temporary bonding of Kapton to the Si substrate using PDMS interlayer

Fig. 3.4 Kapton film bonded on a Si substrate using PDMS

The Si substrate and the Kapton film were bonded using a traditional roller bonder. The bonding should be done ensuring no air bubbles appear between the substrates, to avoid any potential problems during processing. Expansion of the air bubbles due to the heat in various processing steps (e.g. E-beam evaporation, photolithography *etc*) may lead to failure of the bond, thus resulting in de-bonding of the substrates during processing.

After bonding, the PDMS layer is put through an additional cure. This post bond cure improves the strength of the temporary bond. To evaluate the cure parameters, various samples were cured at different temperatures and time and then put in an ultrasonic tank containing acetone, to ensure the sustainability of the bond for lift-off processing. The results obtained for a 2mil Kapton film bonded on a Si substrate are given in Table 3.2. It is clear from the table that a post bond cure at 100°C for 2 hours gives the best results, *i.e.* the strongest bond. It should however be noted that, though these cure parameters may be

optimum for a PDMS layer with a given thickness, they are subject to change depending on the thickness of the PDMS layer. The results obtained for a 1 mil thick Kapton film were similar.

Table 3-2 Performance of the temporary bond for different post bond parameters

No	Cure time	Cure temperature (°C)	Time in acetone	Percentage of lifting
1	60 min	100	30 min	30% - 35%
2	120 min	100	30 min	15% - 20%
3	60 min	120	30 min	40% - 45%
4	120 min	120	30 min	50%
5	None	None	30 min	60% - 70%

Utilizing standard photolithography, the device wafer was then patterned for the metal layers. Two metal layers were deposited on the Kapton film by e-beam evaporation. Electrical leads were defined by dissolving away the photoresist under the metal layers in acetone. To improve the process sustainability and device production yield, no water was used for lift-off. The lift-off was done in an ultrasonic tank filled with acetone, followed by a rinse in IPA.

The low adhesion between the Kapton film and the PDMS interlayer makes the separation of devices fairly easy and the Kapton film can be peeled off from PDMS interlayer upon the Si carrier, once the fabrication is complete, yielding a flexible device sheet. The fabricated samples of the devices on a Kapton film are shown in Fig. 3.5 (a) and (b). As seen from the figures, devices fabricated on the Kapton sheet are flexible

enough to be folded and twisted freely to make any desired shape and form required for various applications.

Using this technique, devices were successfully fabricated on the flexible Kapton substrate (for a complete process flow, refer to Appendix A). To retrieve the flexible devices at the end of fabrication, the Kapton film had to be peeled off manually. This traditional (i.e. manual) de-bonding of the Kapton film, however, poses several challenges:

- Curling of the Kapton film to an extent, which makes dicing difficult;
- Misalignment in photolithography due to the debonding of the Kapton film during processing;
- Damage to the fabricated devices due to curling/handling; and
- Increased cost and time for packaging the device(s).

These issues lead to a poor yield and increased cost of production. To address these issues a “free-floating membrane structure” was investigated and developed.

(a)

(b)

Fig. 3.5 (a) and (b) Devices fabricated on a flexible Kapton film

Chapter 4

Design and Fabrication of a Free-Floating Membrane Structure

4.1 Initial Processing on the Substrates

As discussed in section 3.1, the fabrication process begins with cleaning of the Si substrates. For all the processing, standard, single side polished 4" Si substrates (525 μ m thick) were used. The choice of the Si substrate is not very significant and the substrates were solely chosen based on the ease of availability. The Si substrates were chemically cleaned in piranha solution (1:9 - H₂O₂:H₂SO₄) at 125°C for 10 minutes followed by a clean in HF (100:1) for 30 seconds. A 1 μ m thick PECVD oxide was deposited on the Si substrates. This oxide layer acts as an etch-stop layer for the DRIE process. Precut 6"x6" Kapton sheets were solvent cleaned and then dehydrated in an oven at 120°C for 20 minutes.

4.2 Permanently Bonding the Substrates

In order to achieve a free floating membrane structure (shown in Fig. 4.1), it is very critical to have a strong/permanent bond between the two substrates to ensure reliability

in performance and lifetime of the devices. Since PDMS was the material of choice used for the temporary bonding, for various reasons, we further investigated the chances of achieving a permanent bond using PDMS. After trying numerous different combinations of pre-bond and post-bond cure temperatures, it was concluded that a permanent bond cannot be achieved between the two substrates using PDMS alone.

Fig. 4.1 Free floating Kapton membrane resting on Si support structures

Primers and adhesion promoters can be applied to a substrate to enhance the bond strength between a surface coating (e.g., clear coats, adhesives) and the substrate. They differ in terms of type and chemistry, substrate compatibility, technology, application method, color, and finish. Primers and adhesion promoters are used in a variety of industrial and commercial applications. Based on the recommendation from the manufacturer of PDMS, Dow Corning 92-023 primer was used to enhance the strength of the bond between the Kapton film and the Si substrate.

A thin coat primer was applied on a dehydrated Kapton film by brushing with a wipe. A thin film primer gives best adhesion. Film thickness can be roughly estimated by color,

the thicker the film, the whiter the appearance. If cracks appear in the film, too heavy a coat was applied. White dust or flakes on the surface also indicate too heavy a coating [40]. The primer cures when in contact with air moisture. Figure 4.2 shows the effect of humidity on the drying time of the primer [40]. Based on the humidity in the clean room, a cure time of 2 hours was chosen. As a general rule, drying times of more than 6 hours at normal temperature and humidity conditions should be avoided.

Fig. 4.2 Effect of humidity on drying time of Dow Corning 92-023

Once the primer was cured, the PDMS was spin coated on the Si substrates at a speed of 3000 rpm for 30 seconds. The spin speed was chosen based on the results obtained in section 3.3. Immediately after the coating, Kapton sheets were bonded to the PDMS layer using a roller bonder. The bonded substrates were then allowed to cure for 24 hours at room temperature.

4.3 Effect of Resist Solvents on the Permanent Bond

Most of the MEMS devices require metal layers as a part of the circuit or as electrical contact points. These metal layers can be deposited by e-beam evaporation, sputtering etc. Electrical leads are then defined by dissolving away the photoresist under the metal layers in a resist solvent like acetone. It is thus imperative that the permanent bond be unaffected to lift-off processes. To test the effect of resist solvents on the bond, mock lift-offs were performed on a number of permanently bonded device wafers. The lift-offs were done in resist solvents including acetone, 1165, and PRS 2000 for different time periods to determine the maximum time for which the solvents do not attack the permanent bond. Table 4-1 shows the results of the mock lift-offs. As shown in Fig. 4.3, it was observed that the resist solvents tend to damage the permanent bond. The Kapton film started lifting from the edges of the wafer, and the lifting progressed towards the center, with time. The extent of the damage was more or less similar for all the solvents. One of the reasons for this could be that the solvents attack and swell the PDMS [41].

Table 4-1 Results of the mock lift-off tests

Sr. no.	Resist solvent	Maximum time that the permanent bond can survive the liftoff process in an ultrasonic tank
1	Acetone	20 min
2	1165	8 min
3	PRS 2000	10 min

Fig. 4.3 A permanently bonded Kapton substrate after a 40 minute liftoff in acetone

4.4 Modification of the Lift-off Process

Since the resist solvents attack the permanent bond, a modified lift-off procedure was required. The results of the lift-off indicated that the attack on the bond started at the edge and progressed towards the center of the wafer, with time. The attack on the bond can be prevented if the edges of the wafer are protected by a mechanism/set up to prevent the solvents from seeping between the two substrates. To achieve this, a strip of Parafilm M was used to mask the edges. Parafilm M is a self-sealing, moldable and flexible film for numerous uses in the typical laboratory including electron microscope laboratories. Parafilm M has unique permeability properties, impressive water vapor transport properties, and is resistant to many common reagents [42]. It lifts easily and leaves no residue behind on the surface being protected.

A thin strip of Parafilm M was placed around the entire perimeter of the wafer. It was bound to the substrates manually using finger pressure. The wafer was then put through a lift-off process in acetone for 20 minutes. It was observed that the bond was unaffected. Fig. 4.4 shows the comparison of results for the wafer with the Parafilm M protection and the wafer without any edge protection, after a 20 minute lift-off. Notice that the edges of the wafer without edge protection are lifted (circled in blue in Fig. 4.4 (b)). To ensure the reliability of this technique, four lift-offs of 20 minute each were performed on another set of wafers with Parafilm M protection. The results were very impressive and with very little effect on the permanent bond. From this, it can be inferred that the solvents tend to attack the permanent bond, only if the edges of the wafer are exposed during the lift-off process.

Fig. 4.4 A 20 minute acetone lift-off on (a) a wafer with edge protection, and (b) without edge protection

The use of Parafilm M may not be viable in a manufacturing environment owing to its non-robustness. Thus alternative sustainable processes for edge protection were investigated. One of the potential solutions was to bond a Kapton film of slightly lower diameter (5 - 10 mm less) than the Si substrate. A 25 μ m thick resist film of SU-8 was

coated over the entire wafer. The SU-8 is a negative, epoxy-type, near-UV photoresist based on EPON SU-8 epoxy resin (from Shell Chemical). This photoresist can be as thick as 2 mm and aspect ratio >20 and higher have been demonstrated with standard contact lithography equipment. This is due to the low optical absorption in the UV range, which limits the thickness to 2 mm for the 365nm-wavelength, where the photo-resist is the most sensitive (i.e., for this thickness very little UV light reaches the bottom of the structure) [43].

The SU-8 was patterned and developed such that it a 5-10 mm wide strip of SU-8 was coated over the edges as shown in Fig 4.5. However, due to the poor adhesion between SU-8 and Kapton, as well as the oxide on the Si substrate, the SU-8 strip starts lifting when put it acetone for more than 15 minutes (Fig 4.6). Owing to this, it cannot be used for processes that require processing in acetone for more than 15 minutes. This method, however could be modified by changing the cure temperatures, thickness of SU-8, exposure dose etc. to improve the adhesion between the SU-8 and the substrates.

Another technique for lift-off, using a spin track, was developed. A spin track comprises of a wafer holder/chuck in the centre. The chuck is placed on a shaft, connected to a motor. The principle of the spin track lift-off is to use the centrifugal force of the spin action such that the resist solvent is in contact with only the top surface of the substrate. There is no attack into the edges since the centrifugal force throws off any excess acetone. This technique was initially tested on a Solitec spin coater. The wafer was spun at a speed of 500 rpm and acetone was constantly sprayed on the wafer for over 60 minutes. The results of this test revealed that the spin track lift-off completely avoids any attack to the bond by the resist solvent.

Fig. 4.5 A strip of SU-8 resist coated over the substrates for edge protection

Fig. 4.6 Damage to the SU-8 edge protection after a 15 minute lift-off in acetone

Fig 4.7 shows the wafer after a 60 min lift-off on the spin track. This method is thus suggested for sustainable results in a manufacturing environment. However, the lift-off with Parafilm M edge protection works completely fine and may be used for prototyping or if the spin track lift-off is unavailable.

Fig. 4.7 Result of a 60 minute lift-off on a spin track

4.5 Metallization and Photolithography

After the substrates have been bonded, devices are fabricated on the Kapton film. Instead of fabricating a device, four different metal layers were deposited on the wafer to demonstrate the feasibility of device fabrication. Metal deposition was accomplished using an electron-beam evaporation system. Shipley 1813 (S1823) photoresist was used

for photolithography before every metal layer deposition. S1813 was spin coated to achieve a thickness of 1.2 μm . After each metal layer deposition, the edges of the wafer were carefully protected with a thin strip of Parafilm M for lift-off. The lift-off was done in an ultrasonic tank containing acetone. It took at the most 20 minutes for completely lifting off each metal layer.

4.6 Front Side Protection

Once the devices have been fabricated on the Kapton film, they should be protected to avoid damage of the devices in processing steps that follow device fabrication. The front side protection layer also protects the devices from any possible attack/contamination by the chemicals used, especially the buffered HF. For the front side protection, a layer of Shipley 1827 (S1827) photoresist was used. S1827 is a negative photoresist and it serves as an excellent protection layer against most of the processes and numerous chemicals. S1827 was spin coated at 2000 rpm for 30 seconds and then soft baked at 115°C for 90 seconds.

4.7 Back Side Patterning and Oxide Etch

For the formation of a free-floating membrane structure, the Si substrates have to be etched in a way that results in an open area under the fabricated devices, leaving behind Si support structures for supporting the free floating membrane, as shown in Fig. 4.1. The selective etching can be achieved by patterning the back side of the Si substrate using a protective resist, such that only the areas to be etched are exposed to the plasma of the DRIE system. For this, a 10 μm thick layer of AZ 9260 photoresist was coated on the

back side of the Si substrates. The photoresist was coated at a spread speed of 300 rpm for 4 seconds and a spin speed of 2000 rpm for 30 seconds, followed by a softbake for 4.5 minutes at 110°C. An exposure dose of 1200mJ was used. After developing it in the AZ400K solution for 2.5 minutes, the resist was hard baked for 2 minutes at 110°C.

Since, an oxide layer is needed as an etch stop layer for the DRIE, PECVD oxide was coated on the Si substrates. The PECVD oxide deposits on both sides of the substrate and thus an oxide layer etch is required even prior to the DRIE. As already mentioned, a 1µm thick oxide layer was deposited on the Si substrates. The oxide etch was performed in buffered HF solution for 12 minutes as the etch rate of oxide in a buffered HF solution is about 1000Å/min.

4.8 Deep Reactive Ion Etching of Si

DRIE is a highly anisotropic etch process used to create deep, steep-sided holes and trenches in wafers, with aspect ratios of 20:1 or more. It was developed for MEMS systems, which require these features, but is also used to excavate trenches for high-density capacitors for DRAM and more recently for creating through wafer via's (TSV)'s in advanced 3D wafer level packaging technology. There are two main technologies for high-rate DRIE: cryogenic and Bosch, although the Bosch process is the only recognized production technique. Both Bosch and cryogenic processes can fabricate 90° walls, but often the walls are slightly tapered, e.g. 88° or 92°. Another mechanism is sidewall passivation: SiO_xF_y functional groups (which originate from sulphur hexafluoride and oxygen etch gases) condensate on the sidewalls, and protect them from lateral etching. Using a combination of these processes, deep vertical structures can be made [44].

The proposed research uses Bosch process for etching the Si substrate. The Bosch process, also known as pulsed or time-multiplexed etching, alternates repeatedly between two modes to achieve nearly vertical structures.

1. Standard, nearly isotropic plasma etch. The plasma contains some ions, which attack the wafer from a nearly vertical direction
2. Deposition of a chemically inert passivation layer with a substance similar to Teflon.

Each phase lasts for several seconds depending on the etch features and depth. The passivation layer protects the entire substrate from further plasma attack and prevents further etching. However, during the etching phase, the directional ions that bombard the substrate attack the passivation layer at the bottom of the trench (but not along the sides). They collide with it and sputter it off, exposing the substrate to the plasma etchant. These etch/deposit steps are repeated many times over resulting in a large number of very small isotropic etch steps taking place only at the bottom of the etched pits.

A typical DRIE system entails having an inductively coupled power (ICP) source to provide a high-density plasma, and an independent substrate power bias to provide directional ion bombardment during the etch step. C_4F_8 is the gas typically used for this passivation step, and it deposits on the substrate in a conformal manner. This is followed by the etch step, a simultaneous engagement of the substrate bias and flow of SF_6 . During this step, the sidewalls of the Si trench are relatively protected by the C_4F_8 induced polymer layer. The bottom of the trench being formed, although also coated with polymer, is pierced by the directional ion bombardment. The Si is then etched by means

of reaction. The iteration of these passivation/etch cycles allows the desired anisotropic features to be achieved.

Along with other high density plasma microfabrication processes, the DRIE process in general is well known to have variability in terms of response. Results can differ from day to day, and this can make processing at best challenging, and at the very worst impossible. The responses of main interest include etch rate, mask selectivity, ARDE (Aspect Ratio Dependent Etch), and the uniformity of the etch across the wafer. The etch rate of the process however is of utmost concern, as this typically has a direct influence or link to the other responses of interest.

A STS (Surface Technologies Systems USA Inc., Redwood, CA) Pegasus DRIE system at the Lurie Nanofabrication Facility, MI was used for etching the substrates. A recipe, detailed in Appendix C, was developed to achieve highly anisotropic through wafer etch. Figure 4.8 shows the results of a through-wafer etch in the DRIE system. The wafer showed in the figure has few non-etched areas, which are a result of the poor oxide etching prior to the DRIE. The etch rate, using the developed recipe is highly dependent on the feature sizes and the amount of area to be etched. Based on the mask/pattern used, the through wafer etch took about 40 minutes of etch time. It should although be noted that the etch time will vary depending on the tool condition and the etch features. Figure 4.9 shows a graph of the etch rate versus feature size for the developed recipe. The capabilities of the recipe are as follows:

- Smallest Trench: 0.618 μm
- Smallest Freestanding line: 4.29 μm
- 2 μm Etch Rate: 4.63 $\mu\text{m}/\text{min}$ (Photoresist selectivity 38:1)

- 10 μ m Etch Rate: 7.1 μ m/min (Photoresist selectivity 57:1)
- 100 μ m Etch Rate: 12.5 μ m/min (Photoresist selectivity 88:1)
- Photoresist Etch Rate (SPR220): 77nm/min
- Undercut: 483nm

Before etching, a carrier wafer is bonded to the substrate, for membrane protection. The carrier and the Si substrate were bonded using Crystalbond 555. Crystalbond 555 is a temporary adhesive used for mounting two substrates. It exhibits high bond strength and adheres readily. The best adhesion is obtained when the part to be embedded is first heated to the temperature of the melting point of the Crystalbond (95°C in this case) used. If this is not done, inferior adhesion might be experienced [45]. When processing is complete, Crystalbond adhesive can be removed by reheating and cleaning with a wide range of different solvents and water.

Fig. 4.8 Result of the DRIE on a Si substrate

Fig. 4.9 Etch rate v/s feature size for the DRIE recipe used

It was observed that the Crystalbond reacts with the front side protection layer (S1827). It does not affect the bond strength or the heat transfer during DRIE in any way. However, after de-bonding the carrier, when the etched wafer was put into buffered HF for the oxide etch, it was observed that the metal layers were also etched away. This indicated that the Crystalbond reacts with the S1827 photoresist and takes it off the wafer during de-bonding. Thus a fresh front side protection layer needs to be coated on the devices after the DRIE.

On few samples that were heated to temperatures over 110°C during de-bonding, the Crystalbond and photoresist reacted to form a residue on the device wafer as well as the carrier. Figure 4.10 (a) and (b) show the residue (circled in blue) on the device wafer. The residue was unaffected even after multiple tries to strip it in piranha solution. Care should thus be taken to not overheat the Crystalbond while bonding/de-bonding the carrier.

Fig. 4.10 (a) and (b) Crystalbond residue on the fabricated devices after de-bonding

4.9 Etching of the PDMS Bonding Layer

The DRIE of the Si substrates stops at the oxide layer. This oxide layer has to be etched before etching the PDMS. Based on the standard etch rate, a 12 minute etch time in buffered HF is sufficient to remove the 1 μm oxide layer.

PDMS is a Si-based polymer, thus the required etch chemistry is different from that of polymers consisting mainly of carbon and hydrogen. These polymers can be etched with oxygen, but the siloxane bonds (Si– oxygen–Si) that make up the backbone of the polymer chains in PDMS are not easily broken by oxygen plasma.

Any by-products of the oxygen plasma treatment of Si–O bonds are in general not volatile. Oxygen plasma is useful for surface activation of PDMS. Surface activation in oxygen plasma increases the surface energy and enhances the wettability of the polymer. The effect is only temporary, however, and the surface recovers its natural hydrophobic state over time [46]. Surface activation also enables two surfaces to bond together when brought into contact. This technique is useful for bonding together individual PDMS

device layers [47]. Prolonged exposure of PDMS to oxygen plasma only changes the surface into a brittle silica-like layer with tiny cracks [46]. PDMS cannot be dry etched with oxygen alone, yet it does appear to increase the etch rate of CF_4 [13].

Since PDMS is a Si-based polymer, it requires an etch chemistry similar to that required by Si or silicon dioxide. CF_4 is often used to etch Si and silicon dioxide because the fluorine atoms form volatile compounds with Si. While the exact etching mechanism of PDMS in a CF_4/O_2 plasma has not been determined, the material resembles a combination of silicon dioxide and a carbon-based polymer. CF_4 probably etches PDMS in the same way that it etches silicon dioxide, i.e., by forming volatile SiF_x compounds. There are at least two possible explanations for the increase in PDMS etch rate that occurs when oxygen is added to the CF_4 plasma. First, adding oxygen to CF_4 has been found to increase the etch rate of Si and silicon dioxide by increasing the amount of reactive fluorine atoms present in the plasma [48]. The effect is based on the interaction between atoms in the gas phase and is not dependent on the substrate, so it is equally likely to occur when etching PDMS. The second explanation is based on the fact that while PDMS is a Si-based polymer, it still contains carbon and hydrogen in the form of methyl groups that occur periodically along the polymer chains. It is possible that these methyl groups are more easily removed when oxygen is added to the plasma, enhancing the overall rate of attack on the PDMS structure [13]. PDMS, like silicon dioxide, apparently requires a fluorine-based etch chemistry. Wet etching of PDMS is also possible, but it results in severe undercutting [13]. Furthermore, wet etching of PDMS can adversely affect the bonding of PDMS to substrates [49].

The PDMS was mixed in a 10:1 ratio with its curing agent and then placed in a vacuum desiccator for at least 45 min to remove the bubbles created during mixing. Samples were then made by spinning the polymer on Kapton bonded substrates and curing at room temperature for 24 hours. To determine the etch rate, experiments were performed in a LAM Research Drytek RIE system equipped for reactive ion etching, available at Midwest MicroDevices, OH. Oxygen (O_2) and trifluoromethane (CHF_3) were used for etching the PDMS. All samples used for etch rate determination were etched for 60 min while the CHF_3/O_2 ratio, total gas pressure, and RF power were varied. The surface of each sample coated with S1827 photoresist and patterned prior to etching, in order to create a distinct step feature that could be measured using a Dektak 3030 stylus profilometer. Several samples were etched and the average step-height value was used.

From the data obtained through profilometry, the parameters giving the highest etch rate were determined. The fastest etch rate, 12 $\mu\text{m}/\text{hour}$, was obtained in a mixture of CHF_3 and O_2 at a 3:1 ratio (47 mTorr, 300 W), and in O_2 alone, PDMS was not etched. Based on this etch rate, it took about 2 hours to completely etch through the PDMS bonding layer. The parameters of this etch recipe are detailed in Appendix D.

4.10 Overview of the Fabrication Process

This chapter has documented the development of a novel process to fabricate MEMS devices on flexible substrates (Refer Appendix B). This innovative process has been used to successfully fabricate working MEMS devices on flexible substrates. The free floating membrane is rested on support structures which are obtained by etching through the Si substrate and the bonding layer. The advantages of this configuration are twofold. First,

MEMS devices are fabricated on the flexible film while it is still bonded to the Si substrate, which provides mechanical support. The second benefit arises since a grid pattern of thin membranes is surrounded by Si support structures, thus allowing the flexible circuit to be held flat by vacuum during photolithography.

Since standard MEMS fabrication processes are designed to produce devices on rigid substrates such as Si, glass or alumina, several process modifications were required to handle flexible materials. The adaptation of each fabrication process step to handle flexible substrates has been documented. Furthermore, detailed information regarding the selection of compatible materials, as well as incompatibilities that were encountered, has been presented to aid future researchers in developing flexible MEMS processes. The end result is a viable MEMS fabrication process that yields devices on a flexible substrate. The complete process flow is shown in Fig. 4.11.

Si substrate

Growing SiO_2 -
Etch stop layer

Spin-coating
PDMS

Bonding of the Kapton
film

Resist coating

Device fabrication and
front side protection

Back side protection
for DRIE

AZ 9260 resist

Patterning AZ 9260

SiO₂ etching using buffered HF

DRIE etching of the Si substrate

SiO₂ etching using buffered HF

RIE of the PDMS interlayer

Stripping the resist protection layer

Fig. 4.71 Process flow of the proposed research

Chapter 5

Conclusions and Future Work

5.1 Conclusions

A new micro-machined free-floating membrane on a flexible substrate is presented. Unlike previously reported techniques, a layer of PDMS is used, for the first time, to permanently bond the flexible substrate to a Si wafer. The strength of the bond is further enhanced using the Dow Corning 92-023 adhesion promoter. This makes it possible to fabricate a wide range of MEMS devices on the flexible substrates, using traditional processing equipment. Due to the nature of the bond, the bonded substrates can be processed for temperatures up to 200°C. Areas of the Si wafer and PDMS interlayer are etched to form free-floating membranes. This opens the possibility of employing various devices on thin membranes, thus leading to more compact multi-functional systems on flexible substrates. The substrate maintains overall flexibility while the support structures provide mechanical support to the MEMS devices.

The adaptation of each fabrication process step to handle the bonded substrates has been documented. Modified techniques for lift-off using Parafilm M and spin-track have been presented. Custom recipes for etching the Si substrates and PDMS have been developed. The key advantage of the proposed fabrication technique is that it allows easy

recovery of devices fabricated on flexible substrates. Unlike the currently available techniques, the free-floating membrane structure eliminates the need to de-bond the flexible substrates at the end of fabrication, thus resulting in higher yields, low cost of production and a robust package for the MEMS devices. Using this design, devices can be fabricated on a free-floating flexible membrane with very little modifications to the traditional processing steps.

5.2 Future Work

For future work, the Kapton substrate thermal expansion and interlayer stresses could be characterized in detail. This will enable the designer to compensate for geometry changes during fabrication by varying the size of masks to improve alignment and reduce minimum feature size. Additionally, this information may be used to determine the operating temperature range of MEMS devices on Kapton substrates. The electrical properties of the Kapton substrate could be characterized after being subjected to the different fabrication process steps and temperature cycling. The etch recipes for Si substrate and PDMS can be characterized and modified to achieve higher etch rates. A combination of wet and dry etches could also be used to further enhance the etch profiles and achieve a better anisotropic etch. The MEMS fabrication process currently uses semiconductor fabrication equipment which limits the substrate dimensions to a 4 inch wafer size. Over the longer-term, converting the fabrication procedure to a large-area roll-to-roll process would greatly reduce cost and produce large-area structures that would lead to new applications.

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Appendix A

Process Flow for Temporarily Bonding Kapton to the Si Substrate Using PDMS

Handle Wafer:

Diameter: 100 mm

Orientation: <100>

Thickness: $525\ \mu\text{m} \pm 25\ \mu\text{m}$

Type: P

Dopant: Boron

Kapton Sheets:

Thickness: $25.4\ \mu\text{m}$ (1 Mil: 0.001")

1. Handle Wafer: Piranha Clean

- Tool: Piranha Tank
Temperature: $125^\circ \pm 2^\circ\text{C}$
Solution: 1:9 $\text{H}_2\text{O}_2:\text{H}_2\text{SO}_4$
Time: 10 min
- Dump Rinse Cycles: 4
Tool: 100:1 HF Tank
Solution: 100:1 $\text{H}_2\text{O}:\text{HF}$
Time: 30 s
- Dump Rinse Cycles: 4
- Spin-Rinse-Dry

2. PDMS Coating

2a. Mix PDMS

1:10 Solution

Curing Agent: 0.7g /1 wafer

Base: 7.0g /1 wafer

2b. De-gas PDMS

Time: 45 min

2c. PDMS Application

- Tool: Solitec
- Spread Time: 10 s Spread Speed: 500 rpm
- Acceleration: Set on 0 (40 krpm)
- Spin Time: 30 s Spin Speed: 3000 rpm

NOTES:

- Dispense the PDMS directly from the petri dish or a small glass beaker
- Wipe the bottom surface of the wafer clean using a wipe wet with acetone
- Place the coated wafers in closed containers until the cure process

2d. PDMS Cure

- Tool: Oven Time: 1 hr Temperature: $100^{\circ} \pm 2^{\circ} \text{ C}$

3. Kapton Sheet Preparation

3a. Cut the Kapton Sheets

Cut the kapton sheets into 6" x 6" squares

3b. Clean the Kapton Sheets

Solvent: Acetone Time: 5 min

Solvent: Isopropanol Time: 1 min

3c. Kapton Sheet Dehydration Bake

- Tool: Blue M Oven Time: 20 min Temperature: $120^{\circ} \pm 2^{\circ} \text{ C}$

4. Oxygen Ash

Tool: Barrel Asher

Time: 120 s

Power: 400 W

Pressure: 200 mT

5. Bond and Trim the Kapton

5a. Bond the Kapton

NOTES:

Make sure the Kapton and wafer bond without any air bubbles

5b. Trim Kapton

Trim along the wafer edge with the scissors

6. Post Bond Cure

Tool: Blue M Oven Time: 2 hrs Temperature: 100°C

7. Photolithography 1

7a. Standard OCG Photoresist Application

Process: Coat	Target Thickness: 7300 Å	
Process: Softbake	Tool: Oven	Time: 30 min
	Temperature: $98.5^{\circ} \pm 1.5^{\circ}$ C	
Process: Flood Expose		Time: 4 s
Process: Softbake	Tool: Oven	Time: 30 min
	Temperature: $98.5^{\circ} \pm 1.5^{\circ}$ C	

NOTES:

Do not allow the bake temperatures to exceed a maximum of 100° C

7b. Standard 1813 Photolithography

Process: Coat	Target Thickness: $12,500 \pm 200$ Å	
Oven Softbake	Time: 30 min	Temperature: $98.5^{\circ} \pm 1.5^{\circ}$ C
Process: Exposure		
Process: Develop		

8: Evaporate Metal 1

Tool: E-Beam

9. Lift-off

Standard Acetone / IPA Lift-off

Tools: Ultrasonic Tank

- **Acetone** Time: **(TBD according to pattern & thickness)**

Apply ultrasonic agitation by holding the beaker in the ultrasonic tank

Spray rinse with IPA

Filter the used acetone after every use to remove metal for recycling

- **IPA** Time: ~ 1.5 min

Apply ultrasonic agitation by holding the beaker in the ultrasonic tank

Spray rinse with IPA

NOTES:

DO NOT USE WATER

Blow dry with nitrogen

Appendix B

Process Flow for Permanently Bonding Kapton to the Si Substrate Using PDMS

Handle Wafer:

Diameter: 100 mm

Orientation: <100>

Thickness: $525\ \mu\text{m} \pm 25\ \mu\text{m}$

Type: P

Dopant: Boron

Kapton Sheets:

Thickness: $25.4\ \mu\text{m}$ (1 Mil: 0.001")

1. Handle Wafer: Piranha Clean

- Tool: Piranha Tank
Temperature: $125^\circ \pm 2^\circ\text{C}$
Solution: 1:9 $\text{H}_2\text{O}_2:\text{H}_2\text{SO}_4$
Time: 10 min
- Dump Rinse Cycles: 4
Tool: 100:1 HF Tank
Solution: 100:1 $\text{H}_2\text{O}:\text{HF}$
Time: 30 s
- Dump Rinse Cycles: 4
- Spin-Rinse-Dry

2. PDMS Coating

2a. Mix PDMS

1:10 Solution

Curing Agent: 0.7g /1 wafer

Base: 7.0g /1 wafer

2b. De-gas PDMS

Time: 45 min

2c. PDMS Application

- Tool: Solitec
- Spread Time: 10 s Spread Speed: 500 rpm
- Acceleration: Set on 0 (40 krpm)
- Spin Time: 30 s Spin Speed: 3000 rpm

NOTES:

- Dispense the PDMS directly from the petri dish or a small glass beaker
- Wipe the bottom surface of the wafer clean using a wipe wet with acetone
- Place the coated wafers in closed containers until the cure process

3. Kapton Sheet Preparation

3a. Cut the Kapton Sheets

Cut the kapton sheets into 6'' x 6'' squares

3b. Clean the Kapton Sheets

Solvent: Acetone Time: 5 min

Solvent: Isopropanol Time: 1 min

3c. Kapton Sheet Dehydration Bake

- Tool: Oven Time: 20 min Temperature: $120^{\circ} \pm 2^{\circ} \text{ C}$

4. Application of the adhesion promoter

Adhesion promoter: Dow Corning 92-023

Cure Time: 120 min

NOTES:

- Apply a very thin layer of the adhesion promoter by using a wipe

5. Bond and Trim the Kapton

5a. Bond the Kapton

NOTES:

Make sure the Kapton and wafer bond without any air bubbles

5b. Trim Kapton

Trim along the wafer edge with the scissors

6. Post Bond Cure

Time: 24 hrs Temperature: Room temperature

7. Photolithography 1

7a. Standard OCG Photoresist Application

Process: Coat	Target Thickness: 7300 Å	
Process: Softbake	Tool: Hotplate	Temperature: 115° C
Process: Flood Expose	Time: 4 s	
Process: Softbake	Tool: Oven	Time: 30 min
	Temperature: 98.5° ± 1.5° C	

7b. Standard 1813 Photolithography

Process: Coat	Target Thickness: 12,500 ± 200 Å
Process: Softbake	Temperature: 115° C
Process: Exposure	
Process: Develop	

8: Evaporate Metal 1

Tool: E-Beam

9. Lift-off

Standard Acetone / IPA Lift-off

Tools: Spin Lift-off Track

- **Acetone** Time: (TBD according to pattern & thickness)
- **IPA** Time: ~ 1.5 min

Spray rinse with IPA

NOTES:

DO NOT USE WATER

Blow dry with nitrogen

10. Front Side Photoresist Protection

Standard 1827 Photolithography

Process: Coat Target Thickness: 29,300 Å ± 500 Å

Process: Softbake Tool: Hotplate Time: 2 min

Temperature: $115^{\circ} \pm 2^{\circ}\text{C}$

11. Back Side Patterning

AZ 9260

Process: Dehydration Bake Tool: Blue M Oven

Temperature: $125^{\circ} \pm 2^{\circ} \text{ C}$ Time: 30 min

Process: Dispense AZ9260 Target Thickness: 10 μm

Tool: Solitec Spin Coater Spread: 4 s @ 300 rpm

Spin: 30 s @ 2000 rpm

Sit for 15 min in an enclosed container

Process: Softbake Tool: Oven

Temperature: $95^{\circ} \pm 2^{\circ} \text{ C}$ Time: 60 min

12. Buffered Oxide Etch

Tool: Buffered HF Tank Time: 12 min

13. DRIE of the Si Substrate

13a. Bond to Carrier Wafer

Material: Crystalbond 555

Place the carrier wafer on a hot plate at 95°C.

Put 1g/inch of Crystalbond on the carrier wafer.

Place the substrate to be bonded on the carrier wafer and out it in the vacuum bell for 5 min.

13b. DRIE

Tool: STS Pegasus Recipe: Refer Appendix C Time: 40 min

13c. De-bond the Carrier Wafer

Place the bonded pair on a hot plate at 100 (+/- 2)°C.

Slide the bonded substrate once the Crystalbond is melted.

Rinse the substrate in acetone and IPA followed with a rinse in DI water until the Crystalbond completely disappears.

14. Buffered Oxide Etch

Tool: Buffered HF Tank Time: 12 min

15. PDMS Etch

Tool: LAM Drytek RIE Recipe: Refer Appendix D Time: 2 hrs

Appendix C

Recipe Used for DRIE of the Si substrates

Following are the parameters of the recipe used for the etch

1. General

Generator Connection Mode – Platen LF

Platen Position – Up

Ramping – Disabled

Stabilization – Enabled

Stabilization time – 15 sec

Switching – Enabled

Start phase – Dep

End phase – Etch

Dep cycle time – 4 sec

Etch cycle time – 6.5 sec

2. Pressure

a. Delay Pressure

Item Dep		Mode	Etch	Mode
Thottle	100	Manual	100	Manual
Time	0	N/A	0	N/A

b. Boost Pressure

Item Dep		Mode	Etch	Mode
Thottle	100	Auto	100	Auto
Time	0	N/A	0	N/A

c. Main Pressure

Item Dep		Mode	Etch	Mode
Thottle	25	Auto	100	Auto
Overrun Time	0	N/A	0	N/A

3. Gases

Gases Enabled	Enabled	Dep Flow (sccm)	Etch Flow (sccm)
C ₄ F ₆	Yes	200	0
SF ₆	Yes	0	600
O ₂	Yes	0	60
Ar	No	0	0

4. Generators

Item Enabled	Enabled	Dep Power	Etch Power
13.56 MHz Coil	Yes	2000	4000
13.56 MHz Platen	No	0	0
380 KHz Platen	Yes	0	50

5. Pulse Generators

Item	Dep Duty Cycle	Etch Duty Cycle
Lf Pulse Generator	0	80

6. Matching

Item	Enabled	Dep Mode	Dep Load	Dep Time
Coil Matching Unit	Yes	Full Auto	35	50
Platen Matching Unit	Yes	Manual	37.3	53.1

Item	Enabled	Etch Mode	Etch Load	Etch Time
Coil Matching Unit	Yes	Full Auto	35	50
Platen Matching Unit	Yes	Full Auto	37.3	53.1

7. Temperature

Zone	Enabled	Control Mode	Temperature	Power
Platen Chiller	Yes	Auto	10	N/A
Inner Heater	Yes	Auto	140	N/A
Chamber Heater	Yes	Auto	120	N/A
Magnetic Confinement Heater	Yes	Auto	120	N/A
Plenum Heater	Yes	Auto	120	N/A

8. BGC

Backside Cooling – Enabled

Substrate Clamping – Required

Pressure – 10,000 mTorr

Pressure in Hold – 10,000 mTorr

9. Electromagnet

Outer EM Coil – Disabled

Inner EM Coil – Disabled

Appendix D

Recipe Used for PDMS Etching

CHF_3 – 75sccm

O_2 – 25sccm

Pressure - 47 mTorr

Power - 300 W

Etch rate - 12 μm /hour