IN VIVO RF POWERING FOR
ADVANCED BIOLOGICAL RESEARCH

by

MARK DAVID ZIMMERMAN

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Thesis Adviser: Professor Darrin Young

Department of Electrical Engineering and Computer Science

CASE WESTERN RESERVE UNIVERSITY

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In Vivo RF Powering For
Advanced Biological Research

Abstract

by

MARK ZIMMERMAN

A miniature, implantable, remote RF powering system for a small, un-tethered laboratory animal inside a cage is proposed. The proposed implantable device exhibits dimensions 6 mm x 6 mm x 2 mm and a mass of 100 mg including bio-compatible silicone coating. The external system consists of a Class-E power amplifier driving a tuned 15 cm x 25 cm coil. The implant device includes integrated “capacitor-free” RF→DC and power control circuitry. The full system provides 2 V V_{DD} at up to 1 mA to implant electronics with < 200 μ V DC variation, < 1 mV total RMS noise, and < 25 mV_{pp} 4 MHz ripple and a 3 V supply to CMOS switches over a 10 cm x 20 cm operating region with an implant tilt angle of up to 60°. Additionally, an intelligent power control system is proposed that would reduce external system power consumption and cage temperature increase.

CHAPTER 1: INTRODUCTION

1.1 *Motivation*

Advanced biomedical research often includes identification of genetic variation susceptibility to diseases—such as hypertension, obesity, epilepsy, and cancers—and the ongoing search for new treatments and cures. Researchers often require extensive real-time biological information such as blood pressure, body temperature, activity, and biopotential signals, over long periods of time from a living test subject. The method used to acquire this data, however, must not interfere with the subject’s behavior or physiology. To gather this data, long-lifetime bio-sensing implant systems are used for the advancement of biomedical research [1].

Currently, laboratory mice are highly desirable as a test subject due to its high degree of genetic and physiological homology with human beings. However, the small size and weight of a mouse means that typical pacemaker-sized monitoring devices—comparable in size to a mouse—cannot be used. Furthermore, “backpack” systems or systems that tether the mouse to an external power supply cause alterations in a mouse’s behavior, thus distorting the biological data. An implanted battery is also unfeasible due to the large size and mass and limited lifetime of a battery—a typical coin-cell battery has a lifetime of only ~100 mAh.

Current commercial products utilize RF powering to supply the implant system with the necessary power. RF powering systems have unlimited lifetimes and can operate as long as power is coupled in from an external source. These products, though, rely on bulky discrete architectures involving separate sensors, discrete components, and

multiple processing IC's on a circuit board. This discrete architecture occupies significant volume and requires high levels of power for sustained operation. RF powering is generally highly inefficient, and thus large implanted coils and heavy ferrite cores are also necessary to meet the high power needs of discrete architectures. These coils and cores further increase the size and weight of the implanted system, resulting in a final product exhibiting a mass of up to 20% of a subject mouse's body mass. Such a large implant and the related surgical procedures cause significant post implant trauma in addition to other physiological and behavioral changes. Over the long term, such implanted devices and the related trauma distort natural biological signals, reducing the reliability and confidence of experiments.

As a result, a miniaturized, implantable, wirelessly powered bio-monitoring system is desirable for advanced biological research. Integrating the powering, signal processing, and data transmission electronics into a single microfabricated circuit results in a distinct improvement in system size and system power consumption. The sensors themselves can also be microfabricated and integrated using MEMS sensors [2, 3] or other technologies. Optimized circuit design, especially with respect to the RF to DC electronics, can eliminate the need for off-chip components, further reducing the size and system parasitics. The low power requirements of the system allow for a much smaller implanted RF coil without a heavy ferrite core to be used to receive wireless power and pass it to the integrated microsystem.

In classical RF powering designs [4, 5], the relative position of the internal coil is fixed with respect to the external coil. This architecture yields a fairly constant inductive coupling factor, giving a fairly steady output. The case of an implant in an un-tethered

laboratory animal differs from these typical designs in that the inductive coupling factor, and thus the power coupled into the implant, varies widely over the operating region as the internal coil tilts and changes position with respect to the fixed external coil. Additionally, due to the considerable current through the external coil, a localized temperature increase occurs over the operating region due to the ohmic heating of the external coil. This temperature increase is of concern, as environmental changes could cause behavioral or physiological changes in the mouse. Additionally, there is a many-fold difference between the maximum and minimum power coupled to the implant over such a large operating region. Significant system optimization is therefore necessary to achieve the highest possible coupling efficiency and coupling uniformity over the operating region, and to design integrated RF to DC electronics that prevent power variations from damaging on-chip components or distorting sensitive bio-signals.

Traditional power controls operate by “throwing away” excess received power not needed by the implant system. In other words, significantly more power than necessary is consumed by the external system and supplied to the implant when the implant is in a moderate or high coupling region. An adaptive, intelligent power control system that limits the power consumed by the external amplifier and supplied to the external coil based on the needs of the implant system is, however, more efficient. This power control method reduces the total power consumed by the system, essential for portable applications. The reduced current in the external coil also reduces the corresponding cage floor heating. An adaptive power control loop must be simple and efficient, though, lest it consume additional power and have the opposite effect on the overall system. Such a simple, efficient, adaptive power control system is discussed in this work.

1.2 Thesis Outline

Chapter 2 of the thesis focuses on the discrete (non-integrated) components of the remote RF powering system. It investigates the architecture then presents the analysis and optimization process. Chapter 3 describes the on-chip RF-DC converter, and all relevant components thereof. The chapter analyzes both coarse and fine power control schemes. Chapter 4 outlines testing procedures and then presents and discusses measurement results. Finally, Chapter 5 presents the conclusion and future work of the research.

CHAPTER 2: REMOTE RF POWERING SYSTEM

2.1 Chapter Overview

This chapter presents the architecture and investigates the design of the wireless RF powering system. Focus in this chapter will be given to the off-chip devices, such as the inductor coils and the power amplifier, while the on-chip components will be presented in Chapter 3. First, the overall wireless powering architecture will be presented, followed by a more in-depth description of each critical component. Following that, the design and optimization process of the wireless powering system will be discussed.

2.2 RF Powering System Architecture

Figure 2.1: Overall wireless RF powering system architecture

Figure 2.1 presents the overall system architecture. The *in vivo* microsystem, implanted in the abdomen of the mouse, is wrapped with a small wire coil, which is

inductively coupled to an external coil loop exhibiting dimensions slightly larger than the cage. The external coil chosen for this study is 25 cm x 15 cm. The cage size is derived later in this work and is 20 cm x 10 cm, which is adequate for housing a small laboratory animal. The internal coil maintains approximately 1 cm vertical separation from the external coil. Radio-frequency (RF) power is transmitted to the internal coil from the external coil, at which point the received RF power is rectified, filtered, and regulated, and then passed on to the bio-sensing and telemetry electronics. The power amplifier driving the external coil is not shown in the figure for simplicity. The following subsections will overview the four major elements of this design: the external coil, the internal coil, the power amplifier, and a linear model for inductive coupling. Non-linear concerns such as rectification will be described in Chapter 3.

2.2.1 Inductive Coupling

A wireless powering system is based upon the transmission of an AC signal between two coupled inductors, as shown in Figure 2.2. In this figure, Z_1 and Z_2 represent the total loading impedance for each inductor, including the impedance of the inductor itself.

Figure 2.2: Coupled inductors with loading impedances

The fact that the inductors are coupled means that there is a mutual inductance, M , between the two inductors, as the magnetic field produced by one inductor affects the

magnetic field of the other and vice versa. Due to this mutual inductance, an alternating current through one inductor induces a corresponding AC voltage in the second inductor, shown in Figure 2.3.

Figure 2.3: Coupled inductors with induced voltage source

This induced voltage, V_{ind} , can be expressed as

$$V_{ind} = -j\omega M I_p, \quad (2.1)$$

where ω is the operating frequency in radians/second, M is the mutual inductance between the two inductors, and I_p is the current through the first (primary) inductor. The factor of $-j$ indicates a 90° phase lag from I_p .

This induced voltage produces a current, I_s , in the secondary coil given by

$$I_s = \frac{V_{ind}}{Z_2}. \quad (2.2)$$

The energy expended to induce this current comes from the primary coil, and appears in the form of an additional impedance, Z_{ref} —the reflected impedance—in series with Z_1 .

This impedance is shown in Figure 2.4 and can be expressed as

$$Z_{ref} = \frac{\omega^2 M^2}{Z_2}. \quad (2.3)$$

Figure 2.4: Coupled inductors with reflected impedance

The efficiency of such a coupled inductor system can be improved by tuning both inductors to the same frequency. Tuning the inductors involves adding a capacitance to cancel the imaginary portion of the inductor's impedance at the desired operating frequency, leaving only a real impedance due to the resistance of the non-ideal inductors and capacitors, called the equivalent series resistance or ESR. The appropriate capacitance, C , necessary to resonate with an inductance, L , at a frequency of ω_0 is given by

$$\omega_0 = \frac{1}{\sqrt{LC}}. \quad (2.4)$$

The tuned circuit is shown in Figure 2.5 with the primary and secondary ESR modeled by R_1 and R_2 . The primary coil is serially tuned (placing a capacitor in series with the inductor) by using C_1 , to reduce the magnitude of Z_1 and thus increasing the primary current. The secondary coil has undergone a partial serial to parallel conversion in Figure 2.5, replacing the series impedance Z_2 with R_{ACload} and R_2 , which represent the equivalent AC loading of the implant microsystem and the secondary coil ESR, respectively. The secondary coil is parallel tuned (placing a capacitor in parallel with the inductor) by using C_2 , which decreases the magnitude of the series Z_2 and thus increases the secondary current that flows through the load.

Figure 2.5: Coupled inductors illustrating individual components (Note: Z_{ref} not shown)

In order to calculate Z_2 presented earlier, it is necessary to convert the R_{ACload} that is in parallel with the L_2 - C_2 resonant tank to a resistance in series with R_2 . This equivalent resistance, R_{series} , is the result of a parallel to serial conversion involving C_2 and R_{ACload} and can be calculated as follows:

$$R_{series} = \frac{R_{ACload}}{(Q_{C2}^2 + 1)} \approx \frac{R_{ACload}}{Q_{C2}^2} = \frac{R_{ACload}}{(\omega_0 C_2 R_{ACload})^2} = \frac{1}{(\omega_0 C_2)^2 R_{ACload}} = \frac{(\omega_0 L_2)^2}{R_{ACload}}, \quad (2.5)$$

where ω_0 is the resonant frequency from (2.4), and Q_{C2} is the quality factor of the capacitor, $\omega_0 C_2 R_{ACload}$. Equation (2.4) is used to transform capacitance into inductance.

As a result, an equation for Z_2 can be stated:

$$Z_2 = R_2 + R_{series} = \frac{(\omega_0 L_2)^2}{R_{ACload}} + R_2. \quad (2.6)$$

From (2.1), (2.2), and (2.6), one can calculate the secondary current I_s :

$$I_s = \frac{V_{ind}}{Z_2} = \frac{V_{ind}}{\frac{(\omega_0 L_2)^2}{R_{ACload}} + R_2} = \frac{j\omega_0 M I_p}{\frac{(\omega_0 L_2)^2}{R_{ACload}} + R_2}. \quad (2.7)$$

Furthermore, from (2.3) and (2.6), the current in the primary inductor coil, I_p , can be calculated:

$$I_p = \frac{V_{in}}{R_1 + Z_{ref}} = \frac{V_{in}}{R_1 + \frac{(\omega_0 M)^2}{Z_2}} = \frac{V_{in}}{R_1 + \frac{(\omega_0 M)^2}{R_2 + \frac{(\omega_0 L_2)^2}{R_{ACload}}}} = \frac{V_{in}}{R_1 + \frac{R_{ACload}(\omega_0 M)^2}{R_2 R_{ACload} + (\omega_0 L_2)^2}}. \quad (2.8)$$

Combining (2.7) and (2.8), the secondary current can be expressed as:

$$\begin{aligned} I_s &= \frac{-j\omega_0 M}{\frac{(\omega_0 L_2)^2}{R_{ACload}} + R_2} * \frac{V_{in}}{R_1 + \frac{R_{ACload}(\omega_0 M)^2}{R_2 R_{ACload} + (\omega_0 L_2)^2}} \\ &= \frac{-j\omega_0 M V_{in}}{R_1 R_2 + R_1 \frac{(\omega_0 L_2)^2}{R_{ACload}} + \frac{(\omega_0 L_2)^2 (\omega_0 M)^2}{R_2 R_{ACload} + (\omega_0 L_2)^2} + \frac{R_2 R_{ACload} (\omega_0 M)^2}{R_2 R_{ACload} + (\omega_0 L_2)^2}} \\ &= \frac{-j\omega_0 M V_{in}}{R_1 R_2 + R_1 \frac{(\omega_0 L_2)^2}{R_{ACload}} + (\omega_0 M)^2} \end{aligned} \quad (2.9)$$

This imaginary current, multiplied by the imaginary impedance of the secondary inductor ($j\omega_0 L_2$), results in real output voltage across R_{ACload} . Multiplying (2.9) by this impedance yields

$$V_{out} = \frac{\omega_0^2 M L_2 V_{in}}{R_1 R_2 + R_1 \frac{(\omega_0 L_2)^2}{R_{ACload}} + (\omega_0 M)^2}. \quad (2.10)$$

Thus,

$$A_v = \frac{V_{out}}{V_{in}} = \frac{\omega_0^2 M L_2}{R_1 R_2 + R_1 \frac{(\omega_0 L_2)^2}{R_{ACload}} + (\omega_0 M)^2}. \quad (2.11)$$

This gain equation, equation (2.11), is essential for the design and characterization of an RF powering system.

2.2.2 External Coil

For the proposed RF powering system, it is desirable to reduce the ratio of maximum to minimum coupling—the coupling variation—while still maintaining a coupling sufficient to operate the system, as will be analyzed in greater depth in Section 2.3. To this end, multiple external coil architectures were investigated for the role of external inductor in this system. All external coils presented here were etched from copper-clad prototyping boards in order to achieve uniform and reproducible inductors.

Figure 2.6: Grid powering architecture

The first architecture considered called for an array of square external coils (an array of L_I coils) each 5 cm x 5 cm in size, as shown in Figure 2.6 [6]. In this architecture, the position of the mouse would be tracked and the coil or coils immediately under the mouse would be powered individually. This design provides strong inductive coupling, measured as a high mutual inductance, between external and internal coils. However, the design suffers from certain limitations. First, complex control electronics would be necessary to detect mouse position and selectively power the external coils. Second, the presence of powered inductor coils directly underneath the mouse causes significant cage

floor heating in the vicinity of the mouse. Thirdly, and most importantly, drastic coupling variation occurs at coil boundaries. This is due to the constructive or destructive interference of magnetic fields produced by individual coils.

As a result, the decision was made to investigate a large, single external inductor coil as shown in Figure 2.1. The large coil architecture moves the majority of the coupling variation and temperature increase to the edges of the coil and thus outside the operating region. However, the low coupling between the coils in this architecture reduces efficiency and thus requires significant system optimization to achieve a feasible RF powering system. This optimization process will be described in Section 2.3.

A 3-dimensional coil architecture was also tested. This coil, with the same footprint as the large coil, is wound to varying heights from 2 to 5 cm up the side of the cage. This method offers, at best, about a 30 % improvement in coupling, and also somewhat suppresses the effect of dead zones and peak zones, which will be described in the following sections. However, a 3-dimensional coil would greatly increase the system manufacturing complexity and cost. Given the marginal improvement in coupling, it was decided to pursue the flat, 2-dimensional, large coil architecture as shown in Figure 2.1.

2.2.3 Class-E Amplifier

Figure 2.7: Class-E amplifier schematic

The Class-E amplifier, diagrammed in Figure 2.7, was chosen as the power amplifier to drive the external coil inductor due to its near-zero output resistance and thus near-zero power loss. The primary source of output resistance seen by the resonant network is the channel resistance of the switching transistor, M_1 , and the ESR of L_{choke} . The device chosen for M_1 , the IRF 510 power transistor from International Rectifier, provides a measured channel resistance (r_{DS}) of $0.37 \, \Omega$. The amplifier achieves near-zero power loss by operating in what is known as Zero Voltage Switching (ZVS) mode [7]. When component values are properly chosen, the action of the resonant network and shunt capacitor causes the voltage at the drain of M_1 to be brought to zero immediately before V_{clock} goes high and M_1 turns on. This prevents a wasteful current spike through M_1 at turn-on, significantly increasing efficiency.

Figure 2.8: Measured ZVS Class-E amplifier drain waveform and corresponding clock waveform

Figure 2.8 shows the measured drain voltage and clock waveforms of a constructed and properly tuned Class-E amplifier. Minimal current is drawn through the transistor in this setup, thus minimizing power loss from the switching transistor. In testing, amplifier efficiencies—defined as the ratio of power transferred to R_L versus power drawn from the supply—of up to 95% have been achieved. The efficiency of the amplifier increases with increased R_L , as can be seen by investigating the amplifier from the perspective of a simple resistive divider. Increased R_L also decreases the voltage gain, as seen in equation (2.11), therefore careful analysis is needed to find optimal component values. This analysis is conducted in section 2.3.2.

2.2.4 Internal Coil

Current commercial devices designed for long-term *in vivo* bio-signals monitoring often require large internal coils with heavy ferrite cores in order to couple sufficient power into the implant electronics. One such device, the VitalView by Minimitter [8], is

used here for comparison. The full device (excepting EKG electrodes, pictured in Figure 2.9) is contained within a plastic cylinder that is 26 mm long by 5 mm in diameter. It utilizes an inductive coil and ferrite core with a mass of 450 mg. The total system mass is approximately 2.0 g, which is about 10-20 % of total body mass for a mouse. The device is also shown in Figure 2.10, implanted into a mouse for size comparison. The large volume and mass of the system is undesirable, as described previously.

Figure 2.9: VitalView implant device, showing inductor coil, ferrite core, and implant electronics

Figure 2.10: X-ray photograph of a mouse with an implanted VitalView device

In the proposed system, low power integrated circuits and MEMS sensors are utilized to minimize implant power dissipation as well as to reduce size and mass. Wrapping an RF coil around and in the same plane as the silicon IC maximizes the size and shape advantages of using an integrated microsystem by minimizing any extra volume occupied by the RF coil.

Figure 2.11: Internal coil and on-chip rectifier attached to prototyping board

Figure 2.11 shows an RF coil wrapped around an integrated circuit. The coil and IC are placed on a circuit board that is used for prototyping purposes, only, and would not be present in the final system design. The integrated circuit shown in the photograph does not contain the full functionality of a final bio-sensing microsystem, but exhibits the same size and shape as the expected final design. As a result of these system improvements, including integrated circuits and sensors, elimination of a ferrite core, and planar configuration, the prototype device exhibits a 20x decrease in mass and a 30x decrease in volume over the VitalView and other similar commercial products.

External RF power is coupled to the planar secondary coil by magnetic field lines perpendicular to the internal coil plane. The large external coil produces a vertical magnetic field (perpendicular to the plane of the external coil) over the majority of its area, thus calling for the planar coil to be implanted in the abdomen of a laboratory animal, close to and parallel to the external coil. This means, however, that less power is coupled to the internal coil when the animal stands up and the magnetic field is no longer perpendicular to the internal coil plane. “Dead zones”—spatial regions and/or orientations where the two coils have near-zero coupling due to the alignment of the magnetic field lines—are unavoidable in this un-tethered environment. However, steps

can be taken to minimize the impact on system performance, as will be described in the following section.

2.3 Analysis and Optimization of RF Powering System

There are two goals of the RF powering system analysis and optimization process. The first goal is to determine the optimal operating region given a large, single external coil. This optimal operating region should allow for sufficient inductive coupling to power the implant system for up to a 60° internal coil tilt, but at the same time should prevent large voltage spikes due to overly high coupling and should not excessively restrict the cage area. The powering of the implant up to a 60° internal coil tilt ensures that the bio-signals will not be lost for an extended period of time, as a mouse rarely maintains a tilting angle of greater than 60° for an extended period of time. The second goal is to find the most efficient operating point—defined as the highest ratio of power transferred to R_{ACload} versus power consumed by the Class-E amplifier—for the system as a function of number of turns in the internal coil, number of turns in the external coil, and operating frequency. The efficiency of the amplifier and the efficiency of the coupling between the coils are analyzed separately and then combined to obtain the most efficient operating point.

2.3.1 Operating Region Optimization

The goal of optimization of the operating region is to define an operating region that reduces the coupling variation without overly constricting the roaming area of the laboratory mouse. This is motivated by the problems caused by overpowering of the implant in peak zones, as well as the near-complete loss of power coupling that occurs in dead zones. Significant implant overpowering can cause gate oxide breakdown and pn

junction breakdown. Integrated limiting circuits can be used to prevent this breakdown, but high levels of overpowering would require large currents to be handled by the limiting and powering circuitry, thus requiring large devices and metal traces which occupy a significant amount of silicon area and also generate undesirable waste heat in the implant. As described before, it is also desirable to define a coupling region free of dead zones for all tilting angles up to 60° to prevent loss of bio-signals monitoring for an extended period of time. Though it is possible to vary the input power to provide the required power in either dead zones or peak zones, adjusting the power based upon one region only exacerbates the problems from the other. Therefore, an overall reduction in output variation is desired. This was achieved by analyzing the inductive coupling over the operating region, as described in the following section.

The coupling constant, k , is a factor that defines the strength of the magnetic field interaction between the two coils. The mutual inductance, M , between the two inductors is dependent upon the inductances of both coils, L_1 and L_2 , as well as this coupling constant and can be determined as

$$M = k\sqrt{L_1 L_2} . \quad (2.12)$$

The coupling constant is dependent only upon the shape, size, and orientation of the coils. Being independent to the first order of component values, frequency, number of turns in coils (as long as the coil shape/size remains constant), etc., k is thus essential for simulation and prediction of system performance. Furthermore, combining (2.11) and (2.12), it can be seen that V_{out} is approximately proportional to the coupling constant k . Similarly, the power received by the internal coil, given a constant load and constant

input source, is proportional to the square of k . Therefore, to design a feasible, reliable coupling system, the ratio of maximum k to minimum k must be reduced.

A physical apparatus equivalent to the circuit in Figure 2.5 can readily be constructed. If the component values of the circuit are determined, measuring the output from a known source allows for the calculation of the mutual inductance by rearranging (2.11). From M , the coupling constant, k , can then be calculated from (2.12).

This approach was used to map the coupling constant over the entirety of the operating region at a variety of tilting angles. Key results are shown in the following figures, which plot the coupling constant k , indicated by a color, on a grid corresponding to the cage floor location in units of centimeters.

0 Degree Tilt

Figure 2.12: Measured coupling constant, 0° tilt

60-Degree x-Direction Tilt

Figure 2.13: Measured coupling constant, 60° x-direction tilt

60-Degree y-Direction Tilt

Figure 2.14: Measured coupling constant, 60° y-direction tilt

Here, the darkness of the shade of a region indicates the level of coupling. The grey shades indicate “good” levels of coupling, while indicates dead zones—areas with very little to no coupling. Conversely, the dark shades indicate high coupling regions, while black indicates peak zones—areas with excessively high coupling.

As can be seen from the plots, restricting the mouse to a region defined by a smaller rectangle 2.5 cm from the coil edge (shown by the light rectangles in the above figures) eliminates the peak coupling regions and guarantees appreciable coupling over the entire operating region for an internal coil tilt of 60° or less.

Without this operating region restriction, k varies from a minimum of about 0.0001 to a maximum of about 0.0055, a factor of 55 difference. This variation means that, if the implant system were to require an input power of 5 mW at the region of the lowest coupling, the power received by the secondary coil at the region of the highest coupling would be 15 W! With the smaller cage size, k varies from a minimum of 0.0008 to a maximum of 0.0034, exhibiting a factor of 4.25 difference—feasible for an implantable system and corresponding to a variation in input power of only a factor of 18.

2.3.2 Operating Point Optimization

For the purpose of this analysis, the “system efficiency”, η_s , is defined as the ratio of power received by R_{ACload} versus the power consumed by the external Class-E amplifier. This efficiency is the product of the efficiency of the Class-E amplifier, η_a , and the coupling efficiency, η_c . It is desirable to achieve the greatest possible efficiency to reduce the required implant size and the necessary input power, which also minimizes the increase of cage floor temperature.

The coupling efficiency, η_c , is defined, as per Figure 2.5, as the ratio of power received by R_{ACload} versus the power drawn from the input source V_{in} . The RMS power drawn from V_{in} for the frequency at which L_I and C_I are at resonance can be calculated by

$$P_{Vin} = \frac{V_{in}^2}{R_I \sqrt{2}}. \quad (2.13)$$

Similarly, the RMS power received by R_{ACload} can be calculated as

$$P_{out} = \frac{V_{out}^2}{R_{ACload} \sqrt{2}}. \quad (2.14)$$

Using (2.13) and (2.14) in tandem with (2.11), an expression for η_c can be derived:

$$\eta_c = \frac{\frac{V_{out}^2}{R_{ACload} \sqrt{2}}}{\frac{V_{in}^2}{R_I \sqrt{2}}} = A_v^2 \frac{R_I}{R_{ACload}} = \left(\frac{\omega^2 M L_2}{R_I R_2 + (\omega M)^2 + R_I \frac{(\omega L_2)^2}{R_{ACload}}} \right)^2 \frac{R_I}{R_{ACload}}. \quad (2.15)$$

Power losses from the Class-E amplifier can then be approximated by using equations from Kazimierczuk's and Czarkowski's Resonant Power Converters [7]. Adapting the terms for this particular situation yields the following expression for the efficiency of the amplifier, defined as the ratio of power received by the $L_I C_I R_I$ resonant network to power drawn from the V_{DD} supply

$$\eta_a = 1 - \frac{8r_{L-choke}}{(\pi^2 + 4)R_I} - \frac{(\pi^2 + 28)r_{DS}}{2(\pi^2 + 4)R_I} - \frac{(\pi^2 - 4)r_{C-shunt}}{2(\pi^2 + 4)R_I} - \frac{(\omega t_f)^2}{12}. \quad (2.16)$$

where $r_{L-choke}$ is the resistance of the choke inductor, r_{DS} is the drain resistance of the switching transistor, $r_{C-shunt}$ is the resistance of the shunt capacitor, and t_f is the fall time of the transistor. Of these terms, the second term dominates for frequencies under 10 MHz for an r_{DS} value of 0.37 Ω .

The overall system efficiency, η_s , is the product of the coupling efficiency η_c and the Class-E amplifier efficiency, η_a . The overall efficiency values were calculated for internal coils with 15, 20, 25, and 30 turns and external coils with 1, 2, 3, 4, and 5 turns over the operating frequency range of 1 MHz to 20 MHz. The calculations and accompanying measurements were carried out with the internal coil in the center of the external coil with 1 cm vertical separation and 0° tilt, corresponding to a k value of 0.0017. This measurement point was chosen for its reproducibility and relative insensitivity to slight offsets. Though the magnitude of η_s varies depending upon location, the optimum operating conditions that give the optimum η_s are valid for all locations. This is due to the fact that η_s is approximately proportional to k^2 , and that no other factors vary with changing location.

The exact efficiency values predicted by the above method are heavily dependent upon values such as the external coil ESR or the resistive losses of elements in the Class-E amplifier, such that a mismeasurement of a fraction of an ohm can significantly change the predicted value. As a result, these predictions were used to determine efficiency trends which were then tested with actual prototype measurements to obtain the optimal operating point. To obtain these measurements, an external coil and loaded internal coil were tuned to the same frequency, as shown in Figure 2.5. The external input source was replaced with the Class-E amplifier. The output AC voltage across the R_{ACload} was then measured for the concentric, 0° tilt configuration described previously. The efficiency was then calculated from the measurement as

$$\eta_s = \frac{V_{out-peak}^2}{V_{DD} I_{in} * 2R_{ACload}}, \quad (2.17)$$

where $V_{out-peak}$ is the peak voltage across R_{ACload} , V_{DD} is the Class-E supply voltage, and I_{in} is the Class-E amplifier supply current. The factor of two in the denominator comes from the conversion of peak (amplitude) voltage to RMS voltage.

Equation (2.15) suggests that efficiency should increase with increasing frequency. Conversely, the ESR of an inductor increases with frequency due to skin effect, causing the efficiency to decrease. Self resonance also limits the operation and efficiency of the inductor at increased frequencies. Therefore, it is expected to observe a peak efficiency frequency for each pair of inductors from the interplay of these two effects. Figure 2.15, Figure 2.16, and Figure 2.17 show the calculated system efficiency from (2.15) and (2.16) along with measured values for the 25, 20, and 15 turn internal coils, respectively. This behavior is seen for all inductor pairs, and the measurements follow the expected trends.

System Efficiency with N=25 Internal Coil

Figure 2.15: Predicted and measured system efficiency for 25-turn internal coil

System Efficiency with N=20 Internal Coil

Figure 2.16: Predicted and measured system efficiency for 20-turn internal coil

System Efficiency with N=15 Internal Coil

Figure 2.17: Predicted and measured system efficiency for 15-turn internal coil

The optimal operating condition (peak efficiency) was found to occur—as predicted—with the 20-turn internal coil and 4-turn external coil operated at 4 MHz, as seen in Figure 2.16. Under these operating conditions, component values are $L_1 = 13.2 \mu\text{H}$, $L_2 = 2.6 \mu\text{H}$, $R_1 = 7.0 \Omega$, and $R_2 = 2.5 \Omega$. These optimal operating conditions yield a measured efficiency of 0.078 % under an R_{ACload} of 820Ω (based on early expectations of the worst case R_{ACload}) when the internal coil is positioned 1 cm above the middle of external coil with 0° tilt. This efficiency is limited by the low k value of 0.0017, which limits the coupling efficiency η_c . It should be noted that, for the given coil sizes and load, the optimum operating frequency is near 4 MHz regardless of number of turns. The peak efficiency for any internal coil is within 25% of the overall peak efficiency, as long as a 4-turn external coil is used.

The value of R_{ACload} is defined by the current consumption of the implant device. Increasing the value of R_{ACload} by decreasing the current consumption generally results in an increase in efficiency, as expected from (2.15). The optimum operating point remains the same up to an R_{ACload} of $3.5 \text{ k}\Omega$ —corresponding to a load current of $400 \mu\text{A}$ —at which point the 3-turn external and 20-turn internal coil pair, operating at 6 MHz, provides slightly improved efficiency, as shown below in Figure 2.18. Further decreased current consumption increases the advantage of operating under these new conditions. The final implant is expected to consume more than $400 \mu\text{A}$, so the previously determined operating point (20-turn internal and 4-turn external coil pair operated at 4 MHz) will be used in order to give the system maximum efficiency under the worst case powering conditions.

System Efficiency with N=20 Internal Coil

Figure 2.18: Predicted and measured system efficiency for 20-turn internal coil and 400 μ A load

2.4 Summary

The architecture and discrete components of a remote RF powering system were introduced. A linear analysis of RF powering led to a defining gain equation. Using this equation, measurements were taken to determine the coupling constant k over the coil area and to determine an optimum operating region. The optimum operating region for the 15 cm x 25 cm external coil is a 10 cm x 20 cm located equidistant from coil edges. The system configuration that yields maximum system efficiency was determined to be a 4-turn external coil and 20-turn internal coil, both tuned at 4 MHz.

CHAPTER 3: INTEGRATED RF-DC CONVERTER

3.1 Overview

This chapter presents the architecture and investigates the design of the on-chip RF to DC converter, and addresses the integrated circuit portion of the RF powering system, as the off-chip components are presented in Chapter 2. First, the overall architecture of the RF to DC converter will be presented. Then, a more in-depth investigation will be carried out of the three major portions of the design. The rectifier, the regulators (fine power control), and the power control mechanisms (coarse power control) will be presented.

3.2 RF to DC Converter Architecture

The objective of the RF to DC converter is twofold. The first objective is to convert incoming RF power to a constant, regulated DC voltage to supply the bio-sensing, digital processing, and transceiver electronics. The resulting DC voltage must be resistant to changes in the received power to prevent undesirable alterations of the measured bio-signals. The second objective is to provide power control capability to prevent device breakdown from operation in high coupling regions. Sections 3.3 and 3.4 will focus on the first objective, while section 3.5 will focus on the second objective.

Traditional discrete-component RF to DC converters use a number of large value capacitors to provide the low-pass filtering characteristics necessary to produce a stable output supply. These capacitors—often on the order of nF to μ F in size—cannot be integrated into a system-on-a-chip due to the limited space available. Additional off-chip

components, on the other hand, increase the size of the system, introduce additional parasitics, and increase the manufacturing complexity. Though the current system requires an off-chip tuning capacitor and an off-chip inductor for data transmission, an RF to DC converter with fewer off-chip components has increased research value as other methods may be taken in the future to eliminate the other unrelated off-chip components. Therefore, for this design, efforts have been taken to design a largely “capacitor-free” RF to DC converter that does not require high capacitance, off-chip capacitors.

Figure 3.1 shows the general block diagram of the RF to DC converter. In this diagram, the input source V_{in} drives a current through L_1 , which induces an AC voltage and current in L_2 , as described in Section 2.2.1. The rectifier block then converts this AC voltage to a DC level with ripple. The magnitude of the DC voltage level out of the rectifier is dependent upon the mutual inductance, M , and thus the varying coupling constant k . The regulator block is supplied by the rectifier output and produces a constant V_{DD} supply with reduced ripple. V_{DD} is then used as the supply for the implant electronic system. As indicated in Figure 3.1, the rectifier block presents a loading of R_{ACload} to the internal coil. The elements used for coarse power control—the second objective—are not shown for simplicity as such an objective can be attained in various manners, as will be illustrated in Section 3.5. Many of the major design challenges for this system stem from the wide range of possible values for the mutual inductance M .

Figure 3.1: RF to DC converter overall block diagram

In order to reduce the necessary power draw from V_{in} and thus the cage floor temperature increase, efforts are made to reduce the power consumed by the implant electronics. Various design techniques can reduce the necessary current consumption of any of the bio-sensing components. Reducing V_{DD} , however, ensures reduced implant power consumption across the board.

For the chosen semiconductor process—the AMI 1.5 μm process offered through MOSIS—the implant electronics can be designed to operate from of a V_{DD} as low as 2 V. This level is a few hundred millivolts greater than the sum of the worst case (slow process) NMOS and PMOS thresholds, thus allowing sufficient headroom for standard CMOS design techniques.

Switched-capacitor circuits are to be designed in the signal processing electronics of the bio-sensors and require a higher voltage for proper operation, as follows. Figure 3.2 illustrates a typical CMOS switch used in switched capacitor-circuits. The switch is comprised of two transistors, one NMOS (top) and one PMOS (bottom). To turn on the switch, V_{DD} is applied to the gate of the NMOS transistor and 0 V is applied to the gate of the PMOS transistor. To turn off the switch, V_{DD} is applied to the PMOS gate and 0 V to the NMOS gate. When the switch is turned on as shown in Figure 3.2 and a signal is applied at V_i , the signal should be passed to V_o with minimal attenuation. If the signal is

near 0 V, the NMOS transistor exhibits a large V_{GS} and turns on, passing V_i to V_o . If the signal is near V_{DD} , the PMOS transistor exhibits a high $|V_{GS}|$ and turns on, again passing V_i to V_o . However, if V_{DD} is insufficiently high, it is possible to have a region where the signal is neither low enough to fully turn on the NMOS device nor high enough to fully turn on the PMOS device, presenting a large on-resistance to V_i . This problem is made worse by the fact that there is a significant V_{BS} for both transistors, increasing the thresholds and thus the voltage levels necessary to fully turn on the devices. For the AMI 1.5 μm process, it has been determined that the supply must be at least 2.6 V to allow for proper CMOS switch behavior even in worst-case situations. A supply level of 3 V was chosen in order to have a safety margin and to decrease CMOS switch on-resistance. A similar supply is also necessary to properly control the capacitance of the varactor used to tune the VCO which transmits digitized bio-signals data to an external receiver.

Figure 3.2: Typical CMOS switch (in “on” position) used in switched-capacitor circuits

Though some designs utilize a charge pump or similar device to generate these voltages, the charge pump introduces additional distortion to the supply voltage, which can distort sensitive bio-signals. This distortion occurs at a lower frequency and its harmonics in addition to the existing 4 MHz ripple. Also, a large filter capacitance is often necessary to provide a stable charge pump output supply. Furthermore, achieving a specific, fixed output voltage level independent of load or process parameters is difficult

for simple (small and efficient) implementations of a charge pump. (Voltage level shifting circuits can facilitate the conversion between 2 V digital controls and the CMOS switch signal. If the 3 V level were to vary from the designed value, more complicated level-shifting circuits would be necessary.)

Instead, a dual-regulator design has been used to provide separate 2 V and 3 V output supply levels. The 3 V output supplies low current, and thus consumes little power. In addition to providing a largely distortion-free output supply, this approach allows for other design optimizations as will be described throughout this chapter.

For the purposes of this discussion, the 2 V output supply will be called V_{DD} , and the 3 V output supply will be called V_{DD-3V} .

3.3 The Rectifier

The key element in a rectifier block is the diode, a semiconductor device that only allows current to flow in a single direction. The diode is used to pass only a certain portion of an AC input waveform, effectively producing a DC bias from the AC input.

3.3.1 Half-Wave Rectifier

Figure 3.3: Simple half-wave rectifier

Figure 3.3 illustrates a simple half-wave rectifier. In this design, the diode conducts when V_{in} is greater than V_{out} , depositing charge on C_{filter} . C_{filter} is then gradually discharged by the current through the load resistor R_{load} . C_{filter} and R_{load} act as a low pass

filter; therefore, if C_{filter} is sufficiently large, V_{out} appears as nearly a DC voltage. The magnitude of ripple that appears at V_{out} can be calculated by analyzing the discharging behavior of C_{filter} . Assuming a constant load current, I_{load} , the equation for the peak-to-peak ripple, V_r , for an input source operating at a frequency f (in Hz) is as follows:

$$V_r = \frac{I_{load}}{C_{filter}f}. \quad (3.1)$$

The half wave rectifier presents an equivalent AC load resistance, R_{ACload} , to the input source (or an LC tank). Based upon the R_{ACload} calculation in [4] and applying a correction factor for the diode drop-out voltage, this equivalent AC resistance can be calculated by

$$R_{ACload} = \frac{R_{load}}{2} \left(1 + \frac{V_{drop}}{V_{out}} \right), \quad (3.2)$$

where V_{drop} is the drop across the rectifier diode.

The half-wave rectifier does not lend itself well to the dual-regulator design, as only a single output at a single voltage level is produced. The rectifier output would need to be high enough to supply the V_{DD-3V} output ($V_{out} \sim 4.5$ V); however, this means that the 2 V V_{DD} could only be achieved by creating a large (2.5 V) step down across a transistor—an inefficient method that would consume extra power and diminish the power-saving advantage of the dual-regulator design.

3.3.2 Voltage-Doubler Rectifier

Figure 3.4: Voltage doubler overall schematic

The voltage doubler is a form of rectifier that produces multiple rectified output voltage levels [9]. The doubler is basically two half-wave rectifiers, one formed by D_1 and $C_{filter1}$, and the other by D_2 and $C_{filter2}$. The input voltage is applied between two floating points, rather than between the on-chip ground and an input, as was shown in Figure 3.3. The D_1 - $C_{filter1}$ rectifier captures the downswing of V_{in} , producing the rectified potential GND, which is $V_{in-peak} - V_{drop-D1}$ volts less than $V_{supply-L}$. The D_2 - $C_{filter2}$ rectifier captures the upswing of V_{in} , creating the rectified potential $V_{supply-H}$, which is $V_{in-peak} - V_{drop-D2}$ volts greater than $V_{supply-L}$. This dual-supply rectifier compliments the dual-regulator architecture by providing two supplies at different voltage levels without requiring a “drop-out” device to produce the lower level. As the bio-sensing electronics draw current from $V_{supply-L}$, the overall power savings can be approximated by the ratio of $V_{supply-L}$ to $V_{supply-H}$, as comparatively little current is drawn from $V_{supply-H}$.

In this design, the lowest potential, GND, is used as the on-chip ground. $V_{supply-L}$ is then a potential $V_{in-peak} - V_{drop-D1}$ volts greater than GND. From this perspective, it can be seen that $V_{supply-H}$, referenced to GND, is given by

$$V_{supply-H} = 2V_{in-peak} - V_{drop-D1} - V_{drop-D2}. \quad (3.3)$$

As before, the ripple on an individual supply line can be approximated by (3.1). However, as $V_{supply-H}$ is being referenced to GND, the actual ripple between $V_{supply-H}$ and GND is the sum of the solutions of (3.1) for $V_{supply-L}$ and $V_{supply-H}$.

The doubler exhibits two primary disadvantages. The first deals with the equivalent R_{ACload} . R_{load1} , powered by $V_{supply-L}$, presents an $R_{ACload1}$ to the input as calculated in (3.2), replacing R_{load} with R_{load1} and V_{drop} with $V_{drop-D1}$. R_{load2} , however, is placed between $V_{supply-H}$ and GND, rather than $V_{supply-H}$ and $V_{supply-L}$, and generates an additional equivalent load in parallel with that generated by R_{load1} . As derived in [10], R_{load2} produces an $R_{ACload2}$ calculated by

$$R_{ACload2} = \frac{R_{load2}}{8} \left(1 + \frac{V_{drop-D1} + V_{drop-D2}}{V_{supply-H}} \right). \quad (3.4)$$

For comparable R_{load} , R_{load1} , and R_{load2} , the voltage doubler presents a lower R_{ACload} to the input source as compared to the half-wave rectifier. The second disadvantage is the doubler's additional size, as two filter capacitors are necessary to implement the doubler.

In this application of the doubler, these disadvantages are diminished due to the low current drawn from $V_{supply-H}$. The doubled supply is only used to power components in the RF to DC converter and to drive the gates of CMOS switches, while $V_{supply-L}$ powers all other on-chip electronics. Therefore, the $V_{supply-H}$ current is expected to be

between one to two orders of magnitude less than the $V_{supply-L}$ current. This makes the contribution to the overall R_{ACload} from R_{load2} (Equation (3.4)) negligible, leaving simply

$$R_{ACload} = R_{ACload1} \parallel R_{ACload2} \approx R_{ACload1}. \quad (3.5)$$

Furthermore, from (3.1) it is apparent that the small $V_{supply-H}$ current also calls for a $C_{filter2}$ many times smaller than $C_{filter1}$ to produce the same magnitude of ripple.

Care must be taken with the on-chip implementation of the voltage doubler in Figure 3.4 due to the number of parasitics involved in the design. The p-n diodes in Figure 3.4 are prone to breakdown, especially under high current loads. Low voltage reverse breakdown of the diodes is also possible if doping levels are too high. Additionally, there exists a parasitic lateral NPN BJT between $V_{supply-H}$ (collector), GND (base), and V_{in} (emitter). When V_{in} swings a V_{th} below GND, this parasitic device can activate, shorting $V_{supply-H}$ and discharging $C_{filter2}$.

Replacing the diodes of Figure 3.4 with properly laid out diode-connected NMOS devices (Figure 3.5) eliminates the issue of diode breakdown and controls the peak current. The effect of the parasitic BJT can be marginalized by keeping transistors D_1 and D_2 far from any p^+ regions in the layout. In practice, this was accomplished by locating the doubler transistors at the center of the poly-poly $C_{filter2}$, isolating the transistors from the necessary RF $\rightarrow$ DC guard ring. The natural CMOS p-n parasitics, also shown in the figure, do not interfere with the doubler operation.

Figure 3.5: Implemented doubler with NMOS rectifier devices

Due to the varying possible current from $V_{supply-L}$, $C_{filter1}$ is currently implemented as an off-chip capacitor. A 1 nF capacitor provides good filtering behavior without producing high peak currents. $C_{filter2}$ is implemented on-chip with a value of 110 pF. The capacitor value was chosen from (3.1) to provide a desired worst-case ripple. In future lower-power designs, $C_{filter1}$ could also be implemented on-chip, given a sufficiently high $R_{ACload1}$ (i.e. sufficiently low current).

3.4 Regulator Design and Optimization

3.4.1 Regulator Overview

Figure 3.6: Typical regulator block-level overview

A block-level diagram of a typical regulator is presented in Figure 3.6. The rectifier produces a varying magnitude V_{supply} from the AC input signal. The op-amp compares the reference voltage produced by the bandgap reference to the feedback signal produced by the resistive divider from V_{DD} to GND, and accordingly adjusts the input of the pass device. The pass device then modulates the current flow from V_{supply} to provide the desired V_{DD} . This combination of op-amp, pass device, and negative feedback network is known as a “linear regulator” [11]. The startup circuits (not shown in Figure 3.6) are also essential to the operation of the regulator, and will be presented here as well.

There are three primary goals motivating the design of the linear regulator. The regulator must consume low power, provide high line regulation (DC PSR), and require no off-chip components. The low power dissipation and lack of off-chip components are the essential requirements of a miniature, wireless, implantable system, while the high line regulation controls the distortion on the supplies due to the varying coupling of an un-tethered animal.

The traditional linear regulator design relies on a large capacitor from V_{DD} to ground to provide stability and a low-pass output characteristic. As described previously, such large capacitors are unfeasible; therefore a fundamentally different and “capacitor-free” regulator design is presented in the following subsections. The primary difference between the capacitor-free regulator and the traditional design is the position of the dominant pole. The dominant pole in the traditional regulator is at the regulator output, providing the low-pass filtering characteristic. The capacitor-free regulator, however, is internally compensated [12]. Capacitance at the regulator output causes a non-dominant pole that can lead to instability, thus increasing the complexity of design.

3.4.2 Regulator Requirements

The following table lists the specific requirements for each of the two regulators:

Requirement	2 V Regulator	3 V Regulator
DC Load Current	$\sim 10 \mu\text{A} - 1.25 \text{ mA}$	0 A
Line Regulation (DC PSR)	-80 dB	-40 dB
Regulator Speed	$f_u \geq 400 \text{ kHz}$	$f_u \geq 1.1 \text{ MHz}$
Maximum Ripple at Output	25 mV _{pp}	200 mV _{pp}
Maximum Output Noise	$< 1 \text{ mV}_{\text{RMS}}$	--

Table 3.1: Regulator design requirements

The DC load current range lists the minimum and maximum current that the pass device of the regulator must supply. The 2 V regulator minimum load would require power-saving pulsed output transmission or passive telemetry, but is included as an extreme case. The current design implements none of the above, but the capability has been built into the regulator to allow for the possibility of future design improvement. The 3 V regulator drives only transistor gates, and therefore has zero DC load current.

Power supply rejection (PSR) is defined as the ratio of the variation in regulator output due to a variation on the supply voltage. Line regulation is the DC (or low frequency) PSR of the regulator, and is essential to this design as the majority of variation in the supply lines is due to mouse movement, which causes distortion at low (Hz - kHz) frequencies. Originally, the expected minimum detectable signal of the bio-sensing electronics would result in an output voltage with a magnitude of 200 μV . Variations in V_{DD} are coupled to sensor reference voltages and thus sensor output with only a few dB attenuation due to the design constraints on electronics from the low power supply. The worst-case V_{DD} variation should therefore be equal to or less than the minimum detectable signal. The worst-case expected variation in the supply line is 2 V, as provided by the coarse power control electronics, therefore -80 dB line regulation is necessary for the 2 V regulator. (The minimum detectable sensor output signal has been changed to 1

mV since the system was designed, but operation at -80 dB line regulation allows for design variation tolerance as well as future expansion.) The 3 V regulator supplies digital on/off signals, but it is possible for sufficiently large signals to be coupled through parasitic capacitances to signal processing electronics. The maximum safe low-frequency variation was determined to be 50 mV. Thus, given a maximum $V_{supply-H}$ variation of 4 V, a line regulation of about -40 dB is required.

The speed of the regulator is described by the unity gain frequency, f_u . For the 2 V regulator, a f_u of at least 400 kHz provides at least 70 dB PSR at 128 Hz, a requirement from the intelligent power control system, as will be described in Section 3.5.4. The 3 V regulator must be fast enough to handle the on-off switching of up to 2 pF of load capacitance in 1 μ s—10% of the switch clock speed—to allow for maximum charging time and thus maximum accuracy in switched-capacitor circuits. The speed of $f_u \geq 1.1$ MHz will be derived later.

The output ripple from the regulator is of less concern than low frequency output variations, as the interference is primarily a single tone signal that can be adjusted to prevent down-conversion of the ripple into the signal band. The concern with ripple, then, is the potential for disturbing device operation. The 2 V regulator is given a ripple requirement of 25 mV_{pp} or less, while the 3 V regulator is given a ripple requirement of 200 mV_{pp} or less.

In the linear regulator, the thermal noise on V_{DD} can also distort bio-signals. The noise spectrum of the 2 V regulator integrated from 1 Hz to 240 kHz (the 2 V regulator $\beta \cdot f_u$) must be less than the 1 mV minimum detectable signal, as described above. This corresponds to a V_{DD} noise floor of 2.0 μ V/Hz^{1/2}. As both the bandgap and the regulator

op-amp contribute noise, the total noise requirement is split between the two devices. For this design, the bandgap is allowed to contribute up to 90% of the output noise at the output ($1.8 \mu\text{V}/\text{Hz}^{1/2}$), while the regulator op-amp and pass device are permitted to contribute the remaining 10% noise ($200 \text{ nV}/\text{Hz}^{1/2}$). The noise contributed by the bandgap reference is amplified by the closed-loop gain of 1.67. Therefore, the maximum noise floor at bandgap output is $1.2 \mu\text{V}/\text{Hz}^{1/2}$. There are no noise requirements on the 3 V regulator, as electrical noise is too small to affect the digital switching behavior of the regulator output.

3.4.3 Pass Device Selection

The pass device in a linear regulator is usually a single transistor that controls the flow of current from supply to load to produce a constant, regulated V_{DD} . The pass device can be NMOS or PMOS, as shown below.

Figure 3.7: NMOS pass device (left) and PMOS pass device (right)

The NMOS pass device operates in common-drain (source follower) configuration. Here, the op-amp should have very high PSR in order to prevent signals from coupling from V_{supply} to the pass device gate, and from there to V_{DD} [13]. This is a fairly stable configuration—even in a capacitor-free regulator, as the pass device presents a small signal output resistance of g_m^{-1} at V_{DD} , indicating that stability can be achieved for low load current. Additionally, there is no signal amplification from the pass device,

meaning that no ripple amplification can occur in this setup. One disadvantage of the NMOS pass device setup is that the op-amp must provide fairly high gain, as will be described later. More importantly, the NMOS pass device displays increased power consumption, as it requires a high V_{supply} . In order to turn on the NMOS pass device, a V_{GS} greater than the NMOS threshold voltage must be applied. The source of the pass device is connected to V_{DD} , and therefore the minimum V_{supply} in this configuration is given by

$$V_{supply} > V_{DD} + V_{GS} + V_{dsat-OA} = V_{DD} + V_{TN} + V_{dsat-pass} + V_{dsat-OA} , \quad (3.6)$$

where V_{TN} is the NMOS threshold voltage with body effect ($V_{TN} \approx 0.8$ V), $V_{dsat-pass}$ is the V_{DSAT} of the pass device (~ 0.3 V), and $V_{dsat-OA}$ is the V_{DS} voltage necessary to keep the op-amp in saturation (~ 0.3 V). A minimum V_{supply} of 3.4 V, as calculated from (3.6), negates many of the advantages of using a low-supply, dual regulator system.

The PMOS pass device operates in a common-source amplifier configuration. Here the op-amp must have near 0 dB PSR in order to mirror V_{supply} variations at the pass transistor gate, thus keeping a constant V_{GS} and preventing the variations from being amplified to the output [13]. This configuration can operate with a much lower drop-out voltage, and thus a lower V_{supply} , as the PMOS gate is being pulled low, rather than high, to turn on the pass device. Using the same approach as in (3.6), the minimum V_{supply} for the PMOS pass device is

$$V_{supply} > V_{DD} + V_{dsat-pass} \text{ and } V_{supply} > V_{DD} + V_{dsat-OA} . \quad (3.7)$$

Assuming similar values as for (3.6), the PMOS V_{supply} would only need to be about 2.3 V, thus significantly reducing power consumption. This is known as the low drop-out (LDO) configuration. Additionally, the common source pass device further amplifies the signal, providing a measure of gain in addition to the op-amp, thus reducing the required op-amp

gain. However, the PMOS pass device configuration is less stable in a capacitor-free regulator, presenting an output resistance equal to the transistor's r_o —about 10x to 100x greater than that of the NMOS pass device. Furthermore, at MHz frequencies and beyond the f_u of the op-amp, the pass device can pass on amplified V_{supply} variations to V_{DD} rather than regulating the variations. The 4 MHz ripple and harmonics fall within the range of variations that would be amplified in this configuration, possibly requiring large C_{filter} capacitor to control the ripple.

The two supply voltages provided by the doubler offer a solution for the 2 V regulator that allows the stable NMOS device to operate in an LDO configuration. Supplying the op-amp with the doubled $V_{supply-H}$ and using an NMOS pass device, as shown in Figure 3.8, allows the gate of the pass device to be pulled above $V_{supply-L}$. In this configuration the minimum voltage for $V_{supply-L}$ is only 2.3 V—the $V_{dsat-pass}$ term in (3.6) and (3.7)—while all the advantages of the NMOS pass device (stability, ripple rejection) are preserved.

Figure 3.8: NMOS pass device with doubled supply

The 3 V regulator has much lower ripple rejection and line regulation requirements, as well as the same supply for op-amp and pass device. Therefore, a basic LDO PMOS pass device is the best choice for the 3 V regulator.

3.4.4 Bandgap Placement

Having chosen the NMOS pass device, the placement of the bandgap and its effect on regulator PSR is another important design consideration.

The devices in a traditional linear regulator are arranged as in Figure 3.9, with the bandgap reference supplied by V_{supply} . However, a mathematical feedback analysis of this system reveals certain limitations for a system which requires high line regulation. In the following signal feedback diagrams, A_1 represents the open-loop gain of the op-amp and pass device, A_2 represents the PSR of the op-amp, A_3 represents the PSR of the bandgap, and f is the feedback factor set by the resistive divider. An additional feedthrough path consisting of the pass device PSR is present, but its effects are negligible in this configuration.

Figure 3.9: Traditional regulator device arrangement

Figure 3.10: Feedback analysis of traditional regulator device arrangement

A mathematical analysis of Figure 3.10 yields the following equation for PSR:

$$PSR = \frac{V_{DD}}{V_{supply}} = \frac{A_2}{1 + fA_1} + \frac{A_1}{1 + fA_1} A_3. \quad (3.8)$$

Assuming that, for low frequencies, $A_1 A_3 \gg A_2$ and that $fA_1 \gg 1$, the line regulation, PSR_0 , is given by

$$PSR_0 \approx \frac{A_3}{f}. \quad (3.9)$$

In other words, the low frequency PSR of the bandgap defines the line regulation of the regulator.

The PSR of the bandgap reference is typically improved by adding cascode devices to the current sources and increasing transistor lengths. However, the low value of $V_{supply-L}$ does not leave sufficient headroom for cascode devices. Given the limitations of the system, it is unfeasible to design a bandgap reference with the necessary -84 dB DC PSR to provide the 80 dB line regulation required of the 2 V regulator.

An alternate configuration of regulator elements is shown in Figure 3.11. Here, the bandgap reference is supplied not by V_{supply} , as in Figure 3.10, but by the regulator output, V_{DD} . The feedback analysis is shown in Figure 3.12.

Figure 3.11: Alternate regulator device arrangement

Figure 3.12: Feedback analysis of alternate regulator device arrangement

A mathematical analysis of Figure 3.12 yields the following equation for PSR:

$$PSR = \frac{V_{DD}}{V_{supply}} = \frac{A_2}{1 + A_1(f - A_3)} \quad (3.10)$$

Assuming that, at low frequencies, $f \gg A_3$ and $fA_1 \gg 1$, the line regulation is given by:

$$PSR_0 \approx \frac{A_2}{fA_1} \quad (3.11)$$

Here, the system PSR is given by the op-amp PSR—less than 1—divided by the open-loop gain—a high value—yielding very good line regulation, and the possibility of achieving -80 dB line regulation.

The above model can be extended to the dual supply method described in Section 3.4.4 by noting that, due to the action of the voltage doubler, low-frequency $V_{supply-H}$ variations are simply twice the corresponding $V_{supply-L}$ variations. In other words,

$$PSR_0 \approx 2 \frac{A_2}{fA_1} \quad (3.12)$$

This design provides the necessary PSR but has two disadvantages. First, as indicated by the subtraction function in the denominator of (3.10), there exists the possibility of positive feedback overwhelming the regulating loop. To prevent this, A_3 —

the bandgap PSR—must be less than the feedback factor f up to the unity gain frequency of A_I . Additionally, care must be taken to minimize the capacitance between the feedback node and GND, which could potentially decrease f at increased frequencies. This can be readily achieved, and is not a major design concern. More important, however, is the necessity of a reliable startup circuit in this configuration. Without a startup circuit, the circuit in Figure 3.11 is stable in the condition $V_{DD} = 0$ V and $V_{bandgap} = 0$ V. A circuit is thus necessary to raise V_{DD} sufficiently high to allow the bandgap reference to “turn on” and stabilize, which then ensures that the remainder of the regulator will begin operating normally.

The 3 V regulator uses the same bandgap reference voltage as the 2 V regulator.

3.4.5 Bandgap Reference

The bandgap reference provides a process independent, temperature independent, supply independent voltage reference that the regulator uses to set the output V_{DD} level. The bandgap reference circuit produces an output based upon a physical constant and device ratios, which allows for a precise output unrelated to process parameters. Bandgap references require BJT devices; the chosen AMI 1.5 μ m CMOS process provides parasitic pnp transistors that suffice. Though many bandgap architectures are available, the self-biased bandgap was chosen due to its speed, simplicity, and low power consumption. The bandgap core is shown in Figure 3.13.

Figure 3.13: Self-biased bandgap core

In this self-biased bandgap design, transistors M_{p1} , M_{p2} and M_{p3} are matched and identical in size, as are M_{n1} and M_{n2} . The PMOS devices, all with identical V_{GS} and W/L, supply the same current to each of the three branches. The NMOS devices, also with identical W/L and I_D , are thus forced to have the same V_{GS} , which forces the voltage at the source of both transistors to be the same. In other words,

$$V_{BE1} = V_{BE2} + I_{BG} R_1, \quad (3.13)$$

where V_{BE1} and V_{BE2} are the base-emitter voltages of the pnp transistors, and I_{BG} is the current in any one branch. From the BJT device equations and (3.13), the branch current can be determined as

$$I_{BG} R_1 = V_{BE1} - V_{BE2} = V_T \ln(N), \quad (3.14)$$

where N is the size ratio of Q_2 and Q_1 . As a result, the bandgap output reference voltage is

$$V_{bandgap} = V_{BE3} + V_T \ln(N) \frac{R_2}{R_1} . \quad (3.15)$$

In (3.15), a proportional-to-absolute-temperature (PTAT) value is being added to a complementary-to-absolute-temperature (CTAT) value. Given a proper choice of N and resistor ratio, the temperature variation in (3.15) can be greatly suppressed over a certain temperature range. From the derivation in [10], both N and R_2/R_1 are chosen to be 10 to minimize the temperature variation of the bandgap. These even integer multiples also allow for precise element matching and thus increased accuracy.

As seen from (3.14), the resistor sizes control the current consumption of the bandgap reference. Large resistors reduce power consumption, but reduced current increases thermal voltage noise at the output. The thermal current noise of an individual transistor is approximated using

$$\overline{i_{dn}^2} = \frac{8}{3} kT g_m \Delta f . \quad (3.16)$$

The noise current contributions from each transistor sum (in quadrature) at the bandgap output. This noise current is multiplied by the output resistance of the bandgap reference, equal to R_2 ($r_{o3} \parallel R_2 \approx R_2$), to get the bandgap reference output noise voltage. A transistor's g_m is proportional to $\sqrt{I_d}$, while R_2 is proportional to I_d^{-1} . The output voltage noise is therefore proportional to $1/\sqrt{I_d}$. To achieve a bandgap output noise floor of less than $1.2 \mu\text{V}/\sqrt{\text{Hz}}$ —in order to meet the noise requirement specified in Section 3.4.2—an I_{BG} of $1.0 \mu\text{A}$ or greater is necessary given an estimate of $R_2 = 500 \text{ k}\Omega$. Resistor sizes of $40 \text{ k}\Omega$ and $400 \text{ k}\Omega$ were chosen for R_1 and R_2 , respectively, to provide a designed I_{BG} of $1.5 \mu\text{A}$ and a worst-case I_{BG} of $1.0 \mu\text{A}$.

The bandgap reference core shown above is also stable if the drain of M_{n1} is 0 V and the drain of M_{n2} is equal to V_{DD} . In this case, $V_{bandgap}$ is 0 V , and a circuit is necessary

to pull up the gate of M_{n1} or pull down the gate of M_{p2} . This turns on the PMOS and NMOS devices, which will cause the bandgap reference to re-stabilize in the “on” state. A startup circuit, as shown in Figure 3.14, turns on the PMOS transistors when $V_{bandgap}$ is low, then “disconnects” itself from the bandgap core when $V_{bandgap}$ rises sufficiently. The startup circuit consumes a small bias current ($\sim 0.5 \mu\text{A}$) when inactive, kept low by the very low W/L and therefore high on resistance of M_{s2} . The low W/L of M_{s2} also ensures that M_{s3} will be fully turned off when the startup circuit is inactive. This startup circuit fulfills a different role from the necessary regulator startup circuit mentioned in Section 3.4.4.

Figure 3.14: Complete bandgap reference with startup circuit

The W/L values listed in Table 3.2 were chosen in order to allow the bandgap to operate with a 2 V supply even under the worst-case process parameters such as high V_T and high V_{BE} , and also to provide sufficient PSR at frequencies below 10 MHz to allow the bandgap to operate as an ideal voltage source ($A_3 = 0$) for the purposes of (3.10) and

(3.11). The large device lengths incidentally prevent 1/f noise from being a design concern.

Device	Size (W / L)
M_{s1}	4.8 μm / 4.8 μm
M_{s2}	4.8 μm / 94.4 μm
M_{s3}	4.8 μm / 1.6 μm
M_{p1}, M_{p2}, M_{p3}	160 μm / 12 μm
M_{n1}, M_{n2}	70 μm / 8 μm
R_1	40 k Ω
R_2	400 k Ω
Q_1, Q_3	1x
Q_2	10x

Table 3.2: Bandgap reference device sizes

3.4.6 Operational Amplifier for 2 V Regulator

It is clear from (3.11) that the op-amp in Figure 3.6 and Figure 3.11 controls the line regulation. From (3.11), it is also clear that the op-amp should have $\text{PSR} < 0$ dB, which requires an NMOS current mirror [14]. (The use of an NMOS current mirror and biased PMOS devices rather than a PMOS current mirror and biased NMOS devices helps to separate the op-amp output from supply variations in open-loop operation.) Additionally, in order for the differential pair devices to remain in saturation for a nominal input of 1.2 V (bandgap output) and ~ 3.5 V output, an NMOS differential pair is necessary. Cascoded output devices are essential to produce the necessary high op-amp gain. The doubled supply, $V_{\text{supply-H}}$, provides sufficient headroom for cascode devices to be used—an example of additional advantages from the doubler rectifier. From these requirements, a folded-cascode amplifier topology was chosen for the 2 V regulator op-amp design as shown in Figure 3.15.

The differential inputs to the above op-amp are V_{bandgap} and V_{fb} . The single-ended output which connects to the gate of the NMOS pass device is V_{out} . M_{n1} is biased and

sized to consume 1 μA using V_{bias1} , supplied by a matched current source. Similarly, M_{p1} and M_{p2} are biased and sized to each source 1 μA , and M_{p3} and M_{p4} are both biased and sized to source 0.5 μA . The tail current of 1 μA was chosen to push the op-amp's non-dominant pole to sufficiently high frequency and to meet the thermal noise requirements from (3.16) and section 3.4.2.

Figure 3.15: Folded-cascode operational amplifier for 2 V regulator

In this design, transistor pairs $M_{n2/3}$, $M_{p1/2}$, and $M_{n6/7}$ contribute a significant degree of 1/f noise to the op-amp output, due to the high op-amp gain. The SPICE flicker noise model for CMOS devices is shown as:

$$\frac{K_f I_{DS}}{C_{OX} L_{eff}^2 f} = f_n^2. \quad (3.17)$$

Here, K_f is a modeling constant, I_{DS} is the drain current of the transistor, C_{OX} is the oxide capacitance, L_{eff} is the effective channel length, and f is the frequency of interest. This equation is integrated over a range of relevant frequencies, 1 Hz to 240 kHz, and then multiplied by the individual transistor's noise transfer function (generally, the transistor's r_o) to calculate the transistor's total flicker noise contribution over the region of interest. This analysis provides certain minimum channel lengths for the aforementioned transistors to provide a total $1/f$ noise contribution significantly less than the thermal noise contribution.

The pass device is sized to provide the maximum current load (1.25 mA) with a V_{dsat} of 200 mV. This 200 mV limit keeps the amplifier output V_{out} under 3.5 V, allowing sufficient V_{DS} to keep the PMOS devices in strong saturation. The necessary pass device W/L to achieve this under worst case conditions is $W/L = 440$.

In this design, the NMOS current mirrors give the op-amp a PSR less than 0 dB—approximately -10 dB worst-case to -30 dB best-case. From (3.12), if the op-amp supplies a gain of at least 80 dB, line regulation of -80 dB or better is guaranteed. The cascoded NMOS and PMOS devices with non-minimum channel provide the high output resistance and the necessary gain. The final device sizes are listed in the following table.

Device	Size (W / L * M)
M_{n1}	24 μm / 8 μm * 2
M_{n2}, M_{n3}	64 μm / 16 μm
M_{n4}, M_{n5}	12 μm / 4 μm
M_{n6}, M_{n7}	12 μm / 4 μm
M_{p1}, M_{p2}	40 μm / 4 μm * 2
M_{p3}, M_{p4}	107.6 μm / 3.2 μm
M_{pass} (not shown)	116.8 μm / 1.6 μm * 6

Table 3.3: Device sizes for 2 V regulator op-amp

3.4.7 Compensation, Speed, and Stability of 2 V Regulator

A capacitor-free, internally compensated regulator with an NMOS pass device and bandgap placement as specified in Section 3.4.4 exhibits PSR versus frequency behavior as shown in the following Figure 3.16 [13, 14].

Figure 3.16: PSR versus frequency for 2 V regulator

This behavior can largely be derived from the PSR equations in Section 3.4.4. From (3.11), it is apparent that the PSR inversely mirrors the -20 dB/decade roll off of the op-amp's gain after the op-amp's dominant pole. From (3.10) and (3.11), it can be seen that, near the unity gain frequency of the op-amp (f_u), the regulator PSR plateaus at a value approximately equal to the op-amp PSR. The output pole, p_2 , caused by capacitance from V_{DD} to ground, acts as a low pass filter for high frequencies, causing a 20 dB/decade improvement in PSR. For stable operation, p_2 must be at a higher frequency than f_u .

The internal dominant pole (p_1) and unity gain frequency (f_u) are calculated as follows, where g_m , R_{O-OA} , and C_{O-OA} refer to the op-amp's transconductance, output resistance, and total output capacitance, respectively.

$$f_u = \frac{g_m}{C_{O-OA}} \quad \text{and} \quad p_1 = \frac{1}{R_{O-OA} C_{O-OA}} \quad (3.18)$$

The non-dominant output pole (p_2) which occurs due to the regulator load current and load capacitance is calculated as follows, where I_{load} is the total regulator load current, g_{m-pass} is the transconductance of the pass device, and C_{out} is the total capacitance at the regulator output.

$$p_2 = \frac{1}{\left(\frac{V_{DD}}{I_{load}} \parallel g_{m-pass}^{-1} \right) C_{out}} \quad (3.19)$$

As will be described in Section 3.5.4, a PSR of -70 dB or better is desirable at 128 Hz to suppress distortion from the operation of the adaptive power control system. Given the -20 dB/decade PSR roll off and line regulation of at least 80 dB, f_u needs to be at least 400 kHz to provide -70 dB PSR at 128 Hz. Given the g_m of the op-amp equal to 10 μ S and the load capacitance from the pass device at op-amp output equal to approximately 600 fF, a f_u of 400 kHz can be achieved by adding an additional 3 pF compensation capacitor at the op-amp output.

The f_u is chosen to be 400 kHz, rather than a higher value, in order to take advantage of the high frequency low-pass characteristics shown in Figure 3.16. The output low-pass filter characteristic aids in suppressing supply distortion due to the implant system's integrated VCO and transmitter, as well as reducing crosstalk. For stability reasons, p_2 was designed to be at least $2 * f_u$, or 800 kHz. Using (3.19) and a worst-case (minimum) I_{load} of 10 μ A, it is calculated that a C_{out} of 30 pF will provide the desired p_2 . As it is not desirable for p_2 to drop below the design value—but safe for p_2 to be greater than the design value—only 15 pF of this capacitance is implemented on-chip to ensure stability during testing, allowing up to 15 pF of off-chip and probe capacitance.

3.4.8 Operational Amplifier for 3 V Regulator

The operational amplifier for the 3 V regulator has less stringent requirements than the operational amplifier for the 2 V regulator. A mathematical analysis similar to that undertaken in Section 3.4.4 is applied to the 3 V regulator. The resulting feedback diagram is shown below in Figure 3.17.

Figure 3.17: Feedback analysis of 3 V regulator

In Figure 3.17, A_1 is the gain of the op-amp, A_2 is the PSR of the op-amp, A_3 is the gain of the common-source PMOS pass device, A_4 is the PSR of the pass device, and f is the resistive feedback factor. As the bandgap reference is not directly involved with this network, it is assumed that the bandgap reference behaves as an ideal voltage source. The subtractive contribution from the supply in Figure 3.17 that is not present in Figure 3.12 is due to the V_{GS} of the PMOS pass device being referenced between transistor gate and the varying V_{supply} . A feedback analysis provides the following equation for the 3 V regulator PSR:

$$PSR = \frac{A_3(A_2 - 1) + A_4}{1 - A_1 A_3 f}, \quad (3.20)$$

and, for low frequencies with proper design,

$$PSR_0 \approx \frac{-1}{fA_1A_3} = \frac{-1}{fA_{OL}}. \quad (3.21)$$

In (3.21), it is assumed that $A_4 \approx 1$ (due to the PMOS pass device), and $A_2 \approx 1$ from proper op-amp design.

A PMOS current mirror gives the op-amp a PSR near 0 dB [14], meaning that the line regulation (PSR_0) can be designed using (3.21). As the pass device alone provides a gain of 20-30 dB, the operational amplifier only needs to supply an additional 20-30 dB to provide the desired 3 V regulator behavior. The tail current was chosen to prevent slew rate limiting of op-amp speed. The tail current is set to 4 μ A by a current mirror that produces V_{bias} . The operational amplifier topology and device sizes are shown below in Figure 3.18 and Table 3.4, respectively.

Figure 3.18: Operational amplifier for 3 V regulator

Device	Size (W / L * M)
M _{n1}	24 μm / 8 μm * 8
M _{n2} , M _{n3}	4 μm / 1.6 μm
M _{p1} , M _{p2}	4 μm / 1.6 μm
M _{pass} (not shown)	16 μm / 1.6 μm

Table 3.4: Device sizes for 3 V regulator op-amp

3.4.9 Compensation, Speed, and Stability of 3 V Regulator

As mentioned in Section 3.4.3, speed and stability are concerns of a PMOS pass device regulator. Due to the PMOS pass device providing a gain greater than one, Miller compensation and pole splitting can be used to improve the performance of the regulator by connecting a compensation capacitor between the amplifier output and the regulator output (gate to drain of the PMOS pass device).

The speed requirement of the regulator is derived from the desired switching time, as described in section 3.4.3. To ensure proper switching behavior, the regulator is required to supply 75% of the necessary current within half the settling time (500 ns). For a linear settling system,

$$I_{out} = I_O(1 - e^{-t/\tau}), \quad (3.22)$$

where I_{out} is the output current at any given point in time, I_O is the desired final current, t is the elapsed time, and τ is the time constant. Rearranging the above and redefining the time constant gives:

$$\frac{1}{\beta\omega_u} = \tau = \frac{t}{\ln(0.75)}. \quad (3.23)$$

Here, β is the feedback factor of 0.4 and ω_u is the unity gain frequency. This gives a minimum f_u of 1.1 MHz.

Pole-splitting increases the frequency of the non-dominant pole, thus improving amplifier stability at high speed operation, but also increases the complexity of

compensation. The Miller effect causes the dominant pole to be lowered to a frequency given by

$$p_1 = \frac{1}{A_{pass} R_{O-A} C_{O-A}} = \frac{1}{g_{m-pass} R_{O-pass} R_{O-A} C_{O-A}}. \quad (3.24)$$

A_{pass} is the gain of the pass device, R_{O-pass} and R_{O-A} are the small signal output resistances of the pass device and op-amp, respectively, C_{O-A} is the physical amplifier output capacitance, and g_{m-pass} is the transconductance of the pass device. Similarly, the non-dominant regulator output pole is given by

$$p_2 = \frac{C_{O-A} g_{m-pass}}{C_{out} C_p + C_{O-A} C_{out} + C_{O-A} C_p}. \quad (3.25)$$

In this equation, C_{out} is the regulator load capacitance, and C_p is the parasitic capacitance between the amplifier output and ground.

The simultaneous solutions of (3.24) and (3.25) along with PMOS device parameter equations for r_o , g_m , and V_{dsat} provide the optimum device values and sizes to achieve the desired 3 V regulator operation. These values are: $C_{O-A} = 2$ pF, pass device W/L = 10, and minimum DC load current $I_D = 10$ μ A (provided by feedback resistors). These device values provide the necessary speed and a 60° worst-case phase margin in SPICE simulations.

Though the 3 V regulator could alternately be stabilized with the dominant pole at V_{DD-3V} given the lack of a large DC load, this would lead to a poorly controlled V_{DD-3V} level. The DC load of a regulator acts as a “pull” stage, pulling against the “push” of the pass device. Eliminating the DC load transforms the regulator into a “push-only” device, with large overshoots and significant variation of the V_{DD-3V} level. Additionally, such a

configuration would require significant on-chip area for the large value feedback resistors and large output capacitor necessary to stabilize the regulator.

3.4.10 Digital Buffer

In a mixed-signal system-on-chip design, a major contributor of noise and interference to the analog electronics is the distortion of the supply due to the large number of switching digital logic gates. The distortion takes the form of sudden, large spikes on V_{DD} caused by the sudden current draw of digital transistors being switched from ground to V_{DD} , and the finite time required for the regulator to adjust itself to the new (temporary) load current. Though differentially designed signal processing electronics can minimize the effect of this distortion, the noise can still interfere with sensors operation via reference voltages and less-than-ideal CMRR.

As a result, a buffer is necessary to separate the V_{DD} supplying the digital electronics ($V_{DD-Digital}$) from the V_{DD} supplying the analog electronics ($V_{DD-Analog}$), as shown in Figure 3.19. Separating the supplies prevents the current spike from the switching digital gates from directly distorting $V_{DD-Analog}$. Instead, the current spike is drawn from $V_{supply-L}$, producing a small voltage distortion on $V_{supply-L}$ due to the large rectifier filter capacitor between $V_{supply-L}$ and GND as shown in Figure 3.4. This distortion is further reduced in magnitude by the ~ 20 dB high-frequency PSR of the 2 V regulator as illustrated in Figure 3.16, yielding a distortion on $V_{DD-Analog}$ of less than 1 mV for the expected component values.

Figure 3.19: Block diagram including digital buffer

Figure 3.19 illustrates the buffer architecture and its placement in the overall regulator. In the digital buffer, an op-amp compares $V_{DD-Analog}$ to $V_{DD-Digital}$, and adjusts the gate of the PMOS pass device to provide a $V_{DD-Digital}$ equal to $V_{DD-Analog}$. No feedback resistors are necessary—as opposed to the 2 V and 3 V regulator designs—as $V_{DD-Digital}$ itself is used as the feedback voltage to the digital buffer op-amp. Due to the lack of feedback resistors and the fact that the load is fully digital, the dominant pole can easily be placed at the regulator output. This results in poor control of the average level of $V_{DD-digital}$ due to the “push-only” nature of the buffer (as opposed to a traditional push-pull output), but reduces power consumption, occupied space, and improves stability. As $V_{DD-Digital}$ only supplies digital electronics, a poorly controlled average $V_{DD-digital}$ is acceptable.

The digital buffer design is optimized to meet two additional requirements on $V_{DD-Digital}$. First, $V_{DD-Digital}$ must be prevented from spiking below 1.5 V, in order to prevent logic gates from entering unstable states. Additionally, $V_{DD-Digital}$ should fully recover from a distortion within a single period of the fastest on-chip clock. In this design, the fastest electronics are associated with the clock extractor and are operating at 4 MHz, or with a 250 ns period.

The $C_{storage}$ capacitor in Figure 3.19 acts as a reservoir to supply charge to the switching digital gates and reduce the magnitude of the spike on $V_{DD-Digital}$. The “dip” voltage associated with a switching spike can be estimated as follows:

$$V_{dip} = V_{DD-Digital} \frac{C_{digital}}{C_{digital} + C_{storage}}. \quad (3.26)$$

From (3.26) and the estimated capacitance of the digital electronics, a $C_{storage}$ of 17 pF is derived to prevent $V_{DD-Digital}$ from dipping below 1.5 V. The PMOS pass device in Figure 3.19 was designed with a W/L of 123 to provide the 280 μ A necessary to slew the total load capacitance in 125 ns. The amplifier tail current of 2 μ A was then chosen to slew the pass device gate in an additional 125 ns. This configuration yields an overall settling time of less than 250 ns due to the overlap between the two 125 ns periods.

The remainder of the thesis will continue to refer to $V_{DD-analog}$ simply as V_{DD} , and specify $V_{DD-digital}$ when it is referenced.

3.4.11 Startup Circuit

As mentioned in section 3.4.4, a startup circuit is necessary to raise V_{DD} high enough for the bandgap reference to activate and stabilize at its nominal operating point [15]. The circuit pictured below takes a startup signal, $V_{startup}$, as an input. When $V_{startup}$ is less than the NMOS threshold, M_{s3} , M_{s4} , and M_{s5} are turned on. M_{s5} then pulls up the gate of the pass device, turning on the pass device and pulling up the regulator output, V_{DD} , which turns on the regulator bandgap reference. When $V_{startup}$ rises above the NMOS threshold, M_{s1} pulls down the gate of M_{s3} due to the small W/L chosen for M_{s2} , which turns off M_{s4} and M_{s5} , disconnecting the startup circuit and permitting normal regulator operation. As the bandgap reference controls the bias current for the regulator op-amp,

the op-amp is entirely inactive when the bandgap reference has yet to start up. This means that M_{s5} does not “pull against” the regulator op-amp during startup, and has sole control over the gate of M_{pass} . The device sizes for the startup circuit are recorded in Table 3.5.

Figure 3.20: Basic startup circuit schematic

Device	Size (W / L * M)
M_{s1}	16 μm / 1.6 μm
M_{s2}	4 μm / 80 μm
M_{s3}	8 μm / 8 μm
M_{s4}	40 μm / 8 μm
M_{s5}	16 μm / 16 μm
M_{pass}	116 μm / 1.6 μm * 6

Table 3.5: Device sizes for startup circuit

Originally, it was intended that $V_{startup}$ be controlled by a feedback voltage developed by a resistive divider between V_{DD} and ground. Ideally, this feedback voltage is equal to the NMOS threshold (0.7 V) when V_{DD} is 1.7 V. This requires a resistive divider that produces a feedback voltage equal to 40% of V_{DD} . The startup circuit would raise V_{DD} to 1.7 V and hold V_{DD} at this level until the bandgap activates. With a working bandgap reference, the regulator then pulls V_{DD} up to 2.0 V and the startup circuit shuts off.

In practice, however, the NMOS threshold voltage can vary by up to $\pm 20\%$. As the voltage provided by the resistive divider remains a constant 40% of V_{DD} , the necessary V_{DD} to provide the NMOS threshold to M_{sl} , turning off the startup circuit, also varies by $\pm 20\%$. This means that there is a $\pm 20\%$ variation in the value of V_{DD} provided by the startup circuit (from $V_{DD} = 1.4$ V to $V_{DD} = 2.2$ V). If the NMOS threshold is very low, V_{DD} will not rise high enough for the bandgap reference to turn on, and the regulator will not start. If NMOS the threshold is very high, the startup circuit will raise V_{DD} past 2.0 V and will not shut off when the regulator activates, disrupting regulator performance. Therefore a threshold independent startup control is necessary.

Figure 3.21: Startup circuit overview with threshold-independent control

Figure 3.21 illustrates a method by which the startup circuit can be controlled without regard to process parameters. A voltage reference generates a process-parameter independent reference, which is compared to a voltage developed by a resistive divider between V_{DD} and ground. The output of this comparator then acts as the $V_{startup}$ in Figure 3.20, controlling the startup circuit. The remainder of the startup circuit works the same as before, pulling up V_{DD} to a level that allows the bandgap reference to start-up, activating the regulator op-amp and turning on the regulator loop. At this point V_{DD} rises

to 2 V and startup feedback voltage rises past the 1.2 V reference. The comparator output then switches, shutting off the startup circuit.

As implemented, the comparator is a simple differential-to-single-ended amplifier with a gain of 40 dB (similar to Figure 3.19). The voltage reference is implemented using a bandgap reference with the same structure as in Figure 3.15. Inverting the comparator inputs eliminates the need for M_{s1} and M_{s2} in Figure 3.20. The device sizes for the startup circuit bandgap reference are listed below in Table 3.6. Smaller size transistors were used as PSR requirements are less stringent and there is greater voltage headroom than for the regulator bandgap reference. Additionally, larger resistors were used to decrease current consumption, as thermal noise is not a concern. In the implementation, a feedback voltage equal to 70% of V_{DD} is fed back to the comparator, corresponding to a startup V_{DD} of 1.7 V, sufficient to start the regulator bandgap.

Device	Size (W / L)
M_{s1}	4.8 μm / 4.8 μm
M_{s2}	4.8 μm / 94.4 μm
M_{s3}	4.8 μm / 1.6 μm
M_{p1}, M_{p2}, M_{p3}	16 μm / 8 μm
M_{n1}, M_{n2}	16 μm / 8 μm
R_1	50 k Ω
R_2	500 k Ω
Q_1, Q_3	1x
Q_2	10x

Table 3.6: Device sizes for startup circuit bandgap reference

3.4.12 Regulator Summary

A dual regulator design has been presented that operates from dual power supplies of 2.5 V and 4.5 V (minimums), and provides regulated 2 V and 3 V output supplies. The regulated supplies conform to the specifications listed in Section 3.4.2. The bias current consumption of each component is listed in Table 3.7.

Component	$V_{\text{supply-L}}$ current	$V_{\text{supply-H}}$ current
2 V Regulator	4 μA	2 μA
3 V Regulator	0 μA	14 μA
Current Reference	1 μA	0 μA
Digital Buffer	2 μA	0 μA
Regulator Bandgap	5 μA	0 μA
Startup Bandgap	3.5 μA	0 μA
Startup Circuit	1 μA	0 μA
Misc. Buffers	1 μA	0 μA
TOTAL	15.5 μA	16 μA

Table 3.7: Bias current consumption of regulator electronics

3.5 Coarse Power Control Electronics

3.5.1 Coarse Power Control Overview

In Section 2.3.1, the physical operating region was optimized to reduce the total possible input power variation to a factor of 18.5. However, assuming a constant load current, this reduced power variation still yields a maximum $V_{\text{supply-H}}$ of over 70 V! This high voltage is well beyond the breakdown voltages of the on-chip gate oxide and p-n junctions—approximately 16 V. Additionally, significant supply variation increases the design difficulty of the regulators. Therefore, a system is necessary to restrain the possible range of input voltages, referred to here as the “coarse power control”. Three methods for coarse power control will be discussed in this section.

3.5.2 Voltage Limiter

The simplest form of coarse power control—when Zener diodes are unavailable—is the voltage limiter. The limiter, in this case, is a single, large transistor that sinks extra current from $V_{\text{supply-L}}$ to ground to ‘burn off’ the additional power received by the implant. By increasing the load current by a factor of 10 or more, the limiter can prevent $V_{\text{supply-L}}$ and $V_{\text{supply-H}}$ from increasing by more than a few volts.

The gate of this transistor is driven by a voltage detector, shown below in Figure 3.22. The devices in the detector are sized to output a signal, $V_{detector}$, that is 0 V at $V_{supply-L} = 2.5$ V, as insufficient current flows through R_1 to provide a voltage drop that would turn on M_{p1} . As $V_{supply-L}$ increases, current flows through M_{p1} and R_2 , and $V_{detector}$ undergoes a square-law increase. The drain current of $M_{limiter}$ undergoes a square-law increase with respect to $V_{detector}$, yielding an overall x^4 relationship between limiter drain current and $V_{supply-L}$. In this design, the values of R_1 and R_2 are 100 k Ω and 80 k Ω , respectively, and the sizes of M_{n1} and M_{p1} are 4 μm / 18.4 μm and 16 μm / 1.6 μm , respectively.

Figure 3.22: $V_{supply-L}$ voltage detector and limiter

The voltage detector provides two important advantages over a simple resistive divider. First, the detector shown above allows for a much steeper $V_{detector}$ versus $V_{supply-L}$ characteristic, decreasing the range of $V_{supply-L}$ variation. Additionally, the detector consumes little bias current when $V_{supply-L}$ is low enough to not turn on M_{p1} , reducing power consumption when input power is limited.

The primary disadvantage of the limiter involves the $V_{supply-L}$ ripple. Equation (3.1) shows that ripple is proportional to load current. The voltage limiter limits $V_{supply-L}$ and

$V_{supply-H}$ by drastically increasing the load current, which produces an equivalent increase in ripple. In the current design, $C_{filter1}$ is off-chip, meaning that the capacitor can be sized sufficiently large such that this is not an issue. In future designs with reduced load current, $C_{filter1}$ will be implemented as an on-chip capacitor. In this case, the additional ripple due to the limiter would be a serious concern.

For example, an implant system without a limiter and with a 100 μ A load current that can tolerate 250 mV $V_{supply-L}$ ripple requires a $C_{filter1}$ of 100 pF, which can be readily implemented on-chip. This voltage limiter, however, would sink at least an additional 1.8 mA at maximum implant power, requiring a $C_{filter1}$ of 1400 pF—far too high to be implemented on-chip.

3.5.3 Capacitive Detuning

Another method of controlling power is to reduce the voltage swing out of the implanted LC tank. This can be achieved using capacitive detuning. Figure 3.23 below illustrates this method for the prototype device.

Figure 3.23: Voltage doubler and LC tank with detuning power control

In this implementation, an NMOS transistor and a capacitor in series are placed parallel to the LC tank. The presence of C_{detune} prevents drain parasitics (from M_{detune} drain to the top $RF-in$ node, when the $RF-in$ node swings below GND) from interfering with operation by blocking the one-way current flow associated with the pn junction between the bulk and drain of M_{detune} . $V_{detector2}$ is provided by a second voltage detector, similar in structure to Figure 3.22, but powered from $V_{supply-H}$.

The capacitance C_{detune}' seen by the LC tank can be approximated as follows, for values of Q less than 1:

$$C_{detune}' = \frac{C_{detune}}{1 + \left(\frac{1}{Q}\right)^2} \approx Q^2 C_{detune},$$

where Q is the quality factor of the C_{detune} branch, given by

$$Q = \frac{1}{\omega R_s C_{detune}}. \quad (3.27)$$

Here, the transistor M_{detune} acts as a voltage-controlled resistor, producing the series resistance, R_s . Under normal operation, the transistor is off ($R_s = \infty$, $Q = 0$) and the LC tank does not “see” C_{detune} (i.e. $C_{detune}' = 0$). If $V_{supply-H}$ rises sufficiently, the detector will turn on the transistor by raising the gate above $V_{supply-L}$, reducing R_s , increasing Q , and thus increasing C_{detune}' and detuning the LC tank.

The necessary C_{detune} can be calculated from the necessary 4 MHz impedance of the detuning branch. The detuning branch needs to have a minimum (“fully on”) impedance equivalent to 18.5 times less than the implant “off” impedance of Z_2 from Chapter 2. Reducing the implant load current increases Z_2 and correspondingly decreases the necessary C_{detune} . For an implant load current of 200 μA , C_{detune} must be 200 pF to

sufficiently detune the LC tank under maximum input power—a capacitor that can be implemented on-chip.

3.5.4 Adaptive Power Control

Though the previously discussed coarse power control mechanisms can successfully limit the on-chip voltage levels, they do not save power, as the external power amplifier driving the external inductor coil continues to run at maximum output level. An adaptive power control system—where the power consumed by the external power amplifier is adjusted to meet the needs of the implant system—is desirable as it reduces the overall system power consumption and also reduces the cage floor temperature increase that is due to the resistive heating of the external coil.

Adaptive power control techniques have been proposed in other literature [16,17]. These systems operate by converting the on-chip power level to a digital representation, then transmitting this data to an external system which controls the power provided by the external power amplifier. Multiple bits of power information are used to precisely define the desired power level from the external power supply to minimize variation on the implant supply.

In this proposed system, the variation in k due to a free roaming mouse has led to the development of a linear regulator with very high (≤ -80 dB) line regulation. Therefore, this system can abide the variations on the power supply that the adaptive power control systems in [16] and [17] are designed to minimize. As a result, an adaptive power control system with significantly reduced complexity and simple on-chip implementation can be designed.

The on-chip implementation of this proposed system is straightforward, consisting only of a comparator that compares the output of the existing $V_{supply-L}$ detector to an existing reference level below the NMOS threshold. This reference level is chosen such that, for both fast and slow processes, the comparator does not trigger at $V_{supply-L}$ less than the minimum or more than the maximum voltage. The reference level is chosen to be 0.4 V in the prototype, leading to the comparator triggering at $V_{supply-L} = 2.8$ V. Using this configuration, a digital “power status” signal is produced by the comparator that is high when $V_{supply-L}$ is greater than the triggering level—indicating more than necessary power received by the implant—and low when $V_{supply-L}$ is less than the triggering level—indicating that sufficient or less than sufficient power is received by the implant.

The power status bit is sent by the on-chip transmitter along with other bio-signals data to an external receiver, where the data is decoded and processed. The power status bit then controls the adaptive power control system, shown in Figure 3.24. A digital n-bit counter is set to count either up or down every clock cycle—up when the power status bit is low (indicating sufficient or insufficient power) and down when the power status bit is high (indicating more than sufficient power). A D/A converter converts the counter signal into an analog voltage. The op-amp and BJT down-regulate V_{power} to supply a V_{DD} to the Class-E amplifier that is equal to the D/A converter output. A reduced Class-E V_{DD} reduces Class-E current consumption, thus reducing the total power consumed from V_{power} .

Figure 3.24: Adaptive power control external system

Figure 3.25: Illustration of adaptive power control signals

Figure 3.25 illustrates the operation of the adaptive power control system, based on system behavior as simulated in Matlab. When the coupling factor k decreases, the power coupled to the implant temporarily drops, causing the power data bit to remain low. This causes the Class-E V_{DD} , and thus the external input power drawn from V_{power} , to step up with each external clock cycle, restoring the desired power coupled to the implant. The opposite occurs when the coupling factor increases, conserving external power and

reducing cage floor temperature increase. When the coupling factor is constant, the power data bit alternates between a high and low state, causing a steady power with ripple to be supplied to the RF to DC electronics. The high line regulation and high low-frequency PSR of the 2 V regulator—required to suppress variations in the supplies due to mouse movement and changing k —suppresses the low frequency steady- k ripple from the adaptive powering system. The adaptive powering system must operate at sufficiently low frequency to fall within the high PSR range of the 2 V regulator, preventing this ripple from interfering with the outputs of the bio-sensors. The adaptive powering ripple is also aliased to 4 MHz due to the action of the rectifier. This higher frequency signal is a small variation ($< 5\%$) on the overall RF input magnitude, and is attenuated below significant levels due to the filter capacitor and the 4 MHz PSR of the regulator.

The selection of “ n ”—the number of bits used by the counter—is not a trivial choice. The number of discrete power levels that can be produced by the adaptive power control system is equal to 2^n , and problems can occur with too many or too few power levels. With too many bits, the counter would respond too slowly to changes in k , leading to short periods of power loss on the implant if k were to suddenly decrease. With too few bits, the discrete power levels are spaced so far apart that the implant may occasionally lose power altogether during steady state k . This would occur if a particular power level is too high—turning on the power data bit—but the next lower power level does not even provide the minimum necessary power, shutting off the implant.

The maximum variation on the implant voltage ($V_{supply-L}$) due to switching power levels is designed to be 250 mV, which ensures that the implant is never shut off as described above. Additionally, the adaptive power control system should be able to

switch from maximum to minimum power level between 1 and 0.1 seconds, which should provide sufficient speed to compensate for most mouse movement.

For simplicity of calculations, the following derivation of the optimum “n” and system speed will be carried out for a half-wave rectifier receiver with a constant load current, rather than a doubler. This approximation is quite accurate as, from Figure 3.4, $R_{ACload2} \gg R_{ACload1}$, making the doubler appear as a half-wave rectifier. Additionally, the limiter will not activate if the adaptive power control system is operational, meaning that a constant load current can be assumed. Furthermore, the adaptive power control aims to keep the average implant V_{supply} constant, so the average value will be used for these calculations.

The maximum V_{supply} variation occurs at maximum coupling efficiency, as will be illustrated in the following. Under maximum coupling efficiency, η_{max} , the Class-E amplifier V_{DD} is at a minimum, V_{DD-min} .

First, V_{supply} is calculated from the Class-E V_{DD-min} , where η_{max} is the maximum coupling efficiency, I_{load} is the on-chip load current, V_{drop} is the drop across the PN diode, and $R_{Class-E}$ is the Class-E amplifier’s equivalent DC resistance. $P_{class-E}$ is the power consumed by the Class-E amplifier, assuming 100 % efficient Class-E operation.

$$V_{supply} = \frac{P_{Class-E} \eta_{max}}{I_{load}} - V_{drop} = \frac{V_{DD-min}^2 \eta_{max}}{R_{Class-E} I_{load}} - V_{drop} \quad (3.28)$$

Next, the 1st-order partial derivative of (3.28) is taken to analyze the change in V_{supply} with respect to changes in V_{DD} . (It is assumed that η is constant. This is not the case; however variation in η between two adjacent V_{DD} steps is small and can be ignored for these calculations.)

$$\Delta V_{supply} = \frac{2 * V_{DD-min} \eta_{max}}{R_{Class-E} I_{load}} * \Delta V_{DD} \quad (3.29)$$

ΔV_{DD} is the change in the Class-E V_{DD} due to a single step of the adaptive power control, and can be calculated by:

$$\Delta V_{DD} = \frac{V_{DD-max}}{2^n}, \quad (3.30)$$

where 2^n is the number of discrete power levels and V_{DD-max} is the maximum necessary V_{DD} . V_{DD-max} can be calculated from the required implant power—a fixed value, due to fixed I_{load} and constant average V_{supply} —at minimum coupling efficiency η_{min} , as follows:

$$\begin{aligned} P_{implant-min} &= \frac{V_{DD-max}^2}{R_{Class-E}} * \eta_{min} = V_{supply} I_{load} \\ V_{DD-max} &= \sqrt{\frac{V_{supply} I_{load} R_{Class-E}}{\eta_{min}}} \end{aligned} \quad (3.31)$$

At maximum coupling efficiency η_{max} , the necessary V_{DD-min} is given by

$$V_{DD-min} = \frac{V_{DD-max}}{\sqrt{\eta_{max}/\eta_{min}}}. \quad (3.32)$$

Therefore, the variation in V_{supply} can be expressed as

$$\Delta V_{supply} = \frac{V_{DD-max}}{\sqrt{\eta_{max}/\eta_{min}}} \frac{2\eta_{max}}{R_{Class-E} I_{load}} * \frac{V_{DD-max}}{2^n} = \frac{2 * V_{supply}}{2^n} \sqrt{\frac{\eta_{max}}{\eta_{min}}}. \quad (3.33)$$

For an average V_{supply} of 3 V and a η_{max}/η_{min} ratio of 18.5, an n of 7—corresponding to 128 states—is determined from (3.33) to provide a worst-case ΔV_{supply} of less than 250 mV, as specified earlier. Setting the clock of counter in Figure 3.24 to 128 Hz with a 7-bit system provides sufficient operating speed to meet the 1 second transition from minimum to maximum power as specified above. Alternately, a speed of 1.28 kHz can be chosen to

decrease the maximum transition time to 0.1 seconds. Given a maximum ΔV_{supply} of 250 mV, the 2 V regulator must have a PSR of -62 dB or better at the chosen frequency to keep output variations under 200 μ V. In the prototype device, the PSR at 1.28 kHz is about -67 dB, however 128 Hz as the operational speed for this system to allow for a safety margin in future devices.

In this proposed system, the power consumed by the Class-E amplifier is controlled by modulating the V_{DD} supplied to the amplifier, as in Figure 3.24. An alternate method of power control is duty cycle variation, which involves decreasing the duty cycle of the clock of the Class-E amplifier (Figure 2.7) to reduce the power consumed by the Class-E amplifier. This method eliminates the BJT in Figure 3.24, which slightly increases the efficiency of the system by directly supplying the Class-E amplifier from the power supply.

As precise variations of the duty cycle are difficult, especially at 4 MHz given the large capacitive loading of the gate of the power transistor M_I in Figure 2.7, the system performance for varied duty cycle was simulated in SPICE. Figure 3.26 graphs the output power of the prototype Class-E amplifier as the duty cycle is decreased from 50 %, normalized against the output power at 50 % duty cycle. The Class-E amplifier is optimized for a 50 % duty cycle, however, so altering the duty cycle from 50 % reduces the efficiency of the amplifier. The effect of duty cycle variation on efficiency is graphed in Figure 3.27, normalized against the efficiency at 50 % duty cycle.

Figure 3.26: Normalized Class-E amplifier output power with varied clock duty cycle

Figure 3.27: Normalized Class-E amplifier efficiency with varied clock duty cycle

The efficiencies of the drop-out power control method and duty cycle variation method are compared in Figure 3.28. The efficiencies of each method are normalized

versus a 100 % efficient system and plotted versus power received by the implant to give a common comparison factor. As the duty cycle power control method offers only a few percent improvement in efficiency but requires much more complicated external control—including electronics that can cleanly vary the duty cycle at the gate of the power transistor with high accuracy—the voltage drop method is chosen as the adaptive power control method for this design.

Figure 3.28: Comparison of efficiency for adaptive power control techniques

3.6 Summary

In this chapter, the on-chip RF to DC electronics and coarse power control systems were introduced. The design objectives and requirements were determined first, following which the designs of individual blocks were presented. A dual regulator, dual output design, producing low and high V_{DD} output voltages, offers a number of system

benefits including power savings over a single output at the higher output level. A voltage-doubler rectifier provides a $V_{supply-H}$, $V_{supply-L}$, and GND to power the dual regulators. Using the multiple supplies from the voltage doubler, a low power, high line regulation linear regulator is designed to provide V_{DD} at 2 V DC to bio-sensing and signal processing electronics.

Coarse power control electronics are also designed to prevent on-chip device breakdown due to implant operation in high coupling regions. A traditional limiter was found to be unfeasible due to the high k variation from movement of the laboratory animal, and a detuning power control method was introduced to replace the limiter.

Finally, an adaptive power control scheme to reduce the power consumption of the external power amplifier was proposed. Due to the high line regulation of the linear regulator, the adaptive powering system is permitted to produce baseband variations on the Class-E output. The adaptive powering system can be designed and implemented much more simply than other similar systems due to the high line regulation of the linear regulator. As a result, an adaptive power control system was proposed which offers design advantages over other adaptive power control systems previously put forward in references [16], [17] and [18].

CHAPTER 4: MEASUREMENT RESULTS

4.1 Overview

The previously described components of the RF to DC powering system were constructed and fabricated as designed, and then tested and compared to the original specifications. The implementation of the full adaptive power control system is beyond the scope of this thesis, but the on-chip implementation was completed. This chapter presents the testing processes and results of each component. First, the remote RF powering system is tested, using a dummy load to represent the implant electronics. Next, the voltage doubler and implantable RF to DC converter are thoroughly characterized. Finally, the coarse power control systems are tested and characterized.

4.2 Testing of Remote RF Powering System

The remote RF powering system was constructed as described in Chapter 2. A Class-E amplifier was used to power a 25 cm x 15 cm, 4-turn, external coil, all tuned to 4 MHz. A 20-turn internal coil, also tuned to 4 MHz, was connected to a half-wave rectifier with a voltage drop of approximately 0.7 V, loaded with a DC resistance of 2.4 k Ω . This DC load presents an $R_{ac-load}$ of approximately 1.5 k Ω to the internal coil. Properly air-cooled, the Class-E amplifier can output a sustained power of 25 W without degrading in efficiency. Therefore, 25 W was used as the input power for this experiment. The DC load of 2.4 k Ω represents the worst case powering specification—an implantable system with an average current consumption of 1.25 mA at a DC supply of 3 V. Designing the

external system for an off-chip rectifier output of 3 V allows for the possibility of an on-chip rectifier drop-out voltage of up to 1.0 V—possible in a slow process.

The DC voltage across the load resistor was measured versus position for three horizontal paths across the 25 cm x 15 cm external coil area at a 1 cm vertical separation, for both a 0° and 60° tilt. Using the same measurement system used in Figure 2.12, Figure 2.13, and Figure 2.14, the three paths are: across the center of the operating region ($y = 7.5$ cm), the ‘far’ edge of the cage ($y = 12.5$ cm), and the ‘near’ edge of the cage ($y = 2.5$ cm). The measured voltages are plotted as points in the following graphs, alongside lines that indicate the predicted voltages from k measurements. In the graphs, the shaded vertical bars indicate measurements outside of the region defined by the cage, highlighting the effectiveness of reducing cage size on reducing coupling variation. The horizontal bar indicates the required output voltage of 3 V DC, as specified earlier.

Figure 4.1: Measured (points) and predicted (lines) RF powering DC output voltages for 0° tilt

Figure 4.2: Measured (points) and predicted (lines) DC output voltages for 60° x-direction tilt

As can be seen from the above graphs, Figure 4.1 and Figure 4.2, the required minimum output voltage of 3 V DC for a 2.4 k Ω load is met over the entire selected operating region. Additionally, the measured data points correspond closely with their predicted values. Reference [6] shows that, for this application, *in vivo* voltage measurements are the same as external measurements at the chosen operating frequency. Therefore, the results obtained here can be used as a design guideline for the ultimate *in vivo* system development.

The cage floor temperature increase is also a concern, as described in Chapter 1. The external coil and Class-E amplifier were powered at 25 W for 15 minutes, after which the temperature at multiple locations on the cage floor was measured. The temperature increase above the initial room temperature of the cage is graphed below in Figure 4.3. As before, the vertical shaded bars indicate data outside of the operating region.

Figure 4.3: Cage floor temperature increase over ambient for maximum external coil power

The temperature increase remains below 2° C for the Class-E amplifier running at maximum output, which is not dangerous for a bio-monitoring system. However, it is desirable to reduce the magnitude of this temperature increase as much as possible to minimize possible adverse effects on the laboratory animal—hence the use of high-efficiency electronics and the adaptive power control system.

4.3 Testing of Fine Power Control

The circuits described in Chapter 3 were laid out and fabricated in the 2-metal, 1-poly, AMI 1.5 μm CMOS process. The doubler rectifier, shown in Figure 3.5, was tested first by inputting an AC waveform at 4 MHz between the RF input and $V_{\text{supply-L}}$ nodes (corresponding to the location of the internal coil, though no internal coil was attached at this time). C_{filter2} was implemented on-chip as a poly-poly capacitor and has a value of 110 pF. C_{filter1} was implemented off-chip and thus can be changed as desired. For these tests, C_{filter1} has a value of 1 nF, sufficient to keep the $V_{\text{supply-L}}$ ripple under 250 mV for a load current of up to 1 mA. The regulator outputs were connected to on-chip

circuitry which consumed approximately 200 μ A. An AC input voltage at 4 MHz with a magnitude of 6.5 V_{pp} produced the following $V_{supply-L}$ and $V_{supply-H}$ DC levels and ripple magnitudes at the doubler output as shown in Figure 4.4 and Figure 4.5, respectively.

Figure 4.4: Doubler DC output levels with $C_{filter1} = 1$ nF, $C_{filter2} = 110$ pF, and $V_{RF} = 6.5$ V_{pp}

Figure 4.5: Doubler 4 MHz output ripple with $C_{filter1} = 1$ nF, $C_{filter2} = 110$ pF, and $V_{RF} = 6.5$ V_{pp}

As can be seen in the above figures, the doubler properly produces the desired minimum supply levels of $V_{supply-L} = 2.5$ V and $V_{supply-H} = 4.5$ V. Figure 4.4 suggests

doubler dropout voltages of about 0.7 V for D_1 and 1.2 V for D_2 (as seen in Figure 3.4), as expected. The large D_2 dropout is due to the significant V_{SB} increasing the transistor threshold voltage. Additionally, with the abovementioned filter capacitors, a ripple of approximately 30 mV_{pp} appears on each supply line as predicted by (3.1).

Figure 4.6: Regulator output voltages with $C_{filter1} = 1$ nF, $C_{filter2} = 110$ pF, and $V_{RF} = 6.5$ V_{pp}

Figure 4.7: Regulator 4 MHz output ripple with $C_{filter1} = 1$ nF, $C_{filter2} = 110$ pF, and $V_{RF} = 6.5$ V_{pp}

Figure 4.6 and Figure 4.7 show the 2 V and 3 V regulator outputs given the RF powering conditions mentioned earlier. It is observed that the startup circuits successfully

bootstrap the regulators and bandgap references into the proper operational states. As both regulator outputs are approximately 5% higher than designed, it is concluded that the bandgap reference is producing a $V_{bandgap}$ 5% higher than 1.2 V, or about 1.26 V. This increase causes no problems in the overall bio-sensing microsystem. For this particular implementation of the system, the 3 V regulator output was lowered to 2.5 V for easier interface with the on-chip VCO and FSK transmitter. The V_{DD-2V} ripple is about 4 mV, as expected, and the $V_{DD-2.5V}$ ripple is about 3 mV, as expected when the additional testing load capacitance is taken into account.

Under the same RF powering conditions described above, the output of the digital buffer from Section 3.4.10 was measured. The digital buffer supplies a $V_{DD-digital}$ to electronics including a finite state machine, switched capacitor controls, clock recovery, memory, and transmitter control. The finite state machine involves the largest number of switching digital gates and operates at 200 kHz. The DC level was measured to be 2.244 V, as expected due to the poorly controlled output level as described in Section 3.4.10. The measurement is shown in Figure 4.8, in which the 200 kHz finite state machine transitions can clearly be seen. The maximum spike in Figure 4.8 is 156 mV. Spikes above 200 mV were not measured, meeting the design requirements.

Figure 4.8: Digital buffer output noise due to switching digital gates

Next, the line regulation (DC PSR) of both regulators was tested. $V_{supply-L}$ and $V_{supply-H}$ were both provided by external DC power supplies to achieve highly accurate measurements. The supplies were then varied manually (using a 2:1 ratio between $V_{supply-H}$ and $V_{supply-L}$) from the minimum to maximum voltages (2.5 V to 4.5 V for $V_{supply-L}$ and 4.5 V to 8.5 V for $V_{supply-H}$). The 2 V and 2.5 V regulator output voltages were recorded for every 250 mV increase on $V_{supply-L}$ —which is the same as a 500 mV increase on $V_{supply-H}$. The results are graphed below in Figure 4.9 and Figure 4.10.

Figure 4.9: 2 V regulator output with $V_{supply-L}$ and $V_{supply-H}$ varied together. Best fit line and equation included.

Figure 4.10: 2.5 V regulator output with $V_{supply-L}$ and $V_{supply-H}$ varied together. Best fit line and equation included.

In the above graphs, the light data points indicate the regulator behavior with less than the minimum supply voltage. The dark points indicate the variation from the average V_{DD} in mV when $V_{supply-L}$ and $V_{supply-H}$ are varied. The 2 V regulator has a line regulation

of -91 dB against $V_{supply-H}$ (design target -86 dB), and the 2.5 V regulator has a line regulation of -51 dB against $V_{supply-H}$ (design target -40 dB).

The ability of the regulators to reject high frequency variations was also tested. To test this, a sine wave at a specific frequency was coupled to either $V_{supply-L}$ or $V_{supply-H}$. The resulting signals on the supply line and regulator output were both measured with a dynamic signal analyzer and compared to find the PSR at the test frequency. The results of this test are graphed below in Figure 4.11.

Figure 4.11: Measured PSR versus frequency for 2 V and 2.5 V regulators from both $V_{supply-L}$ and $V_{supply-H}$

These results match the expected trends for both regulators, and illustrate a 4 MHz ripple rejection of about -30 dB for the 2 V regulator and about -6 dB for the 2.5 V regulator. At frequencies below 2 kHz, the variation at regulator output becomes indistinguishable from the background noise as measured by a spectrum analyzer.

The regulator output noise floor was also measured using a signal analyzer. The measurements are shown in Figure 4.12 and Figure 4.13.

Figure 4.12: V_{DD-2V} noise floor ($1.7 \mu\text{V}/\sqrt{\text{Hz}}$)

Figure 4.13: $V_{DD-2.5V}$ noise floor ($2.2 \mu\text{V}/\sqrt{\text{Hz}}$)

The 2 V regulator has a measured noise floor of $1.7 \mu\text{V}/\sqrt{\text{Hz}}$. The requirements mentioned in Chapter 3 indicate a maximum acceptable V_{DD-2V} noise floor of $2.0 \mu\text{V}/\sqrt{\text{Hz}}$. The measured noise floor is slightly higher than the simulation level of $1.4 \mu\text{V}/\sqrt{\text{Hz}}$. This is due to the bandgap reference (Section 3.4.5) having an I_{BG} less than the design level of

1.5 μA but more than the worst case level of 1.0 μA . The 2.5 V regulator has a measured noise floor of 2.2 $\mu\text{V}/\sqrt{\text{Hz}}$.

4.4 Testing of Coarse Power Control

The abilities of the limiter and detuning power control methods to restrict the maximum $V_{\text{supply-L}}$ and $V_{\text{supply-H}}$ were tested. The off-chip implementation and testing of the adaptive power control is beyond the scope of this thesis, but the on-chip implementation was tested.

In order to test the coarse power control methods, the chip must be powered using inductive coupling. The 4-turn external coil and Class-E amplifier were set up and tuned to 4 MHz. A 20-turn internal coil was also constructed tuned to 4 MHz, and connected as in Figure 3.5, between the $V_{\text{supply-L}}$ and RF input nodes on the chip. The internal coil and IC chip were affixed in a high coupling region and not permitted to move with respect to the external coil. For each power control mechanism, the desired mechanism was enabled while the other power control mechanism was disabled. The Class-E input power was then varied from the minimum power necessary to provide minimum $V_{\text{supply-L}}$ and $V_{\text{supply-H}}$ (P_{min}) to 18.5 times that power—the total power variation over the operating region as described in Chapter 2.

The resulting $V_{\text{supply-L}}$ and $V_{\text{supply-H}}$ DC levels and ripple magnitudes were measured for various levels of Class-E power. Equation (3.1) was used to approximate the current consumption from each supply to further understand the effect of each power control method. It is known that (3.1) is only an approximation for small ripple/constant load, and becomes quite inaccurate for the large ripples and varying current load in these trials. The rough estimates from (3.1) are sufficient, however, to analyze trends and draw

comparisons between the limiter and detuning power control methods. Some key results are graphed below, versus the Class-E input power normalized against P_{min} (i.e. $P_{min} = 1$, $P_{max} = 18.5$).

Figure 4.14: Supply levels under normalized, varied input power using voltage limiter

Figure 4.15: Supply levels under normalized, varied input power using detuning control

The above two figures graph the measured $V_{supply-L}$ and $V_{supply-H}$ levels as the Class-E power is increased from P_{min} to $18.5 * P_{min}$. It is clear that both methods successfully limit the on-chip voltage levels, as $V_{supply-L}$ and $V_{supply-H}$ would be expected to

rise to at least 40 V and 70 V, respectively, without coarse power control. The major difference between the two power control methods is illustrated in the following two graphs.

Figure 4.16: Power received by implant versus normalized input power for coarse power control mechanisms

Figure 4.17: Expected V_{DD-2V} ripple for $C_{filter1} = C_{filter2} = 500$ pF for coarse power control mechanisms

Figure 4.16 illustrates the power received by the implant versus the input power. It can be seen that the detuning power control method successfully reduces the power

received by the implant while the limiter still receives full power and is forced to simply “burn off” the extra power on-chip. The result of this is seen in Figure 4.17, which graphs the ripple that would be expected at the 2 V regulator output given proper regulator operating with a $C_{filter1}$ and $C_{filter2}$ of 500 pF. Two filter capacitors of the same value are used in this comparison as the limiter and related detector draw current from $V_{supply-L}$ and the detuning power control detector draws current from $V_{supply-H}$. Using two filter capacitors of equal size allows the effects of the two coarse power control systems to be more easily compared.

In order to meet the design requirement of 25 mV_{pp} ripple at V_{DD-2V} using the voltage limiter power control, a total filter capacitance ($C_{filter1} + C_{filter2}$) of about 4 nF is necessary. In order to meet the same design requirement using the detuning power control, a total capacitance ($C_{filter1} + C_{filter2} + C_{detune}$) of only 200-500 pF is necessary, depending upon the current consumed by the bio-sensing electronics. It is feasible to implement a capacitance of 200-500 pF on-chip but unfeasible to implement 4 nF of capacitance on-chip. Therefore, the detuning power control should be used for coarse power control for a fully monolithic system implementation.

The off-chip implementation and verification of the intelligent power control system is beyond the scope of this thesis, and will not be described here. The on-chip circuitry successfully outputs the power data bit with a threshold of 2.75 V.

4.5 Summary

Table 4.1 summarizes the prototype system testing results.

Parameter	Design Value	Measurement
V_{DD-2V} Level	2.0 V	2.107 V
$V_{DD-2.5V}$ Level	2.5 V	2.53 V
$V_{DD-Digital}$ Level	2.0 V	2.24 V
Current Consumption: $V_{supply-L}$	20 μ A	18 μ A
Current Consumption: $V_{supply-H}$	16 μ A	13 μ A
Line Regulation: V_{DD-2V}	< -86 dB	-91 dB
Line Regulation: $V_{DD-2.5V}$	< -40 dB	-51 dB
Ripple Rejection: V_{DD-2V}	--	-25 dB
Ripple Rejection: $V_{DD-2.5V}$	--	-6 dB
Noise Floor: V_{DD-2V}	< 2.0 μ V/Hz ^{-1/2}	1.7 μ V/Hz ^{-1/2}
Digital Switching Spikes	< 500 mV	< 200 mV
Maximum $V_{supply-L}$, $V_{supply-H}$ (Limiter)	4.5 V / 8.5 V	2.9 V / 5.6 V
Maximum $V_{supply-L}$, $V_{supply-H}$ (Detuning)	4.5 V / 8.5 V	4.5 V / 7.7 V
Maximum Ripple: V_{DD-2V} (Detuning)	< 50 mV _{pp}	~25 mV _{pp}
Maximum Ripple: $V_{DD-2.5V}$ (Detuning)	< 250 mV _{pp}	~210 mV _{pp}
Cage Size	--	200 cm ²
Maximum Implant Tilt Angle	60°	60°

Table 4.1: Overall system testing results

In all categories, the remote RF powering system meets or exceeds the design requirements, providing well-controlled 2 V and 2.5 V outputs over a 200 cm² cage size for an implant tilt angle of up to 60°.

Filter capacitors of 1 nF for $C_{filter1}$ and 110 pF for $C_{filter2}$ were used, which reduced the worst-case output ripple to the levels noted above for the detuning power control. Under limiter power control with the mentioned capacitors, the $V_{supply-L}$ ripple increased to 1.69 V worst-case, and the 2 V and 2.5 V regulators failed to operate properly. Therefore, maximum ripple under limiter power control is not shown in Table 4.1.

CHAPTER 5: CONCLUSION AND FUTURE WORK

5.1 *Conclusion*

In this work, a miniature, implantable, remote RF powering system for a small, un-tethered laboratory animal inside a cage is developed. An external system consisting of a Class-E power amplifier driving a tuned 4-turn 15 cm x 25 cm square external coil is designed and optimized along with a tuned 20-turn 6 mm diameter internal coil to maximize power coupling efficiency. Microfabricated RF to DC electronics are designed that utilize a novel dual-supply and dual-regulator architecture to maximize PSR and stability while minimizing power consumption and eliminating the need for off-chip components. The dual regulators provide a 2 V supply with high line regulation to implant sensors and signal processing electronics as well as a low current 3 V supply for CMOS switches and an FSK VCO transmitter.

Optimization of the operating region via an analysis of the coupling constant, k , reduces the variation in mutual inductance of the remote powering system. Resizing the operating region (animal cage) to be smaller than the external coil and defined by measured peak coupling and minimal coupling zones reduces the k variation from 55 times to 4.25 times. This reduces the corresponding implant received power variation—proportional to k^2 —from a factor 3025 to a factor of 18.5. Reduced variation in implant received power minimizes system design complexity.

Fine power control is provided by the dual regulators. Low frequency variations on the sensitive 2 V supply line are restricted to $< 200 \mu\text{V}$ over the chosen operating region using a non-standard regulator architecture and dual supplies provided by the

voltage-doubler rectifier. Approximately 25 dB of ripple rejection is also achieved, and the total regulator output noise is less than 1 mV_{RMS} integrated from 1 Hz to 240 kHz. The total current consumption for both regulators is 31.5 μ A, which includes current consumption from feedback resistors, a digital buffer, startup circuits, and regulator op-amps and bandgap references.

Coarse power control is essential due to the high variation in coupling characteristic of the remote RF powering system. Reliable coarse power control is provided by an on-chip detuning power control system, which alters the resonant frequency of the internal coil to reduce power received by the implant. This system circumvents the problem of significant ripple increase which would be caused by the operation of a traditional on-chip power limiter system given the high variation in coupling.

An additional adaptive power control method is proposed which reduces external power consumption according to the power required by the implant. A single bit of power status data is produced with simple on-chip electronics and transmitted to an external receiver. The external receiver adjusts the Class-E power supply voltage at 128 Hz, either increasing or decreasing the power consumed by the Class-E amplifier according to the value of the power status bit. The 128 Hz variation falls within the high PSR band of the linear regulators, preventing interference with the bio-signals.

The final implantable device exhibits dimensions 6 mm x 6 mm x 2 mm and a mass of 100 mg including bio-compatible silicone coating. Stable 2 V and 3 V DC are supplied to the bio-sensing electronics over a 10 cm x 20 cm operating region with an implant tilt angle of up to 60°.

5.2 Future Work

The procedures described in this work can readily be applied to optimization of RF powering systems with different cage sizes, animal sizes, powering requirements, and tilting angles. Specifically, the procedures in Chapter 2 can be used to design and optimize a remote powering system for a larger cage containing multiple (or larger) animals, as is often desired in biomedical research. Additionally, for a implant system with sufficiently low power consumption, there exists the possibility of operating at frequencies in the 10 MHz to 100 MHz range. A smaller, high frequency internal coil would then be used along with a much smaller tuning capacitor, possibly implemented on-chip—eliminating the need for off-chip capacitors altogether. Care would need to be taken to avoid unacceptable coupling losses due to the RF absorption of animal tissue at frequencies near 100 MHz.

The AMI 1.5 μm CMOS process used to fabricate this prototype yields large parasitic capacitances and digital blocks that occupy large portions of silicon area. A more modern process would leave additional room for implementation of the filter capacitors on-chip. A different process may also allow larger value feedback resistors to be used, especially with a high resistance poly layer, leading to significantly decreased regulator and detector current consumption. The reduced parasitic and load capacitance would also simplify the design of the 3 V regulator (by reducing C_p and C_{out} in Section 3.4.9) and the digital buffer (by reducing $C_{digital}$), yielding reduced current consumption in these devices, as well.

The adaptively controlled powering system is desirable for a remote RF powering application. The theory presented here and the on-chip implementation in the prototype

should be expanded to a full, closed-loop system by way of the external circuitry described in Chapter 3. This would yield an overall system with significantly increased efficiency and reduced environmental temperature increase.

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