VOLTAGE HARMONIC CONTROL OF WEAK UTILITY GRID
THROUGH DISTRIBUTED ENERGY SYSTEMS

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VOLTAGE HARMONIC CONTROL OF WEAK UTILITY GRID
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Thesis

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ABSTRACT

This thesis proposes a closed loop control method to reduce the voltage harmonics of the weak utility grid through distributed energy systems (DES). It is desired to have uniform voltage and frequency around the grid. Because of the nonlinear behavior of the distributed loads and sources, the voltage of the utility gets distorted. It would be possible to correct the distorted utility grid locally where the DESs get connected. The proposed method imposes the extra responsibility on the DES of estimating the grid voltage harmonics and injecting additional current to rectify the pollution in the grid voltage. Recursive Least Squares Estimation (RLSE) technique has been implemented to estimate the grid voltage harmonics, this estimation technique works harmoniously with closed loop harmonic voltage controller. DES with the proposed control technique reduces the voltage harmonics and provides sustainable energy to the utility grid. The results are verified with simulation and experimental tests on a 5kW utility interactive energy conversion system.

KEY WORDS: Distributed Energy Sources, Recursive Least Square Estimation, Voltage Harmonic Control.

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TABLE OF CONTENTS

	Page
LIST OF TABLES.....	viii
LIST OF FIGURES	ix
CHAPTER	
I. INTRODUCTION.....	1
1.1 Background work	1
1.2 Motivation to research	6
1.3 Thesis organization	9
II. UTILITY INTERACTIVE INVERTER.....	10
2.1 Introduction	10
2.2 Single phase utility interactive inverter topology	10
2.3 Grid interface of utility interactive inverter	12
2.4 Utility phase detection algorithm (Phase locked loop (PLL))	13
2.4.1 Loop filter design for the PLL algorithm	15
2.5 Current control algorithm for utility interactive inverter	15
2.5.1 Design of PI current controller for utility interactive inverters.....	17

2.6	Voltage control algorithm	21
2.7	PWM generation algorithm	23
2.8	Summary	24
III. VOLTAGE HARMONIC CONTROL.....		25
3.1	Introduction	25
3.2	Voltage harmonic control	25
3.3	Measurement of grid harmonics through RLSE method	27
3.4	Voltage harmonic control algorithm	33
3.4.1	Synchronous rotating frame transformation	34
3.5	Controller algorithm design	35
3.5.1	3 rd Harmonic controller design	35
3.5.2	5 th Harmonic controller design	37
3.6	Harmonic control selection	40
3.7	Summary	40
IV. SIMULATION RESULTS.....		41
4.1	Introduction	41
4.2	Simulation setup	41

4.3	Simulation results	43
4.3.1	Grid synchronization using PLL	43
4.3.2	Injection of active/reactive power into utility grid	45
4.3.3	Power flow from grid to inverter (Charging)	51
4.3.4	Injecting active and reactive power utility grid with delay in measurement	53
4.3.5	Active and reactive power injection into the utility grid with delay and updated gains	56
4.3.6	Active and reactive power injection into utility grid in the presence of local load	59
4.3.7	Standalone mode operation of utility interactive inverter	64
4.4	Harmonic voltage control in the weak utility grid	65
4.5	Estimation of the harmonics in utility grid voltage	65
4.6	Voltage harmonic control in weak utility grid	69
4.6.1	Combination of voltage harmonic controllers	77
4.6.2	Active power injection with 3 rd and 5 th harmonic control	81
4.7	Summary	83

V. EXPERIMENTAL SETUP.....	84
5.0 Introduction	84
5.1 Experimental setup	84
5.1.1 Power section	85
5.1.2 Interface board	85
5.1.3 Relay driver circuit	87
5.1.4 Voltage sensor circuit	88
5.1.5 Sensor conditioning circuitry	88
5.1.6 PWM interface circuitry	89
5.1.7 Fault protection circuitry	91
5.2 Digital signal processor	92
5.3 Summary	94
VI. EXPERIMENTAL RESULTS.....	95
6.1 Introduction	95
6.2 Testing of bi-directional inverter	95
6.2.1 Grid synchronization testing.....	96
6.2.2 Active and reactive power injection into utility grid	98

6.2.3	Power flow from grid to DC side (Charging)	103
6.2.4	Standalone mode of inverter operation	105
6.3	Voltage harmonic control in weak utility grid	107
6.3.1	Harmonic measurement of utility grid voltage	107
6.4	Utility grid voltage harmonic control without active power injection...	111
6.5	Utility grid voltage harmonic control with active power injection	117
6.6	Summary	123
VII CONCLUSION AND FUTURE WORK.....		125
7.1	Conclusion	125
7.2	Future work	126
BIBLIOGRAPHY		127
APPENDICES.....		130
APPENDIX A. CONTROL ALGORITHM IN C/C++		131
APPENDIX B. PCB LAYOUT AND SCHEMATICS		167

LIST OF TABLES

Table	Page
1.1 Harmonic frequencies and magnitudes.....	9
2.1 Inverter switch status and Output voltage	11
8.1 Simulation and experimental results	126

LIST OF FIGURES

Figure	Page
1.1 (a) UG voltage waveform	8
1.1 (b) FFT analysis of the UG voltage.....	8
2.1 Single phase converter topology	10
2.2 Single phase grid interface inverter	12
2.3 PLL of single phase system	13
2.4 Block diagram of closed loop system	17
2.5 Bode plot of the current controller	18
2.6 d-q axis current control algorithm	19
2.7 System block diagram with transportation delay	20
2.8 Bode plot of the delayed system	20
2.9 Bode plot of the system with updated controller	21
2.10 RMS voltage control algorithm	22
2.11 Standalone mode of operation of inverter	23

2.12	PWM generation unit	24
3.1	Weak utility grid system diagram	26
3.2	RLS control algorithm for harmonic estimation in utility grid voltage	27
3.3	Control algorithm for active/reactive and harmonic control	33
3.4	3 rd harmonic control in $d-q$ synchronous rotating frame using PI controller ...	36
3.5	5 th harmonic elimination control algorithm	37
3.6	All voltage harmonic control in the weak utility grid	39
3.7	Control algorithm of harmonic selection	40
4.1	Nonlinear load connected to single phase utility grid	42
4.2	Phase Locked Loop results	44
4.3	PLL results of utility grid voltage with harmonics	45
4.4	Active power injection into utility grid during transient ($I_d_ref = 50$ A and $I_q_ref = 0$ A)	46
4.5	Active power injection into utility grid at steady state ($I_d_ref = 50$ A and $I_q_ref = 0$ A)	47
4.6	Active and reactive power injection into utility grid at steady state ($I_d_ref = 25$ A, $I_q_ref = 25$ A)	48

4.7	Active and reactive power injection into utility grid ($I_{d_ref} = 25$ A, $I_{q_ref} = 25$ A) D-axis and Q- axis values of inverter output current	49
4.8	Reactive power injection into utility grid at steady state ($I_{d_ref} = 0$ A and $I_{q_ref} = 50$ A)	50
4.9	Battery charging ($I_{d_ref} = -40$ A and $I_{q_ref} = 0$ A)	52
4.10	Active and reactive power injection into utility grid when there is delay in the measurement ($I_{d_ref} = 30$ A, $I_{q_ref} = 20$ A)	54
4.11	Battery charging with delay in the measurement ($I_{d_ref} = -40$ A and $I_{q_ref} = 0$ A)	55
4.12	Active and reactive power injection into utility grid with updated controller ($I_{d_ref} = 30$ A and $I_{q_ref} = 20$ A)	57
4.13	Charging battery from single phase utility grid with updated controller ($I_{d_ref} = -40$ A and $I_{q_ref} = 0$ A)	58
4.14	Active and reactive power injection into utility grid when the local loads are connected ($I_{d_ref} = 40$ A, $I_{q_ref} = 10$ A)	60
4.15	Active and reactive power injection into utility grid in the presence of local loads ($I_{d_ref} = 40$ A, $I_{q_ref} = 10$ A) currents	61
4.16	Charging battery when local loads are connected ($I_{d_ref} = -40$ A, $I_{q_ref} = 0$ A)	62

4.17	Charging battery when the local loads are connected ($I_d_{ref} = -40$ A, $I_q_{ref} = 0$ A) currents	63
4.18	Standalone mode of utility interactive inverter operation	64
4.19	Voltage of single phase weak utility grid	65
4.20	Fundamental component of single phase utility grid voltage	66
4.21	3 rd harmonic measurement of single phase utility grid voltage	67
4.22	5 th harmonic measurement of single phase utility grid voltage	67
4.23	7 th harmonic measurement of single phase utility grid voltage	68
4.24	9 th harmonic measurement of single phase utility grid voltage	68
4.25	Harmonic analysis of single phase utility grid voltage	69
4.26	3 rd harmonic control in d-q synchronous rotating frame	70
4.27	Harmonic analysis of utility grid voltage after 3 rd harmonic control	71
4.28	PWM output of the 3 rd voltage harmonic control algorithm	71
4.29	5 th harmonic control in d-q synchronous rotating frame	72
4.30	Harmonic analysis of utility grid voltage after 5 th harmonic control	73
4.31	7 th harmonic control in d-q synchronous rotating frame	74
4.32	Harmonic analysis of utility grid voltage after 7 th harmonic control	75

4.33	9 th harmonic control in d-q synchronous rotating frame	76
4.34	Harmonic analysis of utility grid voltage after 9 th harmonic control	77
4.35	3 rd and 5 th harmonic control in d-q synchronous rotating frame	78
4.36	Harmonic analysis of utility grid voltage after 3 rd and 5 th harmonic control.....	79
4.37	Controlling all harmonics in d-q synchronous rotating frame	80
4.38	Harmonic analysis of utility grid voltage after controlling all harmonics	81
4.39	Active power, 3 rd harmonic and 5 th harmonic control in d-q synchronous rotating frame	82
4.40	Harmonic analysis of utility grid voltage after active power, 3 rd harmonic and 5 th harmonic control	83
5.1	Experimental setup	85
5.2	Grid interactive inverter setup	86
5.3	Relay driving circuit	87
5.4	Voltage isolation amplifier AD202 to measure voltage	88
5.5	Processing sensor data using AD713	88
5.6	PWM level shifter and buffer circuit	90
5.7	Fault protection circuit	91
6.1	Phase Locked Loop results	97

6.2	Active power injection into utility grid ($I_{d_ref} = 22$ A and $I_{q_ref} = 0$ A)	99
6.3	Steady state error analysis between reference and actual currents	100
6.4	Active and reactive power injection into utility grid ($I_{d_ref} = 20$ A, $I_{q_ref} = 17$ A)	101
6.5	Reactive power injection into utility grid ($I_{d_ref} = 0$ A, $I_{q_ref} = 20$ A)	102
6.6	Battery charging ($I_{d_ref} = -17$ A and $I_{q_ref} = 0$ A	103
6.7	Charging: battery current for $I_{d_ref} = -17$ A	104
6.8	Standalone mode of inverter operation	106
6.9	Weak utility grid voltage	107
6.10	Fundamental component of utility grid voltage	108
6.11	3 rd harmonic measurement of utility grid voltage	108
6.12	5 th harmonic measurement of utility grid voltage	109
6.13	7 th harmonic measurement of utility grid voltage	109
6.14	9 th harmonic measurement of utility grid voltage	110
6.15	Harmonic analysis of the utility grid voltage	110
6.16	3 rd harmonic control in d-q frame	112
6.17	Harmonic analysis of utility grid voltage after 3 rd harmonic control	113

6.18	5 th harmonic control in d-q frame	114
6.19	Harmonic analysis of utility grid voltage after 5 th harmonic control	115
6.20	3 rd and 5 th harmonic control in d-q frame	116
6.21	Harmonic analysis of utility grid voltage after 3 rd and 5 th harmonic control	117
6.22	3 rd harmonic in utility grid voltage with active power	118
6.23	Harmonic analysis of utility grid voltage after 3 rd harmonic and active/reactive power control	119
6.24	5 th harmonic in utility grid voltage with active power	120
6.25	Harmonic analysis of utility grid voltage after 5 th harmonic and active power control	121
6.26	Active power and 3 rd and 5 th harmonic control	122
6.27	Harmonic analysis of utility grid voltage after 3 rd harmonic, 5 th harmonic and active/reactive power control	123

CHAPTER I

INTRODUCTION

1.1 Background Work

According to the first law of thermo dynamics “Energy cannot be created or destroyed.” It can only be converted from one form to another form, rather than being consumed. Some energy conversion processes result in gasses and particles that pollute the environment and threaten human health. The price of conventional energy sources also keeps increasing. Because of the above reasons, government and private agencies have been looking for alternate energy sources where the energy comes from sunlight, wind, tides and geothermal sources. Now, about 16% of global energy is produced from renewable energy sources (RESs), and enormous progress has been made in the development of RESs in the last decade.

RESs have strong daily and seasonal patterns, for example solar energy is only available during daytime, and wind energy sources have been affected by the weather conditions and the season. The RESs instantaneous power production does not always match with a user power requirement. In order to filter the fluctuation in the power provided by the RESs, the utility grid (UG) needs to be connected at the point where the RESs interact with loads. The applications of power electronics in RESs, especially photovoltaic and wind turbine systems are increasing. Power electronics significantly

improve performance of RESs by controlling frequency and voltage by means of active and reactive power control [1]. RESs are typically interfaced to power system networks at the distribution level. The power electronic technology plays a vital role in integrating the RESs to the UG. Because of recent improvements in power electronic technology, wind power and photo voltaic (PV) systems are becoming interesting alternatives to the primary power generation systems [2]. Wind power generation systems, offshore wind farms, fuel cells and PV cells are the few examples of latest technologies in the RESs. Different interfacing power electronic technologies are developed for the interfacing of the RESs such as multi-string inverters, ac modules, and single cell converters [3].

There are many technical challenges in interfacing the RESs to the UG. These small RESs are called distributed generators (DG), which are integrated to the UG to inject active and reactive power to the UG. Many algorithms are developed to model and control the DG systems in grid-connected (GC) mode and in standalone (SA) mode. The utility interactive inverters are synchronized to the UG through a phase locked loop (PLL). When a DG is connected to the UG, the DG runs in GC mode, and when the UG is not available it can run in SA mode. The DG terminal voltage is controlled through the voltage control (VC) technique when the system is in the SA mode. The active and reactive power control is done through the current control (CC) in GC operation [4]. The performance of the CC and VC techniques are important in maintaining the quality of the UG voltage. Five requirements for the CC and VC techniques can be summarized as:

- (1) Zero steady state error over a wide range of power level,
- (2) High dynamic response in critical conditions,

- (3) Constant Switching frequency throughout the operation,
- (4) Maximum DC link voltage utilization,
- (5) Low Total Harmonic Distortion (THD).

Depending on the above requirements and the performance criteria, many CC and VC techniques are developed and they are mainly classified into two categories. Stationary PI control, synchronous vector control (PI), state feedback control, predictive control and deadbeat control fall into one category called “Linear Control”. Hysteresis, pulse density modulation, on-line optimized controls are examples of “Nonlinear Control”. Recent trends in the development of CC and VC techniques suggesting that easy digital implementation of algorithms are preferred with some sacrifice in performance and accuracy. For low performance applications, PI controllers are better. On the other hand predictive and on-line optimized CC and VC techniques are used for medium and high performance applications. Hysteresis band controllers are used for fast and accurate converter systems [5].

Although the main purpose of the DG based on RESs is to process power into the UG, by the proper control of the power electronic interfacing system we can use them for other purposes at the same time. Minimizing grid voltage harmonics, power conditioning, VAR control and voltage regulation can be done through the RESs inverters as a secondary outcome [6]. The performance of the DG system is affected by the stiffness and the harmonic content of the UG. There are many disadvantages of having high order frequency components in the power system. Hence such research is being done to estimate the harmonic content of the UG voltage and control the harmonics [7].

There are some technical challenges in identifying the harmonic flow in the power system. It is a challenging task to identify whether the power system harmonics are flowing upstream or downstream at a particular location. We can only identify the flow of the harmonics by measuring the phase angle difference between the particular harmonic current and the voltage, but as the power system impedance is primarily an inductive impedance, the phase difference approaches 90 degrees for higher frequencies. Hence, we must use higher resolution Analog to Digital Converters (ADC) to measure the phase angle difference to reduce the effect of the measurement errors in estimating the harmonic content of the UG voltage [8].

Due to the increased use of the power electronic converters in the power system industry, the high frequency switching of the power electronic components contribute to the quality of the UG voltage. It is easy to measure the known harmonics in the system, but we cannot identify the unknown harmonic sources effectively. Many techniques are developed to identify the unknown harmonics. One of them is a computer program called “HARMIND” identifies the flow of harmonics in a radial distribution system. It also traces the exact location of the harmonic sources and reexamines the propagation and assesses the impact of the harmonics [9]. There are many techniques available to measure the UG harmonics. These techniques can be summarized as:

- Methods based on synchronous harmonic d-q frame,
- Methods based instantaneous power theory,
- Methods based on generalized integrators,
- Enhanced PLL based methods are time domain techniques.

In the frequency domain, the Fast Fourier Transform (FFT), Discrete Fourier Transform (DFT) and Recursive DFT (RDFT) are the most used techniques. Advanced techniques such as the neural network technique, fuzzy logic control, adaptive signal processing and sliding mode control are also used to measure the power system harmonics [10]. Most of the techniques used to measure the THD are not able to extract the individual harmonic components. The FFT gives individual measurements of the harmonic components, but when the system fundamental frequency change, the accuracy of the estimation deteriorates significantly. Using the frequency interpolation technique we can obtain better results when the system fundamental frequency varies, and an improved FFT method is developed based on the same concept [11]. An improved FFT method gives improved solution accuracy for online measurement of the harmonics, but the computational efficiency is low.

Earlier, conventional passive filters have been used to eliminate the harmonics in the power distribution system. In recent decades, many filters have been developed using power elements such as resistors, inductors and capacitors combinations. Conventional filters have disadvantages in terms of size and efficiency. To eliminate these problems, active power filters (APFs) are developed based on measuring the current in the power line, and few APFs are developed based on the voltage measurement. The APFs are classified into two types: (1) Pure APFs (PAPFs), and (2) Hybrid APFs (HAPFs) [12] which are a combination of APFs and the power elements. The primary purpose of the PAPFs is to eliminate the power system harmonics, but they can also be used for power conditioning. For high power rated power system networks, the rating of the PAPFs is very high. The power ratings can be reduced using HAPFs, however when using HAPFs,

the size of the filters increases, hence much work has been done to reduce the size and cost of the filters using existing capacitor banks in systems [13]. The HAPFs cannot be used for power conditioning, because we cannot control the active and reactive power of the filters.

Many algorithms are developed to reduce the power system harmonics both selective harmonics and total harmonics. Algorithms are developed to eliminate selective harmonics, in the $d - q$ axis frame and the $\alpha - \beta$ axis frame using instantaneous and the RMS control [17]. A conventional PI controller can be used to control the selected harmonic, but it gives unstable results for unbalanced systems. Stationary-frame generalized integrators give zero steady state error for the specified current harmonic elimination for both balanced and unbalanced system. Generally in this kind of controller, the reference is generated based on instantaneous reactive power theory [18].

We propose to use the RESs to inject the harmonics into the UG to reduce its harmonic content. The grid has harmonics because of nonlinear currents drawn by local nonlinear loads such as rectifiers, furnaces, computers, discharge lamps, etc. If we can supply nonlinear current through RESs to the UG we would be able to cancel the effects of the nonlinear loads.

1.2 Motivation to research

The reduced cost of the fast switching semiconductor devices along with high speed and exceptional performance of digital signal processors have increased the use of the RESs integration into the UG. The harmonic content and the stiffness of the UG make the UG interface challenging.

Figure 1 (a) shows the UG voltage waveform in the lab. Here, we can clearly observe that the UG is quite distorted. An FFT of the UG voltage is shown in Figure 1.1 (b). From the FFT analysis of the UG voltage, it is observed that the voltage THD is 5.68%. As provided in the Table 1.1, 3rd, 5th, 7th, 9th, 11th, 13th and 15th are the major harmonics. Table 1.1 gives the harmonic magnitude, phase angle and their percentage of the fundamental magnitude.

There has been research in reducing the effect of nonlinear loads using active filters. Active filters are standalone devices injecting higher order currents to cancel the effects of the nonlinear loads. If there is no harmonic current being injected into the grid due to the nonlinear loads at the point where the active filters are connected, then the active filters would not do any work for the grid to reduce voltage harmonics. We are proposing the measurement of the voltage harmonics of the UG and correcting them through DES inverters. DES inverters by nature are capable of injecting higher order harmonics as commanded. If we can augment the DES inverter controllers to inject higher order harmonic currents as well injecting real and reactive power at the fundamental frequency we would be able to correct the polluted grid voltage.

On-line measurement of the voltage harmonics is a key in developing the control algorithm to cancel them. The digital realization, solution accuracy, and computational efficiency play a major factor in using an algorithm for measuring harmonics. The FFT and DFT produce accurate results for low frequency operating systems, but we cannot use them for high switching frequency systems because of very low computational efficiency. Other methods such as d-q axis and PLL work at higher frequency. These algorithms measure total harmonics of the system together, and it is difficult to measure

the individual harmonics. Consequently, we have to use digital filters to obtain the individual harmonics which introduce more computations. In this work, an estimation algorithm has been developed in the stationary reference frame and converted into the rotating ($d-q$) reference frame. The RLSE algorithm is adapted as the UG voltage harmonics estimator. Developing the control in the $d-q$ reference frame has the advantage of designing a closed loop controller independent of the utility phase.

Figure 1.1 (a): UG voltage waveform

Figure 1.1 (b): FFT analysis of the UG voltage.

Table 1: Harmonic frequencies and magnitudes

Harmonic order	Magnitude (Peak)	Phase angle (°)	% Of fundamental
Fundamental	165.44	19.3°	100
3	5.89	118.5°	3.56
5	3.70	0.0°	2.24
7	1.30	143.2°	0.78
9	0.66	0.0°	0.40
11	0.87	27.8°	0.53
13	0.30	23.7°	0.18
15	0.44	56.5°	0.26

1.3 Thesis organization

Operation and control of the UG interactive inverter is presented in Chapter II. The UG voltage harmonic measurement, analysis of harmonics, and control algorithm design of the harmonic control is presented in Chapter III. The simulation results are presented in Chapter IV. The experimental hardware and the software setup are presented in Chapter V. In chapter VI, the experimental results are presented. Finally the conclusion and the future work are provided in Chapter VII.

CHAPTER II

UTILITY INTERACTIVE INVERTER

2.1 Introduction

The grid interface of a utility interactive inverter with utility phase estimation, current control and voltage control algorithms are discussed in this chapter. The standalone mode of operation when the utility grid is not available and the bi-directional active and reactive power control are provided for typical applications.

2.2 Single phase utility interactive inverter topology

The power converter which converts the DC form of electric power into an AC form is called an inverter as shown in Figure 2.1.

Figure 2.1: Single phase converter topology

The AC voltage can be synthesized from the DC voltage source by properly changing the status of the switches between ON and OFF. The output voltage of the inverter can be $+V_{dc}$, $-V_{dc}$ or zero depending on the status of the switches.

Table 2.1: Inverter switch status and corresponding output voltage

Switches turned ON	Output voltage (V_{inv})
S1 and S4	$+V_{dc}$
S2 and S3	$-V_{dc}$
S1 and S3	0
S2 and S4	0

The IGBTs or MOSFETs cannot turn on and off instantly. They require some transition time to physically change the status. So, we have to rest in between changing the status of the switches. This accommodated time is called “Dead Time”.

An inverter output voltage is a pulse stream of DC voltage levels. An inductor is typically used to filter the switching frequency component from the inverter output voltage. The switching frequency of the inverter, the magnitude and the fundamental frequency of the inverter output, and the desired amount of ripple dictates the inductor design.

2.3 Grid interface of the utility interactive inverters

Figure 2.2 shows the utility interface inverter being connected to the utility grid through an inductive filter (L) at the point of common connection (PCC). The main aim of the utility interactive RESs inverter is to extract maximum power from the energy sources. This inverter converts the DC power generated from the RESs into AC power to be compatible with the AC UG. Depending on the inverter control, it is possible to achieve a bi-directional power flow if the DC side can absorb the power provided by the AC side of the inverter. This capability is useful for battery storage and Vehicle to Grid systems.

Figure 2.2: Single phase grid interface inverter

2.4 Utility phase detection algorithm (Phase locked loop (PLL))

The grid connection of the inverter is achieved through the synchronization of inverter to the utility grid. A Phase locked loop (PLL) algorithm is one of the most popular ways to track the phase and the frequency of the utility grid. The PLL should respond quickly to changes in the utility voltage and also reject higher order harmonics and noise. The zero crossing method is one of the simplest methods to track the grid phase, but as it only works for every half cycle of the utility frequency, fast tracking of the system phase is not achieved. Figure 2.3 shows the block diagram of the PLL algorithm.

Figure 2.3: PLL of single phase system

Phase voltages are transformed into the $\alpha - \beta$ reference frame as shown in Equation 2.1,

$$V_{\alpha\beta} = T_s \cdot V_{abc} , \quad 2.1$$

where

$$V_{abc} = \begin{pmatrix} V_m \cos(\theta) \\ V_m \cos(\theta - \frac{2\pi}{3}) \\ V_m \cos(\theta + \frac{2\pi}{3}) \end{pmatrix}, \quad 2.2$$

$$T_s = \begin{pmatrix} 1 & -\frac{1}{2} & \frac{1}{2} \\ 2 & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \end{pmatrix}, \quad 2.3$$

$$V_{\alpha\beta} = [V_\alpha \ , \ V_\beta]^T. \quad 2.4$$

For a single-phase system the $\alpha - \beta$ transformation is obtained through Equation 2.5.

$$\begin{aligned} V_\alpha &= V_g = V_m \cos(\theta), \\ V_\beta &= V_g(\theta - \frac{\pi}{2}) = V_m \sin(\theta), \end{aligned} \quad 2.5$$

where the two phase voltage is generated by augmenting the utility grid voltage. Once $V_{\alpha\beta}$ is computed, V_{dq} is calculated using Equation 2.6

$$V_{dq} = T_{dq}(\hat{\theta}) V_{\alpha\beta}, \quad 2.6$$

where $T_{dq}(\hat{\theta}) = \begin{pmatrix} \cos \hat{\theta} & -\sin \hat{\theta} \\ \sin \hat{\theta} & \cos \hat{\theta} \end{pmatrix}, \quad 2.7$

$$V_{dq} = [V_d \ V_q], \quad 2.8$$

$$V_q = V_m \cos(\hat{\theta} - \theta), \quad 2.9$$

$$V_d = V_m \sin(\hat{\theta} - \theta). \quad 2.10$$

For small phase angle error, $\sin(\varnothing) = \varnothing$ then $V_d = V_m(\hat{\theta} - \theta) \quad 2.11$

2.4.1 Loop filter design for the PLL algorithm

The phase estimation is locked to the utility when V_d goes to zero. The compensation is done through the loop filter given in Equation 2.12

$$K_f(s) = K_f + \frac{K_i}{s} = K_p \left(\frac{1+s\tau}{s\tau} \right) \quad 2.12$$

where K_p and K_i are the PI controller constants, and τ is the equivalent time constant.

The transfer function of a PI controller is shown in Equation 2.12. It is compared to standard second order closed loop system to get the controller parameters proportional gain (K_p) and integral gain (K_i).

The standard second order closed loop transfer function of a system is

$$H(s) = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad 2.13$$

In Equation 2.13, ζ is the damping ratio and ω_n is the natural frequency of the system. By comparing the above transfer function to the closed loop PI controller, we get the following Equations 2.14 and 2.15

$$\omega_n = \frac{K_p V_m}{\tau} \quad 2.14$$

$$\zeta = \frac{K_p V_m}{2\omega_n} = \sqrt{\frac{\tau K_p V_m}{2}}. \quad 2.15$$

2.5 Current control algorithm for utility interactive inverter

The maximum power extraction (utilizing a DC source) from the RESs depends mainly on the current controller. Zero steady state error, fast dynamic response, constant

switching and the low Total Harmonic Distortion (THD) are desired performances expected from the current regulators. It is easy to control the steady state error of the system in the $d - q$ reference frame as the sinusoidal currents are converted into DC values. The electrical dynamics of the UG inverter in the $d - q$ axis are as shown in Equations 2.16 and 2.17,

$$v_d(t) = Ri_d(t) + L \frac{di_d(t)}{dt} - \omega Li_q(t) + e_d(t) \quad 2.16$$

$$v_q(t) = Ri_q(t) + L \frac{di_q(t)}{dt} - \omega Li_d(t) + e_q(t) \quad 2.17$$

where $v_d(t), v_q(t)$ are the d and q-axis voltages, $i_d(t)$ and $i_q(t)$ are the d and q-axis currents, $\omega Li_d(t)$ and $\omega Li_q(t)$ are the cross coupling terms, $e_d(t)$ and $e_q(t)$ are the feed forward terms and R and L are the resistance and inductance of the system respectively.

After feed forward compensation and decoupling, the linear model of the plant becomes as shown in Equations 2.18 and 2.19

$$v_d(t) = Ri_d(t) + L \frac{di_d(t)}{dt} \quad 2.18$$

$$v_q(t) = Ri_q(t) + L \frac{di_q(t)}{dt}. \quad 2.19$$

From Equations 2.18 and 2.19 we can get the transfer function of the system as shown below

$$G(s) = \frac{1}{sL+R} = \frac{1/R}{s(L/R)+1} = \frac{V_d}{I_d}.$$

2.20

The transfer function of a PI controller in the s domain is as shown in Equation 2.21

$$D(s) = K_p + \frac{K_i}{s} = \frac{K_p s + K_i}{s} \quad 2.21$$

where K_p and K_i are the proportional and integral gains of the controller respectively.

Figure 2.4 shows the closed-loop diagram of the plant and PI controller. The closed loop transfer function of the system $H(s)$ is shown in Equations 2.22 and 2.23

Figure 2.4: Block diagram of closed loop system.

$$H(s) = \frac{G(s)D(s)}{1+G(s)D(s)} \quad 2.22$$

$$H(s) = \frac{K_p s + K_i}{s^2 + s\left(\frac{R+K_p}{L}\right) + \frac{K_i}{L}} \quad 2.23$$

2.5.1 Design of a PI current controller for utility interactive inverters

The standard second order closed-loop transfer function of a system is shown in Equation 2.13. Comparing the closed-loop transfer function of the system with Equation 2.23, we will get the following Equations

$$\omega_n^2 = \frac{K_i}{L} \quad 2.24$$

$$2\zeta\omega_n = \frac{R+K_p}{L}. \quad 2.25$$

The bandwidth of the system depends on the settling time T_s and damping ratio ζ and can be represented as $\omega_n = \frac{4}{\zeta T_s}$ 2.26

K_p and K_i can be calculated from Equations 2.24 – 2.26 with the desired time T_s and ω_n .

For ζ of 0.707, T_s of one electrical cycle, R of 0.3Ω and L of 1mH ω_n would be 377 rad/sec and K_p and K_i would be 31.38 and 0.09998. The closed-loop Bode plot of this current controller design is presented in Figure 2.5.

Figure 2.5: Bode plot of the current controller

Figure 2.6: $d - q$ axis current control algorithm.

Figure 2.6 shows the block diagram of the current control algorithm in the $d - q$ axis. The measured inverter current is converted to the $\alpha - \beta$ axis and then converted into the $d - q$ axis, where the two separate PI controllers work to regulate the inverter current based on the reference values. The two PI controllers produce V_{d_ref} and V_{q_ref} which are then converted into the $\alpha - \beta$ frame, and fed into the PWM generation module. The reference currents are determined to control the active and reactive power of the system respectively.

The sampling rate of the controller, the PWM output switching frequency and the amount of measurement delays are the key components in the performance of the current regulator. If there are any delays in measuring the current or voltage, the THD of the output current increases considerably. Figure 2.7 shows the block diagram of the system with transportation delay. The Bode plot of the delayed closed loop system is shown in Figure 2.8.

Figure 2.7: System block diagram with transportation delay.

The delay in the measurement of the system parameters can be represented as $e^{-\tau s}$. The Pade approximation of the delay is $e^{-\tau s} = \frac{1-\tau s}{1+\tau s}$. The closed-loop transfer function with the delay is as shown in Equation 2.27

$$H(s) = \frac{(K_p s + K_i)(1 - \tau s)}{s^2(1 - \tau K_p) + s(R + K_p - K_i \tau) + K_i}. \quad 2.27$$

Figure 2.8: Bode plot of the delayed system.

Using Equations 2.24 to 2.26, K_p and K_i of the PI controller for the delayed system are calculated as 0.00959 and 0.3333 respectively.

The closed-loop Bode plot of the delayed system with the updated control is as shown in Figure 2.9.

Figure 2.9: Bode plot of the system with updated controller

2.6 Voltage control algorithm

When the utility grid is not available, an inverter can run in standalone operation. While the system is running in the grid connected mode of operation, it always checks for the voltage and frequency limits of the grid. If the voltage or the frequency is out of certain specified limits, then the inverter turns off the relay and operates in the standalone mode. In standalone mode, the inverter controls the voltage across the PCC to give power to the local loads connected to it. The RMS voltage control technique is one of the most effective and easy to implement techniques that give smooth voltage control at the PCC. Figure 2.10 shows the RMS voltage control technique algorithm. The RMS value of the voltage across the PCC is controlled through a PI controller. The output of the PI controller is multiplied with $\cos(\theta_s)$ where θ_s is calculated using Equation 2.28

$$\theta_s = \theta_{GC-SA} + \int f_s dt$$

2.28

where f_s is the desired frequency of the inverter output voltage.

Figure 2.10: RMS voltage control algorithm

Figure 2.11 shows the block diagram of the inverter in standalone mode of operation.

Figure 2.11: Standalone mode of operation of inverter

2.7 PWM generation algorithm

The PWM pulses are generated based on the voltage reference produced either by the output of current controller or the voltage controller. The reference voltage $V_{\alpha_{ref}}$ is biased to offset the negative values and compared with the high frequency triangle waveform.

Based on the comparison, the output of the generation is either high or low. The PWM generation block diagram is as shown in Figure 2.12.

Figure 2.12: PWM generation unit

2.8 Summary

The utility interactive inverter with standalone capacity for renewable energy and the battery backup systems is presented in this chapter. The grid synchronization, the current control, the voltage control and the PWM generation algorithms are discussed.

CHAPTER III

VOLTAGE HARMONIC CONTROL ALGORITHM

3.1 Introduction

The harmonic estimation and the control of a weak utility grid system through the RESs inverter are developed in this chapter. The recursive least square estimation (RLSE) is presented in detail. The control algorithm in the $d - q$ reference frame for the individual harmonics is developed.

3.2 Voltage harmonic control

The utility grid provides a stable power source for interconnected systems. The voltage and the frequency of the grid are considered to be stable. With the increase in the penetration of distributed renewable storage and other power electronic systems, the frequency and magnitude of the local grid is subject to fluctuations. Additional harmonics are introduced to the utility if the impedance of the utility grid is low. Nonlinear loads introduce additional harmonics on the grid voltage.

There are standalone units to cancel the effect of nonlinear loads on the grid. They are typically called active power filters which inject current to cancel the harmonic currents provided by nonlinear loads. None of the earlier systems try to correct the voltage spectrum directly by controlling voltage harmonics. If the grid is stiff it would be

difficult to control the voltage harmonics directly, but for a weak utility grid as shown in Figure 3.1, it would be possible.

Figure 3.1: Weak utility grid system diagram

The estimation of the individual harmonics is required to be able to reduce the harmonics. We first studied the most effective harmonic estimation techniques that can be implemented in real time. Many methods are available to measure the harmonics of the power system network. The RLSE technique gives an online update of the parameters to be measured and gives high solution accuracy. Though it requires many computations, the digital implementation of the controller can be done easily.

3.3 Measurement of grid harmonics through RLSE method

This method is an iterative method which updates the estimated model of the system for every sample interval of data. Figure 3.2 shows the block diagram of RLSE.

Figure 3.2: RLS control algorithm for harmonic estimation in utility grid voltage.

The control algorithm needs the data to be updated every interval, an employed ADC also measures the data for every sample interval. Hence this approach to measure the system parameters maintains accurate results with every new set of measurement data. In this method, the past information available in $\hat{\theta}(t-1)$ is used to obtain an estimate $\hat{y}(t)$ of the current output. This updated output $\hat{y}(t)$ is compared to the measured value $y(t)$ to compute the error $e(t)$. This algorithm will update $\hat{\theta}(t)$ using the calculated error $e(t)$. Unlike the other methods, it does not store all of its computations. It just stores the previous data $\hat{\theta}(t)$ and computes the new estimates $\hat{\theta}(t+1)$ by using the present measured sample data.

The general form of a discrete transfer function is as shown in Equation 3.1,

$$Ay(t) = Bu(t - 1) + Dv(t) + d(t) + Ce(t), \quad 3.1$$

where $u(t)$, $y(t)$, $v(t)$, $d(t)$ and $e(t)$ are the control input sequence, output, disturbance from the measurable source, drift and the random noise respectively.

$$A = 1 + a_1z^{-1} + \dots + a_{n_a}z^{-n_a},$$

$$B = 1 + b_1z^{-1} + \dots + b_{n_b}z^{-n_b},$$

$$D = 1 + d_1z^{-1} + \dots + d_{n_d}z^{-n_d},$$

$$C = 1 + c_1z^{-1} + \dots + c_{n_c}z^{-n_c}.$$

For estimation purposes, we can assume that the system is having no disturbance or noise. We can rewrite the Equation 3.1 as shown in Equation 3.2,

$$y(t) = \theta_1x_1 + \theta_2x_2 + \dots + \theta_nx_n + e(t), \quad 3.2$$

where $y(t)$ = measured output in the t^{th} sample,

$x_k(t)$ = measurable functions (data) of k^{th} sample

$e(t)$ = measurement error, and

$\theta_k(t)$ = polynomial coefficient.

If the system is unknown, the polynomial coefficients are treated as unknown parameters to be determined by measurement.

For estimation purposes, we can rewrite the Equation in the form of Equation 3.3, where the object to be estimated is emphasized more,

$$y(t) = x^T(t)\theta + e(t), \quad 3.3$$

where $x^T(t) = [x_1(t) \quad x_2(t) \quad x_3(t) \quad \dots \quad x_n(t)]$,

$$\theta^T = [\theta_1 \quad \theta_2 \quad \theta_3 \quad \dots \quad \theta_n]. \quad 3.4$$

Equation 3.4 is the true data mechanism; here we have to determine the system parameter θ from the available data.

Now, assume the correct system structure of a model as shown in Equation 3.5.

$$y(t) = x^T(t)\hat{\theta} + \hat{e}(t). \quad 3.5$$

In Equation 3.5, $\hat{\theta}$ is the vector of an adjustable parameter and $\hat{e}(t)$ is the corresponding modeling error.

Assuming that the system is continuously sampled over a period of time, we can get N sampled values and the model can be described as

$$\begin{bmatrix} y(1) \\ \vdots \\ y(N) \end{bmatrix} = \begin{bmatrix} x^T(1) \\ \vdots \\ x^T(N) \end{bmatrix} \hat{\theta} + \begin{bmatrix} \hat{e}(1) \\ \vdots \\ \hat{e}(N) \end{bmatrix}. \quad 3.6$$

Equation 3.6 in stacked notation is shown below.

$$Y(t) = X(t)\hat{\theta} + \hat{E}(t). \quad 3.7$$

The main aim here is to minimize the error by selecting $\hat{\theta}$. From the Equations 3.3 and 3.4, we can write that

$$\hat{e}(t) = e(t) + x^T(t)(\theta - \hat{\theta}). \quad 3.8$$

Here we compute θ such that the sum of squares of error (J) should be minimal

$$J = \sum_{t=1}^N \hat{e}^2(t) = \hat{e}^T \hat{e} = (y - x\hat{\theta})^T (y - x\hat{\theta}) \quad 3.9$$

$$\frac{\partial J}{\partial \hat{\theta}} = -2x^T y + 2x^T x \hat{\theta} = 0. \quad 3.10$$

Finally the least squares estimator is,

$$\hat{\theta} = [X^T X]^{-1} [X^T Y] \quad 3.11$$

The estimated value of the parameter at time $t+1$ is

$$\hat{\theta}(t+1) = [X^T(t+1)X(t+1)]^{-1} [X^T(t+1)Y(t+1)]. \quad 3.12$$

We know that, $X(t) = \begin{bmatrix} x^T(1) \\ \vdots \\ x^T(t) \end{bmatrix}$ and $y(t) = \begin{bmatrix} y(1) \\ \vdots \\ y(t) \end{bmatrix}$.

Therefore $X(t+1) = \begin{bmatrix} x^T(1) \\ \vdots \\ x^T(t) \\ \dots \\ x^T(t+1) \end{bmatrix} = \begin{bmatrix} X^T(t) \\ \dots \\ x^T(t+1) \end{bmatrix}$ and $y(t) = \begin{bmatrix} y(1) \\ \vdots \\ y(t) \\ \dots \\ y(t+1) \end{bmatrix} = \begin{bmatrix} y(t) \\ \dots \\ y(t+1) \end{bmatrix}$.

Now we can write,

$$\hat{\theta}(t+1) = [X^T(t)X(t) + x(t+1)x^T(t+1)]^{-1} [X^T(t)y(t) + x(t+1)y(t+1)]. \quad 3.13$$

Let $P(t) = [X^T(t)X(t)]^{-1}$ and $B(t) = X^T(t)y(t)$,

We have $\hat{\theta}(t) = P(t)B(t)$ and $\hat{\theta}(t+1) = P(t+1)B(t+1)$,

also $P^{-1}(t+1) = P^{-1}(t) + x(t+1)x^T(t+1)$ and

$$B(t+1) = X^T(t+1)y(t+1) = B(t) + x(t+1)y(t). \quad 3.14$$

Equation 3.14 gives $B(t+1)$ directly from $B(t)$. We should also find $P(t+1)$ from $P(t)$ which is called “covariance matrix”. This can be done using the matrix inverse lemma:

$$(A + BCD)^{-1} = A^{-1} - A^{-1}B(C^{-1} + DA^{-1}B)^{-1}DA^{-1}, \quad 3.15$$

assigning $A = P^{-1}(t)$, $C = 1$, $B = x(t+1)$, $D = x^T(t+1)$ to Equation 3.8.

$$\text{Eventually, } P(t+1) = P(t) \left[I_m - \frac{x(t+1)x^T(t+1)P(t)}{1+x^T(t+1)P(t)x(t+1)} \right]. \quad 3.16$$

Note that $1 + x^T(t+1)P(t)x(t+1)$ is a scalar value, so we do not have to invert any matrix, which increases the computational efficiency

$$e(t+1) = y(t+1) - x^T(t+1)\hat{\theta}(t). \quad 3.17$$

From the Equation 3.15, 3.16 and 3.17

$$\hat{\theta}(t+1) = \hat{\theta}(t) + P(t+1)x(t+1)e(t+1). \quad 3.18$$

To summarize the RLSE algorithm at time step $t+1$:

- 1) Form $x(t+1)$ from the new measured data.
- 2) Form $e(t+1) = y(t+1) - x^T(t+1)\hat{\theta}(t)$
- 3) Compute $P(t+1) = P(t) \left[I_m - \frac{x(t+1)x^T(t+1)P(t)}{1+x^T(t+1)P(t)x(t+1)} \right]$

- 4) Find $\hat{\theta}(t + 1) = \hat{\theta}(t) + P(t + 1)x(t + 1)e(t + 1)$
- 5) Update the parameter variables, wait for next sample time and loop back to (1).

The initial values of $\hat{\theta}$, and the covariance matrix are required for an algorithm implementation. If we have enough prior knowledge of the system, we can assume the initial value for $\hat{\theta}$ close to actual value and the initial value of the covariance matrix $P(t)$ should be small. Otherwise, $P(0)$ is selected as a large value. Generally $P(t)$ is an unit matrix multiplied by a constant value, which varies based on the initial value of $\hat{\theta}$.

For the utility voltage harmonic estimation algorithm, $x(t)$ is the voltage of the utility grid voltage, $\hat{\theta}(t)$ is the voltage harmonic coefficient, $e(t)$ is the error in the measurement and $P(t)$ is the covariance matrix of the system. The above algorithm gives the individual measurement of the harmonic magnitude and phase angle of the utility grid voltage. The harmonic measurement is done in the $\alpha - \beta$ frame to reduce the number of computations compared to the $d - q$ frame.

3.4 Voltage harmonic control algorithm

The harmonic voltage control capability is an add-on to an existing renewable energy source inverter. In addition to the fundamental harmonic responsible for main power transfer, additional harmonics are injected into the utility to be able to reduce the harmonics in the weak utility grid. Figure 3.3 shows the overall block diagram of the proposed system.

Figure 3.3: Control algorithm for active/reactive and harmonic control

The harmonic control can be done in the $\alpha - \beta$ frame or the $d - q$ synchronous rotating frame. In the $\alpha - \beta$ frame, the controlling parameters are sine waves with different frequencies depending on the harmonic order to be controlled. In the $d - q$ synchronous rotating frame, the controlling parameters are the DC values, so controlling the steady state errors in the DC values is more effective compared to varying reference inputs.

The primary purpose here is to control the utility grid voltage harmonics. To control the utility grid voltage harmonics, a harmonic controller in the d-q axis is developed. The developed harmonic controller first measures the harmonics in the grid, and converts them into the $d - q$ frame and a PI controller controls the value of harmonic based on the specified harmonic reference, this reference is ideally zero for the complete harmonic elimination.

3.4.1 Synchronous rotating frame transformation

The typical harmonics in the single phase utility grid system are 3rd, 5th, 7th..... (2n+1)th. The single phase utility voltage with these harmonics would be represented as

$$V = V_1 \sin(2\pi ft + \phi_1) + V_3 \sin(2\pi(3ft) + \phi_3) + \dots \dots \dots + V_{2n+1} \sin(2\pi(2n + 1)ft + \phi_{2n+1}). \quad 3.19$$

We can rewrite the above Equation to estimate the magnitude and phase of the harmonics in the voltage.

$$V = V_1 \{ \cos(2\pi ft) \times \sin(\phi_1) + \sin(2\pi ft) \times \cos(\phi_1) \} + V_3 \{ \cos(2\pi(3ft)) \times \sin(\phi_3) + \sin(2\pi(3ft)) \times \cos(\phi_3) \} + \dots \dots \dots + V_{2n+1} \{ \cos(2\pi(2n + 1)ft) \times \sin(\phi_{2n+1}) + \sin(2\pi(2n + 1)ft) \times \cos(\phi_{2n+1}) \}. \quad 3.10$$

The coefficients of the *cos* and *sin* values are estimated using above equation and the magnitude and phase values are calculated. The individual harmonics are estimated using the RLSE method as described earlier in the α - β reference frame. Since the controller is done in the d-q reference frame, the individual harmonic voltages are transformed into the d-q reference frame rotating at the harmonic frequencies.

After transforming into d-q axis synchronous rotating frame, the components with rotating frequency will become the DC values and the other frequency components become harmonics with either (n+1) or (n-1) multiples of the rotating frequency.

To conclude, in the synchronous rotating reference frame, the components with rotating frequency become DC values, and other frequency components become either (n+1) or (n-1) multiples of the rotating frequency. The delay required to compute V_α to V_β is $\frac{\pi}{2n}$, where n is the order of the rotating frequency.

3.5 Controller algorithm design

The voltage harmonics are compensated through a closed loop controller. A PI controller is used because of its stability and adoptability to different harmonic orders. We can use the same controller for all the harmonics, by changing the gain and bandwidth of the controller. The PI controller gains depend on the bandwidth, settling time, damping ratio and the natural frequency of the system. The PI controller bandwidth changes as we change the order of harmonic to be controlled.

3.5.1 3rd Harmonic controller design

Figure 3.4 shows the 3rd harmonic control algorithm in the $d - q$ synchronous rotating frame. The measured 3rd harmonic $V_{3h} \angle \theta_{3h}$ is converted to the $d - q$ frame. In converting third harmonic to the $d - q$ synchronous rotating frame, the delay between $V_{3h\alpha}$ and $V_{3h\beta}$ should be $\frac{\pi}{2 \times 3} = \frac{\pi}{6}$. Now, V_{3dh} and V_{3qh} are controlled using a designed PI controller based on given 3rd harmonic reference limits V_{3hd_ref} and V_{3hq_ref} . The output of the PI controllers V_{3d_ref} and V_{3q_ref} are converted back to $V_{3\alpha_ref}$ and $V_{3\beta_ref}$

($\alpha - \beta$ reference frame). The reference values $V_{3\alpha_ref}$ and $V_{3\beta_ref}$ are given to PWM generation modules to generate the duty cycles.

Figure 3.4: 3rd harmonic control in $d-q$ synchronous rotating frame using PI controller.

3.5.2 5th Harmonic controller design

The measured 5th harmonic of the utility grid voltage is also controlled by injecting harmonic current into the utility grid.

Figure 3.5: 5th harmonic elimination control algorithm

To convert the 5th harmonic into the $d - q$ frame, the delay between $V_{5h\alpha}$ and $V_{5h\beta}$ should be $\frac{\pi}{2 \times 5} = \frac{\pi}{10}$. Now, V_{5dh} and V_{5qh} are controlled using a designed PI controller based on given 5th harmonic reference limits V_{5hd_ref} and V_{5hq_ref} . The output of the PI controllers V_{5d_ref} and V_{5q_ref} are converted back to $V_{5\alpha_ref}$ and $V_{5\beta_ref}$ ($\alpha - \beta$ reference frame). The reference values $V_{5\alpha_ref}$ and $V_{5\beta_ref}$ are given to PWM generation modules to generate the duty cycles. Figure 3.5 shows the algorithm for controlling the 5th harmonic in a weak utility grid voltage. Similarly 7th, 9th (2n+1)th harmonics are controlled using different controller gains and bandwidths. After generating $V_{5\alpha_ref}$ and $V_{5\beta_ref}$ for 5th harmonic control, adding the harmonic reference voltages $V_{3\alpha_ref}$ and

$V_{3\beta_{ref}}$ eliminates 3rd and 5th harmonic components at the same time in a weak utility grid. Likewise we can eliminate all the harmonics in the system by measuring the magnitude and phase angle precisely. As we are controlling the harmonics in the $d - q$ frame, we can control all the harmonics at the same by using individual controllers for each harmonic.

This controller makes sure that controlling one harmonic does not increase other harmonics in the utility voltage. The controller is shown in Figure 3.6

Figure 3.6: All voltage harmonic control in the weak utility grid

3.6 Harmonic control selection

The developed harmonic controller has the capability of selecting individual harmonics to be controlled. It selects the order of harmonic to be controlled based on the magnitude of voltage harmonics in the utility grid. If 3rd and 5th harmonics are the dominant harmonics, it selects 3rd and 5th harmonics to control. Figure 3.7 shows the harmonic selection control algorithm. Depending on the selected harmonics, the reference voltages $V_{3\alpha_ref}$, $V_{5\alpha_ref}$.. are added and the result will be fed to PWM generation algorithm.

Figure 3.7: Control algorithm of harmonic selection.

3.7 Summary

A control algorithm to control the utility grid voltage harmonics is developed. The RLSE measures the weak utility grid voltage harmonics. The advantage of RLSE is high solution accuracy and computational efficiency. The developed control algorithm controls the harmonics in the utility grid voltage by controlling injected harmonic currents into the grid.

CHAPTER IV

SIMULATION RESULTS

4.1 Introduction

The simulation setup to verify the performance of the proposed controller algorithm is developed in the Matlab/Simulink environment. A weak utility grid with harmonics is emulated using nonlinear loads and the utility interactive inverter. A bi-directional utility interactive inverter is developed to control the active and reactive power. The same utility interactive inverter is used to control the harmonics in the weak utility grid.

4.2 Simulation setup

The simulation of a complete utility grid interactive inverter system developed in the Matlab/Simulink environment with the following design parameters:

Power rating	5 kW,
Utility Grid voltage	Single phase, 120 Vrms,
Inverter output current	0-50 A peak,
Grid frequency	60 Hz,
DC Bus voltage/Current	200 V/0-25 A.

The main purpose of the proposed control algorithm is to control the harmonics in the voltage of a single phase weak utility grid with harmonics. The single phase utility grid with harmonics is emulated using nonlinear loads. A nonlinear load which produces 3rd, 5th, 7th, and 9thetc. harmonics into the utility grid is designed using a single phase rectifier with the inductive and capacitive loads connected. The utility grid considered is a weak utility grid, hence it is assumed that the impedance of the grid is low compared to the strong utility grid. Figure 4.1 shows the connected nonlinear loads across the utility grid to produce the harmonics at the PCC.

Figure 4.1: Nonlinear load connected to single phase utility grid

4.3 Simulation results

The connection of the utility interactive inverter to a single phase utility grid is done through grid synchronization. The grid synchronization is easily achieved using a Phase Locked Loop (PLL). Once the grid is synchronized, the utility interactive inverter is tested for active/reactive power injection and battery charging. The harmonic control of the utility grid voltage is done in the $d - q$ axis and the measurement of harmonics is done using RLSE.

4.3.1 Grid synchronization using PLL

Figure 4.2 shows the PLL results of a single phase utility grid. The utility grid voltage is emulated as the utility frequency and no harmonics are injected. The PLL locks the phase of the utility grid voltage as shown in figure 4.2 (d). Once the phase is synchronized, V_d reaches the peak value of the grid voltage value and V_q stays at zero as shown in Figure 4.2 (b-c). The PLL is also tested with the inverter feeding into a weak grid having a nonlinear load.

The voltage at the PCC has higher order harmonics as shown in the Figure 4.3 (a). The harmonics are also present in V_d , V_q and the estimated phase as shown in Figure 4.3.

Figure 4.2: Phase Locked Loop results: (a) Utility grid voltage (b) d-axis voltage, (c) q-axis voltage, (d) Phase angle of utility grid voltage for grid synchronization.

Figure 4.3: PLL results of utility grid voltage with harmonics: (a) Utility grid voltage (b) d-axis voltage, (c) q-axis voltage, (d) Phase angle of utility grid voltage.

4.3.2 Injection of active/reactive power into the utility grid

The active and reactive power injection into the utility are tested with different operating conditions. In this section the voltage at the PCC is kept such that no higher order harmonics are present. The transient performance of the active power injection into the utility with the RESs inverter is presented in Figure 4.4. The reference value of the d-axis inverter output current is kept at 50A and the q-axis current is kept zero. As shown in

Figure 4.4 the PI controller works fine to regulate the current with low overshoot. The steady state performance of this command condition is presented in Figure 4.5. The phase shift between the inverter output current and the utility voltage is close to zero to be able to inject only the active power into the utility as shown in Figure 4.5.

Figure 4.4: Active power injection into utility grid during transient ($I_{d_ref} = 50$ A and $I_{q_ref} = 0$ A): (a) Utility grid voltage, (b) Inverter output current, (c) Grid voltage/Inverter output current, (d) d-axis and q- axis values of inverter output current.

Figure 4.5: Active power injection into utility grid at steady state ($I_{d_ref} = 50$ A and $I_{q_ref} = 0$ A): (a) Utility grid voltage, (b) Inverter output current, (c) Grid voltage/ Inverter output or grid current, (d) inverter output current in d-q axis.

The command value for the q-axis current is increased to 25A and d-axis current is decreased to 25A to be able to inject reactive power as well as the active power into the utility. Figure 4.6 shows the performance of the inverter operation when we command both active and reactive power at the same time.

Figure 4.6: Active and reactive power injection into utility grid at steady state ($I_d_{ref} = 25$ A, $I_q_{ref} = 25$ A): (a) Utility grid voltage, (b) Inverter output current, (c) Grid voltage/ Inverter output or grid current.

The d and q-axis currents are presented in Figure 4.7. As shown from this figure the controller performs well to follow the command d and q-axis currents.

Figure 4.7: Active and reactive power injection into utility grid at steady state ($I_{d_ref} = 25$ A, $I_{q_ref} = 25$ A): d-axis and q- axis values of inverter output current.

Figure 4.8 shows the results of the utility interactive inverter when the commanded current is only reactive current. The commanded d-axis and q-axis values of current are $I_{d_ref} = 0$ A and $I_{q_ref} = 50$ A. The inverter output current and the utility grid voltage are 90 degrees out of phase as the injected power is only reactive power as shown in Figure 4.8 (c).

The active and reactive power of the inverter output are $P_d = 0$ kW and $P_q = 4.25$ kVAR.

Figure 4.8: Reactive power injection into utility grid at steady state ($I_{d_ref} = 0$ A, $I_{q_ref} = 50$ A): (a) Utility grid voltage, (b) Inverter output current, (c) Grid voltage/Inverter output current or grid current, (d) d-axis and q- axis values of inverter output current.

4.3.3 Power flow from grid to inverter (Charging)

The designed converter is a bi-directional converter. It has the capability of injecting power into the utility grid as well as has the capability of converting utility grid AC power to DC power to feed the DC side loads (battery). Based on the given reference current, the power flows from the utility grid to the inverter, or the inverter to the utility grid. Figure 4.9 shows the battery charging results for the reference command for I_d_ref as - 40 A and I_q_ref as 0A. The phase angle difference between the utility grid voltage and the converter input current is 180 degrees as shown in Figure 4.9 (c).

As shown in Figure 4.9, the d and q axis currents follow the commanded values to provide the power into the DC side.

Figure 4.9: Battery charging ($I_{d_ref} = -40$ A and $I_{q_ref} = 0$ A): (a) Utility grid voltage, (b) Utility grid current, (c) Utility grid voltage/Converter input current, (d) d-axis and q-axis values of converter input current.

4.3.4 Injecting active and reactive power utility grid with delay in measurement

The developed controlled algorithm is tested when there is a delay in the measurement of the utility grid voltage and the inverter output current. Figure 4.10 shows the results of active and reactive power injection into the utility grid when there is a delay in the measurement of the utility grid voltage and current. The command value for I_d_{ref} is 30 A and I_q_{ref} is 20 A. If there is a delay in the measurement, the steady state error between the reference and the actual currents is very high, and the inverter current has the harmonics as shown in Figure 4.10. Similar tests have been conducted where the command currents are such that the power flows from the utility to the DC side.

Figure 4.11 shows the effect of delay in the system performance when the I_{d_ref} command is 40 A and the I_{q_ref} is 0A. As shown from this figure the quality of the phase currents is quite low.

Figure 4.10: Active and reactive power injection into utility grid when there is delay in the measurement ($I_{d_ref} = 30$ A, $I_{q_ref} = 20$ A): (a) Utility grid voltage, (b) Inverter output current, (c) Inverter output current. (d) Inverter output current in d-q axis.

Figure 4.11: Battery charging with delay in the measurement ($I_{d_ref} = -40$ A and $I_{q_ref} = 0$ A): (a) Utility grid voltage, (b) Utility grid current, (c) Utility grid voltage/Converter input current, (d) d-axis and q-axis values of converter input current.

4.3.5 Active and reactive power injection into the utility grid with delay and updated gains

To reduce the steady state error, the controller gains are redesigned considering the delay in the measurement of the utility grid voltage and the converter current. Active and reactive power injections into the utility grid with the updated gains are tested and the results are shown in Figure 4.12. As shown from this figure, the performance of the current regulator is much better with the updated controller considering the delay in the measurement. With the updated gains, charging of the battery is also tested and the results are presented in Figure 4.13. The performance of the controller during charging is also enhanced with the update in the controller.

Figure 4.12: Active and reactive power injection into utility grid with updated controller ($I_{d_ref} = 30$ A and $I_{q_ref} = 20$ A): (a) Utility grid voltage, (b) Inverter output current, (c) Grid voltage/ Inverter output current, (d) Inverter output current in d-q axis.

Figure 4.13: Charging battery from single phase utility grid with updated controller ($I_{d_ref} = -40$ A and $I_{q_ref} = 0$ A): (a) Utility grid voltage, (b) Inverter output current, (c) Grid voltage/ Inverter output current, (d) Inverter output current in d-q axis.

4.3.6 Active and reactive power injection into utility grid in the presence of local load

The developed control algorithm is tested when the local load of a $10\ \Omega$ resistor is connected across the PCC. Active and the reactive power injection into the utility grid are shown in Figure 4.14 with I_d_ref command of 40A and I_q_ref command of 10A. The amount of current taken by the local load with respect to the utility current and inverter output current is shown in Figure 4.15. The portion of the inverter is output current is fed into the local load and the rest of it is pushed into the utility grid. With the same amount of local load, the I_d_ref command is changed to -40A to show the effect of the local loads during charging. Figures 4.16 and 4.17 present the results of this operating condition. As the local load considered in this study is linear, we do not see harmonics in the utility grid voltage.

Figure 4.14: Active and reactive power injection into utility grid when the local loads are connected ($I_{d_ref} = 40$ A, $I_{q_ref} = 10$ A): (a) Utility grid voltage, (b) Inverter output current, (c) Grid voltage/ Inverter output current, (d) d-axis and q- axis values of inverter output current.

Figure 4.15: Active and reactive power injection into utility grid in the presence of local loads ($I_{d_ref} = 40$ A, $I_{q_ref} = 10$ A): (a) Inverter output current, (b) Injected utility grid current, (c) Local load current (Current drawn by local load).

Figure 4.16: Charging battery when local loads are connected ($I_{d_ref} = -40$ A, $I_{q_ref} = 0$ A): (a) Utility grid voltage, (b) Utility grid current, (c) Utility grid voltage/Converter input current, (d) d-axis and q-axis values of converter input current.

Figure 4.17: Charging battery when the local loads are connected ($I_{d_ref} = -40$ A, $I_{q_ref} = 0$ A): (a) Converter input current, (b) Utility grid current, (c) Local load current (Current drawn by local load).

4.3.7 Standalone mode operation of utility interactive inverter

When the utility grid is not available, an inverter can run in standalone mode. Figure 4.18 shows the results of the inverter operation in the standalone mode. The resistive load connected across the inverter is $6\ \Omega$, hence the inverter output current is 28 A as shown in Figure 4.20. The output power of the inverter is 2.4 kW, the RMS value of the inverter output voltage is 120 V, and the frequency command for the inverter operation is considered as 60 Hz.

Figure 4.18: Standalone mode of utility interactive inverter operation: (a) Inverter output voltage, (b) Inverter output current, (c) Load voltage/Load current.

4.4 Harmonic voltage control in the weak utility grid

We previously used a resistive load to show the effects of the local load on the utility grid. In this part of the simulation, we consider nonlinear loads as a local load. The nonlinear local load would cause harmonics with the weak utility grid where there is a source impedance between the stiff portion of the utility grid and the PCC. As shown Figure 4.19 there are higher order harmonics present in the voltage at the PCC.

Figure 4.19: Voltage of single phase weak utility grid.

4.5 Estimation of the harmonics in utility grid voltage

To implement the harmonic control in the weak utility grid voltage, first the harmonics in the utility grid voltage need to be estimated. Based on FFT analysis for the utility voltage shown in Figure 4.19, the major harmonics in the utility grid voltage are the 3rd, 5th, 7th, and 9th. The RLSE technique is used to estimate the harmonics in the utility grid voltage.

As shown in Figure 4.20, RLSE estimates the fundamental harmonic voltage and its phase. The magnitude is 170 V and the phase is zero as expected.

Figure 4.20: Fundamental component of single phase utility grid voltage: (a) Magnitude measurement, (b) phase angle measurement.

RLSE also estimates the magnitude and the phase of the higher order harmonics. Figure 4.21, 4.22, 4.23 and 4.24 show the 3rd, 5th, 7th, and 9th harmonic voltage and phase based on RLSE operation.

Figure 4.21: 3rd harmonic measurement of single phase utility grid voltage: (a) Magnitude measurement, (b) Phase angle measurement

Figure 4.22: 5th harmonic measurement of single phase utility grid voltage: (a) Magnitude measurement, (b) Phase angle measurement

Figure 4.23: 7th harmonic measurement of single phase utility grid voltage: (a) Magnitude measurement, (b) Phase angle measurement.

Figure 4.24: 9th harmonic measurement of single phase utility grid voltage: (a) Magnitude measurement, (b) Phase angle measurement.

We have also done FFT analysis of the voltage at the PCC. As shown in Figure 4.25 there are 3rd, 5th, 7th, and 9th harmonics present at the PCC voltage which contributes to the THD of 7.3%.

Figure 4.25: Harmonic analysis of a single phase utility grid voltage (Fundamental magnitude of the grid voltage is 170 V)

4.6 Voltage harmonic control in weak utility grid

The harmonic control algorithm that has been developed in Chapter III has been implemented. We first applied the controller to reduce the individual harmonics separately with no power processing at the fundamental frequency. Figure 4.26 shows the performance of the 3rd harmonic control. The 3rd harmonic control tries to inject current into utility to reduce the 3rd harmonic voltage at the PCC. As shown in Figure 4.27, the 3rd harmonic content of the PCC voltage is reduced to 1 V which originally was 6.6 V. The PWM out of the control algorithm to control the harmonics in the system is shown in Figure 4.28.

Figure 4.29 shows the performance of the 5th harmonic voltage control. Here the 5th harmonic voltage control injects current into the utility to reduce 5th harmonic voltage at the PCC. As shown in Figure 4.30, the 5th harmonic content is reduced to 1 V which is originally was at the level of 8.45 V.

Figure 4.26: 3rd harmonic control in d-q synchronous rotating frame: (a) Utility grid voltage before harmonic control, (b) Current injected into utility grid for 3rd harmonic control, (c) Utility grid voltage after 3rd harmonic control

Figure 4.27: Harmonic analysis of utility grid voltage after 3rd harmonic control (fundamental is 170 V)

Figure 4.28: PWM output of the 3rd voltage harmonic control algorithm.

Figure 4.29: 5th harmonic control in d-q synchronous rotating frame: (a) Utility grid voltage before harmonic control, (b) Current injected into utility grid for 5th harmonic control, (c) Utility grid voltage after 5th harmonic control

Figure 4.30: Harmonic analysis of utility grid voltage after 5th harmonic control (fundamental is 170 V)

Similarly 7th and 9th harmonic voltage control are also tested. Figure 4.31 shows the performance of the 7th harmonic control. The 7th harmonic control tries to control the 7th harmonic voltage at the PCC through injecting current into the utility grid. As shown in Figure 4.32 the 7th harmonic current is reduced to 1V which is originally was 5V. Figure 4.33 shows the performance of the 9th harmonic control at the PCC. As shown Figure 4.34, the 9th harmonic magnitude after harmonic control is 0.5V which was originally at the level of 2.9 V.

Figure 4.31: 7th harmonic control in d-q synchronous rotating frame: (a) Utility grid voltage before harmonic control, (b) Current injected into utility grid for 7th harmonic control, (c) Utility grid voltage after 7th harmonic control

Figure 4.32: Harmonic analysis of utility grid voltage after 7th harmonic control (fundamental is 170 V)

Figure 4.33: 9th harmonic control in d-q synchronous rotating frame: (a) Utility grid voltage before harmonic control, (b) Current injected into utility grid for 9th harmonic control, (c) Utility grid voltage after 9th harmonic control

Figure 4.34: Harmonic analysis of utility grid voltage after 9th harmonic control (fundamental is 170 V)

4.6.1 Combination of voltage harmonic controllers

After verifying individual harmonic voltage control we first studied combining 3rd and 5th harmonic voltage controllers. Figure 4.35 shows the voltage at the PCC before and after the 3rd and 5th harmonic controller actions. As shown in Figure 4.36, the 3rd and 5th harmonics are reduced to 1V together from 6.58 V and 8.45 V respectively. The THD after the control is reduced to 3.6 % from 7.3 %. We have also combined 3rd, 5th, 7th, and 9th voltage harmonic controllers all together. Figure 4.37 shows the performance of the combined controller. The voltage at the PCC after the control is close to sinusoidal. The THD is reduced to 1.24 % as shown in Figure 4.38.

Figure 4.35: 3rd and 5th harmonic control in d-q synchronous rotating frame: (a) Utility grid voltage before harmonic control, (b) Current injected into utility grid for 3rd and 5th harmonic control, (c) Utility grid voltage after 3rd and 5th harmonic control

FFT analysis

Figure 4.36: Harmonic analysis of utility grid voltage after 3rd and 5th harmonic control (fundamental is 170 V).

Figure 4.37: Controlling all harmonics in d-q synchronous rotating frame: (a) Utility grid voltage before harmonic control, (b) Current injected into utility grid for controlling all harmonics, (c) Utility grid voltage after controlling all harmonics.

Figure 4.38: Harmonic analysis of utility grid voltage after controlling all harmonics

4.6.2 Active power injection with 3rd and 5th harmonic control(fundamental is 170 V).

The performance of the voltage harmonic controller is tested with active and reactive power injection into the utility grid. The 3rd and 5th voltage harmonic controllers are kept with 2.5 kW active power injections. As shown in Figure 4.39 the PCC voltage is corrected with the harmonic controller and the voltage THD is reduced to 3.1 % as shown in Figure 4.40.

Figure 4.39: Active power, 3rd harmonic and 5th harmonic control in d-q synchronous rotating frame: (a) Utility grid voltage before harmonic control, (b) Current injected into utility grid for active power, 3rd harmonic and 5th harmonic control, (c) Utility grid voltage after active power, 3rd harmonic and 5th harmonic control

Figure 4.40: Harmonic analysis of utility grid voltage after active power, 3rd harmonic and 5th harmonic control (fundamental is 170 V).

4.7 Summary

The simulation setup is explained in detail in this chapter. A weak polluted utility grid is emulated to test the voltage harmonic controllers. Active/reactive power control and battery charging are verified. The voltage harmonic control of a weak utility grid is tested with different operating conditions. The simulation results verified that the proposed control algorithm works effectively to reduce the harmonics at PCC voltage.

CHAPTER V

EXPERIMENTAL SETUP

5.0 Introduction

This chapter presents the experimental setup developed to test the harmonic voltage control in a weak utility grid system. The developed algorithm is tested for various operating conditions and the results are observed using Tektronix digital oscilloscopes and an ADSP++ plot analyzer. The results are evaluated by processing the data in the Matlab/Simulink environment.

5.1 Experimental setup

A bi-directional 5kW utility interactive inverter has been developed to test the proposed control algorithms. The experimental setup is shown in Figure 5.1, which shows the inverter, filter (inductor), local load, utility grid, battery, interfacing board, DSP and computer for Visual DSP++. The key parameters of the developed system are:

Grid Voltage:	120 V (rms), 60 Hz,
Battery Voltage:	200V,
Battery Current:	0-25 A,
Inductor:	1mH.

Figure 5.1: Experimental setup

5.1.1 Power section

The power module IAP100T120 is developed as a bi-directional inverter. It has built in DC-link capacitors of $3300 \mu\text{F}$, protective circuits for over-current, short-circuit, over-voltage, under-voltage, over-temperature, and a gate drive circuit to drive the IGBTs. The power module contains three independent IGBT legs which are capable of handling 800 V DC bus voltage, switching frequency of 20 kHz, and peak collector current of 200 A. Figure 5. 2 (a) shows the inverter module used for the experiment.

5.1.2 Interface board

An interface board between the DSP and the inverter module is developed to measure the utility grid voltage, the inverter voltage, the inverter current, the DC bus voltage and the DC current. Additionally, the interface board is equipped with PWM

buffer circuits, protection circuits for over or under, protection circuits for over or under current, and a relay driving circuit. An interface board and EZLITEKIT for Digital Signal Processor (DSP) interfacing are shown in Figure 5.2.

Figure 5.2: Grid interactive inverter setup: (a) Power module, (b) Interface board, (c) DSP development board

5.1.3 Relay driver circuit

The physical connection between the utility grid and the grid tie inverter is achieved using a soft switching relay. A driver circuit to drive the relay is developed on the interface board and is shown in Figure 5.3. The DSP generates a turn ON/OFF which drives a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) after passing through a Schmitt trigger. The MOSFET is connected to the coil of the relay, hence turning ON and OFF of the MOSFET activates the relay coil, which produces the relay ON or OFF status.

Figure 5.3: Relay driving circuit

5.1.4 Voltage sensor circuit

A voltage amplifier AD202 is used to measure the AC and DC voltages of the system. A voltage divider circuit is used to change the AC voltage from 170 V to 4.25 V and the DC voltage from 200V to 5V. The C11, C12, C13 and R13 values are used as recommended for the amplifier. Note that the output of the voltage sensor is a bi-directional signal. Since the DSP cannot read negative values we added a biasing circuit. Figure 5.4 shows the voltage isolation amplifier AD202 and the interface circuit.

Figure 5.4: Voltage isolation amplifier AD202 to measure voltage.

5.1.5 Sensor conditioning circuitry

The output of the voltage sensor is between +4.25 V and -4.25 V for a single phase AC utility grid, and 5V for a dc bus voltage of 200V. The DC voltage sensor data

is passed through a voltage isolator to reduce the high frequency noise. For AC voltage sensor data, first we have to do level shifting by adding +5V, after which the level shift signal changes to 0 to +10V. As the DSP can only read up to +5V, it has to be passed through an amplifier to reduce the signal to between 0 and 5V. An AD713 chip contains four op-amps, one of them is used as the buffer, the second one is used as a level shifter, the third one is used as scaling and the fourth one is used as a buffer to send the data to a comparator for fault detection as shown in Figure 5.5. Finally a Zenor diode is used for protection.

Figure 5.5: Processing sensor data using AD713

5.1.6 PWM interface circuitry

The input signal for the IAP100T120's gate driver circuit is between 0 and 15V, but the DSP can generate the PWM signals of 3.3V magnitude. Hence this signal is level

shifted or magnified to 15V to turn ON/OFF the IGBT modules. Three MCP1404 chips are used for level shifting. A MCP1404 with its supply voltage is as shown in Figure 5.6. The developed PWM signals are processed through a PWM buffer, which works based on a DSP soft shutdown signal

Figure 5.6 PWM level shifter and buffer circuit

A DSP soft shut down signal is generated by DSP, and a hard wired switch is also provided to control the PWM shut down signal. As shown in Figure 5.6, 74LVC541 is used as a PWM buffer. LED R2 is provided on interface board to detect the PWM status.

5.1.7 Fault protection circuitry

Figure 5.7: Fault protection circuit

The utility grid voltage, the dc voltage, the inverter output current and the gate driver fault protection circuit is developed as shown in Figure 5.7. If any of these faults occur, then it generates a fault signal which turns off the PWM signals for the IGBT module. LED signals are provided for easy debugging of the interface board for fault conditions. If there is any fault, then the corresponding LED will glow. Once the fault is cleared, the DSP generates a fault reset signal which resets the LED and fault holding latches.

5.2 Digital signal processor

An Analog Devices DSP BF506F is used for software implementation of the algorithms. Software programs are developed in the Visual DSP++ integrated development and debugging environment. The BF506F is a high performance and low power processor which has many features including the following:

- General-Purpose I/O (GPIO)
- Two-Wire Interface
- Removable Storage Interface (RSI) controller
- General-Purpose (GP) Counter
- Two 3-Phase PWM units
- Parallel Peripheral Interface
- Serial PORT (SPORT) Controllers
- Serial Peripheral Interface (SPI)
- Timers
- Controller Area Network (CAN) Interface

- Internal ADC
- Watch DOG Timer
- Clock Signals

The evaluation board (EZ-KIT Lite) is used to interface the BF506F to VisualDSP++. The VisualDSP++ environment can create, compile, assemble and link programs written in C/C++ to BF506F assembly. We can read or write data/program memory and core/peripheral registers. One of main advantages of the VisualDSP++ development environment is the capability to plot data memory.

The core features of EZ-KIT Lite are as follows:

- a. Analog Devices ADSP-BF506F Blackfin processor
 - Core performance up to 400 MHz
 - External bus performance up to 80 MHz
 - 120-pin LQFP package
 - 25 MHz crystal
- b. Internal parallel flash memory
 - Numonyx M58WT032 – 4 MB (2M x 16 bits)
- c. SPI flash memory
 - Numonyx M25P16 – 16 Mb
- d. Internal ADC
 - Analog Devices AD7266 2 MSPS, 12-bit, 3-channel SARanalog-to-digital converter
 - Twelve single-ended inputs

- Six differential inputs
 - e. Universal asynchronous receiver/transmitter (UART)
 - a. ADM3202 RS-232 line driver/receiver
 - b. DB9 female connector
 - f. LEDs
 - c. Five LEDs: one board reset (red), three general-purpose(amber), and one power (green)
 - g. Push buttons
 - d. Three push buttons: one reset and two programmable flags with debounce logic
 - h. Expansion interface II
 - e. Next generation of the expansion interface design, provides access to most of the processor signals
 - i. Other features
 - f. JTAG ICE 14-pin header
 - g. Processor power measurement jumpers
- 5.3 Summary:

An experimental system is developed to test the proposed control algorithms. The speed of the ADSP BF506F processor is a 400 MHz. The internal memory and clock speeds of the DSP are high enough to implement the developed control algorithm. An interfacing board between power module and EZKIT-LITE is developed to process the power.

CHAPTER VI

EXPERIMENTAL RESULTS

6.1 Introduction

This chapter presents the proposed voltage harmonic control algorithm on the experimental system. The developed algorithm is tested for various operating conditions and the results are observed using a Tektronix digital oscilloscope and an ADSP++ plot analyzer. The results are evaluated by processing the data in Matlab/Simulink to compute the FFT and the THD. The experimental results are observed in a Tektronix DPO 2024 Digital Phosphor Oscilloscope, and the VisualDSP++ memory plot. The voltages are measured using a “Tektronix P5200 high voltage differential probe” and the currents are measured using a “Tektronix A622 AC/DC current probe”.

6.2 Testing of bi-directional inverter

The utility grid interactive inverter is tested extensively for various parameter changes in both the charging and discharging conditions. The developed control algorithm for harmonic control of the utility grid voltage is tested for different command inputs.

6.2.1 Grid synchronization testing

A bi-directional inverter is interfaced to the utility grid through a PLL grid synchronization algorithm. The PLL algorithm locks the estimated frequency to the utility frequency and through integration determines the utility phase. Once the utility grid phase is locked, then the inverter runs with the same phase angle as the utility. The phase estimation of the utility grid voltage for the experiment is shown in Figure 6.1 (a). It is clearly evident from Figure 6.1 that the utility voltage has harmonics. Hence the effect of harmonics is reflected in the d and q-axis voltage and the phase angle. Once the inverter gets synchronized to the utility grid, the power control is done through current control. Therefore we can control active and reactive power through a current controller.

Figure 6.1: Phase Locked Loop results: (a) Utility grid voltage (b) d-axis voltage, (c) q-axis voltage, (d) Phase angle of utility grid voltage for grid synchronization

6.2.2 Active and reactive power injection into utility grid

The experimental power processing is tested first with only active power injection into the utility grid. An I_d_ref of 22A and an I_q_ref of 0A are commanded and the results are presented in Figure 6.2. The controller performs well in processing the command current levels to produce 1.8 kW. As shown in Figure 6.2 (d) there are significant harmonics present on the utility voltage. The error between the commanded current and the reference current are quite small as shown in Figure 6.3.

A non-negative I_q_ref is introduced to the controller to be able inject reactive power as well as active power into the utility grid. Figure 6.4 shows the results for an I_d_ref command of 22A and an I_q_ref command of 17A. An inverter injects 1.7 kW of active power and 1.445 kVAR of reactive power.

Figure 6.5 shows the inverter operation with only a reactive power command. As we inject only the reactive power, the phase difference between the inverter output current and the utility voltage is close to 90 degrees.

Figure 6.2: Active power injection into utility grid ($I_{d_ref} = 22$ A and $I_{q_ref} = 0$ A):

(a) Utility grid voltage, (b) Inverter output current, (c) Grid voltage/ Inverter output current, (d) d-axis and q- axis values of output current.

Figure 6.3: Steady state error analysis between reference and actual currents

Figure 6.4: Active and reactive power injection into utility grid ($I_{d_ref} = 20$ A, $I_{q_ref} = 17$ A): (a) Utility grid voltage, (b) Inverter output current, (c) Grid voltage/ Inverter output or grid current, (d) d-axis and q- axis values of output current.

Figure 6.5: Reactive power injection into utility grid ($I_{d_ref} = 0$ A, $I_{q_ref} = 20$ A):

(a) Utility grid voltage, (b) Inverter output current, (c) Grid voltage/ Inverter output current or grid current, (d) d-axis and q- axis values of output current.

6.2.3 Power flow from grid to DC side (Charging)

It is possible to flow the power from the utility side into the DC side. This mode of operation is typically considered as charging. We can control the charging rate by controlling the active and the reactive power of the inverter. Changing the reference current command sign changes the direction of the current flow of the inverter. A negative sign for the command current charges the battery and a positive sign for the command current discharges the battery. Figure 6.6 shows the charging operation for I_d_ref of -17A. This operation provides 1.445 kW of charging into the batteries. The DC charging current is presented in Figure 6.7. The 120 Hz oscillation is typical for a single phase operation.

Figure 6.6: Battery charging ($I_{d_ref} = -17$ A and $I_{q_ref} = 0$ A): (a) Utility grid voltage, (b) Utility grid current, (c) Utility grid voltage/Inverter input current, (d) d-axis and q-axis values of inverter current.

Figure 6.7: Charging: battery current for $I_{d_ref} = -17$ A

6.2.4 Standalone mode of inverter operation

When the grid is available, the system runs in grid connected mode, where the power control is done through current control. If the utility grid is not available, an inverter can run in islanded (standalone) mode, where the power control is done through voltage control. When the utility grid voltage or frequency is out of the specified range of IEEE nominal values, then the system automatically moves into standalone operation. The system provides power to the local connected loads by controlling the voltage at PCC through RMS voltage control. Figure 6.8 shows the results of an inverter operation in standalone mode. A resistive load of 13Ω is connected across the inverter to test the standalone operation, for which the current from the inverter is 13.07 A (peak) and is shown in Figure 6.8 (b). The output voltage is controlled at 120 V rms magnitude at 60 Hz and the local loads are adjusted such that the inverter provides 1.109 kW in

standalone operation. As soon as the utility grid becomes available, then the inverter goes into grid connected mode of operation through phase synchronization.

Figure 6.8: Standalone mode of inverter operation: (a) Inverter output voltage, (b) Inverter output current, (c) Load voltage/Load current.

6.3 Voltage harmonic control in weak utility grid

The proposed voltage harmonic control algorithm in Chapter III is tested with an experimental setup. The utility grid has significant harmonics presented in section 6.3.1.

6.3.1 Harmonic measurement of utility grid voltage

As shown in Figure 6.9 the utility voltage has significant higher order harmonics. Before implementing the harmonic controller, we have implemented RLSE technique to be able to estimate the higher order harmonics. The magnitude and the phase of the fundamental are presented in Figure 6.10 as expected the phase is zero.

Figure 6.9: Weak utility grid voltage

The 3rd, 5th, 7th and 9th harmonic estimations presented in Figures 6.11, 6.12, 6.13 and 6.14 respectively. Figure 6.15 shows the FFT analysis of the utility voltage. Based on these results we can conclude that the 3rd and 5th harmonic voltage is quite dominant. For that reason we have done our experimental control on reducing 3rd and 5th harmonics.

Figure 6.10: Fundamental component of utility grid voltage: (a) Magnitude measurement, (b) phase angle measurement.

Figure 6.11: 3rd harmonic measurement of utility voltage: (a) Magnitude measurement, (b) Phase angle measurement

Figure 6.12: 5th harmonic measurement of utility voltage: (a) Magnitude measurement, (b) Phase angle measurement

Figure 6.13: 7th harmonic measurement of utility voltage: (a) Magnitude measurement,
(b) Phase angle measurement

Figure 6.14: 9th harmonic measurement of utility voltage: (a) Magnitude measurement, (b) Phase angle measurement

Figure 6.15: Harmonic analysis of the utility grid voltage

6.4 Utility grid voltage harmonic control without active power injection

The proposed voltage harmonic control algorithm is tested experimentally. Since the 3rd and 5th harmonics are predominant in the experimental grid, we have focused on implementing 3rd and 5th harmonic voltage controllers. Figure 6.16 shows the grid voltage before and after the control operation, and the injected 3rd harmonic current into the utility grid. As shown in Figure 6.17 the 3rd harmonic of the utility voltage is reduced to 1.95 V from 8.5 V. The THD is reduced to 2.61 % from 5.68 %.

The 5th harmonic control only operation is presented in Figure 6.18. The THD is reduced to 2.74 % from 5.68 % and the 5th harmonic content is reduced to 1.57 V from 8.45 V as shown in Figure 6.19.

After testing the controller separately we combined the 3rd and 5th harmonic voltage controllers. Figure 6.20 shows the performance of the 3rd and 5th harmonic voltage controllers acting together. The voltage THD is reduced to 1.94 % as presented in Figure 6.21.

Figure 6.16: 3rd harmonic control in d-q frame: (a) Utility grid voltage before harmonic control, (b) Current injected into utility grid for 3rd harmonic control, (c) Utility grid voltage after 3rd harmonic control, (d) Utility grid voltage/current

Figure 6.17: Harmonic analysis of utility grid voltage after 3rd harmonic control

Figure 6.18: 5th harmonic control in d-q frame: (a) Utility grid voltage before harmonic control, (b) Current injected into utility grid for 5th harmonic control, (c) Utility grid voltage after 5th harmonic control, (d) Utility grid voltage/current

Figure 6.19: Harmonic analysis of utility grid voltage after 5th harmonic control

Figure 6.20: 3rd and 5th harmonic control in d-q frame: (a) Utility grid voltage before harmonic control, (b) Current injected into utility grid for 3rd and 5th harmonic control, (c) Utility grid voltage after 3rd and 5th harmonic control, (d) Utility grid voltage/current

Figure 6.21: Harmonic analysis of utility grid voltage after 3rd and 5th harmonic control

6.5 Utility grid voltage harmonic control with active power injection

The proposed controller is tested with the experimental system in parallel with the power processing of the fundamental frequency. The 3rd harmonic control operation with 2.5 kW power processing is presented in Figure 6.22. As shown in Figure 6.23 the THD is reduced to 2.58% and the magnitude of the 3rd harmonic content is reduced to 1.98 V from 8.5 V. The 5th harmonic control operation with 2.5 kW power processing is presented in Figure 6.24. The THD is reduced to 2.93 % and the 5th harmonic content is reduced to 1.7 V as shown in Figure 6.25.

The 3rd and 5th harmonic voltage controllers are combined to inject 37 A peak current into the utility grid. Figure 6.26 shows the utility voltage before and after the

voltage harmonic controller. As shown in Figure 6.27 the THD is reduced to 2.38 %, the 3rd harmonic voltage is reduced to 3.77 V and the 5th harmonic is reduced to 2.2 V.

Figure 6.22: 3rd harmonic in utility grid voltage with active power: (a) Utility grid voltage before harmonic control, (b) Current injected into utility grid for 3rd harmonic control, (c) Utility grid voltage after harmonic control, (d) Utility grid voltage/current

Figure 6.23: Harmonic analysis of utility grid voltage after 3rd harmonic and active/reactive power control

Figure 6.24: 5th harmonic in utility grid voltage with active power: (a) Utility grid voltage before harmonic control, (b) Current injected into utility grid for 5th harmonic control, (c) Utility grid voltage after harmonic control, (d) Utility grid voltage/current

Figure 6.25: Harmonic analysis of utility grid voltage after 5th harmonic and active power control

Figure 6.26: Active power and 3rd and 5th harmonic control: (a) Utility grid voltage before harmonic control, (b) Current injected into utility grid for active and harmonic control, (c) Utility grid voltage after harmonic control, (d) Utility grid voltage/current

Figure 6.27: Harmonic analysis of utility grid voltage after 3rd harmonic, 5th harmonic and active/reactive power control

6.6 Summary

A bi-directional inverter is tested extensively with active and reactive power processing. It is also tested to provide power to the DC side. The results of standalone operation are presented in detail. The harmonic analysis and measurement of harmonics in the utility grid voltage are presented. The voltage harmonic control with active power injection is tested experimentally and the results are presented.

CHAPTER VII

CONCLUSION AND FUTURE WORK

7.1 Conclusion

The voltage harmonic control which controls the harmonics in the utility grid voltage while providing the sustainable energy to the grid is developed and tested. The developed algorithm controls active and reactive power to the utility grid as well as the harmonics on it. The harmonic measurement in the utility grid voltage is done using RLSE. The designed control algorithm is simulated in the Matlab/Simulink environment. The harmonic control is tested while the inverter is providing active/reactive power to the utility grid. The THD of the utility voltage is reduced to 1.24% from 7.30% using the proposed control technique.

The developed control algorithm is implemented in hardware and the obtained results are validated against the simulated results. The 3rd harmonic in the utility grid voltage is reduced to 1.95 V from 8.5 V, and the 5th harmonic is reduced to 1.7 V from 8.45 V. The THD of the utility grid voltage is reduced to 3.28% from 5.68% while providing active/reactive power with little harmonic current. The simulation and experimental results are shown in Table 8.1.

Table 8.1: Simulation and experimental results

Harmonic order	Simulation results		Experimental results	
	Before control (V)	After control (V)	Before control (V)	After control (V)
3rd	6.6	1	8.5	1.95
5th	8.45	1	8.45	1.57
7th	5	1	-	-
9th	2.9	0.5	-	-
THD (%)	7.30	1.24	5.68	1.94

The experimental results of harmonic control while processing active power are as follows.

- 3rd harmonic and active power control
 - THD is reduced to 2.58 % from 5.68 % with 2.5 kW active power
- 5th harmonic and active power control
 - THD is reduced to 2.93 % from 5.68 % with 2.5 kW active power
- 3rd and 5th harmonic and active power control
 - THD got reduced to 2.38 % from 5.68 % while processing 2.5 kW of active power.

7.2 Future work

Further theoretical analysis can be done for the interaction of the individual voltage harmonic controllers between each other. The algorithm can be simplified to be able to implement in the controllers on a low speed processors. The algorithm can be tested for three phase implementations.

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APPENDICES

APPENDIX A

CONTROL ALGORITHM IN C/C++

```

/*****
// Headers and Libraries
*****/
#include<cdefbf506f.h>
#include<stdio.h>
#include<sysreg.h>
#include<signal.h>
#include<sys\exception.h>
#include<math.h>

/*****
// General System Parameters and Constants
*****/

// Crystal clock frequency [kHz]
#define Cry_clock 25000
// Multiplier for core clock
#define core_clock_multiplier 16
// core/system clock ratio
#define sys_clock_ratio 5
// do not change
#define Core_clock Cry_clock
* core_clock_multiplier
#define sys_clock Core_clock
/ sys_clock_ratio
// PWM clock
#define PWM_clock
    (sys_clock)
// Desired switching frequency [Hz]
#define SWTNG_freq 19920
// Desired PWM switching frequency [Hz]
#define PWM_freq SWTNG_freq
    // Switching frequency
// Desired Deadtime [nsec]
#define Deadtime 2000
// Desired Pulse Width of Sync Signal [nsec]
#define SyncWidth 5000
// Desired fundamental frequency [Hz]
#define Fundamental_freq 60
// single- vs. double-update mode

```

```

#define Update_mode          0          // 0 for
single, 1 for double
// Desired ADC SCLK frequency [kHz]
#define ADC_sample_freq      (16666/2)
// Timer Clock
#define TMR_clock
    (sys_clock)

// Defining PWM period, PWM dead time, Syn Width and Timer Period
#define PWM_Period            (PWM_clock *1000 / PWM_freq / 2)
#define PWM_DeadTime          (Deadtime / 1000 * PWM_clock / 2
/ 1000)
#define PWM_SyncWidth         (SyncWidth / 1000 * PWM_clock /
1000)
#define TIMER_Period          (TMR_clock *1000 / SWTNG_freq )
#define B_Size                (SWTNG_freq / Fundamental_freq)

/*****
// prototypes//
*****/
void Init_portPWM(void);
void PWM_Init(int Param_Period, int Param_Deadtime, int
Param_SyncWidth, int update_mode);
void Enable_PWM(void);
void Disable_PWM(void);
void PWM_dutycycle(int);
void TEST_PWM(void);
void Init_Interrupts(void);
void Init_Ports(void);
void Init_DMA(void);
void Init_PWM(void);
void Init_ACM(void);
void Init_SPORT(void);
void Disable_ACM(void);

/*****
//Constants for Algorithms
*****/
#define pi                    3.14159265358
#define N                    800

// Constants for PLL
#define tou                    0.00002521
#define T                    0.1/SWTNG_freq
#define Ts                    10*T
#define Kpp                    306
#define Kip                    10.88

#define L                    0.001

```

```

#define WL          2*pi*60*L

// Reference Values for Controllers
#define Id_r        13*40/13
#define Iq_r        -13*5/13

#define b           0.33333*200*10*T           //Ki*T
#define Tl          T/2
#define d           0.1/(2*pi)
#define e           270/1024
#define f           0.2118012422360224844

#define O_vol_lim   1.15*170                   //380
#define U_vol_lim   0.85*170                   //294
#define O_fre_lim   62
#define U_fre_lim   58

// Predictive Variables
#define R            0.2
#define LoT         13
#define ToL         0.0055

/*****
//Interrupt Handlers
*****/
EX_INTERRUPT_HANDLER(EVENT_STATUS_INTERRUPT);
EX_INTERRUPT_HANDLER(EVENT_MISSED_INTERRUPT);
EX_INTERRUPT_HANDLER(Sport1_RX_ISR);
EX_INTERRUPT_HANDLER(PF_interrupt_A);
EX_INTERRUPT_HANDLER(PF_interrupt_B);
EX_INTERRUPT_HANDLER(Timer0_ISR);

/*****
//Variable Initialization
*****/

// ADC accessing Buffers
short int Rx_Buffer[4];
short int test_ACM_ES[2];
short int Vin1,Vin1p=0,Vin2,Vin3,Vin4,Vin5,temp1;

// Buffers for Dealy functions
double
VBuffer[332]={0},VBuffer1[332]={0},Vdc[332]={0},Cs[332]={0},
Sn[332]={0},S4[332]={0};

// Buffers for Algorithm testing
double Test[N]={0},Test1[N]={0},Test2[N]={0},Test3[N]={0},

```

```

Test4[N]={0},Test5[N]={0};

// Variables for PLL
double Va,Vb,Vdn,Vdp = 0,Vd,Vqn,Vqp = 0,Wn,Wp = 0,fp=0, fn,f1p=0,
f1n;
double xpl,ypl,zpl,Qin,ype=0,zpe=0,Qip = 0,temp=0, Vln, Vlp,
Vl1n;

// Variables for average
double avg=0, avg1=0;

// Variables for Grid Connection
int New_start=1, count_time=0, Timer_status=0, Phase_locked=0,
Fault=0, Relay_ok=0,Zero_cro = 0, Zero_crossing = 0, Relay_on =
0;

// Variables for fault
int O_fre = 0, U_fre = 0, O_vol = 0, U_vol = 0, Isl = 0, fault
=0;

//Variables for turning on DSP
int zerocrossk = 0, waitaftergridcon = 0,Zero_crossing_inverter =
0,Zero_cro_inverter = 0;

// Variables for Voltage Control
double er, yrp=0, yrn, theta,Vrms=0,Vrms_a=0;

// Variables for Current Controller
double Ia,Ib,Idn,Idp = 0,Iqn,Iqp = 0;
double edn,edns=0,eqns=0,eqn,edp=0,eqp=0;

// Variables for Reference generation
double Vd_rn,Vd_rp,Vq_rn,Vq_rp,Van,Vbn;

// Variables for Vdc and Idc
double Vdcn,Vdcn1,Vdcp,Vc;

//Duty cycle Variables
double dutyCycle = 0,dutyl=0;

//Variables for buffers, counters and biasing
int
count=0,i=0,j=0,h=0,k=0,l=0,n=0,g5=0,delay=0,delay1=0,k1=0,k4=0,
m=0,z=0,red = 0, x=0,r=0,s1=0;

//Predictive Controller Variables
double Idf = 0, Iqf = 0, Vde = 0, Vqe = 0, Vd_re=0, Vq_re=0,
eprdp = 0, eprdn=0, eprqp = 0, eprqn = 0;

```



```

// Calling Test PWM function
TEST_PWM();

// Constants

//a = (T/tou-1)*Kpp;
//b = Ki*T;
//T1 = T/2;

/*****
//Generation of DSP Shutdown and DSP clear and Relay Pulses
*****/

// Configuring PF9 for GPIO
*pPORTF_FER = ~(PF9|PF8|PF7);

// Declaring PF9 direction as output
*pPORTFIO_DIR |= 0x0380;

// Setting PF9 as high (+ve edge as high)
*pPORTFIO_SET = 0x0180;

/*****
//Initialization of Timer and timer interrupt
*****/

// Enable the Peripheral functionality for Timer1
*pPORTG_FER = 0x0020;

// Muxing PortG for timer output
*pPORTG_MUX = 0x00000000;

// Enable Timer0 Interrupt at SIC
*pSIC_IMASK1 = 0x00000001;

// Map Timer0_ISR to EVT12: Timer0 default priority is 5
register_handler(ik_ivg12, Timer0_ISR);

// Enable IVG12 at core level -->IMASK for Timer0 interrupt

*pIMASK = 0x001F;
*pIMASK = 0x101F;
*pIMASK = 0x901F;

// Configure Timer0 in PWM mode
*pTIMER0_CONFIG =
PWM_OUT|PERIOD_CNT|PULSE_HI|TOGGLE_HI|IRQ_ENA;

// Timer0 period is assigned to Timer0 period register

```

```

    *pTIMER0_PERIOD = TIMER_Period;

    // As timer0 is in PWM mode, declare pulse width for PWM
    *pTIMER0_WIDTH= 300;

    // Enable Timer0, which generates interrupt automatically
    *pTIMER_ENABLE = 0x0001;

    // Enter to infinite loop
    while(1)
    {
        //asm("nop");
    }

    // Disable ACM module if timer is not enabled
    Disable_ACM();

}

/*****
*   Function:    TEST_PWM
*   Description: This initializes the PWM module and enables PWM.
*****/
void TEST_PWM(void)
{
    // Initialize PWM port.
    Init_portPWM();

    // init the PWM block
    PWM_Init(PWM_Period, PWM_DeadTime, PWM_SyncWidth,
Update_mode);

    // Enable PWM
    //Enable_PWM();
}

/*****
*   Function:    Init_portPWM
*   Description: PIN initialization
*****/
void Init_portPWM(void)
{
    // pin muxing
    /* Enable PWM0_AH, PWM0_AL, PWM0_TRIP, PWM0_SYNC, PWM0_BH,
BL, CH, CL */
    *pPORTF_MUX |= 0x4050;
    *pPORTF_FER |= (PF15 | PF14 | PF8 | PF7 | PF6 | PF5 | PF4 |
PF3 | PF2 | PF1 | PF0);
}

```

```

/*****
*   Function:      Enable_PWM
*   Description:   Enable PWM0
*****/
void Enable_PWM(void)
{
    // now enable the PWM unit
    *pPWM0_CTRL |= 0x0001;
}

/*****
*   Function:      Initialize_PWM
*   Description:   Initializes PWM module
*****/

void PWM_Init(int Param_Period, int Param_Deadtme, int
Param_SyncWidth, int update_mode)
{
    // PWM Status Register
    *pPWM0_STAT = PWM_SYNCINT | PWM_TRIPINT;

    //PWM period, half the value to the timer0 period register
based on SCLK
    //*pPWM0_TM = Param_Period;
    *pPWM0_TM = TIMER_Period/2;

    // PWM dead time (500 ns )
    *pPWM0_DT = Param_Deadtme;

    // PWM synchronous width, used this as PWM clear signal
    *pPWM0_SYNCWT = Param_SyncWidth;

    *pPWM0_SEG = 0x0103;

    // PWM control register
    //*pPWM0_CTRL = PWMSYNCINT_EN | PWMTRIPINT_EN | PWM_SRMODE
| PWM_SYNCSEL | (update_mode << 2);
    *pPWM0_CTRL = 0x01F0;
}

/*****
*   Function:      PWM_dutycycle
*   Description:   Assign duty cycle
*****/

void PWM_dutycycle(dutyCycle)
{
    //Duty cycle of Channel A
    *pPWM0_CHA = dutyCycle;
}

```

```

        //Duty cycle of Channel B
        *pPWM0_CHB = dutyCycle;

        //Duty cycle of Channel C
        *pPWM0_CHC = dutyCycle;
    }

/*****
*   Function:    Disable_PWM
*   Description: Disable PWM module
*****/
void Disable_PWM(void)
{
    *pPWM0_CTRL    &= ~0x1;
}

/*****
*   Function:    Init_ACM
*   Description: Initialization of ACM module
*****/
void Init_ACM(void)
{
    // Creating Event time 50 for first event
    *pACM_ET0=10;

    // Creating Event time 400 for second event
    *pACM_ET1=300;

    // Creating Event time 700 for third event
    *pACM_ET2=600;

    *pACM_ET3=900;
    // Write(ACM_EMSK, 0xffff, 16bit)
    *pACM_EMSK=0xffff;

    // First event configuration - Accessing channel 2 data
    // Data in single mode, direct data.
    *pACM_ER0=0x031;

    // Second event configuration - Accessing channel 3 data
    // Data in single mode, direct data.
    *pACM_ER1=0x033;

    // Second event configuration - Accessing channel 3
data    // Data in single mode, direct data.
    *pACM_ER2=0x035;

```

```

    *pACM_ER3=0x039;

    //write(ACM_IMSK, 0xffff, 16bit)
    *pACM_IMSK=0xffff;

    //write(ACM_TC1, 0x8810, 16bit);
    //Tcsw = 'd10, Th = 'd15, Tz = 'd2
    *pACM_TC1=0x880f;

    //Set proper frame sync polarity, ADC drive edge, trigger
    selects and Sport Unit select before enabling Sport.
    //write(ACM_TC0, 0x0001, 16bit);
    //CKDIV = 'd1, Ts = 'd0 (programming ACM_TC0 at the end)
    *pACM_TC0=0x000;
}

/*****
*   Function:     TEST_ACM
*   Description: Enables ACM modules and produces the triggering
pulses
*****/

void TEST_ACM( void )
{
    // Configure Port G for ACM module
    *pPORTG_FER=0xffdf;

    // Configure Port F for ACM module
    *pPORTH_FER=0xffff;

    // DMA configuration for data accessing
    //write( SPORT1_RXDMA_CFG, 0x0007, 16bit);
    *pDMA4_CONFIG=0x0087;

    //write(ACM_CTL, 0x4012, 16bit)
    //CSPOL=Active Low; ADC neg_edge drive; TRGSEL0=10;
    TRGSEL1=00; SPORT Unit 1 Selected;
    *pACM_CTL=0x4022;

    //Also enable ACM here so that Sport can start receiving
    clock as soon as it is enabled.
    *pACM_CTL|=0x01;//Enable ACM

    Enable_PWM();

    // To give rising edge triggering
    for(i=0;i<2;i++);
    *pPORTGIO_CLEAR=0x0020;

```

```

        for(i=0;i<2;i++);
        *pPORTGIO_SET=0x0020;

        // Check the ACM status, whether event is completed or not
        while((ACM_STAT & 0X0004)!=0X0004)
        {
            asm("nop;");
        }
    }

/*****
*   Function:    Init_Ports
*   Description: Initializes the peripheral, direction and edge
for ACM, SPORT, DMA and PWM
*****/

void Init_Ports(void)
{
    // Initialize port F as peripheral
    *pPORTF_FER =0xFFFF;

    // Initialize Port F direction as Input to access ADC
    *pPORTFIO_DIR=0x0000;

    // Enable the Input
    *pPORTFIO_INEN=0x0400;

    // Set the polarity for Port F
    *pPORTFIO_POLAR=0x0000;

    // Set triggering edge for Port F
    *pPORTFIO_EDGE=0x0400;

    // Enable Interrupt masks for Port F
    *pPORTFIO_MASKA=0x0400;
    //*pPORTFIO_MASKA_SET=0x0200;

    // Enable Port G direction as output PG6
    *pPORTGIO_DIR=0x0020;
    //*pPORTGIO_INEN=0x0020;

    // Port F, G and H muxing for PWM, SPORT, ACM and DMA
    *pPORTF_MUX = 0x4050;
    *pPORTG_MUX = 0x0080;
    *pPORTH_MUX = 0x00;
}

/*****
*   Function:    Init_PWM

```

```

*   Description: Initializes the PWM1 module for ACM triggering
*****/

void Init_PWM(void)
{
    // Initialize synchronous width for PWM1 module
    *pPWM1_SYNCWT=0x1;

    // Initialize PWM1 period for PWM1 module
    *pPWM1_TM=4016/2;
}

/*****
*   Function:      Init_DMA
*   Description:  Initializes and Configures DMA module
*****/
void Init_DMA(void)
{
    //configure DMA module - write( SPORT1_RXDMA_CFG, 0x0087,
16bit)
    *pDMA4_CONFIG=0x0086;

    // Set starting address for DMA access, as Buffer address
    *pDMA4_START_ADDR=(void*)Rx_Buffer;

    // 1-D DMA access, access one byte of data for every sample
    *pDMA4_X_MODIFY=2;

    // No of samples for one access is four
    //write( SPORT1_RXDMA_CNT, 0x0008, 16bit)
    *pDMA4_X_COUNT=4;
}

/*****
*   Function:      Init_SPORT
*   Description:  Initializes and Configures SPORT module
*****/
void Init_SPORT(void)
{
    // Sport accesses the ADC data and transfer to memory
    // Word length of ADC data configuration
    // Write( SPORT1_RCR2, 0x000f, 16bit)
    *pSPORT1_RCR2=0x000B;

    // Set triggering, direction and synchronous frame
    //write( SPORT1_RCR1, 0x1401, 16bit) RCKFE=0; LateRFS=1;
LowRFS=1
    *pSPORT1_RCR1=0x1401;
}

```



```

/*****
*   Function:      Disable_ACM
*   Description: Disables ACM, DMA and SPORT modules
*****/
void Disable_ACM(void)
{
    // Disable SPORT - write( SPORT1_RCR1, 0x0000, 16bit)
    *pSPORT1_RCR1=0x00;

    // Disable DMA - disable_dma(SPORT1_RXD)
    *pDMA4_CONFIG=0x00;

    // Disable ACM - write(ACM_CTL, 0x0000, 16bit)
    *pACM_CTL=0x00;
}

/*****
*   Function:      Init_Interrupts
*   Description: Initialization of interrupts for Events (ACM),
SPORT
*****/

void Init_Interrupts(void)
{
    // Enabling Port and SPORT interrupts
    *pSIC_IAR3 = 0xf54ffffff;
    *pSIC_IAR2 = 0xfffff1ff;

    // EVENT_STATUS_INTERRUPT
    *pSIC_IAR6 = 0xffffffff3;

    //EVENT_MISSED_INTERRUPT
    *pSIC_IAR5 = 0x2fffffff;

    // Register handles for all interrupts
    register_handler(ik_ivg11, PF_interrupt_A);
    register_handler(ik_ivg12, PF_interrupt_B);
    register_handler(ik_ivg8, Sport1_RX_ISR);
    register_handler(ik_ivg10, EVENT_STATUS_INTERRUPT);
    register_handler(ik_ivg9, EVENT_MISSED_INTERRUPT);

    // Masking interrupts
    *pSIC_IMASK0 = 0x60040000;
    *pSIC_IMASK1 = 0x00018000;
}

/*****
*   Function:      EX_INTERRUPT_HANDLER
*   Description: Checks the event status, and updates the buffers
*****/

```

```

*****/

EX_INTERRUPT_HANDLER(EVENT_STATUS_INTERRUPT)
{
    // This makes sure that the event status interrupt is
    getting triggered
    // every time when an event is completed
    test_ACM_ES[count++]=*pACM_ES;
    if (*pACM_ES & 0x0004)
    {
        *pACM_ES = 0x0004;
    }
    else if (*pACM_ES & 0x0020)
    {
        *pACM_ES = 0x0020;
    }
    else if (*pACM_ES & 0x0100)
    {
        *pACM_ES = 0x0100;
        //disable_ACM();
    }
    else if (*pACM_ES & 0x4000)
    {
        *pACM_ES = 0x4000;
        //test_ACM_ES[j++]=*pACM_ES;
    }
    else if (*pACM_ES & 0x0002)
    {
        *pACM_ES = 0x0002;
    }
    else if (*pACM_ES & 0x0040)
    {
        *pACM_ES = 0x0040;
    }
    else if (*pACM_ES & 0x0080)
    {
        *pACM_ES = 0x0080;
    }
    else if (*pACM_ES & 0x1000)
    {
        *pACM_ES = 0x1000;
    }
}

/*****
*   Function:     EX_INTERRUPT_HANDLER
*   Description:  ISR for missed interrupts
*****/

```

```

EX_INTERRUPT_HANDLER(EVENT_MISSED_INTERRUPT)
{
    // To get this case give same ETx value for two events
    if (*pACM_MS & 0x0020)
    {
        *pACM_MS = 0x0020;
    }
}

/*****
*   Function:    EX_INTERRUPT_HANDLER
*   Description: ISR for SPORT
*****/

EX_INTERRUPT_HANDLER(Sport1_RX_ISR)
{
    *pDMA4_IRQ_STATUS=0x1;
}

/*****
*   Function:    EX_INTERRUPT_HANDLER
*   Description: ISR for PF interrupt A
*****/

EX_INTERRUPT_HANDLER(PF_interrupt_A)
{
    *pPORTFIO_CLEAR=0x0400;
}

/*****
*   Function:    EX_INTERRUPT_HANDLER
*   Description: ISR for PF interrupt B
*****/

EX_INTERRUPT_HANDLER(PF_interrupt_B)
{
    *pDMA4_IRQ_STATUS=0x1;
}

/*****
*   Function:    Disable_ACM
*   Description: Disables ACM module
*****/
void disable_ACM(void)
{
    // Disable SPORT
    *pSPORT1_RCR1&=0xfffe;

    // Disable ACM module
    *pACM_CTL&=0xfffe;
}

```

```

    // Disable SPORT
    for(i=0;i<1000;i++)
        *pSPORT1_RCR1|=0x0001;
    *pACM_CTL|=0x0001;

    // Triggering for Port F
    for(i=0;i<1000;i++)
        *pPORTFIO_CLEAR=0x0400;
    for(i=0;i<100;i++);
        *pPORTFIO_SET=0x0400;
}

/*****
*   Function:      EX_INTERRUPT_HANDLER for Timer Zero
*   Description:  Timer0 Interrupt to write algorithms
*****/

EX_INTERRUPT_HANDLER(Timer0_ISR)
{
    // *pPORTFIO_SET = 0x0200;
    // *pPORTFIO_CLEAR = 0x0200;
    *pTIMER_STATUS = 0x0001;

    // *****/
    // *****/      adc data accessing      *****/
    // *****/

    // Call TEST_ACM function, to access ADC data
    TEST_ACM();

    // Channel 1 data - DC Voltage

    if(Rx_Buffer[0]&0x0400)
        // Vin4 = (~Rx_Buffer[0]+0x0001)&0x07FF;
        Vin1 = (Rx_Buffer[0]&0x03FF );

    else

        Vin1 = Rx_Buffer[0]+0x0400;

    Vin1 = Vin1>>1;

    // Dc measurement
    Vdc[k] = Vin1;

    if(Rx_Buffer[1]&0x0400)
        Vin2 = (~Rx_Buffer[1]+0x0001)&0x07FF;

```

```

else
Vin2 = -Rx_Buffer[1];

Vin2=Vin2+26.5;

if(Rx_Buffer[2]&0x0400)
Vin3 = (~Rx_Buffer[2]+0x0001)&0x07FF;
else
Vin3 = -Rx_Buffer[2];

Vin3=Vin3-6;

Vin3=Vin3;

if(Rx_Buffer[3]&0x0400)
Vin4 = (~Rx_Buffer[3]+0x0001)&0x07FF;
else
Vin4 = -Rx_Buffer[3];

Vin4 = Vin4-22;

//*****//
//***** PLL *****//
//*****//

// Buffer Channel one data into VBuffer

VBuffer[k] = Vin3*f;

//VBuffer[k] = 870*sin(k*2*pi/332);

// Defining Va (V - alpha)
Va = VBuffer[k];

Vb = VBuffer[l];

//Define Cos and Sin functions to convert into d and q axis
Cs[k]=cos(Qin);

Sn[k]=sin(Qin);

Q3 = 3*Qin;
Q5 = 5*Qin;

S4[k4] = -5*sin(4*Qin);

// DQ axis conversion from alpha-beta axis
// Vd - direct axis Voltage

```

```

Vdn=Cs[k]*Va+Sn[k]*Vb;

// Vq - Quadrature axis Voltage
Vqn=-Sn[k]*Va+Cs[k]*Vb;

xpl = Kpp*Vqn;
ype = ype+Vqn;
ypl = Kip*ype;

zpl = xpl+ypl;

Qin = T*zpl+Qip;

Qip = Qin;

if(Qip == 0)
Qip = 0.1;
else
Qip = Qin;

// Measure frequency
fn=d*zpl;

f1n=511*fp+fn;

fn=f1n*0.001953125;

fp=fn;

Vln = Vdn;

//*****//
//***** Buffer Variables *****//
//*****//

// Produce 90 degrees delay, switching frequency is 19.92
kHz, so 83 samples give
// 90 degrees phase delay for V beta, and I beta
if(k==B_Size/4-1)
{
    l=0;
    h=1;
}
else
    l=l+1;

// Repeat the buffer for every one cycle, 19.92 kHz/60 Hz
which 332. Therefore
// samples gives one full cycle

```

```

    if(k==B_Size-1)
    {
        k=0;
        Vrms=0;

        if(x==10)
            x=x+0;
        else
            x=x+1;
        Qip=Qip+2*pi;

    }
    else
        k=k+1;

    if(k4==82)
        k4=0;
    else
        k4=k4+1;

    if(k4==2)
        delay=0;
    else
        delay=delay+1;

//*****//
//***** Grid Connection *****//
//*****//

    if(m==0)
    {
        // Check if the Grid Connection is from standalone to grid
        connection or from initial connection
        // New_Start = 1 means initial grid connection
        if(New_start==1)
        {
            // Wait for 1ms before checking the Phase Locked condition.
            As we are timer is for 50us, wait for 20 samples, which
            gives one msec
            if(Timer_status==1)
            {
                // Check the phase locked condition, Band is 2% of the peak
                value of the voltage
                if(-20<Vqn<20)
                {
                    // If Vq is in certain limit, we can lock the phase
                    Phase_locked = 1;

                    // Check Zero Crossing
                    // Check two conditions, 1) Either present sample should be
                    zero, or should cross zero

```

```

if((VBuffer[k]*VBuffer[k-1]<0)||VBuffer[k]==0)

// Set Zero_cros flag to 1, if it is crossing zero
Zero_cro = 1;

else

// present sample is not near to zero
Zero_cro = 0;

// Check the band of the sample, to make sure that exact
results
if((-10<Va<10)&& Zero_cro)
{
// Set Zero crossing to zero, confirming that Sample is at
zero.
Zero_crossing = 1;

// Over or Under voltage condition

// Check Over voltage condition
if(Vdn >O_vol_lim)
{

// 4.5 = 875.4, over voltage is 110% which is 972.8 (4.75)
O_vol = 1;

// Set fault flag to zero, if there is a fault
Fault = 1;

}
else
{

// No over voltage
O_vol = 0;

// Under voltage condition

if(Vdn < U_vol_lim)
{

// If Vqn is < 737.28 (3.6), 80% voltage

U_vol = 1;

// Set fault flag to zero, if there is a fault

Fault = 1;

```



```

    }
    else
    {

        // No Under Voltage
        U_vol = 0;

        // Check Over frequency or Under frequency condition

        // Over frequency condition
        if(fn > O_fre_lim)
        {
            // If frequency is > 60.5 Hz, set over
voltage flag

            O_fre = 1;

            // Set fault flag to zero, if there is a
fault

            Fault = 1;
        }
    else
    {
        // No Over frequency

        O_fre = 0;

        // Under frequency condition

        if(fn < U_fre_lim)
        {

            // If frequency is < 59.5 Hz, set over voltage flag

            U_fre = 1;
            // Set fault flag to zero, if there is a fault

```

```

        Fault = 1;
    }
else
    {
        // No Under frequency
        U_fre = 0;

        //*****//
        //Check Islanding Condition//
        //*****//

        Isl = 0;

        // Check the fault condition
        if(O_vol||U_vol||O_fre||U_fre)

// Set fault flag to zero, if there is a fault
        Fault = 1;
        else

// Set fault flag to 1, if there is no fault
        Fault = 0;
    }
}

}

}

else

// Check for zero crossing again
Zero_crossing = 0;
    }

```

```

else
// If the voltage (Vqn) is not under certain
limit, don't lock the phase
Phase_locked = 0;

}
else

// Wait some more time, up to 1 m sec, check the time again

{

// Check time 20 iterations, 1 m sec
if(count_time>19)
{

// Don't change the counter status, if time is 1 m sec
count_time = count_time;

// Set Time_status to 1, indicating time is 1 m sec
Timer_status = 1;
}

// Wait time is less than 1 m sec, increment the timer
else
{

// Increment the timer
count_time = count_time+1;

// Set Timer_status to "0", indicating time is
less than 1 m sec
Timer_status = 0;
}
}

else
{
// From standalone control to Grid Connection mode
//nop();
}
if(Fault == 1)
fault = 0;
else
fault = 1;

// Check all the conditions, to assign relay status
if(fault&&Phase_locked&&Timer_status&&Zero_crossing)

// Relay condition is satisfied

```

```

        Relay_ok = 1;

else

    // Relay condition is not satisfied
    Relay_ok = 0;

// Check the condition to turn on Relay
if(Relay_ok==1)

    // If relay condition is satisfied, turn on relay
    Relay_on = 1;
else

    // If relay condition is not satisfied, don't
    turn on relay
    Relay_on = 0;

// Turn on relay
if(Relay_on == 1)
{
    // Set port to 3.3 volts to turn on relay
    *pPORTFIO_SET = 0x0200;

    // Turned on
    m=1;

    //Store zero cross time
    zerocrossk = k;

}
else

{
    // Don't turn on the relay
    *pPORTFIO_CLEAR = 0x0200;

    *pPORTFIO_SET = 0x0100;

}
}
else
{
    if(x==10)
    {
        // Check Over voltage condition
        if(Vln > O_vol_lim)
        {

// 4.5 = 875.4, over voltage is 110% which is 972.8 (4.75)

```

```

        O_vol = 1;

// Set fault flag to zero, if there is a fault
        Fault = 1;

    }
else
    {

        // No over voltage

        O_vol = 0;

        // Under voltage condition
        if(Vln < U_vol_lim)
        {
            // If Vqn is < 737.28 (3.6), 80% voltage
            U_vol = 1;

            // Set fault flag to zero, if there is a fault
            Fault = 1;

        }

    else
    {
        // No Under Voltage
        U_vol = 0;
// Check Over frequency or under frequency condition

        // Over frequency condition
        if(fn > O_fre_lim)
        {

// If frequency is > 60.5 Hz, set over voltage flag
            O_fre = 1;

            // Set fault flag to zero, if there is a fault
            Fault = 1;

        }

    else
    {

        // No Over frequency
        O_fre = 0;

        // Under frequency condition
        if(fn < U_fre_lim)

```

```

        {
            // If frequency is < 59.5 Hz, set over voltage flag
            U_fre = 1;

            // Set fault flag to zero, if there is a fault
            Fault = 1;
        }

        else
        {
            // No Under frequency
            U_fre = 0;

            //*****Check Islanding Condition*****//
            Isl = 0;

            // Check the fault condition

            if(O_vol||U_vol||O_fre||U_fre)

                // Set fault flag to zero, if there is a fault
                Fault = 1;
            else

                // Set fault flag to 1, if there is no fault
                Fault = 0;
        }
    }

    if(Fault==1)
    {
        // Don't turn on the relay
        *pPORTFIO_CLEAR = 0x0200;

        *pPORTFIO_SET = 0x0100;

        s1=1;

        //m=0;
    }
}

```

```

//*****
//***** RMS Calculation *****
//*****

if( *pPORTFIO_SET&&0x0200)
{
    if(zerocrossk == k)
    {
        if(waitaftergridcon == 4)
            waitaftergridcon = waitaftergridcon + 0;
        else
            waitaftergridcon = waitaftergridcon + 1;
    }
    else
        waitaftergridcon = waitaftergridcon + 0;

    if(waitaftergridcon == 4)
    {
        if(Zero_crossing_inverter == 0)
        {
            // Check Zero Crossing
            // Check two conditions, 1) Either present
            // sample // should be zero, or should cross
            // zero
            if((VBuffer[k]*VBuffer[k-1]<0)||VBuffer[k]==0)
                // Set Zero_cro flag to 1, if it is crossing zero
                Zero_cro_inverter = 1;

            else

                // present sample is not near to zero
                Zero_cro_inverter = 0;

            // Check the band of the sample, to make sure
            // that exact results
            if((-10<Va<10)&& Zero_cro_inverter)

                // Set Zero crossing to zero, confirming that
                // Sample // is at zero.
                Zero_crossing_inverter = 1;

            else

                Zero_crossing_inverter = 0;
        }
    }
}

```

```

    }

    if(Zero_crossing_inverter == 1)

    {

        //if((*pPORTFIO_SET==0x0200)&&(Vrms_a>50))
        if((*pPORTFIO_SET&&0x0200))
        {
//*****
//***** Control Algorithm *****
//*****

            if(red == 0)

            {

                //Turn on Inverter
                *pPORTFIO_CLEAR = 0x0100;

                g5=1;

            }

            else
            red=1;

            if(s1==1)
            {
                red=2;
                s1=2;
            }
//*****
//***** RLS 3rd harmonic measurement *****
//*****

            if(excl == 1)

            {

                C3 = cos(Q3);

                excl = 2;

            }

            else if(excl == 2)

            {

                S3 = sin(Q3);

```



```

        exc1 = 3;

    }

    //    else if(exc1 == 3)
    //    {
    //        exc1 = 1;
    //    }

    else if(exc1 == 3)
    {

        Xr1 =C3 ;

        Xr2 = S3;

        Er = VBuffer[k]-Xr1*Theta1-Xr2*Theta2;

        //Xr1_Xr2_P1 = Xr1*Xr1*P1;

        Xr1_Xr2_P3 = Xr1*Xr2*P3;

        Xr1_Xr2_P2 = Xr1*Xr2*P2;

        //Xr1_Xr2_P4 = Xr1*Xr2*P4;

        Xr1_Xr1  =Xr1*Xr1;

        Xr1_Xr1_P1  =Xr1_Xr1*P1;

        Xr2_Xr2 = Xr2*Xr2;

        Xr2_Xr2_P4 = Xr2_Xr2*P4;

        De = Xr1_Xr1_P1+Xr1_Xr2_P3+Xr1_Xr2_P2+Xr2_Xr2_P4;

        //De = Xr1*(Xr1*P1+Xr2*P3)+Xr2*(Xr1*P2+Xr2*P4);

        De = 1/(1+De);

        //Pn1 = P1*(1-De*(Xr1*(Xr1*P1+P2*Xr2)));

        Pn1 = P1*(1- De*(Xr1_Xr1_P1+Xr1_Xr2_P2));

```

```

//Pn2 = P2*(-De*(Xr2*(Xr1*P1+P2*Xr2)));

Pn2 = P2*(-De*(Xr1_Xr2_P1+Xr2_Xr2*P2));

//Pn3 = P3*(-De*(Xr1*(Xr1*P3+P4*Xr2)));

Pn3 = P3*(-De*(Xr1_Xr1*P3+Xr1_Xr2_P4));

//Pn4 = P4*(1-De*(Xr2*(Xr1*P3+P4*Xr2)));

Pn4 = P4*(1-De*(Xr1_Xr2_P3+Xr2_Xr2_P4));

Thetan1 = Theta1 + Er*(Pn1*Xr1+Pn3*Xr2);

Thetan2 = Theta2 + Er*(Pn2*Xr1+Pn4*Xr2);

Theta1 = Thetan1;

Theta2 = Thetan2;

P1 = Pn1;
P2 = Pn2;
P3 = Pn3;
P4 = Pn4;

Vq3 = Theta1;

Vd3 = Theta2;

excl = 4;

}

//*****
//***** RLS 3rd harmonic control *****
//*****

else if(excl == 4)
{

edn3 = V3d_r - Theta2;//Vd3;

eqn3 = V3q_r - Theta1;//Vq3;

edn3s = edn3s+edn3;

```

```

eqn3s = eqn3s+eqn3;

xdn3 = Ki3*edn3s;

xqn3 = Ki3*eqn3s;

Vd_r3 = Kp3*edn3+xdn3;

Vq_r3 = Kp3*eqn3+xqn3;

Va3 = S3*Vd_r3+C3*Vq_r3;

if(Van > 50)
    Van=50;
else if(Van < -50)
    Van=-50;

    exc1 = 1;

}

//*****
//***** RLS 5th harmonic measurement *****
//*****

if(exc1 == 1)

{

C5 = cos(Q5);

exc1 = 2;

}

else if(exc1 == 2)

{

    S5 = sin(Q5);

    exc1 = 3;

}

//    else if(exc1 == 3)

```

```

//      {
//          exc1 = 1;
//      }

else if(exc1 == 3)
{

    Xr1 =C5 ;

    Xr2 = S5;

    Er = VBuffer[k]-Xr1*Theta1-Xr2*Theta2;

    //Xr1_Xr2_P1 = Xr1*Xr1*P1;

    Xr1_Xr2_P3 = Xr1*Xr2*P3;

    Xr1_Xr2_P2 = Xr1*Xr2*P2;

    //Xr1_Xr2_P4 = Xr1*Xr2*P4;

    Xr1_Xr1 =Xr1*Xr1;

    Xr1_Xr1_P1 =Xr1_Xr1*P1;

    Xr2_Xr2 = Xr2*Xr2;

    Xr2_Xr2_P4 = Xr2_Xr2*P4;

De = Xr1_Xr1_P1+Xr1_Xr2_P3+Xr1_Xr2_P2+Xr2_Xr2_P4;

//De = Xr1*(Xr1*P1+Xr2*P3)+Xr2*(Xr1*P2+Xr2*P4);

    De = 1/(1+De);


    //Pn1 = P1*(1-De*(Xr1*(Xr1*P1+P2*Xr2)));

    Pn1 = P1*(1- De*(Xr1_Xr1_P1+Xr1_Xr2_P2));

    //Pn2 = P2*(-De*(Xr2*(Xr1*P1+P2*Xr2)));

    Pn2 = P2*(-De*(Xr1_Xr2_P1+Xr2_Xr2*P2));

    //Pn3 = P3*(-De*(Xr1*(Xr1*P3+P4*Xr2)));

```

```

Pn3 = P3*(-De*(Xr1_Xr1*P3+Xr1_Xr2_P4));
//Pn4 = P4*(1-De*(Xr2*(Xr1*P3+P4*Xr2)));

Pn4 = P4*(1-De*(Xr1_Xr2_P3+Xr2_Xr2_P4));

Thetan1 = Theta1 + Er*(Pn1*Xr1+Pn3*Xr2);
Thetan2 = Theta2 + Er*(Pn2*Xr1+Pn4*Xr2);

Theta1 = Thetan1;
Theta2 = Thetan2;

P1 = Pn1;
P2 = Pn2;
P3 = Pn3;
P4 = Pn4;

Vq5 = Theta1;
Vd5 = Theta2;

excl = 4;

}

//*****
//***** RLS 5th harmonic control *****
//*****

else if(excl == 4)
{
edn5 = V5d_r - Theta2;//Vd5;
eqn5 = V5q_r - Theta1;//Vq5;
edn5s = edn5s+edn5;
eqn5s = eqn5s+eqn5;
xdn5 = Ki5*edn5s;
xqn5 = Ki5*eqn5s;

```

```

Vd_r5 = Kp5*edn5+xdn5;

Vq_r5 = Kp5*eqn5+xqn5;

Va5 = S5*Vd_r5+C5*Vq_r5;

if(Va5 > 50)
    Va5=50;
else if(Va5 < -50)
    Va5=-50;

    excl = 1;

}

//*****
//***** Fundamental current control *****
//*****

VBuffer1[k] = Vin4*0.076923;

Ia = VBuffer1[k];

// Defining Ib (I - beta)
    if(h==1)
//Ib = VBuffer1[l1+l2];
    Ib = VBuffer1[l];
else
    Ib=0;

// DQ axis conversion from alpha-beta axis
// Id - direct axis Current
Idn=Cs[k]*Ia+Sn[k]*Ib;

// Iq - Quadrature axis Current
Iqn=Sn[k]*Ia-Cs[k]*Ib;

//step 1
eprdn = Idn - Idp;

eprqn = Iqn - Iqp;

Vdest = Vdp-.1*R*Idp-.1*LoT*eprdn+WL*Iqp;
Vqest = Vqp-.1*R*Iqp-.1*LoT*eprqn-WL*Idp;

```

```

// step 2
Kqin = 377/Qip;

S6 = -0.0276; //*sin(4*Qin);

Vde = Kqin*Vdest*(S6); //-0.0038*S6);
Vqe = Kqin*Vdest*(1+S6); //-0.0038*S6);

// step 5
Idf = (Vdn-R*Idn+WL*Iqn-Vde)*ToL+Idn;
Iqf = (Vqn-R*Iqn-WL*Idn-Vqe)*ToL+Iqn;
//step 6
Idf = 0.5*(Idf+Idn);
Iqf = 0.5*(Iqf+Iqn);

// step 7
erdn = Id_r-Idf+S4[delay];
erqn = Iq_r-Iqf;

Vd_re = R*Idf+LoT*erdn-WL*Iqf+Vdest;
Vq_re = R*Iqf+LoT*erqn+WL*Idf+Vqest;

Van=Cs[k]*Vd_re+Vq_re*Sn[k];
//Vbn=-Sin[k]*Vq_rn+Vd_rn*Cos[k];

if(Van > 300)
    Van=300;
else if(Van < -300)
    Van=-300;

    }

    }

    }

    }

if (n==N)
    n=0;
else
    n=n+1;

// Predictive Algorithm

Vdp = Vdn;
Vqp = Vqn;

```

```

Idp = Idn;
Iqp = Iqn;

eprdp = eprdn;
eprqp = eprqn;

erdp = erdn;
erqp = erqn;

//*****//
//***** DutyCycle *****//
//*****//

// DutyCycle same as grid Voltage
dutyCycle = (Van+Va3+Va5)*2044/Vdc[k];
duty1=1000;

// Set the maximum and minimum limit for duty cycle
if(dutyCycle > duty1)

// Maximum positive value for dutyCycle
    dutyCycle=duty1;

if(dutyCycle < -duty1)

    // Minimum value of duty cycle
    dutyCycle=-duty1;

// Assign duty cycle to duty cycle register
PWM_dutycycle(dutyCycle);

// Accessing the Variables to check the results by plotting
them.
Test[n]=Va;
Test1[n]=Vdn;
Test2[n]=Vqn;
Test3[n]=Iqn;
Test4[n]=Vdn;
Test5[n]=dutyCycle;
}

```


APPENDIX B

PCB LAYOUT AND SCHMATICS

B.1 PCB layout of the interface board

B.1.1 Top layer

B.1.2 Inner layer 1

This image shows a complex PCB layout for a system unit. The board is populated with a variety of electronic components, including integrated circuits, capacitors, and resistors. The layout is organized into functional blocks, with labels indicating specific components like 'SMOULF', 'V80111 CPU', 'V80112 CPU', and 'V80120 CPU'. The board also features several connectors and test points.

Schematics of the interface board are presented below.

Title		File		Date	
c:\Title		c:\Title		Date	
Rev	Document Number	Rev	Document Number	Rev	Document Number
0	<Doc>	0	<Doc>	0	<Doc>
Rev	Document Number	Rev	Document Number	Rev	Document Number
0	<Doc>	0	<Doc>	0	<Doc>
Rev	Document Number	Rev	Document Number	Rev	Document Number
0	<Doc>	0	<Doc>	0	<Doc>

Title		
<Title>		
Size	Document Number	Rev
A	<Doc>	<RevCode>
Date:	Tuesday, May 24, 2011	Sheet 3 of 9

Title		
Connector		
Size	Document Number	Rev
B	<Doc>	<RevCode>
Date:	Tuesday, May 24, 2011	Sheet 4 of 9

Title			
Current_sensors			
Size	Document Number	Rev	
C	<Doc>	<RevCode>	
Date:	Tuesday, May 24, 2011	Sheet	5 of 9

Level shifting of the six PWM signals from 3.3V to 15V.

PWM Signals from DSP to Module

Title			PWM_LevelShifter
Size	Document Number	Rev	<RevCode>
B	<Doc>		
Date:	Tuesday, May 24, 2011	Sheet	9 of 9