CHARACTERIZATION AND DESIGN OF VOLTAGE-MODE CONTROLLED FULL-BRIDGE DC/DC CONVERTER WITH CURRENT LIMIT

A thesis submitted in partial fulfillment

of the requirements for the degree of

Master of Science in **Electrical Engineering**

By

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2018

Wright State University

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25 April 2018
Date of Defense

I HEREBY RECOMMEND THAT THE THESIS PREPARED UNDER MY SUPERVISION BY Nathaniel R. Smith ENTITLED Characterization and Design of Voltage-Mode Controlled Full-Bridge DC/DC Converter with Current Limit BE ACCEPTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF Master of Science in Electrical Engineering.

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Abstract

Smith, Nathaniel, R. M.S.E.E. Department of Electrical Engineering, Wright State University, 2018. *Characterization and Design of Voltage-Mode Controlled Full-Bridge DC/DC Converter with Current Limit.*

Advancements in Direct Current (DC) electrical power systems have enabled new functionality in many, varied applications. Discrete power semiconductor devices are increasing in efficiency, switching frequency, and power density, resulting in greater usage of DC power management and distribution methods, including DC/DC conversion. DC distribution lacks inherent capability to safely and effectively break fault current, particularly in mobile solutions, where larger and slower electromechanical switching devices are not optimal or feasible. One solution is to design a low-energy breaking point into a switching power supply. Simpler converter designs, with a lower number of switching devices, have been modeled and can be functionally utilized for this purpose. However, these designs cannot easily or efficiently provide isolation between the source and the load. A full-bridge DC/DC converter can accomplish this task with galvanic isolation through a transformer. The full-bridge DC/DC converter is fairly complex to analyze with state-space analysis and does not have an existing averaged model. This thesis focuses on developing averaged and small-signal models for the full-bridge DC/DC converter; validating the small-signal averaged models by simulation in SABER circuit simulation software; and using the validated models to design a full-bridge DC/DC converter for simulation in SABER. The converter power stage is designed along with a Type II controller, a comparative current limit, non-Zero-Voltage-Switching gate drives, and a synchronous rectifier. The designed converter is evaluated for closed-loop stability against step changes in input volt-

age, load current, and reference voltage. The results are provided to show sufficient response of the full-bridge DC/DC converter, given the design parameters. The proposed architecture accommodates future work to reduce DC fault let-through energy.

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Acknowledgment

I would first like to thank God for the strength, wisdom, and perseverance to complete the Master's program and this thesis. Accordingly, I would also like to extend my deepest gratitude to my wife and my children, for their enduring patience, encouragement, and love throughout the entire program of study. Without them, I would not have completed this program, especially to the level of success that was accomplished. Thank you for your critical support.

I would like to extend my sincere appreciation to my advisor for his assistance and for sharing his depth of knowledge in the field of power electronics through the last few years. This was critical to any achieved success. I also would like to extend thanks to the teaching assistant staff for timely support with regard to relevant advanced concepts and help with MATLAB, SABER Circuit Simulator, and LaTeX.

I would finally like to thank those who have supported the research effort with their encouragement, flexibility, and understanding throughout the program.

1 Introduction

1.1 Full-Bridge DC/DC Converter

The full-bridge DC/DC converter is a DC/AC inverter, which transfers energy through a transformer to a full-wave rectifier, forming a DC/DC converter. In this project, the output network is an *RLC* filter. The power stage of the full-bridge DC/DC converter consists of eight switching power devices, for the purposes of increased power capability and increased efficiency. This offers an advantage over designs with fewer switches, such as half-bridge.

1.2 Thesis Objectives

This thesis objective is to methodically analyze, model, design, and evaluate the full-bridge DC/DC converter.

1. Characterization of the Full-Bridge DC/DC Converter

    - A reduced, averaged model is developed.
        - This *has not been accomplished, to date*, for the full-bridge DC/DC converter, and is proposed as a *main contribution* of this thesis.

2. Design and Implementation of a closed-loop controlled full-bridge DC/DC converter in simulation [1].

    - The four switches of the full-bridge allow for reduced switch stress for the same power transferred.
    - A voltage-mode controller is implemented.
    - A transformer separates the inverter from the rectifier, providing galvanic isolation between source and load.

- A transformer may also be utilized to ease some of the step-up or step-down stress of the converter.

3. A current limit comparator will be placed in-line between the voltage-mode control output and the gate drives.

    - The current limit reduces the duty cycle, resulting in less energy delivered to the transformer.
    - This also limits the secondary-side and load power dissipation in an overload condition.

1.3 Background

Direct Current (DC) electrical systems are gaining in popularity and utilization, primarily due to advancements in power electronics. DC systems allow for better regulation; better integration of multiple voltage levels; higher transient response; better integration with DC storage devices; and greater range flexibility with electrical machine operation.

However, certain simpler and established functions in Alternating Current (AC) electrical systems remain more complex or prohibitive to implement in DC systems. Particularly for electrical systems on mobile transportation platforms, in which size and weight are at a premium, it is advantageous to raise the operating bus voltage to drive larger electrical loads with acceptable conductor losses. AC electrical voltage is easily adjusted with a transformer, at a size and weight premium; but DC electrical voltage adjustment requires linear regulation or DC/DC conversion to adjust DC electrical voltage. This complicates design and integration. Furthermore, AC electrical systems are more simply interrupted in the case of electrical faulting by utilizing classical I^2t thermally-protective breakers at the natural zero-crossing, allowing let-through energy proportional to the AC operating period. This reduces the required

energy level to break, also resulting in a smaller size for the breaker hardware. DC electrical systems do not have a natural zero crossing, meaning the electrical break must naturally be at full fault current. Even so, sudden electrical disconnect requires a bus clamp to limit the bus voltage from spiking to a level in which the breakdown voltage is reached for the media between terminals. If further advancements in DC electrical systems are to see wider acceptance, a solution is required to adjust voltage level with high efficiency, coupled with the ability to galvanically isolate the input from the output.

1.4 Motivation

As stated, DC systems inherently lack a zero-crossing; thus, they are susceptible to catastrophic fault let-through energy. The following devices have been classically utilized for DC fault prevention.

1. Fuses

    - Fuses are physically designed to be weakest portion of a circuit, providing a controlled failure in the presence of overload current.

    \+ Fuses provide galvanic isolation following a trip event.

    \- Fuses cannot be ”reset” and require physical replacement, following a trip event.

    \- There is difficulty sizing fuses properly, especially for very fast, very energetic events.

2. Contactors / Relays

    - Contactors and relays are controllable mechanical devices which may be commanded open due to some external event.

    \+ Contactors and relays provide galvanic isolation.

+ These are resettable following a trip event.

- Contactors and relays are physically susceptible to bouncing, which may result in welded contacts under fault conditions.

- Due to mechanical coupling, contactors and relays have a relatively longer circuit-breaking time constant.

3. Solid-State Switching Devices

+ Solid-state devices can operate at high switching frequencies and can be operated in the linear region.

+ These are relatively small devices and can be arrayed to limit current per device.

- Solid-state devices do *not* have inherent galvanic isolation.

  o They are susceptible to inductive kick, resulting in uncontrolled overvoltage failure.

- Solid-state devices have higher in-line losses due to switching and conduction, when compared to other breaking methods.

There is a need for a new design which provides rapid, low-energy breaking functionality and combines this circuit protection with other functions, such as inversion or conversion. The intent of this thesis project is to develop and demonstrate this aforementioned capability with flexibility for future improvements toward the design of a robust DC breaker with inherent conversion capabilities.

1.5 Challenges with a Full-Bridge Design

A comprehensive design must start with an analysis of the expected operation. For simpler circuits, validated models may already exist from which the design may be

based. If a model is not available for a given circuit, but the circuit is simple enough, state-space analysis or circuit averaging may not be overly tedious.

The full-bridge converter includes eight switching devices and produces complex waveforms and interactions to analyze, relative to other converters. Since there are no available averaged models, and state-space analysis will be cumbersome, one must start with periodic circuit analysis and work toward an averaged model of the full-bridge converter.

Realistically, each component will include parasitic impedance. To establish a baseline model, it may be expedient to make some assumptions which result in the exclusion of certain parasitic impedance values. However, removing all parasitic losses would be a Type 2 model error, falsely representing an under-damped system, which will affect system stability and controller design. A balance must be found to simplify model development, while not overly affecting model performance.

A general assumption may be made that output filter component values dominate parasitic impedance values. For this to be a valid assumption, filter components must be sufficiently large. However, a larger filter capacitor may cause high inrush current, limited only by the filter inductor's current $i_L = \frac{1}{L}\int_0^t v_L dt$ [1] and in-line resistance, such as the capacitor's equivalent series resistance (ESR). In this case, it is difficult to implement a soft-start function to charge the capacitor slowly, while exiting discontinuous conduction mode (DCM) quickly at start-up, without affecting steady-state operation of the converter.

Finally, an implementation of the full-bridge DC/DC converter with current limit will require a reliable current measurement method. Current measurement must be accurate; must have wide bandwidth; and must impose limited impact on the output current. The current limit must simply integrate with the voltage mode controller and the gate drive.

2 Steady-State Analysis

2.1 Power Stage of the Full-Bridge DC/DC Converter

The full-bridge DC/DC consists of eight switching devices and is seen in Figure 2.1. There are four active switches, S_1 through S_4, functioning as an inverter on the transformer's primary side. Switches S_1 and S_4 are grouped as switch pair "A," and are switch simultaneously in hard-switched configurations. Switches S_2 and S_3 are grouped as switch pair "B" and are turned on 180^o from switch pair "A." The configuration places the input voltage V_I across the transformer's primary winding for the period of time $D_A T$, while $-V_I$ is placed across the transformer's primary winding for the period of time $D_B T$. With time $(1 - D_A T)$ and time $(1 - D_B T)$ included, a modified periodic sine wave is imposed on the primary side of the transformer [1].

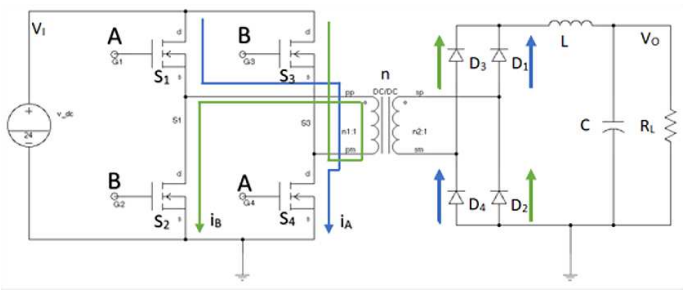

Figure 2.1: Basic circuit diagram of a full bridge DC/DC converter.

The secondary side of the transformer will reflect the primary signal by a factor of the turns ratio n of the ideal transformer, as shown in Equation 2.1,

$$n = \frac{N_{pri}}{N_{sec}} = \frac{V_{pri}}{V_{sec}} = \frac{I_{sec}}{I_{pri}} [2]. \tag{2.1}$$

The full-wave rectifier is formed with four switching devices. These can be diodes, as shown in Figure 2.1, but can also be active devices, such as MOSFETs. The transformer is wound to maintain polarity through to the secondary side, so the modified sinusoid is passed to the rectifier input. The rectifier ideally switches with the same duty cycle and phase as the inverter. Therefore, D_1 and D_4 form the

rectifier's switch pair "A," and D_2 and D_3 form the rectifier's switch pair "B." The four switches convert the full wave of the modified sinusoid to DC over the full switching period.

The output filter arrangement is identical to the LCR of a standard buck converter. This will be helpful when modeling and validating the full-bridge converter small-signal model.

2.2 Assumptions for the Average Model Analysis

As previously stated in Section 1.5, certain assumptions must be made to simplify the average model analysis.

1. The maximum ideal duty cycle per switch pair A or switch pair B is 50%, to prevent shorting of the source, known as "shoot-through" [1]:

$$D_{max} = D_{A,max} + D_{B,max} = 0.5 + 0.5 = 1.0 = 100\% \tag{2.2}$$

2. Linear and non-linear devices are assumed to be somewhat ideal [1].

   - Parasitic resistances are included, so conducting losses may be included in the linear average model.
   - Parasitic inductances and capacitances are excluded, so switching losses are neglected.

3. All MOSFETs are identical, and all diodes are identical [1].

4. Conducting resistance R_F and conducting voltage loss V_F are linear and constant, for the rectifying diodes. Off-state resistance is infinite [1].

5. Conducting resistance r_{DS} and conducting voltage loss $I_S r_{DS}$ are linear. Off-state resistance is infinite [1].

6. Load resistance R_L, filter inductance L, and filter capacitance C are linear, time-invariant, and frequency independent [1].

7. The transformer is considered ideal [2].

    - The reactance is assumed to be zero [1].
        - The winding capacitance is neglected.
        - The magnetizing inductance is neglected.
        - The leakage inductance is neglected.
    - The turns ratio relationship, given in Equation 2.1, is linear.
    - The reluctance $\Re$ is ideal, such that the flux $\phi_{pri} = \phi_{sec}$ [1].

2.3 Cyclic States of Operation

The waveforms for the basic, ideal full-bridge DC/DC converter are seen in Figure 2.2. The absolute levels and timestamps are not terribly important, as the waveforms are simply a reference for analysis. These waveforms were generated using SABER circuit simulation software [18]. Two periods are shown for clarity. Each period is divided into four states, according to the status of the primary gate drives. These four states complete one period. During normal, steady-state operation, states 1-4 repeat.

1. State 1

    - At time $t = 0$, "A" switches are turned on.
    - "A" diodes are conducting.

2. State 2

    - At time $t = D_A T$, "A" switches are turned off. "B" switches are also off.

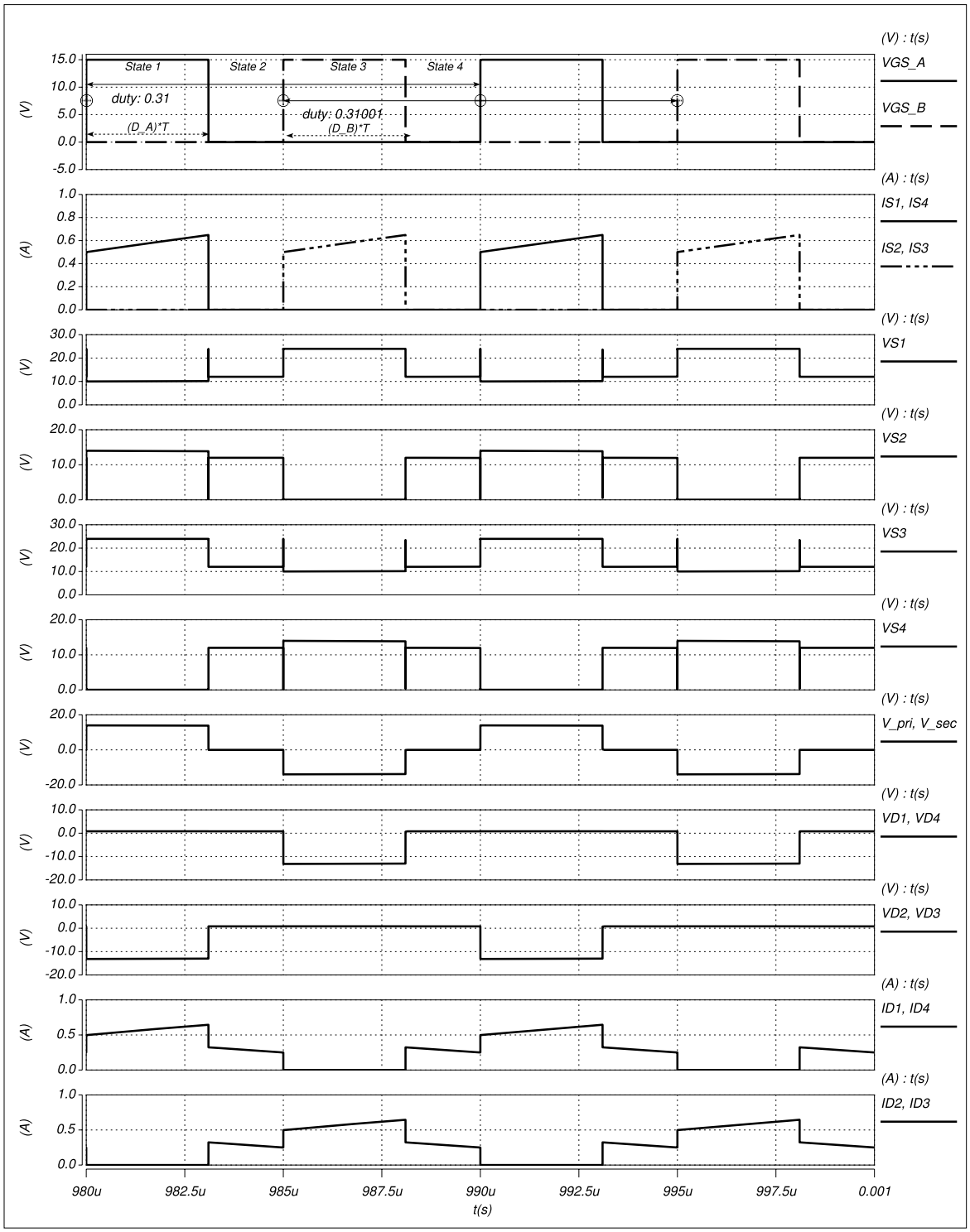

Figure 2.2: General waveforms for the basic full bridge DC/DC converter circuit [1] [18].

- The transformer voltage collapses, placing all four rectifying diodes in parallel.
- All rectifying diodes are conducting at half the *State 1* diode current, assuming equivalent diodes.

3. State 3
   - At time $t = \frac{T}{2}$, "B" switches are turned on.
   - "B" diodes are conducting.
4. State 4
   - At time $t = D_B T + \frac{T}{2}$, "B" switches are turned off.
   - The transformer voltage collapses, placing all four rectifying diodes in parallel.
   - All rectifying diodes are conducting at half the *State 1* or *State 3* diode current, assuming equivalent diodes.

The switches can each be approximated as dependent current sources, with conducting resistance r_{DS}. The diodes can each be approximated as dependent voltage sources, with conducting resistance R_F and conducting voltage loss V_F.

2.4 Time-Averaged Equations

2.4.1 Time-Averaged Currents

The waveforms are foundational to the formulation of the model. One must assume a steady-state average to form an averaged model. Let the duty cycles D_A and D_B be equivalent over the period T, per Equation 2.2, for non-ZVS operation. The terminal voltage produced at the secondary side of the transformer will be

$$V_{sec} = \frac{V_{pri}}{n} = DV_I \frac{N_{sec}}{N_{pri}} = \frac{DV_I}{n} = \frac{2D_A V_I}{n} = \frac{2D_B V_I}{n}. \tag{2.3}$$

The switch current must also be defined. The switch current is the same through the series switches S_1 and S_4: this is the current I_A. One should note that, due to the earlier assumption that the duty cycles were equal for the average model analysis, the switch currents I_A and I_B should be equal as well, over a steady-state period. It is expedient to define this switch current I_S in terms of the inductor current I_L, but the inductor is on the other side of the transformer. In reference to Equation 2.1, the turns ratio n is defined for current as well. Therefore,

$$I_A = I_{S1} = I_{S4} = \frac{1}{T}\int_0^{D_A T} \frac{I_L dt}{n} = \frac{D_A I_L}{n} + I_L(0). \tag{2.4}$$

Recalling Equation 2.2, one may conclude that

$$I_A = \frac{D I_L}{2n} + I_L(0). \tag{2.5}$$

The total average current delivered, per period, to the primary transformer coil includes both I_A and I_B, such that

$$I_{pri(ave)} = D I_S = \frac{D I_L}{2n} + \frac{D I_L}{2n} + I_L(0) = \frac{D I_L}{n} + I_L(0). \tag{2.6}$$

The inductor current, in terms of the switch current, is then

$$I_L = \frac{n I_S}{D} - I_L(0). \tag{2.7}$$

The diodes conduct in pairs during the remainder of the period, and the total diode rectifier current has continuous conduction. The diode current relationship to the inductor current does not depend on the transformer turns ratio, as both are on the secondary side. The rectifying diodes are separated into two equal branches "A" and "B," just as the primary-side inverter switches were separated. Per Figure 2.2, the following equation can be obtained, as

$$\begin{aligned} I_{D_1(ave)} = I_{D_4(ave)} = I_{D_A(ave)} &= \int_0^T I_L dt \\ &= I_L D_A T + \frac{I_L(1 - D_A T)}{2} + \frac{I_L(1 - D_B T)}{2} + I_L(0). \end{aligned} \tag{2.8}$$

Again, recalling Equation 2.2, the diode current for the steady-state period $\frac{T}{2}$ can be expressed as:

$$\begin{aligned} I_{DA(ave)} &= I_L D_A T + I_L(1 - D_A T) + I_L(0) \\ &= I_L D_A T + I_L - I_L D_A T + I_L(0) = I_L + I_L(0). \end{aligned} \tag{2.9}$$

Thus, for the full period T,

$$I_{D(ave)} = 2I_{DA(ave)} = 2I_{DB(ave)} = I_{L(ave)}. \tag{2.10}$$

It is established, then, that the average diode current is equal to the average inductor current. For the full-bridge DC/DC converter, this also equates the average diode current to the average steady-state output current.

2.5 Modeling

2.5.1 Unreduced Model

The unreduced model is shown in Figure 2.3. This model explicitly equates the physical circuit with representative circuit elements, without averaging or reduction.

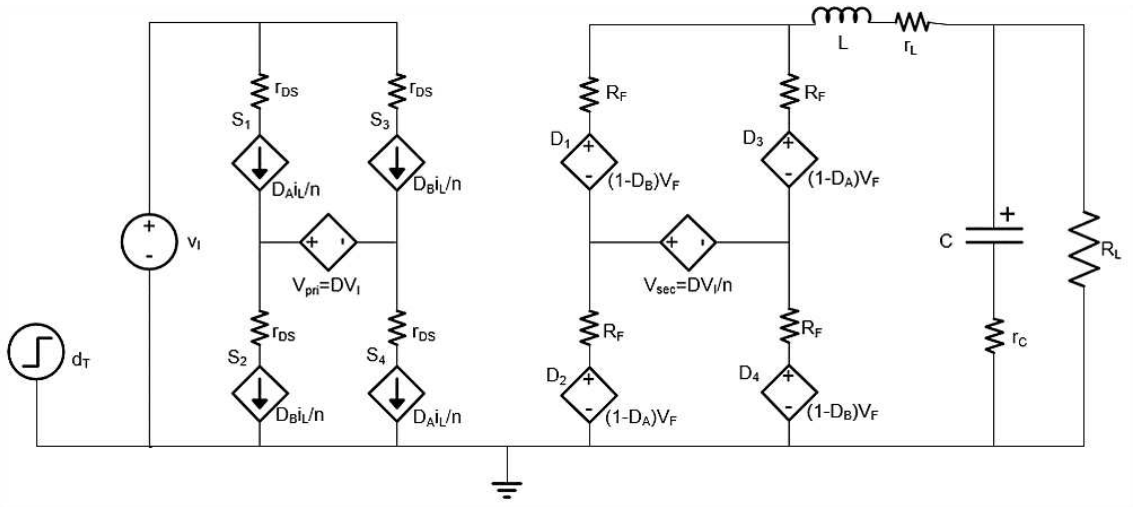

Figure 2.3: The unreduced model of full-bridge DC/DC converter.

2.5.2 Averaged Resistance

The resistance associated with each discrete switching device will be included in the circuit proportional to that device's duty cycle. In order to establish an averaged model, these resistances must also be averaged over the steady-state period.

Using the established assumption that all switches are equal, and the duty cycles for the switched pairs "A" and "B" are also equal, it is simplest to evaluate the averaged resistance starting with one MOSFET. In order to find the average resistance, the principle of conservation of energy must be observed [7]. To evaluate equivalent energy transfer, the root-mean-square current must be utilized. This analysis will simply start with switch S_1. The current is

$$I_{S1,rms}^2 = \frac{P_{1,rDS}}{r_{DS}} = \frac{1}{T}\int_0^{D_A T} i_{S1}^2 dt = \frac{1}{T}\int_0^{D_A T} I_L^2 dt = I_L^2 D_A T + I_L(0). \tag{2.11}$$

This reduces to

$$I_{S1,rms} = \sqrt{I_L^2 D_A} = I_L\sqrt{D_A} = \frac{I_{S1}\sqrt{D_A}}{nD_A} = \frac{I_{S1}}{n\sqrt{D_A}}. \tag{2.12}$$

The power dissipated by switch $S1$ is

$$P_{1,r_{DS}} = I_{S1,rms}^2 r_{DS} = I_{S1}^2 \frac{r_{DS}}{n^2 D_A}. \tag{2.13}$$

The averaged MOSFET resistance of switch S_1 is

$$r_{DS,ave(S_1)} = \frac{r_{DS}}{n^2 D_A}. \tag{2.14}$$

This results in an averaged MOSFET resistance of

$$r_{DS,ave(S)} = \frac{4r_{DS}}{n^2 D}. \tag{2.15}$$

Next, the averaged diode resistance must be found. Recall that the diodes are always conducting, unlike the singular diode in a simpler converter. Because of this, the diode resistance R_F will be the same in the diode and inductor branches of the

averaged model, due to conservation of energy. The total diode series resistance does not utilize the turns ratio, since it resides on the secondary side of the transformer with the inductor.

Once again, the waveforms in Figure 2.2 are key to interpreting the activity of the diodes over a period. One can observe that two diodes conduct with the half duty cycles, while all four diodes conduct during the remainder of the period, as the transformer's secondary coil voltage collapses, shorting the diode branches "A" and "B" together. This results in the following:

$$R_{F,ave(D_A)} = \frac{2R_F}{D_A} + \frac{2R_F}{(1-D_A)} + \frac{2R_F}{(1-D_B)}, \tag{2.16}$$

$$R_{F,ave(D_B)} = \frac{2R_F}{D_B} + \frac{2R_F}{(1-D_A)} + \frac{2R_F}{(1-D_B)}. \tag{2.17}$$

Combining these two equations,

$$R_{F,ave(D_A,D_B)} = \frac{2R_F}{D_A} + \frac{2R_F}{D_B} + \frac{4R_F}{(1-D_A)} + \frac{4R_F}{(1-D_B)}. \tag{2.18}$$

Combined with Equation 2.2, this reduces to

$$R_{F,ave(D_A)} = \frac{4R_F}{D_A} + \frac{8R_F}{(1-D_A)}. \tag{2.19}$$

Averaged over the period,

$$R_{F,ave(D)} = \frac{8R_F}{D} + \frac{16R_F}{2-D} = \frac{8R_F(2-D) + 16R_F D}{D(2-D)}. \tag{2.20}$$

The averaged resistance in the diode branch is therefore

$$R_{F,ave(D)} = 8R_F \left(\frac{2+D}{2D-D^2}\right). \tag{2.21}$$

2.5.3 Averaged Voltage

The diodes switch together in switched pairs, opposite to the primary-side switches. That is, when switch pair "A" is active, diode pair "B", which includes diodes D_2

and D_3, is conducting. Each diode pair conducts with a forward voltage of $2V_F$ for its switched period. For the diodes in the "A" branch,

$$V_{F_A,on(ave)} = \int_0^{D_A T} 2V_F dt = 2V_F D_A = V_F D. \tag{2.22}$$

Similarly, in the "B" branch,

$$V_{F_B,on(ave)} = 2V_F D_B = V_F D. \tag{2.23}$$

For the portions of time $(1 - D_A T)$ and $(1 - D_B T)$, the primary-side switches are off, and the transformer secondary voltage has collapsed. All four diodes conduct. This puts two diodes in parallel, having the same forward voltage. For the two diodes in the "A" branch,

$$V_{F_A,off(ave)} = 2V_F(1 - D_A) = 2V_F\left(1 - \frac{D}{2}\right) = V_F(2 - D). \tag{2.24}$$

For the two diodes in the "B" branch,

$$V_{F_B,off(ave)} = 2V_F(1 - D_B) = 2V_F\left(1 - \frac{D}{2}\right) = V_F(2 - D). \tag{2.25}$$

When diode branches "A" and "B" are in parallel during this time, they share the same voltage. Therefore,

$$V_{F,off(ave)} = 2V_F(2 - D). \tag{2.26}$$

Now, from Equation 2.22, Equation 2.23, and Equation 2.26, the averaged forward voltage from the full-wave diode rectifier, in the diode branch, is

$$V_{F,ave(D)} = V_{F,on(ave)} + V_{F,off(ave)} = 2V_F D + 2V_F(2 - D). \tag{2.27}$$

This simplifies to

$$V_{F,ave(D)} = 4V_F. \tag{2.28}$$

Standard diodes have a conducting voltage loss of $0.6V_{DC}$ to $0.7V_{DC}$: this loss can be increasingly detrimental as design voltage is lower. This loss also goes to heat.

For a lower output voltage, the controller must work harder to maintain the desired voltage. A self-driven synchronous rectifier, as described in [8], can function as diode rectifier, while suffering lower loss. In this case, $4V_F$ is replaced with the specified MOSFET's $4I_{S,rms}r_{DS}$, in Equation 2.28. A self-driven synchronous rectifier will be used in this design; however, the analysis will continue to refer to the rectifier with diode terms, for clarity.

2.5.4 Initial Model Reduction

Present averaged models have been completed for up to two switching elements. In this case, the full-bridge converter has *eight* switches to include in the model. Model reduction becomes equally important, in order to keep the analysis manageable.

From the unreduced model in Figure 2.3, it may be observed that the switches are modeled as current sources [1]. These are dependent on the duty cycle and inductor current only. The two switches in the switched pair "A" are current sources in series and can be combined. The two switches in the switched pair "B" are also current sources in series and can be combined.

The transformer dependent voltage sources will be reduced to the dependent voltage sources of the diode rectifier. Noting that the secondary-side voltage is of interest, one can impose the transformer secondary-side voltage V_{sec} on the diode dependent voltage sources. The primary-side voltage V_{pri} is then represented in the secondary, by reflection.

The diodes, incorporating the transformer secondary-side voltages $\frac{d_{TA}V_I}{n}$ and $\frac{d_{TB}V_I}{n}$ can be reduced by noting that the upper two and the lower two diodes are in parallel and share the same voltage. The forward voltage for each of the two dependent voltage sources is then $2V_F$, and the resistance is $R'_F = \frac{1}{2}R_{F,ave(D)}$. This is seen in Figure 2.4.

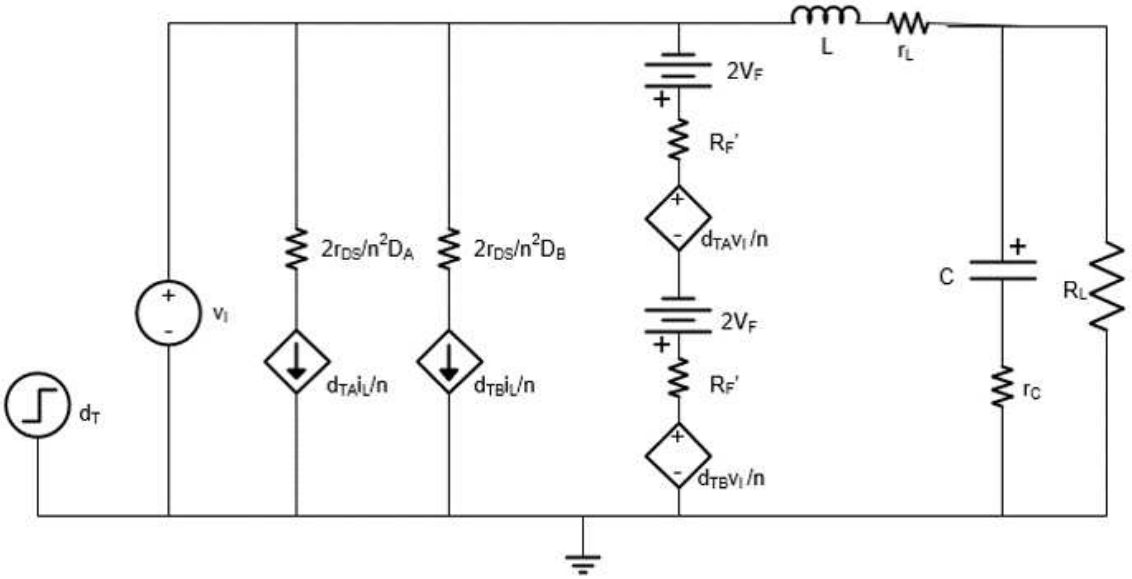

Figure 2.4: The partially reduced model of full-bridge DC/DC converter.

2.5.5 Averaged Model

As previously defined in Equation 2.2, the duty cycles D_A and D_B for the switched pairs combine to form an average duty cycle D, over the period T. It follows that the duty cycles D_A and D_B are $\frac{D}{2}$, on average, for hard-switched control. Note that, for soft-switched control, the switches may not be paired as switch pair "A" and switch pair "B," since the second switch in the pair will have a delayed duty cycle to account for a phase-shift delay [3].

For each switched pair in the PWM converter, the duty cycles D_A and D_B must be limited to 50%, to prevent shorting of the source. The duty cycle D is therefore the normalized duty cycle, such that the ideal converter has a DC transfer function of

$$M_{VDC} = \frac{D}{n} = \frac{nV_O}{V_I}. \tag{2.29}$$

The total duty cycle $d_T = D + d$ includes the average large-signal and small-signal duty cycles. Using the averaging done to this point, the switches and the diodes may now be combined with this duty cycle into a two-switch model, as seen in Figure 2.5.

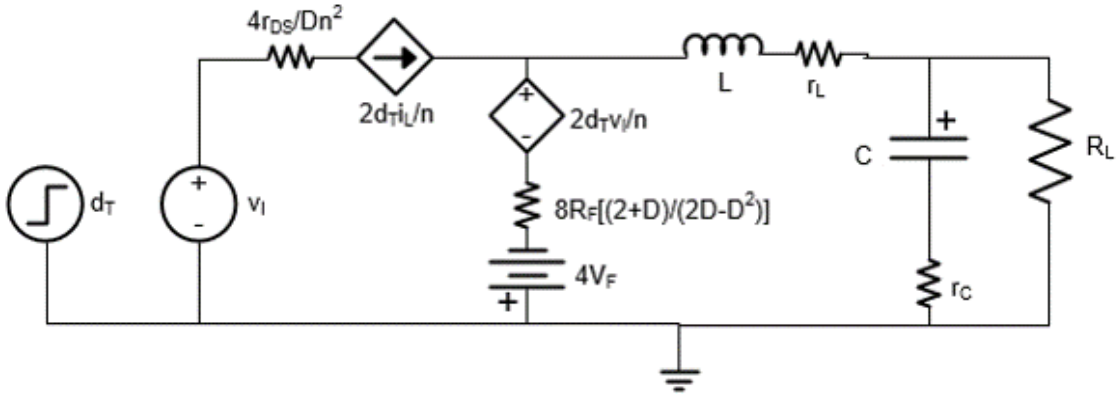

Figure 2.5: The averaged, large-signal and small-signal model of full-bridge DC/DC converter.

2.5.6 Reduced Resistance Model

To this point, the averaged resistances that have been developed are still in series with the respective components. That is, the averaged resistance for the switch may only be assumed valid in the "switch branch," and the average resistance for the diode may only be assumed valid in the "diode branch." To simplify the analysis, it is expedient to move these resistances to the "inductor branch," which is in series with the output.

However, developing the equivalent averaged resistance must be done carefully, using the law of conservation of energy to determine the equivalent averaged resistance of the MOSFET and the equivalent averaged resistance of the diode in series with the inductor. Since it is desired that these be in series with the inductor, the inductor current will flow through each equivalent averaged resistance. Therefore, the energy equations must be expressed in terms of the inductor current I_L, as expressed in [7]. For the MOSFET, the total series averaged resistance must account for the turns ratio n, as shown in Equation 2.6. Thus, recalling Equation 2.15,

$$r_{DS,ave(S)} = \frac{4r_{DS}}{n^2 D_A} = \frac{4P_{rDS}}{I_S^2}. \tag{2.30}$$

This leads to

$$4Pr_{DS} = \frac{4r_{DS}}{D}\left(\frac{I_L D}{n}\right)^2 = 4Dr_{DS}\left(\frac{I_L^2}{n^2}\right). \tag{2.31}$$

Simplifying this equation yields the equivalent averaged resistance of the MOSFET in the inductor branch as

$$r_{DS,ave(L)} = \frac{4Dr_{DS}}{n^2}. \tag{2.32}$$

It has already been established that the current through the averaged diode is continuous, and the averaged switch does not contribute current which is not processed by the diode. From Equation 2.10, the average current through the diode and the average current through the inductor are equivalent. The law of conservation of energy requires that

$$R_{F,ave(D)} = R_{F,ave(L)} = 8R_F \left(\frac{2+D}{2D-D^2} \right). \tag{2.33}$$

By the same analysis,

$$V_{F,ave(D)} = V_{F,ave(L)} = 4V_F. \tag{2.34}$$

The inductor branch now has the averaged, reduced resistances placed in series with the inductor resistance r_L. These are consolidated as

$$r = r_{DS,ave(L)} + R_{F,ave(L)} + r_L = \frac{4Dr_{DS}}{n^2} + 8R_F \frac{2+D}{2D-D^2} + r_L. \tag{2.35}$$

This reduced model is shown in Figure 2.6.

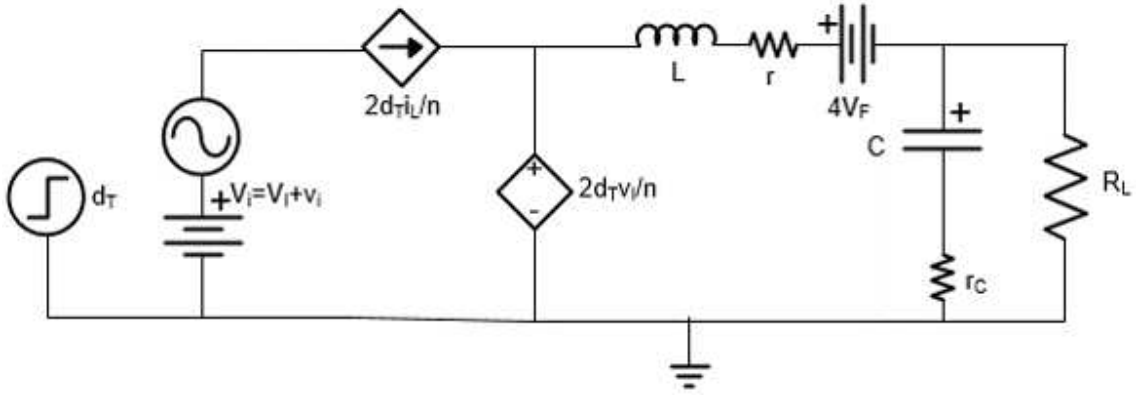

Figure 2.6: The reduced, averaged large-signal and small-signal model of the full-bridge DC/DC converter.

2.5.7 Small-Signal Averaged and Reduced Model

The purpose of the modeling exercise is to arrive at the small-signal model with less effort than required of a state-space model. The reduced model must now be further reduced to break out these small-signal components. To further develop this model, the dependent sources may be split into all possible large-signal and small-signal responses, providing the averaged DC and small-signal, low frequency model. The products $i_l d$ and dv_i may be deemed sufficiently small, as to have negligible impact on the model. This model is shown in Figure 2.7.

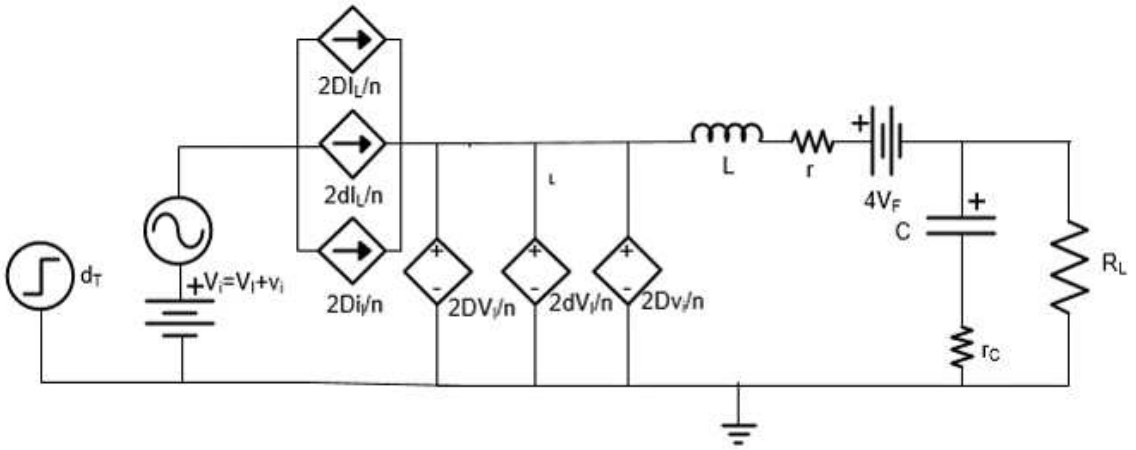

Figure 2.7: Model with explicit large-signal and small-signal switching components.

For the small-signal analysis, the averaged DC components DI_L and DV_I may be omitted, producing the small signal model, as shown in Figure 2.8. Note that the dependent current sources have no effect on the output, using current splitting theory [1]. Also note that L and r_L form Z_1; while C, r_C, and R_L form Z_2. This will be important for the small-signal analysis.

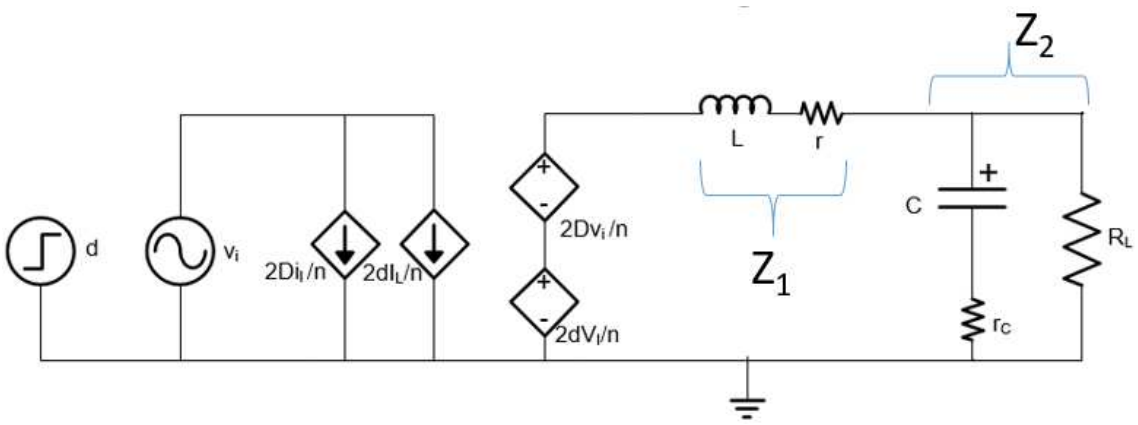

Figure 2.8: The reduced, averaged small-signal model of full-bridge DC/DC converter.

3 Small-Signal Analysis

Now that the small-signal model is obtained, the small-signal, open-loop transfer functions of the power stage may be developed. Since the full-bridge DC/DC converter is of the buck converter family, and the averaged, reduced model is similar to a buck model, given in [1], it may be anticipated that the small-signal transfer functions will be similar.

3.1 Structure of the Small-Signal Converter

The converter power stage has an open-loop, small-signal structure consisting of [1]:

1. The open-loop control-to-output transfer function, $T_p(s) = \frac{v_o(s)}{d(s)}$
2. The input-to-output transfer function, $M_v(s) = \frac{v_o(s)}{v_i(s)}$
3. The output impedance, $Z_o(s) = \frac{v_t(s)}{i_t(s)}$

The structure of the small-signal model is illustrated in Figure 3.1. These transfer functions must be developed for the full-bridge converter. They will define the small-signal response of the power stage (v_o) to perturbations in the duty cycle (d), input voltage (v_i), and load current (i_o).

3.2 Averaged Power Stage Equations

At the input terminal to the inductor, let the averaged voltage $v_{ave}(s)$ be defined as the dependent voltage output, subject to a step function perturbation, such as

$$v_{ave}(t) = 2DV_I \frac{N_{sec}}{N_{pri}} u(t) = \left(\frac{2DV_I}{n}\right) u(t). \tag{3.1}$$

The Laplace transform changes the equation to

$$v_{ave}(s) = \frac{2DV_I}{ns}. \tag{3.2}$$

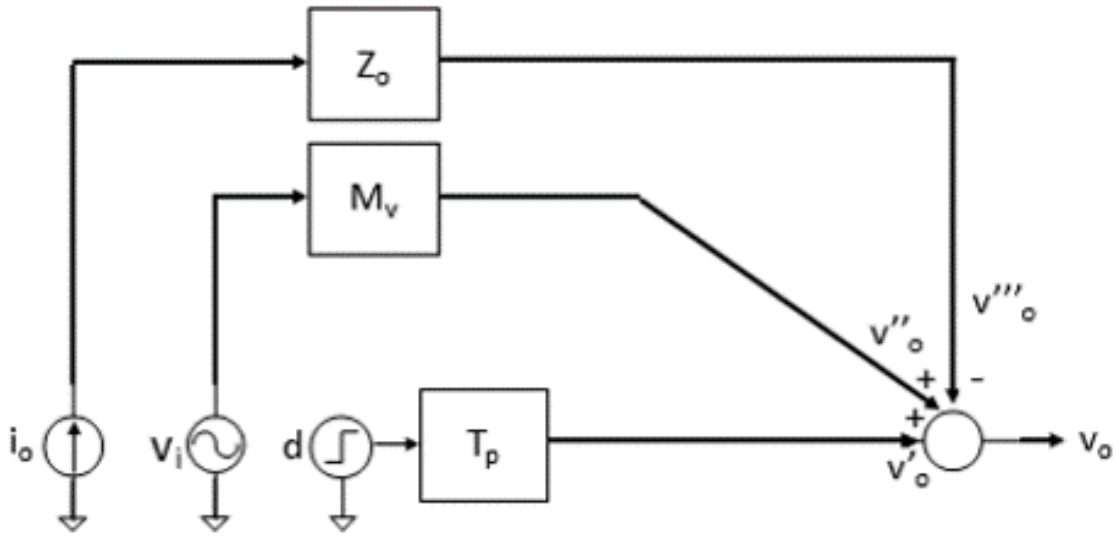

Figure 3.1: Block diagram of the small-signal model [1].

The impedances seen in Figure 2.8 can be defined as:

$$Z_1(s) = r + sL, \tag{3.3}$$

$$Z_2(s) = \frac{R_L r_C + \frac{R_L}{sC}}{R_L + r_C + \frac{1}{sC}}. \tag{3.4}$$

Let the voltage gain for the lossless circuit be

$$A_v(s) = \frac{v_o(s)}{v_{ave}(s)} = \frac{Z_2(s)}{Z_1(s) + Z_2(s)} \frac{ns}{2DV_I} = \frac{n}{LC} \frac{1}{s^2 + \frac{s}{CR_L} + \frac{1}{LC}}. \tag{3.5}$$

This is similar to the voltage gain for the buck converter, given in [1], aside from the full-bridge coefficient. The denominator of the small-signal voltage gain $A_v(s)$ fits the standard format for the lossless second-order filter, where

$$s^2 + 2\xi\omega_0 s + \omega_0^2. \tag{3.6}$$

Therefore, the frequency response may be determined for any of the small-signal transfer functions.

3.3 Small-Signal Control-to-Output Derivation

Let $T_p(s)$ be the transfer function relating the small-signal duty cycle to the small-signal output voltage, such that

$$T_p(s) = \frac{v_o(s)}{d(s)}, v_i = i_o = 0, \tag{3.7}$$

where

$$T_p(s) = \frac{2V_I}{n} \frac{Z_2(s)}{Z_1(s) + Z_2(s)} \tag{3.8}$$

is simply a divider to get the small-signal output voltage in terms of the small-signal duty-cycle-dependent voltage source in Figure 2.8. Recalling Equation 3.3 and Equation 3.4, this makes $T_p(s)$ out to be

$$T_p(s) = \frac{2V_I}{n} \left[\frac{R_L \left(r_C + \frac{1}{sC} \right)}{R_L + r_C + \frac{1}{sC}} r + sL + \frac{R_L \left(r_C + \frac{1}{sC} \right)}{R_L + r_C + \frac{1}{sC}} \right]. \tag{3.9}$$

This simplifies to

$$\begin{aligned}
T_p(s) &= \frac{2V_I}{n} \left[\frac{R_L \left(r_C + \frac{1}{sC} \right)}{\left(R_L + r_C + \frac{1}{sC} \right)(r + sL) + R_L \left(r_C + \frac{1}{sC} \right)} \right] \\
&= \frac{2V_I}{n} \left[\frac{R_L \left(r_C + \frac{1}{sC} \right)}{R_L r + r r_C + \frac{r}{sC} + sLR_L + \frac{L}{C} + sLr_C + R_L r_C + \frac{R_L}{sC}} \right] \\
&= \frac{2V_I}{n} \left[\frac{R_L (1 + sCr_C)}{sR_L rC + srr_C C + r + s^2 LCR_L + sL + s^2 LCr_C + sCR_L r_C + R_L} \right] \\
&= \frac{2V_I}{n} \left[\frac{R_L (1 + sCr_C)}{s^2 (LCR_L + LCr_C) + s (R_L Cr + Crr_C + L + CR_L r_C) + r + R_L} \right] \\
&= \frac{2V_I}{n} \\
&\left[\frac{R_L Cr_C \left(1 + \frac{1}{r_C C} \right)}{LC (R_L + r_C) \left[s^2 + \frac{s}{LC(R_L + r_C)} (R_L Cr + Crr_C + L + CR_L r_C) + \frac{r + R_L}{LC(R_L + r_C)} \right]} \right].
\end{aligned} \tag{3.10}$$

The control-to-input equation becomes

$$T_p(s) = \frac{2V_I}{n} \frac{R_L r_C}{LR_L + Lr_C} \frac{s + \frac{1}{Cr_C}}{s^2 + \left[\frac{L + C(R_L r + r_C r + R_L r_C)}{LC(R_L + r_C)s} \right] + \left[\frac{r + R_L}{LC(R_L + r_C)} \right]}. \tag{3.11}$$

The highest order of s in the numerator reveals the number of left-half plane zeroes in the power stage. In this case, there is one zero in the left-half-plane, due to its sign. The frequency of the power stage zero is simply extracted, by inspection of the numerator, as

$$\omega_z = \frac{1}{Cr_C} \tag{3.12}$$

Likewise, the highest order of s in the denominator reveals the number of left-half plane poles. There are two poles. Comparing the denominator of Equation 3.11 to Equation 3.6, one can extract the resonant frequency ω_0 and the damping ratio ξ. The squared resonant frequency is

$$\omega_0^2 = \frac{r + R_L}{LC(R_L + r_C)}. \tag{3.13}$$

Therefore, the resonant frequency is

$$\omega_0 = \sqrt{\frac{r + R_L}{LC(R_L + r_C)}}. \tag{3.14}$$

Similarly, the damping ratio can be found by solving for

$$2\xi\omega_0 = \frac{L + C(R_L r + r_C r + R_L r_C)}{LC(R_L + r_C)}. \tag{3.15}$$

The damping ratio is

$$\xi = \frac{L + C(R_L r + r_C r + R_L r_C)}{2\sqrt{LC(R_L + r_C)(r + R_L)}}. \tag{3.16}$$

These are the same equations found for the resonant frequency and damping ratio of the Pulse-Width Modulated (PWM) buck DC/DC converter, given in [1]. The differences lie in the coefficient $\frac{2}{n}$ and the contents of r, given in Equation 2.35. From Equation 3.11, the gain for the control-to-output equation can be found as

$$T_{px} = \frac{2V_I}{n}\frac{R_L r_C}{LR_L + Lr_C}. \tag{3.17}$$

When T_{px} is analyzed for DC, the inductor becomes a short circuit, and the capacitor becomes an open circuit. The DC gain is

$$T_{p0} = \frac{2V_I}{n}\frac{R_L}{R_L + r}. \tag{3.18}$$

3.4 Small-Signal Input-to-Output Derivation

Let $M_v(s)$ be the transfer function relating the small-signal input voltage to the small-signal output voltage, such that

$$M_v(s) = \frac{v_o(s)}{v_i(s)}, d = i_o = 0, \tag{3.19}$$

where

$$M_v(s) = \frac{2D}{n} \frac{Z_2(s)}{Z_1(s) + Z_2(s)} \tag{3.20}$$

is simply a divider to get the small-signal output voltage in terms of the small-signal input dependent voltage source in Figure 2.8. Equation 3.8 and Equation 3.20 are similar by $\frac{Z_2(s)}{Z_1(s)+Z_2(s)}$. Therefore, by Equation 3.11, the input-to-output transfer function equation will be

$$M_v(s) = \frac{2D}{n} \frac{R_L r_C}{LR_L + Lr_C} \frac{s + \frac{1}{Cr_C}}{s^2 + \left[\frac{L+C(R_L r + r_C r + R_L r_C)}{LC(R_L + r_C)s}\right] + \left[\frac{r+R_L}{LC(R_L+r_C)}\right]}. \tag{3.21}$$

The resonant frequency given in Equation 3.14 and the damping ratio given in Equation 3.16 remain the same as they were for the control-to-input. From Equation 3.21, the gain for the input-to-output equation can be found as

$$M_{vx} = \frac{2D}{n} \frac{R_L r_C}{LR_L + Lr_C}. \tag{3.22}$$

When M_{vx} is analyzed for DC, the inductor becomes a short circuit, and the capacitor becomes an open circuit. The DC gain is

$$M_{v0} = \frac{2D}{n} \frac{R_L}{R_L + r}. \tag{3.23}$$

3.5 Small-Signal Output Impedance Derivation

Deriving the small-signal output impedance requires a different tactic. In this case, the input voltage and duty cycle are shorted to isolate the impedance of the output filter, consisting of Z_1 and Z_2, as seen in Figure 3.2.

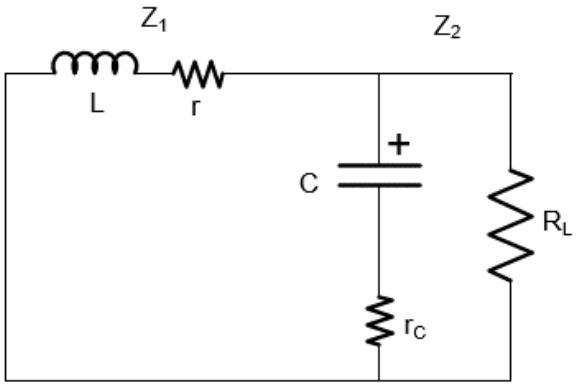

Figure 3.2: Output impedance analysis circuit.

Let $Z_o(s)$ be the transfer function relating the small-signal input voltage to the small-signal output voltage, such that

$$Z_o(s) = \frac{v_t(s)}{i_t(s)}, d = v_i = 0. \tag{3.24}$$

In order to assess the isolated output impedance, a unity test voltage v_t and a unity test current i_t are applied. Utilizing Equations 3.3 and 3.4, this results in

$$\begin{aligned} Z_o(s) &= \left(\frac{Z_1(s)Z_2(s)}{Z_1(s)+Z_2(s)}\right) = (r+sL)\left[\frac{R_L\left(r_C+\frac{1}{sC}\right)}{R_L+r_C+\frac{1}{sC}}\right]\frac{1}{\left[r+sL+\frac{R_L\left(r_C+\frac{1}{sC}\right)}{R_L+r_C+\frac{1}{sC}}\right]} \\ &= \frac{R_L\left(r+\frac{1}{sC}\right)(r+sL)}{R_L\left(r_C+\frac{1}{sC}\right)(r+sL)\left(R_L+r_C+\frac{1}{sC}\right)} \\ &= \frac{R_L\left(s^2LCr_C+sLrr_C+r\right)}{s^2LC(R_L+r_C)+s[rC(R_L+r_C)+r_CCR_L+L]+R_L}. \end{aligned} \tag{3.25}$$

The small-signal output impedance in standard form is

$$Z_o(s) = \frac{R_LLCr_C\left(s^2+\frac{L+rr_CC}{LCr_C}s+\frac{r}{LCr_C}\right)}{LC(R_L+r_C)\left[s^2+s\left(\frac{L+C(rR_L+rr_C+r_CR_L)}{LC(R_L+r_C)}\right)+\frac{R_L+r}{LC(R_L+r_C)}\right]}. \tag{3.26}$$

This can finally be expressed as

$$Z_o(s) = \frac{R_Lr_C}{R_L+r_C}\frac{\left(s^2+\frac{L+rr_CC}{LCr_C}s+\frac{r}{LC}\right)}{s^2+s\left(\frac{L+C(rR_L+rr_C+r_CR_L)}{LC(R_L+r_C)}\right)+\frac{R_L+r}{LC(R_L+r_C)}}. \tag{3.27}$$

From Equation 3.27, the gain of the output impedance transfer function is assessed as

$$Z_{ox} = \frac{R_L r_C}{R_L + r_C} \tag{3.28}$$

It may be observed that, as r_C becomes very small compared to R_L, the gain of the output impedance depresses. Somewhat counter-intuitively, the prudent designer might wish to ensure that r_C is sufficiently large enough to interact well with R_L, producing the desired frequency response. At DC, the inductor is shorted, and the capacitor creates an open circuit. The low-frequency gain for the output impedance is simply

$$Z_{o0} = R_0 = \frac{r R_L}{r + R_L} \tag{3.29}$$

This looks the same as the output impedance of the standard buck converter in [1]. However, one should recall that r in Equation 2.35 is quite different.

4 Design of the Full-Bridge DC/DC Converter

The necessary transfer functions have now been derived using averaged modeling and reduction. To validate the small-signal models, design values must be chosen. Some values given are calculated in the section to follow. These are all given in Table 4.1.

Table 4.1: Design values for the full-bridge DC/DC converter.

Description	Variable	Minimum	Nominal	Maximum	Units
DC Input Voltage	V_I	20	24	28	V
DC Output Voltage	V_O	10	12	14	V
Output Current	I_O	0.14	-	1.4	A
Load Resistance	R_L	8.57	-	85.7	Ω
Transformer Turns Ratio	n	-	1	-	-
Switching Frequency	f_s	-	100	-	kHz
Duty Cycle ($D_A + D_B$)	D	45.68	53.29	63.95	%
Inductance	L	225	240	-	μH
Inductor Resistance	r_L	-	42	-	mΩ
Capacitance	C	8.33	10	-	μF
Capacitor ESR	r_C	-	400	-	mΩ
Supply Voltage	V_{CC}	-	15	-	V
FET Gate-Source Voltage	V_{GS}	-	15	-	V
FET Conducting Resistance	r_{DS}	-	77	-	mΩ
PWM Saw-Tooth Voltage	V_{Tm}	0	-	10	V

4.1 Design Process

To validate the small-signal transfer functions for the full-bridge DC/DC converter, it is desirable to compare the calculated frequency responses for each with the simulated frequency response. The calculations will be done using MATLAB [17], and the simulations will be accomplished with Synopsis SABER circuit simulation software [18]. The specifications given in Table 4.1 are adequate to start a design.

4.1.1 Design Equations

First an efficiency of 90% is assumed. This is an educated guess and will be refined when estimated losses are included. The following equations in this section were

utilized or modified from [1] to design the full-bridge DC/DC converter. The duty cycles were calculated as

$$D_{nom} = \frac{2nM_{V_{DC,nom}}}{2\eta}, \tag{4.1}$$

$$D_{min} = \frac{2nM_{V_{DC,min}}}{2\eta}, \tag{4.2}$$

$$D_{max} = \frac{2nM_{V_{DC,max}}}{2\eta}, \tag{4.3}$$

where

$$M_{VDC,nom} = \frac{V_O}{V_{I,nom}}, \tag{4.4}$$

$$M_{VDC,min} = \frac{V_O}{V_{I,max}}, \tag{4.5}$$

$$M_{VDC,min} = \frac{V_O}{V_{I,min}}. \tag{4.6}$$

Next, the load and output current design limitations are found, as

$$R_{L,max} = \frac{V_O}{I_{O,min}}, \tag{4.7}$$

$$I_{O,min} = \frac{V_O}{R_{L,max}}, \tag{4.8}$$

and

$$R_{L,min} = \frac{V_O}{I_{O,max}}. \tag{4.9}$$

At this point, the minimum inductor value to maintain continuous-conduction mode (CCM) operation can be found as

$$L_{min} = \frac{R_{L,max}(1 - D_{min})}{2f_s}. \tag{4.10}$$

The maximum inductor current ripple will be

$$\Delta I_L = \frac{V_O(1 - D_{min})}{f_s L}. \tag{4.11}$$

This means that the CCM/DCM boundary current I_{OB} will be half of ΔI_L, and the boundary resistance will be

$$R_{LB} = \frac{V_O}{I_{OB}}. \tag{4.12}$$

The minimum capacitor value can be found, if an equivalent series resistance is specified, using the equation

$$C_{min} = max\left[\frac{D_{max}}{2f_s r_C}, \frac{1 - D_{min}}{2f_s r_C}\right]. \tag{4.13}$$

To choose an appropriate transformer, one must know the maximum required peak current on the primary side, which is

$$I_{P,max} = \frac{I_{O,max}}{n} + \frac{\Delta I_L}{2n}. \tag{4.14}$$

The peak magnetizing inductance current must be rated approximately $\frac{I_{P,max}}{10}$. It follows that the rated minimum magnetizing inductance must be

$$L_{m,min} = \frac{10 D_{min} V_{I,max}}{f_s I_{P,max}}. \tag{4.15}$$

This project utilizes an ideal transformer in simulations. Nevertheless, the equations are provided, since follow-on designs utilizing soft-switched control will require them. This project has specified an IRF540 MOSFET for the primary-side switching devices and for the self-driven synchronous rectifier switching devices. The r_{DS} is $77m\Omega$ [5]. The primary-side switches may only see a voltage stress equal to the input voltage, but the current rating must be at least

$$I_{SM,max} = \frac{I_{O,max}}{n} + \frac{\Delta I_{Lm,max}}{2} + \frac{\Delta I_{L,max}}{2n}. \tag{4.16}$$

The rectifying switches will require

$$V_{SMsec,max} = \frac{2V_{I,max}}{n}. \tag{4.17}$$

The rectifying switches must also be rated for

$$I_{SMsec,max} = \frac{I_{O,max}}{n} + \frac{\Delta I_{L,max}}{2}. \tag{4.18}$$

4.1.2 Losses

The system losses are able to be calculated, at this point. The following equations in this section were utilized or modified from [1]. The switches have a conduction loss of

$$P_{r_{DS},pri} = \frac{D_{max} r_{DS} I_{O,max}^2}{n^2} \tag{4.19}$$

and a switching loss of

$$P_{sw,pri} = f_s C_{oss} V_{I,min}^2. \tag{4.20}$$

The power loss in one primary-side switch is equal to

$$P_{MOS,pri} = P_{r_{DS},pri} + \frac{P_{sw,pri}}{2}. \tag{4.21}$$

For the synchronous rectifier switch losses, each switch has a conduction loss of

$$P_{r_{DS},sec} = \frac{(2D_{max} + 1) r_{DS} I_{O,max}^2}{4} \tag{4.22}$$

and a switching loss of

$$P_{sw,sec} = \frac{f_s C_{oss} V_{I,min}^2}{4}. \tag{4.23}$$

The power loss in one secondary-side switch is equal to

$$P_{MOS,sec} = P_{rDS,sec} + P_{sw,sec}. \tag{4.24}$$

This design measures current with a 0.1Ω sense resistor, called r_{CS}, which contributes to system losses. This will be included with the inductor loss. The power loss in the inductor switch is equal to

$$P_{r_L} = (r_L + r_{CS}) I_{O,max}^2. \tag{4.25}$$

The capacitor has a loss of

$$P_{r_C} = \frac{r_C \Delta I_{L,max}^2}{12}. \tag{4.26}$$

Neglecting winding resistance loss, the total power loss that this particular design will see is

$$P_{LS} = 4P_{MOS,pri} + 4P_{MOS,sec} + P_{r_C} + P_{r_L}. \tag{4.27}$$

The maximum possible output power is

$$P_{O,max} = V_O I_{O,max}. \tag{4.28}$$

Now, the efficiency may be recalculated as

$$\eta = \frac{P_{O,max}}{P_{O,max} + P_{LS}}. \tag{4.29}$$

The updated efficiency calculation allows a honing of the duty cycle, becoming

$$D_{nom} = \frac{2nM_{VDC,nom}}{2\eta}. \tag{4.30}$$

4.2 Simulation of the Small-Signal Model

The values acquired at this point may now be used to simulate a small-signal circuit, using SABER circuit simulation software [18]. This is for the purpose of validation against the mathematical model calculated in MATLAB [17]. The small-signal model displayed in Figure 2.8 is constructed in Figure 4.1.

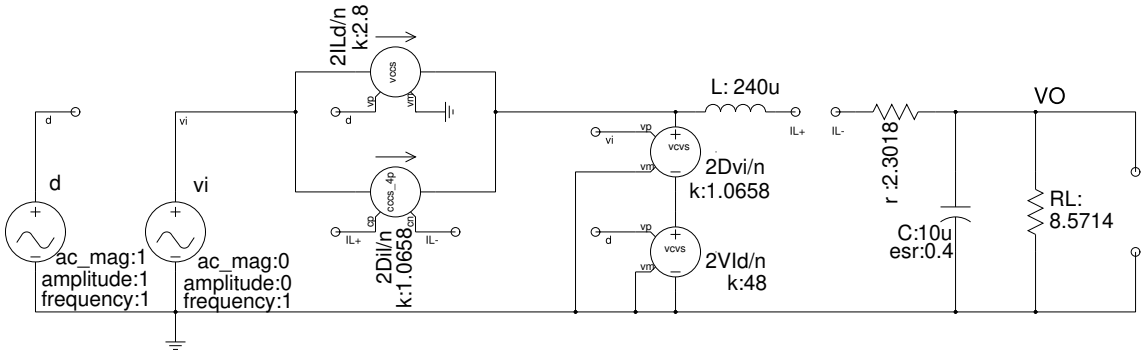

Figure 4.1: Simulated small-signal model for control-to-output analysis.

The model above matches Equation 3.11. The circuit layout is equivalent to that shown in Figure 2.8, but the simulator requires the current sources to connect to the inductor "input" node. The effect of the current sources is the same: the current-splitting theorem was utilized to explicitly show the effect in Figure 2.6. The small-signal duty cycle d is assigned unity amplitude, unity AC magnitude, and unity frequency for model evaluation. The load resistance is set to $R_{L,min}$, as given in Table 4.1, so the current will be set to $I_L = I_{Lmax}$. This is presented in the simulation as $k : 2.8$ for the dependent current source $\frac{2I_L d}{n}$. The small-signal input voltage v_i is given a null amplitude and null AC magnitude to isolate the effects of d on the model output. The duty cycle value D_{nom}, also given in Table 4.1, is used, as well as the turns ratio n, for the upper dependent voltage source $\frac{2Dv_i}{n}$. This value is also used for the dependent current source $\frac{2Di_l}{n}$ and is represented in the simulator as the value $k : 1.0658$. The lower dependent voltage source $\frac{2V_I d}{n}$ is set according to $V_{I,nom}$ and is simply given a value of $k : 48$. The averaged and reduced resistance r contains the resistances defined in Equation 2.35. Note that the derived resistance "$R_{F,ave}$" utilizes the value of r_{DS} for the IRF540 [5] utilized for the self-driven synchronous rectifier, rather than a diode R_F, due to reasons of efficiency, stated earlier.

The circuit from Figure 4.1 was simulated, and the bode plot from this simulation is shown in Figure 4.2. Figure 4.3 is also plotted in Matlab, using Equation 3.11. The results are essentially identical: both have a DC gain T_{p0} of approximately $31.6dB$ and a phase margin of 39.5^o.

The simulated small-signal input-to-output circuit is similar to that shown in Figure 4.1, except the small-signal input voltage v_i is the input, rather than d. The only change then is with the AC magnitude and amplitude; these become unity for v_i and null for d. These results from simulating in SABER in Figure 4.4 and calculated in Matlab, based on Equation 3.21, are shown in Figure 4.5. Again, the results are

very close.

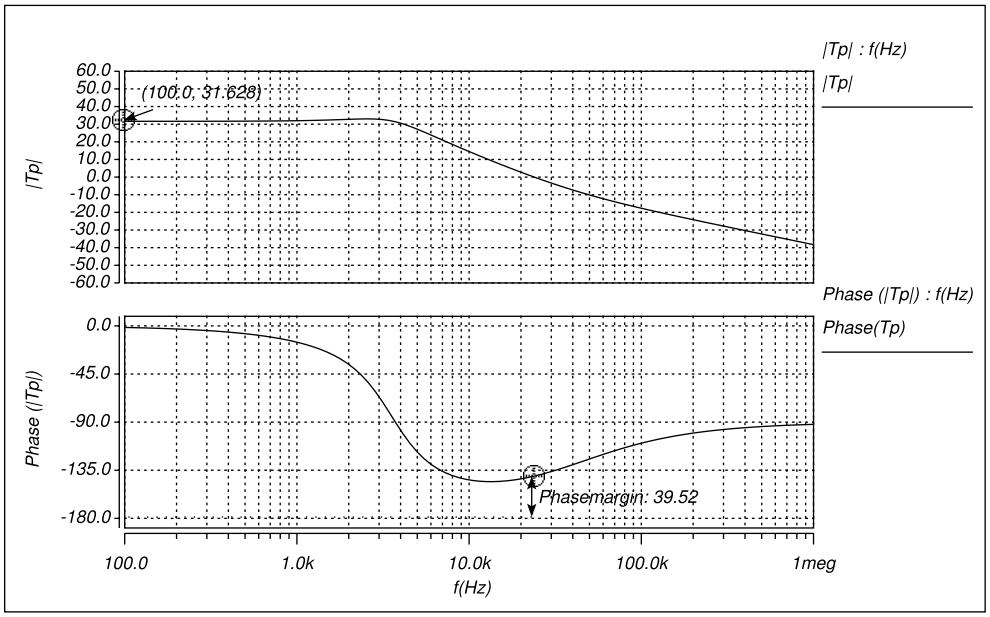

Figure 4.2: Simulated frequency response for control-to-output transfer function.

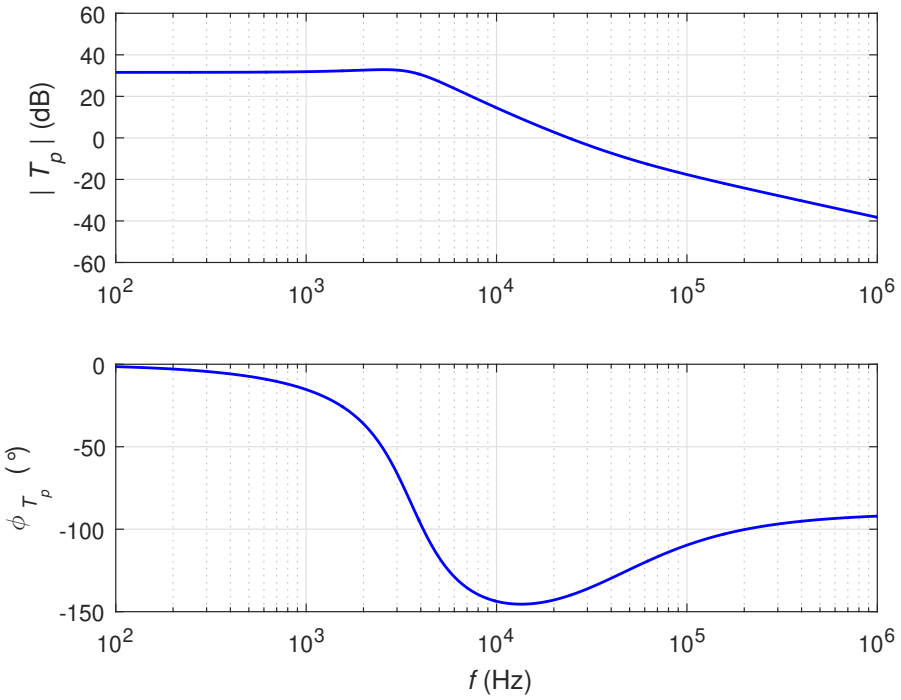

Figure 4.3: Calculated frequency response for control-to-output transfer function.

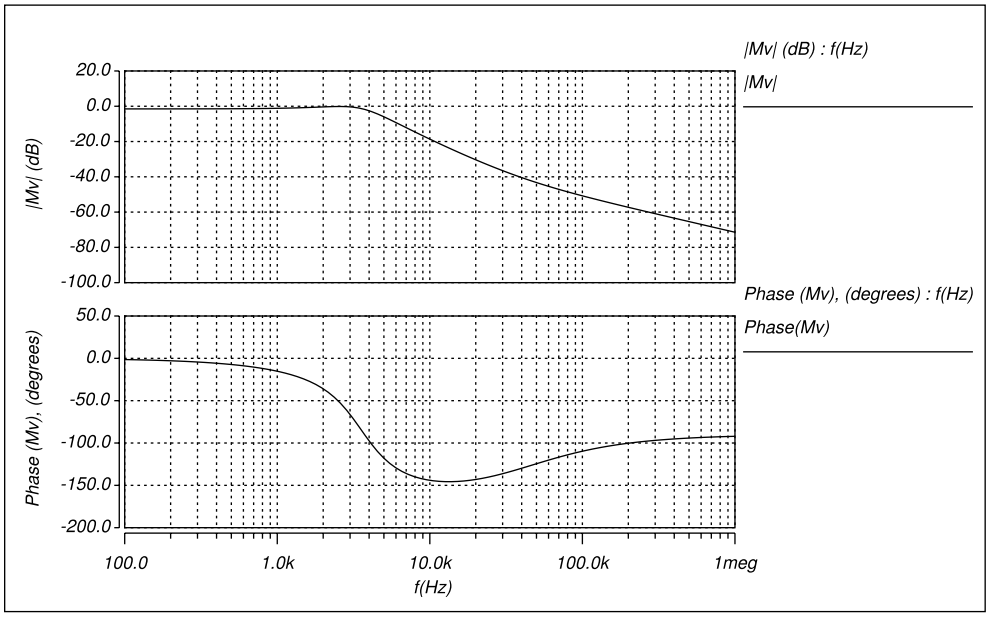

Figure 4.4: Simulated frequency response for input-to-output transfer function.

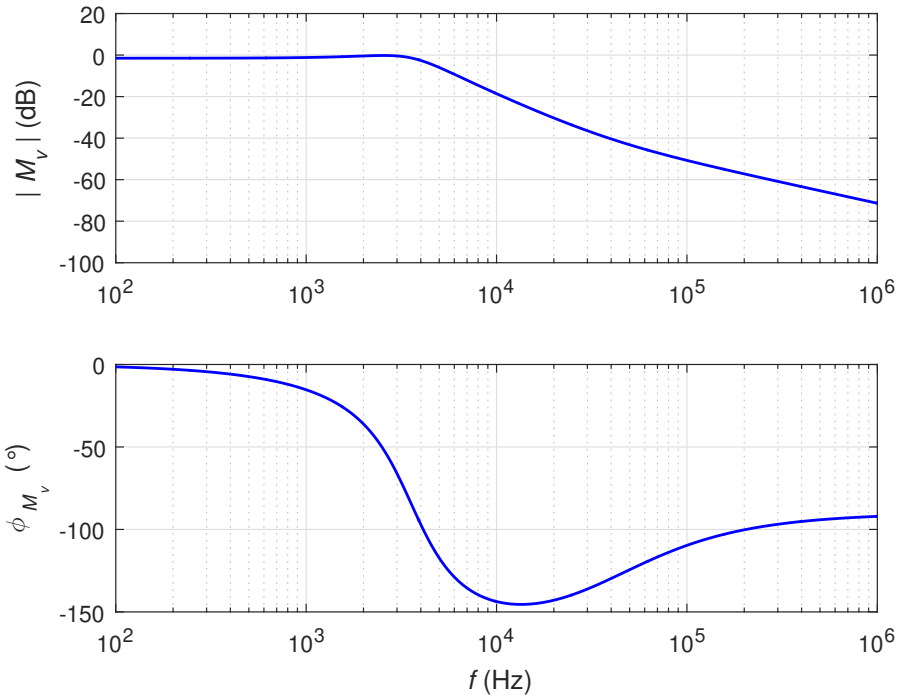

Figure 4.5: Calculated frequency response for input-to-output transfer function.

Measuring the small-signal output impedance response required altering the small-signal circuit for simulation. This is shown in Figure 4.6.

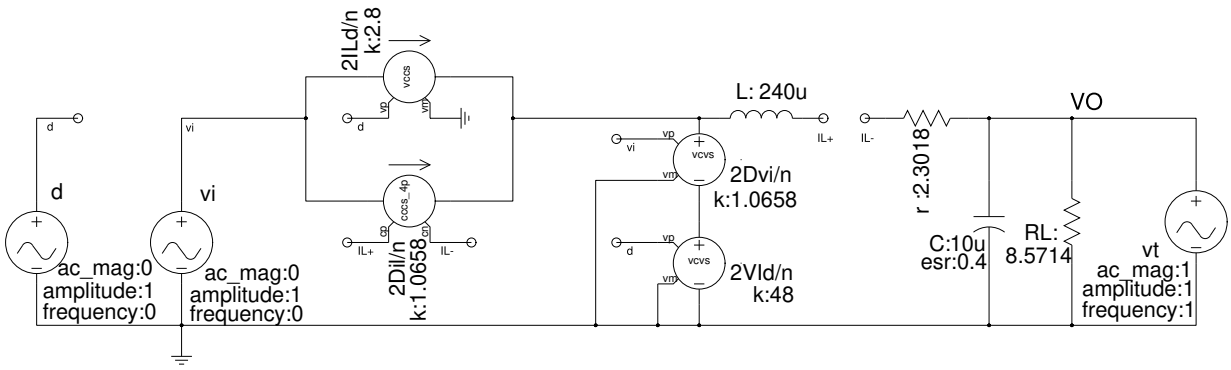

Figure 4.6: Simulated small-signal model for output impedance analysis.

The inputs v_i and d are set to null, while a voltage v_t, with a unity AC magnitude, amplitude, and frequency, is attached to the load. This implements the process described earlier in "Small-Signal Output Impedance Derivation." The test voltage produces a test current i_t, which reveals the isolated output impedance. The response of this simulation is seen in Figure 4.7, while the response of the calculation, based on Equation 3.27, is shown in 4.8. Again, these plots are the same in magnitude and in phase.

4.3 Compensation Characteristics

The agreement of the small-signal simulated and calculated frequency responses for control-to-input, audio susceptibility (input-to-output), and output impedance lead to the next step in the design of a functional full-bridge DC/DC converter. Many PWM converters utilize a comparator to compare the control voltage v_c against a shark-tooth voltage signal at the switching frequency, generating a pulse width to the gate drive. This shark-tooth signal has a maximum voltage V_{Tm}. The transfer function is simply

$$T_m = \frac{1}{V_{Tm}}. \tag{4.31}$$

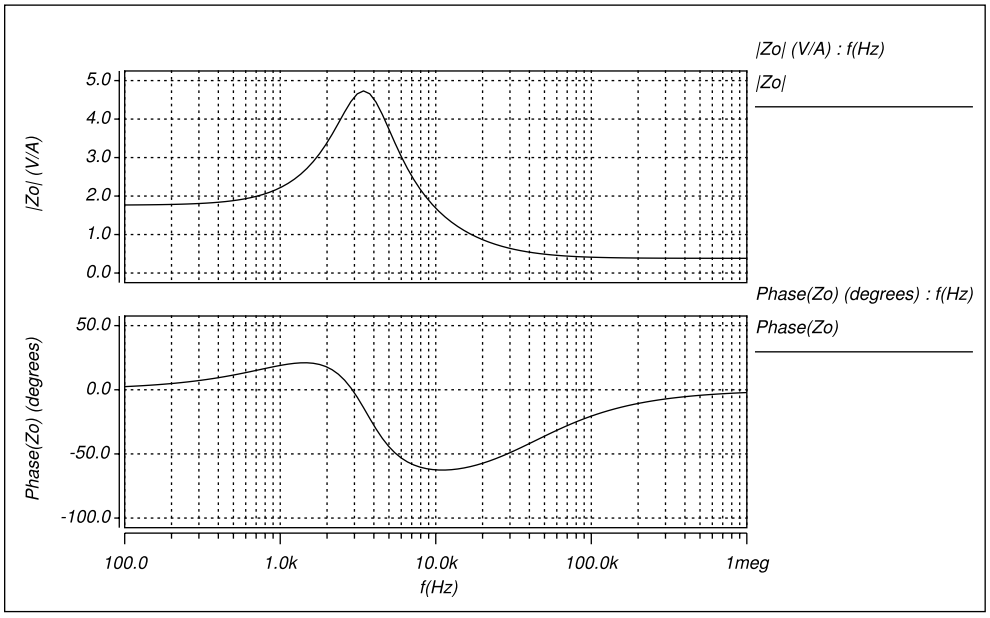

Figure 4.7: Simulated frequency response for output impedance transfer function.

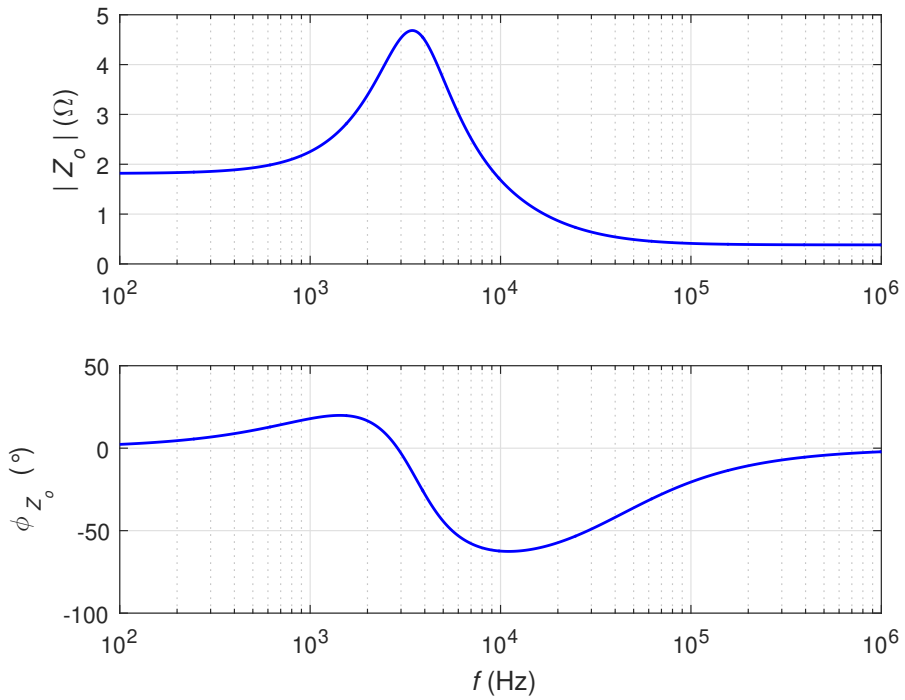

Figure 4.8: Calculated frequency response for output impedance transfer function.

The feedback may now be defined as

$$\beta = \frac{V_R}{V_O} = \frac{DV_{Tm}}{V_O}. \tag{4.32}$$

The transfer function $T_k(s)$ is defined in [1] as

$$T_k(s) = T_p(s)T_m\beta. \tag{4.33}$$

This function represents the uncompensated system response which must be compensated to a degree to achieve the desired margin of stability. Explicitly, Equation 3.17 influences T_k, such that

$$\begin{aligned} T_{kx} &= \left(\frac{2V_I}{n}\right)\left(\frac{R_L r_C}{LR_L + Lr_C}\right)\left(\frac{1}{V_{Tm}}\right)\left(\frac{DV_{Tm}}{V_O}\right) \\ &= \left(\frac{2V_I D}{nV_O}\right)\left(\frac{R_L r_C}{LR_L + Lr_C}\right). \end{aligned} \tag{4.34}$$

From Equation 3.18 and Equation 4.34, the DC gain of the uncompensated system is

$$T_{k0} = \left(\frac{2V_I D}{nV_O}\right)\left(\frac{R_L}{R_L + r}\right). \tag{4.35}$$

Finally, from Equation 3.11 and Equation 3.17, the transfer function of the uncompensated system is

$$T_k(s) = \left(\frac{2V_I D}{nV_O}\right)\left(\frac{R_L r_C}{LR_L + Lr_C}\right)\frac{s + \frac{1}{Cr_C}}{s^2 + \left[\frac{L+C(R_L r + r_C r + R_L r_C}{LC(R_L + r_C)s}\right] + \left[\frac{r+R_L}{LC(R_L+r_C}\right]}. \tag{4.36}$$

The phase of the uncompensated system is given in [1]. This is

$$\phi_{T_k} = -180 + tan^{-1}\left(\frac{f_c}{2\pi C r_C}\right) + tan^{-1}\left[\frac{2\xi\left(\frac{f}{f_o}\right)}{1 - \left(\frac{f}{f_o}\right)}\right]. \tag{4.37}$$

Per Table 4.1, the switching frequency f_s is $100kHz$. According to Nyquist's Theorem [1], the controller frequency f_c must be less than or equal to half the switching frequency. Let the controller frequency be

$$f_c = 40kHz \leq \frac{f_s}{2}. \tag{4.38}$$

Evaluating the response of the uncompensated transfer function T_k is now possible. The calculated bode plot is given in Figure 4.9.

The controller must correct for the response

$$T_k(f_c) = T_{k0}\sqrt{\frac{1 + \left(\frac{f_c}{2\pi C r_C}\right)^2}{\left(1 - \left(\frac{f_c}{f_0}\right)^2\right)^2 + 4\xi^2\left(\frac{f_c}{f_0}\right)^2}}. \tag{4.39}$$

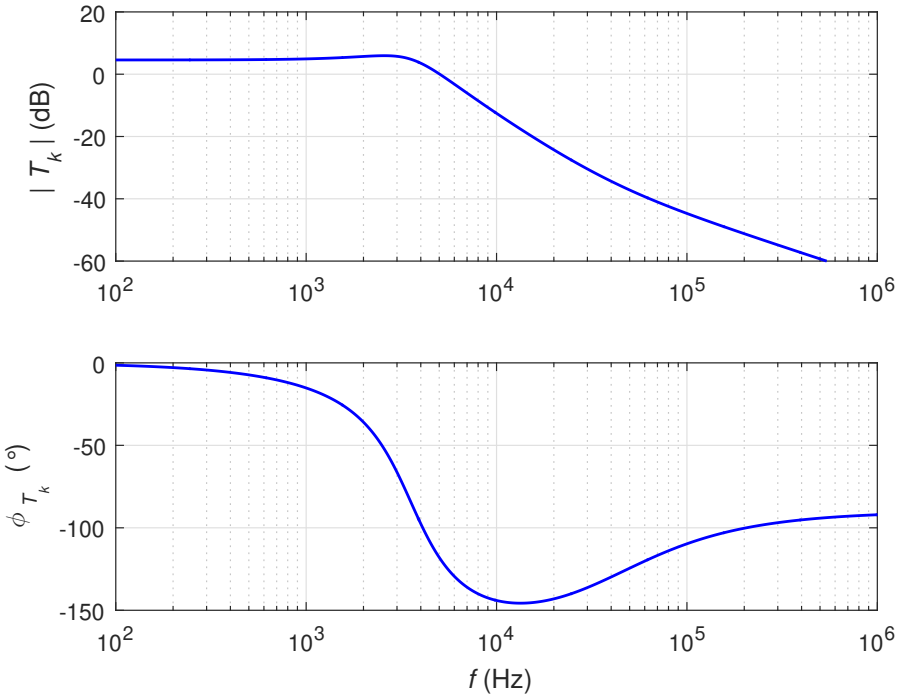

Figure 4.9: Calculated frequency response for the uncompensated system transfer function.

4.4 Voltage-Mode Controller Design

It is desirable to control the converter with higher bandwidth, like a proportional controller provides, while increasing the DC gain, like an integral converter achieves. A proportional-integral converter combines these two controllers, but is not the best solution for rapid, stable control response with high DC gain and low error [1]. In an effort to increase the bandwidth of the control subsystem and to maintain high DC gain, a Type II controller, also known as a Single-Lead Integral Controller, is designed [1], as shown in Figure 4.10. The output of the controller is V_C' and is sufficient to supply the modulator with a signal. In this implementation, this control voltage is gated through a current-limiting override, which will be discussed later.

As with many feedback control systems, this controller connects to the output voltage v_O through a β-network. This network essentially forms a voltage divider

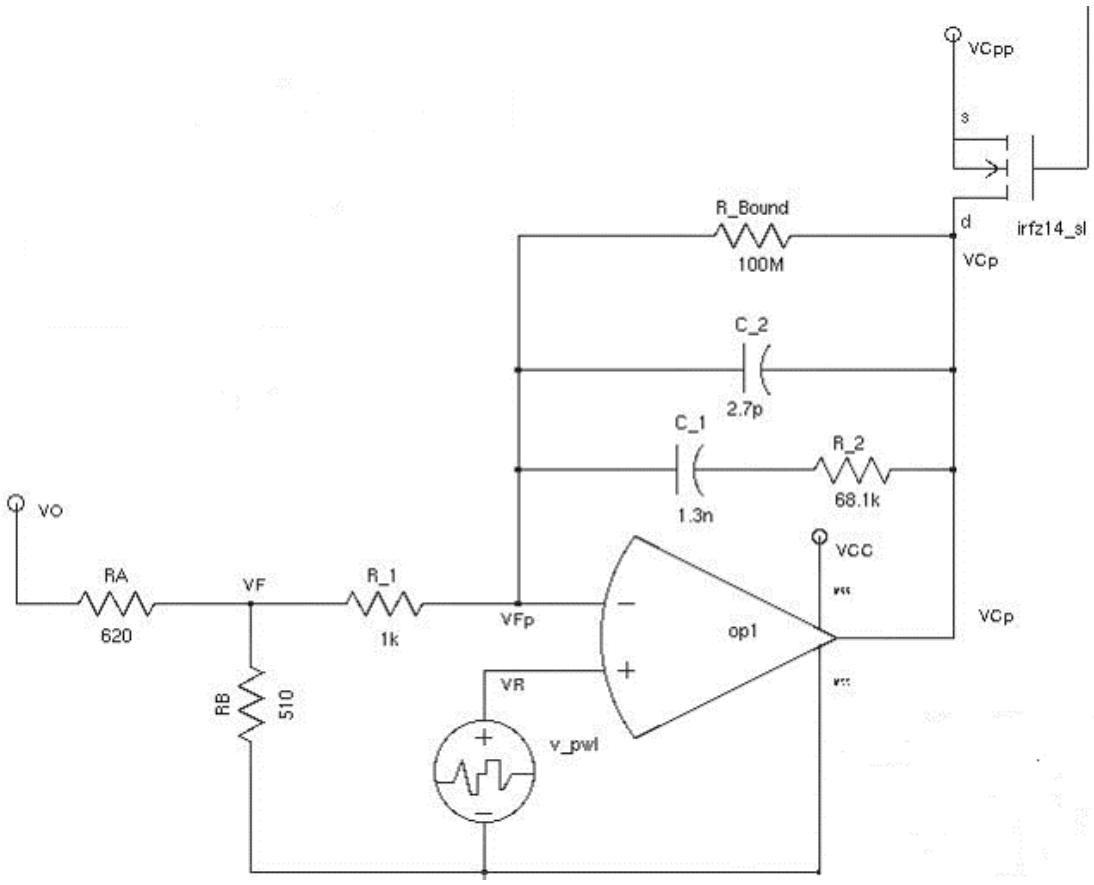

Figure 4.10: Type II voltage-mode controller.

through resistor R_A, referenced through resistor R_B. The feedback ratio β is calculated as 0.44, using Equation 4.32 and Table 4.1. One of the resistors may be chosen, while the other must be calculated. In this case, let

$$R_B = 510\Omega. \tag{4.40}$$

The resistor R_A is then solved as

$$R_A = \frac{R_B}{\beta} - R_B = 638.47\Omega. \tag{4.41}$$

Using standard resistor values, choose $R_A = 620\Omega$. The β-network may also be evaluated using h-parameters, as described in [4] and [1]. Of interest,

$$h_{11} = \frac{R_A R_B}{R_A + R_B}. \tag{4.42}$$

The controller is designed to compensate for T_k with a large "phase boost," as detailed in the following equations from [1]. This adds sizable crossover gain and a design phase margin $P.M.$ to increase system responsiveness. Let phase margin be 45^o. The phase boost is

$$\phi_m = P.M. - 90^o - \phi_{T_k}(f_c) = -45 - \phi_{T_k}(f_c). \tag{4.43}$$

The maximum phase boost ratio may be defined as

$$K = \sqrt{\frac{\omega_{pc}}{\omega_{zc}}} = tan\left(\frac{\phi_m}{2}\right) + P.M. = \sqrt{1 + \frac{C_1}{C_2}}. \tag{4.44}$$

The integral portion of the Type II controller places a pole at the origin, through C_2, defined by

$$B = \omega_c K |T_c(f_c)| = \frac{1}{C_2(R_1 + h_{11})}. \tag{4.45}$$

The other RC pair forms a zero of frequency

$$f_{zc} = \frac{1}{2\pi R_2 C_1}. \tag{4.46}$$

Equation 4.45 can be rearranged to solve for the value of C_2, as

$$C_2 = \frac{|T_k(f_c)|}{2\pi f_c K(R_1 + h_{11}}. \tag{4.47}$$

From Equation 4.44, C_1 can now be found as

$$C_1 = C_2(K^2 - 1). \tag{4.48}$$

Rearranging Equation 4.46 produces a value for R_2, such that

$$R_2 = \frac{K}{2\pi f_c C_1}. \tag{4.49}$$

To contain the DC gain of the operational amplifier, a bounding resistor is sometimes placed in parallel with other controller components. This can be determined with the amplifier equation applied at DC,

$$R_{bound} = T_{c0}(R_1 + h_{11}), \tag{4.50}$$

where the specified bandwidth of the operational amplifier is T_{c0}.

The equations above from [1] were used with values specified in Table 4.1 and Figure 4.10. The response of the controller is shown in Figure 4.11. Of note are the large phase margin over a wide frequency range, as well as the crossover frequency of the controller at approximately 45MHz.

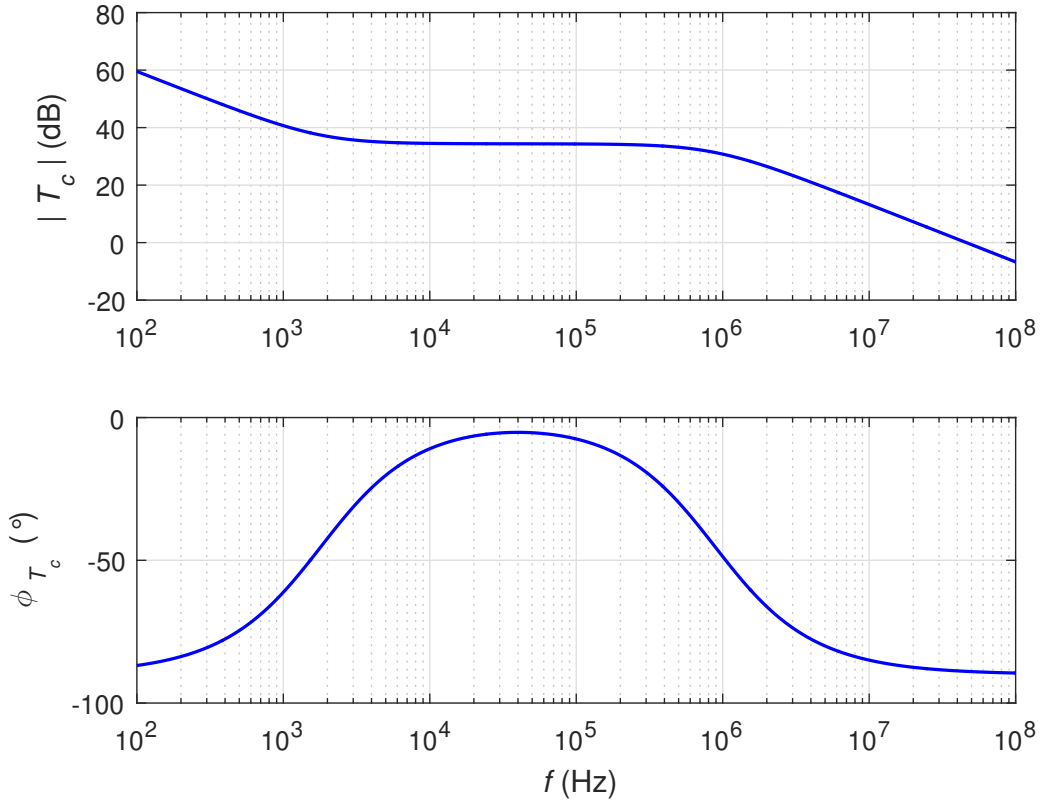

Figure 4.11: Calculated frequency response for the Type II controller transfer function.

4.5 Current Limit

A central purpose of this thesis project remains the ability to isolate a faulted load from the source. This design limits the amount of let-through energy to a low-impedance load, which may include faults. The strategy employed is to actively limit the maximum allowable load current by interrupting the control voltage produced by

the voltage-mode controller from the gate drives. This must occur very quickly, allowing an external system-level controller enough time to execute a follow-on decision. The implemented active current-limiting circuit is given in Figure 4.12.

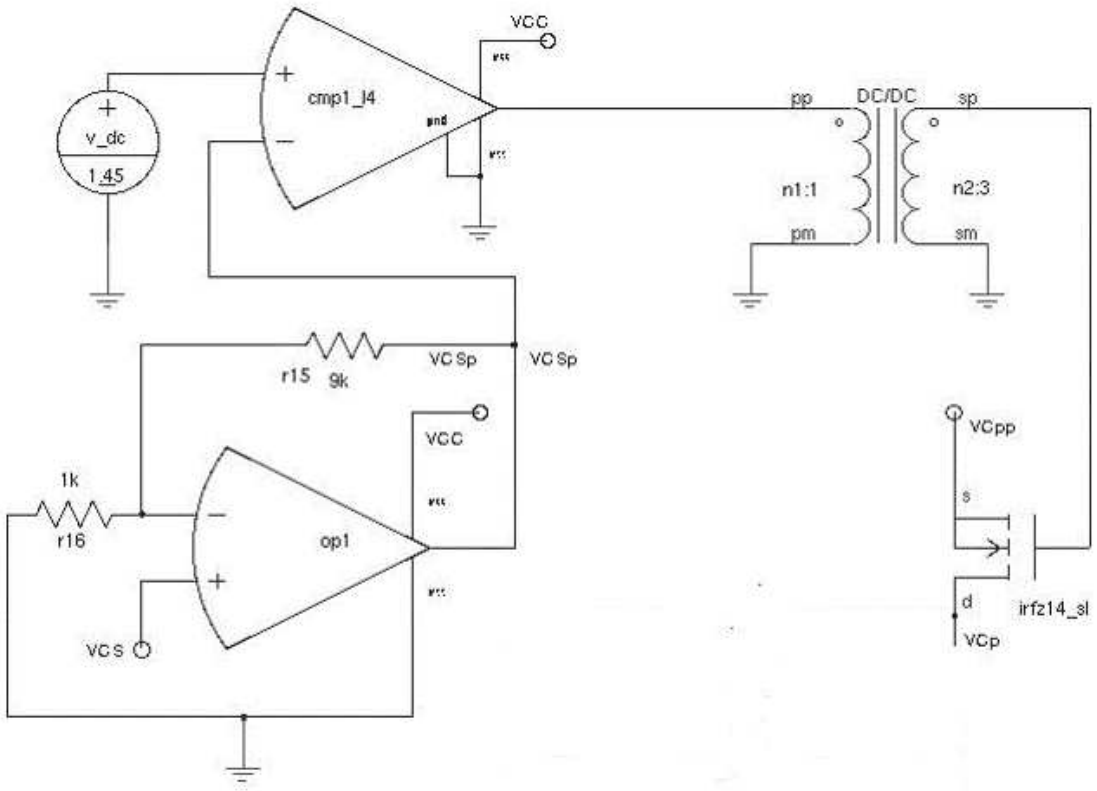

Figure 4.12: Active current-limiting circuit.

The current limit is a comparator which relies on a steady voltage reference and a control voltage representing the inductor current reading. To limit the effect on the output current, a 0.1Ω resistor is utilized to sense inductor current, which happens to be the same as the load current, for this and similar topologies. This current-sensed voltage, V_{CS}, is fed to a non-inverting amplifier [4] of gain $A_v = 10\frac{V}{V}$, to boost the output voltage to V'_{CS}, realizing a 1V/A representation. The reference voltage programs the maximum allowable current, allowing for a small current ripple. Since Table 4.1 lists the maximum design output current as $1.4A$, the current limit is set to $1.45A$. For a current below the limit, the comparator produces a $5V$ output. When

the input voltage V'_{CS} exceeds the current limit, the comparator output drops to zero.

Since it was not readily evident how to easily provide an option to change the comparator output voltage within the SABER circuit simulation software, an ideal transformer with turns ratio $n = 3$ is employed to boost the output voltage back to V_{CC}. As a side note, this method is employed through the simulated circuit wherever a comparator is used. This method would *not* be utilized in a hardware implementation.

The $15V$ output from the current-limiting circuit drives the gate of an IRFZ14 MOSFET [6]. Since the control voltage V_C should remain near the controller reference of approximately $2.6V$, a $15V$ input from the current limiting circuit will provide $V_{GS} = 12.4V$, easily operating the MOSFET as a switch [6]. A zero voltage gate input from the current-limiting circuit will cause a momentary negative voltage on V_{GS}, ensuring that the switch turns off, until the current-limiting comparator is again satisfied.

5 Implementation and Results of Full-Bridge DC/DC Converter in Simulation

5.1 Closed-Loop Response

When the loop is closed by the gate drives, the controller adjusts the uncompensated system response, giving it a design phase margin of 45^o. This closed-loop system frequency response is shown in Figure 5.1. The crossover frequency is indeed at $f_c = 40kHz$, and the phase margin is at 45^o. In fact, the phase margin does not drop below 25^o, out to 1MHz.

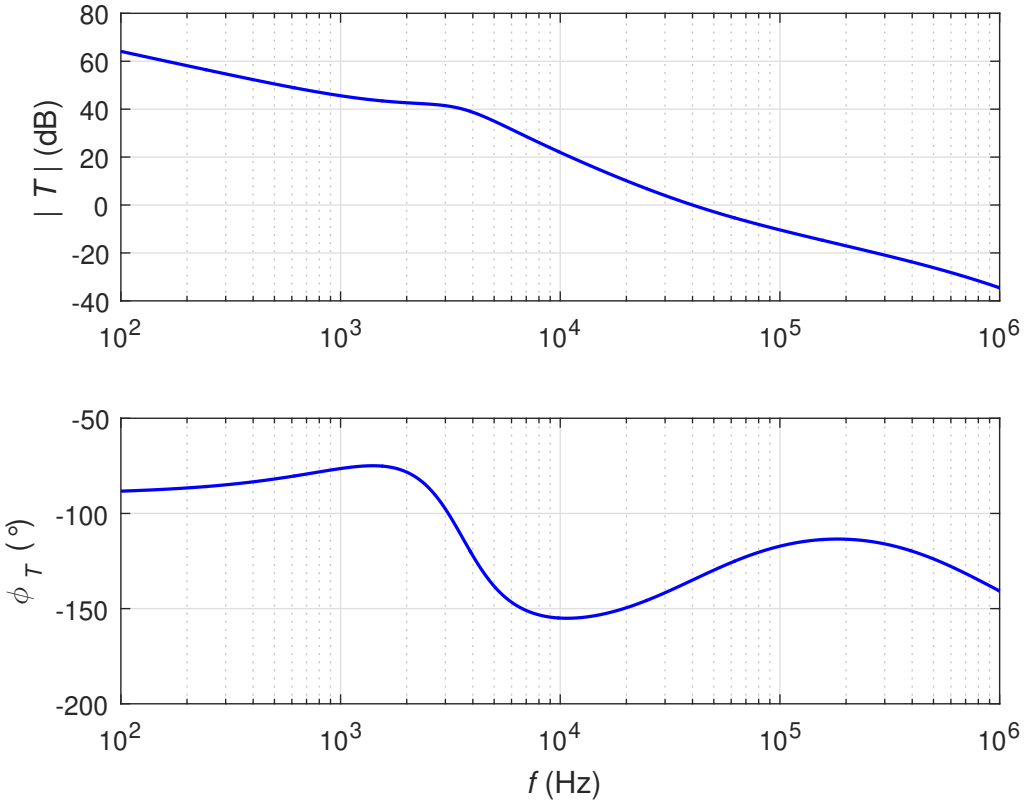

Figure 5.1: Calculated closed-loop system frequency response.

Now that the loop is closed, the small-signal equations may be re-evaluated. The

control-to-output closed-loop transfer function, as described in [1], is

$$T_{pcl} = \frac{T_p T_m T_c}{1 + T}. \tag{5.1}$$

The response of T_{pcl} is given in Figure 5.2. It appears that the closed-loop control increases the bandwidth of the power stage with duty cycle d, but loses some low-frequency gain compared to the open loop response T_p. Phase margin has also increased for T_{pcl}.

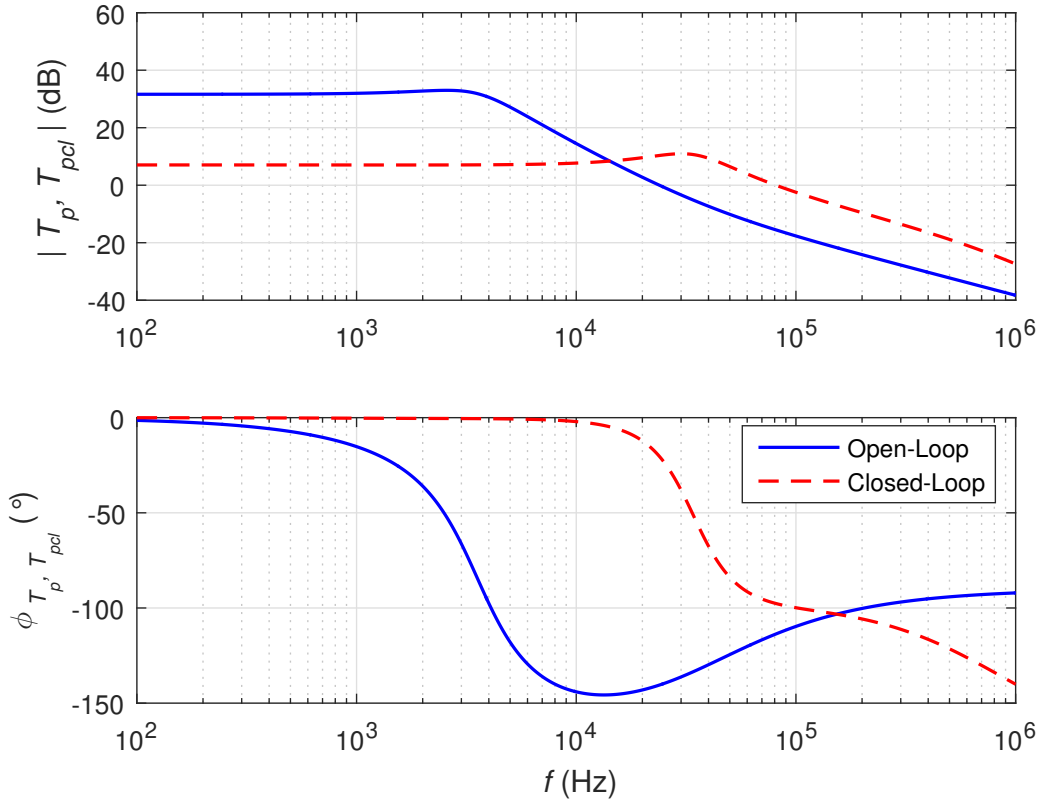

Figure 5.2: Calculated closed-loop control-to-output frequency response, versus open-loop control-to-output frequency response.

The input-to-output closed-loop transfer function, as described in [1], is

$$M_{vcl} = \frac{Mv}{1 + T}. \tag{5.2}$$

The response of M_{vcl} is given in Figure 5.3. The closed-loop control decreases the influence of an input voltage change affecting the output voltage regulation.

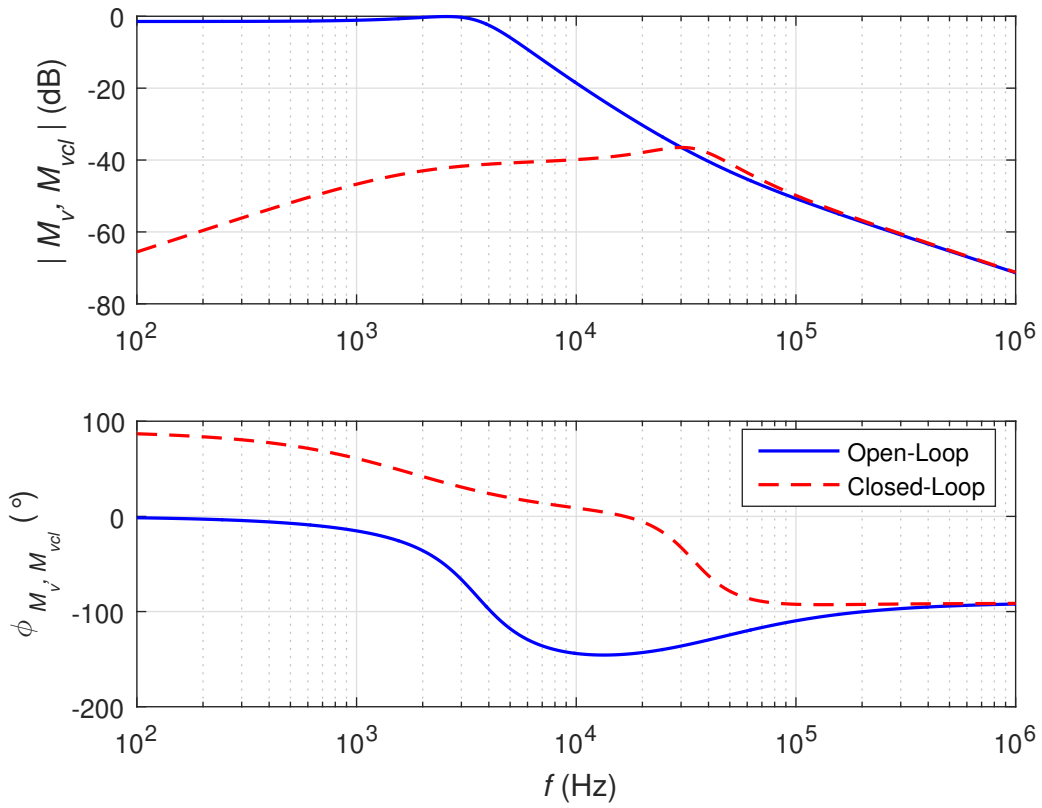

Figure 5.3: Calculated closed-loop input-to-output frequency response, versus open-loop input-to-output frequency response.

The output impedance closed-loop transfer function, as described in [1], is

$$Z_{ocl} = \frac{Zo}{1+T}. \tag{5.3}$$

The response of Z_{ocl} is given in Figure 5.4. The closed-loop control minimizes inductive loading and only has slight capacitive loading near and above the controller frequency $f_c = 40kHz$.

5.2 Full-Bridge DC/DC Converter Implementation

The complete circuit, including the power stage; voltage-mode controller; current limiter; gate drives; and self-driven synchronous rectifier is shown in Figure 5.5. The gate drives and rectifier will be discussed subsequently. Passive component values

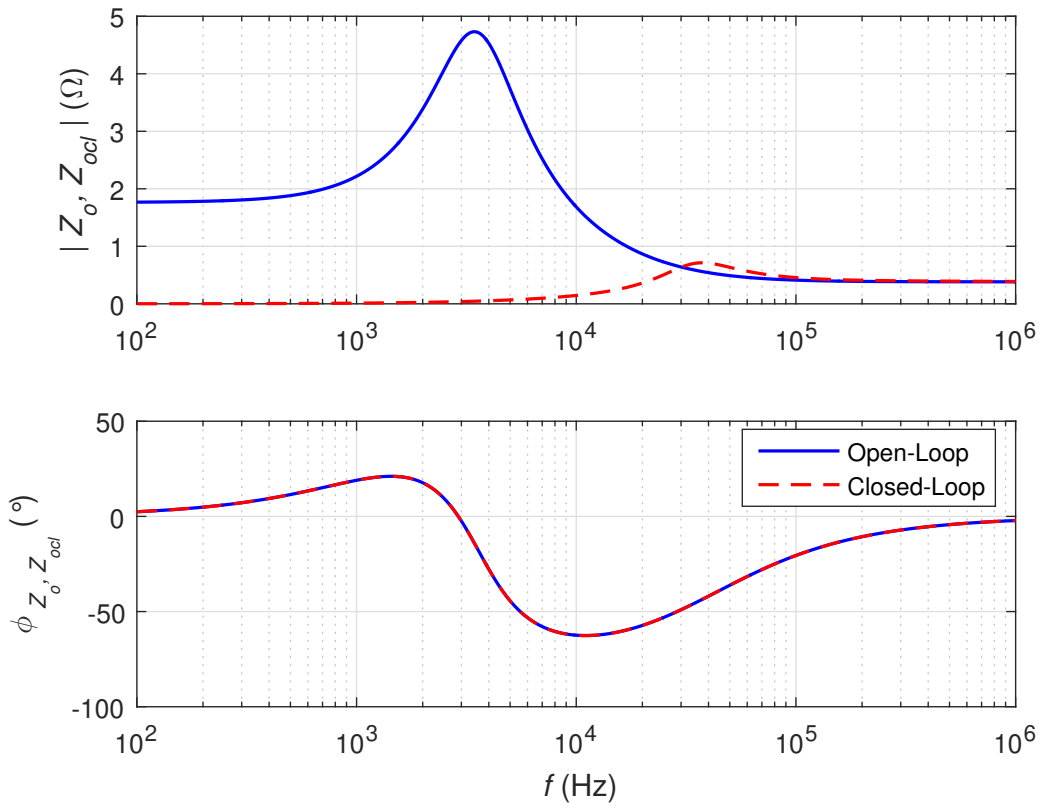

Figure 5.4: Calculated closed-loop output impedance frequency response, versus open-loop output impedance frequency response.

were selected from commonly available values nearest to the calculated value. In particular, resistors were chosen from available values of 1% tolerance.

There is a limitation related to the full circuit simulations. Due to the volume of calculations, the simulator tends to create output files larger than available server storage. Therefore, limitations of approximately $2ms$ per simulation are imposed. This makes it difficult to allow for full settling of the output, especially for the unit-step simulations.

5.2.1 Gate Drives

The gate drives are in the upper right portion of the circuit in Figure 5.5. As previously mentioned, the current-limited controller output signal V_C'' is compared against

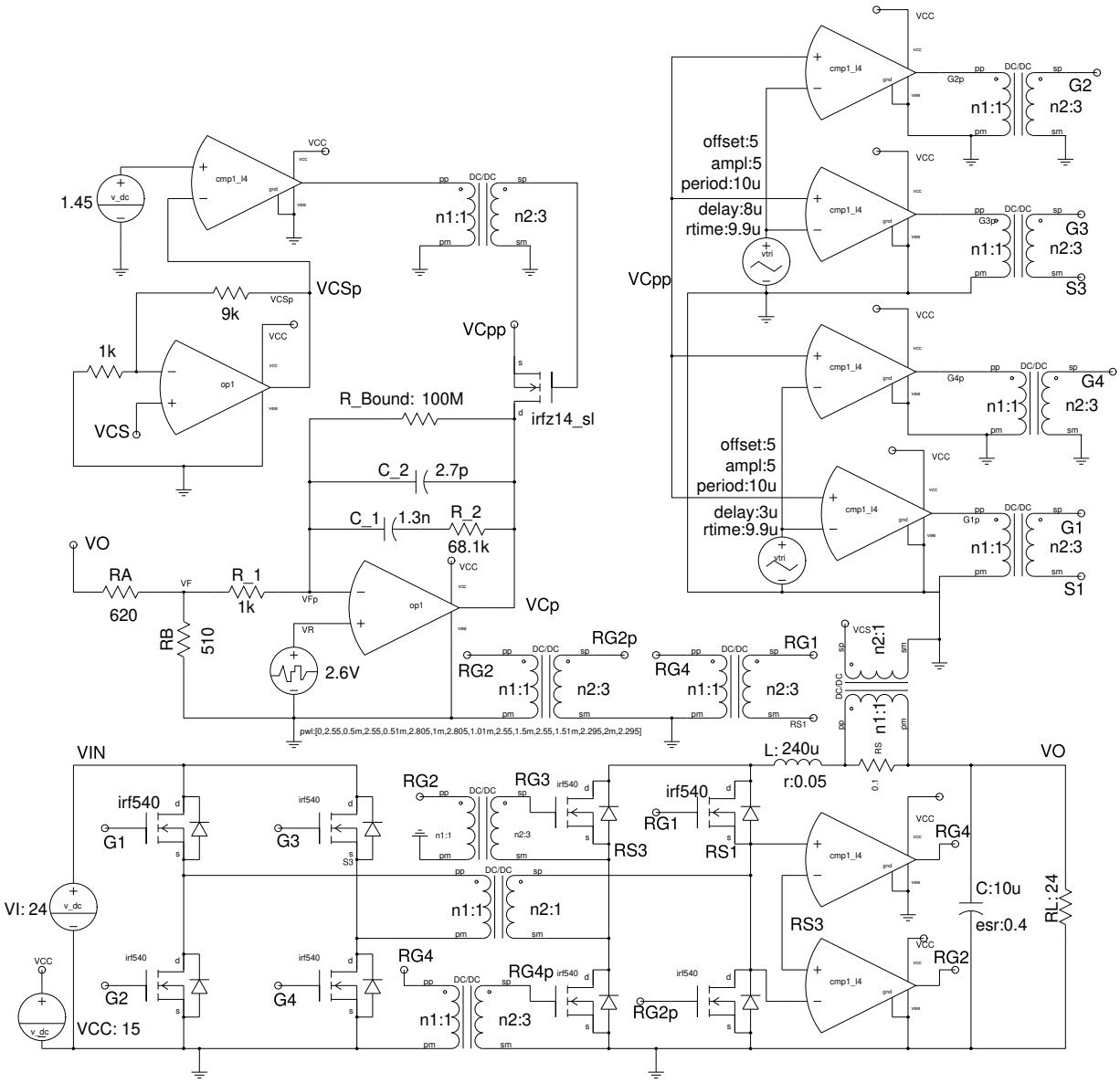

Figure 5.5: Simulated full-bridge DC/DC converter design [18]

the sawtooth signal $V_{Tm} = 10V$ at $f_s = 100kHz$, equivalent to a period of $10\mu s$.

For reference, the voltage is programmed in SABER circuit simulator as having an offset of $5V$ and a peak amplitude of 5V. The simulator malfunctions if the rise time is equal to the period, so the rise time was set to $9.9\mu s$. This does not appear to affect the gate drive function.

There are four comparators, although technically the hard-switched converter

only requires two comparators, with an isolated source reference for each switch. The "lower" switches are ground-referenced, but the upper switches must be source-referenced, to provide the proper differential drive voltage for V_{GS}.

Per Figure 2.2 and Equation 2.2, the switch pairs S_A (including switches S_1 and S_4) and S_B (including switches S_2 and S_3), must be separated by half the period, or $5\mu s$. Due to simulation anomalies related to current-limiting during a high gate drive output, the delays were shifted by an additional $3\mu s$. This results in intended operation.

For soft switching, the gate drives within S_A, for instance, will have additional latency between S_1 and S_4, equivalent to the time constant created by the interaction between the switch output capacitance and the transformer leakage inductance [9].

5.2.2 Self-Driven Synchronous Rectifier

Since the design output voltage is 12V at relatively lower power output, the diode losses derived earlier, due to voltage loss, are too high. To reduce losses without adding much control complexity to this project, self-driven synchronous rectification is utilized, as defined in [8]. The switching is directly regulated by the polarity of the transformer secondary terminals. When the polarity is positive, the rectifier duty cycle D_{RA} is driven high. Conversely, when the polarity is negative, the duty cycle D_{RB} is driven high. When the secondary voltage collapses, the body diodes of the MOSFETs conduct, maintaining continuous conduction of the inductor L. By association then, the self-driven synchronous control is partially driven indirectly by the primary-side gate drives. However, no additional signal is required from the primary-side gate drives for this synchronous rectifier to function the same as a diode rectifier [8].

The anti-parallel diodes included with all switches are ideal diodes. The power MOSFETs chosen are IRF540, since the losses must be realistic enough to converge

on a somewhat accurate efficiency to estimate a proper duty cycle. Since simplifying design assumptions were made to utilize an ideal transformer and hard-switching operation, the ideal diodes are meant to suppress ringing. A more mature design might incorporate either ZVS-driven [11] or non-ZVS-driven dead-time, along with a fast-recovery anti-parallel diode, such as a Schottky diode or a SiC diode.

5.3 Dynamic Response of the Closed-Loop Output Voltage

The dynamic response of the output voltage provides another measure of controller adequacy. Each output of the small-signal transfer functions were given an input step function to determine the predicted steady-state response of the output, both without the closed loop and with the closed loop. Unit-step response here refers to 10% step in duty cycle for T_p and T_{pcl}; a $1V$ step of input voltage for M_v and M_{vcl}; and a step in load current of $1A$ for Z_o and Z_{ocl}.

Open-loop and closed-loop audio susceptibility are calculated and compared in Figure 5.6. The open-loop unit-step response causes a calculated steady-state output of approximately $12.85V$, while the closed-loop output is relatively unchanged, as designed.

The closed-loop audio susceptibility is then tested with a positive and negative step function on the input within the complete full-bridge converter circuit from Figure 5.5. These results are then seen in Figure 5.7. Here, the closed-loop output is estimated to have a shift by $0.5V$ with a unity change of input. These discrepancies may be due to the aforementioned implementation of the IRF540 model with an ideal transformer and ideal diodes.

Open-loop and closed-loop output impedance are calculated and compared in Figure 5.8. The open-loop unit-step response causes a calculated steady-state output of approximately $13.75V$, while the steady-state closed-loop output also remains relatively unchanged, as designed.

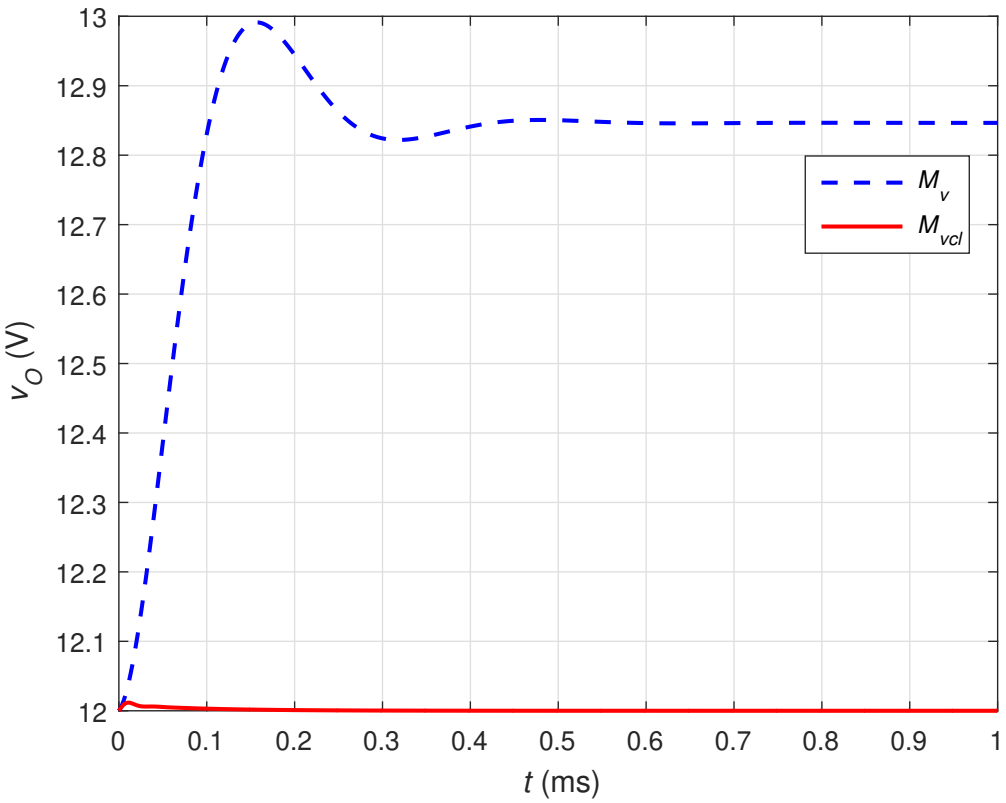

Figure 5.6: Calculated closed-loop input-to-output step response, versus open-loop input-to-output step response.

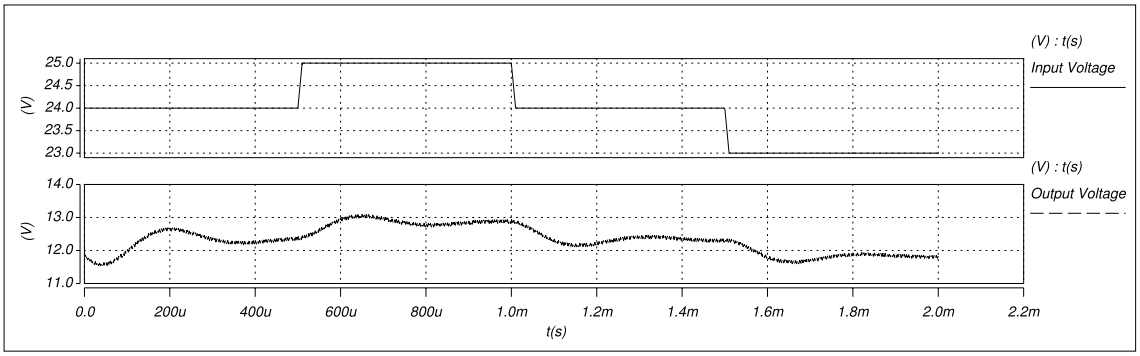

Figure 5.7: Simulated closed-loop audio susceptibility step response.

The closed-loop output impedance is then tested with a negative step function on the input within the complete converter circuit from Figure 5.5. This was done by initializing the converter with a $0.4A$ load, then raising the load to $1.4A$, by adjusting the corresponding load resistance. These results are then seen in Figure 5.9. The

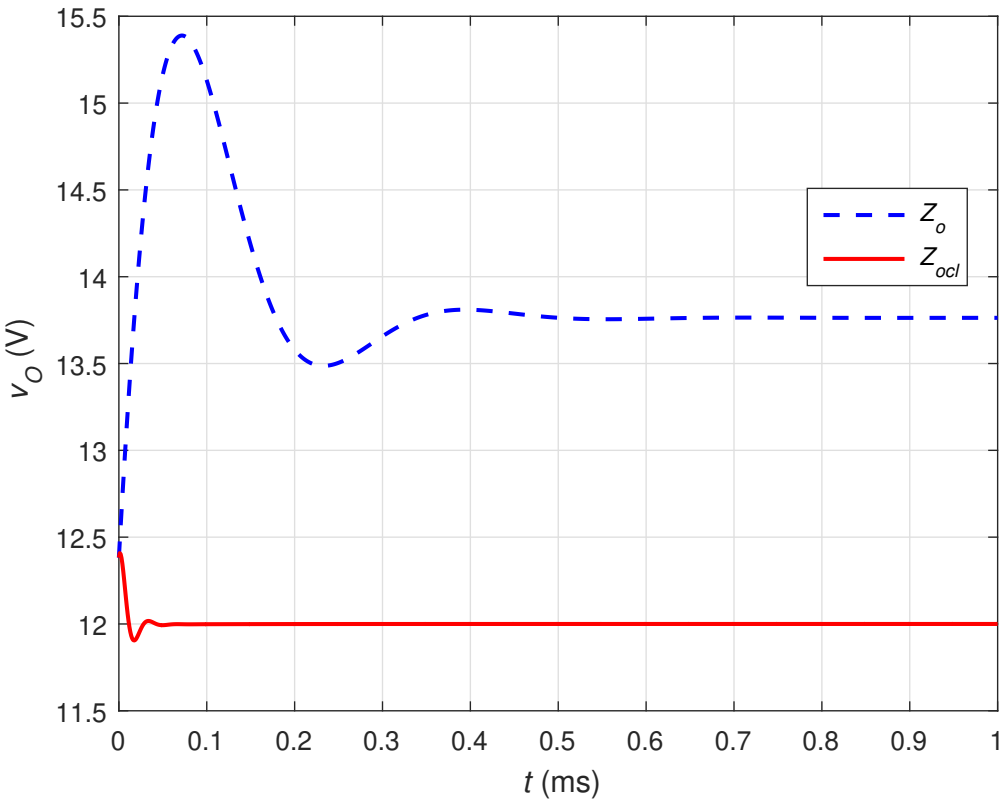

Figure 5.8: Calculated closed-loop output impedance step response, versus open-loop output impedance step response.

closed-loop output is estimated to shift by $0.3V$ with unity change of load current.

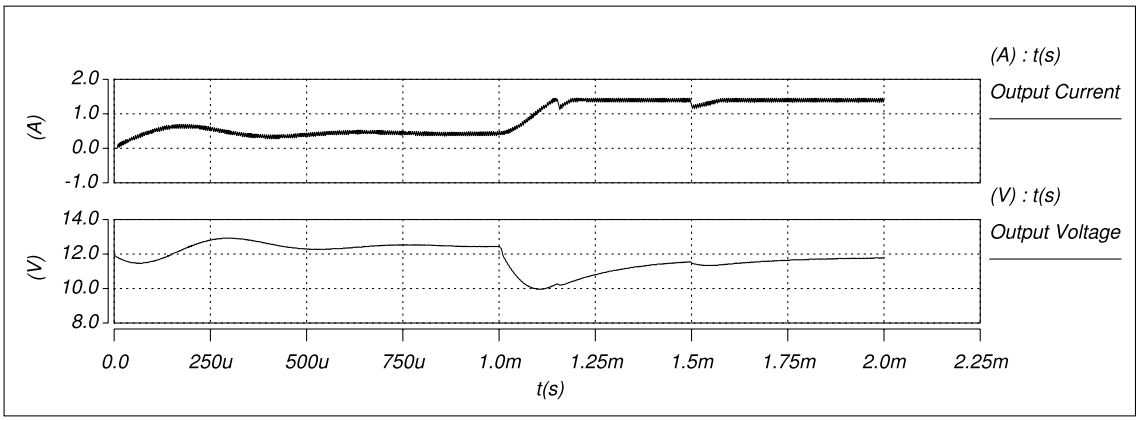

Figure 5.9: Simulated closed-loop output impedance step response.

Open-loop and closed-loop control-to-output are calculated and compared in Fig-

ure 5.10. The unit step is a 10% change in reference voltage.

The open-loop unit-step response causes a calculated steady-state output of approximately $16.8V$, while the steady-state closed-loop output also remains relatively unchanged, as designed. This should indicate the worst step response.

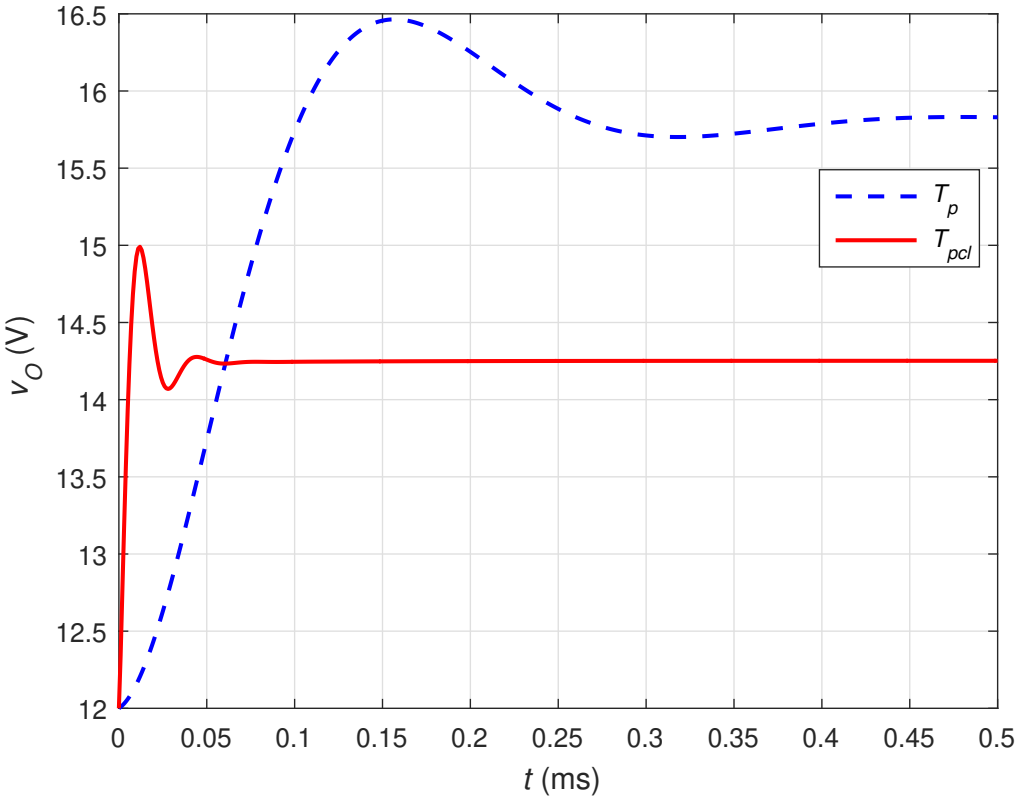

Figure 5.10: Calculated closed-loop control-to-output step response, versus open-loop control-to-output step response.

The closed-loop input-to-output is tested and found to have approximately $1.6V$ change in output voltage for unity change on the input, as seen in Figure 5.11. This result underscores the importance of a stable DC reference voltage.

5.4 Current Limit Results

The current-limiting circuit is tested. When the load reaches the design maximum of $1.45A$, the duty cycle is interrupted to maintain a current limit of $1.45A$ or less.

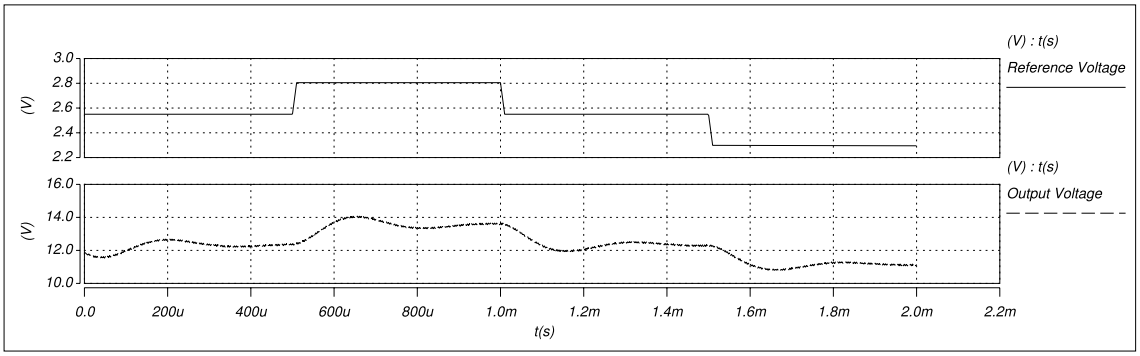

Figure 5.11: Simulated closed-loop control-to-output step response.

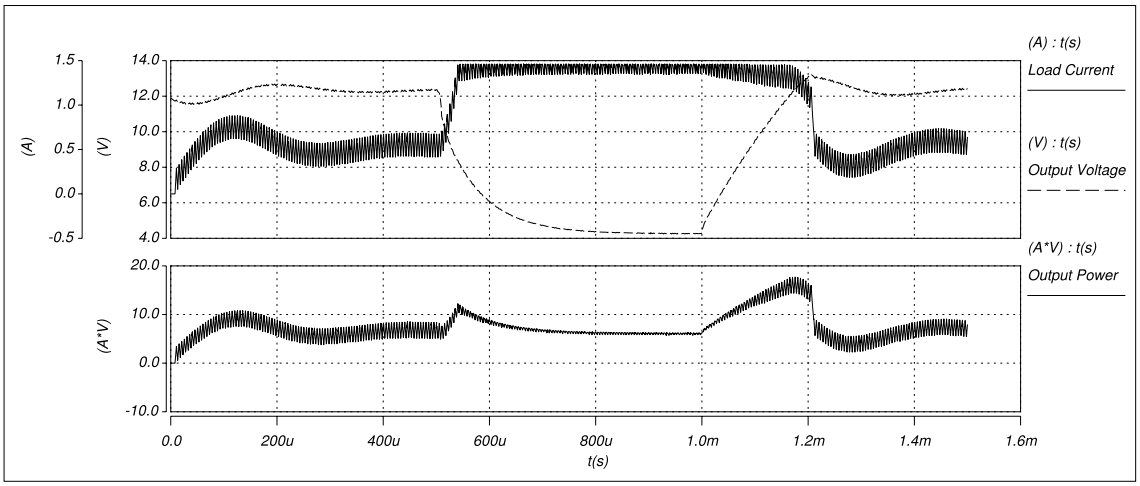

Figure 5.12: Simulated current limit results for an over-current condition in the full-bridge DC/DC converter.

When the control voltage duty cycle drive is interrupted, the output voltage must fall, limiting the power dissipated into a potentially faulted condition. The let-through energy through the over-current condition will be

$$U_{OL}(t) = \int_{t_{OL_{start}}}^{t_{OL_{end}}} VIdt, \tag{5.4}$$

which is limited in this design by minimizing the output voltage, while protecting the switches and conductors from over-current. This effectively limits the worst-case instantaneous output power to simply

$$P_{OL,max} = V_{O,max}\left(I_{L,max} + \frac{\Delta I_L}{2}\right), \tag{5.5}$$

where $I_{L,max}$ is set by the current limiter's reference voltage V_{CLref}. However, care must be taken to ensure that inductive flyback current can freewheel through the secondary-side portion of the converter, to suppress the output voltage V_O, in case of a rapid current limit which results in commanded high-rate voltage change. Through this event, the input voltage is not affected, due to the main power transformer isolation. The maximum output power will occur just after the sum of the output current and its ripple, representing peak inductor current, falls below the limit reference voltage threshold V_{CLref}. This allows the voltage-mode controller to increase the output voltage with near maximum output current.

When coupled with an average current-mode controller, the current-limiting circuit can increase bandwidth against a catastrophic failure, without affecting the controller design. Furthermore, the current-limiting circuit allows integration of a non-intrusive override function.

6 Conclusions

The overall purpose of this project was to explore a solid-state-based isolated solution to the dilemma associated with safely breaking DC load fault current. After initial investigations, the full-bridge DC/DC converter topology was chosen to provide:

1. High-bandwidth fault-breaking frequency
2. Architectural capability for zero-energy breaking point
3. Galvanic isolation between source and load
4. Dual-purpose functionality combining relatively high-power DC/DC conversion with isolated circuit protection
5. Good steady-state operational efficiency

The work presented herein provides initial work in support of these goals, but these goals have, by no means, been fully accomplished. The results are promising enough to continue this research. The full-bridge DC/DC converter is in usage in some power supply applications [1]. Complexity of the design may be prohibitive for integration analysis of electrical system designs, affecting wider procurement of promising technology. Integration analysis requires stability analysis based on the large-signal and small-signal transfer functions. State-space modeling is intensive, although not impossible; but certain assumptions must be made anyway to expedite analysis. Averaged models for the full-bridge DC/DC converter had not yet been developed and tested, prior to this thesis, potentially easing the beneficial utilization of this architecture within power supply designs.

6.1 Summary of Work

The research for this thesis project required developing the transfer functions for the full-bridge DC/DC converter and demonstrating a functional design based on this

foundational work. In summary:

1. The averaged and reduced model of the full-bridge DC/DC converter was developed.
    - The large-signal and small-signal models for the full-bridge DC/DC converter were developed.
    - The parasitic resistances were moved to the inductor branch, reducing the average model for simplified analysis.
    - The calculated model was tested in MATLAB and compared well to the simulation results.
2. The parameters of the model were used to design a converter circuit, which was implemented within a full-bridge DC/DC converter for completeness.
    - Design sufficiency of the model was demonstrated with successful simulation results.
3. A simple current-limiting circuit was integrated and simulated.
    - The current limiter set a peak limit, which reduced output voltage, and therefore reduced output power, when over-loaded.
    - Ideally, the current would also be reduced. Nevertheless, current was successfully limited.

6.2 Project Contributions and Accomplishments

Within the work performed on the project, there are a few accomplishments which represent the author's contribution to the industry's body of knowledge. These are:

1. Development of the averaged model of the full-bridge DC/DC converter

- A design example validated the full-bridge converter, using the developed small-signal equations and a simulation.

2. Design of a current-limiting circuit integrated with the voltage-mode controller and gate drives.

   - The design was functionally validated through simulation.

3. An end-to-end design process was presented for the full-bridge DC/DC converter, using the circuit-averaging method.

   - The process may be utilized to improve state-of-the-art DC/DC conversion and protection systems.
     - The high-power DC solid-state breaker, *which does not yet exist*, can be developed using the methods presented herein.
     - Conversion and protection functions may be combined, thereby reducing size, weight, and complexity.

6.3 Lessons Learned

Over the course of this project, several principles and consequences manifested. Some of these are useful for continuing research efforts.

1. The development of the averaged and reduced model for the full-bridge DC/DC converter was somewhat intimidating, but fairly straightforward.

   - The analysis ultimately became similar to a standard buck converter analysis, after the model reduction and inclusion of the transformer turns ratio.
   - The transformer turns ratio n could be utilized to assist with voltage conversion. However, this requires some additional electromagnetic analysis, since the modified sine wave produced by the inverter may begin to saturate the core, if it is over-utilized.

2. Integrated current limit proved less reliable and less responsive when the design was more complex.
    - The final, and best-working, design was also the simplest design.
3. The full-wave diode rectifier was found to be very lossy, and especially intolerable at lower voltages.
    - Implementing a self-driven synchronous rectifier, to switch passively as a diode rectifier, was a somewhat trivial task.
    - The efficiency gains from utilizing a synchronous rectifier are significant.
4. Soft switching is much more complicated to implement than simply inducing a switching delay for some of the switches.
    - Modeling efforts must be the first step to implementing soft switching: shortcuts will result in design inadequacies.

6.4 Future Work

The design, as presented in this thesis, is not a fully-fledged zero-energy DC breaker; but it is certainly a first step in this direction, which encourages further development toward this end. The next steps are listed below.

1. The converter should be validated in hardware.
    - Sizing the transformer is critical for high voltage, high power applications.
        - If a contactor is to be replaced, then the transformer core cannot exceed the size and weight of the existing contactor.
    - Identifying a nearly ideal reference voltage source, resistant to fluctuation, will reduce susceptibility to undesired response.

2. Soft-switching techniques, such as Zero Voltage Switching (ZVS), could be utilized with this architecture, to break fault current at zero potential and zero current, at up to the switching frequency.

    - Additional model analysis is required to implement ZVS [13].
        - Designing for ZVS means the switch duty cycles cannot be divided into pairs D_A and D_B, complicating the model analysis and reduction.
    - Primary-side ZVS is required to implement a true DC breaker.
    - ZVS may be employed on both sides of the transformer, to protect against both source-side and load-side faults [9].
        - This development would also benefit the implementation of bi-directionality in the full-bridge DC/DC converter.

3. Soft-start capability, as described in [10], may be explored to prevent start-up transients and ringing due to charging the output filter capacitor, over a wide range of starting conditions.

    - A fully control-driven synchronous rectifier [8] or an active rectifier with ZVS may be employed for further control and efficiency gains [9].
    - Soft-starting may also benefit recovery from a current limit event.

4. The current limit circuit would benefit from further integration with the controller.

    - Integrated frequency analysis including the current limiter could provide a more elegant and functional solution.
        - Current-mode control programs the desired inductor current and controls on that point, increasing bandwidth of the controller [15] [16].

- Hard switching from the current limiter produces harmonics and intermodulation products.
- The ZVS break on a "zero crossing" equivalent must be ensured, possibly by designing in a zero crossing detector circuit [4].

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