DESIGN OF A HIGH-POWER, HIGH-EFFICIENCY, LOW-DISTORTION DIRECT FROM DIGITAL AMPLIFIER

A thesis submitted in partial fulfillment
of the requirements for the degree of
Master of Science in Engineering

By

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B.S., Wright State University, 2003

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I HEREBY RECOMMEND THAT THE THESIS PREPARED UNDER MY SUPERVISION BY Weston R. Earick ENTITLED Design of a High-Power, High-Efficiency, Low-Distortion Direct from Digital Amplifier BE ACCEPTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF Master of Science in Engineering.

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ABSTRACT

Earick, Weston R., M.S. Egr., Department of Electrical Engineering, Wright State University, 2006. Design of a High-Power, High-Efficiency, Low-Distortion Direct from Digital Amplifier.

For the process of converting low-power digital signals into their high-power analog counterparts, the functions of digital-to-analog conversion (at low power) and analog power amplification are separately implemented. This thesis proposes a new "STAC-DAC" circuit topology which directly realizes high-power analog output from low-power digital input signals. The ability to achieve a "direct from digital" high-power analog output in a single high-efficient, low-distortion design has significant potential in audio reproduction, and flexible signal generation applications.

In this thesis, the "STAC-DAC" is described and its implementation via MATLAB and LTSpice is discussed. The results of simulations are used to prove the concept of the design. The 16-bit design features a high-power output of 100 watts or more at an efficiency of 93%. The design is optimized to feature low total harmonic distortion (THD) of 0.055% for a 1 kHz signal at 100 watts into an 8 Ω load and low phase distortion of less than 10˚ for a 20 kHz signal and only 1˚ at 1 kHz.

The "STAC-DAC" design is applicable to any design which requires a high-power analog output that is controlled by a logic level digital input. The results validated that the "STAC-DAC" can produce low-level THD figures over the audio frequency

range. If very low THD figures are not necessary, high-power analog operation can be achieved into the hundreds of kilohertz while maintaining high efficiency. These results show that the power "STAC-DAC" is capable of simultaneously achieving the highly efficient circuitry associated with digital-to-analog converters with the low harmonic and phase distortion requirements associated with high fidelity analog audio amplifiers.

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1. INTRODUCTION

1.1 Thesis Motivations

Currently, digital-to-analog converters and power amplifiers are considered two separate entities. This does not have to be the case. There exists a need to efficiently produce high power analog outputs directly from easy to store and generate digital input signals. A “direct from digital” power analog output implemented all in one design, with low distortion figures fulfills a need within digital audio to directly drive a loudspeaker.

1.2 Thesis Objectives

It is the objective of this thesis to achieve the following:

- Present a brief overview of current digital-to-analog converters and power amps
- Propose a new design to merge D-A conversion and power amplification into one circuit
- Derive design equations for the new design
- Simulate the design for proof of concept
- Investigate the ability of the new design to produce high power analog outputs directly from logic level digital inputs at high efficiency
- Investigate ability of the new design to maintain low total harmonic distortion and low phase distortion over audio frequency band for application in an audio system
- Discuss limitations and future enhancements to the design

1.3 Thesis Organization

Chapter 2 presents the current types of DAC's and audio power amplifiers. The new top-level design is proposed along with its expected advantages.

Chapter 3 discusses the design of the "STAC-DAC" system in detail including both single-bit and multi-bit functionality along with power and efficiency calculations.

Chapter 4 discusses the filtering required at the output of the "STAC-DAC" along with the implementation of a volume control to the system.

Chapter 5 shows the test simulations that were run on the "STAC-DAC" and analyzes the results in order to obtain an optimal final design.

Chapter 6 shows the design conclusions and contributions as well as the design limitations and areas for future enhancements.

Appendix A shows the MATLAB code used to implement the ADC required on the front-end of the system.

Appendix B shows an example output from LTSpice where the frequency spectrum of a signal is analyzed and the THD is calculated.

2. IMPACT OF NEW DESIGN

2.1 Background Information

The storage, transmission and processing of information is a key component of our world today. This flow of information has become primarily performed in a digital manner due to the ease of digital technologies to perform the preceding tasks. Data conversion allows information that is normally analog, such as voice, to be stored, transmitted and processed in a digital fashion and then converted back to analog later as needed. Digital-to-analog converters, or DAC's, are circuits which accept n-bit digital words and output an analog signal that is equivalent to the digital input.

Some current DAC circuit topologies include R-2R, Binary-Weighted Resistor and Current-Scaled DAC's. The primary function of a DAC is simply to convert a low-power digital signal to its analog equivalent in a fast, efficient and precise manner. R-2R DAC's have a variable Thevenin equivalent resistance seen by the output depending upon which resistor "ladders" are switched into the circuit. The resistive ladders are switched into the circuit by the digital input bits. Depending on the value of the Thevenin resistance in the circuit, the output voltage is scaled to a corresponding analog output voltage. Similarly, Binary-Weighted Resistor DAC's have binary weighted resistors which directly scale the analog output voltage depending on which branch is switched into the circuit. This switching is also controlled by the digital input bits. In both topologies, the output voltage can be no more than the reference input voltage which is a

logic level digital input. In order to provide isolation from heavy loads and also to increase the output voltage, an amplifier stage can be cascaded after the R-2R or Binary-Weighted networks. The amplifier stage is usually an operational amplifier which can step up voltages but can not output large currents to drive things such as a motor or a loudspeaker. Current-Scaled DAC's, as the name suggests, simply scale binary weighted constant current sources or sinks depending on which current source is inserted into the circuit based on the digital input. All of the above examples are implemented on a low-power level where the main concern is the conversion of the signal. If a high-power analog signal is needed, another amplifier stage must be cascaded to provide the needed voltage or current drive.

Analog power amplifiers are any circuit which accepts a low-power analog input and increases the voltage, current or both, in order to provide a high-power analog output signal which is needed to drive heavy loads. An example where a high-power analog output is needed is in the field of audio reproduction. The types of power amplifiers are defined by their "class". The different classes are distinguished by their angles of conduction for the devices in the circuit. Common amplifier classes include: Class A, Class B, Class AB and Class D. Class A amplifiers operate over the full 360˚ of conduction. Class B amplifiers operate for exactly 180˚ and therefore need a second device acting in a push-pull fashion. Class AB amplifiers operate in the region between 180˚ and 360˚ and also require a complimentary device. Class D amplifiers operate between two voltage rails and are driven by a high-voltage pulse-width-modulated, or PWM, signal.

Though power amplifiers do a good job of supplying high-power analog outputs, they are limited by either low efficiency or high distortion figures. In general, it can be shown that those two figures of merit work together in an inverse manner for these amplifier classes. The more efficient the amplifier is the worse its distortion, as in Class B and Class D amplifiers. The lower the distortion is, the lower the efficiency of the amplifier, as in Class A amplifiers.

For the case where a power analog signal needs to be generated from a digital source than a DAC and power amplifier must be cascaded. If a low-distortion output is needed than the low efficiency of the power amplifier negates the high efficiency of the DAC. If a highly efficient circuit is desired than the increase in distortion of the amplifier negates the precision of the DAC. Neither of these results are desirable.

2.2 Design Overview

This thesis proposes a new circuit topology called a "STAC-DAC". This circuit has the ability to realize a high-power analog output directly from a low-level digital input. The "direct from digital" power analog output is contained in one single design. Therefore, the issues of cascading a data conversion stage with an amplification stage are nullified. Due to this, this design can attain high efficiency and low distortion figures simultaneously. This design has significant potential in the field of audio reproduction and will be simulated as a viable system to directly drive an 8 Ω loudspeaker load.

A top-level block diagram of a possible stereo audio system utilizing the "STAC-DAC" is shown in Figure 2-1.

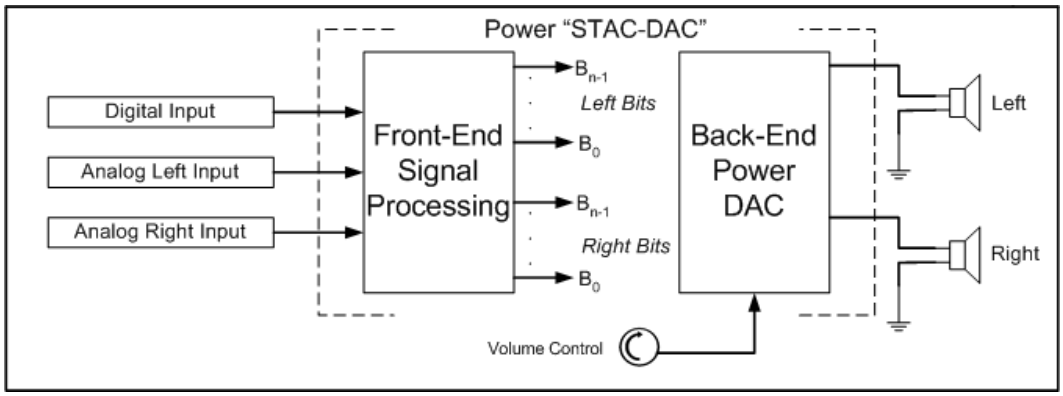


Figure 2-1 Top-level stereo audio system

An expansion of the front-end can be shown in Figures 2-2 and 2-3 and is shown for completeness.

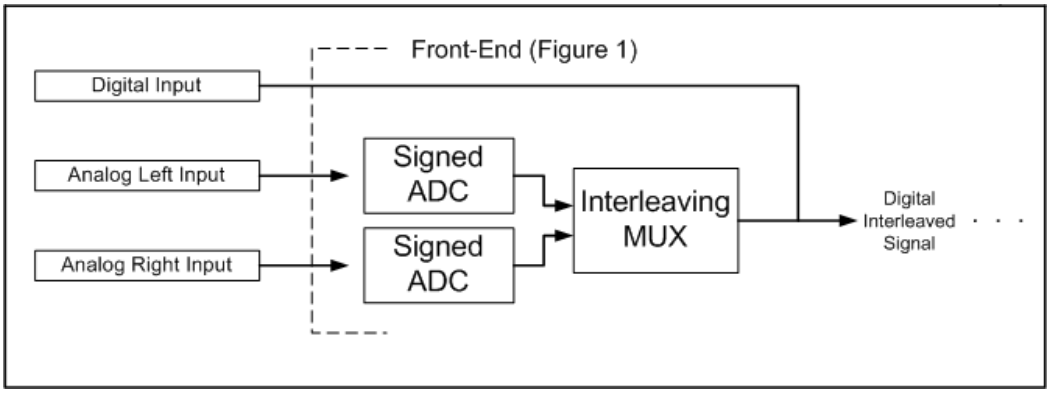


Figure 2-2 Front-End Block Diagram #1

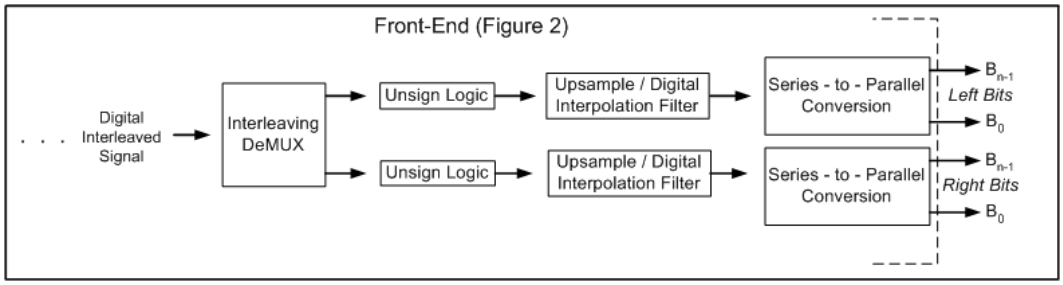


Figure 2-3 Front-End Block Diagram #2

The front-end of the system should simply allow for either digital or analog signal inputs and make sure the inputs to the power DAC are in their correct format. The two most notable blocks of this front-end design are the digital up sampling filters and the series-to-parallel converters. The digital filter allows the digital data to be up sampled to a larger effective sampling rate. Doing this allows the "STAC-DAC" to process digital data with a higher sampling rate as determined by the needs of the design. The series-to-parallel conversion is needed because the "STAC-DAC" makes use of the digital input bits simultaneously, therefore they must be presented in a parallel fashion.

From this point forward, this thesis focuses on the back-end power "STAC-DAC" design. A block diagram of the power DAC stage for a stereo application is shown in Figure 2-4.

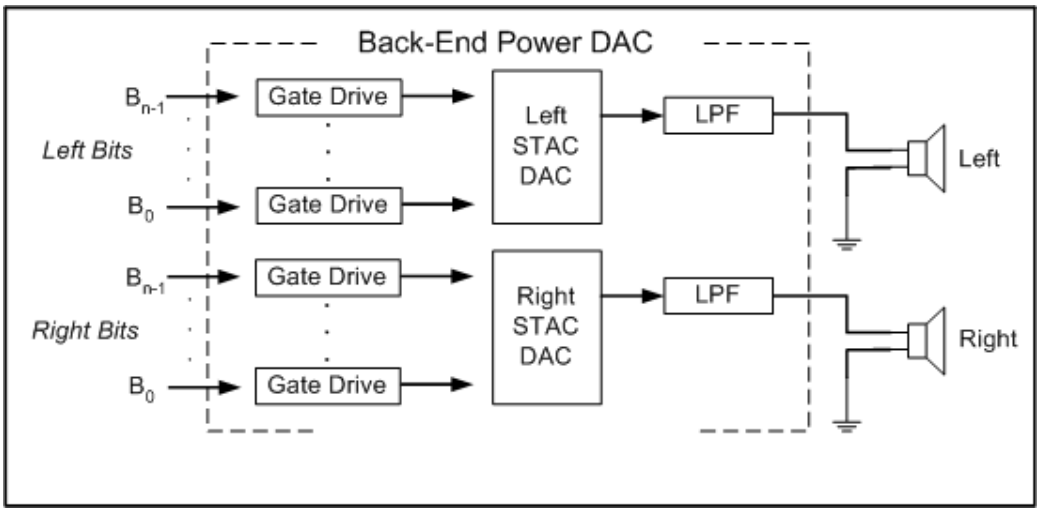


Figure 2-4 Block Diagram of power DAC

The "STAC-DAC" design implemented should be able to directly convert a logic level digital input to a high-power analog output to drive the loudspeaker load. The DAC

simulated in this thesis was chosen to have 16-bits of resolution to mimic the Red Book CD standard PCM digital inputs. In order to be a viable audio system the "STAC-DAC" should have a full power bandwidth exceeding the audible range of 20 kHz. The high power rating associated with this thesis was chosen to be 100 watts into an 8 Ω load. To meet the high efficiency requirements, the "STAC-DAC" should be able to obtain an efficiency of at least 90% while simultaneously providing a low-distortion output with a total harmonic distortion of less than 0.1% and phase distortion of less than 5˚ over the audio frequency band.

The power "STAC-DAC" will be shown to be capable of simultaneously achieving the highly efficient circuitry associated with digital-to-analog converters with the low harmonic and phase distortion requirements associated with high fidelity analog audio amplifiers. This results in the "STAC-DAC" design being applicable to any design which requires a high-power analog output that is controlled by a logic level digital input.

3. “STAC-DAC” DESIGN

3.1 Isolated Supply Concept

The idea for the power DAC designed in this thesis started with the goal of being able to sum a number of voltages in series. The same idea applies as when multiple batteries are connected together end-to-end to achieve a larger final voltage. This is only possible if the voltage supplies are isolated, or non-referenced, supplies.

Isolated point power supplies will supply a given voltage potential across their output leads which are not necessarily in reference to potential ground. This is accomplished by isolating the output from earth ground by use of a non-referenced transformer. To explain further, in the case of a ground referenced voltage supply, shown below in Figure 3-1, the negative output will be at earth ground. The positive output will be constant at the desired voltage giving the potential difference across the leads.

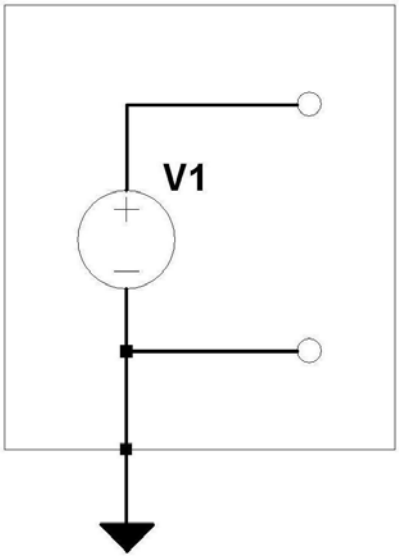


Figure 3-1 Ground Referenced Voltage Supply

For a non-referenced supply, shown in Figure 3-2, the negative output is not at earth ground and can actually take on any number of voltages. The positive output adjusts to remain the desired voltage above the negative output, keeping the potential difference across the leads constant. This attribute makes isolated power supplies suitable for summing voltages in series.

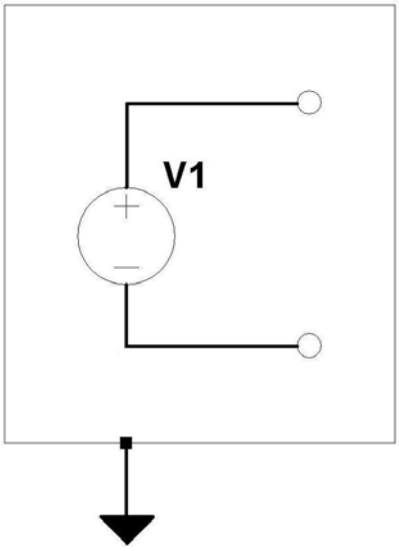


Figure 3-2 Floating Voltage Supply

When two or more isolated supplies are connected in series, the negative terminal of the top supply is forced to take on the voltage of the positive terminal of the lower supply. This causes the positive terminal of the top supply to adjust accordingly. When looking at the total potential difference from top to bottom of the series connection it can be seen that the voltages are indeed summed together, just like batteries, as desired. An example of this is shown below in Figure 3-3.

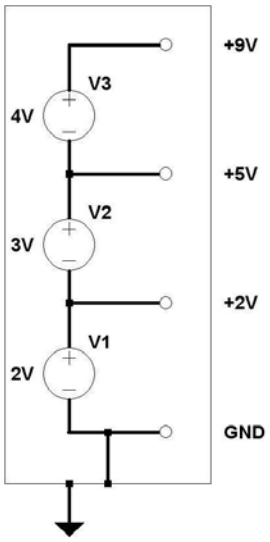


Figure 3-3 Series connected isolated supplies

With the ability to use isolated voltage supplies in order to sum voltages in series, a means of control was needed. The ability to toggle these isolated voltage sources in and out of the series circuit was required in order to produce an entire array of analog output voltages. Not only was the ability to toggle the voltages in and out of the series chain needed, but also to make the transitions as distortion less as possible and to make the entire circuit as efficient as possible.

3.2 Single bit "STAC" Functionality

The building block that was designed to accomplish toggling the isolated supplies in a series chain consisted of using a CMOS pair of MOSFET transistors. The single-bit "STAC" is shown in Figure 3-4.

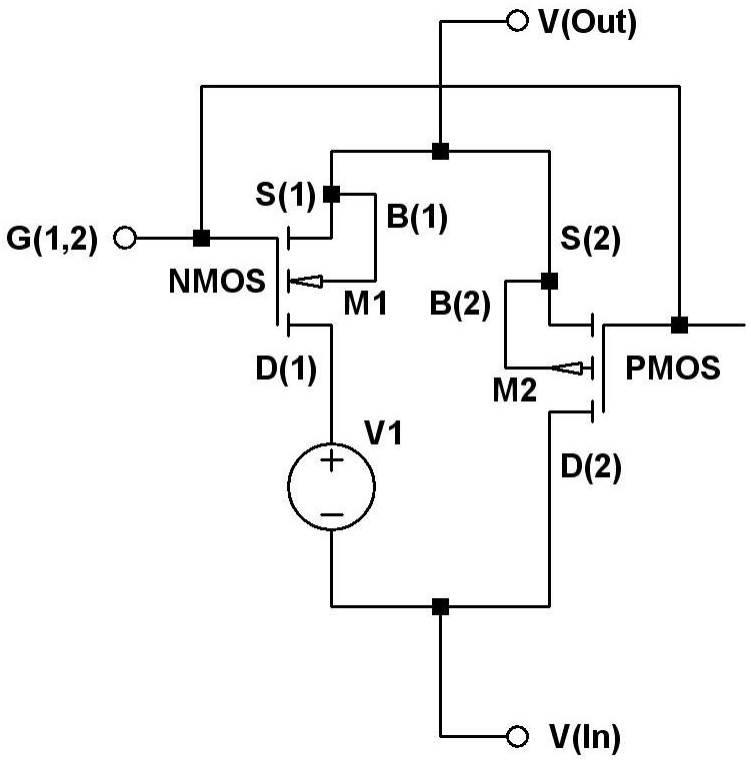


Figure 3-4 Single bit "STAC"

The name "STAC" is an acronym which stands for Source Toggled Addition CMOS. The isolated voltage sources are toggled, or switched, in and out of the circuit in order to add their voltages together by use of a CMOS pair of MOSFETs. The name is also a convenient play on words from the word stack, as this block is what physically links the voltage sources together in order to sum them or stack them on top of each other in series as explained earlier.

The two MOSFET transistors share a common gate and are therefore both driven by the same signal. These devices will be operated as analog switches. They are turned "on" or "off" by their gate-to-source voltage V_{GS}. The NMOS transistor will be turned on when its V_{GS} voltage is greater than its threshold voltage V_{THN} and conversely the PMOS transistor will be turned on when its V_{GS} voltage is less than its threshold voltage V_{THP}. Operation of the MOSFET transistors as switches means that they will be operating in their linear, or triode, regions as opposed to most analog designs which call for them to be operated in their saturation regions. Not only do these two transistors share a common gate terminal but they share a common source terminal as well. Knowing this, it can be seen that if their gate voltage is driven high enough with respect to their source voltage then V_{GS} will be greater than V_{THN} which will turn the NMOS transistor on and the PMOS transistor will remain off. An equivalent circuit diagram of this case is shown in Figure 3-5.

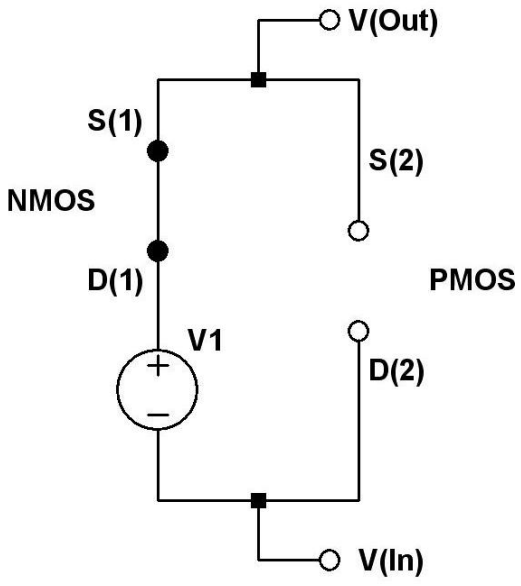


Figure 3-5 Single bit "STAC" with NMOS transistor conducting

For the case when the NMOS transistor is conducting, the equation for the top output voltage is shown in Equation 3-1.

$$V_{(OUT)} = V_{(IN)} + V_{(1)} \qquad \text{Equation 3-1}$$

If the gate voltage is driven lower than their source voltage, V_{GS} will be less than V_{THP} and the NMOS transistor will be turned off while the PMOS transistor will be turned on and will conduct current as shown in Figure 3-6.

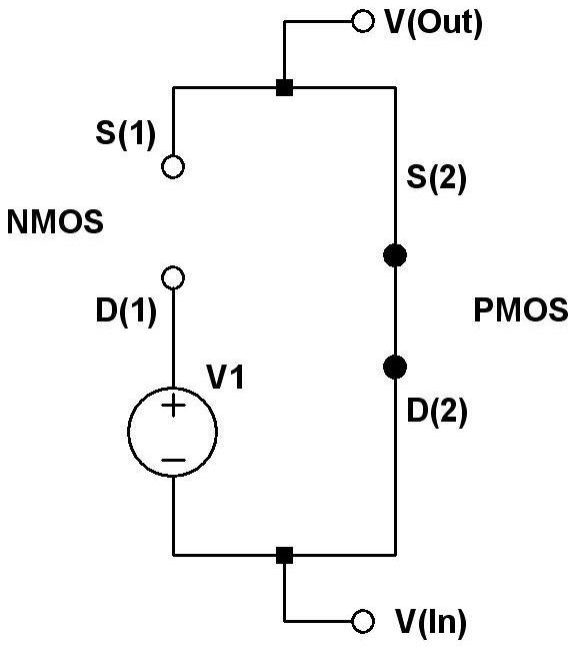


Figure 3-6 Single bit "STAC" with PMOS transistor conducting

For the case when the PMOS transistor is conducting, the equation for the top output voltage is shown in Equation 3-2.

$$V_{(OUT)} = V_{(IN)} \qquad \text{Equation 3-2}$$

In both cases, only one of the two transistors will be conducting at a given time. By operating the two transistors in this fashion it is shown that they act as a means of control in order to insert the voltage sources when desired simply by the voltage on their respective gates. Either the isolated voltage source is toggled into the series combination by turning the NMOS transistor on or the supply is bypassed, and not added, by turning the PMOS transistor on. This functional block allows the voltages in series to be summed as desired.

3.3 Gate Drive Circuitry

The gate voltage on each "STAC" in the digital-to-analog converter is the controlling voltage which toggles its corresponding voltage source into the series combination. Recall that in order to do this the gate voltage must be driven above or below the source voltage depending on which transistor is to be turned on. For the NMOS to be conducing, $V_{GS}>V_{TH(N)}$. For the PMOS to be conducting, $V_{GS}<V_{TH(P)}$. In basic digital circuit designs this is a trivial task; however that is not the case for this design.

For this digital-to-analog converter, the input is a multi-bit digital word. It is this digital word that will be used as the control signal for the DAC as was shown in Figure 2-4. Each bit of the digital word will be split from series to parallel in such a way that every "STAC" is directly controlled by a single digital bit.

Depending on what type of digital system you have to supply the digital word input, the range of voltages for a digital "1" and a digital "0" will vary. Most digital systems use 0 volts as the reference for logic level "0". Logic level "1" started out as 5 volts from the days of TTL logic and has since come down to 3.3 volts or even lower.

What specific reference level is used does not matter. As long as the reference system is known, it can be adjusted for accordingly, as will be shown later.

Looking at the single bit "STAC" it is seen that the source voltage is at the top. This means that for the top transistor, the source will be taking on the voltage of the desired output. Recall that in order to turn the NMOS transistor on $V_{GS}>V_{TH(N)}$, or $V_G-V_S>V_{TH(N)}$. It is also known that V_S=V(Out). Substituting and solving for V_G, the following equation is obtained.

$$V_G > V_{OUT} + V_{TH(N)} \qquad \text{Equation 3-3}$$

For the other instance, to turn on the PMOS transistor $V_{GS}<V_{TH(P)}$. Again, substituting and solving for V_G, the following is obtained.

$$V_G < V_{OUT} + V_{TH(P)} \qquad \text{Equation 3-4}$$

Large power analog outputs will put an extreme demand on the driving gate voltages to insure correct switching operation. It can also be seen that neither the source nor the drain of either transistor is referenced to any specific voltage, but they are both isolated in the same fashion as the voltage sources. The detrimental affect of this is that a typical digital voltage reference system will not be suitable to drive the gates of the two transistors. Additional gate driving circuitry is needed in order to step up the digital voltage supplied. This is similar to the gate drive circuitry needed in a DC-DC power converter or any power analog system which must operate transistors which do not have either their source

or drain referenced. The gate drive circuitry chosen to step up the digital input signal is shown below in Figure 3-7.

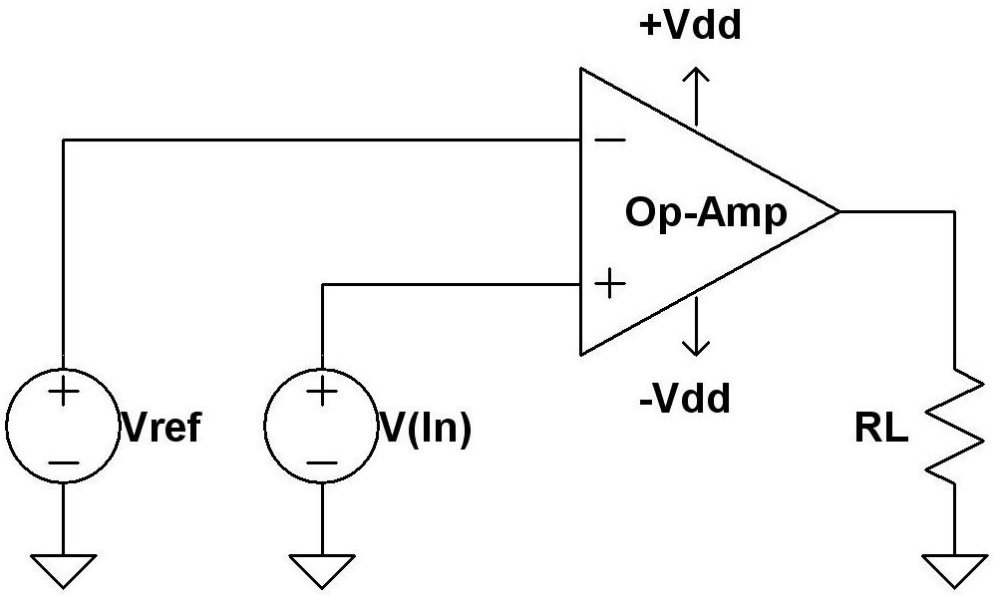


Figure 3-7 Gate Drive Circuit

The operational amplifier is operated in an open-loop fashion such that it acts as a comparator. The open-loop gain of an operational amplifier is extremely large. The amplifier, however, can not output any voltage larger than it is supplied with. Because of this, if driven high enough, the op-amp output will eventually saturate at approximately +/-Vdd – 2V. For the operational amplifier, the inverting and non-inverting input terminals are the input signals to the first stage of a differential amplifier. To analyze the ideal operation of the op-amp in closed-loop fashion it is shown that the voltage between the inverting and non-inverting terminals is zero. When operated in open-loop fashion, however, this is not the case. Therefore, any difference in voltage on the input will get amplified by the full open-loop gain. With the open-loop gain being so extremely large then any miniscule voltage difference on the input pins will cause the op-amp to

immediately saturate to one of its two power rails. This attribute lends itself to operation as a comparator as the op-amp will compare the voltage on the two input pins. The op-amp will detect whichever voltage is slightly larger than the other and output a voltage of +Vdd if the non-inverting terminal is larger or –Vdd if the inverting terminal is larger.

V(In), as shown in Figure 3-7 above, refers to a single bit digital control input voltage. V_{REF} is the reference voltage for the op-amp comparator and is held at a constant DC value for a given digital reference system. V_{REF} should be placed at exactly the middle voltage between the two digital reference voltages for logic "0" and logic "1". For instance, if a 0 volt to 5 volt digital reference system is used then V_{REF} should be placed at 2.5 volts. Obviously if any number of different digital reference systems are utilized then V_{REF} can, and must, be adjusted accordingly. This placement of V_{REF} is required because the fixed reference will become the voltage axis of symmetry for the op-amp output voltage. Whenever the non-inverting terminal goes above V_{REF} then approximately +Vdd-2 will be output and whenever the non-inverting terminal is below V_{REF} then approximately –Vdd-2 will be output. By placing V_{REF} in the middle of the digital reference system it allows the output voltage to mimic V(In) as closely as possible, only at a much higher voltage level. Figure 3-8 below shows the results of a circuit simulation in LTSpice illustrating this point.

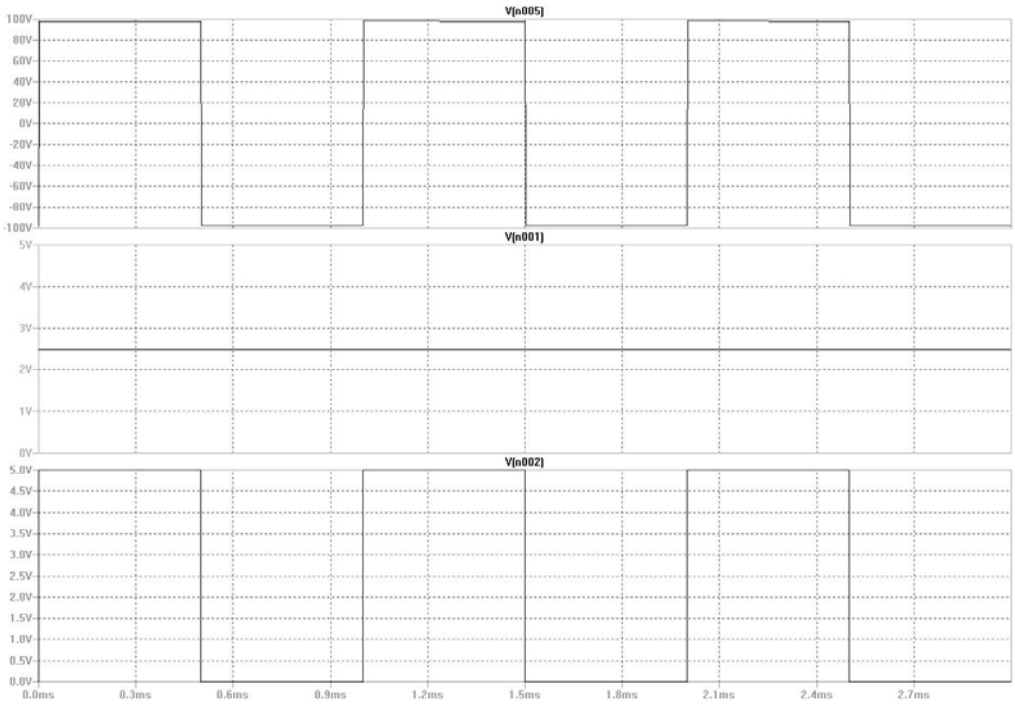


Figure 3-8 Example simulation of comparator gate drive circuit

In this simulation the signal V(n002) refers to the digital input voltage V(In) which ranges from 0 to 5 volts. The signal V(n001) refers to the DC reference voltage V_{REF} and is set to 2.5 volts. The signal V(n005) refers to the output voltage of the op-amp comparator. As can be seen from this simulation, when the digital input is logic "1" then the output voltage goes to +Vdd, in this case 100 volts, and when the digital input is logic "0" then the output voltage goes to –Vdd or -100 volts. This shows that the output voltage to the transistor gate terminals mimics the digital input voltage and is stepped up to a much larger value. Also, notice that the use of a positive and negative power supply on the op-amp comparator allows the voltage on the gate to be raised to acceptable levels in both the positive and negative directions. This meets the requirements stated as being needed in Equations 3-3 and 3-4.

Operational amplifiers have the ability to supply large output voltages. They do not have the ability to supply large output currents however. Using the op-amp in this fashion, for the gate drive circuit, still remains a viable solution. The voltage on the gate is what induces a channel in the MOSFET transistor and provides a path for current to flow. Since this circuit is simply driving the gate of two MOSFET transistors, no large output current is needed. In fact, the gate current for a MOSFET should be zero, neglecting small offset currents on the order of nanoamps. This makes this circuit sufficient to drive the gate voltages for the transistors in the "STAC".

3.4 Multi-Bit "STAC-DAC" Functionality

With the gate drive circuitry in place to correctly be able to drive the CMOS pair of transistors in each "STAC" it is then needed to hook them together in series to produce an analog output voltage which is the sum of the isolated supply voltage sources. Each single "STAC" is controlled by a single digital bit so for every additional bit an additional "STAC" is stacked on top to create the entire "STAC-DAC". A simple 4-bit circuit example is shown below in Figure 3-9.

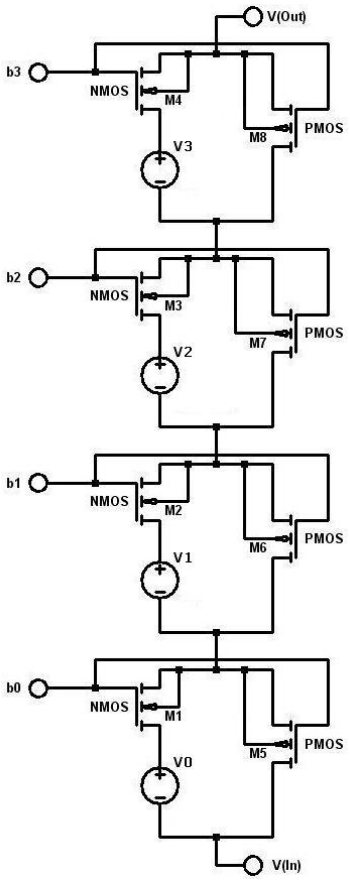


Figure 3-9 Simplified 4-bit "STAC-DAC" circuit

In the simplified circuit shown above the gate drive circuitry is not included. The inputs are labeled as a 4-bit digital input following the format $b_3b_2b_1b_0$, where b_3 refers to the most significant bit and b_0 refers to the least significant bit. As can be seen, the most significant bit will control the "STAC" at the very top of the stack and then decrease by bit until you get to the least significant bit at the very bottom of the entire stack. This implementation allows for the parallel digital input control. To fully illustrate the multi-bit functionality of the example circuit a truth table is shown below in Table 3-1. The input for the truth table is the 4-bit digital input and the output is the corresponding analog output voltage V(Out) with respect to V(In).

Digital Input ($b_3b_2b_1b_0$)	Analog Output V(Out)
0000	V(In)
0001	V(In) + V0
0010	V(In) + V1
0011	V(In) + V1 + V0
0100	V(In) + V2
0101	V(In) + V2 + V0
0110	V(In) + V2 + V1
0111	V(In) + V2 + V1 + V0
1000	V(In) + V3
1001	V(In) + V3 + V0
1010	V(In) + V3 + V1
1011	V(In) + V3 + V1 + V0
1100	V(In) + V3 + V2
1101	V(In) + V3 + V2 + V0
1110	V(In) + V3 + V2 + V1
1111	V(In) + V3 + V2 + V1 + V0

Table 3-1 Truth table for 4-bit "STAC-DAC"

Table 3-1 shows how b_3, or the MSB, being a "1" will correspond to adding the voltage source V3 into the series circuit while it being a "0" simply bypasses that voltage source. This continues in a similar fashion down to the LSB, or b_0, where it being a "1" will add the voltage source V0 into the series circuit or likewise become bypassed by a "0". The output of the DAC then becomes a stair-step output with a quantization level equal to the smallest possible step. In the example shown above, the quantization level would be equivalent to the voltage source V0 controlled by the digital input bit b_0.

Notice from the truth table output in Table 3-1 that this type of DAC can only add voltages to the output but can not subtract voltages. This means V(Out) can never be any less than V(In). This requires the use of a digital system where all 0's will correspond to the absolute minimum voltage and all 1's will correspond to the absolute maximum voltage. Not only does the digital system have to be referenced properly but then so does V(In) at the bottom of the stack. For this Power DAC circuit it is needed to be able to output not only positive voltages but negative voltages as well. Again, since the DAC can

only add voltages this means that V(In) must correspond to the absolute minimum output voltage desired, which in this case can not be ground but rather a negative voltage power supply set to $-V_{MAX}$.

The digital input control for this DAC is assumed to be a CD standard PCM signal which stands for Pulse-Code Modulation. In digital formats such as this each bit is weighted by a power of two, also called binary weighting since there are two possible states for each bit. For a 4-bit system, as shown in the example circuit above, the least significant bit b_0 will count as 1 or 2^0. Similarly, b_1 counts as 2 or 2^1, b_2 counts as 4 or 2^2 and b_3 counts as 8 or 2^3. By binary weighting each bit, it can be seen how it is possible to count, or represent, from 0 to 15 in this fashion for 4 bits. In this Power DAC design it is the aim to be able to exactly mimic the digital input at an amplified level by summing up the "1" bits together by use of the isolated voltage supplies. If the bits are weighted, this means that the power supplies need to be weighted in a similar fashion in order to correctly sum the output voltage.

The binary weighted voltage supplies in the "STAC-DAC" have to allow the output to swing all the way from $V(Out)_{MIN}$ to $V(Out)_{MAX}$. This maximum output swing is represented by $\Delta V(Out)_{MAX}$. For any N number of bits in a binary system there will be 2^N possible states where the lowest state of all 0's will correspond to $V(Out)_{MIN}$ and all 1's will correspond to $V(Out)_{MAX}$. Dividing the output waveform into 2^N different output levels corresponds to having 2^N-1 levels above $V(Out)_{MIN}$. The quantization level for the DAC, represented by ΔV_{QUANT}, is shown in Equation 3-5.

$$\Delta V_{QUANT} = \frac{\Delta V(Out)_{MAX}}{2^N - 1} \qquad \text{Equation 3-5}$$

This equation is derived by simply dividing the total voltage output swing by the number of quantized levels above the minimum. An illustration of this is shown below in Figure 3-10.

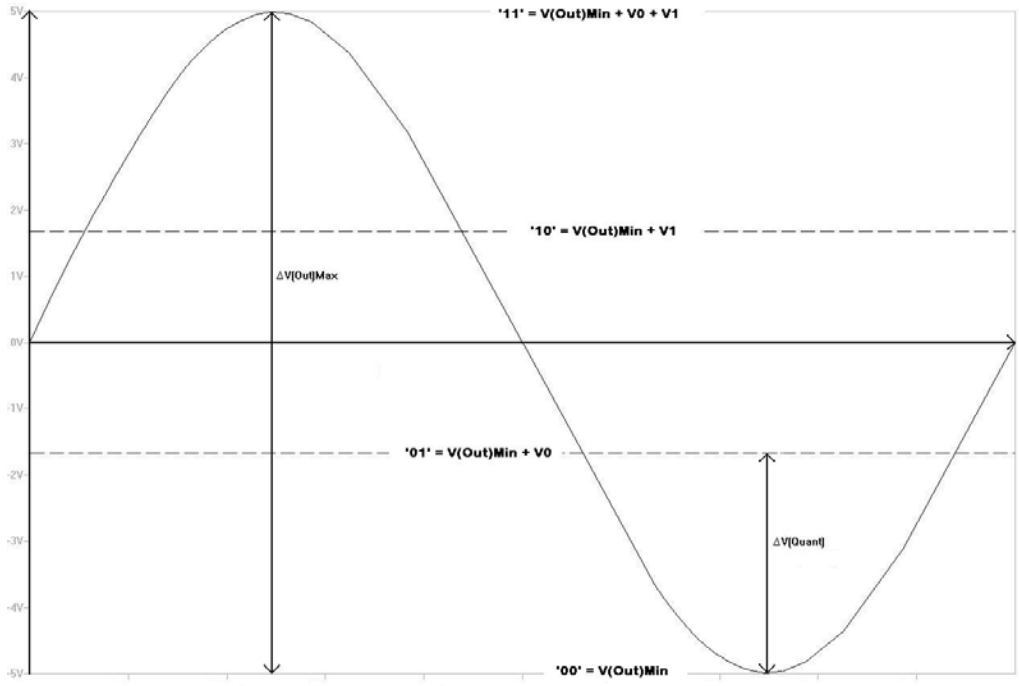


Figure 3-10 2-bit example of supply quantization

In the example shown above there are 4 quantized levels. This is accomplished using 2 bits of data. As explained earlier, the lowest state will correspond to $V(Out)_{MIN}$ so there are 3 remaining states above this value which need to be added to $V(Out)_{MIN}$ to obtain all four levels. These are the values needed by the isolated power supplies, in this case V_0 and V_1.

Knowing the quantization level it is possible to determine the exact values needed for each voltage supply to have them correctly binary weighted. Again, since the binary system is based on powers of 2, then so too are the voltage sources. This means that each voltage source up the "STAC" should be two times larger than the one directly below it.

By doing this it allows for each quantized level of output to be separated by exactly ΔV_{QUANT} when summing over the entire digital range. Each voltage source will be denoted as V_X. The variable "x" corresponds to each different individual voltage source and will vary from 0 up to N-1, which is equal to the total number of bits. For the case of a 4-bit system where the input will have the form $b_3b_2b_1b_0$ then the x-th power supply voltage will be denoted as V_3, V_2, V_1 and V_0 respectively. As the value of x increases up each "STAC" in the DAC, the corresponding voltage supply up the "STAC" is doubled. This simply means the quantization level needs to be multiplied by 2^X to get the corresponding value of the x-th voltage supply. The exact values of the binary weighted power supplies are dependent on two variables: the number of bits in the system represented by N and what spot in the "STAC" it occupies represented by x. The full equation for the binary weighted supplies is shown below in Equation 3-6.

$$V(N,x) = \frac{\Delta V(Out)_{MAX} * 2^X}{2^N - 1} \qquad \text{Equation 3-6}$$

In order to understand the full functionality of the multi-bit "STAC-DAC", the load it is driving needs to be known. It was the goal of this thesis to develop a Power DAC capable of directly driving a loudspeaker for use in audio applications. Though it is not exact, a first order approximation is used to model the loudspeaker as simply an 8 Ω resistor. An example of a full 4-bit "STAC-DAC" circuit including load, gate drive circuitry and a negative voltage supply reference is shown in Figure 3-11.

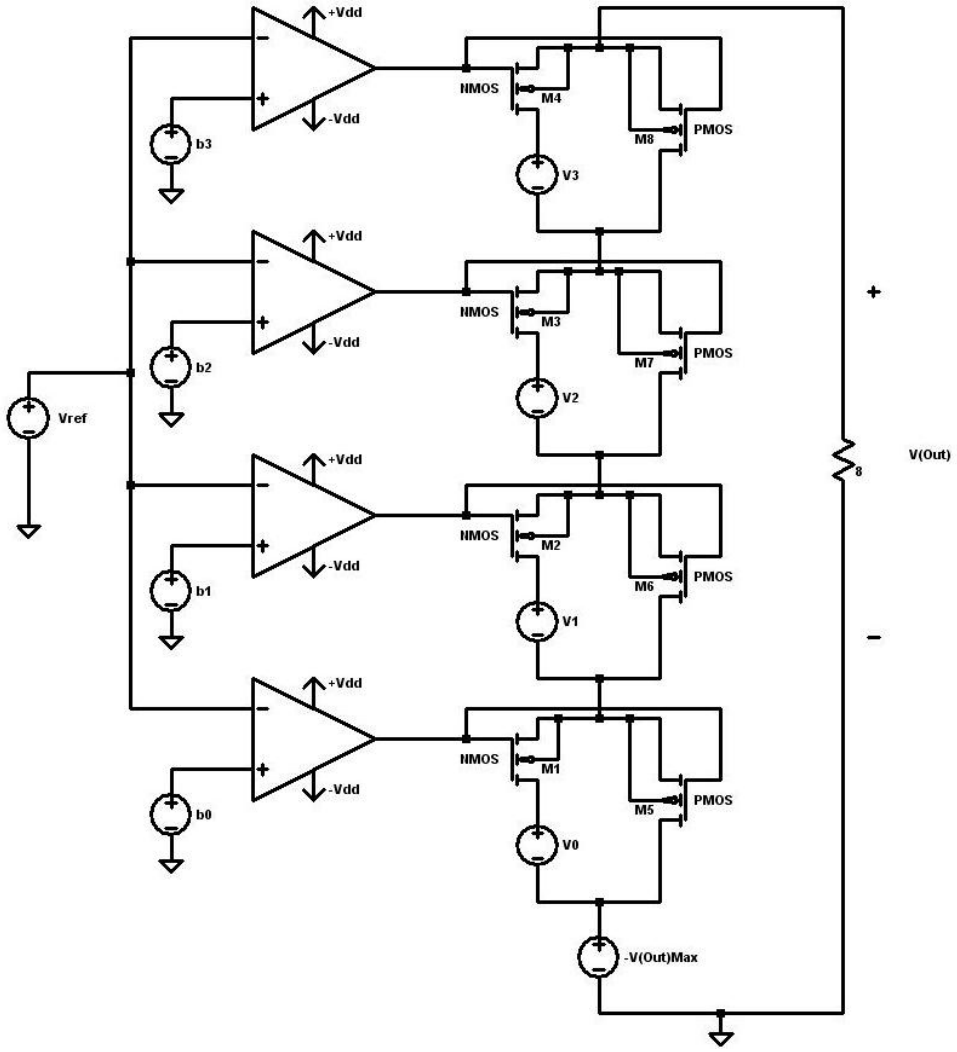


Figure 3-11 Complete 4-bit "STAC-DAC" example

3.5 Bi-Directional Current Flow

In order for the DAC to be able to output both positive and negative output voltages, the bottom of the "STAC" is referenced to a negative voltage supply. Once this is established, it is seen that the current flowing through the resistive load must be able to flow in both directions also. This implies that the MOSFET transistors are not going to simply act as uni-directional switches but as bi-directional switches.

Integrated MOSFET transistors have the ability to conduct current in either direction. Both the drain and source terminals are built into the same substrate. Due to this, the drain and source terminals are not distinctly specified but are referenced based upon the direction of the current flow. For a NMOS transistor, current will flow from the drain to the source. Whatever terminal has the lower potential is considered the source and the higher potential is considered the drain. For a PMOS transistor it is exactly the opposite, as current flows from source to drain.

There are two main implications to the current flowing in both directions for this integrated CMOS process. The first implication is that when the total current flowing through the series "STAC-DAC" switches direction, the drain and source terminals for every transistor which is conducting for that state will also get switched. Recall that the voltage V_{GS} is the voltage which turns each transistor on and off. As the source terminal changes from one side of the transistor to the other then the reference voltage for V_{GS} is also changed so it can no longer be assumed it is simply the voltage at the top of each "STAC". The amount in which the source voltage changes is equal to the voltage across the transistor switch when it is turned on. This is the voltage difference between the drain and source voltages, denoted as $V_{DS(ON)}$. This voltage develops because the transistor is not a perfect switch but has some dynamic "on" resistance r_{DS} between the drain and source when it is conducting. The relationship is shown in Equation 3-7 below.

$$\Delta V_{S(MAX)} = V_{DS(ON)} = r_{DS(ON)} * i_D \qquad \text{Equation 3-7}$$

Since it is already the aim to output a large power analog signal as efficiently as possible then the dynamic "on" resistance for each transistor should be minimized, otherwise all

the power will be dissipated as heat in the internal resistance of the transistors and the efficiency will be reduced. The fact that this value is small is advantageous as it means the source voltage will not experience a noticeable change.

The second implication of the drain and source switching physical sides of the MOSFET transistors in the "STAC-DAC" is that the bulk terminal will no longer always be tied directly to the source. By not having these terminals tied directly together it is possible to have a voltage difference V_{SB} present. A voltage V_{SB} will cause transistor body effect. The body effect which is induced by this voltage results in a change in the threshold voltage V_{TH} of the transistor. Under normal operation, when no body effect is present, the threshold voltage V_{TH} is equivalent to V_{TH0}. When there is body effect the threshold voltage is given by Equation 3-8.

$$V_{TH} = V_{TH0} + \gamma\left[\sqrt{2*\phi_f + V_{SB}} - \sqrt{2*\phi_f}\right] \qquad \text{Equation 3-8}$$

In the case where body effect is present, the bulk will be tied to the drain instead of the source. Therefore, the voltage V_{SB} will be equal to the negative voltage across the transistor V_{DS} as shown in Equation 3-9.

$$V_{SB} = -V_{DS} \qquad \text{Equation 3-9}$$

Substituting Equation 3-9 into Equation 3-8 we can obtain the body effect threshold voltage as a function of V_{DS} shown in Equation 3-10.

$$V_{TH} = V_{TH0} + \gamma\left[\sqrt{2*\phi_f - V_{DS}} - \sqrt{2*\phi_f}\right] \qquad \text{Equation 3-10}$$

As was the case with V_{GS} changing only slightly due to V_{DS} being a small number, the body effect will also be very slight. Notice however that since V_{DS} is being subtracted in Equation 3-10 that when the body effect is present, the threshold voltage will actually decrease as opposed to normal body effect causing a higher V_{TH}. At first glance this could appear to be a disturbing feature for this circuit with potential current runaway, but it will be shown later that it indeed is not a problem.

It is possible to implement the "STAC-DAC" using discrete MOSFET transistors also. When using discrete transistors, as opposed to integrated transistors, the source and drain are separated on each side of the substrate. Because of this, the drain and source are fixed and not interchangeable. This means the current is only supposed to flow in one direction conventionally. Discrete transistors will conduct normally when operated in the forward-biased region. When the current changes direction, however, this forces the transistors to operate in the reverse-biased region where V_{DS} is negative.

With the source and drain terminals separated by the body, this acts as a P-N junction between the two. This P-N junction has the function of a diode. When modeling the operation of a discrete MOSFET then, one must consider an anti-parallel body diode in parallel with the device. The anti-parallel diode allows for the conduction of current in the opposite direction as conventionally shown. This occurs in the reverse-biased breakdown region. A circuit schematic showing the anti-parallel body diode is shown in Figure 3-12 below.

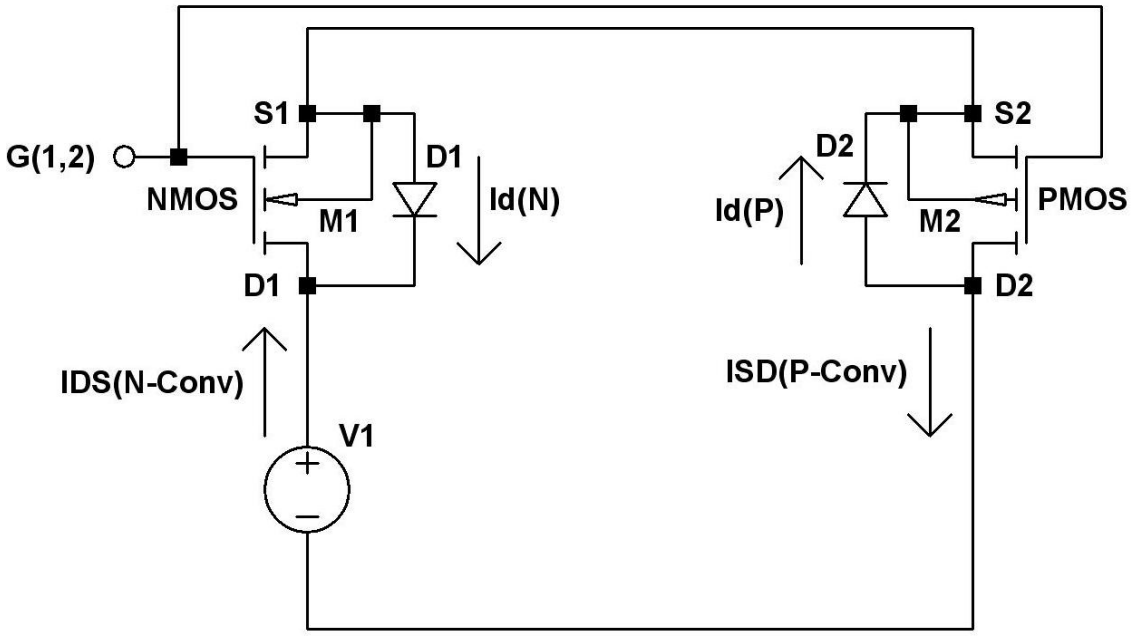


Figure 3-12 Discrete MOSFET "STAC" with anti-parallel diodes

When each transistor is forward biased it allows the conventional current to flow. The conventional current is denoted as I_{DS}(N-Conv) for the NMOS transistor above and I_{SD}(P-Conv) for the PMOS transistor above. Once breakdown is reached, the anti-parallel diodes will allow current conduction in the opposite direction.

Upon simulation of a discrete MOSFET it is seen that the transistor will actually conduct current in the reverse-biased region even before the anti-parallel diode conducts. The discrete transistor will in fact operate in reverse-bias in much the same way an integrated MOSFET would, with the current curve being reflected about the origin. This operation continues in the reverse-biased linear region until the turn-on voltage of the diode is reached. Depending on the make-up of the P-N junction and material of the diode, a normal diode will drop approximately 0.7V across it when conducting. Until this voltage is applied across the diode it does not conduct. Once this voltage is overcome, the

diode takes over the conduction from the transistor and breakdown occurs where the current increases rapidly for small increases in voltage. Figure 3-13 below shows a theoretical i-v characteristic curve for a NMOS discrete MOSFET with the anti-parallel body diode.

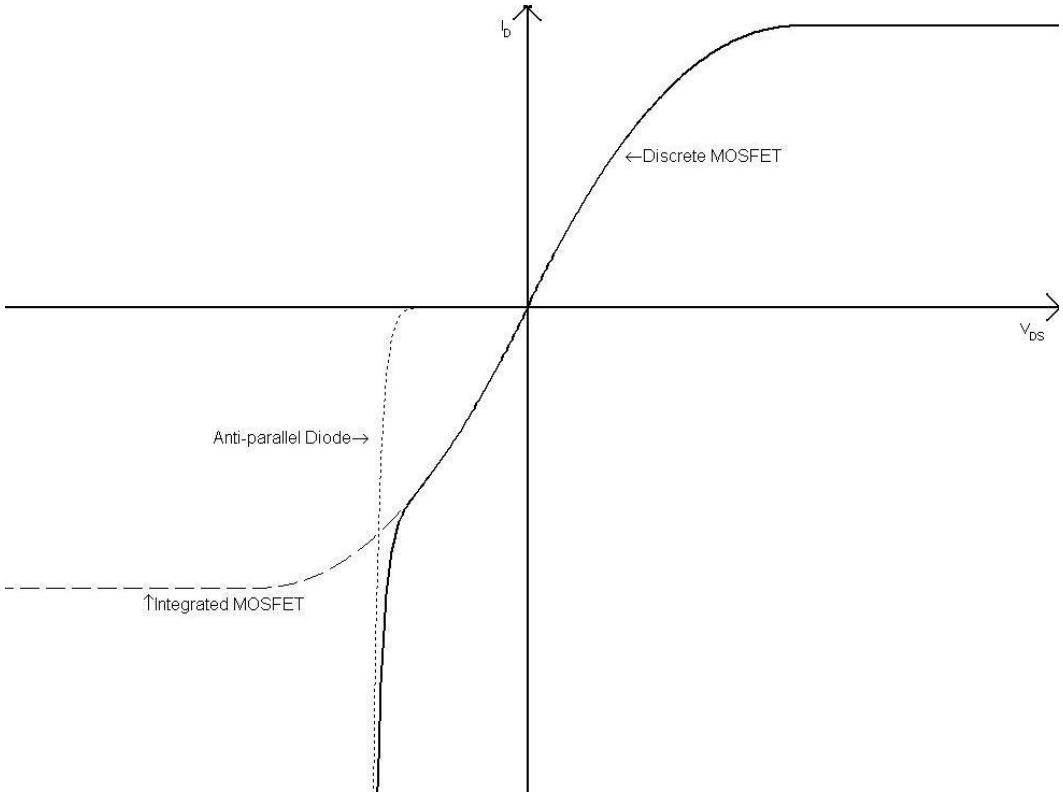


Figure 3-13 Theoretical discrete MOSFET i-v characteristic curve

Figure 3-14 below shows the four distinct regions of operation for the discrete MOSFET.

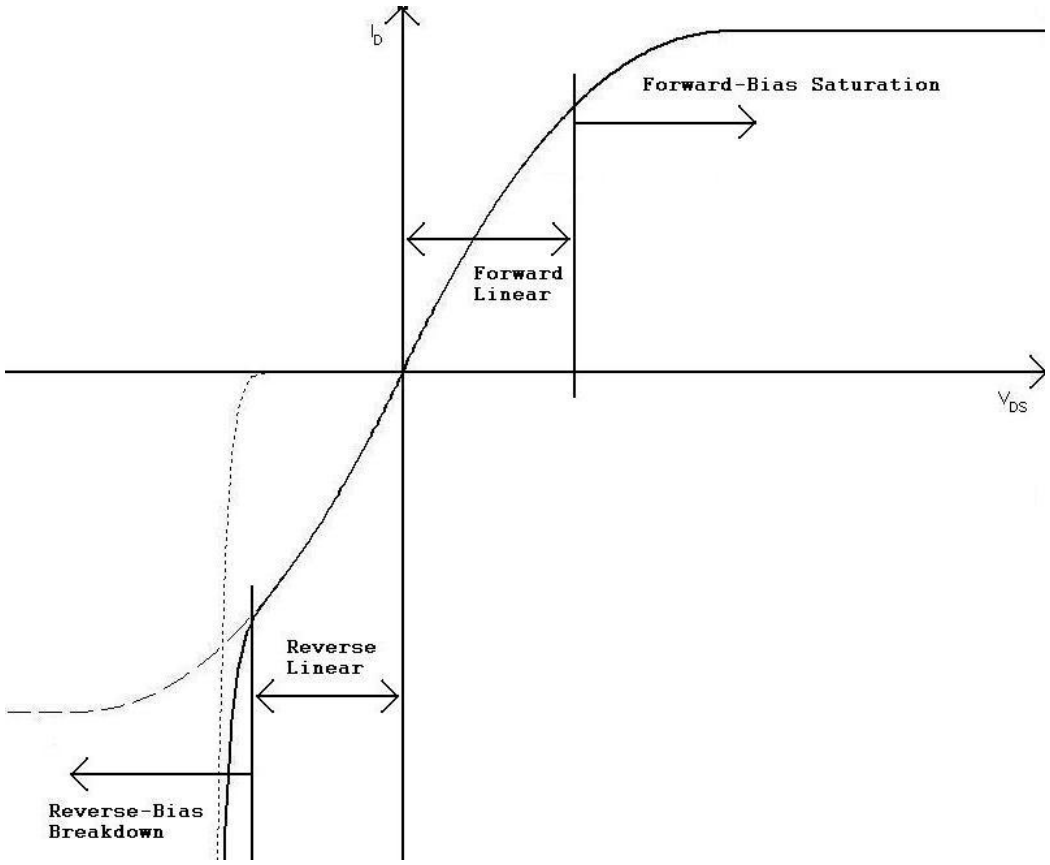


Figure 3-14 Discrete MOSFET regions of operation

From the figures it can be seen that the discrete MOSFET and integrated MOSFET operate identically when in the forward-biased linear region as well as the forward-biased saturation region. In the reverse-biased linear region the discrete MOSFET will also conduct in the opposite direction much like the integrated MOSFET. The difference is seen when the discrete MOSFET reaches the reverse breakdown region and the diode takes over while the integrated circuit simply goes into reverse-biased saturation. A simulation of a discrete MOSFET in LTSpice is shown below in Figure 3-15 which correctly verifies this type of operation.

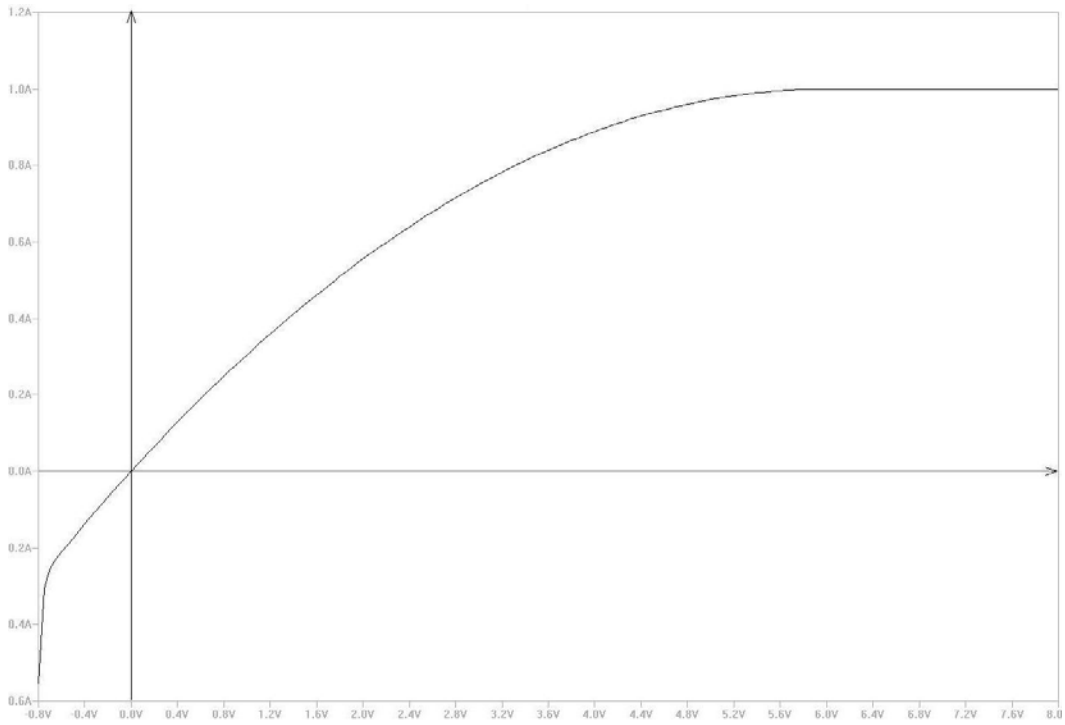


Figure 3-15 LTSpice simulation of discrete MOSFET

With the desired operation of the "STAC-DAC" to be a high power output device with high efficiency, then a very small voltage drop V_{DS} is required across the transistor when it is conducting. This means that the MOSFET will be operating only in the linear, or triode, regions of operation. Due to this, the reverse-biased breakdown region should never be entered such that V_{DS} never reaches the -0.7V needed to turn the anti-parallel diode on. This also means the device should operate linearly about the origin, or in other words, it should conduct by the same amount, independent of the direction of the current.

3.6 Current Drive Capabilities

For MOSFET transistors operating in the linear regions, the current equation which describes their characteristic curve is defined by the Sah equation given in Equation 3-11.

$$i_D = K'\left(\frac{W}{L}\right)\left[(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right] \qquad \text{Equation 3-11}$$

In order to produce a high power output to drive a loudspeaker load directly from the DAC, the current drive needs to be very high, on the order of amps to tens of amps. For efficiency issues and to keep the transistor switch in the linear regions of operation, V_{DS} needs to remain very small. Also, since each "STAC" in the DAC forms a series circuit than the maximum output current must be able to flow through each transistor equally.

Notice that since the current flowing through each transistor is now known, it is possible to define the dynamic "on" resistance $r_{DS(ON)}$ as well. By simply using Ohm's Law the resistance is defined as the voltage divided by the current. The "on" resistance of each transistor is the voltage across it, V_{DS}, divided by the current through it, i_D. This resistance is dynamic however, so it actually refers to the change in voltage divided by the change in current. Taking the limit as the change in current becomes very small we can get this ratio at a single point which is simply defined as the derivative of V_{DS} with respect to i_D. When looking at the characteristic curves for a transistor we see that it is plotted as current, i_D, versus voltage, V_{DS}. In the desired linear regions of operation the slope of this line is defined as the change in the y-axis variable divided by the change in the x-axis variable which is the change in current divided by the change in voltage. Again

taking the limit so this change becomes small this becomes the derivative of i_D with respect to V_{DS} as shown below in Equation 3-12.

$$slope = \frac{\Delta y}{\Delta x} = \frac{\Delta i_D}{\Delta V_{DS}} \rightarrow \frac{di_D}{dV_{DS}} = K'\left(\frac{W}{L}\right)\left[\left(V_{GS} - V_{TH}\right) - V_{DS}\right] \qquad \text{Equation 3-12}$$

Notice that the equation for the slope of the transistor curve is the inverse of that defined for the dynamic "on" resistance. The full derivation of this resistance is shown below in Equation 3-13.

$$r_{DS(ON)} = \frac{\Delta V_{DS}}{\Delta i_D} \rightarrow \frac{dV_{DS}}{di_D} = \frac{1}{slope} = \frac{1}{K'\left(\frac{W}{L}\right)\left[\left(V_{GS} - V_{TH}\right) - V_{DS}\right]} \qquad \text{Equation 3-13}$$

It should also be noted that the dynamic resistance $r_{DS(ON)}$ is not a physical resistance but is simply a model of the "on" resistance across the transistor. This dynamic resistance emerges due to the fact that the drain and source terminals are not physically connected together within the semiconductor device therefore the current is not completely free to flow without resistance. If $r_{DS(ON)}$ were equal to zero then that would imply a slope on the characteristic curve of infinity. This would mean that the transistor would never operate in the linear region but would go immediately from being turned on into saturation.

Recall, however, that for this application we desire a large output current with a very low value for V_{DS}. This implies that we need the slope of the characteristic curve to be very large and, in turn, the dynamic resistance $r_{DS(ON)}$ must be very small.

Equation 3-11 shows three possible ways to get large currents out of each transistor while maintaining a highly efficient analog switch with small voltage losses making the characteristic curve's slope larger.

The first way to get large transistor currents with a small voltage drop across it is by using a transistor with a very large value of K'. K' is known as the transconductance parameter and has the units of $\left(\frac{A}{V^2}\right)$. The equation for the transconductance parameter of a NMOS transistor is given in Equation 3-14.

$$K' = \mu_n C_{OX} \qquad \text{Equation 3-14}$$

In this equation μ_n is the electron mobility and is a constant determined by the material used to build the transistor. For example, intrinsic silicon has an electron mobility of approximately $1350\left(\frac{cm^2}{Vs}\right)$. In the case of a PMOS transistor, Equation 3-14 is changed by replacing μ_n with μ_p which is the mobility of holes. The second parameter in Equation 3-14, C_{OX}, is the oxide capacitance per unit area of the parallel-plate capacitor formed between the gate terminal and the induced channel within the transistor. The oxide capacitance is defined in Equation 3-15.

$$C_{OX} = \frac{\varepsilon_{OX}}{t_{OX}} \qquad \text{Equation 3-15}$$

In the above equation ε_{OX} is the permittivity of the oxide layer of the transistor. This parameter will also change depending on what material is used in designing the transistor, for example silicon oxide. The bottom number in Equation 3-15, t_{OX}, is simply the thickness of the oxide layer. Substituting Equation 3-15 into Equation 3-14 we can get the transconductance as a function of physical device parameters as shown in Equation 3-16.

$$K' = \mu_N \left(\frac{\varepsilon_{OX}}{t_{OX}} \right) \qquad \text{Equation 3-16}$$

It is easily seen from Equation 3-16 that the physical design of the transistor and material used is what directly affects the transconductance parameter. An example integrated transistor could have a transconductance on the order of $20\left(\frac{\mu A}{V^2} \right)$.

Recent advancements in semiconductor technology have led to the rise of discrete Power MOSFET transistors. Power MOSFET transistors employ a different physical design than previous transistors and also utilize different physical materials. Due to this, it allows them to have transconductance parameters much larger than integrated or typical discrete transistors. An example Power MOSFET transistor could have a transconductance on the order of $1\left(\frac{A}{V^2} \right)$, or 50,000 times larger than the example integrated transistor detailed above.

A second option to get larger transistor currents is to increase the channel size, or width of the transistor. Discrete Power MOSFET transistors are designed at a given size for a particular part number. One must review the datasheets to select the appropriate transistors to supply the correct amount of current drive. Integrated transistors, however, can be designed to whatever size the designer desires. Depending on what size technology is being used in the CMOS fabrication process, the length of the channel should be kept at the minimum value allowed by that technology. By holding the channel length to a minimum and then increasing the channel width, the ratio $\left(\frac{W}{L}\right)$ is increased, therefore allowing larger current drive.

Referring back to the MOSFET characteristic curves in Figure 3-14 it should be noted that generally, in the reverse-biased linear region, the output current i_D is usually very small. Since the transistors in this DAC are forced to operate in this region than large currents are needed in this region as well. By utilizing transistors with very large transconductance parameters or by using extremely large transistor sizes, the slope of that characteristic curve will be increased to a large enough value that sufficient forward and reverse-biased output current can be supplied without forcing the transistor into either the saturation or breakdown regions.

A third and final option to increase the current to sufficient levels is to use a large V_{GS} voltage. As described earlier the source voltages will be isolated and variable, so the only way to accomplish this is by utilizing large gate voltages. The gate drive circuitry detailed earlier is sufficient to supply these fairly large voltages. Due to the fact that the voltage V_{GS} needs to be large for current drive purposes then it is advantageous to drive the gates with even larger voltages than required in Equations 3-3 and 3-4.

Recall from the last section that for current flowing in the opposite direction, as conventionally shown, there will be body effect present which affects the threshold voltage of the transistor. A typical threshold voltage will be on the order of a couple volts. If the gate voltage is driven to a high enough level, such as to produce a voltage V_{GS} which is much larger than V_{TH}, then any small changes in V_{TH} from the body effect will only have a negligible affect on the transistor current characteristics. It was stated earlier that during reverse-biased operation the bulk terminal is tied to the drain terminal instead of the source terminal. The body effect in this case was then shown in Equation 3-10. The relationship between the threshold voltage and the current is shown in Equation 3-11. Combining these two equations we can see how the body effect will directly affect the current shown in Equation 3-17 below.

$$i_D = K'\left(\frac{W}{L}\right)\left[\left(V_{GS} - \left(V_{TH0} + \gamma\left[\sqrt{2\phi_f - V_{DS}} - \sqrt{2\phi_f}\right]\right)\right)V_{DS} - \frac{V_{DS}^2}{2}\right] \quad \text{Equation 3-17}$$

From this equation it can be seen why this could appear to be a very troublesome attribute for integrated transistors. When the transistor is conducting in the reverse-biased region than the voltage V_{DS} will be some small positive number after the drain and source terminals are flipped for the sake of reference. A positive V_{DS} will cause the new threshold voltage V_{TH} to actually be lower than V_{TH0} without body effect. A lower threshold voltage will cause the transistor current to want to increase. As the transistor conducts more current it will cause the voltage V_{DS} to rise slightly more. This increased V_{DS} will cause the threshold voltage to go even lower and the transistor to conduct more still. Quickly, it can be seen how a current runaway state could be reached. The saving

grace to the multi-bit "STAC-DAC" is that it is a series circuit. Because of this, the current through each "STAC", and therefore each conducting transistor, will be forced to be at the desired current to satisfy KVL around the series circuit. The implication of this is that even if the transistor exhibits body effect and wants to enter a current runaway state it will not be allowed to do so because the rest of the circuitry will force the current to stay at the desired level.

3.7 Power and Efficiency

This "STAC-DAC" is designed to be a high power output device. This is accomplished by using transistors that have large current drive capabilities and also by using large isolated point voltage supplies. The exact values of these binary weighted voltage supplies were derived in Equation 3-6. This equation is a function of $\Delta V_{OUT(MAX)}$ and varies depending on the desired power output of the system.

The power output rating of a device is defined as its average power output for a sinusoidal signal. This rating is calculated using the rms value of the voltage output and is shown below.

$$P = \frac{V_{rms}^2}{R_L} \qquad \text{Equation 3-18}$$

The parameter $\Delta V_{OUT(MAX)}$ is physically the difference between $V_{OUT(MAX)}$ peak and $V_{OUT(MIN)}$ peak. Because of this, it is needed to relate the power to the peak output voltage instead of the rms value. The rms value of a sinusoidal voltage is equal to the peak value of the voltage divided by $\sqrt{2}$. Substituting this into Equation 3-18 yields the power as a function of peak voltage shown below.

$$P = \frac{V_{pk}^2}{2R_L}$$ Equation 3-19

Solving Equation 3-19 for the peak voltage shows the needed $V_{OUT(MAX)}$ peak voltage for a desired output power.

$$V_{pk} = \sqrt{2R_L P}$$ Equation 3-20

For a sinusoidal signal which is centered around zero, $V_{OUT(MIN)}$ peak is equal to negative $V_{OUT(MAX)}$ peak. Substituting this yields the result that $\Delta V_{OUT(MAX)}$ is equal to 2 times $V_{OUT(MAX)}$ peak, or simply the peak output voltage. Substituting this into Equation 3-20 above yields an equation which shows $\Delta V_{OUT(MAX)}$ as a function of the desired output power.

$$\Delta V_{OUT(MAX)} = 2\sqrt{2R_L P}$$ Equation 3-21

Equation 3-21 can be substituted back into Equation 3-6 in order to obtain the values of the binary weighted power supplies as a function of the output power.

$$V(N, x, P) = \frac{2 * \sqrt{2R_L P} * 2^x}{2^N - 1}$$ Equation 3-22

Once the desired output power is known, the maximum peak voltage across the resistive load can be determined. Once this is known, the "STAC-DAC" can be designed to output this voltage correctly by adjusting the voltage supplies as shown above. Also, once the peak output voltage is known, the peak output current can be determined. Assuming a purely resistive load this is calculated simply by using Ohm's Law. By knowing the maximum output current drive, the transistors in the "STAC-DAC" can either be chosen or designed for properly as defined in section 3.6.

Another parameter that needs to be worried about, especially for a high power device like the "STAC-DAC" is the efficiency of the device. For most audio amplifiers, the audible quality of the system is inversely proportional to the efficiency. The "STAC-DAC" attempts to achieve both audio quality as well as high efficiency simultaneously. Much like switching power supply technology and Class D audio power amplifiers, it can be seen that the only source for power losses in the "STAC-DAC" is the voltage drop V_{DS} across each conducting transistor due to its dynamic resistance r_{DS}. Since the "STAC-DAC" was specifically designed to keep this voltage drop low, as discussed previously, it will be able to achieve high efficiency numbers.

The maximum theoretical efficiency of the "STAC-DAC" can be derived by looking at a simple 2-bit "STAC-DAC". Figure 3-16 below shows the 2-bit "STAC-DAC" with resistive load used for the derivation. For the ease of calculations, the bottom of the "STAC-DAC" is referenced to ground instead of $-V_{OUT(MAX)}$.

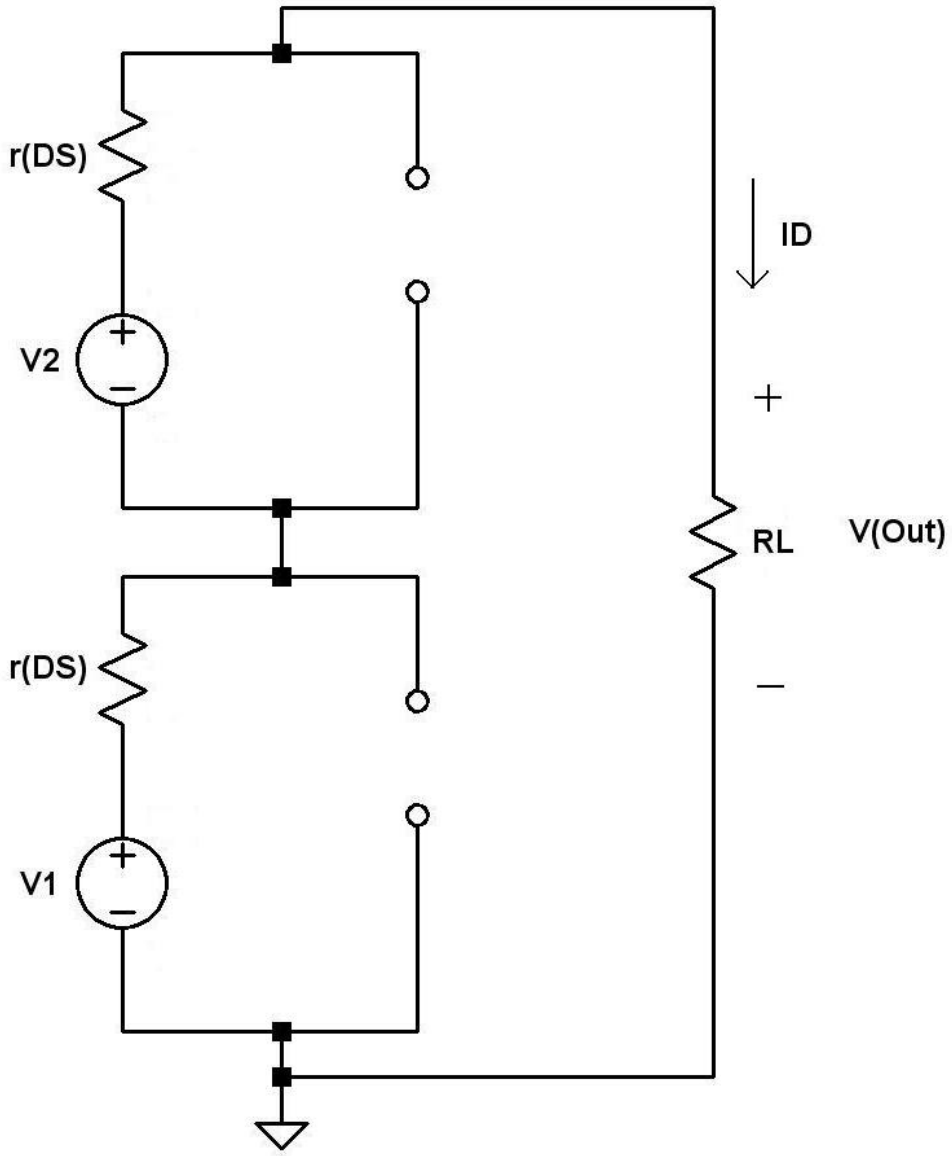


Figure 3-16 2-bit efficiency example

In this derivation for the maximum efficiency of the "STAC-DAC", it was assumed that the dynamic resistance, r_{DS}, of each transistor is the same. Notice that for each individual "STAC" in the DAC either the PMOS or NMOS transistor will always be on. By assuming that every transistor has the same dynamic resistance, the efficiency calculation can be made independent of what digital state the DAC is in.

Since the "STAC-DAC" is a series circuit, the output current i_D is the same current that runs through every component. Knowing this, KVL can be applied around the circuit loop as shown below.

$$V1 - i_D r_{DS} + V2 - i_D r_{DS} - i_D R_L = 0 \qquad \text{Equation 3-23}$$

Equation 3-23 can then be solved for the output current i_D. This equation is then expanded from this 2-bit example to any number of bits N.

$$i_D = \frac{V1 + V2}{2 * r_{DS} + R_L} \rightarrow \frac{\sum V_{input}}{N * r_{DS} + R_L} \qquad \text{Equation 3-24}$$

From Ohm's Law, the output voltage V(Out) is simply the current found in Equation 3-24 multiplied by R_L.

The efficiency of a circuit is defined as the power output divided by the power input. The power input to the "STAC-DAC" is just the sum of the voltage supplies. Because of this, the efficiency can be defined as the ratio of V(Out) to the sum of the voltages supplied. The difference between these numbers will be the power dissipated by the conducting transistors as heat. The theoretical efficiency for any N-bit "STAC-DAC" is shown below.

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT}}{\sum V_{input}} = \frac{R_L}{N * r_{DS} + R_L} \qquad \text{Equation 3-25}$$

Figure 3-17 shows a plot of the theoretical efficiency of the "STAC-DAC" versus the transistor dynamic resistance r_{DS} for an 8-bit, 16-bit and 24-bit DAC.

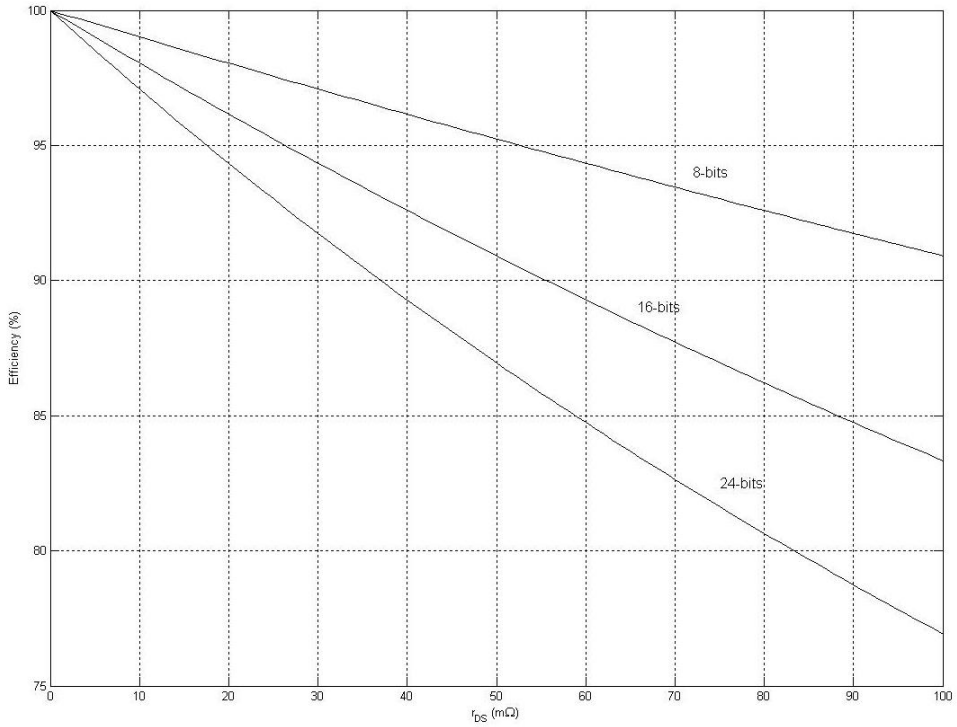


Figure 3-17 Theoretical efficiency of "STAC-DAC"

As can be seen from this figure, as long as the dynamic resistance of the transistors is held to a minimum, the efficiency can exceed 90 to 95 percent for an 8 Ω load. The efficiency improves beyond this figure if the load is increased.

4. SIGNAL CONDITIONING

4.1 Low-Pass Output Filter

The output of the "STAC-DAC" will be a high power analog signal. This signal, however, will be in the shape of a stair-step since it is just the sum of the weighted voltage supplies. The precision of the stair-step output is defined by the quantization size of the DAC. For the "STAC-DAC" design, the quantization was derived in Chapter 3, Equation 3-5. The quantization is equivalent to the minimum length, from top to bottom, of each "step" in the stair-step output. The width, from left to right, of each stair-step is equal to the time between digital samples and is defined as $\frac{1}{f_S}$, where f_S is the sampling frequency of the system. Figure 4-1 shows an example stair-step output and Figure 4-2 shows the stair-step output of a 4-bit "STAC-DAC" for a 20 kHz input signal.

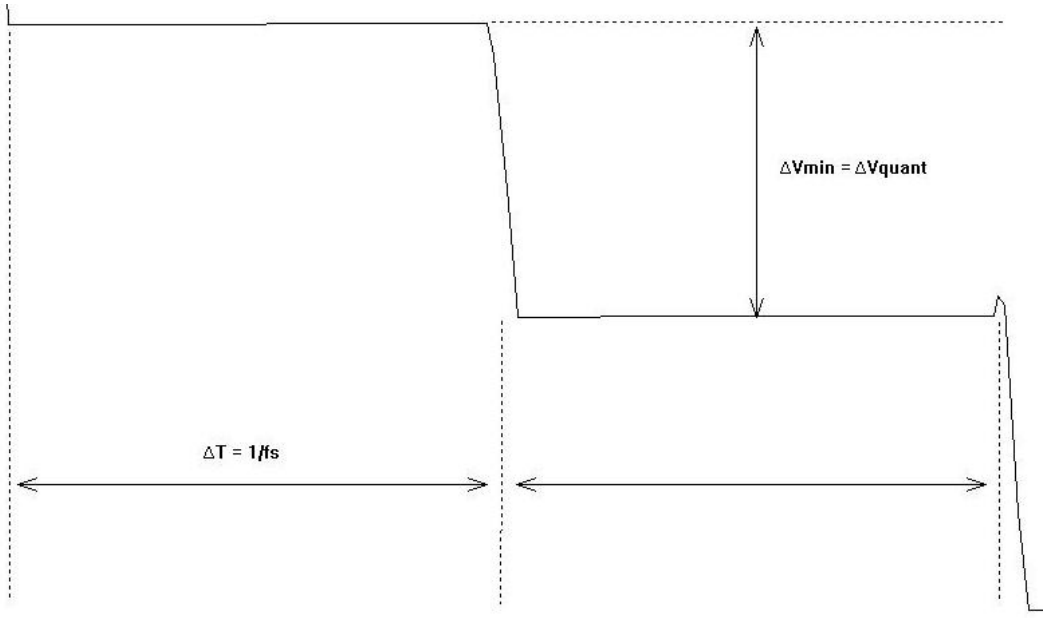


Figure 4-1 Example stair-step output

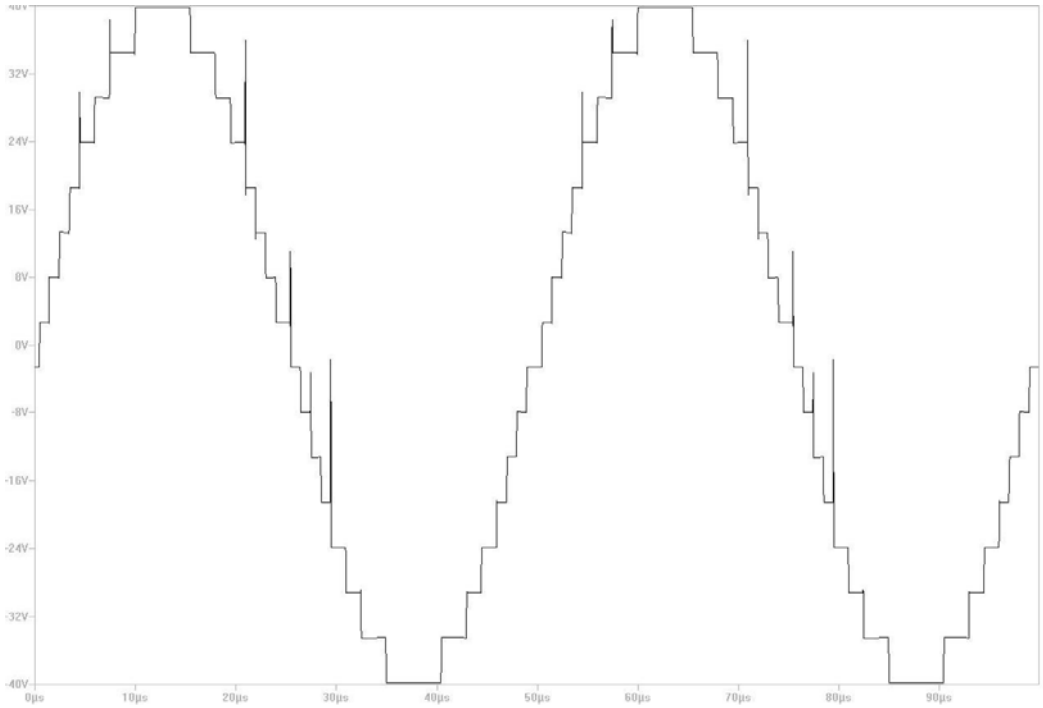


Figure 4-2 4-bit stair-step output

The final output of the "STAC-DAC" needs to be a smoothed signal in order to accurately represent sinusoidal input voltages or musical signals. This means that the stair-step output of the DAC needs to be integrated over time in order to smooth the signal. Integration can be accomplished by the use of a low-pass filter.

In order to understand how a low-pass filter accomplishes integration, a fundamental understanding of how a low-pass filter operates is needed. A low-pass filter will simply allow signals with low frequencies to pass unchanged while attenuating signals with high frequencies. The easiest way to represent this functionality is by looking at its step-response. Figure 4-3 shows a step-response for a low-pass filter.

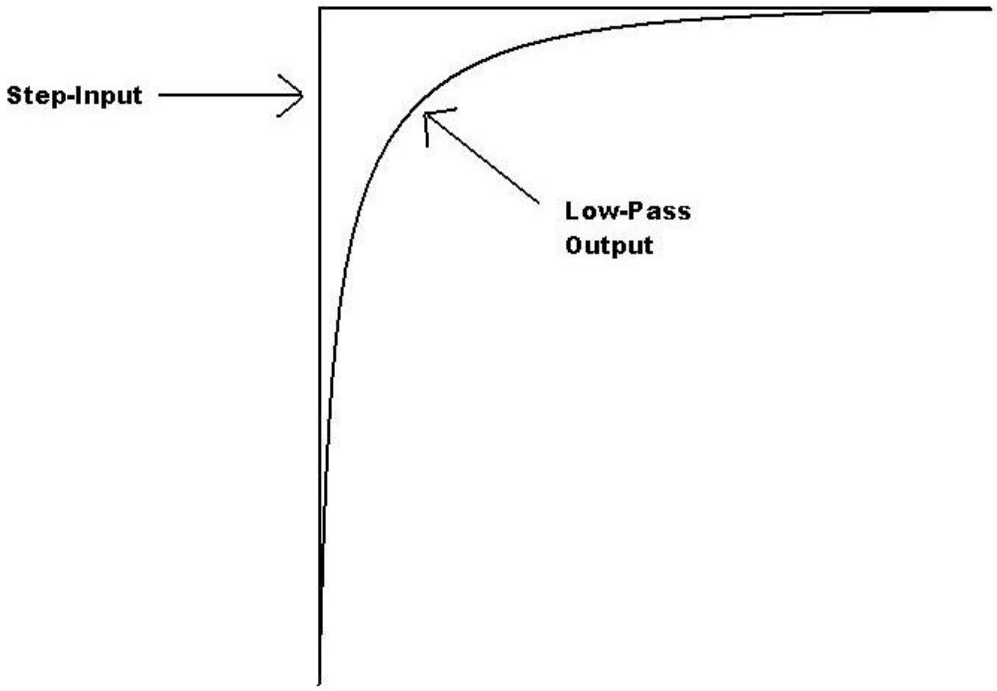


Figure 4-3 Step-response of a low-pass filter

At the far left, the step input changes. This corresponds to a very high frequency, approaching infinity. The low-pass filter will not allow this signal to be passed and

therefore the output remains unchanged. After the step-input changes it levels off at a constant value which corresponds to a frequency of zero. The low-pass filter allows this frequency of signal to pass to the output so the output rises up until the output equals the input. It can be seen from this figure that the output signal is simply the integral of the input, verifying that a low-pass filter is in fact an integrator.

The frequencies that a filter removes can be shown by its frequency response diagram, known as the Bode plot. A Bode plot of an example first-order low-pass filter is shown in Figure 4-4 below.

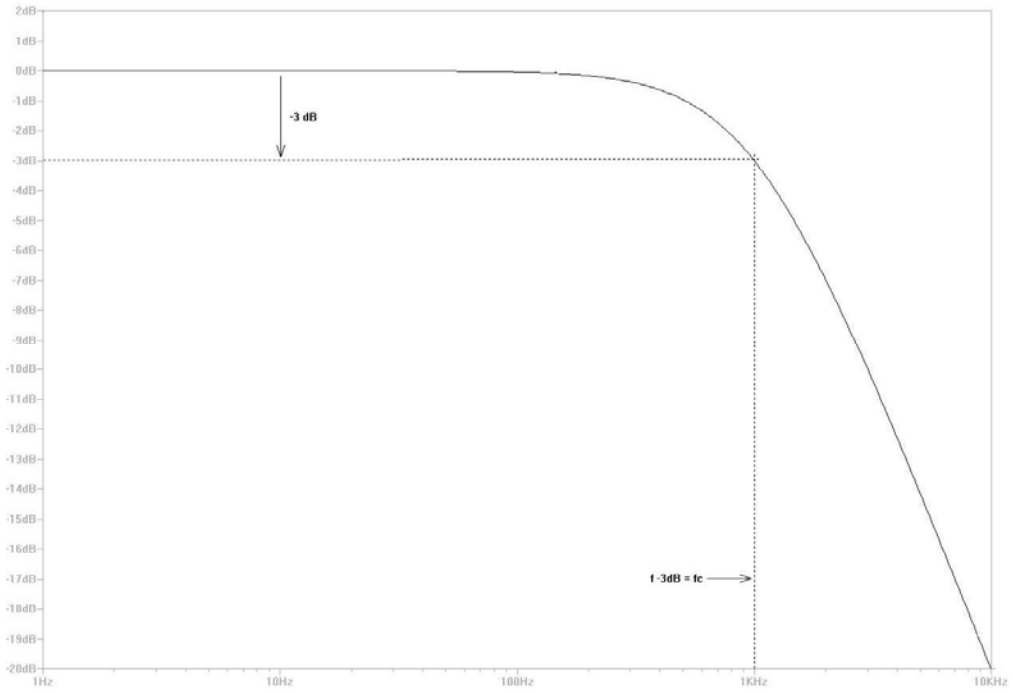


Figure 4-4 1st order LPF Magnitude Bode Plot

The Bode plot shows the magnitude of the filter transfer function in dB versus frequency. The cutoff frequency, f_C, of the filter defines the cutoff between frequencies that the filter passes and frequencies which are attenuated. The cutoff frequency occurs where the

magnitude of the filter transfer function is 3 dB down from the pass band. Due to this, f_C is also sometimes referred to as f_{-3dB}.

The frequency spectrum of the stair-step output will contain many frequencies. It contains the fundamental frequency of the input signal as well as the frequency of switching and many harmonics. The switching frequency is actually the sampling frequency of the system and is present because this is the frequency in which the DAC changes states. Harmonic frequencies are present because each step in the stair-step output can be approximated by a square wave. The frequency spectrum of a square wave contains the fundamental frequency as well as all of the odd multiples of the fundamental frequency, known as the odd-ordered harmonics. It is intuitive that the harmonic frequencies present will be at higher frequencies than the desired fundamental frequency output, for a pure sinusoid. In order to satisfy the Nyquist sampling theory, the sampling, or switching, frequency will also be larger than the fundamental frequency output. The use of an integrating low-pass filter will remove the high frequency content present in the stair-step output and leave the low frequency fundamental. In doing this integration a smoothed, sinusoidal version of the stair-step will be obtained.

Placing the cutoff frequency of the low-pass filter low enough will result in only the fundamental frequency remaining. Doing this causes the output to be a pure sine wave. This is the generally desired output for typical sinusoidal DAC's. The "STAC-DAC" designed in this thesis however, is aimed at reproducing music. Music does not consist of a single frequency sinusoid but many frequencies all at the same time. The range of these audible frequencies is determined by the range of human hearing. This range is generally accepted to be from 20 Hz to 20 kHz. This range for human hearing

only applies to pure tones, or pure sine waves, which as stated above is not musical at all. Not only does music contain multiple frequencies all at the same time, but it also contains harmonics, or overtones, of these frequencies. These musical overtones affect the tone color. For a musical instrument, this is known as its timbre. It can be shown that humans can sense, and therefore "hear" harmonics well beyond the generally accepted 20 kHz figure. All of this information is needed in order to select a proper cutoff frequency for the low-pass filter in order to maintain its musical tonality and accuracy.

The order of a filter refers to the number of poles present in the transfer function. In general, the number of reactive, or energy storing, circuit elements in the filter equals the number of poles in the system which also equals the order of the filter. In relation to the Bode plot, the order of the filter refers to how quickly the filter attenuates the signal after the cutoff frequency is reached. This is also sometimes referred to as the "roll off" of the filter. The higher the system order, the faster the filter will roll off. Figure 4-5 compares the roll off of a 1^{st} and 2^{nd} order low-pass filter at the same cutoff frequency.

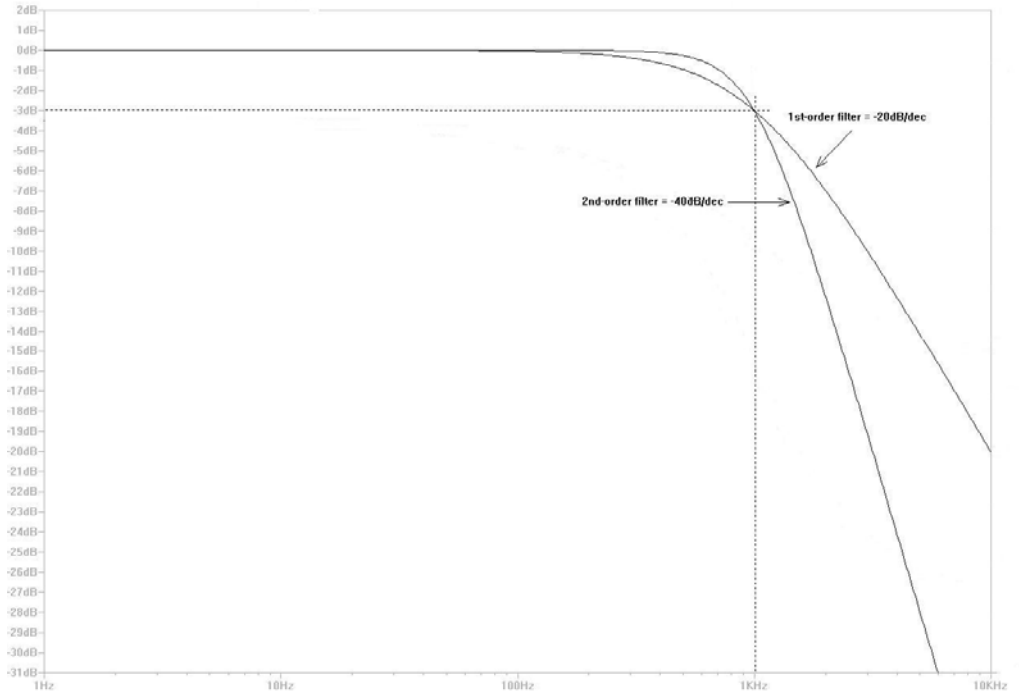


Figure 4-5 Comparison of 1st order and 2nd order low-pass filters

As can be seen in the above figure, a first order filter will roll off at a rate of 20 dB for every decade increase in frequency. A second order filter will roll off at a rate of 40 dB for every decade increase in frequency.

A filter not only affects the magnitude of the output signal but its phase as well. In normal DAC operation, the phase response is not necessarily critical but for audio applications it is very important. Phase is important for audio applications because it is what gives us our directional cues for sound. Our brain distinguishes the direction of a sound based upon the difference in time in which the sound is received by our respective ears. A delay in time is a phase shift. These directional cues occur mainly at short wavelengths which correspond to high frequencies. This means that in order for an audio system to maintain stereophonic sound then it must maintain as close to a phase less

response as possible over the audible range, especially at the high frequency end of the spectrum.

A filter begins changing the phase of the output a decade below the cutoff frequency and continues up to a decade above the cutoff frequency. Figure 4-6 shows the phase distortion for the same two filters as were compared in Figure 4-5.

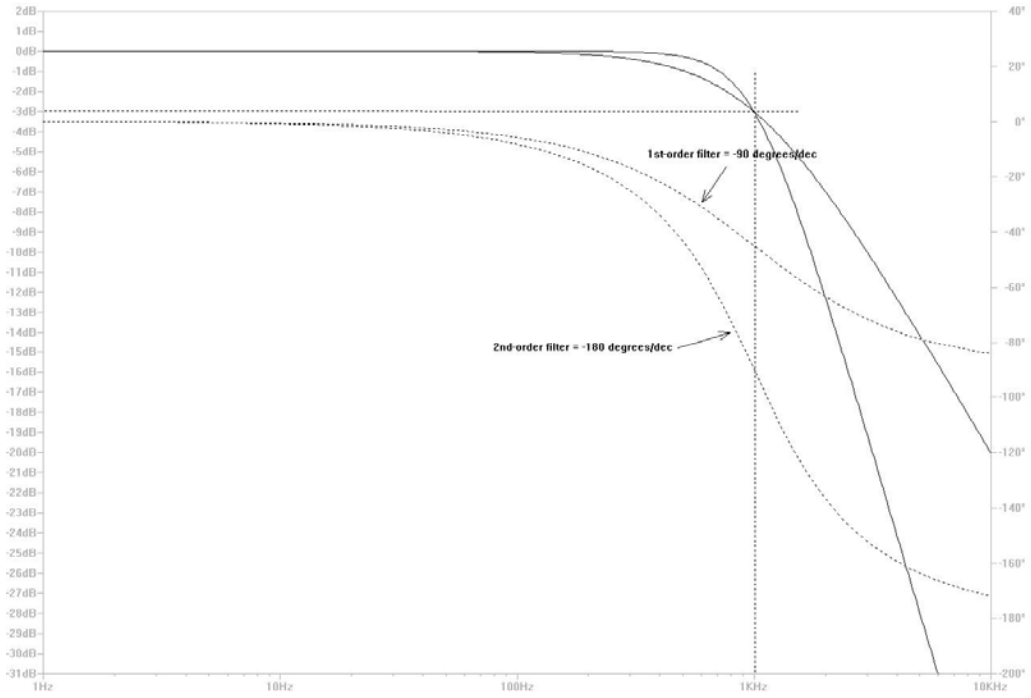


Figure 4-6 Phase response of low-pass filters

As shown in the figure, the phase for a first order filter will change by 90 degrees per decade increase in frequency. This means that the output will be out of phase by 45 degrees at the upper cutoff frequency. The phase for a second order filter will change by 180 degrees per decade and will be out of phase by 90 degrees at the upper cutoff frequency.

It is the aim of this thesis to design a DAC for audio applications which requires it to have both low harmonic distortion as well as low phase distortion. The higher the order

of filter used, the better the harmonic distortion because it will attenuate the unwanted high order harmonics better. Conversely, the higher the order of the filter, the worse the phase distortion becomes. Since these attributes work in the opposite directions, a second order low-pass filter is a good compromise between the two.

As discussed earlier, a second order filter will have two energy storing components. This is implemented using one inductor and one capacitor and is known as an "LC" low-pass filter. A schematic of an LC low-pass filter is shown below in Figure 4-7.

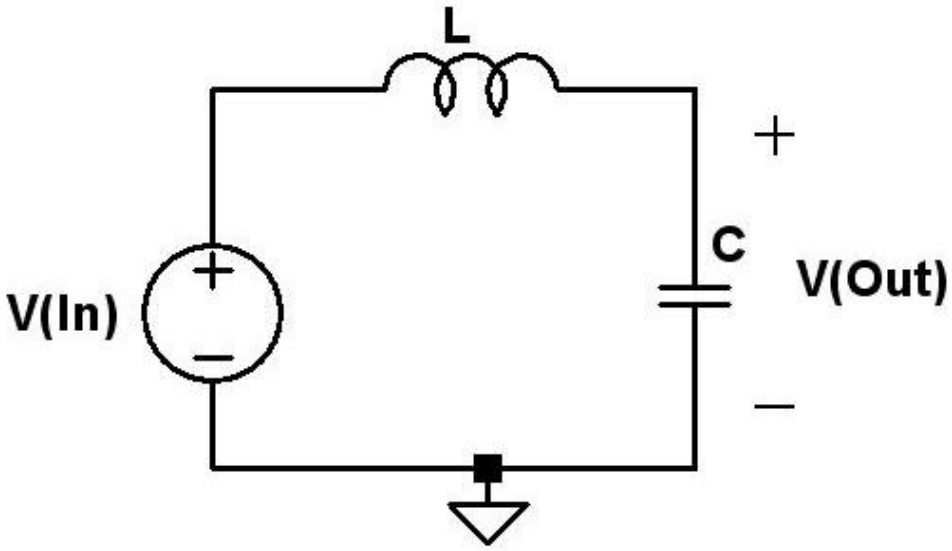


Figure 4-7 LC low-pass filter

To illustrate how the above circuit functions as a low-pass filter it is necessary to convert all the reactive components to their impedances. Impedance is a measure of the amount of resistance in a reactive component and is defined in the complex frequency domain $s=j\omega$. The impedance of an inductor is given in Equation 4-1.

$$Z_L = sL = j\omega L = j2\pi fL$$ Equation 4-1

The impedance of a capacitor is given in Equation 4-2.

$$Z_C = \frac{1}{sC} = \frac{1}{j\omega C} = \frac{1}{j2\pi fC}$$ Equation 4-2

A quick analysis of Equations 4-1 and 4-2, at the two extreme frequency cases f = 0 and f = ∞, shows the equivalent circuits for both components. Table 4-1 shows these relationships.

Component	Frequency	Impedance	Equivalent Circuit
Z_C	0	∞	Open Circuit
Z_C	∞	0	Short Circuit
Z_L	0	0	Short Circuit
Z_L	∞	∞	Open Circuit

Table 4-1 Reactive component equivalent circuits

When the frequency is zero, the inductor becomes a short circuit and the capacitor becomes an open circuit. In this configuration $V_{OUT}=V_{IN}$ and the signal is passed through unchanged. When the frequency is infinite, the inductor becomes an open circuit and the capacitor becomes a short circuit. In this configuration $V_{OUT}=0$ and the signal is completely attenuated. This shows that as the frequency is increased the filter attenuates the signal more and more and thus realizes a low-pass filter.

The exact transfer function for an LC low-pass filter can be derived by applying a simple voltage divider. Once the components are converted to their impedances than they are treated the same as resistors. Following the voltage divider equation, the equation for V_{OUT} with respect to the two impedances is given in Equation 4-3.

$$V_{OUT} = V_{IN}\left(\frac{Z_C}{Z_L + Z_C}\right) \qquad \text{Equation 4-3}$$

The transfer function is defined as the ratio of V_{OUT} divided by V_{IN} and is denoted as H(s) in the complex frequency domain. Substituting Equations 4-1 and 4-2 into 4-3 and dividing by V_{IN} gives the transfer function for the low-pass filter shown in Equation 4-4.

$$TF = H(s) = \frac{V_{OUT}}{V_{IN}} = \frac{\left(\frac{1}{LC}\right)}{s^2 + \left(\frac{1}{LC}\right)} \qquad \text{Equation 4-4}$$

The output of the low-pass filter will be an integrated, and smoothed, power analog signal. This power analog signal will be directly driving a loudspeaker load. As mentioned in Chapter 3, the loudspeaker is modeled as an 8 Ω resistor. When attaching this load resistance across the output terminal of the low-pass filter the schematic shown in Figure 4-8 results.

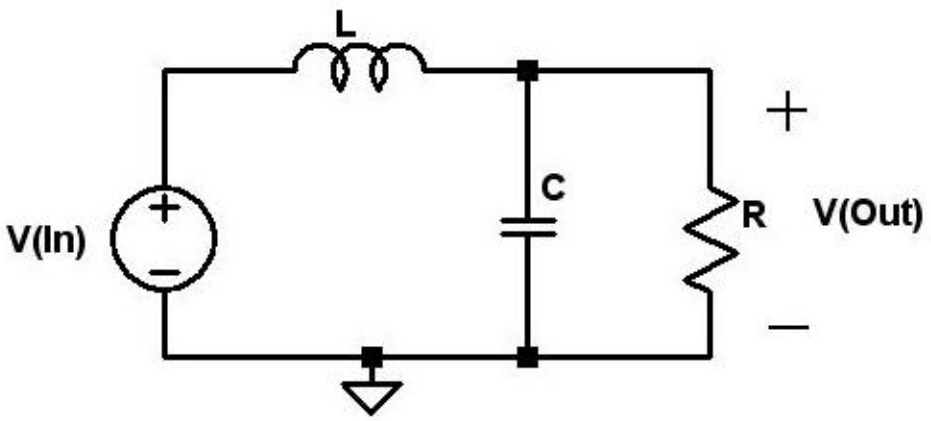


Figure 4-8 Low-pass filter with load

Analyzing the low-pass filter with load requires analyzing the RLC circuit above.

Just as in the case of the LC filter, the first step is to convert each component to its respective impedances. After doing this it is again treated like a simple resistive circuit. The impedance of the capacitor and resistor are combined in parallel and then the voltage divider equation can be used to derive the transfer function shown below in Equation 4-5.

$$H(s) = \frac{\left(\frac{1}{LC}\right)}{s^2 + \left(\frac{1}{RC}\right)s + \left(\frac{1}{LC}\right)} \qquad \text{Equation 4-5}$$

The transfer function derived above is of the same form as the general, second order transfer function shown below.

$$H(s) = \frac{\omega_0^2}{s^2 + 2\zeta\omega_0 s + \omega_0^2}$$ Equation 4-6

In Equation 4-6 the term ω_0 refers to the natural frequency of the circuit and ζ refers to the damping ratio. Another parameter of interest for a second order filter of this nature is the quality factor, Q. The quality factor and damping ratio are related by Equation 4-7.

$$2\zeta = \frac{1}{Q}$$ Equation 4-7

Different second order filter topologies have different filter "Q" values. Certain common designs are named for the engineers that designed them, such as the Bessel filter. Table 4-2 shows the four most common filter types along with their filter "Q" and associated damping factor.

Filter Name	Filter "Q"	Damping ζ
Chebychev	$\frac{1}{\sqrt{1}} = 1.0$	.5
Butterworth	$\frac{1}{\sqrt{2}} = .707$	.707
Bessel	$\frac{1}{\sqrt{3}} = .577$	.866
Linkwitz-Reilly	$\frac{1}{\sqrt{4}} = .5$	1.0

Table 4-2 Second order filter "Q" values

The higher the "Q" value of a filter, the lower the damping factor. This parameter shows how quickly the filter responds near the cutoff frequency. Lower damping changes faster while higher damping responds slower. Low damping causes overshoot or ringing, however, near the cutoff frequency. This overshoot can become very musically displeasing. Figure 4-9 shows the four different filter magnitude responses for a given cutoff frequency.

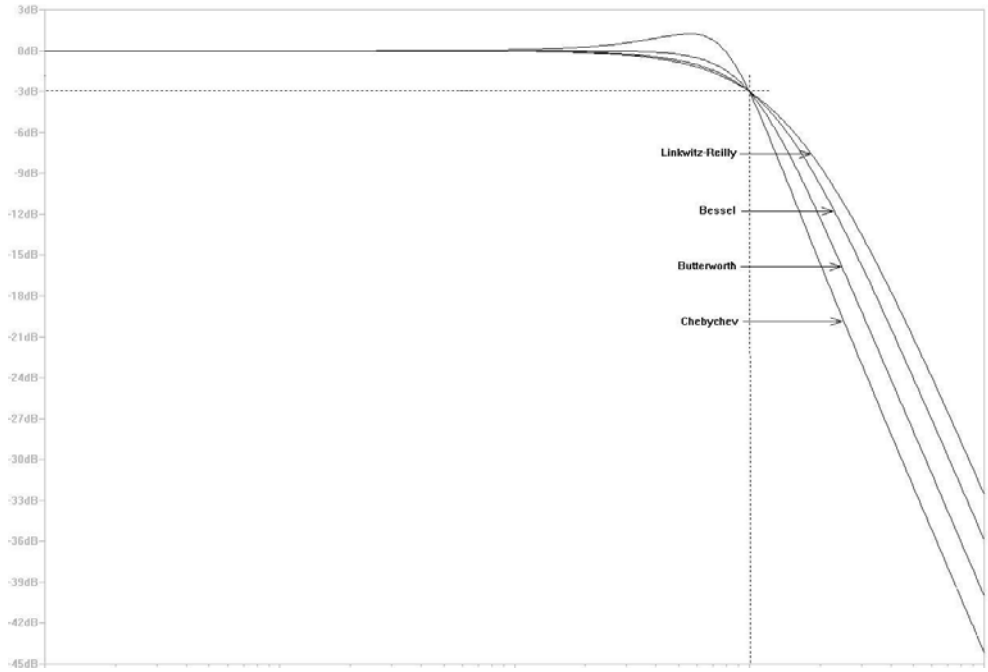


Figure 4-9 Magnitude response for different 2nd order filters

Because of this displeasing musical overshoot, the Chebychev filter can be ruled out as a viable audio low-pass filter. Notice that as the damping is increased, the filter must begin rolling off sooner to achieve the desired cutoff frequency since it changes at a slower rate. This causes frequencies which should be in the upper pass band to get attenuated. Due to this, the high damped Linkwitz-Reilly filter can also be ruled out. Which of the two remaining filter types is best suited for audio is the subject of some debate. The Bessel

filter will have a better phase response while the Butterworth filter will have a better magnitude response. For this thesis the Butterworth low-pass filter was chosen.

Knowing the order of the filter to be used, and the type of filter to be used, design equations can be derived. For this design the resistive load of the speaker is known, as well as the "Q" value and damping ζ for the filter. The general transfer function in Equation 4-6 is in terms of the natural frequency and damping but it is desired to have design equations for a specified cutoff frequency ω_C. Recall that the cutoff frequency occurs when the signal is 3 dB down from the pass band. This corresponds to when the magnitude of the transfer function is equal to $\frac{1}{\sqrt{2}}$. Substituting this into Equation 4-6 and solving for the cutoff frequency gives the cutoff frequency as a function of the natural frequency and damping as shown in Equation 4-8.

$$\omega_C = \omega_0 \sqrt{\sqrt{4\zeta^4 - 4\zeta^2 + 2} - 2\zeta^2 + 1} \qquad \text{Equation 4-8}$$

In order to get the design equations in terms of actual components in the filter, the actual transfer function in Equation 4-5 and the general transfer function in Equation 4-6 can be related together. This results in the two relations shown below in Equations 4-9 and 4-10.

$$\omega_0 = \frac{1}{\sqrt{LC}} \qquad \text{Equation 4-9}$$

$$2\zeta\omega_0 = \frac{1}{RC} \qquad \text{Equation 4-10}$$

Substituting Equation 4-9 into Equation 4-8 gives the following result.

$$\omega_C = \frac{\sqrt{\sqrt{4\zeta^4 - 4\zeta^2 + 2} - 2\zeta^2 + 1}}{\sqrt{LC}} \qquad \text{Equation 4-11}$$

Substituting Equation 4-9 into Equation 4-10 and solving for the $\sqrt{LC}$ term gives the following result.

$$\sqrt{LC} = 2\zeta RC \qquad \text{Equation 4-12}$$

Substituting Equation 4-12 into Equation 4-11 finally gives an equation with only known quantities and the desired value for the capacitance. Solving the equation for C and replacing ω_C by $2\pi f_C$ yields the first design equation shown in Equation 4-13 below.

$$C = \frac{\sqrt{\sqrt{4\zeta^4 - 4\zeta^2 + 2} - 2\zeta^2 + 1}}{4\pi * \zeta * R * f_C} \qquad \text{Equation 4-13}$$

Solving Equation 4-12 for L and substituting Equation 4-13 yields the second, and final, design equation shown in Equation 4-14.

$$L = \frac{\zeta * R\sqrt{\sqrt{4\zeta^4 - 4\zeta^2 + 2} - 2\zeta^2 + 1}}{\pi * f_C} \qquad \text{Equation 4-14}$$

Figure 4-10, shown below, shows an example 16-bit “STAC-DAC” output after the low-pass filter for a 20 kHz signal.

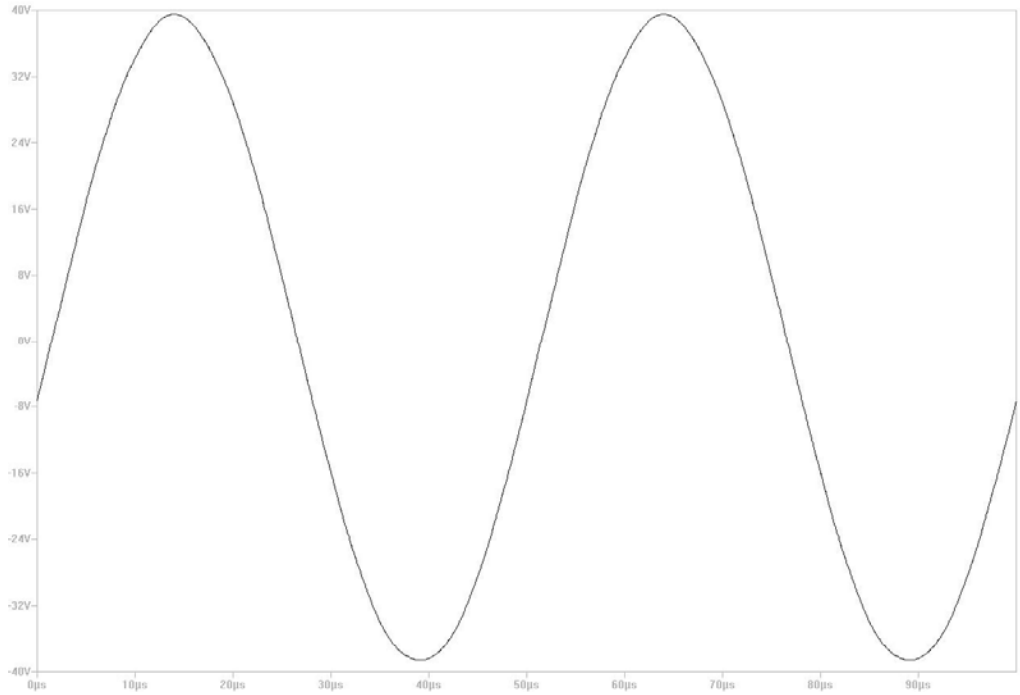


Figure 4-10 Example 16-bit filtered output

4.2 Switching Spike Capacitor

A quick look at the stair-step output of the “STAC-DAC” shows that the circuit contains many switching spikes between each quantized step. Figure 4-11, shown below, is a simulation from LTSpice of the 16-bit stair-step output before the LC low-pass filter.

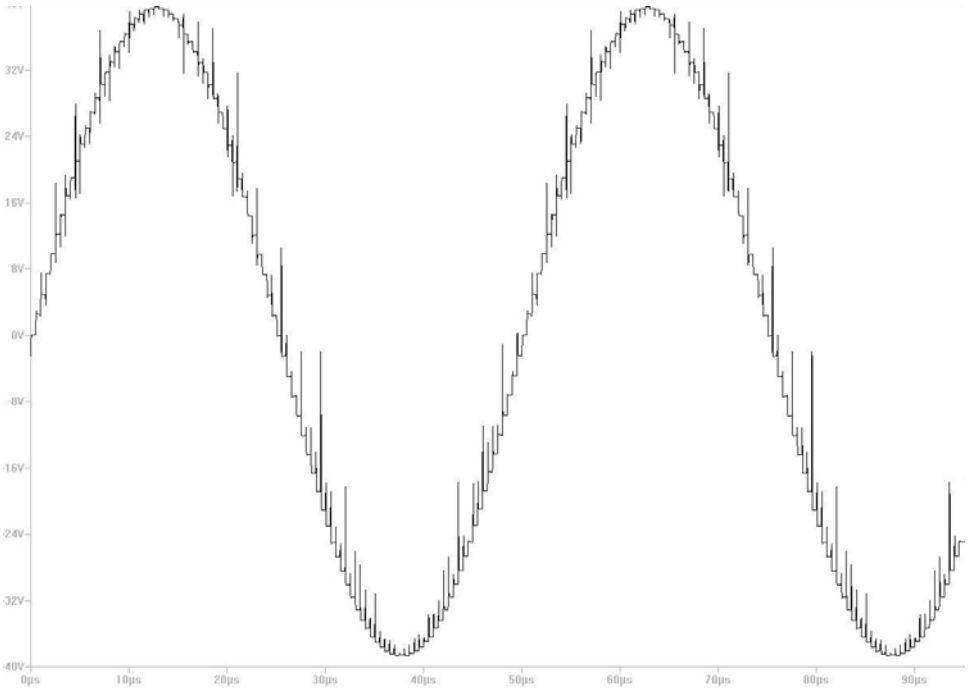


Figure 4-11 16-bit unfiltered stair-step output

Switching spikes in the “STAC-DAC” can be caused by two main things. The first issue is in the turn-on and turn-off times of the transistors. The heart of this problem is that in a digital CMOS circuit, it is assumed that when any single NMOS transistor is “on” or “off” then its partner PMOS transistor will correspondingly be in the opposite state. The problem with this assumption is that, even in the digital realm, all circuit devices are inherently analog. Due to this, there will be a small amount of time when either both transistors are slightly “on” or both transistors are slightly “off”. This error in turn-on and turn-off times results in temporary undesired voltages which can be seen in the form of switching spikes.

The second cause of switching spikes in the “STAC-DAC” is the transistor current runaway caused by the reverse-biased body effect. As discussed in Chapter 3, when the transistor is reverse-biased it will experience body effect. Due to the physical

design of the “STAC-DAC”, the body effect causes the threshold voltage of the transistor to decrease which causes the current to increase. This would continue forever, resulting in current runaway except for the fact that the series circuits forces the output current to level off at the steady-state current desired. Before this steady-state is reached, however, for a short amount of time the current will want to runaway. This brief change in current can be large and will result in a brief, but large change in the output voltage. This is seen as a switching spike on the output.

Removal of the switching spikes does not seem essential for operation of the “STAC-DAC” but will be beneficial for two reasons. The first benefit is increased audio quality and the second benefit is to provide a path to ground for the reverse-biased runaway current. Recall that the low-pass filter acts as an integrator. When integrating a signal with a large switching spike, even if it is over a brief period in time, the integrated signal will change slightly in an attempt to follow that signal. The lower the magnitude of the spike and the shorter the duration, the smaller the integrated output will change. These undesired changes in the output can cause audible harmonic distortion. Removal of this distortion allows for better audio output.

Removal of the switching spikes is accomplished by adding a capacitor at the top of the “STAC-DAC” which is the output to the LC low-pass filter. This switching spike capacitor is tied between the output and ground and therefore needs to be a high voltage, non-polarized capacitor. As discussed earlier, the impedance of a capacitor causes it to act like a short circuit at high-frequencies and an open-circuit near DC. In the stair-step output, each step is a DC value. Since the capacitor acts like an open circuit, for this case, the DC stair-step output will be unchanged. The switching spikes, however, occur only

for a very short amount of time and are therefore at a very high frequency. Since the capacitor acts as a short circuit at high frequencies then these components will get shorted out to ground and will not be passed to the output.

The ability to provide a path to ground for the momentary current runaway is the most important benefit to removing the switching spikes. Without the switching spike capacitor, the stair-step output goes directly into the input of the LC low-pass filter. For high frequencies the inductor acts as an open circuit. Since this is the first component seen, the low-pass filter is essentially disconnected from the "STAC-DAC" output meaning there is no path for this runaway current to flow.

Since the "STAC-DAC" is a series circuit then the total on-resistance is equal to N-bits times the r_{DS} resistance as shown in Chapter 3. This means that the switching capacitor is going to act like a simple low-pass filter when combined with the equivalent resistance of the "STAC-DAC". This simple RC circuit can be used in order to determine a design equation for the switching capacitor. Figure 4-12 shows a graphical representation of this design consideration.

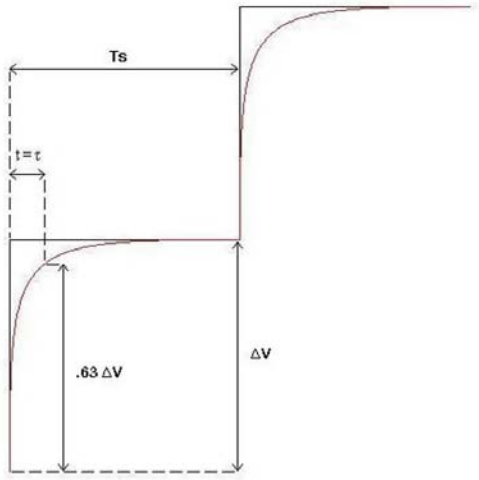


Figure 4-12 Graphical representation for capacitor design

Each stair-step output coming out of the DAC is equivalent to a step input to the RC circuit. Knowing this, it can be seen that the output voltage will act just like the voltage for a charging capacitor. The equation for this is given in Equation 4-15.

$$v(t) = \Delta V(1 - e^{\frac{-t}{\tau}}) \qquad \text{Equation 4-15}$$

Using Equation 4-15, the 63% rule can be applied. This states that, for a charging capacitor, if t is set equal to the time constant τ, then the voltage will have risen to 63% of the total ΔV. Notice that the actual value of ΔV does not change the design equation at all. Whether the stair-step is a very tiny change from only the LSB changing or a very large change from all 0's to all 1's, the output will still rise to 63% of whatever that change in voltage corresponds to in one time constant. It is next needed to know how soon the capacitor will allow the voltage to rise to this 63% value with respect to T_S. This was arbitrarily determined to happen in $T_S/10$ or $.1*T_S$. Based on the 63% rule, this means that $.1*T_S$ should equal the time constant. For an RC circuit, the time constant τ is equal to $R_{eq}*C$. The quantity $.1*T_S$ is equivalent to $.1/f_S$. Substituting these and solving for C yields the final design equation for the switching capacitor shown below.

$$C_S = \frac{.1}{f_S * R_{eq}} = \frac{.1}{f_S * N * r_{DS}} \qquad \text{Equation 4-16}$$

Figure 4-13 shows an example “STAC-DAC” output with the switching spike capacitor before the “LC” low-pass filter.

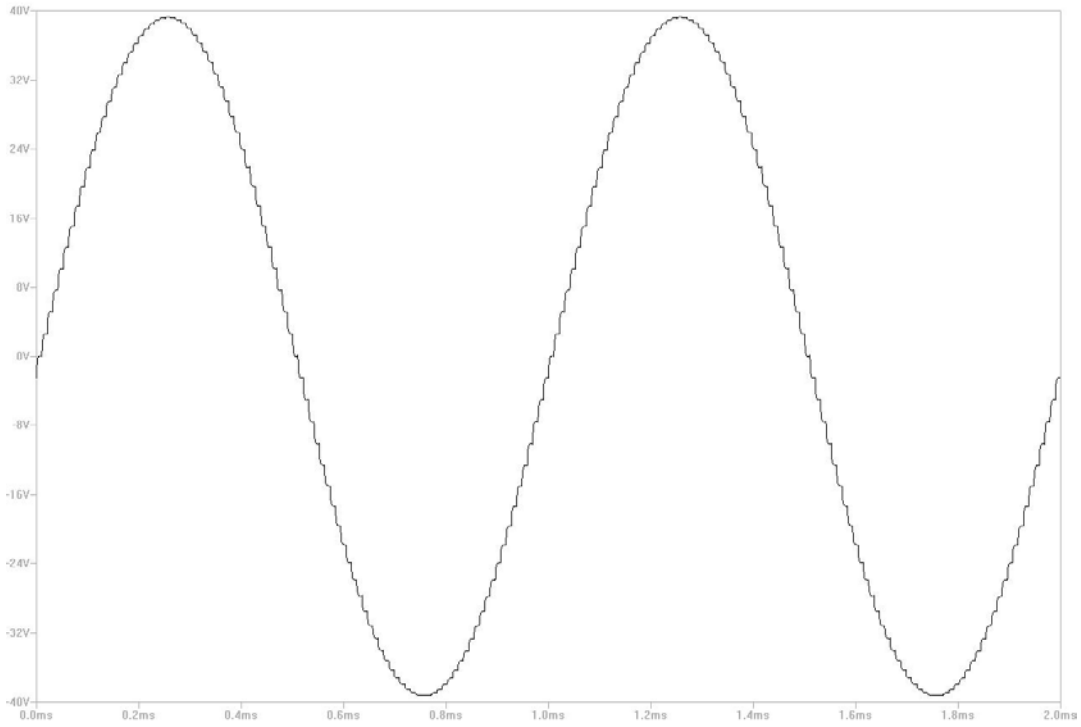


Figure 4-13 “STAC-DAC” output with switching spike capacitor

As can be seen by this figure, the switching spike capacitor does a good job of removing the switching spikes as designed. It allows a current path to ground for the current runaway transistors and will increase the audio quality.

The reduction of harmonic distortion and therefore increase in audio quality is physically accomplished by more greatly filtering out the high frequency switching noise with the addition of the first order RC pole located at the following frequency.

$$f_{Cs} = \frac{1}{2\pi * N * r_{DS} * C_S} \qquad \text{Equation 4-17}$$

A circuit showing the equivalent resistance of the "STAC-DAC" along with the switching spike capacitor and the low-pass filter with load is shown below.

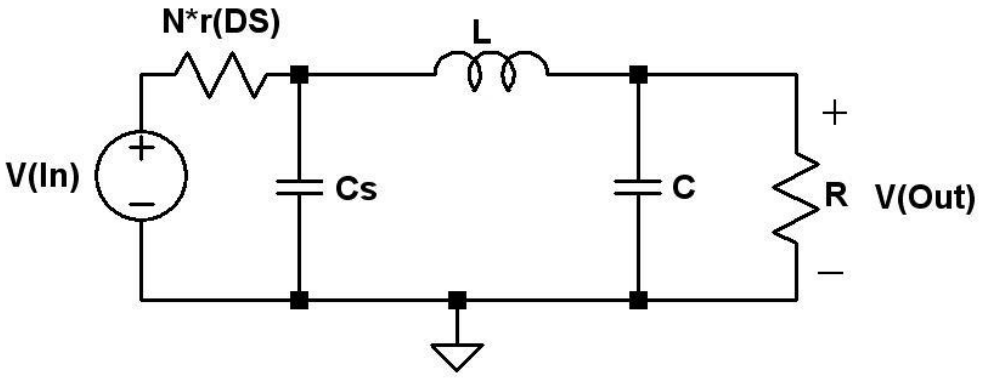


Figure 4-14 Low-pass filter with Cs

The magnitude Bode plot of the system with and without the switching spike capacitor C_S is shown in Figure 4-15.

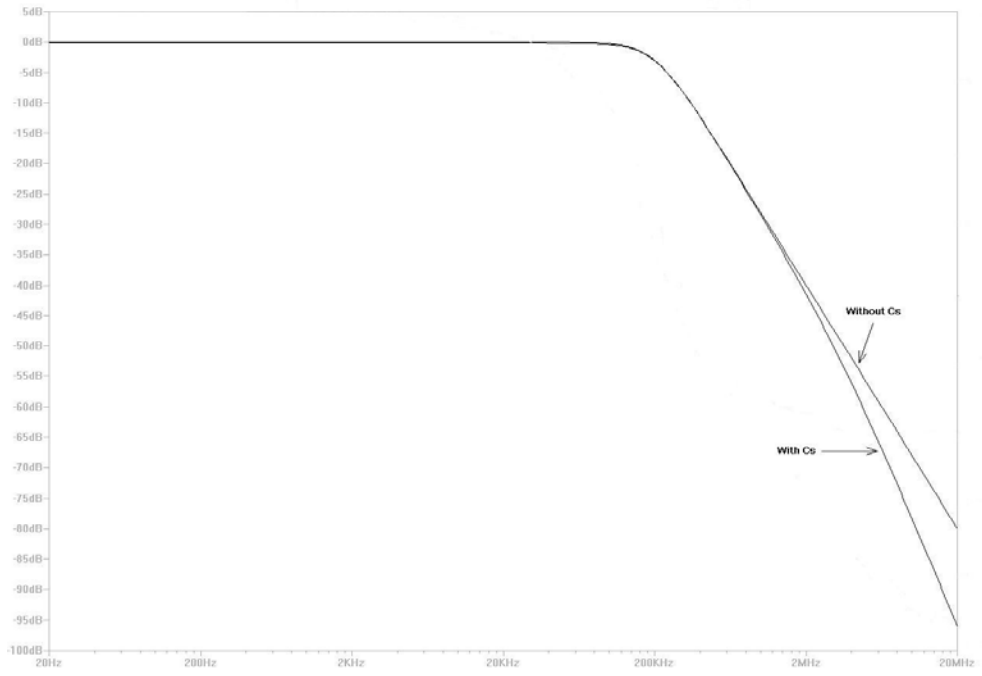


Figure 4-15 Magnitude Bode plots with and without C_S

4.3 Volume Control

In order for the "STAC-DAC" to act as an audio amplifier it must provide a means of volume control. This volume control should be an interface to the outside world that the listener can directly control for desired listening levels. In physical terms, the volume of a sound is defined by its sound pressure level, or SPL. Changing the SPL requires changing the air pressure. This is accomplished by the amount of excursion, or movement, in the loudspeaker. To change the amount of movement in a loudspeaker requires changing the amount of current driving that speaker. For a purely resistive load, changing the current corresponds to changing the output voltage. This outside user control is provided by a volume knob. In most audio amplifiers, turning this knob corresponds to changing the wiper position in a resistive potentiometer.

The volume potentiometer will act like two separate resistors, shown as R1 and R2 in the following figure. The sum of resistances R1 and R2 equals the total resistance of the potentiometer. As the position of the wiper changes, by turning the volume knob, the ratio of resistances between R1 and R2 will change. The load resistance is in parallel with R2 which causes the output voltage to be equivalent across the two. By varying the resistance R2 by use of the volume potentiometer, the output voltage and therefore output volume can be regulated. Figure 4-16 shows this typical implementation.

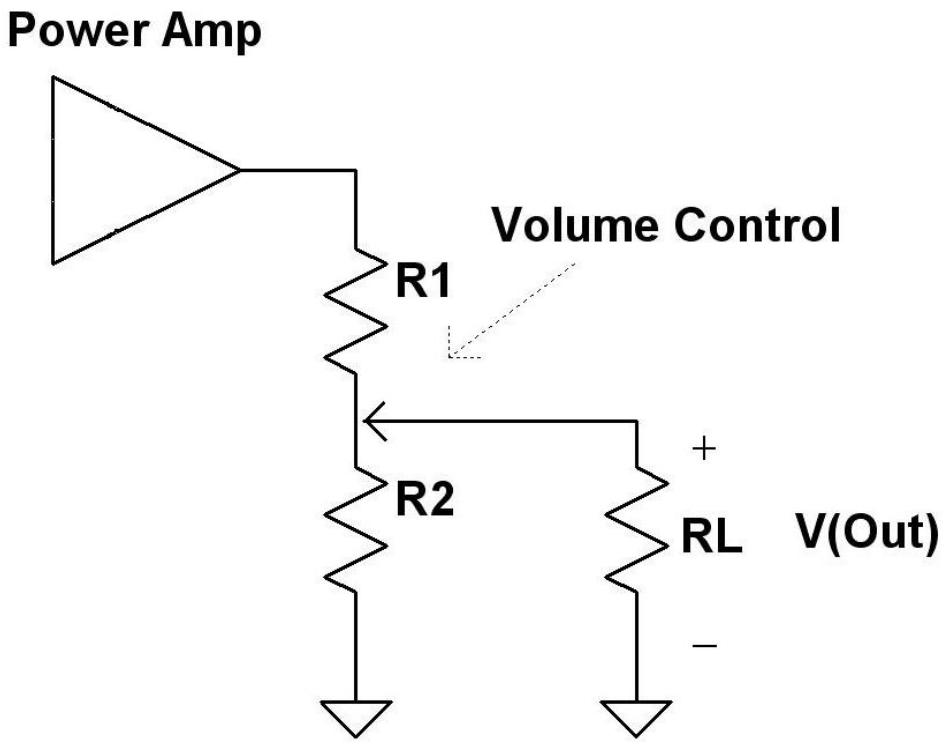


Figure 4-16 Typical Volume Control

As it turns out, this type of volume control is not an acceptable design strategy for the "STAC-DAC" for two reasons. The first reason deals with the value of the output load seen by the low-pass filter. In the above configuration, the equivalent resistive load seen by the low-pass filter is shown in Equation 4-18.

$$R_{eq} = R1 + R2 \parallel R_L \qquad \text{Equation 4-18}$$

For low load resistances, as is the case with a loudspeaker, it can be seen that $R2 \| R_L \approx R_L$. The volume potentiometer could have a total resistance on the order of 500 Ω. From Equation 4-18, this implies that $Req \approx R1 + R_L \approx R1$. This is a very detrimental affect from an audio standpoint. When the listener has the maximum volume output selected,

R1 will be at a minimum. In this case Req ≈ R_L and the cutoff frequency of the low-pass filter will be as expected. When the listener turns the volume down, however, the value of R1 increases causing Req to increase correspondingly. This increased Req will cause the cutoff frequency of the low-pass filter to drop radically. A variable cutoff frequency based upon listening levels is certainly not a desirable attribute. The amount in which the cutoff frequency will vary will be the ratio of the potentiometer resistance to the speaker load resistance as shown in Equation 4-19.

$$\Delta f_{C(MAX)} = \frac{R_{pot}}{R_L} \qquad \text{Equation 4-19}$$

For the case of a 10 kΩ potentiometer and an 8 Ω speaker, this means the cutoff frequency can be reduced by a factor of 1250!

The second issue that arises with this type of volume control deals with efficiency. The theoretical efficiency of the "STAC-DAC" was derived in Chapter 3 and can be expressed as the efficiency of a voltage divider between the series resistance of the DAC and the load resistance. When the volume potentiometer is added however, the equivalent output resistance becomes R1+R_L ≈ R_{pot} + R_L as shown in Figure 4-17.

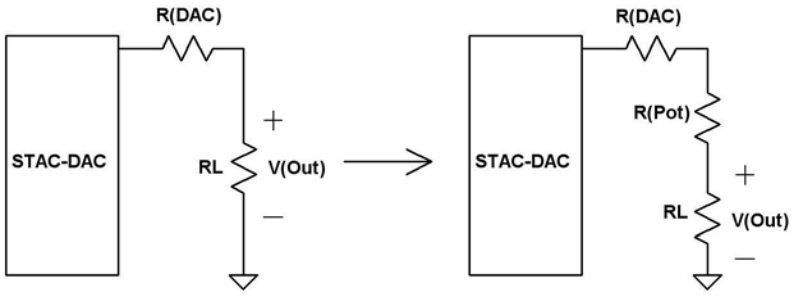


Figure 4-17 Equivalent output load with volume potentiometer

Due to this, the efficiency would drop to the value shown in Equation 4-20.

$$\eta = \frac{R_L}{R_{DAC} + R_{pot} + R_L}$$ Equation 4-20

The issues of reduced efficiency and variable cutoff frequency could be alleviated in two possible ways for this type of volume control. The first option would be to use a potentiometer with an extremely low resistance, even lower than the resistance of the loudspeaker. If this is possible then the equivalent resistance seen by the low-pass filter can be approximated as simply R_L and therefore the cutoff frequency will not vary. Also, if the potentiometer resistance is held very small then Equation 4-20 shows that it will have only a negligible effect on the efficiency of the system. This would require a potentiometer value on the order of 1 Ω or less, which is most certainly not a readily available part. Not to mention this low impedance path would allow more current to flow through it than the loudspeaker load by application of the current divider.

A second option would be to decrease the equivalent resistance of the volume potentiometer by stringing multiple instances together in parallel. Doing this would require connecting the output of each wiper to the loudspeaker. The equivalent resistance of any number "n" potentiometers in parallel is shown in Equation 4-21.

$$R_{pot(eq)} = \frac{R_{pot}}{n}$$ Equation 4-21

A volume control in this configuration would allow the equivalent resistance of the potentiometer to be reduced. This implementation is not realistic, however, as it would

take a very large amount of potentiometers in parallel to reduce the resistance to an acceptable level. For example, if it is a 1 kΩ potentiometer, then 125 of them would have to be connected in parallel just to get the equivalent resistance down to 8 Ω and even more would be required to get this figure lower.

Due to these detrimental implications of a general volume control, another way to control the volume is needed for the "STAC-DAC". A control system can not be placed before the "STAC-DAC" as this information is just parallel bits of digital information. The volume control can not be placed after the "STAC-DAC" because of the aforementioned effects. This means that the volume control must be incorporated within the DAC itself. This is accomplished by simply allowing the isolated voltage supplies to be variable.

The voltage supplies for the "STAC-DAC" should be designed following the equation derived in Chapter 3. In using this equation, the power output should correspond to the maximum power desired for the system. This means that the voltage supplies will be designed to output their max voltages to correspond to this maximum power. If a lower listening volume is desired than the output voltage and power are decreased by each of the voltage supplies decreasing in value. This means that the user interface must be tied directly to each voltage supply in the DAC so that they are all scaled accordingly.

Equation 4-22 reiterates the equation derived in Chapter 3 describing the relationship between each voltage supply and the output power.

$$V(N,x,P)_{MAX} = \frac{2 * \sqrt{2R_L P_{MAX}} * 2^x}{2^N - 1} \qquad \text{Equation 4-22}$$

Based on this relationship it can be seen that in order to maintain a linear power output, each voltage supply needs to vary based upon the square root of the output power. This criterion would be hard to meet and is actually not a necessity. The output voltage can change linearly with respect to a change on the volume control knob. This allows the voltage supplies to change linearly as well. A linear change in voltage will correspond to a squared output power. Therefore, for every turn a listener makes on the volume knob, the output power will increase by the amount of change squared as shown in Figure 4-18.

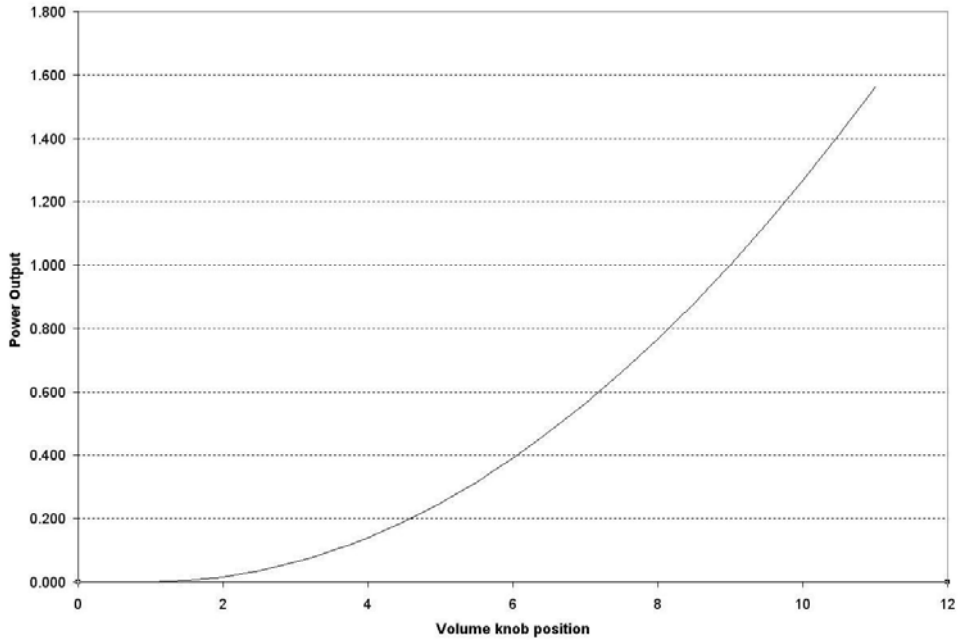


Figure 4-18 Power versus volume position

Recall that the actual volume of a sound was shown to be proportional to the voltage of a signal, for a purely resistive loudspeaker, and not the power. Due to this, a linear changing voltage output should correspond well to a linear changing output volume. This linear relationship is shown in Figure 4-19.

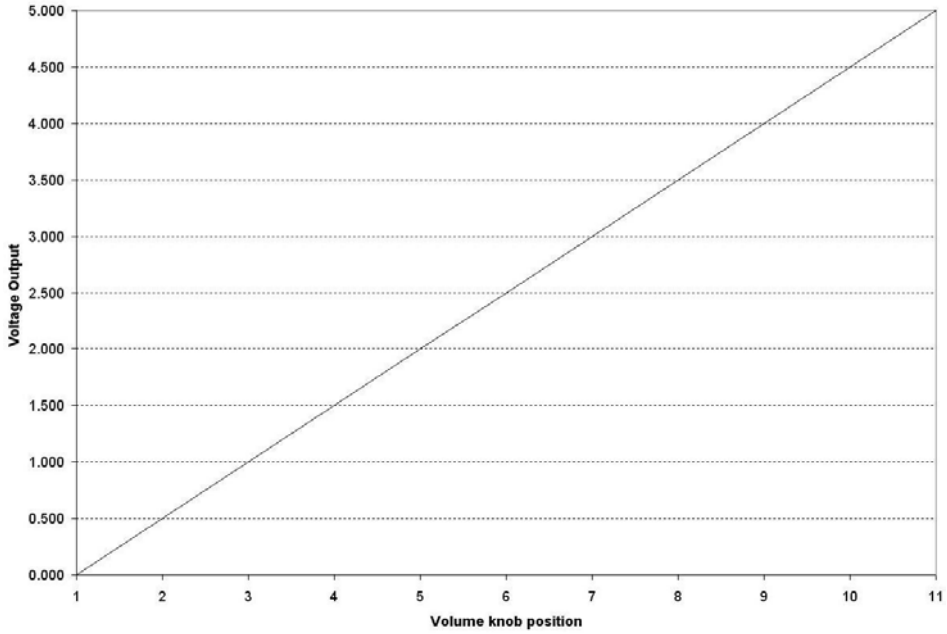


Figure 4-19 Voltage versus volume position

Also, the volume control is a user controlled interface. Because of this, it does not necessarily have to exhibit a perfectly linear relationship to be effective. If one turn does not raise, or lower, the output volume sufficiently, the listener can simply adjust the knob further until the desired volume is reached.

Designing the linear volume control for the "STAC-DAC" in this fashion has two requirements. The first is that not only does each voltage supply in the "STAC" have to change when the volume knob is changed, but so too does the negative reference voltage at the bottom of the entire stack. If this voltage does not change accordingly, the output waveform will no longer be centered on earth ground and could, in fact, be entirely negative which would permanently damage the loudspeaker. The second requirement is that each incremental change on the volume knob must correspond to a certain percentage change for each voltage supply. If this is not true then the linear relationship

breaks down. Figure 4-20 shows a partial example of this volume control implementation within the full “STAC-DAC”.

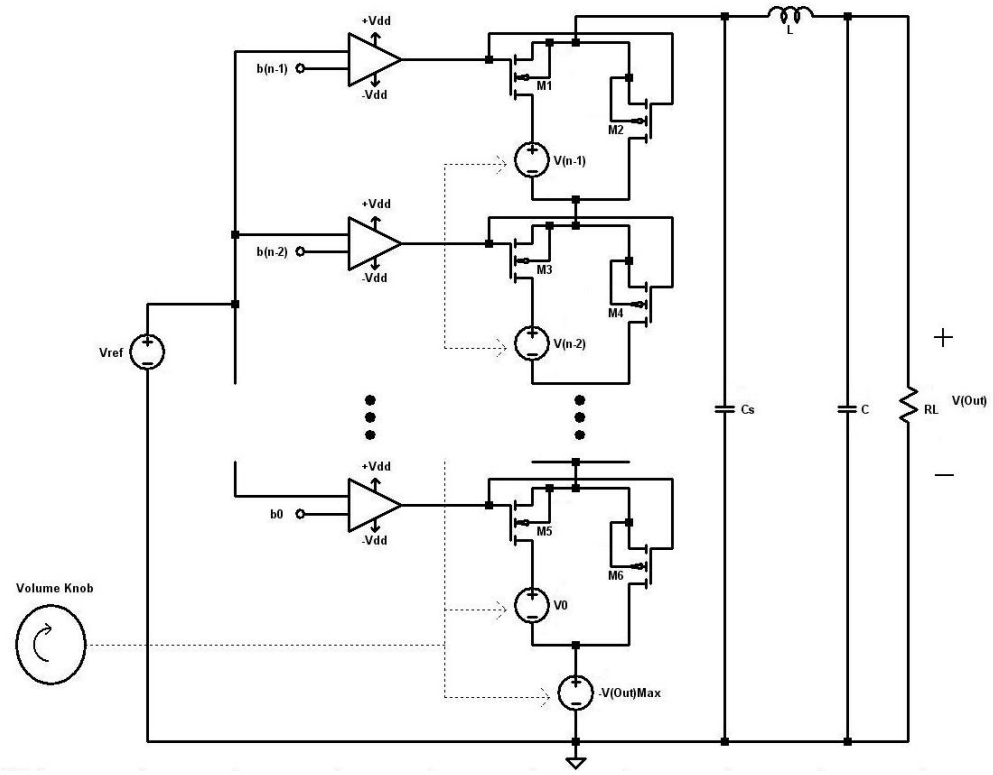


Figure 4-20 Volume Control Implementation

To illustrate this further, consider the case of a 4-bit, 1.5625-Watt “STAC-DAC” with a 10% volume change resolution. Table 4-3 shows the corresponding maximum supply voltages for all 4 supplies plus the negative reference supply and also shows the incremental change needed for each supply.

Voltage Source	Max Voltage	ΔV increment
V3	5.333333 V	.533333 V
V2	2.666667 V	.266667 V
V1	1.333333 V	.133333 V
V0	.666667 V	.066667 V
-Vdd	-5 V	.5 V

Table 4-3 Example showing incremental volume resolution

Notice that this makes the volume control no longer a continuous, linear process but instead a quantized process based on the volume change resolution which is dependent on two things. The first factor in the volume resolution is how many incremental steps are desired on the volume knob. A 10% resolution would correspond to having 11 possible volume increments ranging from 0% to 100% while a 1% resolution would correspond to 101 possible volume increments. The second factor in determining the volume resolution lies in the resolution capabilities of the voltage supplies. As the maximum voltage for each supply decreases, then the incremental percentage change also decreases, requiring more precision. There will reach a point where the power supplies are not capable of the required precision. Implementing the volume control in this fashion is a feasible solution.

5. "STAC-DAC" SIMULATION AND OPTIMIZATION

5.1 Design Verification

It was the goal of this thesis to design and verify the operation of the power "STAC-DAC" in order to directly drive a loudspeaker load from logic level digital inputs. Since this is a brand new design topology, only the back-end power "STAC-DAC" portion of the audio system was explored. Figure 5-1 shows the very top-level block diagram of the stereo audio amplifier.

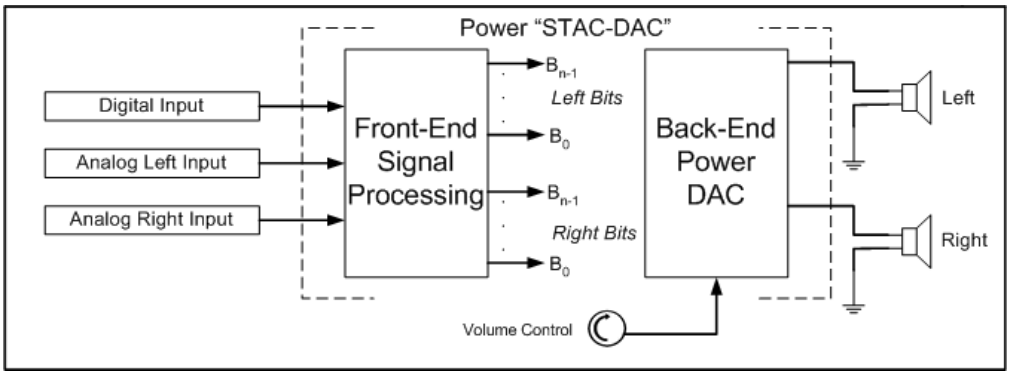


Figure 5-1 Top level block diagram for Power "STAC-DAC"

The input to the simulated system was assumed to be a single channel analog signal. Because of this, the audio channel interleaving and demultiplexing are neglected. The front-end signal processing is assumed to be already present at the input of the back-end design. The verification of this design is realized via simulation from MATLAB and LTSpice. The analog input signal was converted to digital format by use of an analog-to-

digital converter implemented in MATLAB. This code can be seen in its entirety in Appendix A. The MATLAB digital output was then used as the input to the "STAC-DAC" design implemented in LTSpice. Figure 5-2 shows the block diagram of the design verified in this thesis.

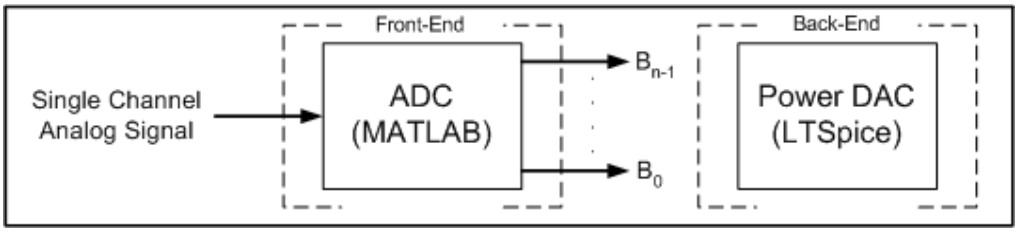


Figure 5-2 Block diagram of thesis implementation

The first step of the simulation was to prove that the "STAC-DAC" functioned properly for a given number of digital input bits. This was accomplished by starting with the 4-bit circuit shown below in LTSpice.

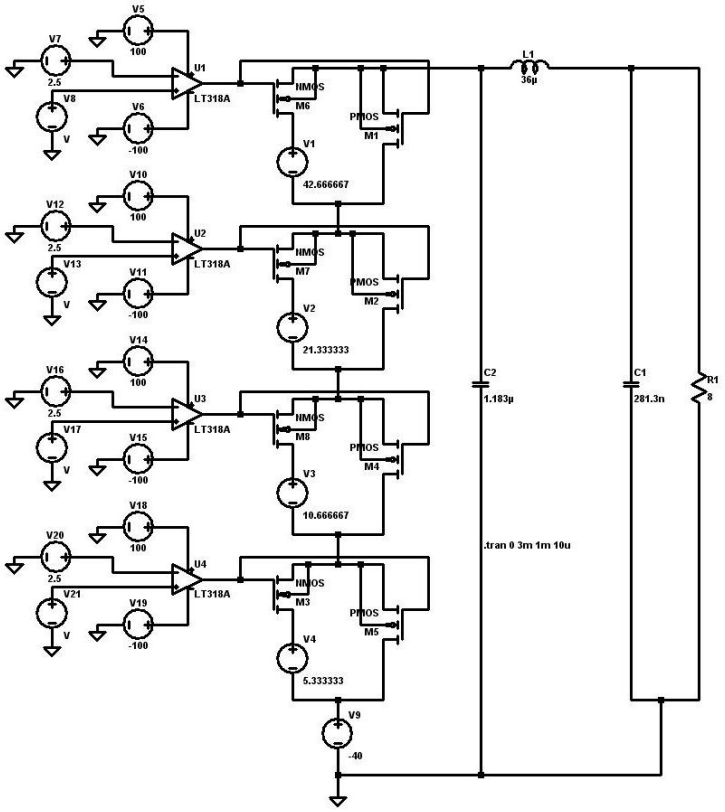


Figure 5-3 4-bit simulation circuit

For this simulation, the output power was designed to be 100 watts across the 8 Ω load. The sampling frequency was set to 96 kHz and the cutoff frequency of the low-pass filter was set to 50 kHz. The input signal was set to a frequency of 1 kHz. Figure 5-4 shows the filtered 1 kHz output voltage across the resistive loudspeaker load.

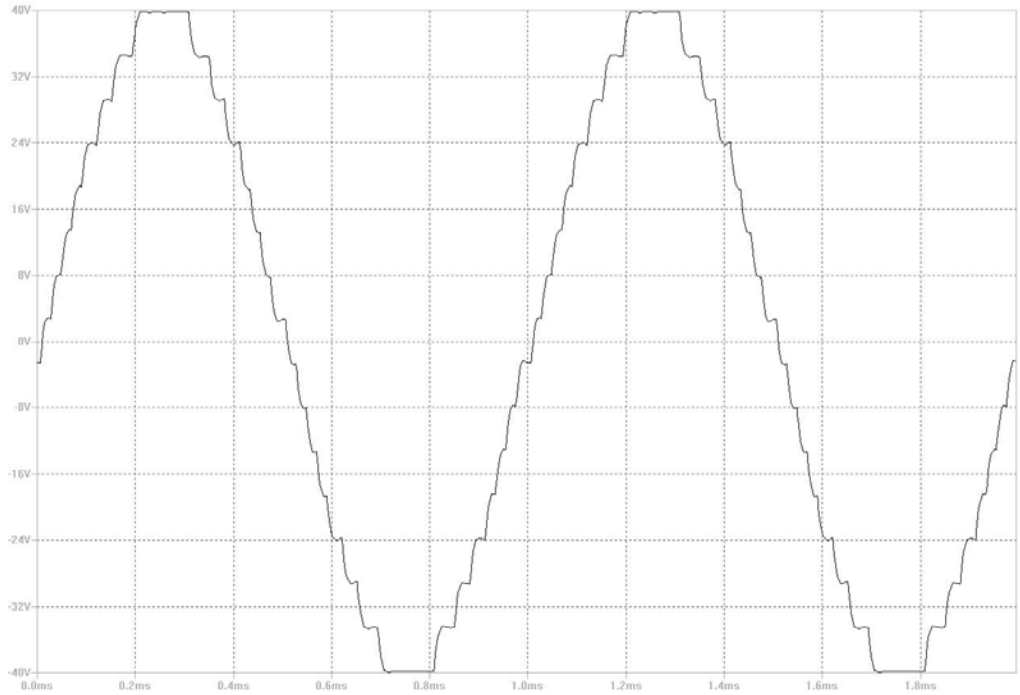


Figure 5-4 4-bit 1 kHz output

This simulation verifies that the 4-bit "STAC-DAC" circuit functions as expected with the full 100-watt output seen. Notice that even with the low-pass filter, the output is still not perfectly smooth. This is because the resolution for a 4-bit circuit is so low that each state change is very large. This could have been corrected by using a lower cutoff frequency.

Seeing that the full circuit functioned properly, it is desired to see the voltage and current waveforms for a single transistor within the series circuit of the "STAC-DAC". Figure 5-5 shows the voltage V_{DS} across the NMOS transistor for the second most significant bit stack.

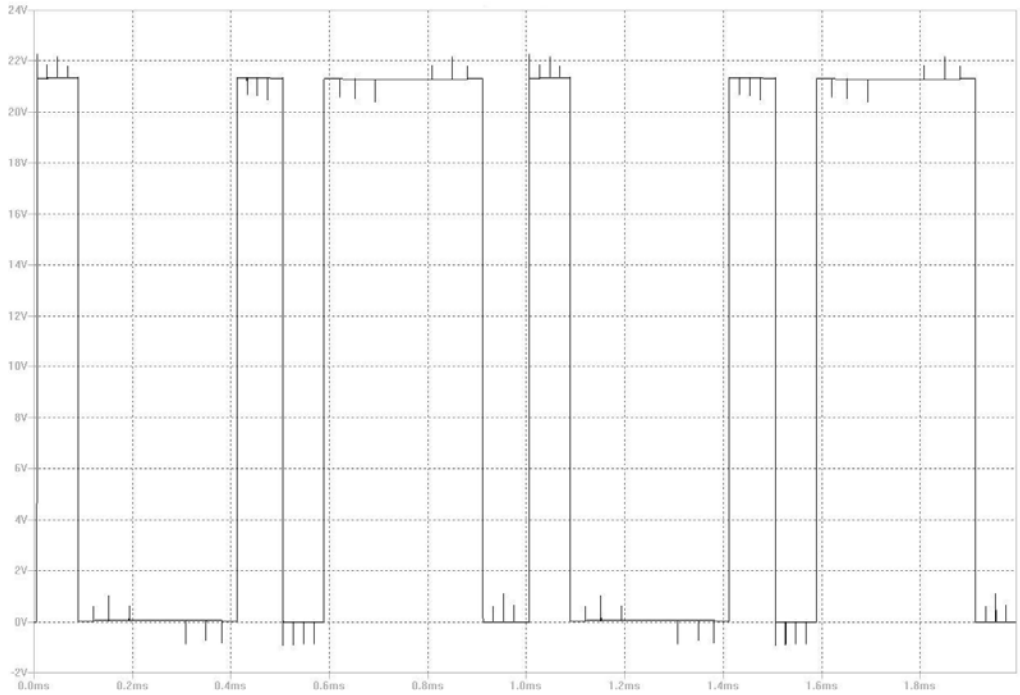


Figure 5-5 V_{DS} across single transistor

As can be seen from this waveform, when the transistor is "on" the voltage across it is approximately zero, while when it is "off" the voltage dropped across each transistor is equal to the supply voltage for that individual "STAC". In this case, that voltage was 21.333 volts. Zooming in on one of the sections where the transistor is conducting will reveal the voltage drop V_{DS} across the transistor due to the dynamic resistance r_{DS}. Figure 5-6 shows this voltage waveform.

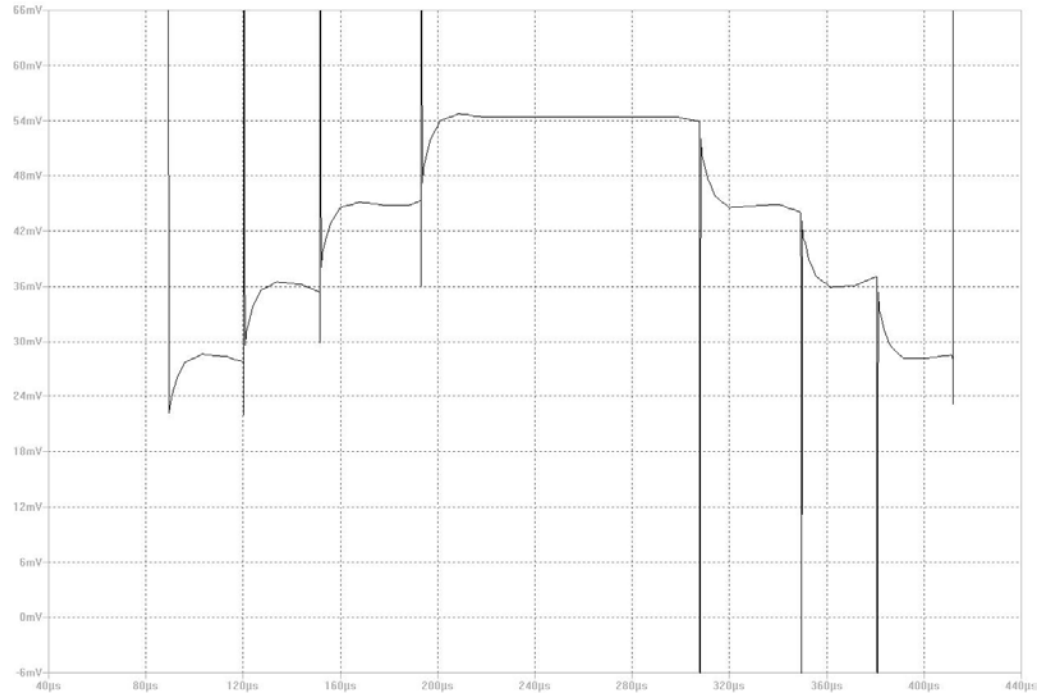


Figure 5-6 V_{DS} voltage during "on" state

Notice that this voltage varies as the DAC changes states because the current through the transistor changes. This is a very small voltage, ranging from 25 mV to 55 mV for this case and corresponds to a low "on" resistance as desired. The current through the same transistor is shown in Figure 5-7 below.

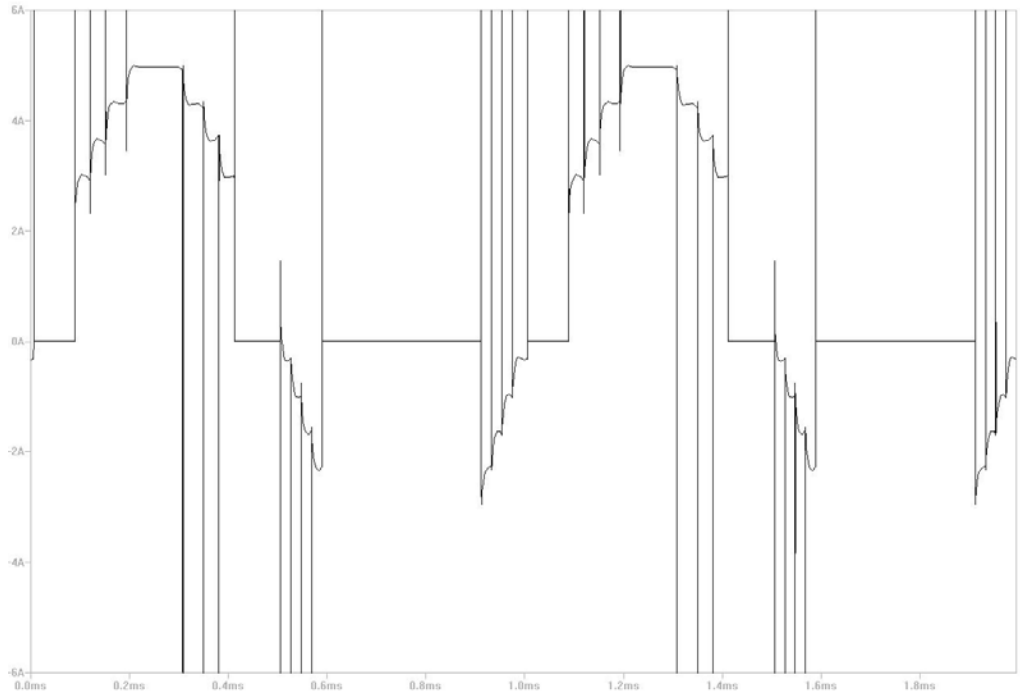


Figure 5-7 Current waveform for a single transistor in 4-bit design

This figure shows the incremental changing current and also verifies the functionality in the reverse-biased regions where the current is negative. It should be noticed that, while very short in duration, the current switching spikes are fairly severe. At the worst case scenario, the switching spikes reached a value of 100 amps but lasted for only 1.5 ns.

With the 4-bit design validated, the full 16-bit design was implemented in LTSpice. The design parameters were kept the same as for the 4-bit design. Figure 5-8 shows the 16-bit filtered output at 100 watts and 1 kHz.

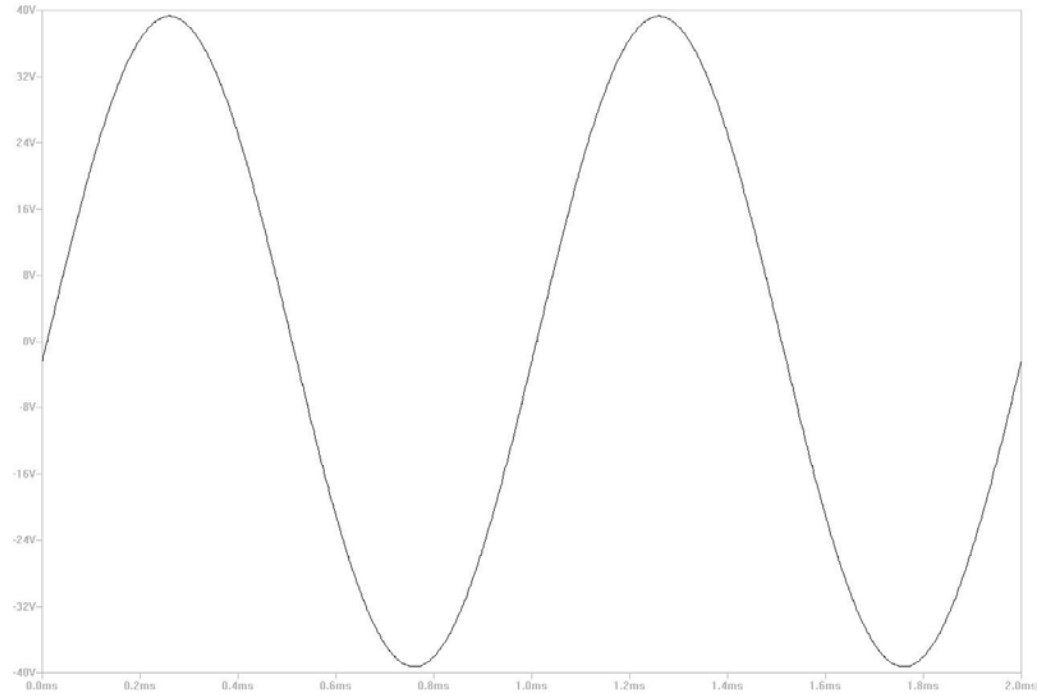


Figure 5-8 16-bit 1 kHz output

This simulation verifies that the 16-bit "STAC-DAC" circuit also functions as expected. Notice that with the increased bits of resolution, the sine wave output is much smoother and less distorted. The voltage waveform for the 16-bit simulation looked virtually identical to that of the 4-bit simulation with V_{DS} ranging from millivolts when conducting to the corresponding voltage supply voltage when off. The current waveform, again for the second most significant bit is shown in Figure 5-9.

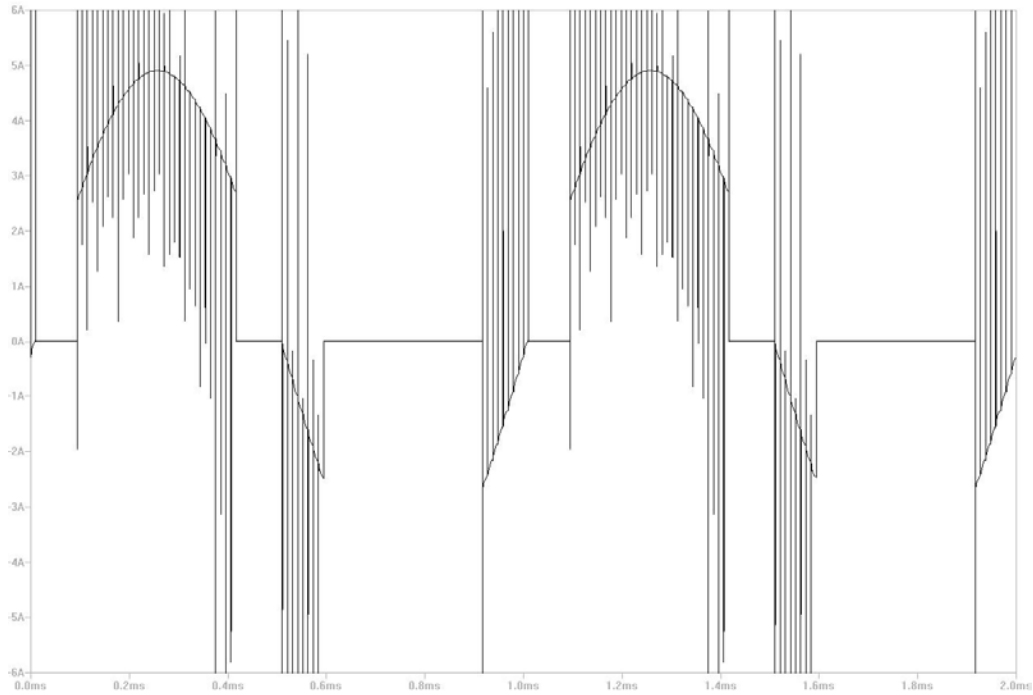


Figure 5-9 Current waveform for a single transistor in 16-bit design

As can be seen from this figure, the current still operates in both directions and the current spikes are still present. The worst case spike for the 16-bit simulation was 70 amps and lasted 1.2 ns. This simulation also shows how the current through each transistor, when conducting, is equal to the output current due to the "STAC-DAC" being a series circuit. Since the load is purely resistive, this current mimics the sinusoidal output voltage except in a piece-wise fashion since it is only "on" during certain digital states.

5.2 Design Optimization

Once the 16-bit "STAC-DAC" design had been verified to function, it was desired to adjust all of the possible design parameters in order to achieve an optimal final design. In order to decide upon an optimal design, the figures of merit used to analyze the

design need to be known. Since the "STAC-DAC" is designed to directly drive a loudspeaker it needs to be a high power output device. The power output decided upon for this thesis was 100 watts into an 8 Ω load, in a non-bridged manner. Another figure of merit for a high power device is consequently the efficiency of the design. The efficiency of this system is desired to be above 90%.

Another design consideration is the fact that the "STAC-DAC" needs to be able to accurately reproduce musical signals. One figure of merit to determine this ability is the total harmonic distortion, or THD, of the system. The THD of an amplifier is a measure of the non-linear distortion which the system adds to the signal. This non-linear distortion will be present in the form of harmonics. The THD measurement is defined as the ratio of the power of the harmonics divided by the power of the fundamental frequency. The full equation for THD is shown in Equation 5-1.

$$THD = \frac{\sqrt{P_{f2}^2 + P_{f3}^2 + \ldots + P_{fn}^2}}{P_1} = \frac{\sqrt{V_{f2}^2 + V_{f3}^2 + \ldots + V_{fn}^2}}{V_1} * 100\% \qquad \text{Equation 5-1}$$

In the above equation, V_{f1} corresponds to the voltage of the fundamental frequency; V_{f2} corresponds to the voltage of the second harmonic and so on up to any number of n harmonics. In order to calculate the THD of the system, the output waveform must be converted to its frequency components by use of the Fourier Transform. LTSpice has the ability to perform a Fast Fourier Transform, or FFT, on any signal and will therefore be used for this calculation. Also built into LTSpice is the ability to directly calculate the THD of the system. When the FFT of the signal is taken, the THD number is output. For a high-fidelity audio system, the THD should be limited to a fraction of a percent.

Not only must the system have minimal non-linear harmonic distortion but for audio quality the phase distortion must be minimized as well. If the phase distortion is not minimized, stereophonic quality is sacrificed as the directionality of the sound will become “blurred”. For high-fidelity audio systems the phase distortion over the entire audible frequency range should be lower than the minimum amount of phase detectable by the human ear. This minimum detectable amount of phase is approximately 5 degrees of phase shift.

A final design consideration is the maximum operating frequency of the system. This figure can be shown by the Full Power Bandwidth, or FPBW. The FPBW is related to the slew-rate of the device by Equation 5-2.

$$FPBW = \frac{SR_{\max}}{2\pi * V_{OUT(MAX)}} \qquad \text{Equation 5-2}$$

The slew-rate, or SR, as shown above is defined by Equation 5-3.

$$SR_{\max} = \left(\frac{dV_{OUT}}{dt} \right)_{MAX} \qquad \text{Equation 5-3}$$

The FPBW figure will show the maximum frequency where the full desired power is still delivered to the load, unchanged. In order to output the full desired power to the loudspeaker in an undistorted manner, this frequency must be above the maximum audible frequency of 20 kHz.

The five figures of merit discussed above were the five values that were used to determine the optimum design, and therefore the full capabilities of the power "STAC-DAC" design. The parameters that were available to be optimized in the design included: transistor sizes, the ratio of PMOS/NMOS transistor sizes, the voltage supplied to the transistor gate terminals, the sampling frequency and the low-pass filter cutoff frequency. Also investigated were the distortion effects of the switching spike capacitor, the distortion effects associated with the variable volume control and the advantages of the 16-bit design.

The first step in the design process was to account for the desired power output. The design called for 100 watts of power to be delivered into an 8 Ω load with 16-bits. In order to supply the required amount of power, the 16 individual power supplies and negative reference voltages were designed using Equation 3-22 and Equation 3-20 respectively. Table 5-1 shows these voltages.

Voltage Source	Value	Voltage Source	Value
V_{15}	40.000610 V	V_6	0.078126 V
V_{14}	20.000305 V	V_5	0.039063 V
V_{13}	10.000153 V	V_4	0.019532 V
V_{12}	5.000076 V	V_3	0.009766 V
V_{11}	2.500038 V	V_2	0.004883 V
V_{10}	1.250019 V	V_1	0.002441 V
V_9	0.625010 V	V_0	0.001221 V
V_8	0.312505 V	$-V_{MAX}$	-40 V
V_7	0.156252 V		

Table 5-1 Voltage supply values for 100 watt output with 16 bits

The first parameter that was varied for this design was the sizing of the transistors. The 100-watt output required a maximum output current of 5 amps. Recall that there are three possible ways to achieve this large current drive. Those ways consist

of having a large transistor transconductance, having large transistor widths or having a large gate voltage. For this implementation a .18 μm transistor technology was utilized for all transistor lengths. The transconductace of the transistor model supplied by LTSpice was given as $20\frac{\mu A}{V^2}$ for an NMOS device and $10\frac{\mu A}{V^2}$ for a PMOS device. These numbers could have been changed to a larger number by changing the transistor models but was deemed reasonable for the small-size transistor technology used. Since the transconductance of the transistors modeled was a low number this meant that the transistor sizes needed to be very large and that the gate voltage needed to be very high in order to achieve the needed current output.

For the first set of simulations, the same sizes were used for both the NMOS and PMOS transistors. The analog input signal was set to a frequency of 1 kHz while the sampling frequency was set to 96 kHz and the cutoff frequency was set to 50 kHz. The voltage on the gates, supplied from the gate drive circuit, was set to +/- 100 volts. Figure 5-10 shows a plot of the THD, measured in LTSpice, versus the transistor sizes.

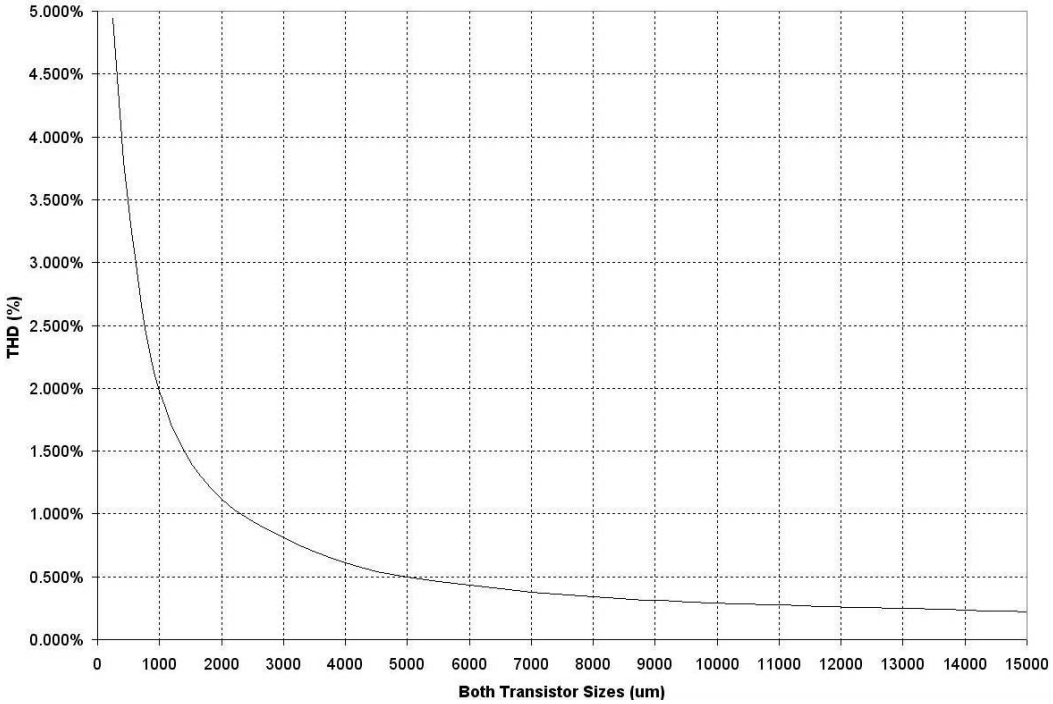


Figure 5-10 “STAC-DAC” THD vs. Transistor Sizes

As can be seen from the above figure, the larger the transistor sizes, the lower the THD. This occurs due to the fact that if the transistors are not large enough, there is not enough current drive and the output waveform becomes distorted. Figure 5-11 shows a plot of the efficiency versus the same transistor sizes.

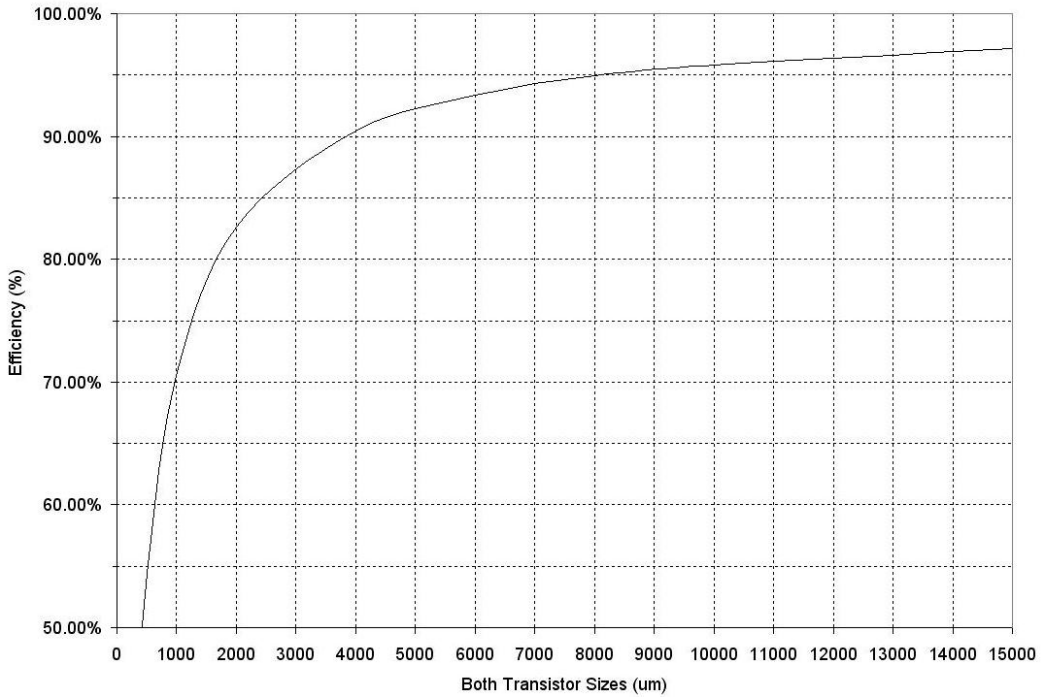


Figure 5-11 "STAC-DAC" Efficiency vs. Transistor Sizes

It can be seen from this figure that the efficiency curve has the exact same shape as the THD curve except that it is the inverse. Again, with lower transistor sizes, the circuit does not have enough current drive to reach the desired power output. The smaller the transistor sizes are, the larger the dynamic "on" resistance r_{DS} becomes for each transistor. A larger dynamic resistance causes the efficiency to decrease.

To achieve an optimum sizing, the smallest transistor size which corresponds to a minimized THD should be used. An optimum design would also make use of the smallest possible transistor sizes which correspond to a maximized efficiency. Looking at both figures it can be seen that the THD and efficiency begin to flatten out at a certain level. In order to achieve a THD of less than 0.5% and an efficiency of approximately 95%, the transistors need to be sized at a width of approximately 8,000 μm.

The efficiency and THD curves exhibit the same shape because they are both directly related to the amount of current drive in the circuit. This meant that the current drive of the transistors is a very important parameter to design for. It is known that the transconductance for a PMOS and NMOS device are different. To examine the effect of this, the next round of simulations dealt with varying the ratio of PMOS transistor sizes to an NMOS transistor size of 8,000 μm. All other parameters were kept the same as in the previous simulations. Figure 5-12 shows the THD versus the transistor size ratio.

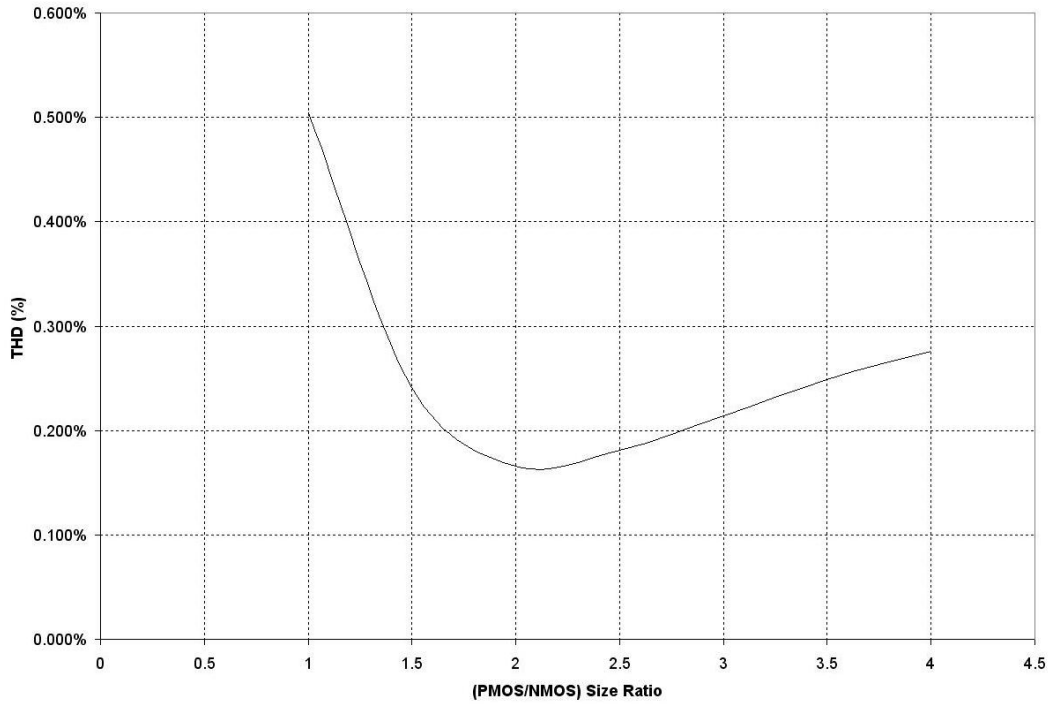


Figure 5-12 “STAC-DAC” THD vs. Transistor size ratio

The above graph shows that the THD is minimized when the ratio of PMOS to NMOS sizes is equal to 2. It also shows that the THD has been held below 0.5% for all cases due to the sizing determined from the previous simulations. The optimized PMOS/NMOS size ratio corresponds to the ratio of the PMOS/NMOS transconductances.

The THD will be minimized when the system has the same amount of current drive for both positive and negative voltages, regardless of which transistors are conducting at a given state. If the current drive is equivalent in all cases, it allows the output waveform to be symmetrical about the earth ground axis. When the current drive is not equivalent then the waveform becomes asymmetrical and this asymmetry is seen in the form of harmonics. In order to maintain a constant current drive for both the NMOS and PMOS transistors then the quantity K' * (W/L) should be equivalent for both devices. Since the PMOS device in this simulation had a transconductance equal to one half of the NMOS transconductance, then the width of the device must be doubled to get equivalent current drive capabilities.

Along with the THD, the efficiency was plotted against the (PMOS/NMOS) ratio as shown in Figure 5-13.

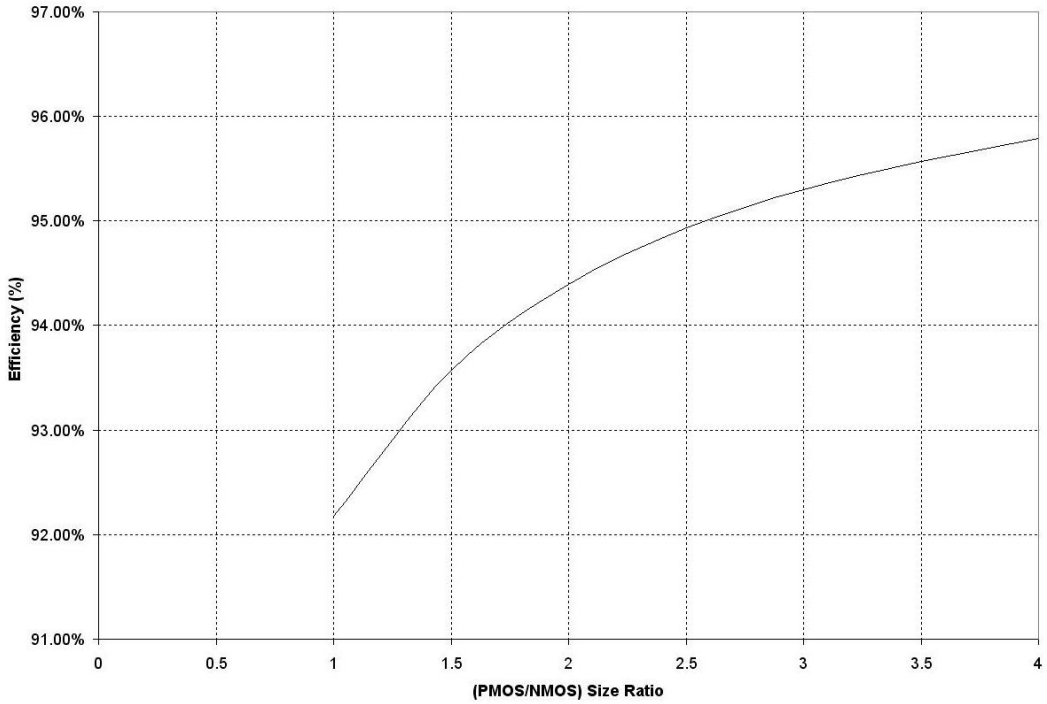


Figure 5-13 "STAC-DAC" Efficiency vs. Transistor size ratio

Again it can be seen that increased transistor sizes cause a reduced value of r_{DS} and therefore a better efficiency. At these already large transistor sizes, however, the amount of change in the efficiency is minimal and all the simulations operated at acceptable efficiencies of greater than 92%.

The next set of simulations explored the effects of varying the input frequency. This simulation is of utmost importance for the audio design as it will represent how the "STAC-DAC" adds distortion across the entire audio frequency spectrum. The input signal was varied from 20 Hz to 20 kHz. All the other parameters were kept constant from the previous simulations and the transistors were sized at 8,000 μm and the 16,000 μm respectively. Figure 5-14 shows the THD verses the logarithm of the signal frequency.

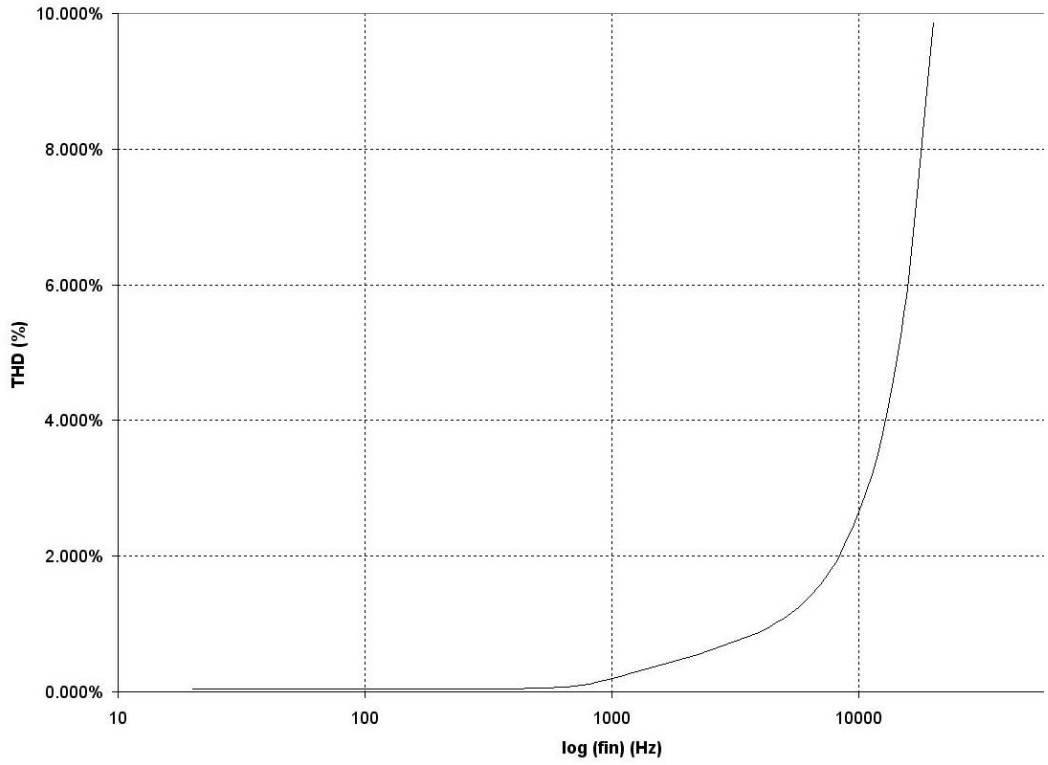


Figure 5-14 "STAC-DAC" THD vs. input frequency

This figure shows that the THD remains low and constant for low input frequencies but quickly explodes for frequencies above 5-10 kHz. The frequencies where the THD gets much larger are at the upper end of the human vocal range and are definitely well within the audible range. This amount of THD in these audible frequencies is simply not acceptable for high fidelity audio applications. The reason for the large increase in THD for higher frequencies is due to the sampling frequency of the system. Recall that the above simulation was run with a sampling frequency of 96 kHz. Based on the Nyquist sampling theorem, this means that the system should be able to reproduce signals with frequencies up to half of the sampling frequency, or 48 kHz in this case. The sampling theorem does not specify how accurately the signal can be reproduced however. As the frequency of the input is increased, there are less digital samples of the signal taken per cycle. The drastic reduction in samples per cycle causes the resolution to correspondingly decrease. In the "STAC-DAC" system, the analog output is a direct reconstruction of the digital samples therefore it will also mimic this low resolution and the output becomes distorted.

The internal sampling rate of the "STAC-DAC" can be adjusted in the front-end of the design. The 96 kHz sampling frequency shown above is not good enough to produce the desired high quality audio output desired. The distortion was shown to be directly related to the ratio of the sampling frequency to the input frequency. In order to find a sampling frequency which is suitable for audio, the THD was plotted versus the ratio of the sampling frequency to the input frequency. Figure 5-15 shows the results of this set of simulations.

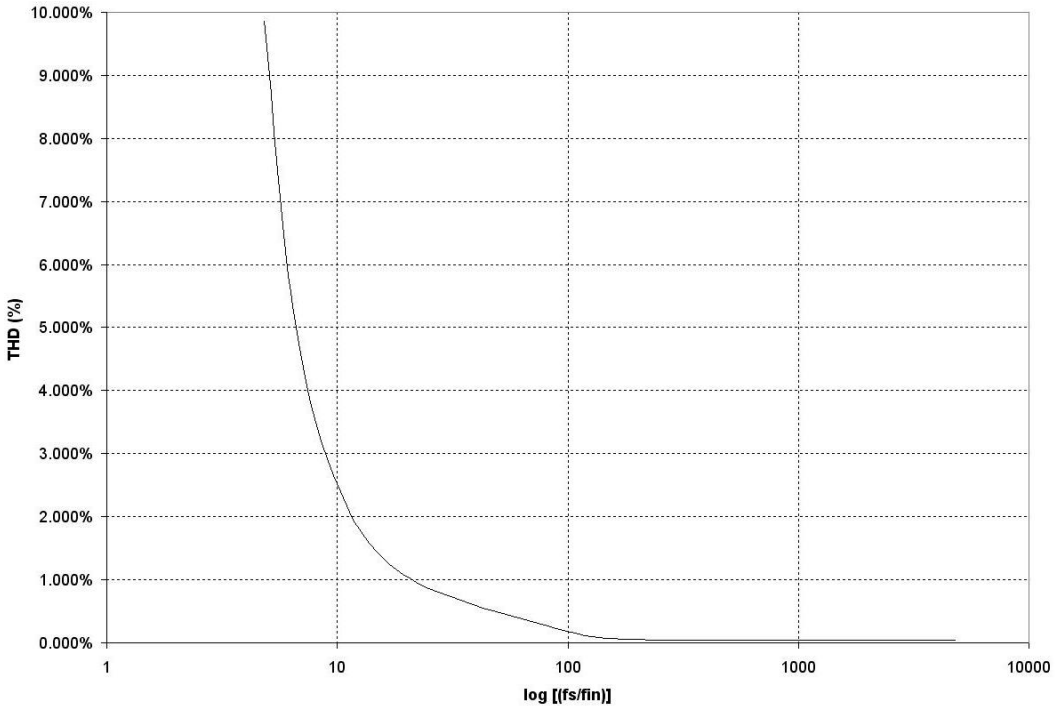


Figure 5-15 "STAC-DAC" THD vs. (f_S/f_{IN}) ratio

The above figure shows that to maintain a low level of THD that the ratio of the sampling frequency to the frequency of the input should be at least 100. If the maximum input frequency for the audio system is assumed to be 20 kHz, then to maintain low THD up to that frequency requires the internal sampling frequency of the "STAC-DAC" to increase to 2 MHz.

The next set of simulations show the THD versus the input frequency with the sampling rate increased to 2 MHz. All other parameters remained constant. Figure 5-16 shows these results.

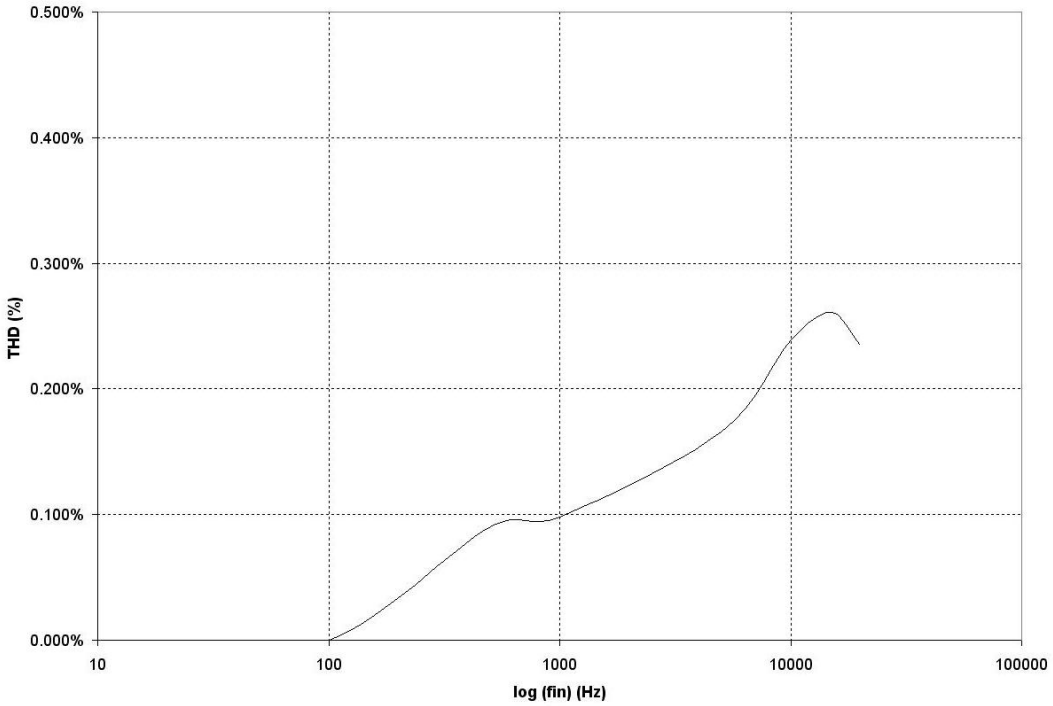


Figure 5-16 “STAC-DAC” THD vs. input frequency at 2 MHz sampling frequency

It should be noted that for the above set of simulations, no frequencies under 100 Hz were tested. This was due to the extremely large amount of digital data produced for a low frequency signal sampled at a higher rate. These large amounts of data required immense computational time to simulate. Since it was shown that the THD increases with increasing frequency then the THD for these omitted frequencies should be very low, therefore not making them necessary.

The figure shown above verifies that a 2 MHz sampling frequency satisfies the need for low THD figures over the audible frequency ranges. The maximum THD will still occur at the highest frequencies present, but the amount of THD was reduced to a value always below 0.3%.

Once the sampling frequency was set to 2 MHz, the next step was to determine an optimal cutoff frequency for the low-pass filter. Since the sampling frequency was increased this means that the switching noise and associated harmonics will also be increased in the frequency spectrum. Recall that it is the goal of the low-pass filter to remove this high frequency switching noise and to smooth the output signal. Because of this, the next set of simulations was run with respect to the ratio of the sampling frequency to the cutoff frequency while the sampling frequency was held constant. The frequency of the input signal was set to 20 kHz since this should represent the worst-case scenario for the simulations. All remaining design parameters remained constant. Figure 5-17 shows the effect on the THD.

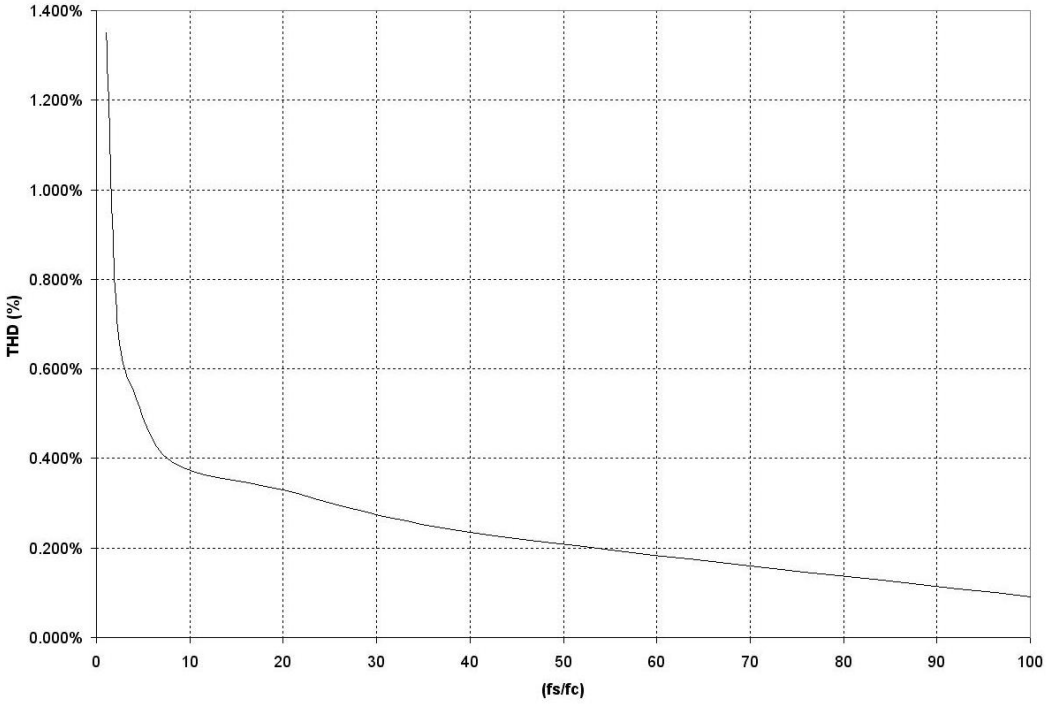


Figure 5-17 "STAC-DAC" THD vs. (f_S/f_C) ratio for 20 kHz input

As can be seen in the above figure, as the ratio of (f_S/f_C) increases, which corresponds to a lower cutoff frequency, the better the THD becomes because the filter is attenuating more and more of the high frequency harmonics. Recall that for audio filters, the phase distortion is just as important as the harmonic distortion. Figure 5-18 shows the phase distortion for the different ratio of filter cutoff frequencies.

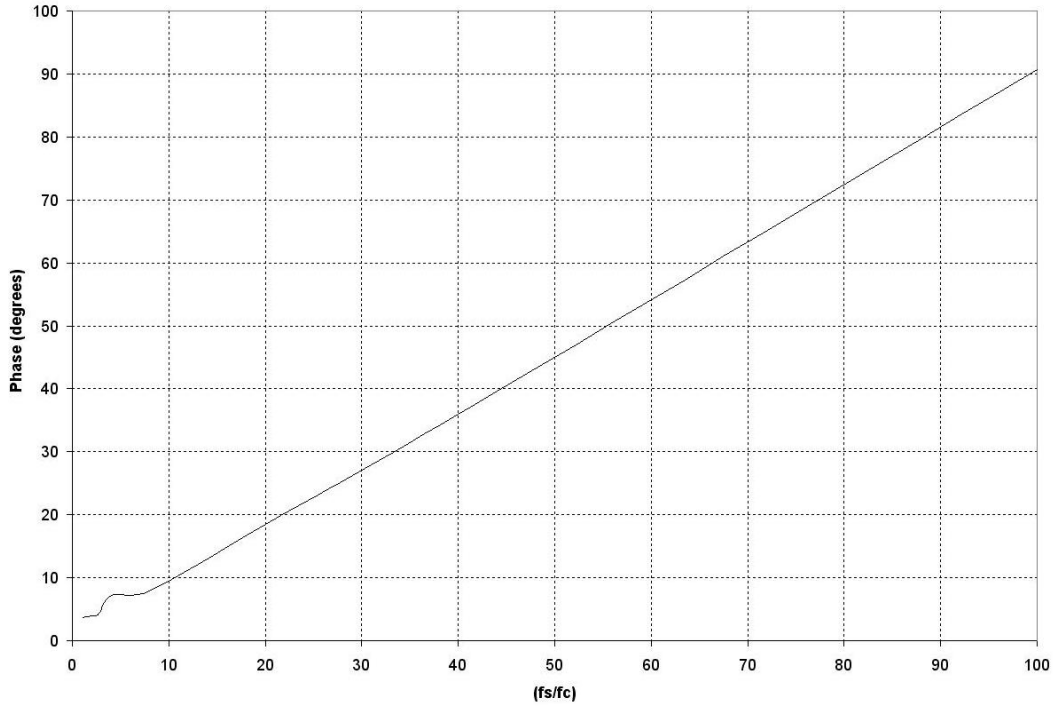


Figure 5-18 "STAC-DAC" Phase vs. (f_S/f_C) for 20 kHz input

The above figure shows that as the cutoff frequency is lowered, the phase distortion becomes worse. Recall that for a 2nd-order filter the phase will change by a total of 180 degrees and will be out of phase by 90 degrees directly at the cutoff frequency. The phase distortion starts to occur one decade before the cutoff frequency however, so the closer the cutoff frequency becomes to the audible range, the worse the phase distortion becomes.

A design trade-off must be made with the cutoff frequency of the low-pass output filter. The lower it is, the better for THD but the higher it is, the better for phase. In comparing the two sets of simulations it is determined that the phase distortion changes more quickly than the THD distortion as long as the ratio (f_S/f_C) is greater than or equal to ten. Due to this, the phase should be minimized as much as possible for a ratio above this. Since the phase gets worse the higher the ratio becomes then that ratio is determined to be optimally 10. For a sampling frequency of 2 MHz this requires that the upper cutoff frequency be set to 200 kHz. At a 200 kHz cutoff frequency, a 20 kHz input signal will have approximately 10 degrees of phase shift, which will be the worst-case scenario. It is said that the human ear can detect as small as approximately 5 degrees of phase shift so this phase distortion will be audible but should only be present for the very high end of the audible frequency range and should be much minimized. Also, with this cutoff frequency the THD remains below 0.4% for all audible frequencies.

To this point the Full Power Bandwidth has not been investigated. The bandwidth will vary depending on the sampling frequency and cutoff frequencies determined above. Since they are now designed for optimal THD, phase distortion and efficiency for a given power output it is now needed to verify that the FPBW is suitable for full power audio reproduction up to 20 kHz. Figure 5-19 shows the FPBW versus a varying cutoff frequency.

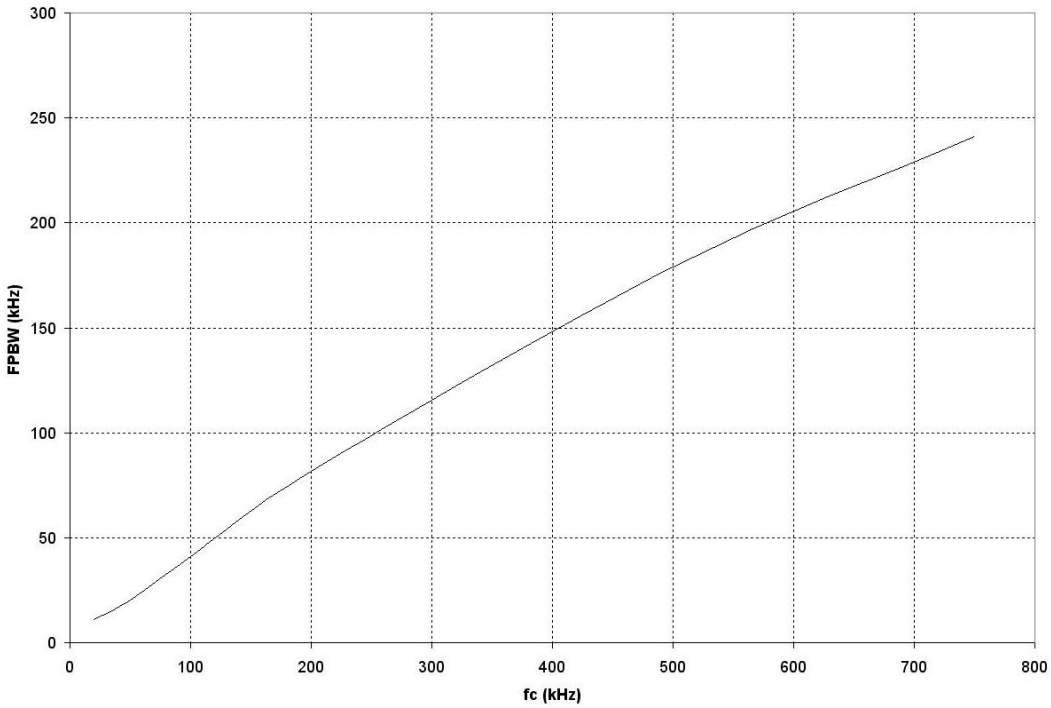


Figure 5-19 “STAC-DAC” FPBW vs. cutoff frequency

This figure shows that for any cutoff frequency above approximately 50 kHz, then the desired FPBW of 20 kHz will be met. For the 200 kHz cutoff frequency designed above the FPBW was approximately 80 kHz which is well beyond the necessary level. This figure also shows that if THD is not a concern, than by raising the value of f_C the “STAC-DAC” can operate with a full power bandwidth well beyond 100 kHz.

Another set of simulations were run to see the effects the addition of the switching spike capacitor had on the THD of the system with respect to the input frequency. Figure 5-20 shows the comparison THD both with and without the switching spike capacitor.

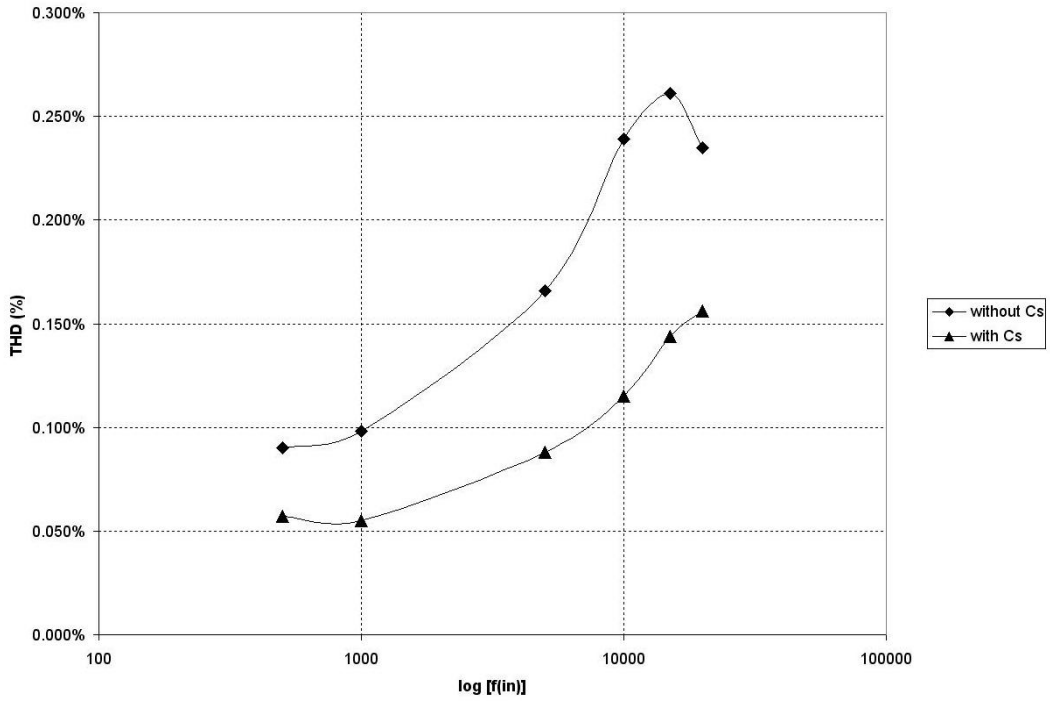


Figure 5-20 “STAC-DAC” THD vs. input frequency with switching capacitor

This figure shows that the switching spike capacitor does indeed lower the THD by adding another high frequency pole to the system to remove the switching spikes. The maximum THD drops from just under 0.3% all the way down to 0.15% and is below 0.1% for all frequencies below approximately 8 kHz. Since the pole created by the switching capacitor is a first order pole and is set at a much higher frequency than the audible range, it adds no additional detectable phase distortion to the system.

Another set of simulations was run to investigate the THD at various power outputs which will correspond to a varying listening level. The input frequency was again set to 20 kHz. Figure 5-21 shows the THD at different power levels.

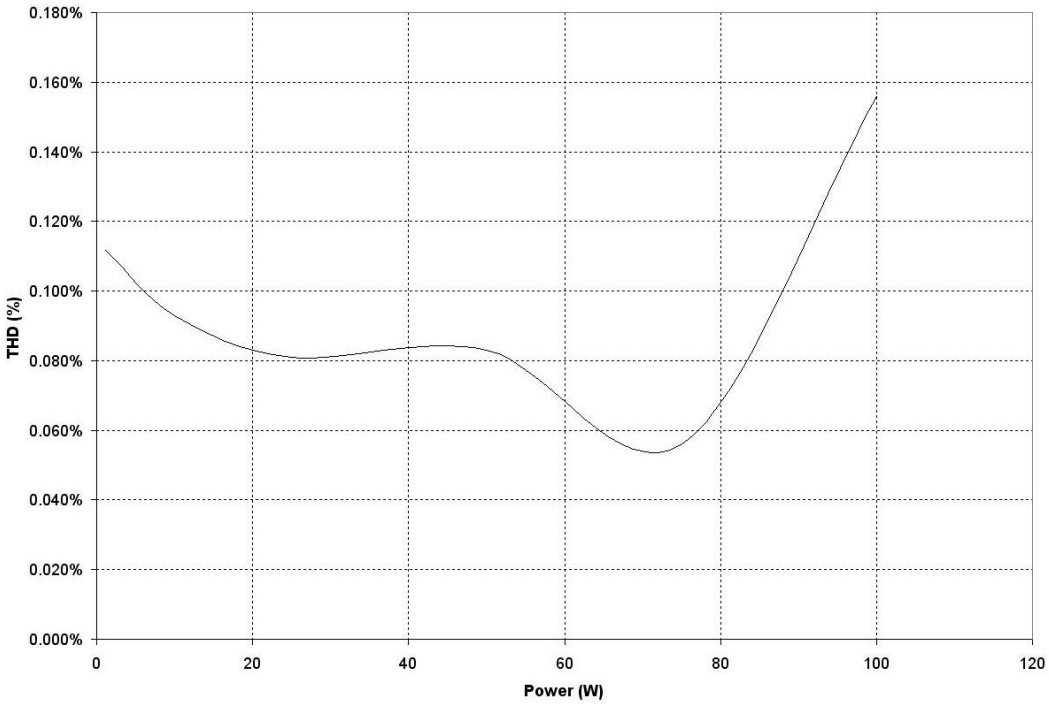


Figure 5-21 “STAC-DAC” THD vs. Power output

This figure shows that for medium power outputs the THD will be at its minimum levels. The THD rises on the two extreme ends of the power spectrum. When the power output is low the increase in THD is due to the precision of the power supplies in the “STAC-DAC”. For each voltage supply down the series circuit the precision must increase to maintain distortion less reproduction. When the output power is very low, the precision required simply can not be met and the distortion increases. When the power output is at a maximum the increase in THD is due to slewing distortion as is the case with most audio amplifiers.

A final set of simulations was run to compare the THD, efficiency and FPBW at the full power for a 20 kHz input signal for a 4-bit, 8-bit and 16-bit design. Figure 5-22 shows the effect on the THD.

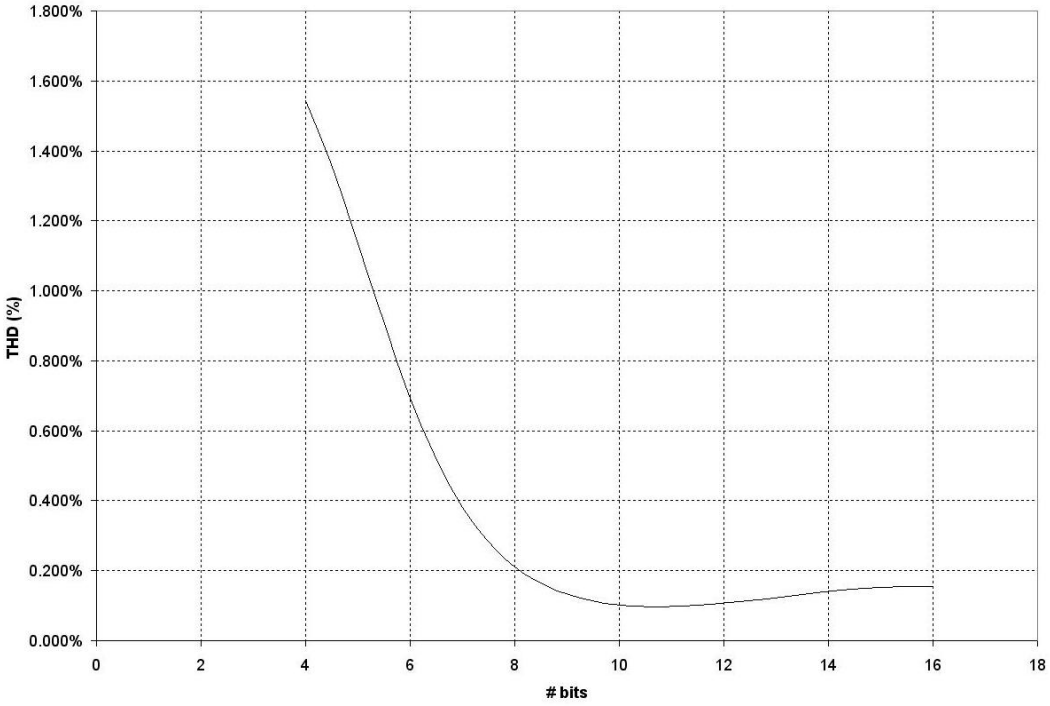


Figure 5-22 “STAC-DAC” THD vs. # of bits

Figure 5-23 shows the efficiency versus the number of bits.

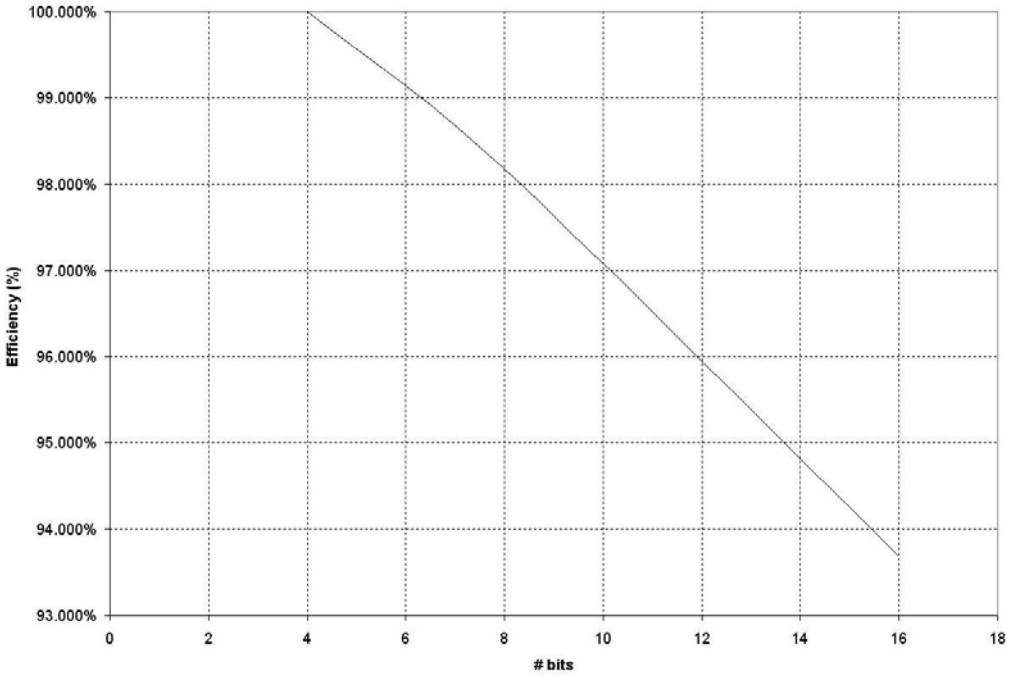


Figure 5-23 “STAC-DAC” Efficiency vs. # of bits

Finally, Figure 5-24 shows how the FPBW is affected.

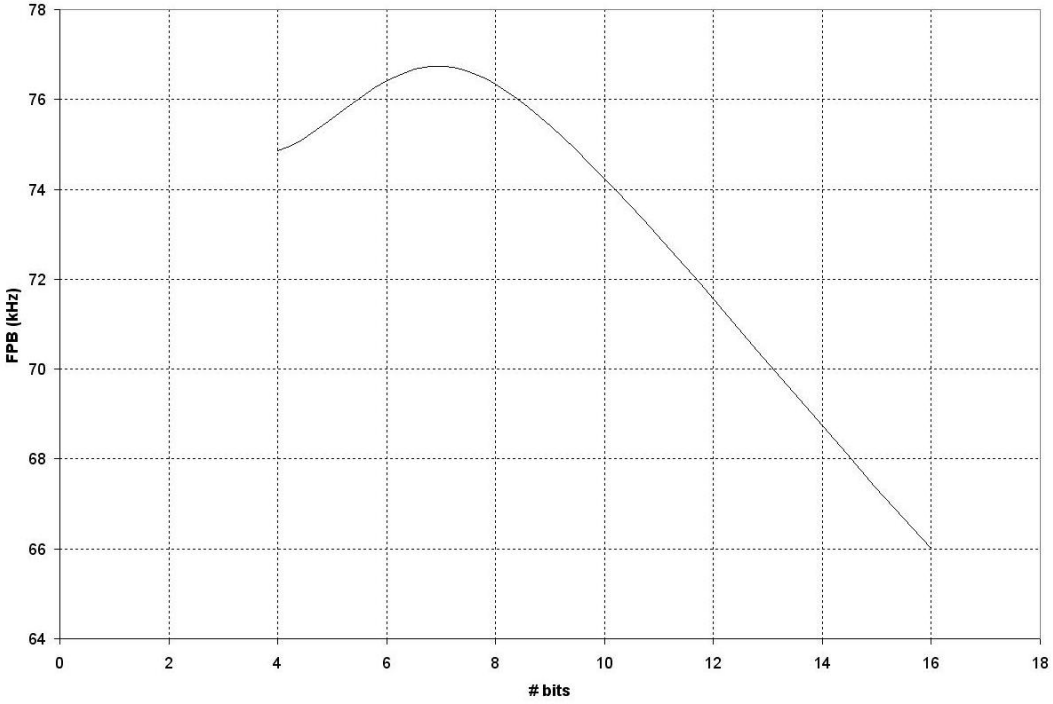


Figure 5-24 “STAC-DAC” FPBW vs. # of bits

5.3 Final Design

With all of the simulations for the “STAC-DAC” complete it is now possible to get a picture of the final, optimum design and also the performance capabilities of this power DAC system. Figure 5-25 shows the power analog output of the final “STAC-DAC” design.

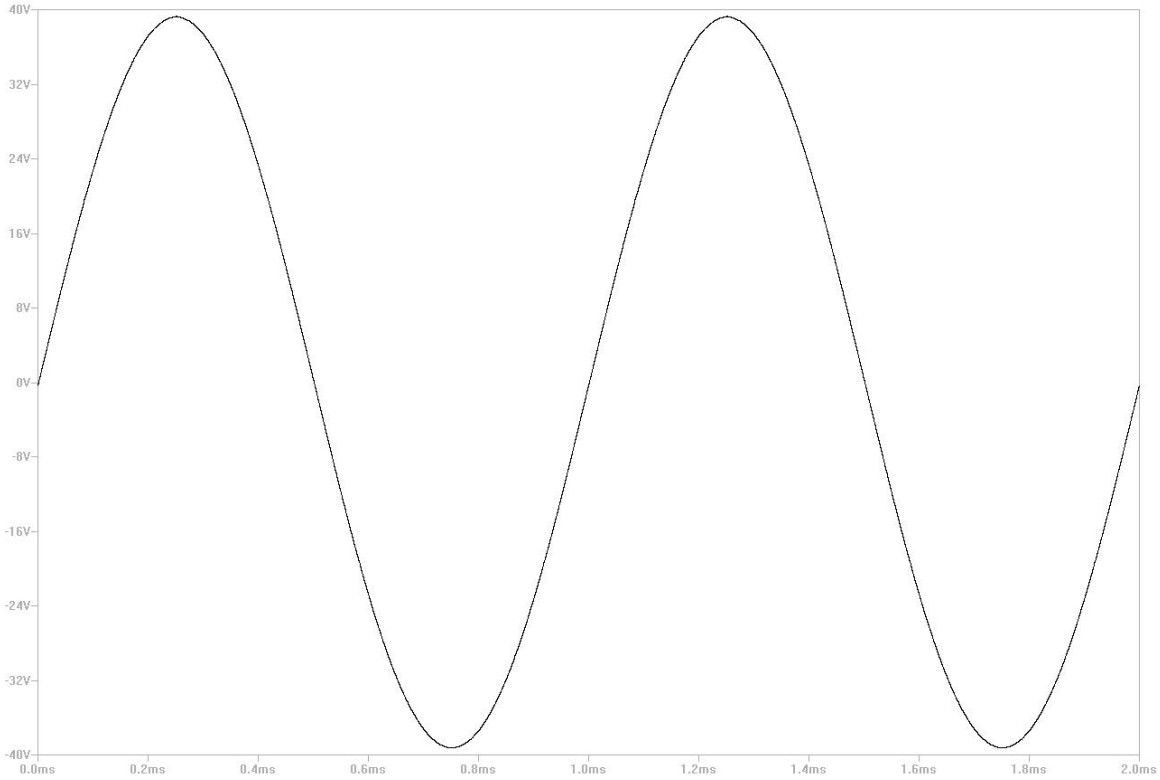


Figure 5-25 Final 16-bit, 100-watt “STAC-DAC” output

Table 5-2, shown below, summarizes all of the final optimized design parameters and all of the performance metrics tested in this thesis.

Number of bits	16
Loudspeaker Load	8 Ω
Power Output	100 W
Transistor Technology (L)	.18 μm
NMOS Size (W)	8,000 μm
PMOS Size (W)	16,000 μm
Sampling Frequency (f_S)	2 MHz
Low-pass Cutoff Frequency (f_C)	200 kHz
Efficiency (η)	93 %
Full Power Bandwidth	0-65 kHz
THD (20 kHz @ 100 W)	.156 %
Phase (20 kHz @ 100 W)	10.8 °
THD (1 kHz @ 100 W)	.055 %
Phase (1 kHz @ 100 W)	1.3 °
THD (20 kHz @ 50 W)	.080 %
THD (1 kHz @ 50 W)	.028 %

Table 5-2 Final Design Figures

Appendix B contains the frequency spectrum output by LTSpice for the final "STAC-DAC" design at 1 kHz and also shows the THD calculation output by LTSpice in its entirety. Since the "STAC-DAC" system implemented in this thesis is meant to be able to reproduce music, a simulation was run with a multi-frequency input as opposed to a pure tone. The results of that simulation are shown below in Figure 5-26.

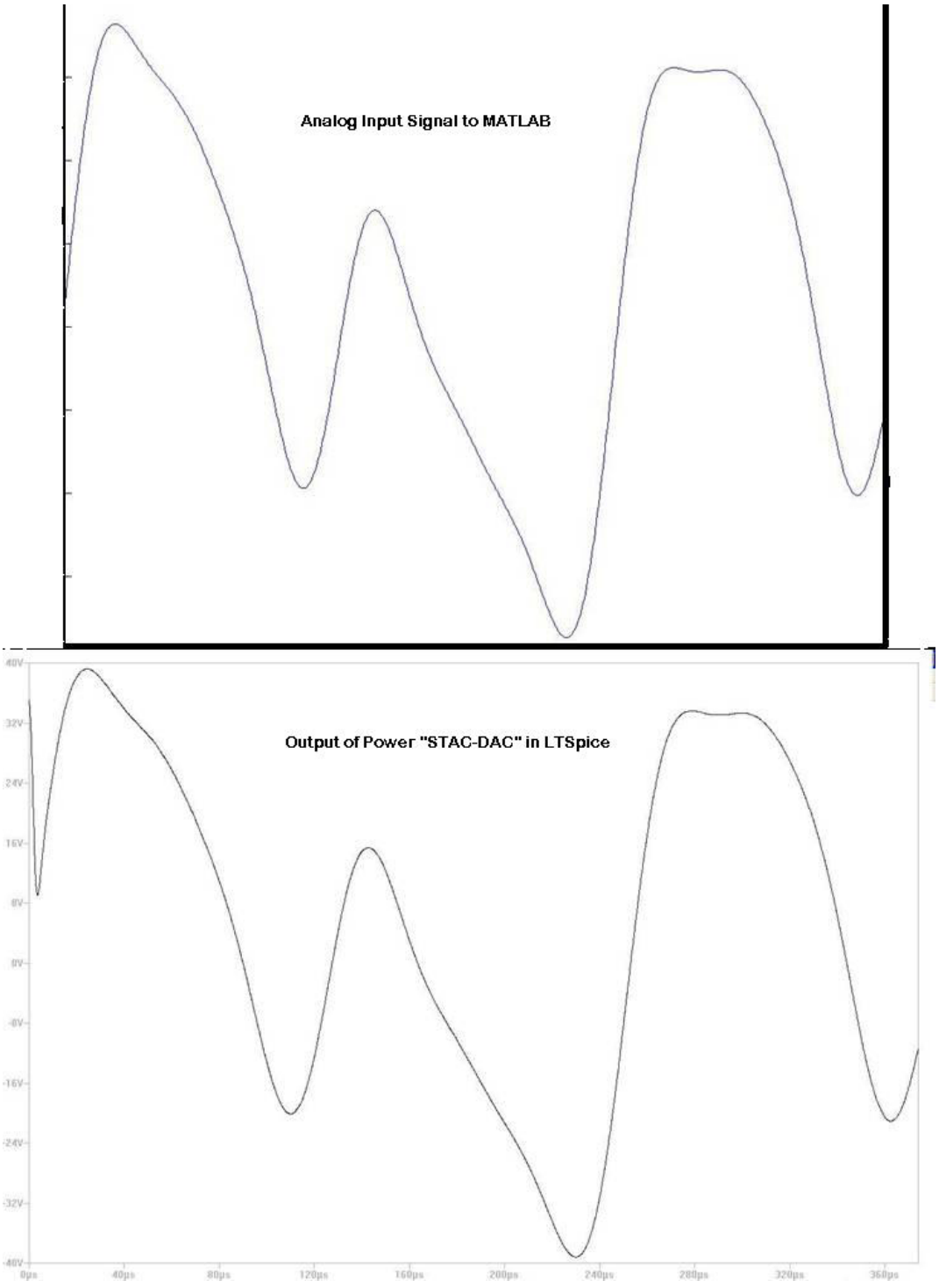


Figure 5-26 “STAC-DAC” reproduction of multi-frequency signal

These results obtained indicate that the objectives of the thesis were met by implementing the design and validating the proof of concept that a DAC and a power amplifier were successfully combined into one circuit. The results were shown to meet or exceed the requirements set forth in this thesis of high power output and high efficiency while maintaining low harmonic and phase distortion figures over the audio frequency band.

6. CONCLUSIONS

6.1 Summary of Work

In this thesis current digital-to-analog converters and types of audio power amplifiers were discussed. These two circuits have been considered as two separate and distinct entities. A new design was introduced which proposed the ability to merge a DAC with a power amplifier into one single power DAC system with the ability to produce a high power "direct from digital" output. This system was shown to be capable of merging the highly efficient circuitry associated with digital technologies with the low harmonic and phase distortion requirements associated with high fidelity analog audio systems. To meet these requirements the following specifications were desired:

Number of bits	16
Loudspeaker Load	8 Ω
Power Output	100 W
Transistor Technology (L)	.18 μm
Efficiency (η)	> 90 %
Full Power Bandwidth	> 20 kHz
THD (across FPBW)	< 0.1 %
Phase (across FPBW)	< 5°

Table 6-1 Expected Results

The front-end of the system was not investigated but assumed to already be functional and the back-end power "STAC-DAC" circuit implementation was explored in detail. The "STAC-DAC" design functionality was proven conceptually and then specific design equations were derived. Using the design equations, the "STAC-DAC" was built and tested via MATLAB and LTSpice. The results of these simulations were used to prove the validity of the design. Parameters of the design were then varied to see the effects each had on the performance of the system. Once the performance relationships were established it was possible to find an optimal final design for the "STAC-DAC" to meet the performance specifications desired. The final design achieved the results shown in the following table.

Number of bits	16
Loudspeaker Load	8 Ω
Power Output	100 W
Transistor Technology (L)	.18 μm
NMOS Size (W)	8,000 μm
PMOS Size (W)	16,000 μm
Sampling Frequency (f_S)	2 MHz
Low-pass Cutoff Frequency (f_C)	200 kHz
Efficiency (η)	93 %
Full Power Bandwidth	0-65 kHz
THD (20 kHz @ 100 W)	.156 %
Phase (20 kHz @ 100 W)	10.8 °
THD (1 kHz @ 100 W)	.055 %
Phase (1 kHz @ 100 W)	1.3 °
THD (20 kHz @ 50 W)	.080 %
THD (1 kHz @ 50 W)	.028 %

Table 6-2 Final Results Summary

These results obtained from Chapter 5 indicate that the objectives of the thesis were met and the results were shown to meet or exceed the requirements.

6.2 Thesis Contributions

This thesis proposes a design which allows for the combination of a digital-to-analog converter and a power amplifier into one single, high power, efficient circuit. Any design which requires a high power analog output to be controlled by a logic level digital

input can make use of the “STAC-DAC” design. For this thesis the design was intended for an audio application. The results validated that the “STAC-DAC” can produce low level THD figures over the audio frequency range. If very low THD figures are not necessary, however, depending on the tuning of the output filtering, power analog operation can be achieved into the hundreds of kilohertz all while maintaining high efficiency numbers.

6.3 Problems and Limitations

As is the case with most topologies, the weak link in the design is the amplification stage. This primary limitation of the “STAC-DAC” design deals with the operational amplifier used for the gate drive circuit. In order for the “STAC-DAC” to be optimal, it puts a large demand on the op-amps for each bit. The first hurdle is the fact that the op-amp needs to be able to accept very high voltage supply rails, on the order of 100 volts for a 100-watt design. The reason the high supply voltages are needed is that the output rail voltages supplied by the op-amps need to be larger than the largest possible peak analog output voltage to drive the transistors properly. Due to this, the maximum possible power output of the “STAC-DAC” design will be directly dependant upon the maximum possible power rails supplied to the op-amps. This relationship is shown in Equation 6-1.

$$P_{MAX} \approx \frac{V_{op-amp}^2}{2 * R_L} \qquad \text{Equation 6-1}$$

Also, a greater difference between the voltages supplied by the op-amp and the maximum analog output voltage implies a larger V_{GS} voltage for each transistor. The larger the value of V_{GS}, the larger the current drive capability becomes for the transistors. The simulations indicated that the THD decreases as the current drive increases as shown in Figure 5-10. Due to this, the larger the value of the op-amp supply rails, the lower the THD of the system.

The limiting factor on the op-amp operation for high output voltages is that it must maintain a high slew rate at the same time. This relationship is shown in Equation 6-2.

$$SR_{MIN} = \frac{\Delta V}{\Delta t} = 2 * V_{op-amp} * f_S \qquad \text{Equation 6-2}$$

This shows that for an op-amp switching between +/- 100 volts at a sampling frequency of 2 MHz requires the op-amp to have a minimum slew rate of 400 V/μs. As was the case with the voltage output, the larger the value of the slew rate for the op-amp, the lower the THD becomes for the "STAC-DAC" system. For a higher power output, the higher the rail voltages of the op-amp must become. Equation 6-3 shows the relationship between the slew rate and the power output.

$$P_{MAX} = \frac{SR_{MIN}^2}{8 * f_S^2 * R_L} \qquad \text{Equation 6-3}$$

Another limiting factor in the "STAC-DAC" design deals with the precision of the isolated voltage power supplies. In order to achieve the desired results, the power supplies need to maintain precision to 5 decimal places, or 10 μV. This voltage corresponds to the desired amount of change for the voltage supply V_0, corresponding to the LSB b_0, for a volume change resolution of 1% in the 100 watt design. If this precision can not be achieved then a larger volume change resolution is required. Also, since the output voltage is a sum of the supply voltages then the more accurate the supplies are the more accurate the output will be to the desired signal and therefore the lower the THD.

Discussing the limitations of the power supplies brings up a few more limitations to the design. The first is that the power supply rejection on each power supply needs to be very large. If the power supply rejection is not large, this noise will pass directly to the output. Even worse is the fact that this noise will be at approximately 120 Hz which is well into the audible band. Another fact about the power supplies is that they need to maintain a constant output under a widely variable load. The load seen by each voltage source will change depending on what digital state the "STAC-DAC" is in and therefore which other transistors and supplies are hooked into the series circuit. In order to maintain a low THD number, the power supplies need to remain unchanged in their outputs for all of these possible loads. A final limitation with the power supplies is seen during an incremental volume change. In order to maintain the linear volume control response, each power supply must correspond to a percentage change for each change in volume. These incremental changes in output voltage act like step changes to the supply. The power supplies need to exhibit minimal ringing during these step changes, otherwise this ringing will get sent to the output during each volume change.

6.4 Future Enhancements

Since the audio system presented in this thesis is a brand new design there is still room for future endeavors. There are also more topics that need to be investigated with greater detail to make this entire system a functioning reality. Some of these ideas for future enhancements are discussed below.

The first and most obvious topic that needs further research is the design of the front-end of the audio system presented since it was not a part of the research for this thesis. Understanding and designing the digital signal processing circuitry needed to supply the power "STAC-DAC" section correctly is critical for the full design.

Another area for future research includes using a more realistic model for the loudspeaker load instead of a purely resistive load. The more realistic model that is used, the more realistic the results obtained from the simulation will be. Along with a more realistic model of a loudspeaker impedance, the effects of adding crossover filters and any type of audio equalization should be investigated since these types of filtering circuits will most likely be present on the output of most audio systems.

Future research should be done on the power supply issues as well. It should be investigated to see what types of power supply designs would be best suited to meet the specifications needed, in a non-referenced manner, for this design. Also, it should be investigated as to exactly how good the power supply figures such as PSRR, load independence, low step-change ringing, and μV precision truly need to be to maintain the low distortion desired across the audio band. Also, an area for future research could be to try and design a "STAC-DAC" which also uses negative voltage supplies in the series circuit. This would allow the circuit to subtract voltages as well as add voltages instead of

only adding voltages. This would also allow the system to be referenced to ground instead of a negative voltage.

Possible ways to eliminate the reverse-biased body effect should be researched. A possible idea could be to tie the bulk terminals to the power rail voltages of the op-amp so that they are permanently at the extreme voltages in the circuit. Any possible ways to eliminate the body effect would be helpful as it would alleviate the current runaway states the "STAC-DAC" encounters. Reduction of the current runaway would make the circuit more stable and also reduce the pulsed power stresses on the devices.

Other possible areas for future enhancements include the op-amp and other volume control designs. Operational amplifier designs need to be researched to see the feasibility of a high voltage and high slew rate circuit which the "STAC-DAC" needs to incorporate. A different voltage control scheme could alleviate the step-change issue on the power supplies and would allow the volume adjustment to be continuous as opposed to quantized.

In order for the full design to become an actual product safety measures should be added in addition to the circuitry discussed. Two safety measures that could be added to the design include short circuit protection and gate protection circuits. The gate protection circuitry should be investigated so that oxide breakdown does not occur on the gate oxides of the transistors. This can happen due to the very large voltages being applied to the gates. Breakdown of this nature is permanent. Finally, the true test for an audio design is to actually build the device and listen to how it sounds. This test alone will be the final figure of merit for the actual audio abilities of the power "STAC-DAC" design.

APPENDIX A

MATLAB CODE

A.1 MATLAB Implementation of ADC

MATLAB was used to generate the digital inputs, at the desired sampling frequency, needed as the inputs to LTSpice for the "STAC-DAC" design. The code used to implement the ADC is shown below in Figure A-1.

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Weston R. Earick                              %
% Thesis Project                                %
% Initially created by Andrew Kondrath          %
% MATLAB program which implements functionality %
% of ADC for STAC-DAC and writes the digital    %
% outputs as PWL vectors to be read into LTSpice %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% set the number of bits to be used
bits=16;
% setting percentage of maximum peak to peak amplitude after quantization
% must range (0,1]
max_volts_in = 2;
volts_in = 2;
percent_max = volts_in/max_volts_in;

max_volts = 1;
volts= max_volts/(2^bits-1)*2.^((bits-1):-1:0);
volts = ones(size(volts))*100;

% setting sampling frequency
fs = 2e6;
% setting frequency of analog input(s)
f1 = 500;
% generating time vector
t = 0:1/fs:(3/f1);
% creating sine wave
v = volts_in*sin(2*pi*f1*t);
% scaling sine wave to be from 0 to 2^N ALWAYS!
v_scaled = percent_max*(v-min(v))/(max(v)-min(v))*(2^bits-1);
% rounding scaled bits to integers
v_round = round(v_scaled);
% getting binary value of the integers
v_bin = dec2bin(v_round,bits);

% setting up a time index
t_ind=t(2:end);
% opening a file to write to
fid = fopen('bits.dat','wt');

% looping through for each bit
for ind= 1:bits
    % making a vector to be 1 where a change occurs, and
    % 0 elsewhere
    d_v_bin= abs(diff(str2num(v_bin(:,ind))));
    % finding where changes occur
    [d_ind]=find(d_v_bin==1);
    % for every change, there are two times listed
    % (time at beginning of change and time at end of
    % change)
    t_ind2= zeros([1 2*length(d_ind)]);
    % needs to be a voltage for every time given
    v_ind= zeros(size(t_ind2));
    % setting the times
    ind2=2*(1:length(d_ind));
    t_ind2(ind2-1)= t_ind(d_ind);
    t_ind2(ind2)= t_ind(d_ind)+ 10^-7;
    % setting the voltages at each of the times
    v_ind(ind2-1)= volts(ind)*str2num(v_bin(d_ind,ind));
    v_ind(ind2)= volts(ind)*str2num(v_bin((d_ind+1),ind));
    ii = find(v_ind == 0);
    v_ind(ii) = -volts(ind);
    % creating the PWL vector
    pwl_vect= [[10^-9 t_ind2];[volts(ind)*str2num(v_bin(1,ind)) v_ind]];
    % writing to the file
    fprintf(fid,'PWL(');
    fprintf(fid,'%d %e ',pwl_vect);
    fprintf(fid,')\n');

end
% closing the file
fclose(fid);
```

Figure A-1 MATLAB Code for ADC implementation

APPENDIX B

LTSpice Output

B.1 LTSpice FFT Display and THD Calculation

LTSpice has a built in FFT function which allows it to output the frequency spectrum of any signal within the simulation. Figure B-1 shows the output signal of the "STAC-DAC" for the final design at 1 kHz.

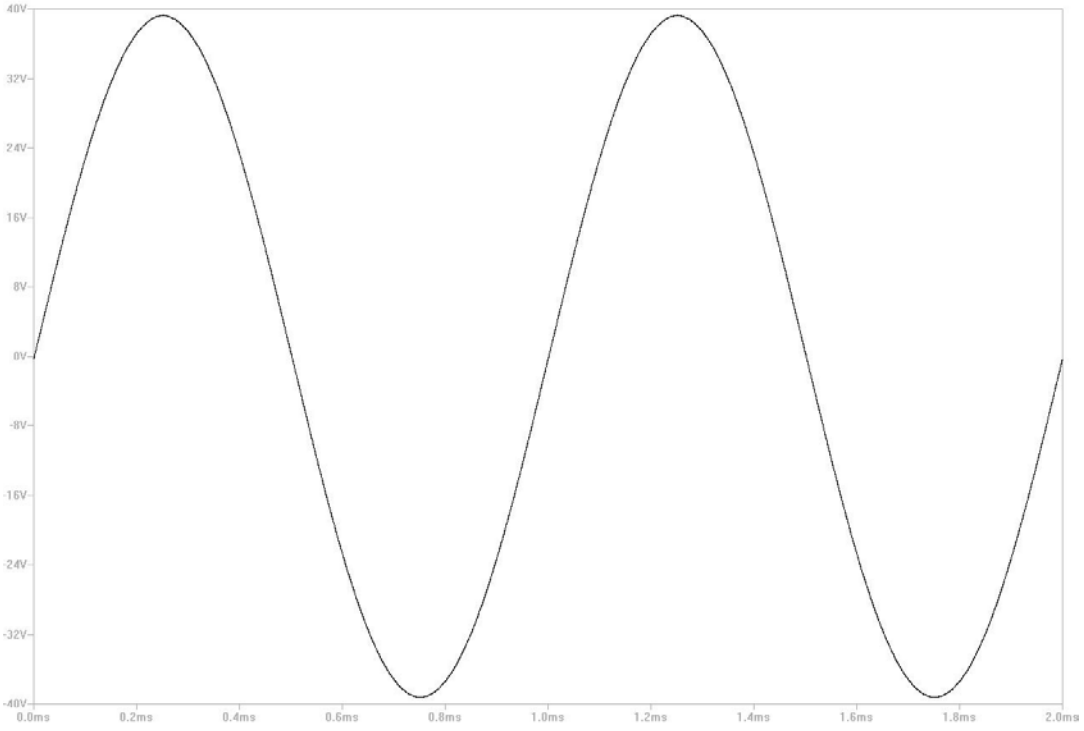


Figure B-1 Final "STAC-DAC" Output

The FFT of this signal as output by LTSpice is shown in Figure B-2 below.

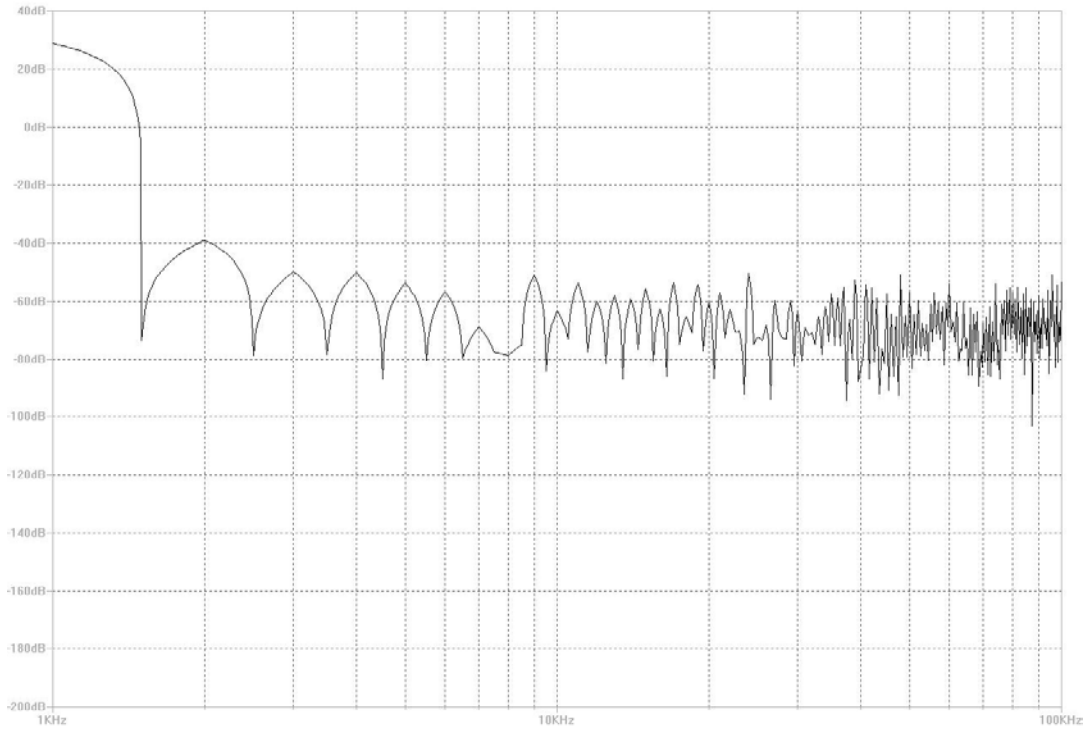


Figure B-2 Frequency spectrum of 1 kHz "STAC-DAC" output generated by LTSpice FFT

This shows that the dominant harmonic is a second harmonic. The 1 kHz fundamental has a value of 28.9 dB while the 2 kHz harmonic is at -39.1 dB or 68 dB down from the fundamental. The percentage of the total power associated with each harmonic up to 20 kHz is shown in Figure B-3.

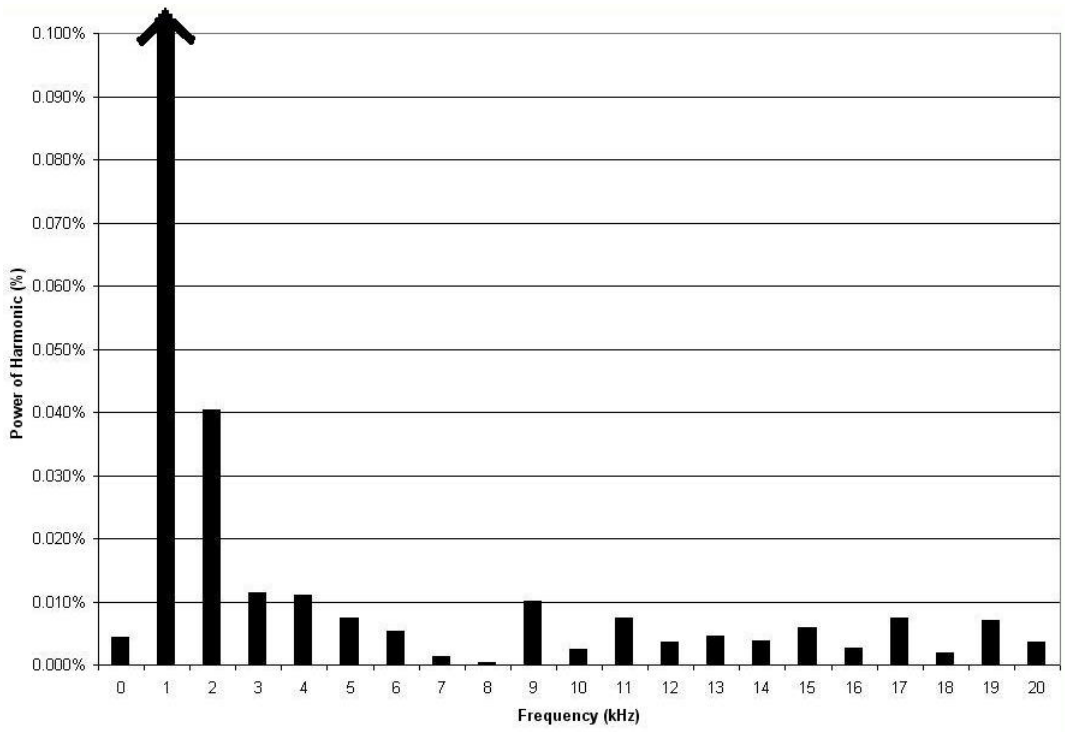
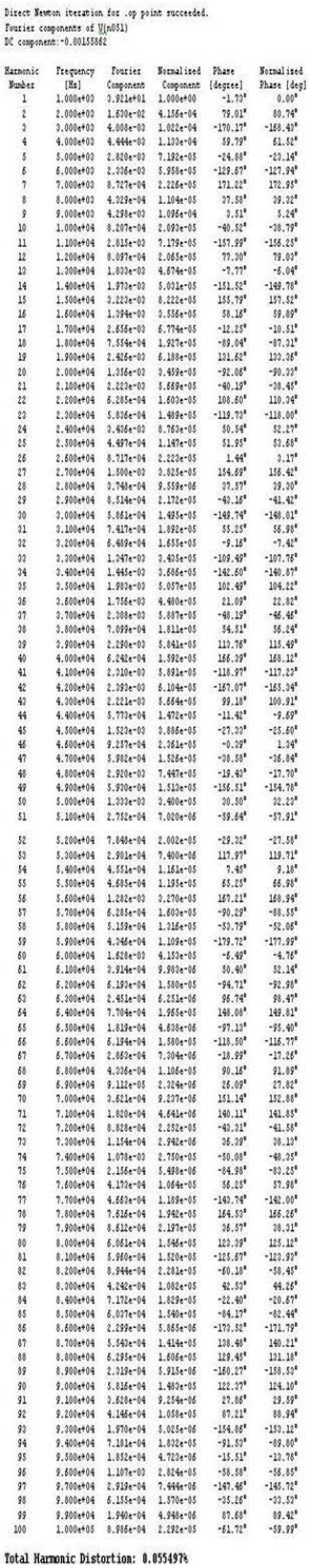


Figure B-3 Power percentages of signal harmonics

In order to see the power of the harmonics the above graph was condensed to below 0.1% which is why the fundamental frequency continues off the chart. The fundamental frequency corresponds to 99.86% of the total signal power followed by the second harmonic at 0.04% and then the third harmonic at 0.011%.

LTSpice has the ability to calculate the THD of any signal as well. An example of the output of the LTSpice THD calculation is shown in Figure B-4.



Direct Newton iteration for .op point succeeded.
Fourier components of V(n051)
DC component: -0.00155862

Harmonic Number	Frequency [Hz]	Fourier Component	Normalised Component	Phase [degree]	Normalised Phase [deg]
1	1.000e+03	3.921e+01	1.000e+00	-1.73°	0.00°
2	2.000e+03	1.630e-02	4.156e-04	78.01°	80.74°
3	3.000e+03	4.008e-03	1.022e-04	-170.17°	-168.43°
4	4.000e+03	4.644e-03	1.183e-04	59.79°	61.52°
5	5.000e+03	2.820e-03	7.192e-05	-24.88°	-23.14°
6	6.000e+03	2.336e-03	5.958e-05	-129.67°	-127.94°
7	7.000e+03	8.727e-04	2.226e-05	171.22°	172.95°
8	8.000e+03	4.329e-04	1.104e-05	37.58°	39.32°
9	9.000e+03	4.298e-03	1.096e-04	3.51°	5.24°
10	1.000e+04	8.207e-04	2.093e-05	-40.52°	-38.79°
11	1.100e+04	2.815e-03	7.179e-05	-157.99°	-156.25°
12	1.200e+04	8.097e-04	2.065e-05	77.30°	79.03°
13	1.300e+04	1.833e-03	4.674e-05	-7.77°	-6.04°
14	1.400e+04	1.972e-03	5.031e-05	-151.52°	-149.78°
15	1.500e+04	3.223e-03	8.222e-05	155.79°	157.52°
16	1.600e+04	1.394e-03	3.556e-05	58.16°	59.89°
17	1.700e+04	2.656e-03	6.774e-05	-12.25°	-10.51°
18	1.800e+04	7.554e-04	1.927e-05	-89.04°	-87.31°
19	1.900e+04	2.426e-03	6.188e-05	121.62°	123.36°
20	2.000e+04	1.356e-03	3.459e-05	-92.06°	-90.33°
21	2.100e+04	2.223e-03	5.669e-05	-40.19°	-38.45°
22	2.200e+04	6.285e-04	1.603e-05	108.60°	110.34°
23	2.300e+04	5.816e-04	1.483e-05	-119.72°	-118.00°
24	2.400e+04	3.416e-03	8.712e-05	50.54°	52.27°
25	2.500e+04	4.497e-04	1.147e-05	51.95°	53.68°
26	2.600e+04	8.717e-04	2.223e-05	1.44°	3.17°
27	2.700e+04	1.500e-03	3.825e-05	154.69°	156.42°
28	2.800e+04	3.740e-04	9.539e-06	37.57°	39.30°
29	2.900e+04	8.514e-04	2.172e-05	-40.16°	-41.42°
30	3.000e+04	5.861e-04	1.495e-05	-149.74°	-148.01°
31	3.100e+04	7.417e-04	1.892e-05	55.25°	56.98°
32	3.200e+04	6.469e-04	1.650e-05	-9.18°	-7.42°
33	3.300e+04	1.347e-03	3.435e-05	-109.49°	-107.76°
34	3.400e+04	1.945e-03	4.960e-05	-142.60°	-140.87°
35	3.500e+04	1.983e-03	5.057e-05	102.49°	104.22°
36	3.600e+04	1.755e-03	4.476e-05	21.09°	22.82°
37	3.700e+04	2.308e-03	5.887e-05	-48.13°	-46.40°
38	3.800e+04	7.099e-04	1.811e-05	54.51°	56.24°
39	3.900e+04	2.290e-03	5.841e-05	112.76°	114.49°
40	4.000e+04	6.242e-04	1.592e-05	166.39°	168.12°
41	4.100e+04	2.310e-03	5.891e-05	-118.97°	-117.23°
42	4.200e+04	2.393e-03	6.104e-05	-167.07°	-165.34°
43	4.300e+04	2.221e-03	5.664e-05	99.18°	100.91°
44	4.400e+04	5.772e-04	1.472e-05	-11.42°	-9.69°
45	4.500e+04	1.523e-03	3.886e-05	-27.33°	-25.60°
46	4.600e+04	9.257e-04	2.361e-05	-0.39°	1.34°
47	4.700e+04	5.982e-04	1.526e-05	-38.50°	-36.84°
48	4.800e+04	2.920e-03	7.447e-05	-19.40°	-17.70°
49	4.900e+04	5.920e-04	1.512e-05	-156.51°	-154.78°
50	5.000e+04	1.339e-03	3.400e-05	30.30°	32.23°
51	5.100e+04	2.752e-04	7.020e-06	-59.64°	-57.91°
52	5.200e+04	7.848e-04	2.002e-05	-29.32°	-27.58°
53	5.300e+04	2.901e-04	7.400e-06	117.97°	119.71°
54	5.400e+04	4.551e-04	1.161e-05	7.45°	9.18°
55	5.500e+04	4.603e-04	1.195e-05	65.25°	66.98°
56	5.600e+04	1.282e-03	3.270e-05	167.21°	168.94°
57	5.700e+04	6.285e-04	1.603e-05	-90.23°	-88.55°
58	5.800e+04	5.159e-04	1.316e-05	-53.79°	-52.06°
59	5.900e+04	4.346e-04	1.109e-05	-179.72°	-177.99°
60	6.000e+04	1.628e-03	4.152e-05	-6.48°	-4.76°
61	6.100e+04	3.914e-04	9.983e-06	50.40°	52.14°
62	6.200e+04	6.193e-04	1.580e-05	-94.71°	-92.98°
63	6.300e+04	2.451e-04	6.251e-06	96.74°	98.47°
64	6.400e+04	7.704e-04	1.965e-05	148.08°	149.81°
65	6.500e+04	1.813e-04	4.626e-06	-97.12°	-95.40°
66	6.600e+04	6.194e-04	1.580e-05	-118.50°	-116.77°
67	6.700e+04	2.863e-04	7.304e-06	-18.99°	-17.26°
68	6.800e+04	4.306e-04	1.106e-05	90.16°	91.89°
69	6.900e+04	9.112e-05	2.324e-06	26.09°	27.82°
70	7.000e+04	3.621e-04	9.237e-06	151.14°	152.88°
71	7.100e+04	1.820e-04	4.641e-06	140.11°	141.85°
72	7.200e+04	8.828e-04	2.252e-05	-43.31°	-41.58°
73	7.300e+04	1.154e-04	2.942e-06	36.39°	38.13°
74	7.400e+04	1.078e-03	2.750e-05	-50.08°	-48.35°
75	7.500e+04	2.156e-04	5.498e-06	-84.98°	-83.25°
76	7.600e+04	4.172e-04	1.064e-05	56.25°	57.98°
77	7.700e+04	4.663e-04	1.189e-05	-140.74°	-142.00°
78	7.800e+04	7.616e-04	1.942e-05	164.53°	166.26°
79	7.900e+04	8.612e-04	2.197e-05	36.57°	38.31°
80	8.000e+04	6.061e-04	1.546e-05	123.39°	125.12°
81	8.100e+04	5.960e-04	1.520e-05	-125.67°	-123.93°
82	8.200e+04	8.944e-04	2.281e-05	-60.18°	-58.45°
83	8.300e+04	4.242e-04	1.082e-05	42.53°	44.26°
84	8.400e+04	7.172e-04	1.829e-05	-22.40°	-20.67°
85	8.500e+04	6.037e-04	1.540e-05	-84.17°	-82.44°
86	8.600e+04	2.299e-04	5.865e-06	-173.32°	-171.79°
87	8.700e+04	5.542e-04	1.414e-05	138.46°	140.21°
88	8.800e+04	6.295e-04	1.606e-05	129.46°	101.18°
89	8.900e+04	2.319e-04	5.915e-06	-160.27°	-158.52°
90	9.000e+04	5.816e-04	1.483e-05	122.37°	124.10°
91	9.100e+04	3.628e-04	9.254e-06	27.86°	29.59°
92	9.200e+04	4.146e-04	1.058e-05	87.21°	88.94°
93	9.300e+04	1.970e-04	5.025e-06	-154.86°	-153.12°
94	9.400e+04	7.181e-04	1.832e-05	-91.53°	-89.80°
95	9.500e+04	1.852e-04	4.723e-06	-15.51°	-13.78°
96	9.600e+04	1.107e-03	2.824e-05	-58.59°	-56.85°
97	9.700e+04	2.919e-04	7.444e-06	-147.46°	-145.72°
98	9.800e+04	6.155e-04	1.570e-05	-35.26°	-33.53°
99	9.900e+04	1.940e-04	4.948e-06	87.68°	89.42°
100	1.000e+05	8.986e-04	2.292e-05	-61.72°	-59.99°

Total Harmonic Distortion: 0.055497%

Figure B-4 Output of THD calculation in LTSpice

REFERENCES

1. Aminian, Ali and Marian Kazimierczuk, *Electronic Devices: A Design Approach*, New Jersey: Prentice-Hall, 2004.

2. Sedra, Adel S. and Kenneth C. Smith, *Microelectronic Circuits, 4th Ed.,* New York: Oxford University Press, 1998.

3. Allen, Phillip E. and Douglas R. Holberg, *CMOS Analog Circuit Design, 2nd Ed.,* New York: Oxford University Press, 2002.

4. Jacob, J. Michael, *Analog Integrated Circuit Applications,* New Jersey: Prentice-Hall, 2000.

5. Nilsson, James W. and Susan A. Riedel, *Electric Circuits, 6th Ed.,* New Jersey: Prentice-Hall, 2001.

6. Leach, W. Marshall, *Introduction to Electroacoustics & Audio Amplifier Design, 3rd Ed.,* Iowa: Kendall/Hunt Publishing, 2003.

7. Eargle, John and Chris Foreman, *Audio Engineering for sound reinforcement,* Wisconsin: Hal Leonard Corporation, 2002.

8. Haykin, Simon, *Communication Systems, 4th Ed.,* New York: John Wiley & Sons Inc., 2001.

9. Kamen, Edward W. and Bonnie S. Heck, *Signals and Systems, 2nd Ed.,* New Jersey: Prentice-Hall, 2000.

10. Moscal, Tony, *Soundcheck: The Basics of Sound and Sound Systems,* Wisconsin: Hal Leonard Corporation, 1994.

11. Kazimierczuk, Marian K. and Dariusz Czarkowski, *Resonant Power Converters,* New York: John Wiley & Sons Inc., 1995.

12. Seashore, Carl E., *Psychology of Music,* New York: Dover Publications, 1967.