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Spontaneous Spin Polarization due to Lateral Spin-Orbit Coupling in InAs Quantum Point Contacts

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Abstract

This dissertation reports the first experimental observation of spontaneous spin polarization due to lateral spin orbit coupling (LSOC) in side- gated (SG) quantum point contacts (QPCs). The QPC devices are fabricated on InAs/InGaAs quantum well structures using e-beam lithography. The low band gap InAs semiconductor was chosen because of its large intrinsic spin-orbit coupling. The side gates are realized by wet etching technique which is optimized to pattern the QPC devices. The width of the QPC is varied from 200 nm to 500 nm, while the length of the QPC is kept in the range 150-200 nm. The gradient in the lateral potential confinement in a side gated (SG) quantum point contact (QPC) causes a spin-orbit coupling (SOC). This LSOC induces a spontaneous spin polarization of opposite nature at the two edges of the QPC *in the absence of any applied magnetic field*. We have observed an anomalous conductance plateau at $G \cong 0.5\ (2e^2/h)$ (0.5 structure) in the SG QPCs fabricated on InAs/InGaAs QW structures. The 0.5 structure moves up in perpendicular magnetic field and approaches the normal conduction quantization at $G = (2e^2/h)$ in high magnetic field, whereas in-plane magnetic field has no effect on it. The evolution in magnetic field clearly indicates LSOC is responsible for the 0.5 structure. We believe it is the asymmetry in the confining potential of the QPC that leads to a net spin polarization giving the 0.5 structure. By electrically modulating the asymmetry of the QPC confinement, we have succeeded in making this structure appear and disappear. Such a QPC can conceivably be used as a spin polarizer or detector on demand by tuning the gate voltages. We also have proposed a dual-QPC device to experimentally validate the spin polarization by electrical means.

Dedicated

To

My Parents

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Chapter 1

Overview

The field of *spintronics* is based on the manipulation of the spin and charge degrees of freedom simultaneously. The field of metallic spintronics has already proven enormously successful, and delivered functional devices such as GMR read heads in hard disks and MRAM of insulator spintronics. Despite the enormous success of metal-based spintronics, the emerging field of *semiconductor spintronics*, compatible with conventional microelectronics, is recognized as the next leap on information technology. It holds promise for the development of all-semiconductor MRAMs, very fast and low-power spin FETs, and spin-based quantum computation [1, 2]. The basic Physics research is currently focused on the fundamental problems in semiconductor spintronics, such as: all-electrical spin control via spin-orbit interactions, transporting spins between different locations within conventional semiconductor environments, coherent manipulation of electron spin at a given location, diluted magnetic semiconductors, and fixed or mobile spin qubits for quantum computing [1, 2, 12].

The controlled creation, detection, and manipulation of spin-polarized currents by *purely electrical means* are the challenges facing semiconductor spintronics [1]. In this context, the spin-orbit coupling (SOC) is envisioned as a possible tool for *all-electrical* spin control in semiconductor devices without ferromagnetic elements or external magnetic fields. SOC in the III-V semiconductor lifts the spin degeneracy and may have different physical origins. The Rashba SOC (RSOC) [3] arises from the asymmetry in the confining potential of a two-dimensional (2D) electron or hole gas. The Lateral SOC (LSOC) [4, 5] arises from an in-plane electric field resulting from the lateral confining potential of a quantum wire. The SOC can polarize the electrons in the semiconductor. The *RSOC* and the *LSOC* can be considered as two ideal tools to achieve this objective

since both can be varied *in situ* by an external gate voltage. In this research work, one of the objectives is to study the influence of the SOC on electron transport in 1D quantum point contact (QPC) made from semiconductor structures with large SOC.

Numbers of theoretical studies have proposed ways to produce spin polarization in semiconductor channels using LSOC. It has been reported in Refs [4] and [5] that due to LSOC opposite spins accumulate along the edges of the lateral confinement. Still there is no experimental evidence of LSOC in a 1D system. Can this spin polarization due to LSOC cause an anomalous conductance plateau in a 1D quantum? We aim to study the spontaneous spin polarization in QPC due to LSOC.

In a ballistic 1D system (e.g. QPC) conduction is quantized in integral multiple of $2e^2/h$, where the factor 2 is coming from the spin degeneracy of the electrons. A few years after the discovery of the conductance quantization, an additional plateau was observed at $G \cong 0.7$ ($2e^2/h$) in the absence of any magnetic field in a AlGaAs/GaAs QPC [4]. Since then, this anomalous plateau has been observed in many experiments, both in GaAs electron and hole 1D systems [4,6,13-16], and commonly referred as the ' *0.7 structure*'. Based on the characteristics of this 0.7 structure (such as, evolution of 0.7 structure in temperature, in parallel magnetic field, formation of the zero bias anomaly), there have been many theoretical attempts to understand its origin. The most intriguing of them are the spin polarization models [6-8] in which static spin polarization of the electrons has been predicted that gives a plateau in the range (0.7-0.5) ($2e^2/h$). But, this anomaly is not a universal feature since it is not observed in all devices. Its existence is found to depend on gate voltage adjustments and hence on the details of the lateral confining potential [9, 10]. The intrinsic SOC in the GaAs electron system is very small.

And, therefore, the 0.7 structure observed in the quantum wires or QPCs, fabricated on the GaAs electron systems, cannot be explained in terms of the LSOC.

The SOC in an InAs quantum well (QW) is very large [11]. The side gated (SG) QPC devices fabricated on InAs QW structures offer a strong lateral confinement. Thus, the LSOC in the SG QPC is expected to be enhanced. Moreover, the profile of the confining potential in the SG QPC can be tuned by applying bias voltages to the gates. This gives an opportunity to manipulate the spin polarization in the QPC. Can then the QPC devices, fabricated on InAs QW structure, be used as a spin polarizer by totally electrical means?

We have observed an anomalous conductance plateau observed at $\boldsymbol{G \cong 0.5\ (2e^2/h)}$ (we will latter call it as '0.5 structure') on SG QPC devices fabricated on InAs/InGaAs QW structures. The origin of the 0.5 structure is the spontaneous spin polarization due to LSOC. The potential profile of the lateral confinement can be manipulated by applying asymmetric gate voltage to the side gates of the SG QPC device. The anomalous 0.5 structure can be made to appear or disappear by adjusting the bias voltages of the gates that create the potential confinement of the SG QPCs. *This is the first experimental observation of the LSOC in semiconductor heterostructures.*

This dissertation is organized as follows: In Chapter 2, we will discuss on the current theoretical and experimental status of the SOCs and anomalous conductance quantization due to spontaneous spin polarization. Chapter 3 will focus on the growth of InAs QW structures and their characterization. In this chapter we will also highlight the different fabrication steps of 1D nano-scale devices. The experimental and measurement techniques will be discussed in the Chapter 4. In Chapter 5, we will underline the

experimental results. We will discuss the experimentally observed 0.5 structure, its behavior in both perpendicular and parallel magnetic fields and the temperature dependence of this anomalous structure. We will discuss how asymmetry in the confining potential affects the 0.5 structure. The new device that is proposed to detect the spin polarization by transport measurements will also be discussed in this chapter. Finally, we will summarize our results and give a brief comparison between our 0.5 structure and the anomalous plateau observed by other groups. In Chapter 6, we will give a brief outlook of future work.

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Chapter 2

State-of-the-Art

2.1 Introduction

Spin electronics or *spintronics* is based on the simultaneous manipulation of the spin and charge degrees of freedom in a multitude of systems and aims to develop electronic devices based on the control of the electron spin. It holds promise for the development of all-semiconductor MRAMs, very fast and low-power spin FETs, and spin-based quantum computation [1, 2].

In III-V semiconductors, spin-orbit coupling (SOC) lifts the spin degeneracy of the conduction band electrons without any external magnetic field. Since, spin transport is strongly affected by coupling of the spin and orbital degrees of freedom, the spin-orbit coupling (SOC) is visualized as a possible tool for *all-electrical* spin control in semiconductor devices without ferromagnetic elements or external magnetic fields. SOC may have different physical origins and can play a vital role in spintronics to realize active spin devices like Spin-filters, Spin-FET etc. In this context, the *Rashba spin-orbit coupling* (RSOC) [3] and recently proposed *lateral spin orbit coupling* (LSOC) [4, 5] offer an interesting possibility since both of these SOCs can be varied by an external electric field in semiconductor heterostructures and quantum wells.

SOC may cause the spontaneous spin polarization in a 1D system such as quantum point contact (QPC). A deeper understanding of different SOCs and spontaneous spin polarization may help to generate future usable devices based on spin transport. In this chapter, we will discuss the current theoretical and experimental status of different kind of SOCs. The current status of the spontaneous spin polarization and the anomalous conductance quantization observed in a 1D quantum point contact (QPC) will also be discussed.

2.2 Spin Orbit Coupling

Spin orbit coupling (SOC) is a relativistic effect which may arise in a semiconductor and cause spontaneous spin polarization. The SOC may have different physical origins. In the subsequent section SOC and different types of SOCs will be discussed.

I. What is SOC?

SOC is a relativistic effect which can be derived from the Dirac equation [6] and expressed as

$$H_{SO} = \lambda \hat{\sigma}.\left(\vec{k} \times \vec{\nabla} V\right), \tag{2.1}$$

where $\lambda = -\frac{\hbar^2}{4m_o^2 c^2} \approx -3.7\times10^{-6}\,\text{Å}^2$, m_o is the vacuum electron mass, $\boldsymbol{k} = \boldsymbol{p}/\hbar$, c is the speed of the light and $\boldsymbol{\sigma}$ are the Pauli spin matrices . The potential, V, in the semiconductor may arise due to impurities, asymmetry in the confinement well, boundaries and also by external means. In Dirac equation, the positive and negative energy are separated by an energy gap of $2m_oc^2 \approx 1$Mev and is known as Dirac gap. For a slow electron ($v/c << 1$) and a weak electric field (in Eq. (2.1) the field arises due to the voltage gradient), the SOC is very small because of the large Dirac gap. In semiconductor materials and structures with the approximation of a two band model the equations of the band theory are similar to Dirac equation and the Dirac energy gap is replaced by the energy gap between conduction and valence band which is only 1 eV or less in many III-IV semiconductors [7-9]. The SOC in narrow band gap semiconductor thus enhance a lot and thus make the SOC very prominent in semiconductor.

The voltage gradient in Eq. (2.1) gives rise to an electric field which appears as:

$$\vec{E} = \left(\frac{1}{e}\right)\vec{\nabla}V\,. \tag{2.2}$$

The electrons, in their reference frame, feel that electric field as an effective magnetic field,

$$\vec{B}_{eff} = 1/c\left(\vec{v}\times\vec{E}\right), \tag{2.3}$$

which causes the spin orbit coupling. Thus, spin degeneracy of the conduction band electrons of a III-V semiconductor can be lifted without any external magnetic field due to SOC. The static electric field that causes the SOC results from different physical origins such as inversion asymmetry of the microscopic crystal potential in the bulk zinc-blende semiconductor and is known as bulk inversion asymmetry (BIA). The second is the inversion asymmetry of the macroscopic potential that confines the 2DEG and is known as the structure inversion asymmetry (SIA). The voltage gradient along the edges of the lateral confinement also causes a spin orbit coupling which is known as lateral spin orbit coupling (LSOC).

II. Dresselhaus Spin Orbit Coupling

Bulk inversion asymmetry (BIA) causes a spin orbit coupling which refers to the lack of an inversion center in the III-V zinc-blende semiconductor structures. The inversion symmetry in space and time, change the wave vector ***k*** into –***k***. In addition, the time inversion also flips the spin. Combining these two symmetry operations one get a twofold degeneracy of the single particle energies as $E(\boldsymbol{k},\uparrow) = E(\boldsymbol{k},\downarrow)$ and is common in group-IV elements such as diamond, Si, Ge. But the III-V zinc blende structure does not

maintain the inversion symmetry and $E(\boldsymbol{k},\uparrow) \neq E(\boldsymbol{k},\downarrow)$. Thus, BIA lifts the spin degeneracy for a given direction of the wave vector $\boldsymbol{k}$. Dresselhaus first pointed out BIA [10] and the SOC that arises due this BIA is know as Dresselhaus SOC. For a quasi-two dimensional case in a sufficiently narrow quantum well (QW) grown in [001] direction, the Dresselhaus SOC term can be written as [11, 12]

$$H_D = \beta\left(k_x\sigma_x - k_y\sigma_y\right), \tag{2.4}$$

where β is the characteristic parameter that is proportional to $1/d^2$ with d being the width of the QW. For $d = 100$ Å, it is found that β ranges from 2×10^{-10} to 2×10^{-9} eV cm [8]. The Dresselhaus SOC is experimentally observed in bulk InSb by analyzing the Shubnikov-de Haas (SdH) effect [13] and by an optical method on the GaAs (110) surface [14]. Since the Dresselhaus effect depends strongly on the crystallographic direction, it is possible to find the direction in which this effect is minimum [15]. These optimal directions are, respectively, [1 2 0] and [1 0 0] for GaAs and InAs channels realized from the 2DEGs in quantum wells with [0 0 1] as the growth direction.

III. Rashba Spin Orbit Coupling

The structural inversion asymmetry (SIA) in the confining potential well of a 2D electron system gives rise to an interface electric field E perpendicular to the plane of the well. This inversion asymmetry field causes an enhanced spin-orbit coupling, known as Rashba spin orbit coupling (RSOC). The Hamiltonian that describes the RSOC is given as [3]

$$H_R = \alpha\left(\vec{\sigma} \times \vec{k}\right)\hat{z}\ , \tag{2.5}$$

where $\boldsymbol{\sigma}$ are the Pauli matrices, $\boldsymbol{k}$ is the quasi 2D momentum vector and α is the Rashba parameter that defines the strength of the SOC.

The RSOC causes the spin splitting without any external magnetic field and is finite for a nonzero *k*. Due to the relativistic effect, the moving electrons feel the interface electric field E as an effective magnetic field ($B_R = \alpha k / \mu_B$). This pseudo magnetic field, known as Rashba magnetic field, lies in the plane of the 2DEG and is perpendicular to the electric field, *E*, and the wave vector, *k*. The spins of the electron moving with the wave vector *k* precess around the direction, B_R.

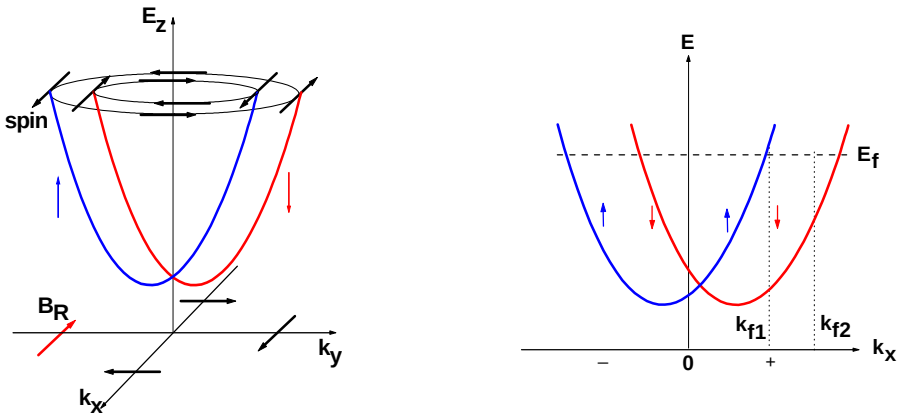


Fig. 2.1. Energy dispersion of Rashba spin-split subbands: (a) 2D case: black arrows represent spin eigen states. (b) 1D case: spin-up and spin-down electrons travel with different Fermi velocities.

Due to RSOC the electron density of states split into spin up and spin down subbands with the energy dispersion relation (Fig. 2.1) given by

$$E(k) = \frac{\hbar^2}{2m^*}k^2 \pm \alpha k \,, \tag{2.6}$$

where k magnitude of the momentum wave vector and m^* is the electron effective mass. The Rashba parameter α is defined as,

$$\alpha = \alpha^* |e| E \,, \tag{2.7}$$

with α^* being the SOC parameter. The magnitude of α depends on the confining potential and can also be controlled by external means (by applying gate voltage).

So, the spin degeneracy of a 2DEG is lifted for $k \neq 0$ without any external magnetic field. The spin splitting energy is given by $\Delta_R = 2\alpha k_F$ at $k \neq 0$, where k_F (= $(2\pi n)$)$^{1/2}$ is the average Fermi wave vector and can be determined from the 2DEG carrier concentration, n. The Fermi surface of a 2DEG in the presence of Rashba spin splitting consists of concentric circles with radii k_{F1} and k_{F2} (Fig. 2.1 (a)), the Fermi wave vectors of the two spin split energy bands. In 1D, electrons are spin polarized and travel with different velocities in the same direction as shown in Fig. 2.1 (b). These two Fermi wave vectors correspond to two electron gases with slightly different carrier concentration $n_{\pm}$ and can be observed from the beating pattern in the Shubnikov-de Haas oscillations (SdH) [16, 17]. The nodes in the beating pattern occur at the half integer values of $\Delta_R / \hbar\omega_c$ [18], where $\omega_c = eB/m^*$ is the cyclotron frequency. The node index, N, is derived as a function of $1/B$ as [17],

$$N = \frac{m^* \Delta_R}{e\hbar}\left(\frac{1}{B}\right) + \left(\frac{g^* m^*}{2m_0} + \frac{1}{2}\right), \tag{2.8}$$

where g^* is the effective electronic g factor and μ_B is the Bohr magneton. By plotting N against $1/B$, spin orbit splitting energy Δ_R and g^* can be found. Then knowing the Fermi

energy k_F from the total concentration in the SdH measurement, the Rashba parameter α can be determined. Typical values of α ranged from 10^{-9} eV-cm to 6×10^{-9} eV-cm for InAs based QWs [7, 19].

The Rashba spin-orbit coupling and its manipulation by an external electric field in 2DEGs at an asymmetric heterojunction or in an asymmetric quantum well have been well established from experimental studies of the beating pattern in SdH oscillations [17, 20, 21]. Very recently, the evidence of the Rashba spin precession has been reported in strained bulk GaAs and InGaAs using ultrafast optical techniques [22]. However, *so far there has been no unambiguous experimental observation of the Rashba spin precession tuned by electrical means*, the corner stone of the concept of the Datta-Das spin FET [23]. Attempts have been made to observe the Rashba spin precession with inconclusive results in electron channels of widths large enough so that the channels are 2D [24, 25]. The 1D channel offers a unidirectional propagation wave vector ***k,*** and therefore the *spin quantization axis* defined by the Rashba magnetic field B_R is well defined [61]. This is not the case in a 2D system since the Fermi surface is a circle. Despite several advantages, 1D or 1D ballistic systems have not been used so far for studying the Rashba spin precession.

IV. Lateral Spin orbit Coupling

The other kind of SOC, which has been proposed in 2006[4, 5, 26], arises due to the lateral confining potential known as lateral spin orbit coupling (LSOC). Consider a quantum wire with a current flowing in the x direction, y is the lateral direction and 2DEG is lying in the x-y plane (Fig 2.2(a)). The confining potential, $V(y)$, is defined in

the y-direction where it is constant at the center of the quantum wire and rises up along the edges (Fig 2.2(b)). The electrons confined by such a non-uniform lateral potential well are moving with relativistic speed and the spin and orbital degrees of freedom of the electron are coupled together [6].

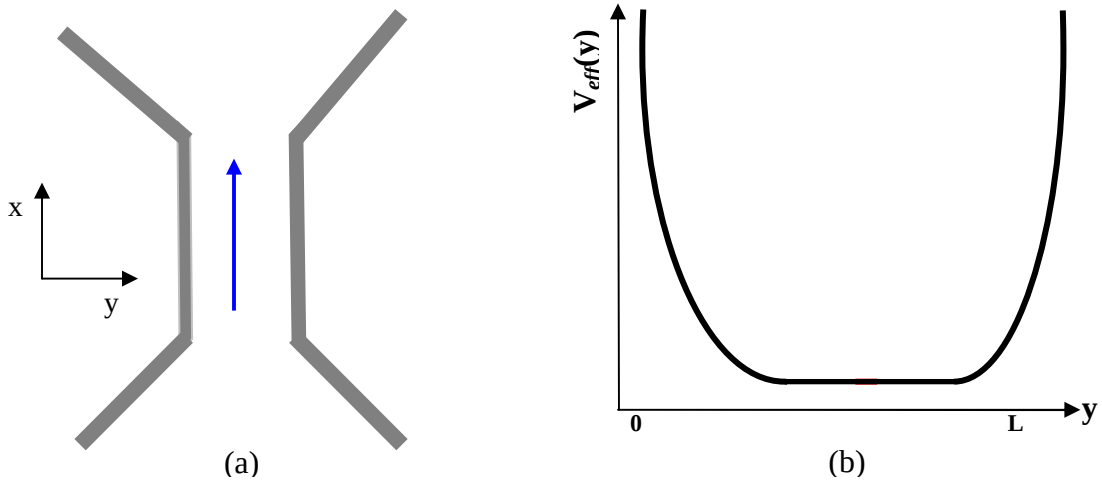


Fig. 2.2. (a) Schematic of the 1D Quantum Wire . The blue arrow shows the channel direction, (b) Lateral confinement in 1D.

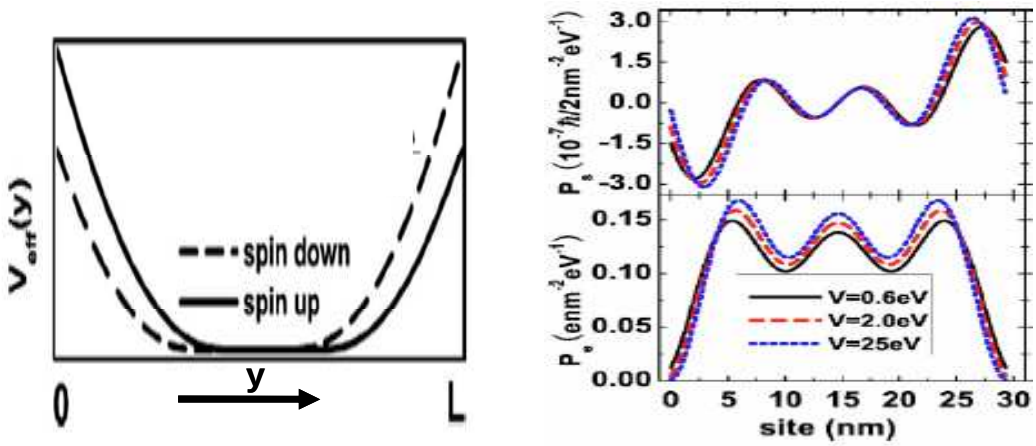
The SOC due to lateral confinement (LSOC) has the form [6, 27],

$$H_{SO} = -\frac{\hbar^2}{4m_o^2c^2}\hat{\sigma}.\left[\vec{k}\times\vec{\nabla}V(y)\right], \tag{2.9}$$

where $\hat{\sigma}$ are the Pauli matrices, $\vec{k}$ is the wave vectors, and $V(y)$ is the lateral (transverse) confining potential. The voltage gradient along the edges gives rise to an electric field perpendicular to the edge [see Eq. (2.2)]. Due to the relativistic effect, that electric field causes a SOC along the edges with SOC energy [5],

$$V_{SO} = -\frac{\hbar^2}{2m^{*2}c^2}\sigma_z k_x \partial V(y)/\partial y\,, \tag{2.10}$$

It is clearly seen from Eq. (2.10) that, the effective potential for spin up (σ_z = +1) and spin down electrons (σ_z = -1) have different values along the two edges (y = 0 and y = L). When the electrons are moving in the positive k_x direction at y = 0, the effective potential is lower for spin-down electrons *(σ_z = -1)* than for spin-up electrons *(σ_z = 1)* (Fig. 2.3(a)). But at y = L the effective potential of spin-up electrons is lower than spin-down electrons for positive k_x (Fig. 2.3(a)). Thus, opposite spins are accumulates along



(a) (b)

Fig. 2.3. (a) Spin-up and spin-down electrons have different effective potential along the two edges, (b) different spin accumulates along the two edges [5].

the two different edges with electrons moving in k_x direction under longitudinal bias voltage (Fig. 2.3(b)). The sign of spin accumulation is reversed when the electrons are moving with -k_x. So, LSOC can cause the spin polarization along the edges. The numerical results in Refs. 4 and 5 suggested that spin accumulation can occur in both

square and parabolic confining potential and the spin accumulation density $P_s(y)$ is zero for $V = 0$ and $P_s(y)$ increases as V increases.

The bottom part of Fig. 2.3 (b) shows the charge density $P_e(y)$ as a function of lateral direction, y. The top part of Fig. 2.3 (b) is the spin accumulation density $P_s(y)$ which indicates the two opposite spin accumulates along the two opposite transverse edges. It is shown that the spin accumulation in the middle of the channel is small and oscillates which is due to the quantum interference between the spin-up and spin-down components of the electron wave functions. It is also reported that in the presence of random impurity the oscillations of the spin density in the middle of the strip are suppressed strongly [4, 5]. This is because the random impurity scattering destroy the quantum interference of the spin-up and spin-down electron wave functions in the middle of the strip

A number of theoretical studies have proposed ways to produce spin polarization in semiconductor channels using the SOC. The most intriguing among them is the spin Hall effect (SHE) which states that a transverse spin current is created when a charge current is flowing in the longitudinal direction and different types of spins accumulates along the lateral edges of sample due to the transverse spin current [28-31]. This phenomenon is very attractive in semiconductor spintronics as it predicts an effective way of producing spin currents or spin polarization in a semiconductor without using magnetic material or external magnetic field. Two types of SHE are predicted in theory. One of them is *intrinsic* SHE that arises due to intrinsic SOC and occurs even in the absence of any impurity [28, 29]. The other one is *extrinsic* SHE that arises due to extrinsic SOC coming from impurity scattering [31, 32]. The intrinsic SHE discovery has

generated a tremendous amount of interest in the research community and there has been a flurry of theoretical work in the area. The subject remains highly controversial. The extrinsic SHE was experimentally observed by Kato *et. al.* in n-doped bulk GaAs [33]. Another work claimed to have experimentally observed intrinsic SHE by measuring the circular polarization of light emitted by p-n junction LED [34]. But the direct observation of SHE is still missing.

The LSOC implies that, under longitudinal bias voltage, different spins accumulate along the two opposite edges of the sample strip. This is very similar to SHE but the spin polarization occurs due to a different mechanism. The experimental result of SHE [33, 34] can be explained using this new theory. In Ref [5], LSOC has predicted the spin density distribution $P_s \approx 0.3 \times 10^{-6}$ nm^{-2} eV^{-1} and the spin polarization as 0.8×10^{-4}, which are in good agreement with the experimental results obtained from Ref [33]. In a recent paper Hattori and Okamoto [26] proposed that in cross wires transverse spin separation and spin Hall effect can be observed due to LSOC in the ballistic limit. Still there are no experimental results regarding the LSOC.

2.3 Anomalous Conductance Plateau and Spontaneous Spin Polarization in GaAs QPCs

In a 1D ballistic quantum point contact (QPC) the conductance is quantized in unit of $2e^2/h$ as:

$$G = n\left(2e^2/h\right). \tag{2.11}$$

Here n is the number of occupied energy subbands with the subband energy bottom lower than the Fermi energy E_F and each subband is doubly degenerate [35, 36]. The Fermi

energy can be swept up or down by changing the gate voltage in the QPC. So, as a function of Fermi energy or gate voltage a staircase conductance behavior is observed in

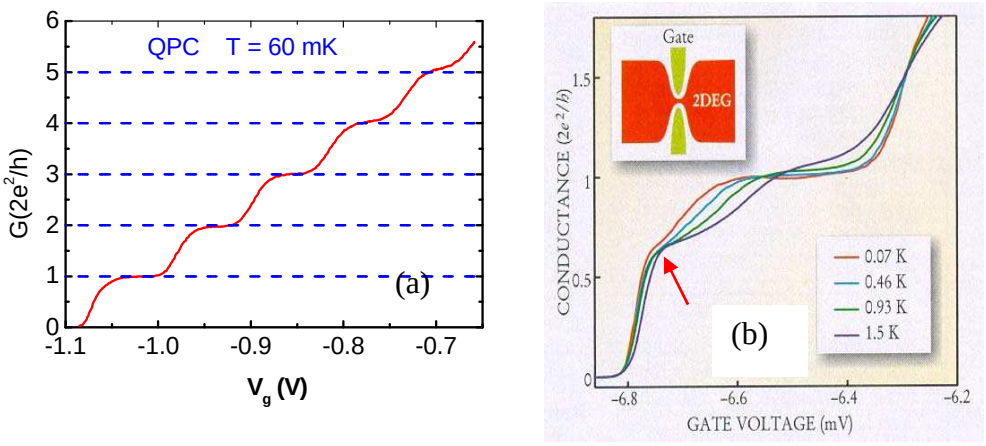
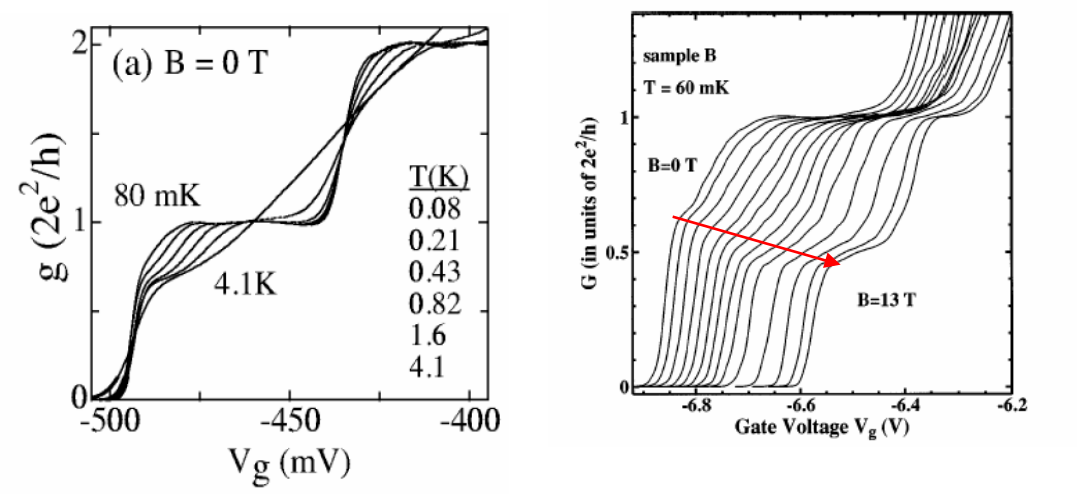


Fig. 2.4. (a**)** Conductance quantization observed in a QPC fabricated on GaAs/AlGaAs Heterostructure in zero magnetic field [50]. (b) The 0.7 Structure observed in a QPC of length 400 nm fabricated on GaAs/AlGaAs hole system in B = 0 [37]. The arrow points to the location of the anomalous plateau.

1D QPC. Figure 2.4(a) shows the conductance quantization in the absence of magnetic field observed in a quantum point contact (QPC) of length 100 nm made on AlGaAs/GaAs heterostructure [50]. After the discovery of the normal conductance quantization in QPC, an additional conductance plateau is observed at G ≅ 0.7 ($2e^2/h$) in 1D systems in many experiments in the absence of magnetic field [37-45]. This anomalous plateau is in general referred as *0.7 structure* (Fig 2.4(b)).

This anomalous conductance plateau (‘0.7 structure’) was first reported in 1996 in a QPC that is realized on GaAs/AlGaAs 2DEG [37]. It is then observed in many GaAs/AlGaAs based short (QPC) and long quantum wires with different geometry and

size [38-45]. This 0.7 structure recently appeared in a QPC made on a two dimensional hole gas (2DHG) [46-48]. It is also found in 1D carbon nanotube [49].



(a) (b)

Fig. 2.5. (a) The temperature dependence of the *0.7 Structure* in an AlGaAs/GaAs QPC of length 500 nm [51]. (b) Evolution of the *0.7Structure* into a $0.5(2e^2/h)$ plateau in parallel magnetic field 0-13T [37]. The arrow indicates the evolution.

To pin down the origin of this 0.7 structure, the evolution of this anomalous plateau in temperature and magnetic field has been thoroughly studied. The evolution of this 0.7 structure with source-drain bias voltage has also been studied. The behavior of the 0.7 structure at different temperatures, observed in different experiments using various quantum wires of different of lengths and sizes, is qualitatively the same. The evolution of this anomaly with temperature is shown in Fig. 2.4 (b) and Fig. 2.5 (a) in a temperature ranged from 70 mK to 4.1 K. The 0.7 anomaly is weak at low temperatures but fully developed at higher temperature, while the normal quantization plateaus disappear as the temperature is raised. *This clearly indicates that the 0.7 structure is not*

associated with ballistic transport. The 0.7 structure shows a strong dependence on the in-plane magnetic field. Figure 2.5 (b) shows the evolution of the 0.7 structure as the in-plane magnetic field is increased. As the parallel magnetic field is increased gradually, the 0.7 structure decreases smoothly to the fully polarized state (Zeeman spin-split state) at 0.5 ($2e^2/h$) [37, 39-41]. Similar behavior of the 0.7 structure in a parallel magnetic field is also reported in the QPC devices created from 2DHG [46, 47].

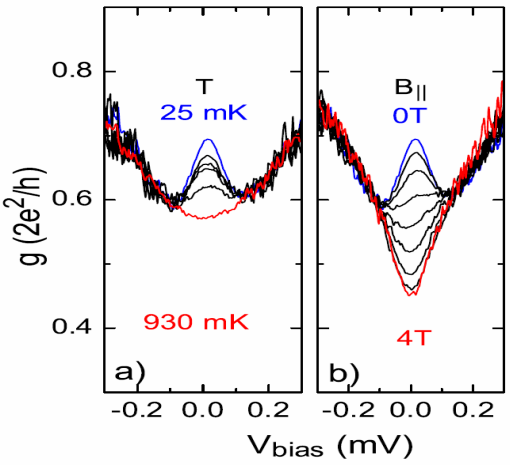


Fig. 2.6. Differential conductance g as a function of source-drain bias voltage observed in hole QPCs made on p-type AlGaAs/GaAs heterostructure: (a) at temperatures 25-930 mK in zero magnetic field. (b) at 25 mK in parallel magnetic fields 0 - 4 T [47].

An interesting feature of the *0.7 Structure* is the behavior of its non-linear differential conductance $g = dI/dV$, where V is the source-drain bias voltage. As shown in Fig. 2.6, a distinct peak is observed around zero source-drain bias voltage at low temperature. The zero bias anomaly (ZBA) decreases as the temperature is increased or related to the disappearance of the *0.7 Structure* as the temperature is lowered (Figs. 2.4(b) and 2.5 (a)).

In some experimental work, a conductance plateau is observed at G = 0.5 ($2e^2/h$) in zero magnetic field [39, 44] on quantum wires fabricated from GaAs/AlGaAs heterostructures with different geometries. The 0.5 ($2e^2/h$) plateau was observed in zero magnetic field along with the 0.7 structure in GaAs quantum wires created on AlGaAs/GaAs heterostructures using erasable electrostatic lithography and a positively biased scanning probe tip [44]. Figure 2.7 indicates that the 0.5 plateau is best defined when the potential is most symmetric and in that situation the 0.7 structure moves toward $2e^2/h$. The 0.7 structure has the same temperature dependence as discussed above. The 0.5 plateau also survives at higher temperature and increases slightly with increasing temperature from 150 mK to 3.0 K. A magnetic field perpendicular to the plane of the

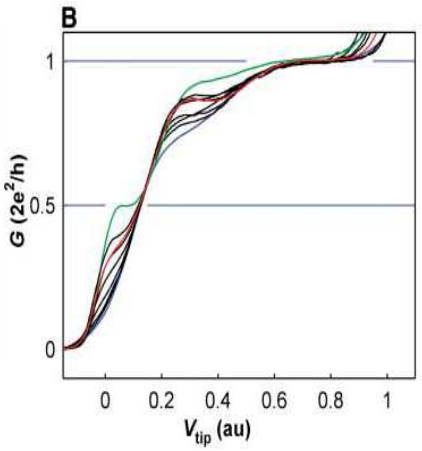


Fig. 2.7. Conductance of quantum-wire device as a function of tip bias voltage at 150 mK for different potential landscapes. The green plot is for symmetric potential landscape. The plots have been offset and linearly scaled along x-axis for clarity [44].

device up to 1.2 T shows no effect on both the 0.5 and 0.7 plateaus. Though in-plane parallel magnetic field has been routinely used to study this anomaly, this is the first time that a perpendicular magnetic field was used.

In a very recent study, a tunable quantum dot has been used to study the *0.7 Structure* [52]. By adjusting the bias voltages of various gates, that form the quantum dot, it is possible to tune on and off the anomaly or to make it continuously evolve into a normal integral conductance plateau. *A small magnetic field of 0.15T applied perpendicular to the plane of the device suppressed the 0.7 anomaly*.

It is noted that the anomalous conductance plateaus have been observed in the range (0.7- 0.5) ($2e^2/h$) depending on the device. In the same device the anomalous feature also depends on the gate bias voltages. In addition, the 0.7 Structure is not a regular feature of the ballistic conductance of QPCs or 1D quantum wires. There are many cases where it is absent.

The experimental observations of the 0.7 structure show the following main features:

(1) The 0.7 structure is feeble at low temperature but becomes prominent at higher temperature (Figs. 2.4 (a) and 2.5(b)). The 0.7 structure exists at temperatures when the normal conductance plateaus disappear due to thermal smearing and indicates *that this anomaly is not related with the ballistic transport*,

(2) In a parallel magnetic field this anomalous plateau smoothly evolved to the Zeeman spin-split plateau at $G = 0.5(2e^2/h)$ (Fig. 2.5 (b)),

(3) The formation of a zero-bias anomaly (ZBA) in the non-linear differential conductance. The ZBA disappears with an increase of temperature in zero magnetic field and also disappears with an increase in applied parallel magnetic field (Fig.2.6), and

(4) These anomalous plateaus do not appear on all devices and very much depend on the bias gate voltages of the device. Hence, this 0.7 structure strongly depends on the details of the lateral confining potential [44, 47, 52]

These experimentally observed features of the 0.7 structure inspired many theoretical models to explain the origin of this anomalous structure. The 0.7 structure disappears with the appearance of the zero bias anomaly (ZBA) peak, which suggests a relation between the appearance of the ZBA and the 0.7 structure. The formation of ZBA and its disappearance as the temperature is raised and in parallel magnetic field are the characteristics of the Kondo effect in quantum dots [53, 54]. The Kondo model is based on local moments or localized spins. But it is hard to understand how this localized spin can form in the open QPC device. Based on the spin-density functional theory (SDFT), it has been shown that a 'dynamical' local moment with a net of one spin forms in the vicinity of the QPC barrier [55]. The Kondo resonance gives rise to a dynamic unpaired spin and should result in *dynamic* spin polarization that cannot lead to static spin polarization that can be detected in low-frequency conductance measurements.

In attempt to explain the 0.7 structure, a semi-empirical model was proposed [56] that considers a spin gap opening up as the electron density in the QPC is increased by adjusting the gate bias voltages. This results in a static spin polarization and a feature near 0.5 ($2e^2/h$) at low temperature is predicted. This model also shows that as the temperature is increased this feature moves smoothly and settles around 0.7 ($2e^2/h$). This explains the temperature behavior of the 0.7 structure. This spin-polarization model was later adopted by others and put on microscopic theoretical grounds using DFT [57]. In this theoretical work [57], two models were considered: (a) with exchange only and (b)

with exchange and correlations. The exchange only model predicts a feature at 0.5 ($2e^2/h$) and suggests a fully spin-polarized ground state. But, in the exchange and correlations model, a metastable state is predicted as soon as the correlation is introduced. This weakens the polarization and as a consequence the conductance rises from 0.5 ($2e^2/h$) toward the normal conduction quantization and manifests the 0.7 structure. As the temperature is raised, the metastable states become thermally activated, and as a consequence, the conductance decreases for a given voltage. This explains the temperature dependence of the 0.7 anomaly. A Green's function technique within DFT has also been used and gives spontaneous spin polarization [58]. The spin polarization models, nevertheless, fail to explain the zero-bias anomaly. Moreover, the well-known theory of Lieb and Mattis [59] forbids spin polarization in the ground state of a 1D system in the absence of magnetic field.

Based on strictly one-dimensional Luttinger liquid (LL) state, a *Wigner-crystal model* has also been proposed to explain the *0.7 structure* and its temperature dependence [60]. In a 1D system the Coulomb interaction becomes prominent with decreasing electron density *n*. In the low density regime, the Coulomb energy dominates over the kinetic energy of the electron and electrons occupy equidistant position in 1D to minimize the Coulomb repulsion. This is known as a 1D Wigner crystal. Therefore, the ground state of a strictly 1D system with low electron density and strong electron-electron interaction is a Wigner crystal. The electrons occupy fixed positions on the Wigner lattice and are antiferromagnetically coupled. The ground state is not thus spin-polarized and is therefore in agreement with the Lieb and Mattis theorem. The low energy properties of the system are described by the Luttinger liquid (LL) theory. The

resistance of the 1D quantum wire is determined by the charge and the spin excitations of the system, $R = R_\rho + R_\sigma$, where R_ρ is the resistance due to charge and R_σ is the resistance due to the spin excitations. At low temperature the contribution of the charge mode is always $R_\rho = h/2e^2$. At very low temperatures when $T << J$, the exchange energy, the spin contribution to resistance vanishes so that the conductance is $G = (2e^2/h)$. At higher temperatures due to thermal activation R_σ grows and at $T >> J$, it saturates at $R_\sigma = h/2e^2$. This theory predicts the conductance anomaly at 0.5 $(2e^2/h)$ but fails to explain the anomaly at 0.7 $(2e^2/h)$. The thermal length, L_T, is inversely proportional to temperature ($L_T \propto \hbar v_F/KT$). Therefore, for a QPC or a short wire the device length, L, is smaller than the thermal length ($L << L_T$) for low temperatures. So, it is difficult to understand how LL theory can be applied to a QPC or a short quantum wire, especially at low temperatures when the thermal length can considerably exceed the device length.

From the above discussion it can be concluded that as of now there has been no satisfactory explanation of the origin of the *0.7 Structure* or other anomalous conductance plateaus. *A complete understanding of the existence of these anomalous conductance plateaus remains elusive*.

The spin-polarization model does, however, deserve a special attention. As it has been stated earlier that, a QPC or a short quantum wire is very likely not a strictly 1D system; hence the theorem of Lieb and Mattis may not be applicable to them. Moreover, a static spin polarization has been experimentally found to be associated with the 0.7 anomaly in a hole QPC [47]. In this work, the authors made use of the large spin-orbit interaction (SOI) in a hole gas. The SOI causes spin splitting of the 1D subband along the direction of the k propagation vector. As a result, carriers with opposite spin travel with

different Fermi momenta and have different cyclotron orbits in external perpendicular magnetic

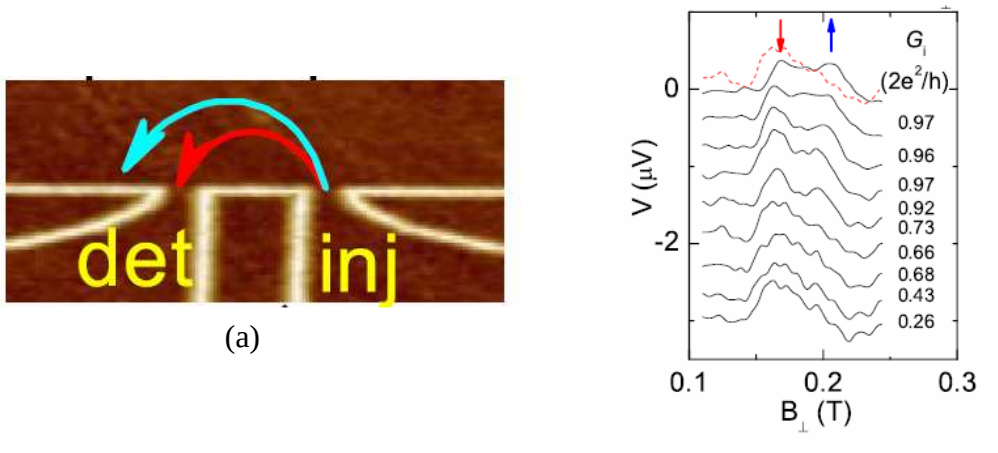


Fig. 2.8. (a) Magnetic focusing geometry showing injector and detector QPCs and the schematic trajectories of holes with two spin states. (b) Focusing peak measured at different injector conductance G_i. The curves are vertically offset by -0.4μV relative to the top one. The $G = 0.66(2e^2/h)$ is also plotted without offset (dashed red) [47].

field. The experiment used two QPCs: QPC1 as the injector and QPC2 as the detector of electrons in a magnetic focusing geometry (Fig. 2.8(a)). A current was injected through QPC1 and the voltage drop was measured across QPC2. The transmission of both the QPCs, QPC1 and QPC2, were set at the conductance value of $G = (2e^2/h)$ and two voltage peaks were observed at two different focusing magnetic fields corresponding to the two spin. One of the peaks slowly disappeared as the transmission of QPC1 was lowered and is shown in Fig. 2.8(b). This allowed a measurement of the polarization of the injected current. A polarization of 40±15% was measured for $G<0.9G_0$. It should be noted that the appearance of the anomalous 0.7 plateau and other similar anomalous plateaus requires an energy spin splitting of

the two spin bands comparable to or larger than the energy level broadening. In cases where this condition is not met, the anomalous plateaus cannot be observed. *The origin of the spin splitting that causes the spontaneous spin polarization remains an unanswered, open question.* Since the anomalous 0.7 structure and other similar anomalous plateaus in the range (0.5-0.7) ($2e^2/h$) can be tuned to appear or disappear by adjusting the bias voltages of the gates that create the potential confinement of the QPCs, it seems likely that *the profile of this confinement plays a crucial role* in this phenomenon.

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Chapter 3

Semiconductor Microstructures and Device Fabrication

3.1 Introduction

An ideal material for use in the study of spintronics is InAs based quantum wells (QW) which have a very large spin orbit coupling (SOC) [3] along with a high mobility in the 2DEG. In this research work, InAs/InGaAs QW structures are used which are grown commercially by Molecular Beam Epitaxy (MBE). Such a QW structure is created by sandwiching a thin layer of low band gap InAs semiconductor between two large band gap InGaAs semiconductors. The electrons are then trapped in the growth direction and are free to move in the other two directions. Such an electron system is known as two dimensional electron gas (2DEG). The 2DEG in the QW structures are characterized by standard Hall and SdH measurements. The 1D devices are fabricated on these QW structures using e-beam lithography and other fabrication processing steps. In the scope of this chapter, we will discuss the MBE growth technique of the QW well structure, formation of the InAs/InGaAs QW structures and the technique for characterizing such QW structures. We will also discuss, in detail, the different steps of the device fabrication. In the last section, we will talk about the fabrication technique of the nano-scale 1D single-QPC and dual- QPC devices.

3.2 Growth of InAs Quantum Well (QW) Structures

The choice of material is very important to work in the area of nano-spintronics. Modern growth techniques, like Molecular Beam Epitaxy (MBE), make it possible to grow semiconductors and several heterostructures with a very high degree of accuracy. MBE grown InAs/InGaAs quantum well (QW) structures are used throughout this research work. In this section, we will discuss the growth technique of semiconductor

heterostructures, the layer sequence of MBE grown InAs/InGaAs QW structures and characterization techniques employed to study QW structures.

3.2.1 MBE Technique

Molecular beam epitaxy (MBE), developed in 1970s [1, 2], is a popular technique to grow compound semiconductors layer by layer with very high precession. In MBE, source material such as Gallium (Ga), Indium (In) and Arsenic (As) are evaporated onto a heated crystal substrate inside an ultra high vacuum (UHV) environment to grow layers of crystals. A schematic of a typical MBE is shown in Fig. 3.1.

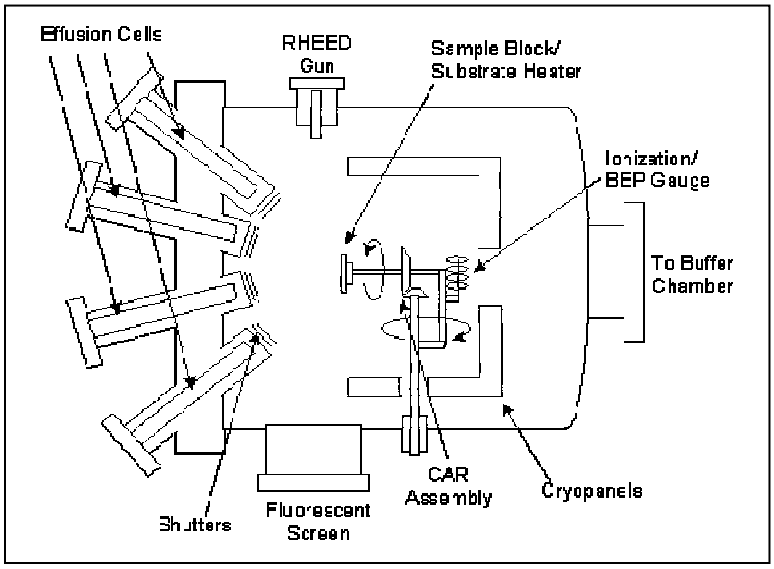


Fig. 3.1. Schematic of a MBE system.

A typical MBE system has three main vacuum chambers: the growth chamber, the buffer chamber and the load lock. The load lock is simply used to load and unload the sample while maintaining a constant vacuum in the growth chamber. The sample is

prepared for growing in the buffer chamber which is also used to store and characterize the sample. Using the load lock, a sample substrate is loaded into the growth chamber where "vapors" from various heated sources are deposited onto the substrate surface and arrange themselves in a crystalline lattice based on that of the substrate. The sample holder is designed in such a way that it holds the sample facing towards each material source. It is also designed in a way to move the sample in a continual azimuthal rotation (CAR) for high quality layer growth. A cryopanel, cooled by liquid nitrogen, is located between the CAR and the chamber wall to absorb residual gases. Cryopumps are also used to remove undesired gases and keep the pressure of the chamber very low ($\sim 10^{-11}$ Pa) and thus ensure that the mean free path of the beam is larger than the geometrical size of the chamber. This condition is vital in order to have a homogeneous film growth. The parts of the MBE system that are heated (e.g. crucibles, sample holder) are made of metals such as Ta, Mo, and pyrolytic boron nitride (PBN) which do not outgas impurities and are chemically stable up to 1400ºC.

The source materials are placed in effusion cells which are heated to a temperature necessary to achieve the desired molecular flux. Only ultra pure materials are used as a source material. The material flux then travels to the heated substrate surface where the deposited material arranges itself to form a crystalline structure. Small variations of the effusion cell temperature can change the beam flux on the order of one percent. Therefore, by changing the cell temperature the growth rate of the compound can be controlled. It is possible to switch on/off the beam flux to within a fraction of a second by closing or opening the shutter in front of the effusion cells. Precise control of crucible temperature and shutter on/off times are needed for well defined layers with sharp atomic

boundaries, such as we require for our InGaAs samples. However, when growing GaAs on a GaAs substrate, we do not require precise regulation of the molecular beam flux since Ga flux has a sticking coefficient of 1 on the GaAs substrate, meaning that all Ga atoms that reach the substrate stick to the surface. On the other hand, As atoms have almost zero sticking coefficient on a GaAs substrate. However, the sticking coefficient of As increases and approaches 1 with the increase of Ga atoms onto the substrate so that depositing a monolayer of Ga onto the substrate will allow the As atoms to stick very easily, permitting us to grow GaAs layers.

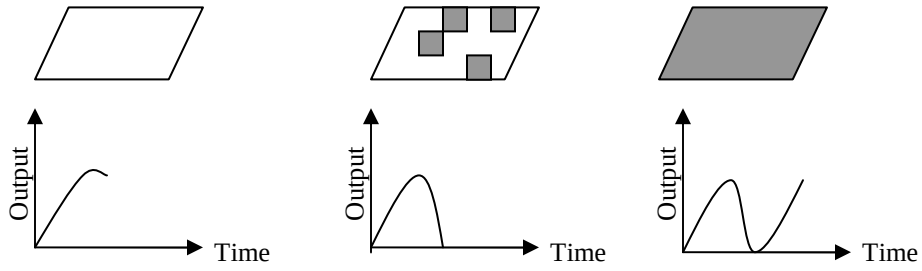


Fig. 3.2. Growth layer detected by RHEED.

One of the useful tools embedded with MBE system is reflection high-energy electron diffraction (RHEED) analyzer which is used to monitor the growth layer. The output of the RHEED starts oscillating with the growth of the layer. At the beginning, when there is no growth, it shows particular output intensity. When the growth is in progress RHEED output intensity starts oscillating and give back the starting intensity pattern when one monolayer of growth is completed. Such a process is shown in Fig. 3.2.

3.2.2 InAs Quantum Well (QW) Structures

Using MBE it is possible to make different heterostructures (such as GaAs/AlGaAs) with a very high degree of precession. It is also possible to grow QW structures (such as InAs/InGaAs) using such epitaxial techniques with high accuracy. To grow a QW structures a thin layer of low band gap semiconductor (e.g. InAs) is sandwiched between two large band gap semiconductors, called barrier layers (e.g. InGaAs), thus constructing narrow quantum well (QW) structures (Fig. 3.3). Electrons trapped into these QWs are restricted to move in the growth direction (i.e. z-direction) but are free to move in the other two directions. Such a system is known as a two dimensional electron gas (2DEG).

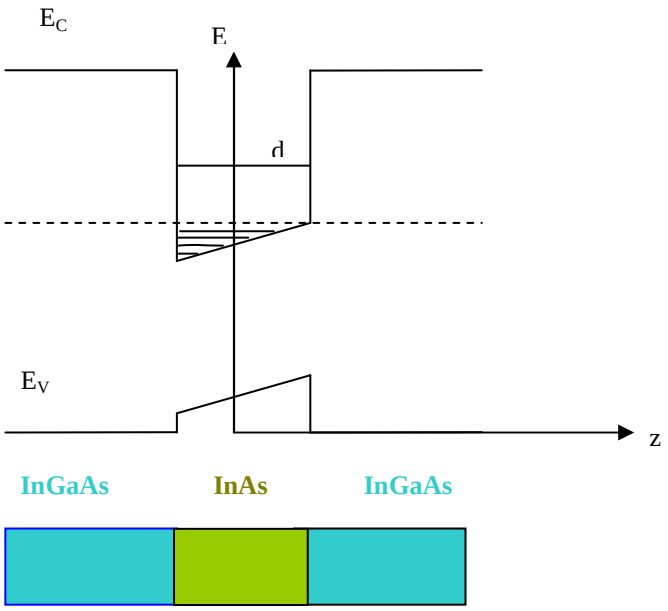


Fig. 3.3. Band Alignment in InAs QW structures.

The energy levels of the QWs can be found by considering a square well potential. The electrons waves are simply standing waves and the lowest energy levels can be written as:

$$E_n = \frac{\hbar^2 \pi^2}{2m_z^*} \frac{n^2}{d^2}, \text{ n = 1, 2, 3…...} \tag{3.1}$$

where n is the quantum numbers designate different levels, d is the thickness of the potential well in z-direction. Electron motion in the other two directions (parallel to the heterointerfaces) is not restricted and the wave function for such electron can be written as:

$$\Psi(r) = f(z)e^{ik_x x + ik_y y} = f(z)e^{i\vec{k}.\vec{r}}, \tag{3.2}$$

and the energy eigenvalues of these electrons are,

$$E_{xy} = \frac{\hbar^2 k_x^2 + \hbar^2 k_y^2}{2m_{xy}^*}. \tag{3.3}$$

Hence, the electron energy in the 2DEG is,

$$E = \frac{\hbar^2 k_x^2 + \hbar^2 k_y^2}{2m_{xy}^*} + E_n, \tag{3.4}$$

where E_n is given by Eq. (3.1) and corresponds to an energy sub-band. The density of states of these 2D sub-bands can easily be obtained using an approach similar to that of 3D electrons. In k-space, the number of states dN between k and k+dk is given as

$$dN = \frac{2 \times 2\pi k dk}{(2\pi)^2}, \tag{3.5}$$

where the extra factor of 2 in the above equation comes to accommodate spin degeneracy of the electrons. Therefore, combining Eq. (3.4) and Eq. (3.5) the density of states is found to be,

$$D = \frac{dN}{dE} = \frac{m_{xy}}{\pi\hbar^2}. \tag{3.6}$$

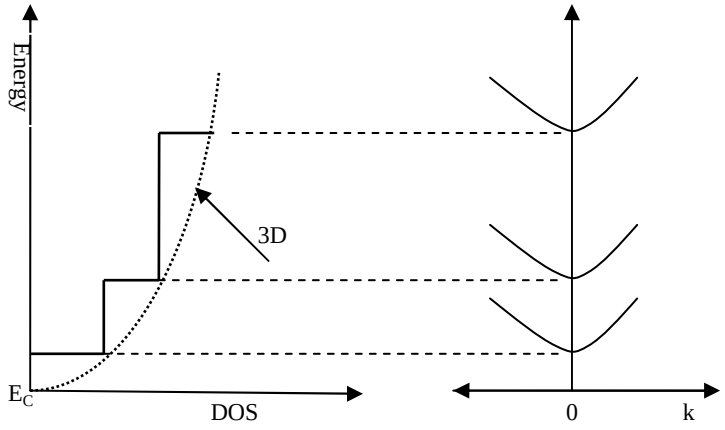


Fig. 3.4. 2DEG density of states.

It is seen from Eq. (3.6) that the density of states of each sub-band depends only on the 2DEG electron's effective mass, a constant for each subband. Total density of states *D (E)* of all the sub-bands is superposition of all these contributions and has a staircase shape, as shown in Fig. 3.4.

3.2.3 Two-Dimensional Electron Gas (2DEG) and its Characterization

The SOC in InAs QW is very large which makes this heterostructure an ideal material to study in the area of *spintronics* [3]. In this study, InAs/InGaAs QWs are used where the 2DEG is formed in the InAs layer. These structures are grown on semi insulating InP substrates by MBE (Fig. 3.5) and are commercially available. The QW structure shown in Fig. 3.5 (a) is obtained from Mark Johnson, Naval Research lab as part of the collaborative effort and the wafer is called a NRL wafer. Figure 3.5 (b) shows the InAs/InGaAs QW structures bought from Intelligent Epitaxy Technology (which we called a Cond.1 wafer). The layer sequences of these QW structures are shown in Fig. 3.5. A thick InAlAs (300 nm) buffer layer is first grown on the substrate to accommodate any

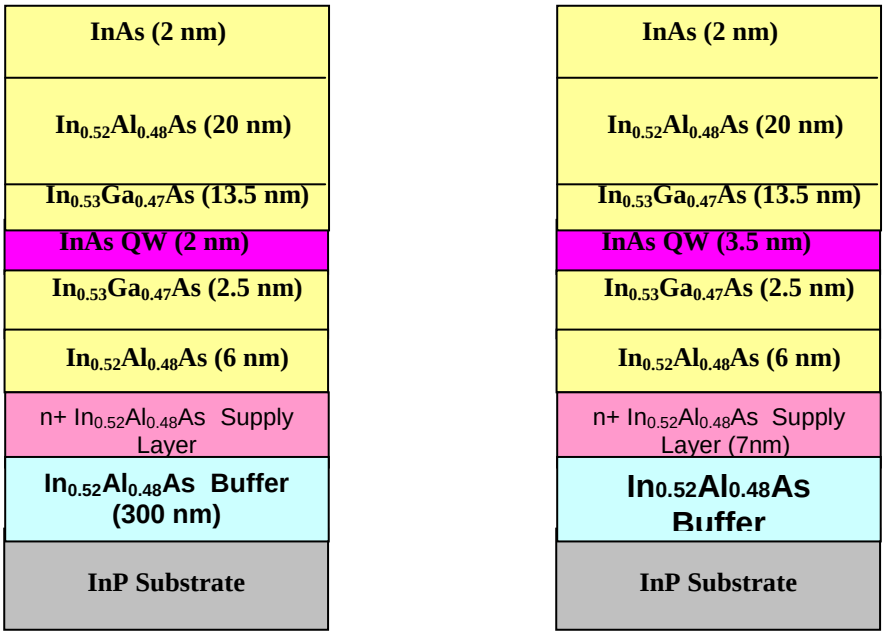


Fig. 3.5. MBE grown InAs/InGaAs QW structure: (a) NRL wafer and (b) Commercially bought Cond-1 wafer.

lattice mismatch. The next layer grown is n-doped InAlAs (7 nm) which is called the supply layer as electrons are supplied to the QW from this layer. To separate this supply layer from the active layers, a 6 nm spacer layer of undoped InAlAs is grown. The 2DEG is formed in the InAs (pink Layer in Fig. 3.5) which is only 3.5 nm thick in the case of Cond.1 wafer (Fig. 3.5 (b)) and 2 nm thick in the case of NRL wafer (Fig. 3.5 (a)) and is sandwiched between two large band gap InGaAs layers. The top InAs layer (2 nm) is called the cap layer which is separated from the active InGaAs layer by 20 nm InAlAs layer. The cap layer prevents the wafer from surface oxidation and/or other physical damages.

Before fabricating the QPC devices, it is very important to characterize the 2DEG in the wafer. By using standard Hall and SdH measurement techniques (described below), commercially grown InAs/InGaAs 2DEG QW structures may be characterized and the electron concentration, n, and mobility, μ, may be calculated.

I. Classical Hall Measurement:

Consider a magnetic field, B, applied perpendicular to the direction of the current (J_x) flow in a conductor. The magnetic field exerts a transverse force ($-ev \times B$) on the charge carriers pushing them to one side of the conductor as shown in Fig. 3.6. Equilibrium is established when the magnetic force is balanced out by the transverse electrostatic force created due to the deflected charge build up along the side. E.H. Hall first described this effect, known as Hall effect, in 1879.

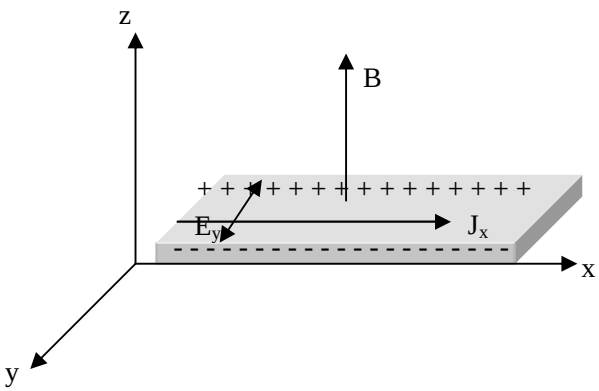


Fig. 3.6. Schematic view of the Hall experiment.

At the equilibrium, the transverse or the Hall voltage is given as,

$$E_y = E_H = R_H J_x B, \tag{3.7}$$

where E_H is the Hall voltage, J is the current density, and R_H is the Hall coefficient. Since $J_x = v_x nq$ and if all the carriers have the same drift velocity, the Hall coefficient is given as,

$$R_H = 1/ne. \tag{3.8}$$

In the classical Hall regime $R_H = dR/dB$, that is, at small magnetic field R_H is the slope of the magnetic field vs. transverse resistance plot (Fig. 3.7 (b)). Therefore, knowing R_H from the plot, it is easy to find the 2DEG concentration, n, using the following relation,

$$n = \frac{1}{eR_H} = \frac{1}{e(dR/dB)}. \tag{3.9}$$

By knowing the 2DEG resistivity, ρ_0, at zero magnetic field, it is easy to find the mobility, μ, of the 2DEG as,

$$\mu = \frac{dR/dB}{\rho_0} \quad . \tag{3.10}$$

At low temperature a 2DEG shows a series of steps in Hall resistance instead of a straight line as in the classical case. According to Klaus von Klitzing [4], winner of the Nobel prize for Physics in 1985 for discovering these quantum steps, this resistance is quantized in steps of h/ne^2, where n is an integer. This phenomenon is now known as Quantum Hall Effect.

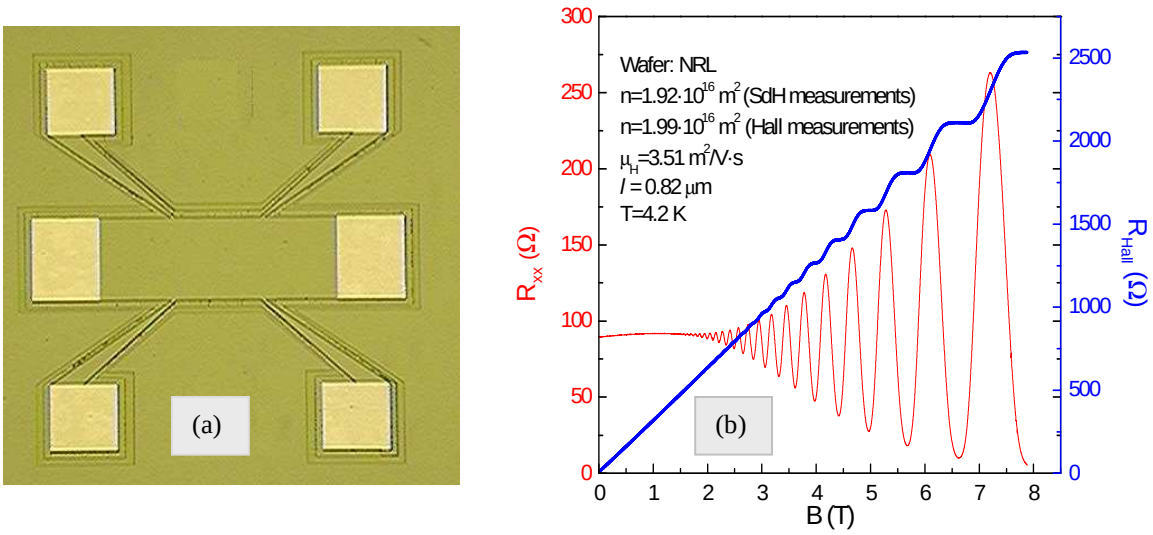


Fig. 3.7. (a) Hall bar device fabricated on InGaAs/InAs QW (NRL) using the Raith 150 e-beam lithography. (b) SdH oscillation observed on InGaAs/InAs QW structures (NRL) as a function of magnetic field at 4.2 K.

II. Shubnikov- de Hass Measurement

At zero magnetic field, the 2DEG electron energy is given by Eq. (3.4) as,

$$E = \frac{\hbar^2 k_x^2 + \hbar^2 k_y^2}{2m_{xy}^*} + E_n .$$

We now consider a strong magnetic field applied perpendicular to the x-y plane. The electron trajectories will be circles about the magnetic field lines with orbital frequency,

$$\omega_C = \frac{eB}{m_{xy}} \ . \tag{3.11}$$

Due to the applied magnetic field, the motion of the electrons in x-y plane is quantized with energy,

$$E_j = \left(j + \frac{1}{2} \right) \hbar \omega_C , \tag{3.12}$$

where j = 1,2,3….. . Hence, the energy levels, E_j, are called Landau Levels (LL) and thus, the total 2DEG electron energy in a magnetic field is,

$$E = E_n + \left(j + \frac{1}{2} \right) \hbar \omega_C . \tag{3.13}$$

At zero magnetic field, the 2DEG density of states for a particular sub-band is step like (Fig. 3.4). In a non-zero magnetic field this density of states splits into several δ-function-like steps, which are separated from one another in energy by $\hbar\omega_C$ (Fig. 3.8). The degeneracy of a LL is given as eB/h, which is proportional to B so that by altering B, both the splitting energy, $\hbar\omega_C$, and LL degeneracy, eB/h, can be changed. In an ideal case, the density of states are a sharp function of energy, but in reality they are broadened due to scattering process (such as phonon scattering) and crystal defects. If the magnetic field is increased, the LLs start moving to higher energies and eventually cross the Fermi

energy level, E_F, which is the maximum energy state for the occupied electrons. Thus, the Landau states are emptied and the electrons find themselves in the next lower level.

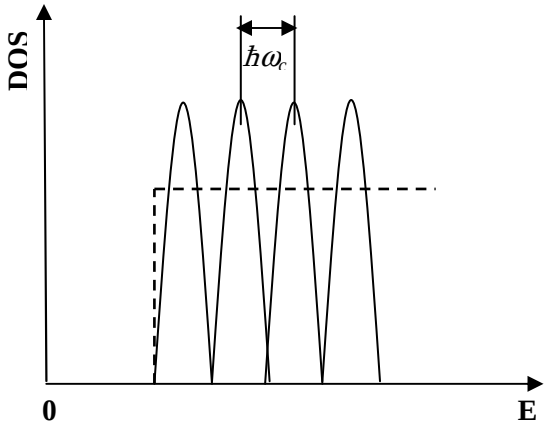


Fig. 3.8. Density of states of 2DEG in the first sub-band in magnetic field. The dashed line is the DOS in the first sub-band without magnetic field.

With increasing magnetic field, the energy increases until the next LL is emptied. This causes an oscillation of the resistivity near the vicinity of E_F known as Shubnikov-de Hass (SdH) oscillations [4, 5].

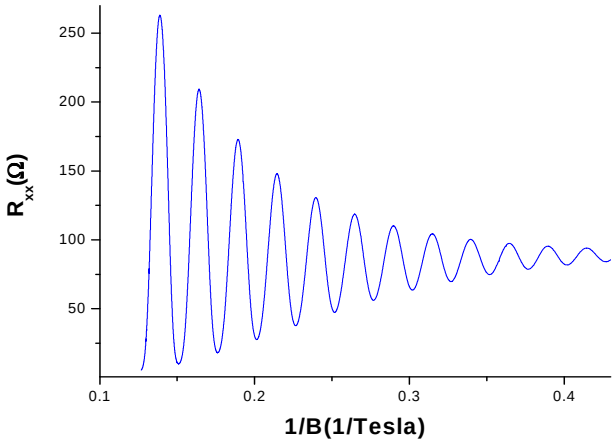


Fig. 3.9. SdH Oscillations are periodic in 1/B.

Interestingly, these oscillations are periodic with *1/B* (Fig. 3.9). The period, $P_{1/B}$, of these oscillations are related to the 2DEG concentration as,

$$P_{1/B} = \frac{hn}{2e} \ . \tag{3.14}$$

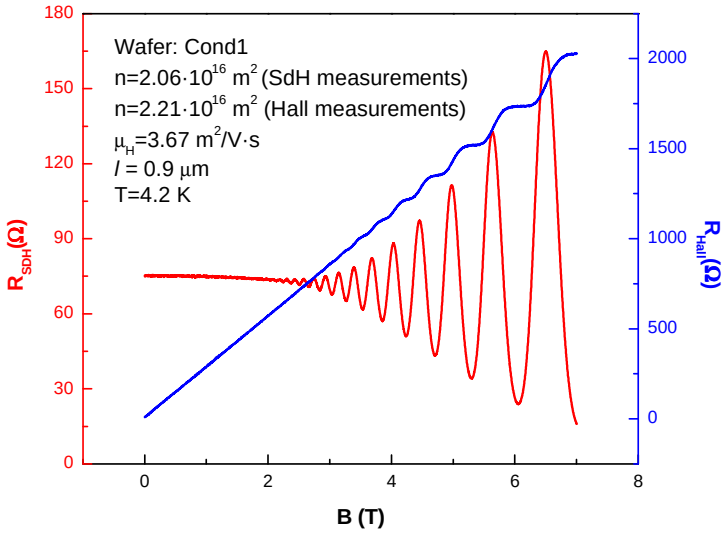


Fig. 3.10. SdH and Hall measurement on Cond.1 wafer.

Table 3.1. Carrier concentration, *n*, mobility, μ and the mean free path, *l* of different wafers used in this research work.

Wafer	T = 4.2 K		
	n (m^{-2})	μ (m^2/V.s)	l (μm)
Cond1-F	2.17×10^{16}	4.14	1.01
Cond1-010	2.21×10^{16}	3.67	0.9
Cond2-F	2.21×10^{16}	3.77	0.925
NRL	1.99×10^{16}	3.51	0.82

Therefore, by knowing the periodicity of the oscillation (Fig. 3.9), the concentration and the mobility of the 2DEG can be calculated. In this research work several InAs/InGaAs samples have been used. We have characterized all these wafers by standard Hall and SdH measurements. Fig. 3.7(b) shows the SdH and Hall measurement plots on NRL wafer and Fig. 3.10 shows SdH and Hall measurement carried out on Cond1 wafer. The carrier concentration, n, the mobility, μ and the mean free path, l of the 2DEG of these wafers calculated from these characterization techniques are shown in Table 3.1.

3.3 Device Fabrication

Micro-fabrication using photolithography is well established and widely used in the industry to make integrated circuits, MEMS, solar cells and many other micro devices [6] while Electron Beam Lithography (EBL) open the door to fabricate nano-structure devices. In both cases, many steps are involved in device fabrication, such as cleaning, spinning resist, etching, metal evaporation, annealing, dicing and bonding. Processes for fabricating devices on GaAs based wafers (e.g. GaAs/AlGaAs heterostructures) are well known [7, 8], but fabricating devices on InAs based wafers is very uncommon and thus extremely challenging. In this section, several fabrication processing steps on InAs based samples will be discussed. All the fabrication steps are done in the clean room environment except for the metal deposition and AFM. A typical fabrication process is shown in Fig. 3.11.

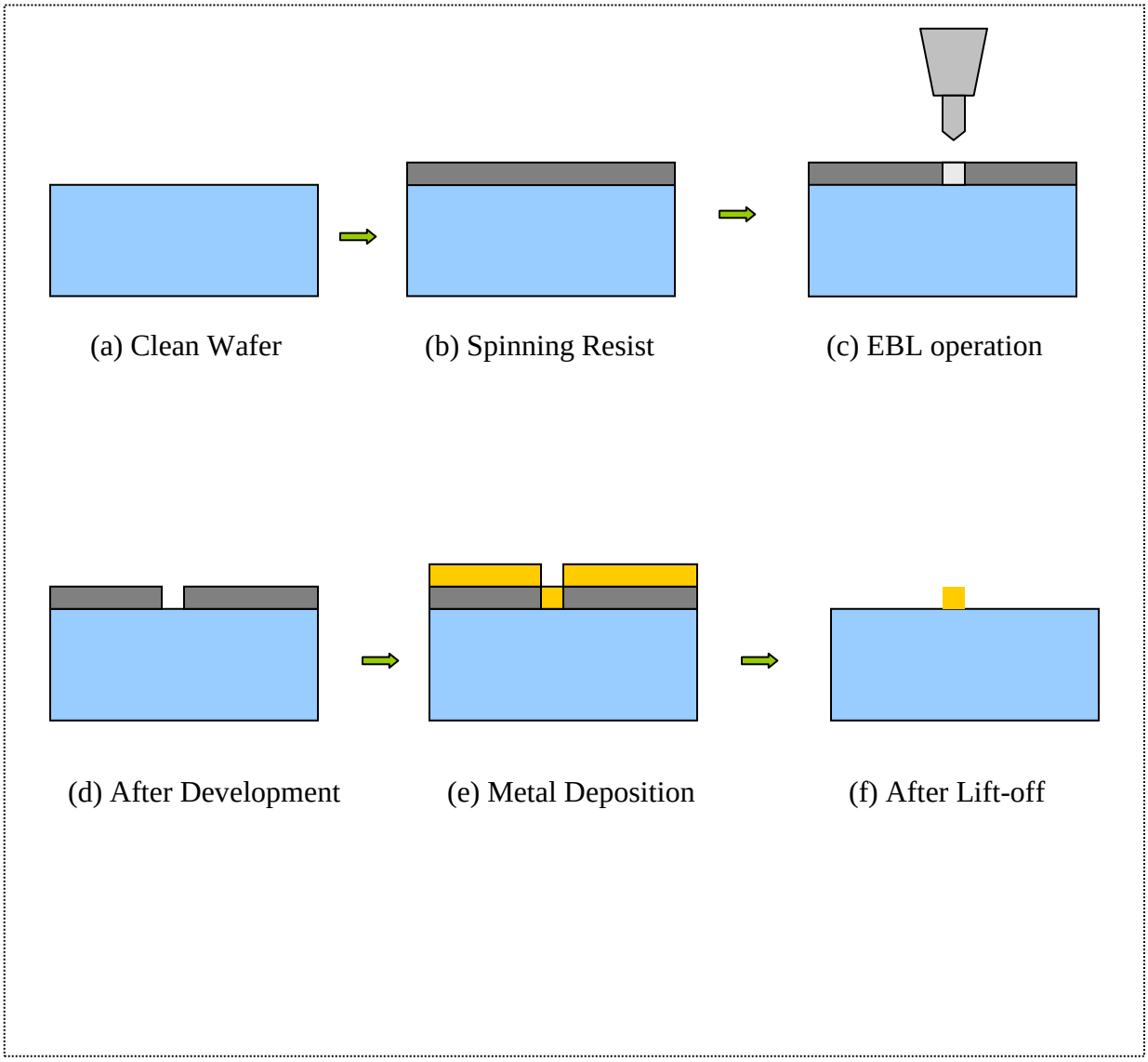


Fig. 3.11. Different processing steps in a typical device fabrication.

3.3.1 Wafer Cleaning

InAs 2DEG wafers are first prepared for device fabrication by cleaning and dicing them into 5mm/5mm pieces using Tempress Wafer Scriber (Model no: 1713-10C sn 1267-C). A single piece is then put into a beaker of warm acetone (~50^0 C) for 15 minutes with the additional assist of ultrasonic bath for 1 minute. It is then rinsed in isopropyl alcohol (IPA) and blown dry using N_2 gas. Cleaning essentially removes all the unwanted dirt particles and resist sitting on the surface and thus ensures the successful fabrication and the reproducibility.

3.3.2 Resist Spinning

Resists are special kind of polymers dissolved into liquids that are sensitive to electrons or ultraviolet light (UV). For electron beam lithography (EBL), typically polymethyl methacrylate (PMMA) resist, dissolved either in Anisole or Chlorobenzene are used. A QPC device has large features (such as metal pads, isolation trench) and small features (Side Gate for QPC). For processing different features different kind of resists with different thickness are used for proper exposure and development. Commercially, PMMA of different concentrations and molecular weights are available [Fig. 3.12] [9]. The thickness of the PMMA can vary by choosing different speeds (rpm) of the coater along with different concentration of the PMMA. Also spinning time can control the thickness of the resist.

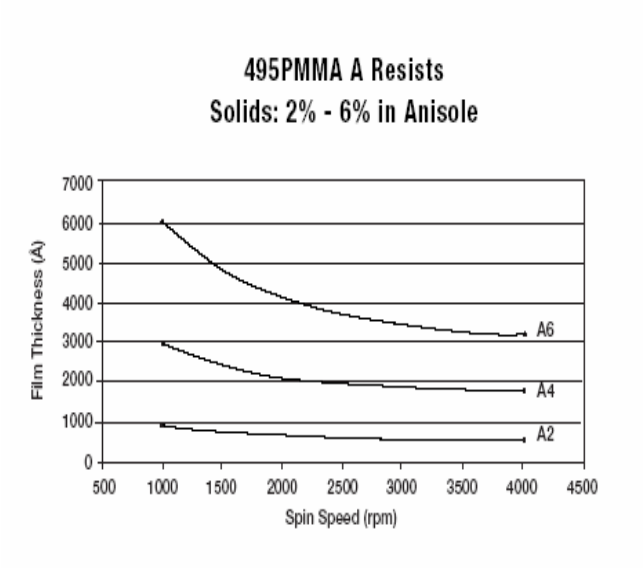


Fig. 3.12. PMMA resist thickness varied with the spin speed as well as with the concentration [9].

For example, the thickness of the 6% PMMA resist dissolved in anisole is 3000 Å when the spin speed is 4000 rpm when the spinning time is 45 sec while keeping all other parameter same, 2% PMMA dissolved in anisole gives a thickness ~1000 Å. For a given concentration and spin speed, the thickness can be varied by choosing different spinning times. In general a larger spinning time defines a thinner resist.

Depending on the fabrication process, monolayer or bi-layer resists with different thicknesses and concentrations are used. For example, for processing an isolation trench a thicker resist (950 4% PMMA dissolved in Chlorobenzene (C4), thickness ~ 2200 Å) is used for 60 sec with 5000 rpm while for a side gate QPC trench a resist thickness of about 800Å is needed. The smaller thickness for the latter processing step helps to get good focus needed for good writing and such thickness is achieved by using 150 2% PMMA dissolved in Anisole (A2) or Chlorobenzene (C2) keeping the spinning speed

4000 rpm for 40 sec. But for processing the pads (metal pads and known as ohmics), bi-layer resists are used for mainly two reasons: to get a larger thickness which is usually equal to or greater than the metal thickness (that will be deposited after exposing and developing) and to get a good undercut while developing. Both of these reasons help to get a good metal lift-off. The first layer that is spun for metal pads is 495 15% PMMA dissolved in Anisole (A15) and is thicker than the second layer which is 495 3% PMMA dissolved in Chlorobenzene (C3). The number 495 defines the molecular weight of the PMMA. Both layers are spun with 5000 rpm speed for 60 sec. The total thickness is found to be greater than 4000 Å.

Table 3.2. PMMA used in different fabrication process.

Process	**Layer**	**PMMA**	**Mol. Weight (× 1000)**	**Spin Speed (rpm)**	**Spin Time (sec)**	**Thick. (nm)**	**Baking Type**	**Baking Time (Sec)**	**Baking Temp. (^{0}C)**
Ohmics	Bi-layer	A 15 + C3	495	5000	60	400	Hotplate	90	180
Isolation Trench	Mono-layer	C4	950	5000	60	150-200		90	180
SG Trench	Mono-layer	C2	150	4000	40	< 90		90	180

The top PMMA layer is thicker and heavier while the bottom layer is thinner and lighter. During the electron beam lithography (which will be discussed in the next section) high energy electrons penetrate both the PMMA layers with small forward angle. But, as the

beam reaches the substrate, it is backscattered with large angles. So, some extra parts in the bottom layer are exposed due to this backscattering. While developing PMMA from the exposed parts are washed away. In the lift-off process, the chemical that dissolved the PMMA can slip through the undercut part of the PMMA and help to achieve a good lift-off. The sample is baked on a hot plate at 180°C for 90s after each spinning. The different resists needed for different processing steps are summarized in Table 3.2.

3.3.3 Electron Beam Lithography

Electron beam lithography (EBL) [10] creates patterns by scanning a beam of electrons across a resist covered sample in order to fabricate patterns as small as few tens of nanometers. A block diagram of a typical EBL system is shown in Fig. 3.13 [10]. The

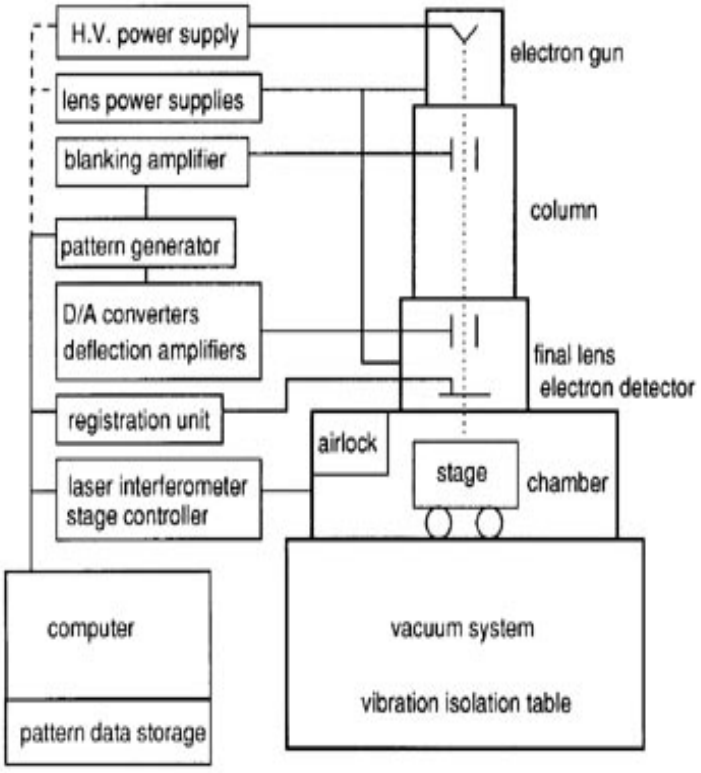


Fig. 3.13. Block Diagram of a typical EBL [10].

electron beam is produced by tungsten tip accelerated with high voltage. There are several sets of magnetic and electrostatic lenses present in the EBL system to collimate and deflect the beam onto the right spot. For a good exposure, the beams need to be focused properly and the aperture as well as the stigmation alignment needs to be corrected.

Raith-150 e-beam writer is used to fabricate all the devices needed in this research project. It works with a Gaussian type of electron beam. The sample covered with resist is loaded into the stage using the load lock for patterning. On the stage the sample is attached with a metal clip. After loading, global coordinate of the sample is defined so that one can write at the exact place on the sample with respect to this coordinate. The beam current is then measured using Faraday cup which is used later to calculate the dose. The beam is then moved to one corner of the sample by recalling the global coordinate. The next step is to prepare the e-beam for patterning by adjusting the focus properly and fine tuning the stigmation and aperture alignment. The focusing is said to be good if a small round spot of ~20 nm diameter can be burnt on the sample. It can then be fine tuned by aperture alignment and stigmation. The write field is usually set as 100 μm. If the pattern is more than 100 μm, then the e-beam needs more than one write field. For the proper matching of the adjacent write fields, an alignment procedure is done before writing using the small burnt spot (~ 20 nm) and the procedure is known as three-point alignment.

After having a good focus and making the three-point alignment, the dose and other parameter need to be set for patterning. The dose is defined as,

$$Dose = Beam\ Current \times Dwell\ time,$$

where dwell time is the time for exposing one point. By making several test patterns the dose for big patterns is set as 215 $\mu C/cm^2.s$ when 60 micron aperture is used along with 10 KV accelerating voltage. Aperture, that control the beam current, is an important parameter for exposing a pattern and in general the bigger aperture defines small writing time. Therefore, for writing big features 60 micron aperture is used to minimize the writing time. One disadvantage of higher aperture is that the sharp corner of the feature is rounded off and known as proximity effect. This rounding off usually happen due to the large angle backscattered electron from the surface. The forward electron beam that is penetrating the resists has high energy and small scattered angle. But when it reaches the semiconductor surface it creates low energy backscattered electron that cause the proximity effect. One way to minimize this problem is to use high energy electron (i.e. using higher accelerating voltage). The step size (minimum incremental interval) is another important parameter which then needs to be set so that areas can be exposed using raster scanning (vertically oriented beam moved through regular modes). Usually the step size is kept $1/10^{th}$ of the minimum feature size. If the step size is comparable with the feature size the sharp corner of the feature can not be patterned properly. For small patterns 7.5 micron aperture is used along with smaller dose (~100 $\mu C/cm^2.s$) keeping the accelerating voltage as 10 KV. Setting all the parameters, the design of the pattern (created by GDSII editor) is then recalled from the list and set the position coordinate to write the pattern with respect to the global coordinate.

3.3.4 Development

The device is patterned by exposing the PMMA by electron beam during the EBL. The cross-linking of the exposed part of PMMA becomes weak during such exposure. Development is the process by which the exposed part of the PMMA is removed chemically. The chemical mixture that is used to develop is called as **developer**. To develop InAs based samples, mixture of MIBK (methyl iso-butyl keton) and IPA (Iso- propyl Alcohol) with the ratio of MIBK: IPA: 1:1 is used as a developer. For developing big features patterned on InAs wafer (pads and isolation trench) the development time is 60 seconds while for small features (SG trench) the development time is 50 seconds.

3.3.5 Ohmics and Markers: Deposition and Lift-off

The first EBL operation is markers and ohmics. Markers are usually a cross structure which are used for the alignment in the overlay exposure. Ohmics are each 200 μm × 200 μm feature (pads) on which different layers of metals are deposited after EBL operation and used as source/drain, voltage probes as well as gate pads (controlling bias voltages). Usually, bi-layer resists are used for writing ohmics and markers. Typically, A15 resist (15% PMMA with 100 K molecular weight on Anisole) is spun as the bottom layer with C3 (3% PMMA with 495 K molecular weight on Chlorobenzene) as a top layer. The bilayer is used to get a large thickness of resist and to get a large undercut during the development process which in turn helps to get a clean lift-off.

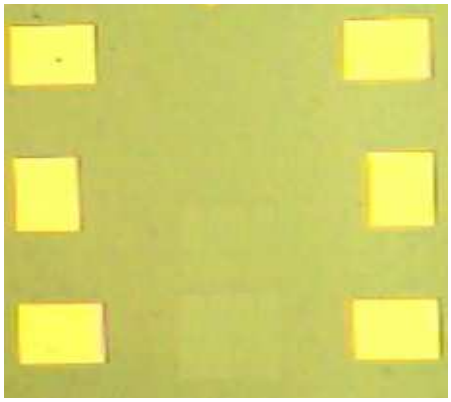


Fig. 3.14. Ohmics after Lift-off.

The deposition system (Cooke Vacuum Products, CVE-600-EB-FR-S-DC) has a Temescale four pocket e-gun and a resistive boat. So without breaking vacuum one can deposit five different types of metals. High vacuum (~8×10^{-7} Torr) is created before deposition. Different types of alloys and metals with different thicknesses are used on InAs based wafers to get good ohmics [12, 13, 14]. Three types of metals are used for ohmics and markers in the devices that are fabricated on InAs/InGaAs wafer and used in this research work. The metals used in the ohmics are **Ni 12 nm, Ge 20 nm and Au 400 nm.** Among those, **Ni** is used to adhere to the semiconductor surface and **Ge** has a smaller molecular size which is diffused while annealing. And **Au,** the thickest layer, is also diffused to ensure a good ohmic contacts as well as to provide the surface for bonding. The deposition rate for different metals are different, such as, for Ni and Ge the deposition rate is 2 Å/Sec while for the Au the deposition rate is 10 Å/Sec. Ni and Ge are deposited using e-gun evaporator while Au is deposited using the resistive boat. The ohmic recipe is summarized in the Table 3.3.

Table 3.3. Ohmic Recipe

Layer	**Metal**	**Thickness (nm)**	**Deposition Rate** (Å/Sec)	**Current (mA)**
1	Nickel (Ni)	12	2	65
2	Germanium (Ge)	20	2	55
3	Gold (Au)	400	10	120

After metal deposition, the sample is dipped into warm acetone which removes the PMMA as well the metal from the unexposed area (Fig. 3.14). Typically, the acetone temperature is kept at **~70 ^{0}C** and the sample is dipped into acetone for **15 minutes**.

3.3.6 Etching

Chemical etching is used to remove part of the sample layers from the wafers. The wafer is patterned by EBL and developed, leaving the exposed surface free of resist. Wet or dry etching is then used to remove layers from the exposed part of the wafer. For InAs based wafers, the etching process is not well established and it is extremely difficult to control. Both dry and wet etchings are possible for InAs based wafers [15-19]. The dry etching offers a better width to depth aspect ratio. That is, during dry etching the lateral etching is much smaller compare to the wet etching. But, the main disadvantage of the dry etching is that the walls of the trenches are not smooth. The wet etching gives a smoother trench wall. Thus, we have chosen wet etching over dry etching. Only the wet etching is involved in this fabrication process.

I. Isolation Trenches

Devices are isolated from the rest of the wafer or from other devices on the wafer by etching an isolation trench into the 2DEG layer sequence. Isolation trenches are patterned by EBL on the wafer covered by C4 resist (4% PMMA with 950 K molecular weight on Chlorobenzene). It is then developed and patterned parts are free of resist which allows the chemicals to attack the surface.

Phosphoric acid based [16] or Acetic acid based [17] et chants are usually used for chemically etched InAs and InAs based wafers. An acetic acid based etchant is used to etch the InAs/InGaAs wafer, whose structure is shown in Fig 3.5. The recipe of which is Acetic Acid: H_2O_2: H_2O: 15:20:125. It etched the InAs portion very fast (~5nm/s) but the etching process slows down with the presence of other atoms (like Al or Ga) in InAs.

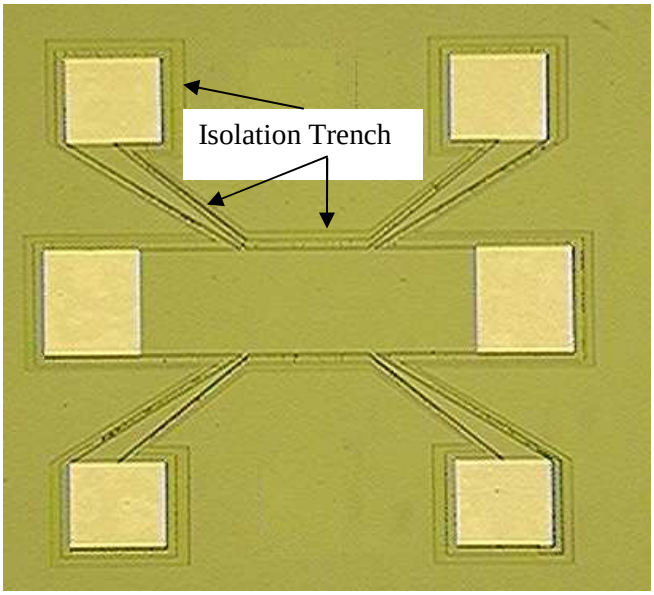


Fig. 3.15. Isolation Trench defines a Hall bar Device.

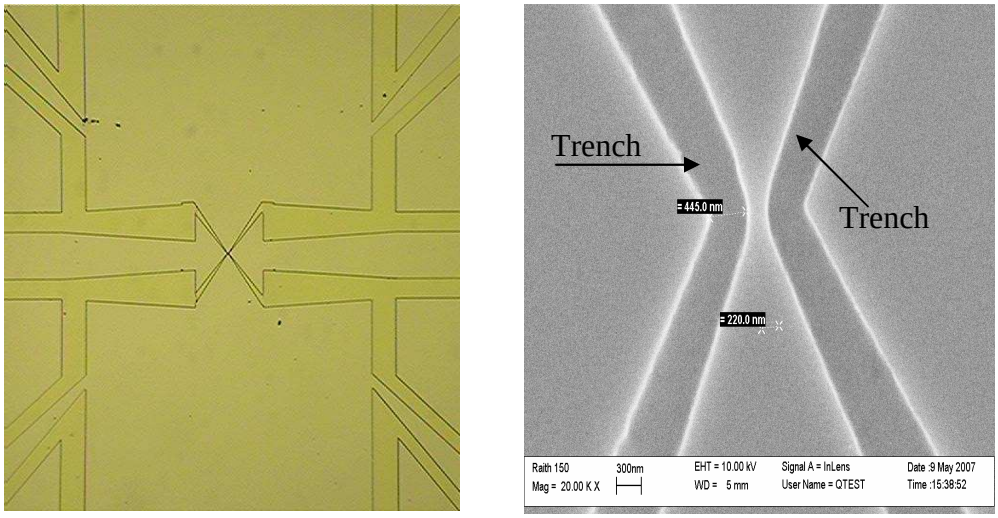
Table 3.4. Etching recipe for InAs/InGaAs wafer shown in Fig 3.5.

Wafer	**Etching**	**Etchant**	**Rate (nm/min)**	**Time (Sec)**
InAs/InGaAs (Fig 3.5)	Isolation Trench	**Acetic Acid (15): H_2O_2 (20) :H_2O(125)**	80	120
	Side gate Trench			67

In Fig. 3.5, it is shown that the InAs 2DEG is 35 nm deep from the surface. Therefore, for good isolation, one needs to etch below the 2DEG. In practice, we etch down to buffer layer to avoid any leakage, otherwise the devices will not be isolated from each other and from the rest of the wafer completely. The overall etch rate is about 80 nm/min. A typical Hall bar device is shown in Fig. 3.15 which is defined by cutting the isolation trench. The recipe for etching the isolation trench is summarized in Table 3.4.

II. Side Gate Etching

A side gate is simply a piece of 2DEG bordered by isolation trenches. Since it is difficult to make non-leaky Schottky gates on InAs, side gates are used to create the 1D devices. Side gate (SG) etching is similar to the isolation etching but requires better control. With the precise control of time and etchant, it is possible to keep the trench



(a) (b)

Fig. 3.16. (a) Optical micrograph of trench of a Side Gated (SG) QPC fabricated using the Raith 150 e-beam lithography. (b) SEM image of QPC trench.

width and depth at desired level. The etchant used to realize the SG trench is the same as depicted in the previous section but the etching time is 67 seconds. The depth of the trench is found to be ~ 100 nm (Fig. 3.16). The use of side gates offers a number of advantages: (1) It is fairly straightforward to create a side gate using e-beam lithography; (2) there is no need for metal deposition and lift-off are needed for conventional gates; and (3) the shape of a side gate can be easily defined. The recipe for the side gate trench is shown in Table 3.4.

3.3.7 AFM

Atomic Force Microscopy (AFM) is a powerful form of scanning probe microscopy (SPM) that performs its imaging function by measuring a local property of the surface being inspected, such as its height, optical absorption, or magnetic properties. An AFM has a cantilever tip that touches the surface while scanning (raster scan). A repulsive ionic force from the surface causes the cantilever to bend and the deflection is detected by a detector and gives the profile of the surface [20, 21]. This type of measurement is called the contact mode and the resolution of the imaging depends on the tip length and radius. A very good tip has a length of 5-10 μm with the radius being 10 nm. Using an AFM, a typical image is collected over a period of ~ 30 s, but now it is possible to obtain an image in less than 20 ms [21].

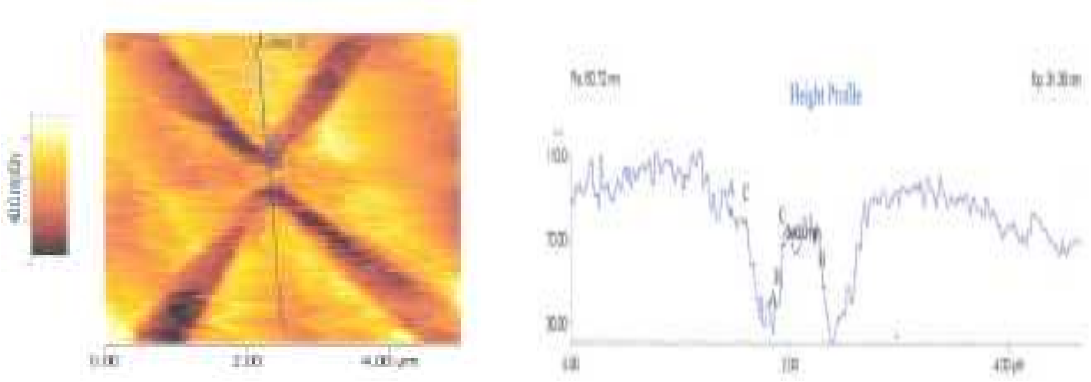


Fig. 3.17. AFM image of a quantum point contact (QPC) device and depth measured by using the AFM.

A Veeco CP-II AFM is used in this fabrication process to scan the devices to determine the depth and the width of the isolation trench. Most importantly, the AFM gives the width and depth of the SG trench of the QPCs as well as the QPC channel width. Fig 3.17 shows a typical image and the scanning profile of a QPC device.

3.3.8 Annealing

Annealing is a heating process through which the metal in the ohmics thermally diffuses into the semiconductor in order to make a good ohmic contact with the 2DEG. It is relatively easy to anneal metal on InAs based wafer as it has very small Schottky barrier. In this fabrication process, a rapid thermal annealing (RTA) system (A G Associates, Heatpulse 210T RTA) is used. For short annealing times (1 sec to 5 min) RTA is very useful. The RTA gives the facility to anneal in a wide range of temperature from 300°C to 1100°C. For the Ohmics in our case, the RTA is done at **350°C for 60 s**.

3.3.9 Scribing, Packaging and Bonding

The final step for device fabrication is to cut the 5mm×5mm wafer into two small units using a Tempress Wafer Scriber (Model no: 1713-10C sn 1267-C). Each unit usually has two devices. One of these units is then glued to chip carrier using GE varnish.

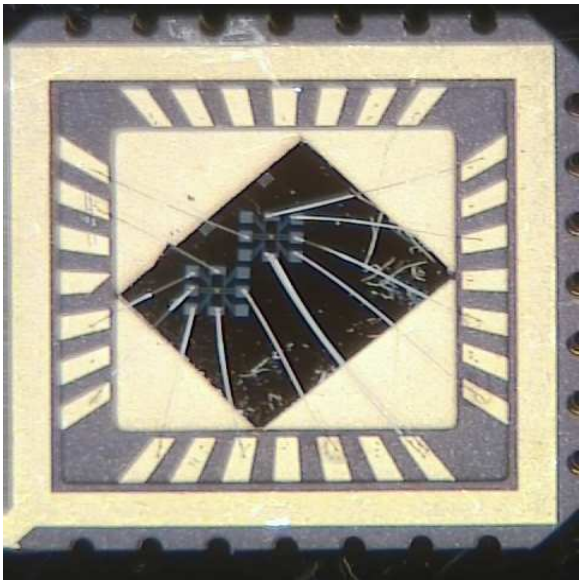
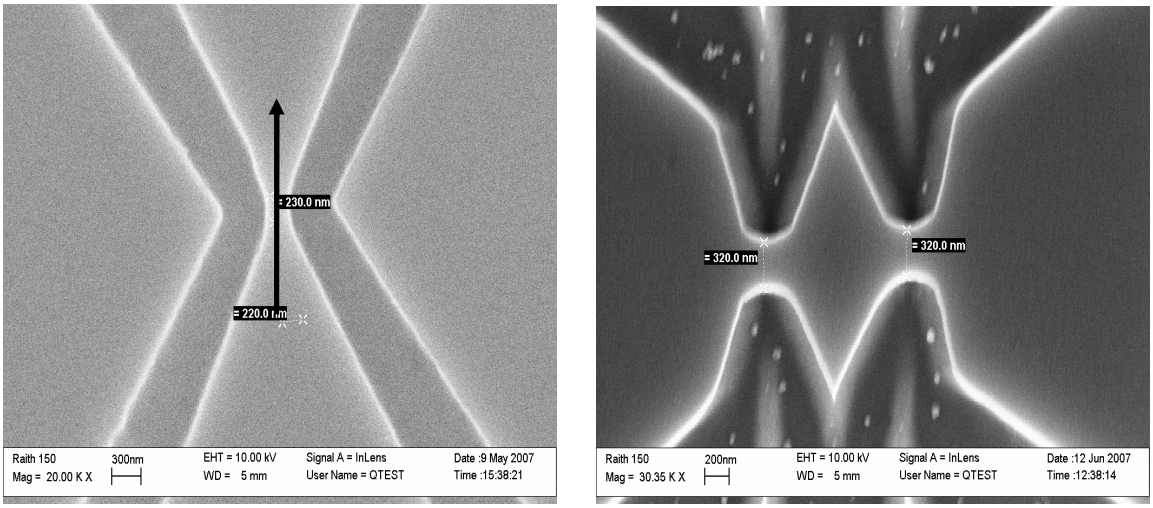


Fig. 3.18. Device glued and bonded in the chip carrier.

It takes usually one hour for the glue to dry. Ohmic and Gate pads are then bonded with the chip carrier using a bonder made by Kulicke and Soffa. Usually, an Au or Al wire is used for bonding. In Fig. 3.18, a complete device bonded with a chip carrier is shown.

3.4 Nano-Scale QPCs

Fabrication of 1D nanoscale devices on InAs/InGaAs quantum well structures is very challenging. In the last two sections, we have discussed the growth technique of the material and the characterization needed for this work, along with different fabrication steps. In this section we will discuss the devices made on InAs/InGaAs QW structures. In order to study lateral SOC in 1D systems, we have fabricated 1D QPC devices on such QW structures since it has large SOC. We have fabricated both single-QPC and dual-QPC devices on such structures.



(a) (b)

Fig. 3.19. **(**a) SEM of a Side Gated (SG) single-QPC and (b) SEM of a dual-QPC device fabricated on InAs/InGaAs QW structures using the Raith 150 e-beam lithography.

3.4.1 Single-QPC Device

A single-QPC device fabricated using EBL by the Raith 150 e-beam has a Hall bar geometry. QPC devices of different dimensions as well as with different orientations on InGaAs/InAs QW structures are fabricated. Usually, a single-QPC device has two contact pads (ohmics) for source and drain, four contact pads (ohmics) for voltage probes and two Ohmics for gates. The QPC or the active part of the device is patterned at the center of the Hall bar and are created by a pair of side gates (SG) defined by isolation trenches cut by wet etching. Fig. 3.19 (a) shows the SEM image of a QPC device which has a length of the order of 100 nm. The width of the channel is ~ 200 nm. By applying a negative bias voltage to the SG, a 1D conduction channel is created. The arrow shows the direction of the channel.

3.4.2 Dual-QPC Device

Dual-QPC devices are also fabricated on InAs/InGaAs QW structures by EBL on which there are two QPCs in series (Fig. 3.19 (b)) at the center of a longer Hall bar. Each QPC is crated by a pair of SG defined by wet etching. Separation between the two QPC is kept less than a micron (less than the mean free path of electron). There are four gate pads to control these two QPCs independently. By applying the gate voltages to the corresponding gate pads, it is possible to narrow the width of the channel without affecting the other gate and vice versa.

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Chapter 4

Experimental Techniques

4.1 Introduction

All the measurements involved in this dissertation are low noise transport measurements done at low temperature. The *ac* measurements (f = 33 Hz) have been carried out by the standard lock-in technique. Most of the experiments are done at liquid helium temperature (4.2 K) but some of the experiments are carried out at mK temperatures which are achieved by a dilution refrigerator. In this chapter, we will discuss the operating principle of the dilution refrigerator and the details of the measurement techniques.

4.2 Dilution Refrigerator

Dilution refrigerator uses a mixture of ^{3}He and ^{4}He gases to achieve a temperature as low as 2mK [1]. It is an essential tool for ultra low temperature measurements in research laboratories. In 1951, H. London proposed to use only ^{3}He gas in the refrigerator to cool down to well below 4.2 K. The ^{3}He gas was simply pumped out to reach the lowest temperature which was 0.3 K. But, in 1962 H. London proposed a refrigerator that used ^{3}He/^{4}He for refrigeration and in 1965 the first ^{3}He/^{4}He dilution refrigerator operated down to 0.22 K [5]. Dilution refrigerators are now available commercially which can operate between the 2mK to 1K. In this research work, a MINDIL-OD70- 30mK dilution refrigerator manufactured by Air Liquide is used. The principle and the operation of the dilution refrigerator will be discussed in the following sections.

I. Principle of the Dilution Refrigerator

When a mixture of ^{3}He and ^{4}He is cooled below a critical temperature of 0.86 K, the liquid separates into two phase: one phase is rich in ^{3}He and the other in ^{4}He (Fig. 4.1). The density of ^{3}He is lower than ^{4}He which makes the ^{3}He-rich lighter 'concentrated phase' float on the ^{4}He-rich heavier 'dilute phase'. As the temperature, $T \rightarrow 0$, the lighter concentrated phase becomes pure ^{3}He. On the other hand, the ^{4}He-rich heavier dilute phase is almost 94% ^{4}He with the remaining 6% ^{3}He. This finite concentration of ^{3}He, even at very low (~ 0 K) temperature (Fig. 4.1), plays a crucial role in the dilution refrigerator mechanism. The lighter concentrated phase of ^{3}He can be considered as

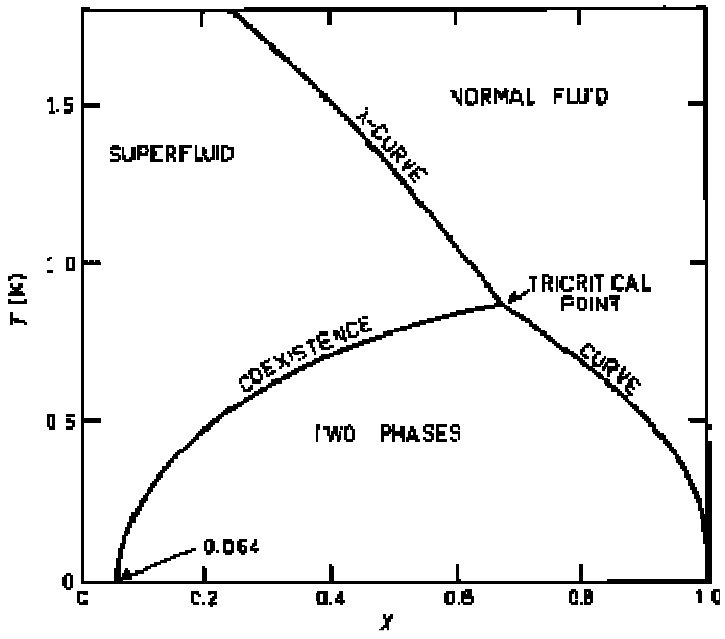

Fig. 4.1. The phase diagram of a liquid helium mixture as a function of the percentage (x) of ^{3}He in the mixture. Phase separation takes place when temperature is below the tri-critical point ~ 0.86 K.

liquid whereas the heavier dilute phase (94% ^{4}He with 6% of ^{3}He dissolved in it) can be considered as the "vapor" phase of ^{3}He. It is thus possible to obtain cooling by continuously moving ^{3}He atoms downward from the concentrated phase to the dilute phase – which is equivalent to the evaporation technique used in *evaporation refrigerator*.

II. Operation

A schematic of the MINDIL-OD-30mK Air Liquide dilution refrigerator is shown schematically in Fig. 5.2. The mK cooling occurs at the mixing chamber where mixture of ^{3}He and ^{4}He separates into two phases: the bottom layer is ^{4}He rich (~94% ^{4}He and ~6% ^{3}He) and the pure ^{3}He layer float on the ^{4}He rich layer. Cooling is achieved by transferring ^{3}He atoms continuously from ^{3}He rich phase to the dilute phase (~94% ^{4}He and ~6% ^{3}He). After each circulation, the temperature is lowered when the ^{3}He moves from high pressure area to low pressure region. The continuous circulation of ^{3}He is done by a pump that operates at room temperature. For operating a dilution refrigerator continuously, it is necessary to provide a condenser at 1-2 K to liquefy the room temperature gas entering the refrigerator. When the refrigerator begins operation, a ^{4}He pot at about 1 K is used to condense the ^{3}He-^{4}He mixture in the dilution unit. It does not cool the mixture sufficiently to form the phase boundary but simply brings it close to 1K. But the condensation of ^{3}He/^{4}He mixture in MINDIL-OD-30mK dilution refrigerator is not obtained in a usual 1K pot. Instead the condensation is done after pre-cooling in the Joule-Thomson stage by a compressor which is located behind the pump (Fig. 4.2).

Further cooling takes place at the still (kept at ~ 0.75 K) where the incoming mixture is cooled by the still before it enters the heat exchangers and the mixing chamber. Phase separation takes place below the tri-critical point of ~ 0.86 K. The relative volumes of the components of ^{3}He-^{4}He mixture are determined in a way so that the phase boundary occurs inside the mixing chamber and the overall liquid surface lies in the *still*. They are calculated from the known volumes of the heat exchangers and the mixing chamber.

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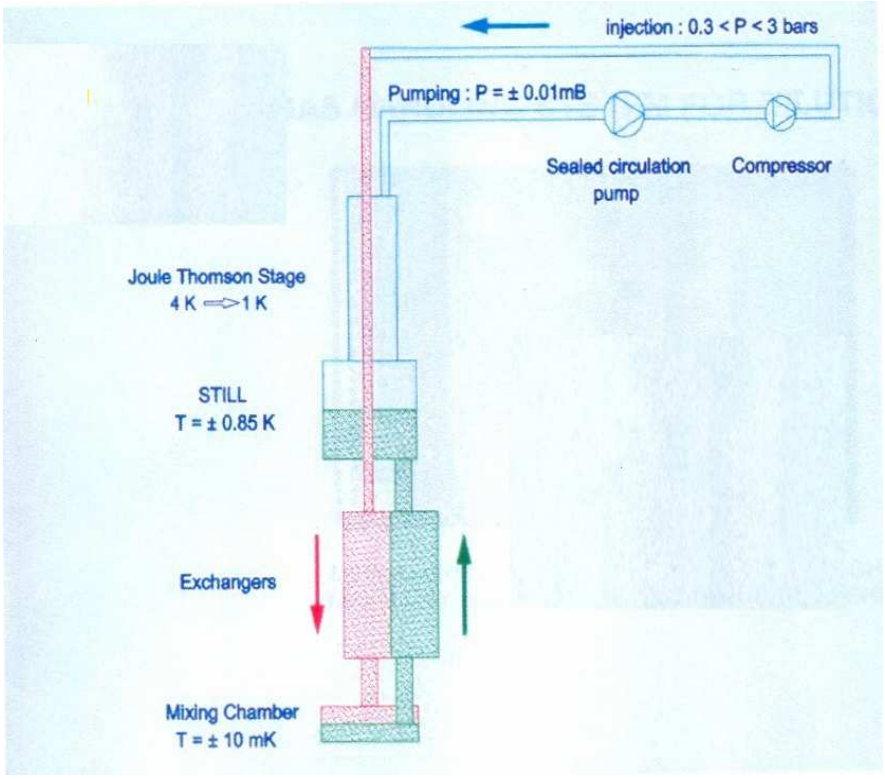


Fig. 4.2: Schematic of a MINDIL-OD70- 30mK dilution refrigerator.

During continuous operation, ^{3}He has to be removed from the dilute phase and re-supplied to the concentrated phase. This is done by pumping away ^{3}He from the liquid surface in the *still*, where at 0.75 K ^{3}He evaporates preferentially (Fig. 4.2). The evaporating ^{3}He are pumped through a room temperature pump and compressed before passing it through an impurity-removing cold trap (at 77 K) and returning it to the cryostat. The condensation of ^{3}He is then achieved by using the compressor. The ^{3}He then enters the *still* heat exchanger at about 0.75 K and passes through several other main heat exchangers before entering the mixing chamber. Heat exchangers are mainly small diameter coaxial tubes with the inner tube used to carry the compressed ^{3}He returning to the mixing chamber whereas the outer tube carries the ^{3}He leaving the mixing chamber

In the mixing chamber the ^{3}He atoms, due to an osmotic pressure gradient, crosses the phase boundary and proceeds in reverse order through the outer tube of the heat exchangers, all the way up to the *still* where the liquid column ends. The process thus continues in a cycle while creating low temperature in the mixing chamber. The sample chamber is placed very close to the mixing chamber with proper thermal contact to have a temperature as low as possible for measurements. The dilution refrigerator used in this research work is made by AIR LIQUIDE (Model: MINDIL-OD70-30mK) and the lowest temperature achieved by this refrigerator in our lab is 22 mK.

4.3 Experimental Setup

Most of the experiments presented in this dissertation are done at liquid Helium (LHe) temperature, i.e. at 4.2 K using a standard LHe cryostat. Some of the experiments

are performed at mK temperature using the MINDIL-OD70-30mK insert and AIR LIQUIDE dilution refrigerator. The Dewar can be adopted for both the MINIDIL and LHe insert.

A superconducting magnet is fixed into the Dewar which can provide a magnetic field up to 8 T which is powered by an AMI model 420 (manufactured by American Magnetics Inc) magnet power supply system. It can provide a magnetic field in both positive (+ z direction) and negative (- z direction) direction. The sample in the MINIDIL insert is placed at the holder that has a fixed plane perpendicular to the magnetic field direction. The LHe insert has two sample holders: in one orientation the sample is perpendicular to the magnetic field and in the other the sample is parallel to the magnetic field. The LHe insert used in the experiments is very simple[1]. This insert has a supporting

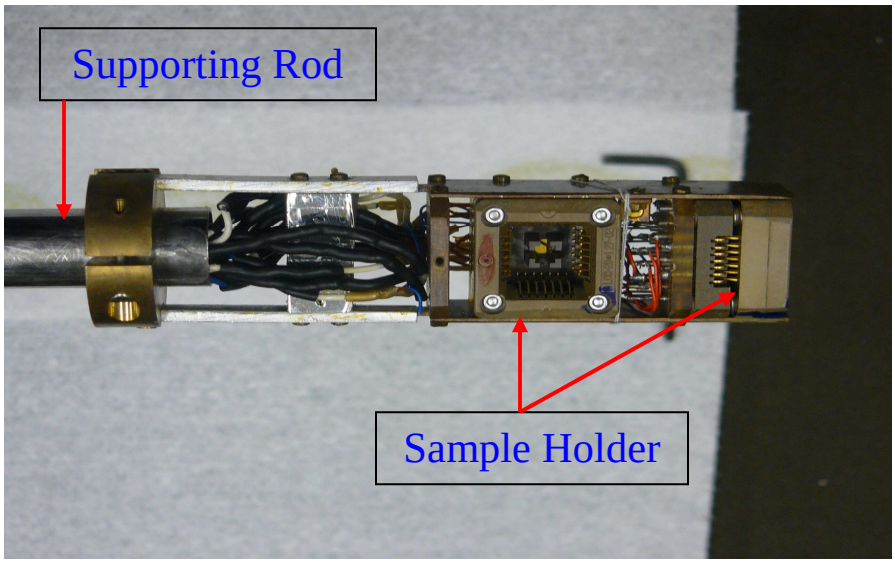


Fig. 4.3. Bottom part of the LHe Insert.

[1] Designed and fabricated at CEA, Saclay, France.

rod, two sample holders and a 12 pin connector for making the electrical connection with sample. The two sample holders are perpendicular to each other. Therefore, samples can be experimented on both in parallel and perpendicular magnetic field just by switching the sample position (Fig. 4.3). Close to the sample holder there is a thermometer to measure the sample temperature. This probe can be cooled down to LHe temperature in a very short time.

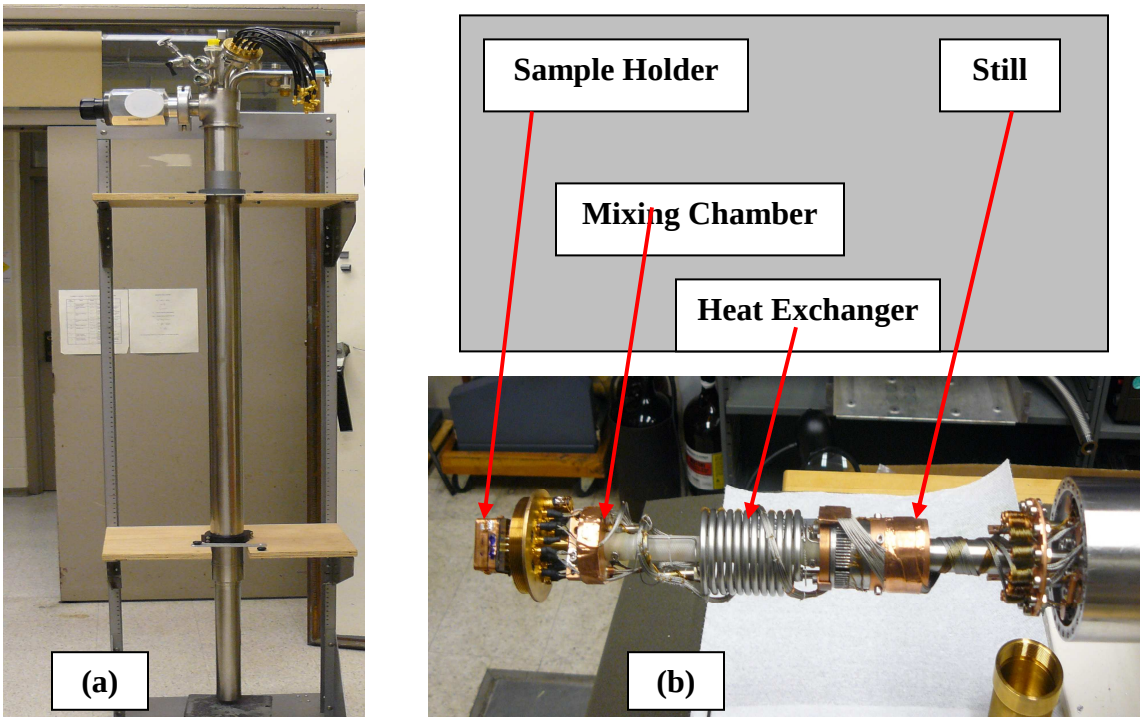


Fig. 4.4. (a) MINDIL-OD70-30mK Insert. (b) Tail of the MINIDIL Insert.

The important parts of the MINDIL insert are shown in Fig. 4.4. It has a dilution unit consists of mixing chamber, heat exchanger and a still. The sample holder lies close to the mixing chamber where the cooling occurs under dilution conditions to achieve the minimum temperature to carryout experiments on the sample. The inner part of the

dilution unit is kept under vacuum by a can called the inner vacuum can (IVC). The IVC is designed in a way that it can fit into the borehole of the superconducting magnet. The temperature is controlled by the TRMC temperature controller which also measure temperature of the Still and the Sample. Using this temperature controller, the sample chamber temperature can be varied from 20 mK to1.5 K.

4.4 Measurement Techniques

The measurements described in this dissertation have been carried out by a high sensitivity lock-in technique. Most of the instruments used in the measurement are commercially available. They are AMETEK (Model 5210) dual phase lock-in amplifier, Keithly 2000 multimeter, Hewlett Packard 3325B function generator, AMI model 135 liquid Helium level meter, Agilet E 3642A DC power supply and AMI model 420 magnet power supply. There are few instruments, such as a DC power supply and a sample connection box which are home built. The measurement circuits are rather simple. Different measurement circuits have been used in different experimental measurements along with different measurement techniques. Before starting any measurement, the quality of the device needs to be checked. We check the contact resistance between the pads of the device. The gate leakage of the device is also checked to ensure proper isolation. In the following sections we will discuss the quality control of the device and the conductance measurement techniques.

I. Device Quality Control

It is necessary to have a good ohmics of the device for the experimental measurements. It is, therefore, very important to check the ohmics of the device before starting any measurement. Figure 5.5 (a) shows a optical micrograph of a SG QPC device on which we have eight metal pads (ohmics). The pads are fabricated in a way that they are in good contact with the 2DEG and thus have the same ohmics (for more details please recall Chapter 3). The SGs are isolated by cutting the trench by wet etching from the rest of the device and the wafer which can be controlled separately by using the gate pads. The sample is glued in the chip carrier and the contact pads are bonded with the chip carrier pads (Fig. 4.5 (b)). The chip carrier is then mounted in the sample holder of the Insert and thus the electrical connection in the device is established.

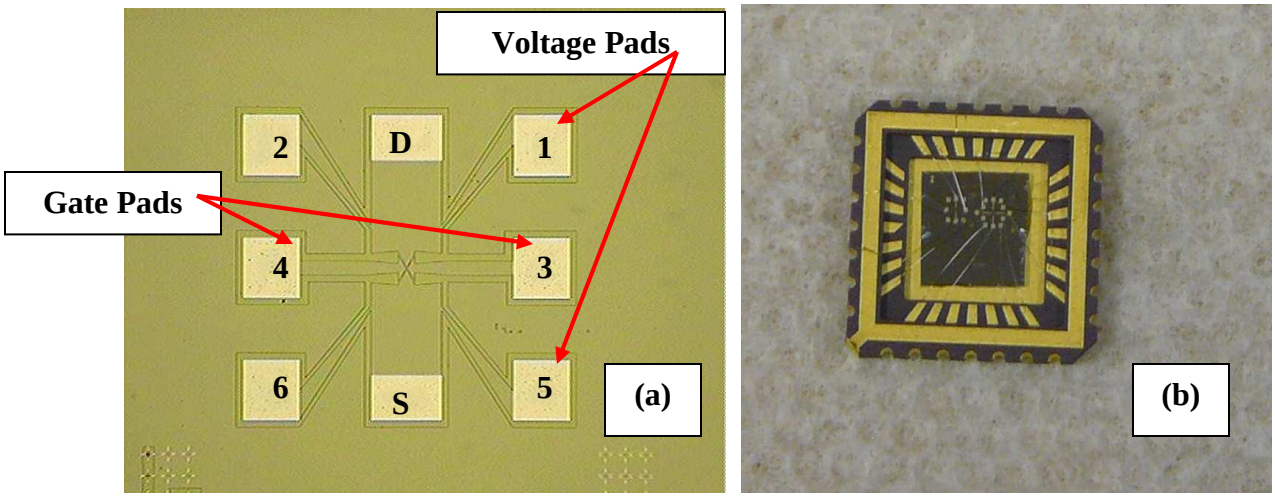


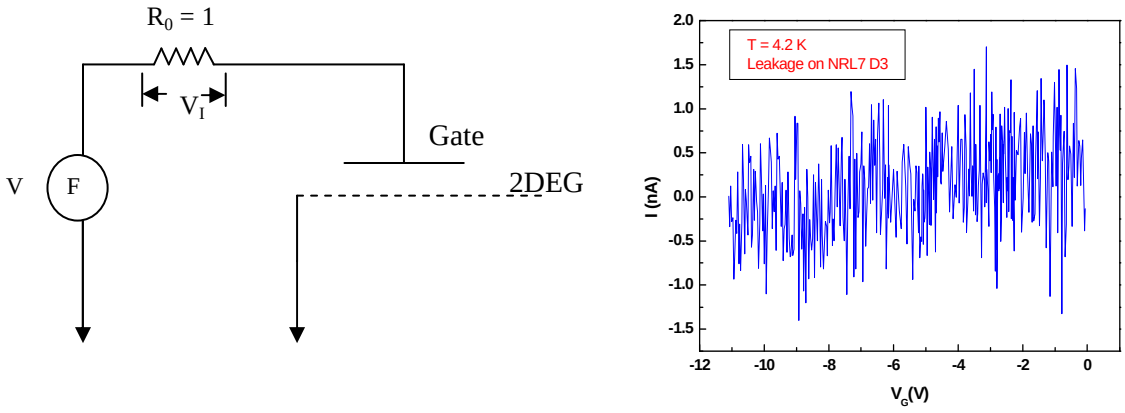
Fig. 4.5. (a) Optical micrograph of a SG QPC device. S/D represents the Source/Drain pads (b) The QPC device glued and bonded with Chip Carrier.

To check the contact resistance between the pads, a small current is established between the contact pads, which is measured by a lock-in using a standard resistance connected in series with the sample. The voltage drop between the pads is also measured by another lock-in. Measurements of resistance are done at 300 K and 4.2 K; resistance for good ohmics is expected to decrease as temperature goes down. The contact resistances at different temperature among the pads of the device, shown in Fig. 5.5 (a), are given in Table 4.1. The resistances among the pads indicate that the ohmics of the device are good. Moreover, at 4.2 K between source and the side gates, there were no signals. These indicate that the gates are completely isolated from the device which is essential to operate a side gated QPC device.

Table 4.1. Contact resistance of ohmic pad pairs of the SG QPC device of Fig. 5.5(a) at 300 K and 4.2 K.

Ohmic contacts measurements (Device: Cond1-010-3-D3)		
Contacts	R (KΩ) at T = 300 K	R (KΩ) at T = 4.2 K
S-D	3.5	1.6
S-5	3.7	1.4
S-1	7.2	3.0
S-3	9000	No Signal
S-4	6000	No Signal

After the ohmics check, the other measurement of interest is to check whether the side gates leak across the trenches in the sample. The side gates are completely isolated from the rest of the device by an isolation trench. These gates must be completely



(a) (b)

FIG. 4.6. (a) Circuit used for gate leakage current measurement. A function generator, FG, is used as a variable d.c. source. The 2DEG is connected to the ground via ohmic contact pads. (b) Leakage current as a function of gate voltage, V_G. The side gates don't leak and completely isolated from the rest of the device.

isolated in order to create a 1D conduction channel. The circuit used for gate leakage check is shown in Fig. 4.6(a). We use a function generator (Hewlett Packard 3325B) to apply a *dc* drive voltage on the gates while the 2DEG is grounded via ohmic contacts. The leakage measurement shown in Fig. 4.6(b) shows an absence of gate leakage current through the 2DEG which means the gates are of good quality. The measurement is carried out at 4.2K.

II. Conductance Measurement

The conductance of the 1D channel of different SG QPC devices fabricated from various InAs/InGaAs wafers is also measured. Figure 4.7 (a) shows the optical image of the QPC device and Fig. 4.7 (b) shows the SEM image of the SG QPC. The channel width of the QPC is controlled by the gate voltage. If the lithographic width of the QPC is large (~ 500 nm), a high negative gate voltage is needed to narrow down the channel. The more negative the gate voltage, the narrower the channel width is. If the lithographic channel width is small (~250 nm), the channel is already depleted due to surface charge depletion and a positive gate voltage is needed to open up the channel.

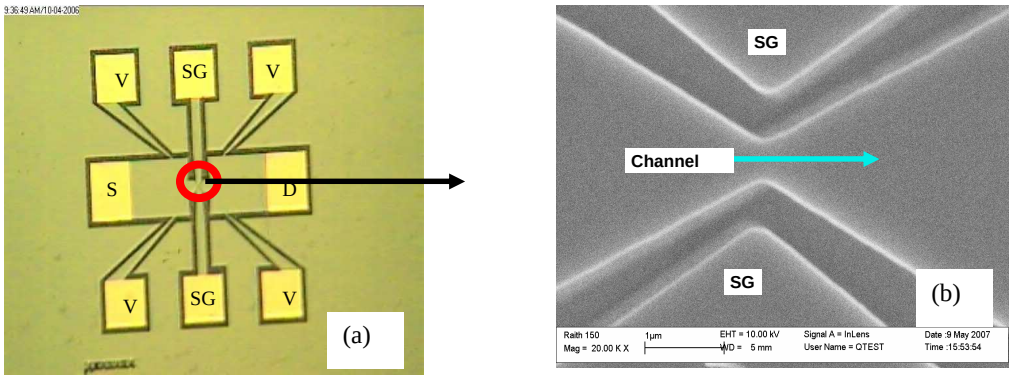


Fig. 4.7. (a) Optical micrograph of a SG QPC device. (b) SEM image of the QPC device.

The main idea of the conductance measurement is to measure the current into the QPC channel after applying a small bias voltage between source and drain and measure the voltage drop across the sample while changing the gate voltage. The conductance measurement circuit is shown in Fig. 4.8. A small bias voltage (100 μV) is created between the source and drain of the sample which is controlled by the output voltage of

the internal oscillator of the Lock-in (AMETEK 5210). A current is thus established into the device which is measured by a standard resistance, R_o, (usually 1K resistor) that is connected in series with the sample. The voltage drop across the standard resistance, V_{Ro}, is measured using the Lock-in1 (LI1). Thus the current through the sample is known by

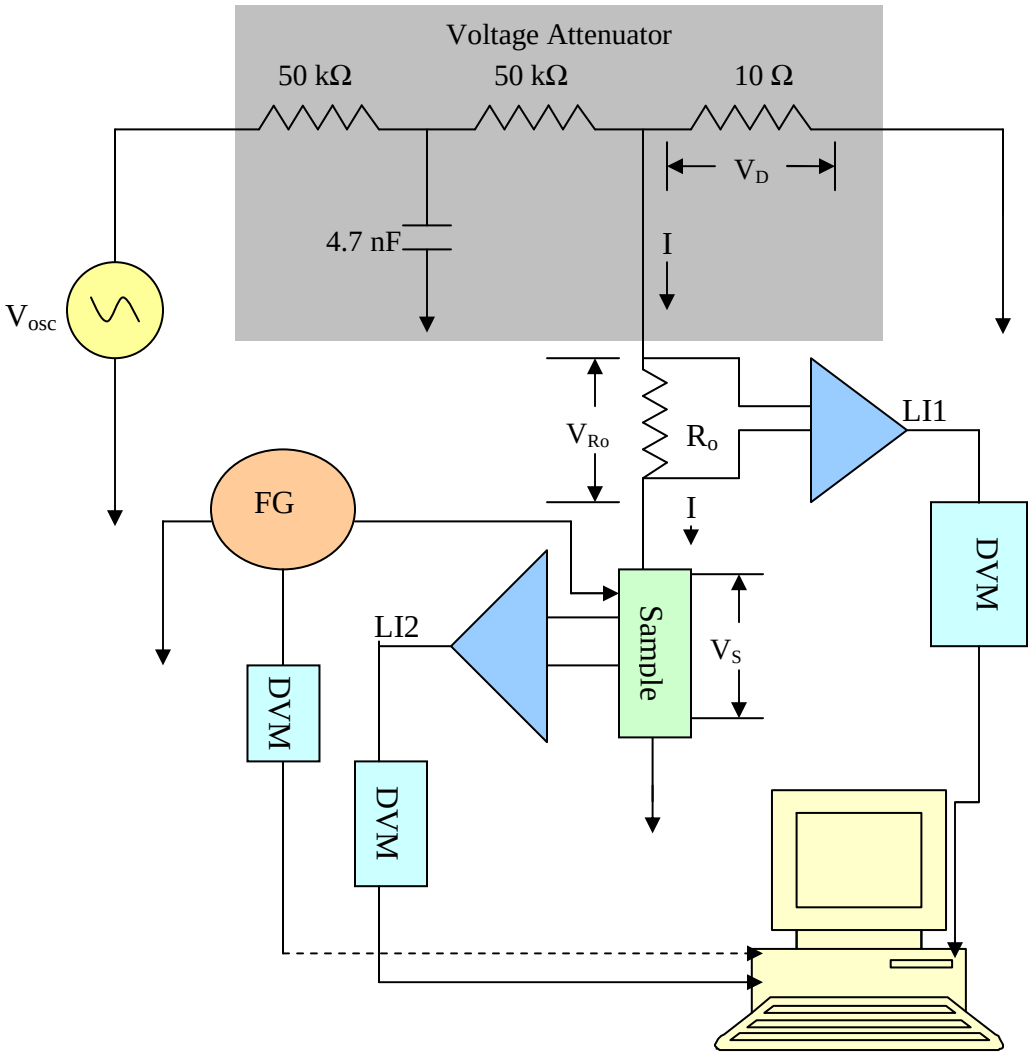


Fig. 4.8. Block diagram of the conductance measurement circuits.

dividing the voltage drop across the standard resistance, V_{Ro}, with the standard resistance, R_o. The Lock-in, LI1, is connected to the Keithly 2000 multimeter. The voltage drop, $V_{R,}$ across the sample is also colleted by another Lock-in, LI2, which is then connected to another multimeter (Keithly 2000). The gate voltage can be applied to both the gates together or individually using a Hewlett Packard (model 3325B) function generator (FG). This FG can supply ±5 V which is usually varied using a very small frequency (0.003 Hz). The additional voltage is supplied (if needed) to the gates by using the DC Power supply which is connected to the FG in series. The DC power supply has four different units and each unit can supply ±3 V. The FG is connected to the DVM (Keithly 2000). All these instruments are controlled by the computer via GPIB bus. As the gate voltage

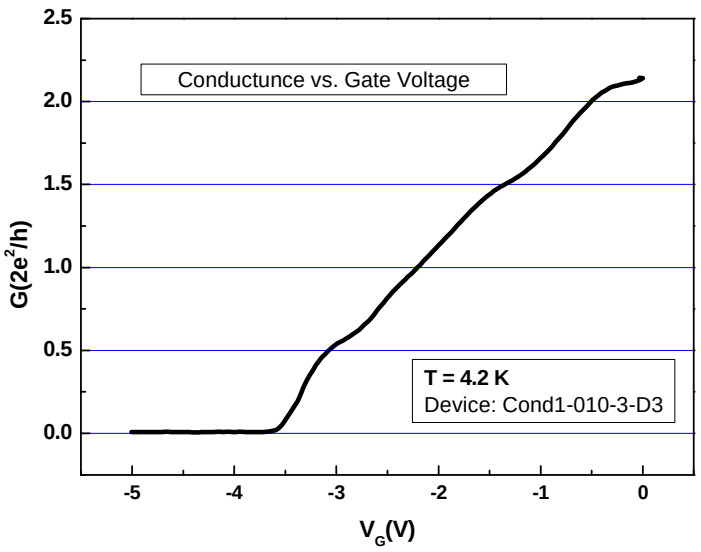


Fig. 4.9. Conductance of the 1D QPC channel as a function of the gate voltage.

changes, the current and voltage drop across the sample changes, so do the conductance. The conductance is measured as a function of the gate voltage. Before taking data, the

gate voltages need to sweep several times between the depletion and the maximum possible conductance to reach a stabilized condition. At the beginning of the measurement, there are lots of impurities that contribute to the conductance. But, when it is stabilized, we get no or less contribution from the impurities. The measured conductance as a function of gate voltage is shown in Fig. 4.9.

All these data points are collected by the computer using a special computer program which is accomplished by LabVIEW software. The external magnetic field is supplied by a superconducting magnet that can provide magnetic field up to 8T. This magnet is controlled manually by the AMI (model 420) magnet power supply and also individually controlled by the computer via a GPIB bus.

Reference

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2. O. V. Lounasmaa, *Experimental Principles and Methods Below 1 K* (Academic Press, London, 1974).
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5. H. London, G. R. Clarke and Eric Mendoza, *Osmotic Pressure of He^3 in Liquid He^4, with Proposals for a Refrigerator to Work below 1°K*, Phys. Rev. B **128** (5), 1992-2005 (1962).

Chapter 5

Experimental Results and Discussion

5.1 Introduction

The conductance in a one-dimensional system, e.g. in a QPC, is quantized in unit of $2e^2/h$. In this chapter, we will report an anomalous conductance plateau that is observed in the 1D side gated (SG) QPC devices which are fabricated from various InAs/InGaAs QW structures. The side gates in the QPC are defined by isolation trenches cut by wet etching and the 1D channel in the QPC is created by side gating. All the experimental measurements involved in this research work are low noise low temperature transport measurement. We measure the ballistic conductance of the constriction as a function of the gate voltage. Most of the experiments are done at 4.2 K while a few are carried out at mK temperature using a dilution refrigerator. In the following sections, we will briefly discuss the conductance quantization in 1D QPC and present the behavior of the anomalous plateau in perpendicular and parallel magnetic fields. This anomalous conductance plateau can be made to appear or disappear by creating an asymmetry in the confining potential. The effect of the asymmetry on the anomalous plateau will also be discussed. Based on the effect of asymmetry in the 1D SG QPC, we propose a new device, called as Dual-QPC device, to detect the spin polarization due to the lateral spin-orbit coupling (LSOC) by transport measurements. We will also discuss the working principle of the dual-QPC device and discuss the result obtained from such a device. We will compare our 0.5 structure with the well known 0.7 structure observed by other groups on GaAs based QPC. We will summarize the results in the end of this chapter.

5.2 Conductance Quantization

Ballistic transport occurs when both the length and width of the 1D system are smaller than the electronic mean free path and electrons propagate without any dispersion and scattering. It has already been discussed in Chapter 2 that the *ballistic conductanc*e, *G*, of such 1D system is quantized and is given by the Landauer formula,

$$G = \left(\frac{2e^2}{h}\right)N \quad , \tag{5.1}$$

where N = 1,2,3… is the number of occupied modes or 1D subbands with the subband energy bottom lower than the Fermi energy E_F and each subband is doubly degenerate due to the spin of the electrons [1, 2]. When the spin degeneracy is removed, e.g., by a strong external magnetic field *B*, the conductance is quantized at integral values of $0.5(2e^2/h)$. By applying a gate voltage, the channel width of the QPC can decrease (increase); this causes the separation of the 1D subbands to increase (decrease) and thus

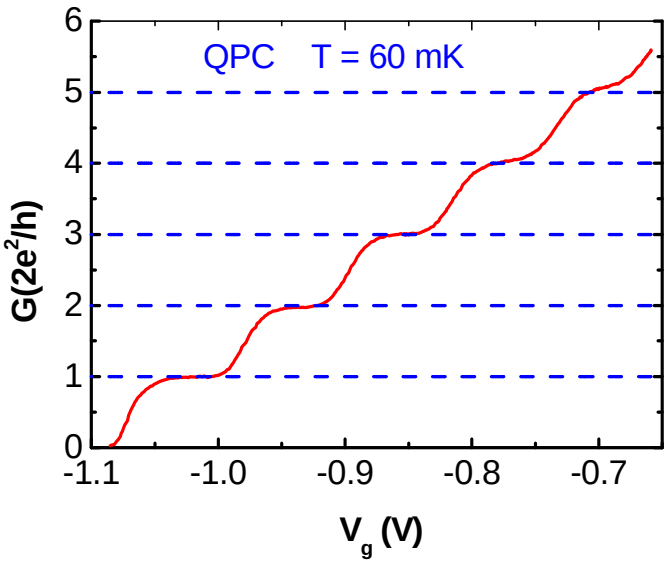


Fig. 5.1. Ballistic conductance as a function of gate voltage through a split-gate QPC fabricated on GaAs/AlGaAs heterostructure [3].

the subbands can cross the Fermi energy. The subbands contribute to the conductance in unit of $2e^2/h$, resulting in conductance quantization. Figure 5.1 shows the measured conductance of a 1D ballistic conductor created by the split-gate technique on a QPC made on GaAs/AlGaAs heterostructure.

In this research work, we measure the conductance of the 1D side-gated (SG) QPC devices fabricated on the InAs/InGaAs QW structures (Fig. 5.2 (a)). A side gate is simply a piece of 2DEG bordered by isolation trenches which is cut by wet etching. Since it is difficult to make non-leaky Schottky gates on InAs, side gates are used to create the 1D channel of the QPC devices. We expect to create vertical and symmetric trenches by wet etching which cannot achieve all cases.

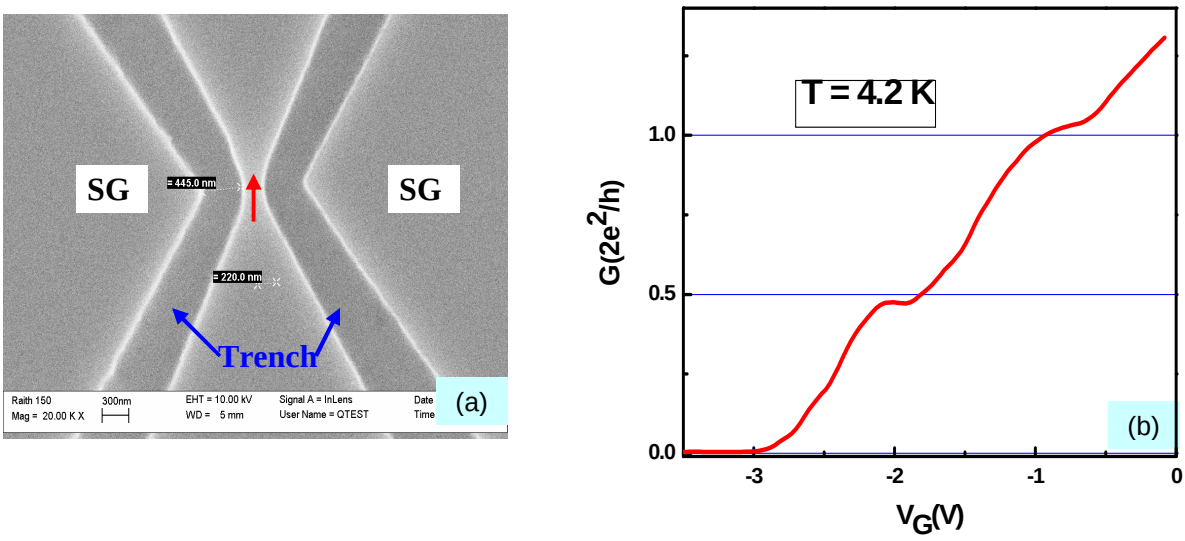


Fig. 5.2. (a) SEM micrograph of a Side Gated QPC. The darker parts, indicated by the blue arrows, are the trench cut by wet etching and the red arrow represent the channel. (b) The 0.5 structure observed on such QPC.

We find that the two trenches that define the QPC are not always symmetric: one is wider than the other in some cases. It is also not certain whether these trenches are exactly vertical, symmetric to each other or have some asymmetry between them. The trenches act as the hard walls of the lateral confining potential in the QPC. So, the confining potential may be symmetric or asymmetric depending on the etching process and is very difficult to control.

An anomalous conductance plateau is observed at $\boldsymbol{G \cong 0.5\ (2e^2/h)}$ in *zero magnetic field* on such SG QPC devices realized on InAs/InGaAs wafers and is called the **0.5 structure.** Figure 5.2 (b) shows the measured conductance on InAs SG QPC device as a function of the gate voltage. The conduction is pinched-off at -3V. The plot shows a normal conductance plateau at $G = 2e^2/h$. In addition to that an anomalous plateau is observed at $G \sim 0.5(2e^2/h)$. We believe this anomalous 0.5 structure occurs due to LSOC and is not an artifact. It is reproduced in several SG QPC devices fabricated on different InAs/InGaAs wafers. The 0.5 structure is also not due to impurity scattering. This 0.5 structure is reproduced after several cooling cycles. Also, it has a strong magnetic field dependence. The detailed behavior of the 0.5 structure in magnetic field will be discussed in the following section.

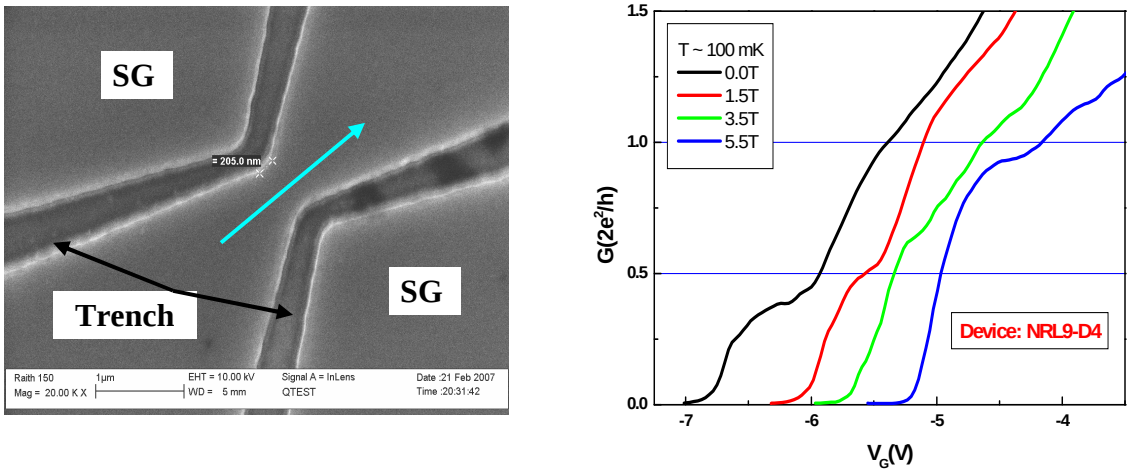
5.3 Magnetic Field dependence of the 0.5 Structure

To explore the origin of the 0.5 structure, we apply a magnetic field perpendicular to the plane of the device. This perpendicular field creates an additional confinement, the magnetic confinement. In high perpendicular fields, the electrons are confined and are traveling along the middle of the channel (far from the edges of the lateral confinement).

So, the electrons moving through the middle of the channel do not feel any LSOC which is purely an edge effect and one, therefore, expects a normal conductance behavior in high perpendicular magnetic field. The parallel magnetic field, along the current direction, should not have any effect on the 0.5 structure. The behavior of the 0.5 structure in perpendicular and parallel (in-plane) magnetic field will be discussed in the following subsections.

I. 0.5 Structure in Perpendicular Magnetic Field

We have observed the 0.5 structure in various QPC devices fabricated on different InAs/InGaAs wafers at zero magnetic field. The first set of QPC devices were fabricated on NRL wafer that has a low mobility (μ = 3.51 m^2/V.s) in the 2DEG. Figure 5.3 (a) shows a SG QPC device, NRL9-D4, fabricated on the NRL wafer (Please see Chapter 2 for the details of the wafer) on which we observe the 0.5 structure at mK temperatures without any magnetic field. The lithographical width of the QPC is around 600 nm while the length of the device is around 200 nm. The top and bottom trenches (darker area in Fig. 5.3 (a)) define the 1D channel of the QPC. The top trench has a width of 350 nm while the bottom trench's width is around 365 nm. The 1D channel (blue arrow in Fig. 5.3 (a)) is oriented in the [100] crystallographic direction to reduce the Dresselhaus SOC. At zero magnetic field, the 1D channel is completely depleted at -7.0 V. We have applied a magnetic field perpendicular to the 1D channel and observe the evolution of the 0.5 structure which shows a very interesting pattern.



(a) **(b)**

Fig. 5.3. (a) SEM image of the NRL9-D4 device. The blue arrow shows the direction of the 1D channel. The black arrows show the trenches that define the QPC, (b) Evolution of 0.5 structure in perpendicular magnetic field. The magnetic field increases from left to right. The gate voltage axis (x-axis) corresponds to the black curve (zero magnetic field plot). All the plots except the zero magnetic field plot (black curve) have been shifted along the x-axis for clarity.

Figure 5.3(b) shows conductance traces from device NRL9-D4 at various fixed magnetic field as a function of gate voltage from 0 T on the left and 5.5 T on the right. The voltage axis (x-axis) in Fig. 5.3 (b) corresponds to the leftmost (black) curve which represents the conductance plot at zero magnetic field. The pinch off voltage for the conductance plot at zero magnetic field (the leftmost (black) curve in Fig. 5.3(b)) is -7.0 V. All the other conduction plots, shown in Fig. 5.3 (b), are also depleted around the same voltage. All the plots, except the black one, have been shifted along the x-axis (to the right) for clarity. The red curve is shifted along the x-axis by 0.9 V, the green curve is shifted by 1.25 V and the dark blue curve is shifted by 1.75 V.

At zero field, an anomalous conductance plateau appear at $G \cong 0.5(2e^2/h)$ (black trace in Fig. 5.3 (b)). We will refer it as '0.5 Structure'. It is clearly observed that in high

perpendicular magnetic field this 0.5 structure evolves towards the higher conductance value and approaches the normal conductance plateau ($G = 2e^2/h$) (Fig. 5.3 (b)). At B = 0 T, the 0.5 structure has a conductance less then 0.5($2e^2/h$) but reaches to $G = 0.5\ (2e^2/h)$ at B = 1.5 T. It moves further up with the increase in magnetic field and at B = 5.5 T the conductance value of this structure is $G = 0.9\ (2e^2/h)$.

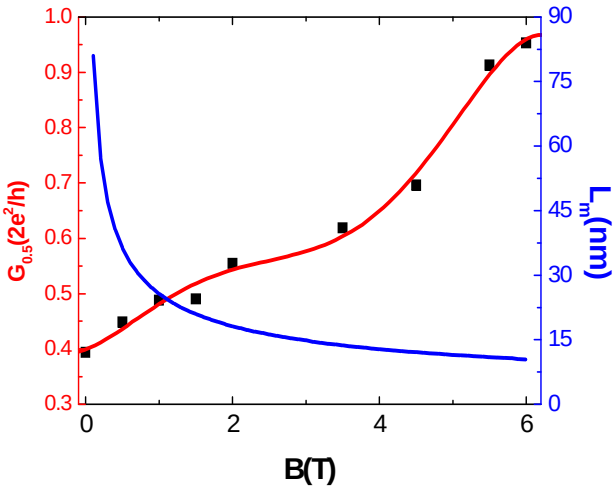


Fig. 5.4. The 0.5 structure moves up in perpendicular magnetic field and approaches to G ≈ $2e^2/h$. The red line is a guide to the eye. The blue curve is the plot of magnetic length as a function of magnetic field.

The conductance values, $G_{0.5}$, of the 0.5 structures are plotted as a function of magnetic fields in Fig. 5.4. The black squares in Fig. 5.4 are the conductance value of the 0.5 structure at different magnetic fields. It is clearly observed that the conductance values, $G_{0.5}$, increase as the (perpendicular) magnetic field is raised and approach the normal conductance state ($G = 2e^2/h$) in a high perpendicular magnetic field at B = 6.0 T. This indicates that the electrons are confined in the magnetic confinement and thus *the*

0.5 structure originated from lateral spin orbit coupling (LSOC). The blue curve in Fig. 5.4 is the plot of magnetic length as a function of magnetic field, which is defined as,

$$L_m = \left(\frac{\hbar}{eB}\right)^{1/2} , \tag{5.2}$$

where e is the electron charge and B is the magnetic field. The magnetic length defines the strength of the confinement and will be discussed in the discussion section.

The 0.5 structure also survives at LHe temperature (4.2 K). Figure 5.5 shows the cond1-010-1-D3 device fabricated on the cond1-010 wafer in which we observe the 0.5 structure at 4.2 K without any external magnetic field. The device has a lithographical length of 160 nm and width of 460 nm. The trench has the width of about 550 nm which larger than the NRL9-D4 device. The pinch-off for the zero magnetic field conductance plot (Black trace in Fig 5.6) occurs at -11.0 V. The device is parallel to the cleaved edge so that the 1D channel is oriented in the [110] crystallographic direction.

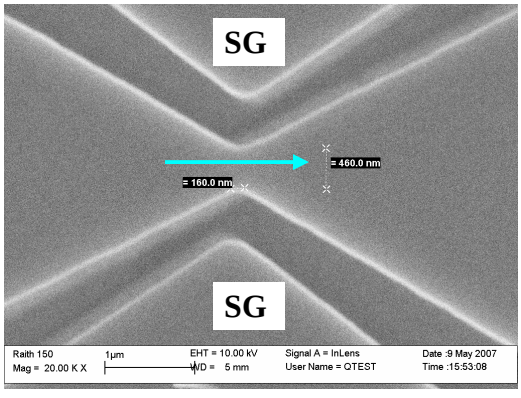


Fig. 5.5. SEM image of the Cond1-010-1-D3 device. The blue arrow shows the direction of the 1D channel.

The behavior of the 0.5 structure in high perpendicular magnetic field has also been reproduced (Fig. 5.6) in Cond1-010-1-D3 device at 4.2 K. We apply a magnetic field from 0 T to 8 T. The 0.5 structure reaches to the normal conductance plateau at 8.0 T. The evolution of the 0.5 structure is same in both Cond1-010-1-D3 and the NRL9-D4 device. Since, the trench width of the trench (550 nm) in this device is greater than the NRL9-D4 device (~350 nm), a more negative voltage is needed to deplete the device. All the traces are depleted at slightly different gate voltages which are close to –11 V. In Fig. 5.6, the gate voltage axis (x-axis) corresponds to the zero magnetic field conductance plot (the leftmost black trace) which depletes at -10.96 V. The other plots are shifted along the x-axis for clarity. The red curve is shifted along the x-axis by 0.5 V, the green curve is shifted by 1.25 V, the dark blue curve is shifted by 1.25 V and the light blue curve is

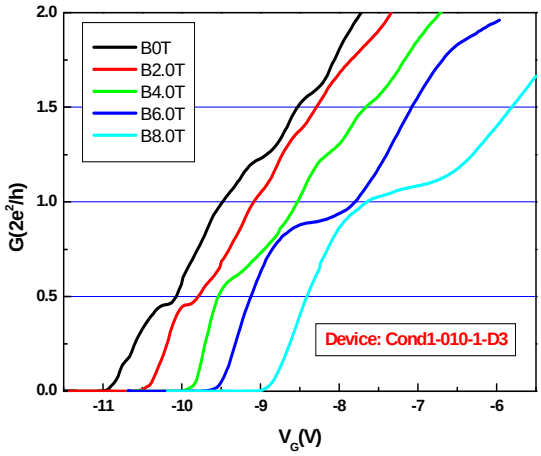


Fig. 5.6. The behavior of the 0.5 structure in perpendicular magnetic field is reproduced in Cond1-010-1-D3 QPC device at 4.2 K. The magnetic field increases from left to right. The x-axis scale corresponds to the black curve. The conductance plots are shifted along the x-axis.

shifted by 1.75 V. It is found that, the conductance become smaller initially (between 0.5 T to 1.0 T) but increases and approaches G= $2e^2/h$ in a high perpendicular magnetic field. The anomalous plateau reaches the conductance value of $G = 2e^2/h$ at B = 8.0 T, which is the first observed plateau in the case of normal conductance quantization.

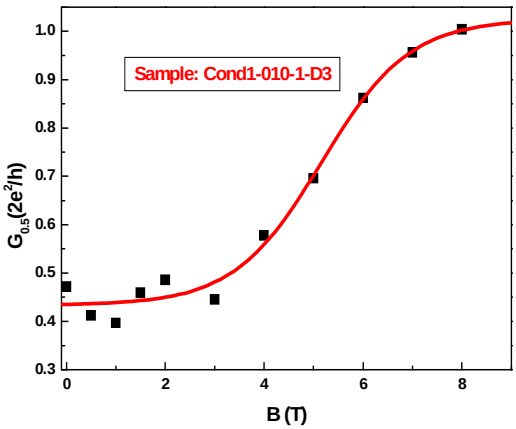


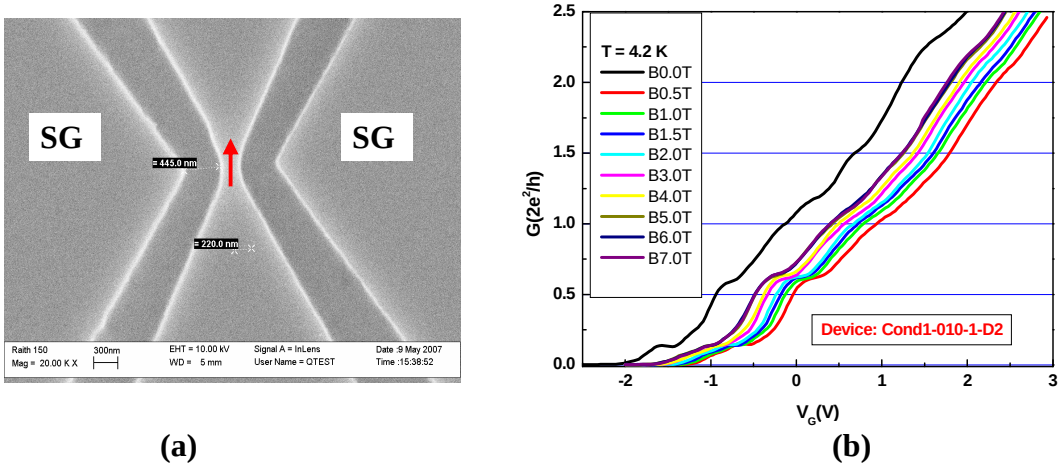
Fig. 5.7. The 0.5 structure moves up in high perpendicular magnetic field. The black squares are 0.5 structures in different magnetic fields taken from the data shown in Fig. 5.6. The red curve is the guide to the eye.

The black squares in Fig. 5.7 are the conductance value of the 0.5 structures in different magnetic field, taken from the data shown in Fig. 5.6. It shows clearly the evolution of this anomalous structure towards the normal conductance quantization.

II. 0.5 Structure in Parallel Magnetic Field

The behavior of the 0.5 structure indicates that this anomalous conductance arises due to the LSOC in the confinement potential of the QPC. This premise is confirmed by parallel magnetic field experiments. The magnetic field lies in the x-y plane (and thus is called in-plane field), where x is the current direction and y is the lateral direction. The

field is applied in the current direction (x-direction). The experimental results of the in-plane magnetic fields, obtained from Cond1-010-1-D2 device, are summarized in Fig. 5.8 (b). The SEM of the Cond1-010-1-D2 device is shown in Fig. 5.8 (a). The length and width of the device are 230 nm and 220 nm respectively. The width of the trench is around 400 nm. Since the QPC channel width is very small, positive gate voltage needs to apply to open up the channel.

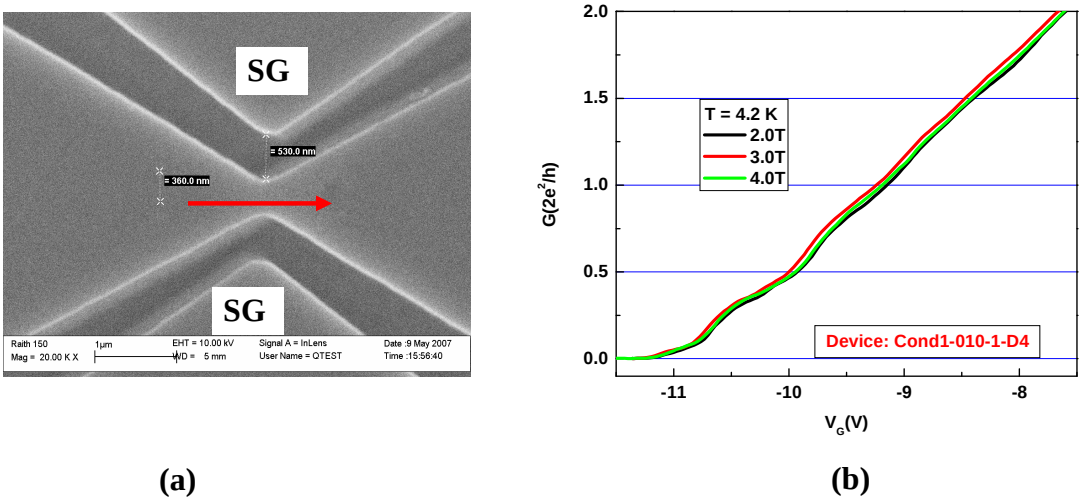


(a) **(b)**

Fig. 5.8. (a) The SEM image of the Cond1-010-1-D2 device. The red arrow shows the direction of the 1D channel. The darker region corresponds to the trenches that define the QPC, (b) the behavior of the 0.5 structure in parallel magnetic field observed in Cond1-010-1-D2 sample at 4.2 K. The field is applied parallel to the current direction. The conductance value of the 0.5 structure remains unchanged in magnetic field.

The anomalous conductance is observed at $G = 0.58(2e^2/h)$ on Cond1-010-1-D2 device fabricated on Cond.1-010 wafer. The in-plane magnetic field applied in the current direction has no significant effect on this anomalous structure. The plots are not shifted. The left most trace (Black) is at zero magnetic field which depleted at -2V. The conductance plots are measured at different magnetic fields spacing 0 and 7 T. The

conductance value of this 0.5 structure does not change with the increase of magnetic field, but the structure becomes well defined with the introduction of the magnetic field (Fig. 5.8 (b)) as some of the impurities washed away with the introduction of the magnetic field.



(a) **(b)**

Fig. 5.9. . (a) The SEM image of the Cond1-010-1-D4 device. The red arrow shows the direction of the 1D channel. The darker region corresponds to the trenches that define the QPC, (b) the behavior of the 0.5 structure in parallel magnetic field observed in Cond1-010-1-D4 sample at 4.2 K. The field is applied in the current direction. The conductance value of the 0.5 structure remains unchanged in in-plane magnetic field.

The behavior of the 0.5 structure in parallel magnetic fields is reproduced on another QPC device (Cond1-010-1-D4) and shown in Fig. 5.9. The SEM of the device is shown in Fig. 5.9 (a). The lithographical width of the QPC is around 360 nm while the length of the device is around 200 nm. The width of the trench is 530 nm. The width of the trench can be compared with the Cond1-010-1-D3 device (550 nm). So, the pinch-off voltage of these two devices is almost same. The pinch-off voltage for the Cond1-010-1-D4 device is -11.2 V while Cond1-010-1-D3 device is pinched-off around -11.0 V. So,

the width of the channel and the trench define how much voltage is needed to deplete the conduction channel.

Figure 5.9 (b) shows the conductance plot in different in-plane magnetic fields ranging from B = 2 T to B = 4 T. An anomalous structure is clearly observed at G ~ $0.5(2e^2/h)$ and the structure does not move up as the in-plane magnetic field is raised.

III. Discussion

The evolution of this **0.5** structure in perpendicular and in in-plane magnetic fields has been presented in the above two sections. The **0.5** structure moves up as the *perpendicular* magnetic field increases and approaches the normal conductance plateau at $\boldsymbol{G = (2e^2/h)}$ in high magnetic fields (**Sec. 5.2.I**). The 0.5 structure, however, does not move up with the increasing of in-plane magnetic field (**Sec. 5.2.II**).

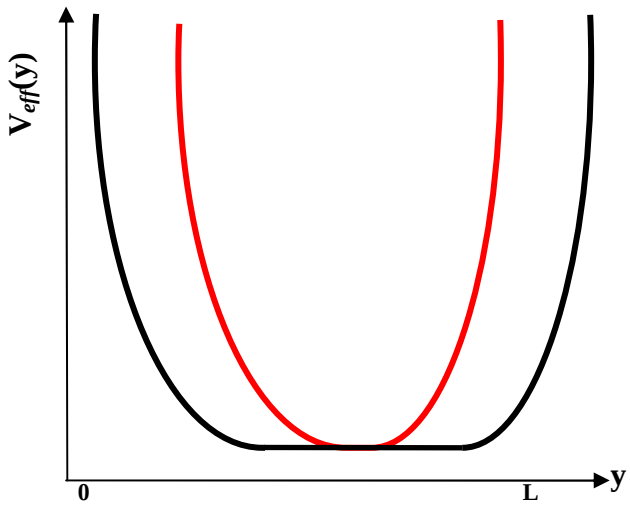


Fig. 5.10. The black curve represents the Lateral confinement in the SG QPC. The middle of the strip the potential is flat and rises quickly along the edges. The red curve shows the magnetic confinement created when the perpendicular magnetic field is applied to the QPC.

The evolution of the 0.5 structure in high perpendicular magnetic field can be explained by postulating the magnetic confinement hypothesis. The SG QPC creates a strong lateral confinement. The confining potential is flat in the middle of the channel and rises quickly along the edges (Black curve in Fig. 5.10). The voltage gradient along the edges gives rise to an electric field perpendicular to the edge. Due to the relativistic effect, that electric field causes a SOC along the edges of the lateral confinement known

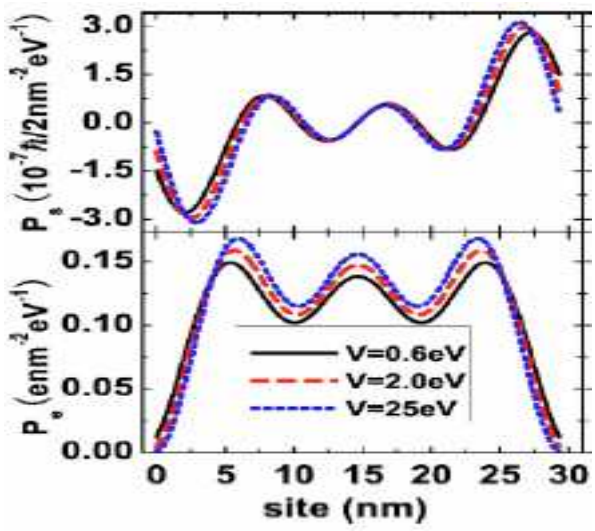


Fig. 5.11. Spin polarization in the lateral confinement [4]. Spin accumulation is plotted with respect to the lateral axis (site) in the top part of the figure. It shows that opposite spin accumulates along the two opposite edges. The bottom part shows the charge accumulation with respect to the lateral coordinate.

as lateral spin orbit coupling (LSOC). In a theoretical paper, published in 2006, Xing et al. showed that spontaneous spin polarizations can occur due to LSOC and opposite spins accumulate along the two edges in the lateral confinement [4]. Their numerical result is shown in Fig. 5.11. Similar results were also reported by Yongin Jiang and Liangbin Hu, in a separate paper [5], published almost the same time, which also claimed that

spontaneous spin polarization occurs in the lateral confinement and that opposite spin accumulate along the two different edges. (For more details see sec. 2.1.IV of chapter 2).

There is no net spin polarization nor spin accumulation in the middle of the lateral confinement. So, this LSOC is clearly an edge effect. Let us consider the current is flowing in the x direction and y is the lateral direction in the side gated QPC. The confining potential is created along the y direction due to the side gates. In the QPC, the magnetic field is applied perpendicular to the x-y plane along the z-direction which creates a magnetic confinement in the lateral direction (Red curve in Fig. 5.10). The energy of the electron can be approximated as,

$$E_n\left(k_x\right)=\left(n+\frac{1}{2}\right)\hbar\Omega+\frac{\hbar^2k_x^2}{2m^*} \quad . \tag{5.3}$$

For simplicity, we assume the lateral confinement as parabolic confinement with bare frequency ω_0. That is, ω_0 the frequency of the electrostatic confinement in the absence of magnetic field. The electrons are moving freely in the x-direction in the QPC with energy $\hbar^2k_x^2/2m^*$. The Ω in Eq. (5.3) can then be defined as,

$$\Omega^2=\omega_0^2+\omega_c^2 \ ,$$

with, $\omega_c = eB/m^*$, is the cyclotron frequency. The blue curve in Fig. 5.4 is the plot of the magnetic length as a function magnetic field and the magnetic length is defined in Eq (5.2). In a strong magnetic field, the magnetic confinement is such that the channel width of the QPC is comparable to twice of the magnetic length. When the channel width is more than the twice the magnetic length, the electrons moving in the channel are completely confined in the magnetic confinement and are far from the edges of the lateral

electrostatic confinement. Since, LSOC causes the spin polarization only along the edges in the lateral confinement, the electrons trapped in the magnetic confinement in high magnetic field do not notice any edge effect and one can expect the normal conductance quantization Thus, the 0.5 structure moves up in perpendicular magnetic field and approaches $\boldsymbol{G = (2e^2/h)}$ in high perpendicular magnetic field. The plot in Fig. 5.4 indicates a channel width of around 25 nm at which the 0.5 structure approaches $\boldsymbol{G}$ = ($\mathbf{2}\boldsymbol{e^2/h}$). This seems to be a reasonable value.

This hypothesis is confirmed by the in-plane magnetic field (parallel to the current direction) measurements which show that in-plane magnetic field has no effect on 0.5 structure (**Sec. 5.3.II**). In such a case, the magnetic fields do not create any confinement in the lateral direction and thus the 0.5 structure is unaltered in high parallel magnetic field. Therefore, it can be concluded that *the 0.5 structure originates from the spontaneous spin polarization due to LSOC. This is the first experimental observation of the LSOC in 1D system (QPC).*

5.4 Temperature dependence of the 0.5 Structure

The temperature is also a very important parameter to investigate in studying the origin of the 0.5 structure. The above results have shown that the 0.5 structure survives over a large range of temperature, from 100 mK to 4.2 K. The temperature behavior of the 0.5 structure in NRL9-D4 device is recorded in which the temperature is varied from 150 mK to 1.1 K (Fig. 5.12). Our dilution refrigerator does not allow further increase in temperature. Using the LHe insert, we observe 0.5 structure at 4.2 K in Cond-1-010-D3 device. We check the behavior of the 0.5 structure on this device in a temperature range

from 6 K to 13 K. The results of these two experiments along with a discussion will be presented in the following subsections.

I. Results

Figure 5.12 shows the temperature dependence of the 0.5 structure in the range of 150 mK to 1.1 K. These data are taken from NRL9-D4 device. Temperature has no significant effect on the 0.5 structure in the mK range. The voltage axis (x-axis) in Fig. 5.12 corresponds to the red curve at 150 mK temperature which depletes at -7.6 V. The other plots in Fig. 5.12 have been shifted in a way to have the same depletion voltage. In the temperature range of 150 mK to 1.1 K, the anomalous structure remains unchanged as shown in Fig. 5.12.

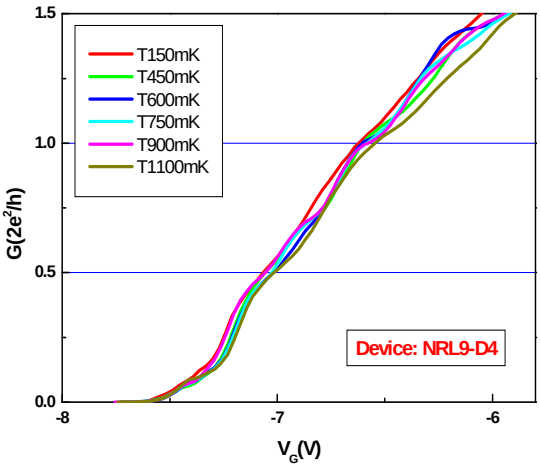


Fig. 5.12. The conductance plots at different fixed temperature on NRL9-D4 device. The measurements are taken in the temperature range from 150 mK to 1100 mK. The x-axis corresponds to the red curve at 150 mK which deplete at -7.59 V. All the other plots are shifted to the same pinch-off voltage.

The 0.5 structure also survives at 4.2 K (Fig. 5.2(b)). The behavior of the 0.5 structure at higher temperatures (6.0 K to 13.0 K) in the Cond1-010-1-D3 device is plotted in Fig. 5.13. The black trace in Fig. 5.13 corresponds to the conductance plot at 6K. The pinch-off voltage for this plot is -11.5 V. All the other plots have been shifted to have the same pinch-off voltage. At 6K, the anomalous plateau appears at a conductance value of G < 0.5 ($2e^2/h$). This structure moves up, approaching G = 0.5 ($2e^2/h$), when the temperature is increased further (see the plot corresponding to 8 K). Between 8K and 10K, the conductance value of the anomalous structure does not change. The 0.5 structure disappear at a temperature T ~ 13K that corresponds to energy ~ 1.1 meV which is of the same order as the LSOC energy.

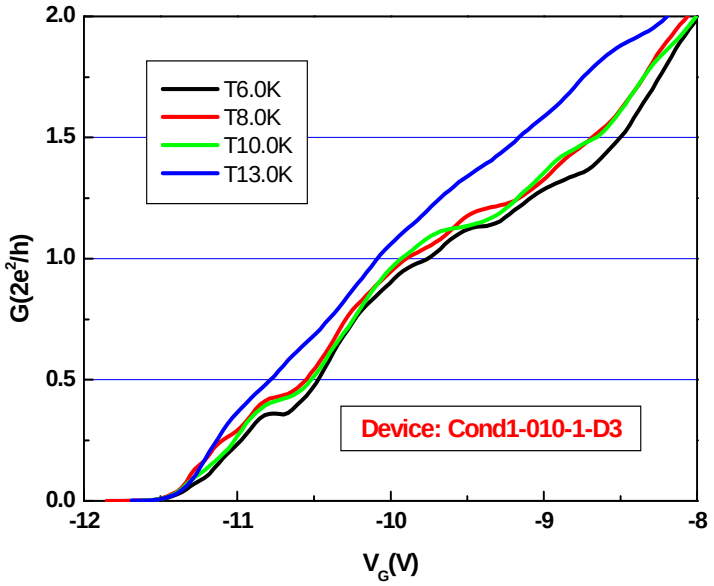


Fig. 5.13. The 0.5 structure at different higher temperature. Thermal smearing is observed at T ~ 13 K. The x-axis corresponds to the black curve at 6K which deplete at -11.5 V. All the other plots are shifted to have the same pinch-off voltage.

II. Discussion

Figure 5.12 shows measurements of the conductance in NRL9-D4 device at different temperatures ranging from 150 mK to 1.1 K. The unchanged conductance plateau at 0.5 ($2e^2/h$) within this temperature range (150 mK to 1.1 K) indicates that *the LSOC energy is higher than the thermal energy*. The 0.5 structure is also observed at LHe temperature which survives even higher temperature (a temperature less than 13 K). Figure 5.13 shows the conductance plots at higher temperatures (6 K to 13 K). So, it can be said that *the 1D subband energy separation is greater than or comparable to the thermal energy up to 13 K*. Both the 0.5 structure and the normal conductance plateau persist up to ~ 13 K.

5.5 Effect of Asymmetry on the 0.5 Structure

The 0.5 structure observed in the SG QPC fabricated on InAs wafer originated from the spontaneous spin polarization due to the lateral spin orbit coupling (LSOC). But the exact mechanism that creates the 0.5 structure is yet unknown. So far we have presented the results obtained from NRL9-D4, Cond1-010-D2, Cond1-010-D3 and Cond1-010-D4 devices in sections 5.3 and 5.4. We apply the same voltage to both the gates of those QPC devices to obtain those results. The side gated QPC is defined by trenches cut by wet etching. From the SEM images of the QPC devices, we find that the SG trenches are not always equal. This happens due to wet etching that attacks different part of the wafer in slightly different ways. Therefore, the lateral confining potential well, created by the hard wall of the SG trenches, may be symmetric or there may have a built in asymmetry in the potential profile. By applying different gate voltages to the gates of

the QPC, the built in asymmetry in the confining potential can be enhanced or reduced. In some QPC devices, the 0.5 structure is absent when same voltage is applied to both the gates and the potential profile may be symmetric in these cases. By applying different voltages to the gates of such QPCs, the 0.5 structure can be made to appear. The 0.5 structure is, therefore, related to the asymmetry in the confining potential well. In the following subsection we will present the results of the influence of asymmetry of the confining potential on the 0.5 structure. A discussion of the results will also be presented.

I. Result

Figure 5.16 shows the conductance quantization measured on Cond2-F1-D4 QPC device as a function of the sweeping gate voltage. The 1D channel in the Cond2-F1-D4 QPC device is created by the two gates: **G4** and **G7**. The black trace in Fig 5.16 is the plot of the conductance quantization when asymmetry between the gates is very small. In this case we apply -4.9 V on **G4** and -5.2 V on **G7**. So, the asymmetry between the gates is 0.3 V. Both the gates are connected together to the function generator which supplies sweeping voltage ranged from 0 to – 5 V. The trace shows no 0.5 structure and a weak plateau at $G = 2e^2/h$. This situation represents the symmetric condition in the confining potential.

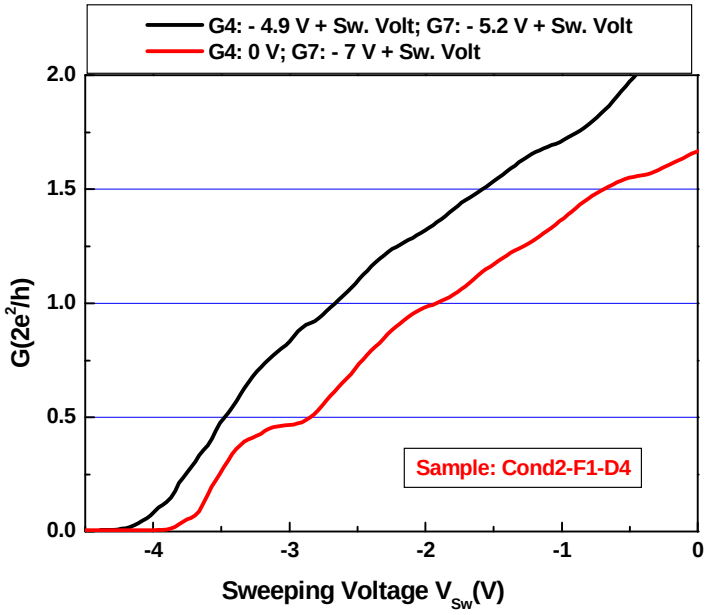


Fig. 5.14. Conductance a function of sweeping voltage measured in Cond-2-F1-D4 device. The black trace represents the symmetric gate voltage condition where almost the same voltage is applied to both the gates. The red curve is the conductance when -7.0 applied to Gate 7 but 0 V is applied to Gate 4.

The red trace in Fig. 5.16 represents the asymmetric profile in the confining potential. We apply zero gate voltage to the gate **G4** and - 7.0 V to the gate **G7.** The function generator is connected to both the gates to sweep the voltage between 0 to -5.0 V. In this case, an anomalous structure is observed at $G = 0.5(2e^2/h)$ along with the normal conductance plateau at $G = 2e^2/h$. So, by creating asymmetry in the confining potential the 0.5 structure can be made to appear.

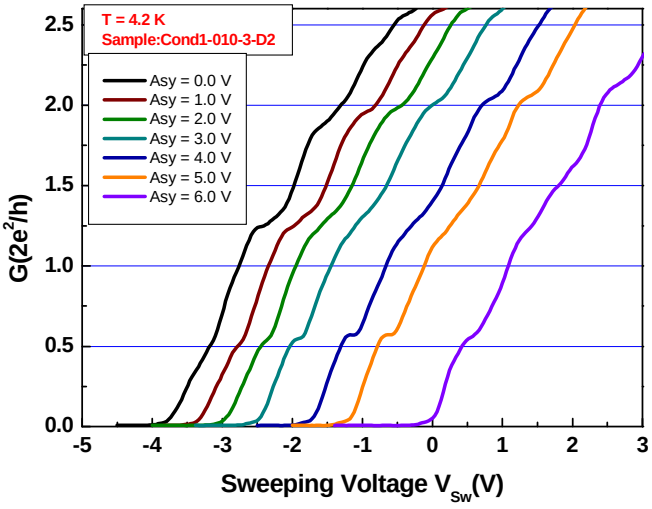


Fig. 5.15. Conductance plot measured in Cond-1-010-3-D2 device as a function of sweeping gate voltage at various positive gate asymmetries.

We have made the 0.5 structure appear in Cond2-F1-D4 QPC device by applying asymmetry to the gates in one sense (Fig. 5.16). *Is it possible to make the 0.5 structure appear by applying opposite sense of asymmetry to the gates?* To answer this question, the asymmetry is studied in the Cond1-010-3-D2 device. The device has two gates: Gate A and Gate B. Both the gates are connected together to the function generator. The asymmetry is created in the confining potential by applying different DC voltages (from the DC voltage source) to the gates. The confining potential will have a positive asymmetry when Gate A = 0 V and Gate B > 0 V and a negative asymmetry when Gate A > 0 V and Gate B = 0 V. In Fig. 5.17, conductance of the QPC is measured as a function of sweeping gate voltages under different asymmetric conditions. The positive asymmetry is increased from 0 V (left) to 6 V (the right) with the increment of 1V as shown in Fig. 5.15. The leftmost trace in Fig. 5.15 represent the zero asymmetric

condition (Gate A = Gate B = 0 V), where the 0.5 structure is very feeble. But the 0.5 structure become prominent as soon as the positive asymmetry is imposed. From Fig. 5.15 we see that when the positive asymmetry is 2 V (Gate A = 0 V and Gate B = 2 V), the anomalous structure has appeared and has the conductance value $G = 0.5(2e^2/h)$.

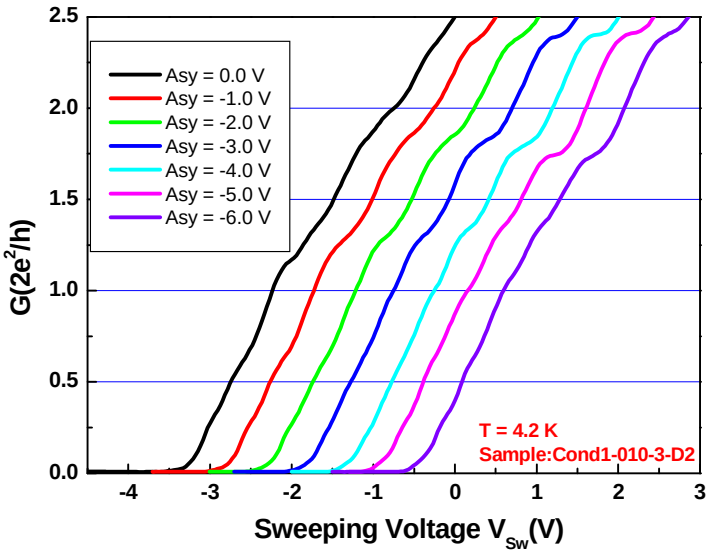


Fig. 5.16 Conductance as a function of sweeping gate voltage in Cond-1-010-3-D2 device at various negative gate asymmetries. The 0.5 structure is absent in the negative asymmetry range from 0 V to 6.0 V.

The 0.5 structure can be created by establishing an asymmetry in the confining potential in one sense (e.g. creating positive asymmetry in Cond-1-010-3-D2 device as shown in Fig. 5.15).

Figure 5.16 shows the conductance plots when the negative asymmetry is applied to the gates of the same Cond-1-010-3-D2 device. In the negative asymmetry case, we change the potential profile in the confining potential in the opposite way as the positive asymmetry (Now Gate A > 0 V and Gate B = 0 V). The negative asymmetry also

increased from 0 V to 6.0 V. Figure 5.16 shows the conductance plots as a function of sweeping gate voltage at different negative asymmetric conditions. The plots in Fig. 5.16 give no indication of the 0.5 structure even at the negative 6 V asymmetric condition (Gate A = 6.0 V and Gate B = 0 V).

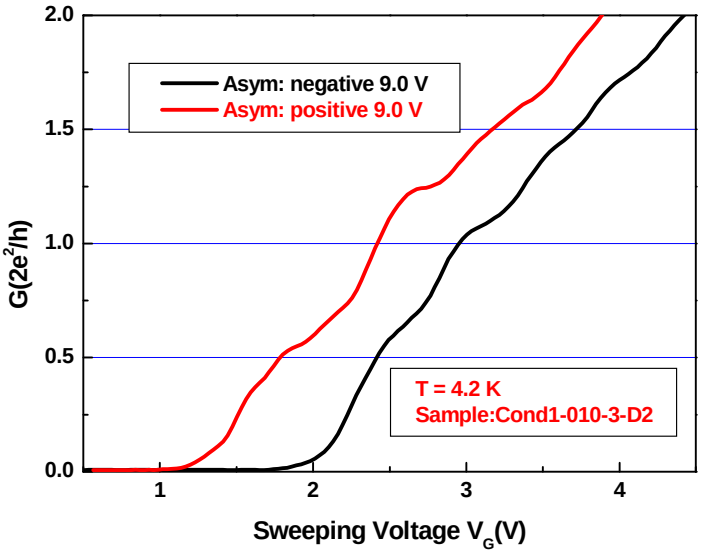


Fig. 5.17. Conductance plot measured in Cond-1-010-3-D2 device as a function of sweeping gate voltage at both positive 9.0 V asymmetry and negative 9.0 V asymmetry. The 0.5 structure is present in both asymmetries.

The negative asymmetry is then further increased on the same device (Cond-1-010-3-D2). The 0.5 structure is finally observed when the asymmetry is –ve 9.0 V (Black trace in Fig. 5.17). Therefore, the 0.5 structure can be created by applying both positive and negative asymmetry. Figure 5.17 shows two conductance plots that have opposite asymmetry. The black trace in Fig. 5.17 corresponds to the negative asymmetry (Asym: –ve 9.0 V) which shows an anomalous conductance plateau at G = 0.56($2e^2/h$). The red curve in Fig. 5.17 represent the positive asymmetry situation (Asym: +ve 9V) which shows an anomalous plateau at G = 0.52($2e^2/h$). These results clearly show that the 0.5

structure can be created by applying both positive and negative asymmetry to the confining potential. The two conductance plots in Fig. 5.17 are not exactly the same. This is because the asymmetries in those two cases are very different. Also, the asymmetry in the confining potential may not be mirror image of each other.

II. Discussion

The side gates of the QPC are created by wet etching which in turn define the hard wall of the confinement potential. The wet etching is very much process dependent and is very hard to control. The confinement potential well created in this way may have a symmetric configuration or have a built in asymmetry. It is hard to determine which way it creates the asymmetry.

In sec. 5.2.III, it has been already discussed that due to LSOC spontaneous spin polarization occurs in the lateral confinement and opposite spin accumulates along the two edges. But we observe an anomalous plateau at G ~ 0.5 ($2e^2/h$) which indicates that only one type of spin contributes to the transport measurement.

In Cond2-F1-D4 device no 0.5 structure is observed when same voltage is applied to the two side gates of the QPC (Black trace in Fig. 5.14). So, the lateral confinement created by the side gating is *symmetric*. And, *in the transport measurement both types of spin contribute equally*. The 0.5 structure is then made to appear by applying very different gate voltage to the two gates of the QPC (Red trace in Fig. 5.14). This QPC has two gates: Gate4 and Gate7. The Gate 4 is kept at 0V while a voltage is supplied to Gate7, -7 V is applied from the DC source along with the sweeping voltage (0 V to -5 V) from the function generator. So, at $G = 0.5$ ($2e^2/h$) the asymmetry is close to -10 V. This

large negative gate voltage changes the potential profile on the edge at gate G7. Therefore, on that edge spin accumulation may be enhanced or reduced. But, at the other edge, where opposite spin might accumulate, no effect is seen as there is no gate voltage applied. *Therefore, in the lateral confinement of the QPC, one kind of spin dominates over the other and thus, the 0.5 structure is observed through transport measurement.*

Figure 5.15 shows the conductance plot as a function of the sweeping gate voltage at different positive asymmetries, from which it is clear that the 0.5 structure appears after creating an asymmetry in the confining potential. When the asymmetry is zero or small (The left two traces in Fig. 5.15), the 0.5 structure is very feeble but becomes prominent with the increase of positive asymmetry (see the conductance plots that correspond to positive asymmetry 3 V to 6 V in Fig. 5.15). But, the negative asymmetries in the range from 0 to 6.0 V do not indicate the 0.5 structure (Fig. 5.16). *The potential profile of the lateral confinement is symmetric in this negative voltage asymmetry range (negative 0 V to negative 6V). This explains the absence of any 0.5 structure in Fig. 5.16.* Interestingly, when the negative asymmetry is increased to 9 V, the 0.5 structure appears (Black trace in Fig. 5.17). In this case, we create enough asymmetry in the confining potential well to make one kind of spin dominate over the other. *Therefore, the 0.5 structure can be made to appear by applying both positive and negative asymmetry in the confining potential well.* So, by applying a large positive asymmetry, electrons with one type of spin (say, spin-up) are made to dominate over the other type of spin (say, spin-down) and by applying negative asymmetry, electrons with the opposite spin (spin-down) are made to dominate over the other (spin-up). Therefore, if the spin-up electrons

contribute to the 0.5 structure in the case of positive asymmetry, the spin-down electrons contribute to the 0.5 structure when negative asymmetry is applied.

5.6 Detection of the Spin Polarization

The 0.5 structure can be manipulated by creating the asymmetry in the side gated QPC fabricated on InAs/InGaAs QW structures. From the discussion of the previous section, it is possible to create the 0.5 structure due to spin-up electrons by changing the asymmetry in the confining potential in one sense (say, positive asymmetry) and the 0.5 structure can also be created due to spin-down electrons by changing the asymmetry in the opposite sense (say, negative asymmetry). Based on these facts, we have proposed a device, called as Dual-QPC device (Fig. 5.18), to experimentally validate the spontaneous spin polarization due to LSOC by transport measurements. In the following two sub-sections we will discuss the working details of the proposed dual-QPC device and the experimental results obtained from that device.

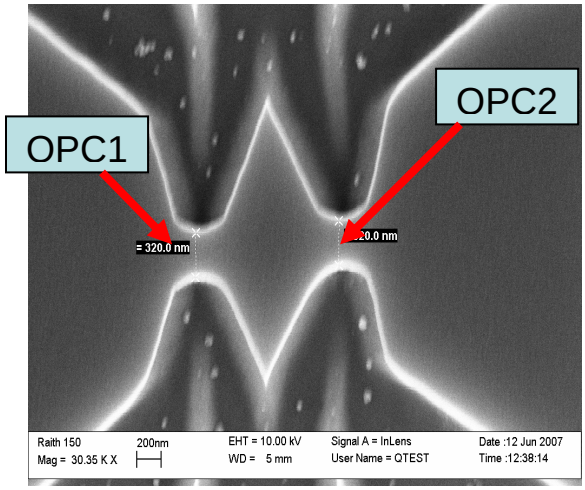
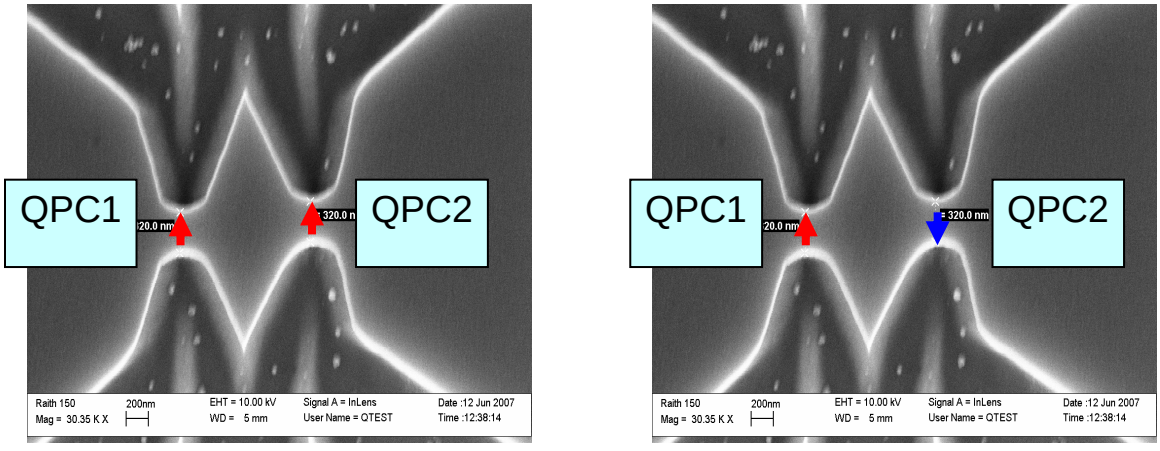


Fig. 5.18. SEM image of a Dual-QPC device fabricated on Cond1 InAs/InGaAs QW structures.

I. Dual-QPC Device

The dual-QPC device consists of two identical SG QPCs in series (Fig. 5.18). Each QPC has two side gates realized by wet etching which can be controlled independently. The channel width of the QPC is ~ 300 nm and the length is approximately 200 nm. The distance between the two QPC is around 1 micron. We call the left QPC as QPC1 and the right QPC as QPC2. The QPCs can be characterized separately to find out the gate voltages and asymmetry under which the 0.5 structure is observed. Then one sets the gate voltage and asymmetry of QPC2 that corresponds to the 0.5 structure. By changing the asymmetry in both ways (applying positive and negative asymmetry) on the QPC1 the output conductance will be plotted. If the 0.5 structure observed in those two QPCs are due to the same spins (say spin up), then the output



(a) (b)

Fig. 5.19. Working principle of the dual-QPC device: (a) If QPC1 and QPC2 allow the same kind of spins; we expect full transmission, (b) If QPC1 and QPC2 allow opposite spins there will be no transmission in the ideal case.

should also give the 0.5 structure plateau (we expect full transmission). But if they are due to opposite spins, then we expect a substantial drop in the conductance of the 0.5 plateau (Fig. 5.19). This is basic working principle of the dual-QPC device.

II. Result

The SEM of the dual-QPC device is shown in Fig. 5.18. The channel of the device is closed due to surface charge depletion. To open up the conduction channel, a positive voltage needs to apply to both the QPCs. A large positive voltage is applied to both the gates (+ 9.0 V in this case) of the QPC1 to completely open up the channel. The QPC2 is then characterized by measuring the conductance and to find the conditions under which the 0.5 structure is observed. The conductance characterization plot is shown in Fig. 5.20.

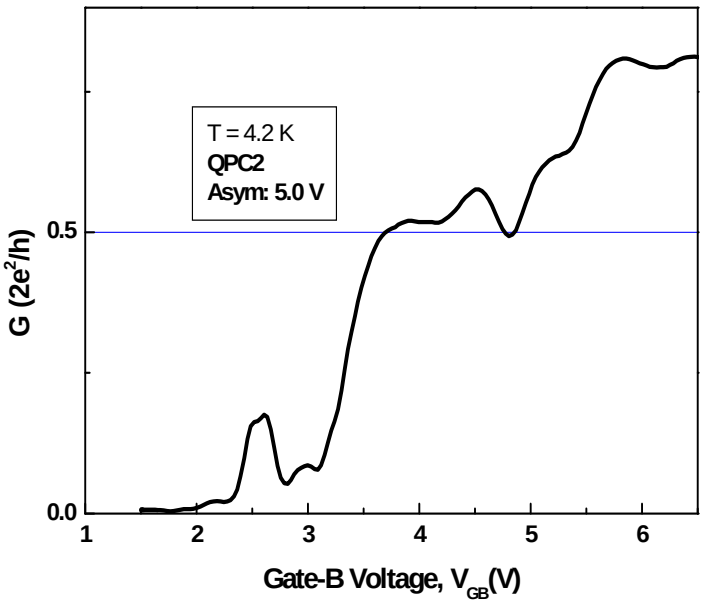


Fig. 5.20. Characterization of the QPC2 keeping the channel of the QPC1 open. QPC2 has two gates: Gate A and Gate B. Conductance of the QPC2 is plotted as a function of the Gate-B voltage.

The QPC1 is kept wide open by applying + 9V to both the gates so that the conductance of the QPC1 corresponds to $G \sim (2e^2/h)$. The QPC2 has two gates: Gate-A and Gate-B. From the DC voltage source +5 V is applied to the Gate-B while Gate-A is kept at zero voltage. The function generator is connected to both Gate-A and Gate-B and is swept between - 3.5 V to +1.5 V. The conductance of the QPC2 is plotted as a function of the Gate-B voltage and is shown in Fig. 5.20. The 0.5 structure is observed when the total voltage on Gate-A is zero while the total voltage in Gate-B is +5.0V.

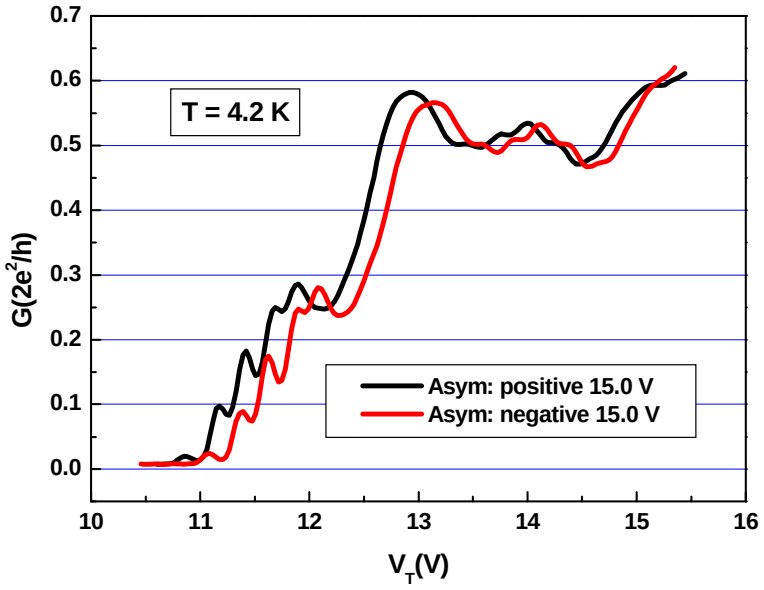


Fig. 5.21. QPC2 is fixed at ~0.5 ($2e^2/h$) while output conductance is plotted as a function of the gate voltage in the QPC1. The black trace corresponds to the conductance at positive 15.0 V asymmetry and the red trace corresponds to the conductance at negative 15.0 V asymmetry.

QPC2 is then set at the conduction value $G = 0.5\ (2e^2/h)$ by applying zero gate voltage to Gate-A and +5.0 V to Gate-B. Then we apply both positive and negative asymmetry to the QPC1 and measure the output conductance in both cases. Figure 5.21

shows the output conductance as a function of the total gate voltage, V_T. The red trace in Fig. 5.21 is the case when positive 15 V asymmetry is applied to the gates of the QPC1. There are two gates in QPC1: Gate1 and Gate6.

In the case of positive15V asymmetry, Gate1 is kept at 0 V while +ve 15 volt is applied to the Gate6. The function generator is connected to both the gates and sweeps between -4.5 V to +0.5 V. The black trace in Fig. 5.21 shows the conductance when negative 15 V asymmetry is applied to the QPC1. In this situation, Gate1 is kept at positive 15 V and Gate6 is kept at 0 V. The function generator is connected to both the gates and sweeps between -4.5 V to +0.5 V. In both cases, a very wide 0.5 structure plateau is observed. *But the expected drop in the conductance in the 0.5 plateau in one case is absent.*

III. Discussion

We first set the gate voltages in QPC2 so that it represents the 0.5 structure. This 0.5 structure is the contribution of one kind of spin (say spin-up). After that the conductance of the QPC1 is measured at different opposite asymmetry voltage. Figure 5.20 shows the conductance plots obtained from QPC1 at +ve 15 V asymmetry and –ve 15 V asymmetry. In both cases, we observe a large plateau at 0.5 ($2e^2/h$) and the expected drop of conduction in one case has not been observed.

By applying voltages to the side gates, it should be possible to adjust the widths of the two QPCs of the dual-QPC device together or independently. The QPC1 and QPC2 in the preliminary dual-QPC device shown in Fig. 5.18 are separated by 900 nm. Moreover, the channel widths in these two QPC are around 300 nm and the channels are initially

closed due to surface charge depletion. The area between these two QPC is also closed due to the same reason. A large positive voltage is needed to open up the channel widely. We find that *the two QPCs are not independent of each other*. The gate voltage of one of the QPC has an effect on the other QPC. When we change the gate voltage in the QPC1, the conductance channel in QPC2, which is fixed at $G \sim 0.5\ (2e^2/h)$, is also changed. The *area between the two QPCs act like a quantum dot* and the area of the dot is changing with changing the gate voltage of any of the QPC. *Thus, the output conductance of the QPC1 at different asymmetry condition is not only due to QPC1 alone; rather conductance of the QPC2 and the conductance of the quantum dot contribute to the output conductance.* Therefore, we have not observed the expected drop in the output conductance of the QPC1 in one of the asymmetric conditions (either in positive 15 V asymmetry or in negative 15 V asymmetry).

The oscillations in the conductance in Fig 5.21 are observed due to the quantum dot that is created in the central region between the two QPC (see Fig. 5.18). While changing the gate voltages in the QPCs, the area of the quantum dot also changing. While changing the area, the Fermi energy sweeps through the energy levels in the quantum dots which causes the rise and drop of the conductance in the plateau area.

5.7 Comparison: Our 0.5 Structure and the 0.7 Structure Observed by Others

The 0.5 structure, which is observed in our experiments, is clearly different from the 0.7 structure or other anomalous plateaus observed by different groups. We have observed the 0.5 structure in a SG QPC fabricated on InAs QW structures whereas the

0.7 structure and/or other anomalous plateaus were observed on GaAs based 1D systems (see chapter 2, sec. 2.3). The 0.7 structure is feeble at low temperature but becomes prominent at higher temperatures [6]. *The 0.5 structure persists over a large range of temperatures from 70 mK to ~ 13 K*. The evolution of the 0.5 structure in magnetic fields clearly indicates that it is originates from the spontaneous spin polarization due to LSOC. In a *parallel magnetic field* the *0.7 structure smoothly evolved to the Zeeman spin-split plateau at* $G = 0.5(2e^2/h)$ [6, 7]. In our case, we have observed the *0.5 structure at* $G = 0.5(2e^2/h)$ in the *absence of any external magnetic field* and *the parallel magnetic fields has no effect on the 0.5 structure* (Fig. 5.8). The 0.7 structure *disappears* in a *small perpendicular magnetic field* [8]. In our case, the 0.5 structure *evolves towards the normal conductance plateau at* $G = 0.5(2e^2/h)$ *in perpendicular magnetic field* (Figs. 5.3 and 5.6). An anomalous conductance plateau at $G = 0.5(2e^2/h)$ was also reported in Ref. [9] along with the 0.7 structure, where the authors reported a *perpendicular magnetic field* (up to 1.2 T) showed *no effect* on the anomalous structures. They also observed that the *0.5 plateau* is *best defined* when the potential of the lateral confining well is *most symmetric* and in that situation 0.7 structure moves toward $2e^2/h$. Chung et. al. [8] reported that by adjusting the gate bias it is possible to tune on and off the 0.7 anomaly or to make it continuously evolve into a normal integral conductance plateau. *We are able to make the 0.5 structure appears by applying both positive and negative asymmetry in the confining potential well.*

5.8 Summary

An anomalous conductance plateau is observed at $G = 0.5\ (2e^2/h)$ in SG QPC made on InAs/InGaAs QW structures and is known as 0.5 structure. The 0.5 structure moves up in perpendicular magnetic field and approaches the normal conductance plateau at $G = (2e^2/h)$ in high magnetic fields (Figs. 5.3, 5.6). In contrast, the in-plane magnetic field has no effect on this structure (Figs. 5.8 and 5.9). *The evolution in the magnetic fields clearly indicates that the origin of the 0.5 structure is the spontaneous spin polarization due to LSOC.*

The 0.5 structure exists over a large temperature range, spanning 70 mK to at least 10 K. This anomalous structure smeared out at temperature T ~ 13 K. *The thermal smearing indicates that at T ~ 13 K, the thermal energy, KT, is comparable or greater than the 1D subband energy separation.*

By electrically manipulating the asymmetry of the confining potential well, the 0.5 structure can be made to appear and disappear (Fig. 5.14). This indicates that *the asymmetry in the confining potential of QPC leads to a net spin polarization giving the 0.5 structure.* It is also possible to create this anomalous structure by applying both positive and negative asymmetry in the confining potential well (Fig. 5.17). *This indicates that opposite spins cause the 0.5 structure in the cases of positive and negative asymmetry.*

Based on the above idea, we have proposed a device, named a Dual-QPC, to experimentally validate the spontaneous spin polarization that arises due to LSOC by transport measurement. The dual-QPC device has two QPC in series. If the two QPCs in the device are set in a way that both of them allow the same type of spin, we expect to

observe the 0.5 structure. But, if the two QPC allow opposite spins, then a drop in the conductance in the 0.5 plateau is expected. *The results from the preliminary device (Fig. 5.22) show no indication of the drop in the conductance in the 0.5 plateau as we change the asymmetry in one of the QPC in both positive and negative ways. This happens because the two QPCs of the dual-QPC device are not completely independent.* They influence the conductance of each other. *The spontaneous spin polarization can be detected directly by transport measurement if we are able to manipulate the two QPCs in the dual-QPC device independently.*

The magnetic field (see sec: 5.3) and the temperature dependence (see sec: 5.4) of the 0.5 structure clearly indicate that our 0.5 structure (observed in InAs QPC) is different than the 0.7 structure observed on GaAs QPC by different groups (see sec: 5.7).

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Chapter 6

Future Work

The results presented in the Chapter 5 demonstrate that in InAs SG QPC we observe the 0.5 structure, an anomalous conductance plateau at $G = 0.5\ (2e^2/h)$. The origin of the 0.5 structure is the spontaneous spin polarization due to LSOC. We have shown that the 0.5 structure can be made to appear or disappear by applying both positive and negative asymmetry to the lateral confining potential well. Finally, we have proposed a dual-QPC device to detect the spin polarization directly by transport measurement. We have not succeeded to detect the polarization. But it is possible to detect the spin polarization in number of ways.

First of all, we would like to improve the design of the dual-QPC device to detect the spin polarization directly via transport measurements. The dual-QPC device has two QPCs in series in which the QPCs *must* function independently. In other words, we should able to manipulate the gates of the two QPCs separately without influencing each other. This condition can be achieved by separating the two QPCs further apart (~ 2 μm). In that way, the length of the channel between the two QPCs will increase automatically. The channel will also be made wider (> 500 nm). Thus, the area between two QPCs will remain open with the application of gate bias voltages. The QPCs in dual-QPC device will then be set in a way that either both of them will allow the same kind of spin or they will allow the opposite spins. We would expect an undisturbed 0.5 structure when the QPCs will allow the same kind of spin otherwise a substantial drop in the conductance of the device— no transmission in the ideal case. Thus, we would be able to detect the spin polarization due to LSOC using the dual-QPC device.

Another possibility is to detect the spin polarization by a magnetic focusing technique. We propose a new device to detect the spin polarization based on the magnetic

focusing technique. There will be two QPC in this new device: one will act as Injector and the other will act as Detector. The schematic of the device is shown in Fig. 6.1. Due to the strong LSOC in the SG InAs QPC, the electrons are spin polarized and have different momenta. Therefore, the electrons have different cyclotron orbits in

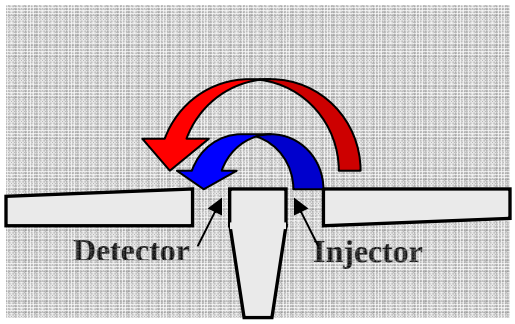

Fig. 6.1. Schematic of injector and detector QPCs and the trajectories of electrons with two spin states.

magnetic field. A current will be injected through the injector and the voltage drop will be measured across the detector. We would expect two voltage peaks at two different focusing magnetic fields corresponding to the two spin states, when the conductance value of both the injector and detector will be at $G = 2e^2/h$. With the lowering of the conductance of the injector, one would expect a slow disappearance of one of the peak.

The controlled creation, detection, and manipulation of spin-polarized currents by *purely electrical means* are challenges facing semiconductor spintronics. Finally, the SG QPC can be used as 100% spin polarizer and analyzer by *purely electrical means*, which are the essential tools to implement several semiconductor spintronics devices, such as spin filters and the Datta-Das spin-FET.