A Dissertation entitled Performance Improvement of Rigid and Flexible CdTe Solar Cells through CdCl2 Activation and Cu Engineering by

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Submitted to the Graduate Faculty as partial fulfillment of the requirements for the Doctor of Philosophy Degree in Physics

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The University of Toledo August 2022

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An Abstract of

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Cadmium telluride (CdTe) is a leading thin-film solar cell technology that achieved 22.1% small cell and 19% module efficiency. While for flexible CdTe solar cells, the record efficiency is around 16%. CdTe has an optimum direct band gap with a high absorption coefficient, which makes it possible to reduce electricity cost per watt by reducing material consumption compared to market-dominating silicon-based technology. However, this achievement is still far below its maximum theoretical limit (33%). Extensive research and development work is carried out to understand the differences between experimental and theoretical value by the universities, national labs, and the leading industries. So far, the understanding is that the major obstacle is the recombination-induced loss due to the deficient band alignment at the front interface, the low doping density, and the high work function of CdTe caused loss at the back interface. In this dissertation, we introduced a high band gap window layer, i.e., oxygenated cadmium sulfide (CdSO) and magnesium zinc oxide (MZO), to reduce parasitic loss at the front interface. Further, we studied ionic copper (Cu) doping, which generated a gradient Cu profile with most of the Cu concentrated at the back side of the CdTe. We

further demonstrated that ionic Cu doping could effectively reduce the bulk defect density and back-barrier height and improve the CdTe doping density.

Guided by these principles, we innovatively introduced a high band gap CuSeO₃ back buffer layer in CdTe solar cells. CuSeO₃ is a Cu-based compound that is the source of ionic Cu, acting as a hole transfer layer simultaneously to reduce the back barrier height. Additionally, we incorporated selenium at the front interface by thermally evaporating 130 nm cadmium selenide (CdSe) before CdTe deposition and formed CdSe_xTe_{1-x} alloy with composition and bandgap gradient (from 1.4 to 1.5 eV) at the front interface after CdCl₂ treatment. This reduced absorber bandgap at the front interface increases photon collection at longer wavelengths, improving current density and overall solar cell performances.

Further, we fabricated lightweight and flexible CdTe solar cells via delamination and reconstruction methods. Here, we developed three different delamination techniques: (1) water-assist lift-off, (2) mechanical lift-off, and (3) thermal stress delamination for rigid CdTe solar cells and finally fabricated CdTe solar cells with high specific power (W/kg).

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List of Abbreviations

AFM	Atomic Force Microscopy
СВ	Conduction Band
CBO/VBO	Conduction Band/Valance Band
CdTe	Cadmium Telluride
CdS	Cadmium Sulfide
CdSe	Cadmium Selenide
CdCl ₂	Cadmium Chloride
CSS	Closed Space Sublimation
Cu	Copper
CuCl	Copper(I) Chloride
CuCl ₂	Copper (II) Chloride
CuSCN	Copper Thiocyanide
CuSeO ₃	Copper Selenium Oxide
EDS	Energy Dispersive X-ray Spectroscopy
EQE	External Quantum Efficiency
FTO	Fluorine dope Tin Oxide (SnO ₂ :F)
HRT	High Resistive Transparent
IR	Infra-Red
ITO	Indium tin oxide
IZO	Indium zinc oxide
KPFM	Kelvin Probe Force Microscopy
MZO	Magnesium zinc oxide
PCE	Power Conversion Efficiency
PV	Photovoltaic
QNR	Quasi-Neutral Region
SCR	Space Charge Region
SEM	Scanning Electron Microscope
SLG	Soda Lime Glass
SHR	Shockley-Reed-Hall

TCO.....Transparent Conducting oxide

VB.....Valence Band

List of Symbols

θ	Angle
η	Power Conversion Efficiency
χ	Electron affinity
σ _t	Defect capture-cross-section area
A	Diode quality factor
С	Capacitance
	-
ε	Permittivity
E _A	Electron affinity of the conduction band
E _C	Electron affinity of the valance band
E _F	Fermi energy level
E _g	Energy band gap
Evac	Energy of vacuum level
FF	Fill Factor
J	Current density
J ₀	Dark saturation diode current density
J _{SC}	Short-circuit current density
J _{Dark}	Diode current measured in dark
Імр	Current density at the maximum power point
5 IVII	current density at the maximum power point
Kr	Boltzmann constant
К	Degrees Kelvin
Nd	Donor concentration
Ns	Acceptor concentration
Nc	Effective density of states at the edge of the conduction band
Ny	Effective density of states at the edge of the valance band
Nt	Tran density
ni	intrinsic electron concentration
n	Electron density
	indication denoity
Øn	Work function of n-type semiconductor
фп Øn	Work function of n-type semiconductor
۳۲	

Chapter 1

Introduction of Solar Cells

1.1 Motivation

The industrial revolution and the development of fast and effective transportation and communication systems brought people together and shared their ideas that helped improve the living standard and increase the global population. In the last two centuries, the global population has increased from around 1 billion to 7.5, soaring global energy demand. Fossil fuels supply about 80 % of this demand- and the remaining comes through different renewable energy sources, including solar, wind, hydro, biofuels, nuclear, and other forms of renewable sources [1]. Fossil fuels are based on carbon-rich organic compounds and burning fossil fuels produces a tremendous amount of carbon dioxides and other greenhouse gases. Moreover, extensive oil and gas extraction from the ground reduced insulators from the earth's inner core, which eventually heated the earth's surface. Climate.gov tracking shows the global average atmospheric carbon dioxide level of 412.5 parts per million (ppm) in 2020 is a new record high in the past 800,000 years [2] and is continuously increasing. As a result, global temperature has increased by 1 $^{\circ}$ C compared to the 20th century. Suppose the global temperature rises above 1.5 °C. In that case, it will cause a series of problems like increases in sea level, extreme weather conditions, a disorder in the ecosystem, food scarcity, and health problems for humans

and the entire planet. At present time, geopolitical instability fluctuates oil and gas prices, severely affecting the global economy, which motivates the search for alternative energy sources.

At the beginning of the 20th century, renewable energy, especially solar and wind, emerged as an alternative and sustainable solution for clean energy to overcome increasing energy demand. In 2021, nearly 10.3% of global energy came from wind and solar, which supplied 38% of the world's electricity. The most appreciating part is that solar energy generation rose by 23 %. [4] which is a promising achievement to reduce carbon emissions, keep global warming to 1.5 degrees as defined by the Paris Agreement by 2040 [3] and to reach net zero-emission of carbon by 2050 [3].

Among various renewable sources, solar energy is the most abundant energy resource. One report shows that total recoverable solar energy is 23,000 TW per year, whereas the present world energy demand is around 18TW-yr [4]. Therefore, solar energy has enormous potential to supply global clean energy demand.



Figure 1- 1 The spectral irradiance of the standard solar spectrum. Image: Adopted from http://thegreenstalk.com/2010/08/

Solar irradiance can be converted into solar thermal and solar photovoltaic energy. Electricity generated from solar photovoltaic technology depends on the solar cell material and its solar spectral response. Sun emits light in the range of wavelengths from ultraviolet, visible, and infrared spectrum. The amount of radiation received from the sun per unit area per unit time is called solar irradiation. The solar spectrum and irradiation are similar to the spectrum of 5760 K black body radiation (Figure 1- 1). Therefore, the sun can be assumed as black body radiation, which gives a basic theoretical framework for the photovoltaic study. The total solar irradiation outside the Earth's atmosphere is 1353 Wm⁻², called AM0. At sea level, solar radiation is reduced due to the absorption and scattering of light by the various atmospheric constituents, quantified by air mass (AM). Mathematically, the air mass is the ratio of optical path length to the sun to the optical path length if the sun is directly overhead. On the earth's surface (sea level), solar irradiation is about 1000 Wm⁻², is defined as AM1.5, and is the fundamental spectrum used to characterize photovoltaic cells. AM1.5 correspond to the position of the sun 42 degrees above the horizon. However, the overall efficiency of solar cell devices depends on the material properties. In 1961, Shockley and Queisser theoretically calculated the maximum efficiency for a single p-n junction solar cell [5]. According to them, the power conversion efficiency of a single-junction solar cell is a function of material band gap and their spectral response. Under AM1.5 illumination, the maximum solar conversion efficiency for a single junction solar cell with a band gap 1.4 eV is around 33 %. Therefore, the performance of an ideal single-junction solar cell depends on the choice of material. This calculation also known as the detailed balance limit, gives the roadmap for future innovation for new PV materials.

Based on the innovation and development of solar technology, it can be broadly divided into three generations. 1st generation includes monocrystalline and polycrystalline silicon cells. 2nd generation of solar cells is usually called thin-film solar cells. These solar cells are made from direct band gap materials having high absorption coefficients like amorphous silicon, gallium arsenide (GaAs), cadmium telluride (CdTe), and copper indium gallium diselenide (CIGS). 3rd generation includes novel solar cells like perovskite solar cells, organic solar cells, and tandem solar cells. Although crystalline silicon PV technology occupies more than 90 % of the total PV market, CdTebased PV technology is quickly growing with better lifetime advantages [6]. Figure 1- 2 summarizes the improvement train of the best research-cell efficiency maintained by NREL [7].

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Figure 1-2 NREL best research-cell efficiency chart[7].

1.2 Solar Cell Basics

1.2.1 Semiconductor

A semiconductor is the basic building block of solar cells. The solar cells' performance depends on the semiconductor properties like band gap, Fermi level, electron affinity, doping density, etc. A semiconductor band gap is an energy gap between the conduction band minima (E_C) and the valance band maxima (E_V). At absolute zero temperature, the conduction band is empty, the valance band is filled with electrons, and the Fermi level lies between E_C and E_V . Fermi energy is the energy level having a 50% probability of being filled with electrons. When increasing the temperature, electrons jump from the valance band to the conduction band. These mobile free electrons are the charge carrier of the conduction band. The electron deficiency in the valance band is considered positively charged pseudo-particles called a hole are the

charge carrier of the valance band. At equilibrium, the distribution of corresponding carriers (f_o) is given by a Fermi-Dirac distribution function.

$$f_o(E, E_F, T) = \frac{1}{e^{(E-E_F)/K_BT} + 1}$$

Where E_F is the Fermi energy level, K_B is the Boltzmann constant, and T is the absolute temperature.

While the position of the Fermi level in band gap can change by introducing impurities or dopants. For n-type semiconductor, Fermi level shifts towards the conduction band due to the presents of donors and for p-type semiconductor Fermi level shifts towards the valance band due to the presents of acceptors as shown in Figure 1- 3. When E_F is far away from both band edges (i.e., E_C and E_V), f_o can be well approximated by the Maxwell-Boltzmann distribution and the density of electron (n) or hole (p) can be calculated as:

$$n = N_C \exp\left((E_F - E_C)/K_B T\right)$$

Where the constant N_C is called effective state density at the conduction band.

$$p = N_C \exp\left((E_V - E_F)/K_B T\right)$$

Where the constant N_V is called the effective state density at the valance band.

The product of electron and hole density is constant, gives intrinsic carrier density n_i .

$$np = n_i^2 = N_C N_V e^{-E_g/K_B T}$$

Where $E_g = (E_C - E_V)$ is the bandgap of the semiconductor.

Electron affinity (χ) is another important quantity in semiconductor and photovoltaic. It is the amount of energy required by the semiconductor to move an electron from E_C to the vacuum level (E_{VAC}). E_{VAC} is the energy level at which electron is free of force in semiconductor.



Figure 1- 3 Position of Fermi level and acceptor/doner level related to the conduction band and valance band edges in semiconductors.

1.2.2 The P-N Junction and Solar Cells

A solar cell is a device which generates voltage under illumination. A produced voltage depends on electric charge asymmetry generated by the illumination. These

electric charge carriers are separated by the built-in filed. Traditionally a concept of p-n junction is used to define the built-in field in photovoltaics. When p-type semiconductor and n-type semiconductor materials are in contact, the excess holes from the p-type material diffuse towards the n-type region, and the excess electrons diffuse from the ntype material to the p-type region, leaving behind a charge-free region called the depletion region. It is also called space charge region (SCR). The opposite charge accumulates on either side of the depletion region; it sets up an electric field that opposes further diffusion of charge carriers across the junction and gets equilibrium. At this point, the Fermi level of n-region and p-region is equal, generating energy bands bending at the vicinity of the interface between two semiconductors and generating built-in potential (V_{bi}), which depends on the difference in the work function of semiconductor materials. But it is not necessary to have p-n junction in every solar cells, more detail can be found in book "Physics of Thin-Film Photovoltaics" [8]. The work function (ϕ) of materials is the minimum amount of energy required to move electrons to the vacuum level or the energy gap between the Fermi and vacuum levels. Mathematically:

$$V_{bi} = \frac{1}{q} \left(\phi_n - \phi_p \right)$$

Where q is electric charge, ϕ_n and ϕ_p are the work function of n-type and p-type semiconductor material respectively.

In the presence of dopants, the built-in potential can relate to doping level as:

$$V_{bi} = \frac{K_B T}{q} \left(\frac{N_d N_a}{n_i^2} \right)$$

Where, N_d is donor density and N_a is acceptor density.

Usually, a p-n heterojunction solar cell consists of either a n-type semiconductor window layer or a p-type semiconductor absorber layer or both. When photons are incident with energy greater than the bandgap of the absorber layer, photons will be absorbed and generate electron-hole pairs which are the essential function of the solar cell. Due to built-in potential, electrons diffuse towards the n-type layer, and holes diffused towards the p-type layer and collected through front and back metal electrodes. But at the same time, recombination of electron-hole pairs happens simultaneously due to presence various factors like recombination mechanism and defect level, which determines the overall performance of solar cells together with the electron-hole generation.

1.2.3 PV Characterization and Relevant Parameters

The performance of the solar cells is characterized by current density-voltage (J-V) measurement. J-V measurement is the fundamental characterization of any photovoltaic cell. Through the J-V curve, the photovoltaic parameters open-circuit voltage (V_{OC}), short-circuit current (J_{SC}), fill factor (FF), power conversion efficiency, series resistance (R_S), and shunt resistance (R_{SH}) are calculated.



Figure 1- 4 Current density-voltage (J-V) curve of a solar cell.

A J-V curve of the solar cell consists of dark and light-generated features. In the dark, solar cells show diode behavior. Under an applied voltage or bias, current flow through the solar cell in the dark is called dark current $(J_{Dark} (V))$, which flows opposite the photo-generated current. In the non-ideal case, to define the J-V characteristics following diode equation is used.

$$J = J_O\left\{\left[\exp\left[\frac{q(V_{OC} - J_L R_S)}{K_B T A}\right] - 1\right\} - J_L + \frac{V - J R_S}{R_P}$$

Where R_S is series resistance, and $R_P = R_{SH}$ is shunt resistance parallel to the cell are defined as parasitic resistances as shown in the circuit diagram of Figure 1- 4 and A is the diode ideality factor and other parameters has their standard meaning. Further in J-V curve a slope at V_{OC} is called open circuit resistance (R_{OC}) and the slope at J_{SC} is called short circuit resistance (R_{SC}) are calculated as following [9].

$$R_{SC} = \frac{R_S + R_S \frac{R_L}{R_P} + R_L \exp\left[\frac{q(V_{OC} - J_L R_S)}{K_B T A}\right]}{1 + \left(\frac{R_L}{R_P}\right) \exp\left[\frac{q(V_{OC} - J_L R_S)}{K_B T A}\right]}$$
$$R_{OC} = \frac{R_S + R_S \frac{R_L}{R_P} + R_L}{1 + \frac{R_L}{R_P}}$$
$$R_L = \frac{K_B T A}{q J_L}$$

In general, a series resistance arises from the semiconductor material's layers and contact metals. Higher series resistance reduces the FF and current collection in solar cells. The shunt resistance arises from leakage current generated by pinholes or the leakage through the edge of the solar cell. Therefore, a higher shunt resistance value is desirable for better device performance. An ideal solar cell $R_S \sim 0$ and $R_P = R_{SH} \sim \infty$. Then the diode equation becomes,

$$J = J_{SC} - J_{O} \left[exp \left(\frac{eV}{AK_{B}T} \right) - 1 \right]$$

Where diode ideality factor A define how much solar cell diode deviated from an ideal diode. For and ideal solar cells A=1, where recombination is limited by only minority carrier recombination. It A=2 than the recombination is limited by both minority and majority charge carrier. However, in solar cells its value varies between 1 to 5 [8].

Under illumination of solar cell, an electron-hole pairs are generated and separated by built-in potential which flow photocurrent opposite to the dark current due to which J-V curve shifts up as shown in Figure 1- 4. Under illumination of the solar cells, a photo-excited charge generates voltage (i.e., potential difference between front and back contacts). If the two opposite terminals of a solar cell are isolated, then the potential difference between them is called open-circuit voltage (V_{OC}). It is the maximum voltage available to drown out from the solar cell. Mathematically:

$$V_{OC} = \frac{AK_{B}T}{q} ln \left[\frac{J_{SC}}{J_{o}} + 1 \right]$$

Where dark saturation current (J_o) is a current generated by the thermally generated electron-hole pairs, also called reverse saturation current. A diffusive flow of minority electron from p-region to n-region and hole flow from n-region to p-region creates a dark saturation current. So, the more prominent dark saturation current means more significant recombination at the interface.

 J_{SC} is short-circuit current is maximum current generated in a solar cell is measured when two terminals are connected without a load resistor (short-circuit).

Fill factor (FF) is one of the vital parameters of solar cell analysis. At V_{OC} point, the current density is zero and at J_{SC} point, external voltage is zero. Therefore, a product

of maximum voltage and current in a solar cell does not characterize the maximum power of the solar cell. Then a term fill factor (FF) is defined as ratio of a maximum power of solar cell to the product of V_{OC} and J_{SC} . FF is equivalent to the area under the J-V curve. FF is essential to determine the power conversion efficiency of the solar cells. Mathematically:

$$FF = \frac{J_{MP} \cdot V_{MP}}{J_{sc} \cdot V_{OC}}$$

Finally, the most important term of photovoltaic characterization is power conversion, defined as the ratio of maximum power (J_{MP}, V_{MP}) generated by the solar cell to the incident solar power gives the efficiency.

$$\eta = \frac{J_{SC.}V_{oc}.FF}{P_S}$$

Where, P_S is the input power of light for solar cell.



Figure 1- 5 Quantum efficiency of a CdTe solar cell measured at AM1.5 spectrum (Adopted fron https://www.pveducation.org/pvcdrom/solar-cell-operation/quantum-efficiency).

Quantum efficiency (QE) is another important term that gives the relation between J_{SC} and the incident spectrum. External Quantum efficiency (EQE) is expressed as the probability of an incident photon with energy E delivering one electron to the external circuit. The EQE of a photon with energy below the band gap is zero, and EQE of the photon with higher energy than the band gap is also lower than 100% due to the presentation of recombination in the solar cell device. An ideal EQE curve is square, but in the actual case, it is reduced into a curve shape, as shown in Figure 1- 5 due to recombination effects in the device and insufficient absorption by the absorbing material. Real EQE depends on the solar cell material's absorption coefficient, charge separation, and collection efficiency but does not depend on the incident spectrum. Therefore, it is essential to study solar cells under different conditions comparatively.

1.3 Dissertation Outline

CdTe solar cell technology is commercially successful and a leading thin-film technology. First Solar Inc. delivers a world-record PCE of 22.1 % on a lab-scale and 19 % PCE in their module [9], approaching the market-dominant crystalline silicon photovoltaic technologies (26.1% and 24.4%). However, these PCE values are still far below the theoretical efficiencies (> 30%) predicted by the Shockley–Queisser limit [6]. This inferior performance is mainly due to the current loss caused by the parasitic light absorption by the front buffer layer, and V_{OC} and FF loss due to the non-Ohmic back contact caused by the high CdTe electron affinity (4.4 eV) and inferior carrier transport caused by the low carrier density (10¹⁴ cm⁻³) of CdTe. Therefore, this dissertation aims to build an understanding for high quality front/back interface and bulk doping for efficient rigid CdTe solar cells and further introduces lightweight and flexible CdTe solar cells. This thesis starts with the background and motivation of solar cells Chapter 1 Followed with the introduction of the fundamental of cadmium telluride (CdTe) solar cells in Chapter 2.

Chapter 3 presents the research results on Cu doping, aiming to improve the carrier density and reduce the recombination at the front and back interfaces. Traditionally, Cu is used as a dopant to increase p-types conductivity of CdTe and to improve the back contact junction. However, an excessive amount of Cu causes long-term stability problems. To overcome this problem, we develop the ionic Cu doping for

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CdTe with a comparative study with metallic Cu. Further, we studied the effect of Cu doping in CdTe devices with two different front buffer layers, namely oxygenated CdS and wide band gap magnesium zinc oxide (ZMO) and a detailed discussion of the result was reported.

Chapter 4 introduces the wide band gap back-buffer layer CuSeO₃ for CdTe devices. The characterization of the band gap of CuSeO₃ buffer layer, details about solution preparation, device fabrication, and solar cell performance with electrical characterization were conducted in this section to understand the effect of CuSeO₃ in CdTe solar cells. CuSeO₃ as a hole transport material is also further applied in CdSe/CdTe solar cells. After careful CdCl₂ optimization low band gap CdSe_xTe_{1-x} absorber layer is introduced at the front interface which busted the current collection. Figure 1- 6 summarizes the physical structure of three different rigid CdTe solar cell devices in chapter 3 and 4.



Figure 1- 6 The Physical structure of baseline rigid CdTe solar cell fabricated at UT.

Chapter 5 presents the lightweight and flexible CdTe solar cells fabricated using a water-assisted lift-off process. Chapter 5 shows the technologies to delaminate CdS/CdTe film stacks from a mediator substrate mica and transfer it to a substrate of interest. Due to the sensitivity of mica to humidity, thermally evaporated CdCl₂ treatment instead of traditional solution method was conducted and optimized for CdS and CdTe buffer layers. Our results suggest that the CdCl₂ treatment for the CdS buffer layer is essential to improve performance of flexible devices. Further, mechanical delamination of CdSe/CdTe from mica sheet and thermal stress generate delamination of rigid CdSe/CdTe solar cells from glass was introduced to fabricate high specific power flexible solar cells. Figure 1- 7 summarizes the physical structure of flexible and lightweight CdTe solar cell fabricated in this thesis.

Finally, chapter 6 summarizes the work of dissertation and provides suggestions for future works.



Figure 1- 7 The Physical structure of baseline flexible CdTe solar cells fabricated at the UT.
Chapter 2

Fundamentals of CdTe Solar Cells

2.1 Introduction

CdTe solar cells are dominated by the superstrate configuration, which is fabricated on a rigid glass substrate through which the light illuminates the devices. While its counterpart substrate configuration, which gives the flexibility of using an opaque substrate, has rarely been investigated due to its low electron diffusion length in CdTe film. No matter which kind of device configuration, the device consists of transparent conduction oxides (TCO), front window layer, CdTe absorber layer, and back contact layers. Due to the unique material properties compared to other streamed photovoltaics, such as crystalline silicon, CIGS, and hybrid halide perovskite solar cells, each layer being used in CdTe solar cells has special requirements to maximize the device performance. This chapter describes these essential parts of CdTe solar cells.

2.2 Transparent Conductive Oxide (TCO)

Transparent conduction oxide (TCOs) is a doped metal oxide with a wide band gap (>3.0 eV), excellent transmittance (>80%) of the incident light, high conductivity, high mobility, and high doping density. TCO can be deposited by various deposition methods like reactive magnetron sputtering, metal-organic chemical vapor deposition (MOCVD), metal-organic chemical beam deposition (MOCBD), and chemical bath deposition (CBD), and pulsed laser deposition (PLD). TCO is an essential part of solar cells, which allow photons passes to absorb layers and generate electron-hole pairs. The photo-generated electrons diffuse/drift to the TCO layer and then to the external circuit. Therefore, TCO should require high transparency, conductivity, and mobility. Tin oxide (SnO₂), fluorine-doped thin oxide (FTO), indium zinc oxide (IZO), and indium tin oxide (ITO) are the most popular TCO layers used in solar cells because of their high stability, high transmittance, and optimum electric properties.

For superstrate CdTe solar cells, due to the high deposition temperature of CdTe films (>600 °C), FTO shows outperforming properties due to its higher stability than IZO and ITO, i.e., NSG TECTM provided by Pilkington North America. A property of selected commercial TCO supplied by Pilkington North America is listed in the table below (Table 2- 1). NSG TECTM T12D and NSG TECTM T15M glasses are coated with intrinsic SnO₂, a high resistive transparent (HRT) layer. For substrate CdTe solar cells, normally sputtered ITO or IZO, which don't need high temperature annealing for desired conductivity are used as a TCO.

Product	Thickness (mm)	Transmittance (%)	Sheet Resistance	
			(Ohm/sq.)	
NSG TEC TM T10	3.2	80	9	
NSG TEC TM T12	3.2	80	12	
NSG TEC TM T12D	3.2	82	12	
NSG TEC TM T15	3.2	84	15	
NSG TEC TM T15M	3.2	81	15	

Table 2-1 Optical property of commercially available TCO layers.

2.3 Window Layer

A window layer, also known as an emitter, is used in solar cells to create a p-n heterojunction in a CdTe solar cells. To be a window layer, the material is required to have wide bandgap to reduce the parasitic absorption loss, high conductivity to improve the build-in potential, well matched band alignment with the absorber to reduce the interface recombination. An efficient window layer should have a wider band gap (>2.6 eV), thinner (50 to 100 nm), and high transmittance to allow the light directly to the absorber layer. Compared to the absorber layer, the high doping density of the window layer creates a wider quasi-Fermi level splitting and a larger built-in potential that helps separate generated charge carriers. A CdTe is a single heterojunction solar cell where p-type doped CdTe is an absorber layer and n-type doped semiconductor material like CdS and ZMO are used as a window layer. The performance of the CdTe solar cell solely depends on the properties of these window layers, defined below:

2.3.1 Cadmium Sulfide (CdS)

CdS is a direct band gap semiconductor (2.42 eV) material with wurtzite (hexagonal) and Zinc-Blende (cubic) structure. It is stable and has high conductivity at room temperature. Several deposition techniques have been developed for CdS thin film, like RF magnetic sputtering, CBD, close space sublimation (CSS), etc. Among them, sputtering and CBD are the most popular methods. In the mid-1960s, CdS/CdTe heterojunction diodes were firstly studied for solar cells [10]. Later this structure evolved as a successful candidate for photovoltaic conversion [11]. Since then, CdS has been the first-choice window layer in CdTe solar cells until 2010s.

The parameters of CdS are very crucial for efficient CdS/CdTe solar cells. For example, by reducing the thickness of CdS, more light can transmit to the CdTe region and improve the J_{SC} [12]. This is because the blue light absorbed by CdS layer does not contribute to photocurrent, known as parasitic absorption loss. However, thinner CdS (<50 nm) can't fully cover the FTO underneath, which would result with nonuniform subsequential CdTe deposition and create shunting paths between TCO and CdTe as well, resulting in a decrease in overall device performance. To overcome the shunting effect, thin HRT layer, i.e., intrinsic SnO₂, is inserted in between TCO and CdS. Additionally, the existence of lattice mismatch between the hexagonal CdS and cubic CdTe (~10 %), a negative conduction band offset (cliff) at the CdS/CdTe interface induces less downward band bending in the vicinity of the CdTe side, resulting with a large hole carrier density. This would increase the cross-interfacial recombination when the photogenerated electrons drifting through the CdS/CdTe interface. As a result, the diode saturation current increases, reducing with low Voc and device performance [13].

To overcome these issues some modifications are made on CdS by changing the deposition conditions and parameters, post deposition treatment or by applying direct electric field which create a strong piezo- or pyro active effect on CdS film. Under modified condition a dipole types of electric polarization create a static electric field on CdS film which strongly effect the charge separation in photovoltaic device [9]. On the other hand, experimentally CdS buffer layer was modified by incorporating oxygen, forming a oxygenated CdS (CdSO) layer with a larger bandgap and up-shifted CBM as shown in Figure 2-1. Thus, both the parasitic light loss caused by window layer and the interfacial recombination due to the negative conduction band offset are reduced. As a result, both the J_{SC} and V_{OC} can be significantly improved [14-16]. However, the optimum band gap for the oxygenated CdS window layer is around 2.6 eV, which is still relatively small. Further increasing the oxygenation level would increase the resistivity of CdSO and controversially reduce the device performance. It is recommended to introduce a more suitable semiconductor material with a wider band gap like magnesium zinc oxide (ZMO).



Figure 2-1 Transmittance spectrum and Tauc plot of 600 nm CdS and CdSO film.

2.3.2 Magnesium Zinc Oxide (ZMO)

Zinc oxide (ZnO) has a band gap of 3.37 eV and Magnesium oxide (MgO) has band gap of about 7.6 eV. Mixing ZnO and MgO forms an alloy $Mg_xZn_{1-x}O$ (ZMO) with tunable bandgap from 3.37 to 7.8 eV by adjusting the composition ratio of MgO and ZnO, which makes it the most promising material for CdTe solar cells[17-19]. As the Mg concentration increases, the band gap of ZMO increases with modified optical and electrical properties, i.e., higher transparency, shallower CBM, et. al.[17, 20]. Thereby, a positive conduction band offset (CBO), the so-called spike, forms at the ZMO/CdTe interface [21]. A 1D-SCAPS simulation helped to understand the effect of positive CBO. An input parameter for SCAPS modeling is tabulated in

Table 2- 2. Figure 2- 2a shows the simulated band diagram of CdS/CdTe (cliff at CBO) and ZMO/CdTe (spike at CBO) solar cells. It shows that spike-like offset for ZMO/CdTe device generates downward band bending, creating a higher potential barrier for holes. It reduced interface recombination at ZMO/CdTe interface compared to the

CdS/CdTe interface and improves the V_{OC} and overall device performance (Figure 2- 2b). Further, device modeling has shown that a small spike is beneficial for high-performing devices because it introduces a large barrier for the hole to reach the interface due to the downward band bending, reducing the nonradiative recombination at the front interface. But a high CBO (>0.3 eV) generally introduces a significant barrier at the ZMO/CdTe interface that blocks electrons transferring from CdTe into TCO electrode, increase interface recombination velocity, and causing the S-kink in the J-V curves, leading to poor FF and low J_{SC} (Figure 2- 3a-b) [13, 21, 22]. Additionally, the electron conductivity of ZMO film can be varied by tuning the concentration of oxygen vacancies, which supplies possibilities to reduce the barrier caused by the large CBO values and eliminate the S-kink in the J-V curves, a SCAPS simulated J-V corresponding to different ZMO conductivity clearly shows in Figure 2- 3c that with increasing conductivity of ZMO Skink removed due to significantly reduced in interface recombination (Figure 2- 3d).



Figure 2- 2 Simulated band bending for CdS/CdTe and ZMO/CdTe SCAPS and their effect on J-V curve.



Figure 2- 3 SCAPS simulated band diagram for CBO, (b) simulated J-V curve, (c) J-V curve at different ZMO conductivity with CBO 0.4 eV, and (d) ZMO/CdTe interface current density.

Table 2- 2 SCAPS input parameters were used to simulate band diagram and J-V curves of CdS/CdTe and ZMO/CdTe solar cells with different work functions.

Parameters	FTO	CdS	ZMO	CdTe
Thickness (nm)	400	80	80	4000
Band gap (eV)	3.6	2.42	3.7	1.45
Electron affinity (eV)	4.4	4.5	4.2 (Vary)	4.4
Dielectric constant	9.0	10	10	10
CB DOS N _C (cm ⁻³)	2.2 x 10 ⁺¹⁸	2.2 x 10 ⁺¹⁸	2.2 x 10 ⁺¹⁸	8. x 10 ⁺¹⁷
VB DOS N _D (cm ⁻³)	1.9 x 10 ⁺¹⁹	1.9 x 10 ⁺¹⁹	1.9 x 10 ⁺¹⁹	1.8 x 10 ⁺¹⁹
Electron mobility (cm ² /s)	100	100	100	320
Hole mobility (cm ² /s)	25	25	25	40
Shallow donor	1.0 x 10 ⁺¹⁹	1.0 x ¹⁰⁺¹⁶	(vary)	
density (cm ⁻³)				
Shallow acceptor				5.0 x 10 ⁺¹⁴
density (cm ⁻³)				
Lifetime (ns)	0.1/0.1	0.001/0.001	1/1	10/10
Interfaces	S _n (cm/s)	S _p (cm/s)		
(ZMO/CdTe)	1.0 x 10 ⁺⁶	1.0 x 10 ⁺⁶		
(CdS/CdTe)	1.0 x 10 ⁺⁶	1.0 x 10 ⁺⁶		

2.4 Cadmium Telluride (CdTe) Absorber Layer

A direct band gap of 1.5 eV and a relatively high absorption coefficient of 1×10^4 cm⁻¹ makes CdTe an excellent absorption material for solar cell applications [23]. These key properties of CdTe allow it to absorb 99 % usable sunlight in less than 2 µm thick film. CdTe can exist in p-type, n-type, or i-type depending on the doping condition. Ptype doped polycrystalline CdTe is widely used for CdTe-based solar cells where Cu and Group V elements are successfully used as a dopant. A various deposition methods are used to make CdTe film, e.g., RF-sputtering [24], closed-space sublimation (CSS) [15, 25], vapor transport deposition (VTD) [26], and thermal evaporation [27]. The quality of the CdTe absorber layer significantly depends on the deposition technique. For example, sputtered CdTe has a slow deposition rate and small grain size in compared to CSS deposited CdTe, but the film is dense and highly uniform. CSS is the most popular CdTe deposition technique in academic research. In comparison to sputter deposition, CSS has a high deposition rate: within 3 minutes, it gives 4-micron thick CdTe film. The thickness and deposition time depend on sublimation temperature, substrate temperature, and pressure, which also control the properties of CdTe film sublimated. Further, the properties of CdTe film depends on the substrate used to for the deposition. Figure 2-4 is the photo image of the homemade CSS system used to deposit CdTe film at the University of Toledo.



Figure 2-4 Close-space sublimation system for CdTe deposition.

2.5 Cadmium Chloride (CdCl₂) Treatment

CdCl₂ treatment, which is conducted after CdTe deposition, is a vital processing step for highly efficient CdTe devices. The CdCl₂ treatment for CdTe solar cells was first reported in the mid-1970s [26]. Since then, CdCl₂ treatment was widely used for highefficiency polycrystalline CdTe solar cell. CdCl₂ treatment can drastically improve the power conversion efficiency from single-digit to double-digit figures, which makes it an inevitable step for CdTe-based photovoltaic cells. This treatment has been introduced in CdTe thin film by various methods like thermal evaporation [28], close space sublimation [29], and spray coating [30], followed with annealing treatment at a temperature range from 350 to 450 °C for 20-60 mins in air atmosphere. The multiple effects of CdCl₂ treatment are discussed below:

2.5.1 Grain Growth and Recrystallization

CdCl₂ treatment has a noticeable influence on grain growth, grain boundaries reduction, and recrystallization of CdTe film. Less grain boundaries generally indicate lower defects density and smaller probability for the carriers being scattered in CdTe. Grain growth and recrystallization has been observed in sputtered, low-temperature deposited CdTe, which initially has a relatively small grain size. Further, the carrier gas during of CdCl₂ treatment atmosphere can determine the surface morphology of CdTe film. CdTe treated in dry air (i.e., containing oxygen) shows a larger grain size than the CdCl₂ in inert gas, e.g., helium. It suggests that chlorination in an oxygen environment is beneficial for recrystallizing the CdTe grains and improving the electric properties of the device. Chapter 5 will define grain growth and recrystallization effect of CdCl₂ treatment for both CdS window layer and CdTe absorber layer. However, oxygen in the CdCl₂ treatment is not always beneficial depending on the device configuration.

In our previous work we observed that, CdCl₂ treatment in an environment with oxygen is detrimental for ZMO/CdTe device. It is believed that oxygen can migrate to the ZMO buffer layer and reduce ZMO conductivity and introduces a S-kink in J-V curves. Therefore oxygen free CdCl2 treatment is recommended for ZMO/CdTe define to eliminate J-V distortion [21].

2.5.2 Grain Boundary Passivation

Grain boundaries are the dip gap states in polycrystalline CdTe. They act as a nonradiative recombination centers. Interestingly CdCl₂ treated device has fewer grain boundaries and superior device performance. It means there should be relation between

CdCl₂ treatment and grain boundary passivation. Chen Li and co-workers used electron beam induced current (EBIC) microscopy to study the CdCl₂ treated CdTe and observed that Cl atoms replaced Te atoms are mainly incorporated in CdTe grain boundaries. Through the microscopic and first principle-based calculation, they found that Cl aggregating converts grain boundaries from p-type to n-type while the grain interior is still p-type. This inversion of grain boundaries produces a local electric field that provides a more efficient pathway for electron-hole pair separation [31].

Additionally, CdCl₂ treatment introduced point defects Cl_i and Cl_{Te}. Krasikov and Sankin calculated that an interstitial point defect Cl_i quickly bind with Te_{Cd} to form a most stable neutral complex (Cl_i-Te_{Cd}). Moreover, an excessive amount of Cl_i also forms some neutral complex defects like (Cl_i - Cl_i) and (Cl_i - Cl_{Te}), due to which Cl does not affect the conductivity of CdTe. Later, after the Cu doping, Cl forms a complex defects with Cu that affects the conductivity of the CdTe depends on the doping concentration and diffusing of Cu atoms[32].

2.5.3 Interface Interdiffusion

CdS and CdTe has about 10% lattice mismatch, which generates structural defects at the interface [33]. CdCl₂ treatment appears as a key processing step to mitigate the effect of lattice mismatch by enhancing the diffusion of S and Te to produce a ternary compound (CdS_xTe_{1-x}) and create a graded band gap structure at CdS/CdTe interface. The diffusion of S to create CdS_xTe_{1-x} phase entirely depends on the CdCl₂ treatment temperature. While the low solubility of S in CdTe limits the diffusion depth of S, resulting with a CdS_xTe_{1-x} phase with x< 5 % near the interface [34].

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Figure 2- 5 Band gap bowing effect of CdSe_xTe_{1-x} measured and calculated by different method [35]. Reproduced from Advanced Thin Film Materials for Photovoltaic Applications" Coatings <u>http://shura.shu.ac.uk/</u> with permission.

While CdSe_xTe_{1-x} alloy with large x range from 0 to 1 can be created at the front interface through CdCl₂ treatment for the CdSe/CdTe bilayer. This is because Se has a high solubility in CdTe. Colegrove et.al., reported that Se diffusion rate is much higher in CdCl₂ treatment than the thermal annealing without the application of CdCl₂. A suitable CdCl₂ treatment condition can create an optimum low band gap CdSe_xTe_{1-x} alloy by optical bowing[35, 36], allowing additional infrared photons to be absorbed, leading to increased J_{SC} of CdSe/CdTe solar cells. Figure 2- 5 summarize the band gap bowing in CdSe_xTe_{1-x} alloy measured through different experimental methods and first-principles DFT calculation showing similar patterns. Incorporation of Se in a front interface of CdTe is groundbreaking achievement. Cathodoluminescence measurement shows that Se diffuse through grain boundaries and passivate deep level defect at the front interface due to which carrier lifetime and the overall device performance improved [37, 38]. Various reports suggest that optimum band gap for $CdSe_xTe_{1-x}$ is with 0.2<x<0.35 [27, 39, 40]. For x > 0.35, $CdSe_xTe_{1-x}$ change from cubical to cubical + hexagonal structure which create a photoinactive layer might be the one region for lower device performance [40, 41].

2.6 Doping and Back Contact Buffer Layer

CdTe has a high work function of 5.75 eV and no metal can match with CdTe to form a Ohmic contact, creating a metal-semiconductor barrier called the Schottky barrier. This barrier opposes the extraction of the hole and increases back surface recombination, which limits the current in large forward bias, appearing as a 'rollover' effect in device J-V curves. If the device has a severe rollover characteristic, both the V_{OC} and FF are suppressed. To reduce the effect of the Schottky barrier, various approaches has been reported in the past decades. It has been demonstrated to be an efficient approach to dope the CdTe with Cu prior to metal electrode deposition [42-45]. When Cu is added in CdTe, Cu substitute the cadmium vacancy sites (V_{Cd}) to create non-shallow acceptor point defect Cu_{Cd}. The solubility level of Cu in CdTe is about 3 x 10¹⁴ atoms per cm³ [46, 47] which is like the measured CdTe doping density. However, the amount of Cu added on CdTe is way large. When about 3 ~ 4 nm Cu is added on rare side of CdTe it introduced about 1×10^{19} atoms per cm³ [48]. This excessive amount of Cu segregate on grain boundaries and create Cu interstitial point defect (Cu_i) which is shallow donor in nature and generate compensative effect. Cu is doped after the CdCl₂ treatment. It means

there are already Cl related defect sides on CdTe. So, Cu also formed some complex defects like ($Cl_i - Cu_{Cd}$) is donor defect which gives compensative effect [32]. Also, the Cu migration introduces a concern about long-term stability of CdTe solar cells [49]. To reduce the compensative effect an effective control Cu doping is needed which will be explain in Chapter 3. Another alternative approach to CdTe doping and mitigate fast Cu diffusion is to introduce a buffer layer between CdTe and metal contact. Various organic and non-organic hole transfer layers are successfully applied after the $CdCl_2$ treatment to improve the back junction quality. ZnTe has been extensively used as a successful back buffer layer between CdTe and metal contact. ZnTe has a similar lattice structure to CdTe with a small valance band offset ($\sim -0.14 \text{ eV}$) [50], due to which it gives a better band alignment. ZnTe also act as electron reflector due to its large conduction band offset with CdTe, which helps to reduce the back surface recombination. Further, one of our work shows that Cu doped ZnTe can achieve a doping concentration up to 10¹⁹ cm⁻³ [51]. Solution processed Cu contain compounds like CuSCN is another successful back buffer layer which can significantly reduce the back barrier height [52, 53] with facile procedure and low cost. We developed $CuSeO_3$ as a hole transfer layer in CdTe, which will be describe in chapter 4.

Chapter 3

Effect of Cu Precursor on the Performance of Efficient CdTe Solar Cells

Copper (Cu) incorporation is a key process for fabricating efficient CdTe-based thin-film solar cells and has been used in CdTe-based solar cell module manufacturing. Here, we investigate the effects of Cu precursors on the performance of CdTe-based thinfilm solar cells by incorporating Cu through post-deposition annealing using a metallic Cu source (evaporated Cu) and ionic Cu sources (solution-processed cuprous chloride (CuCl) and copper chloride (CuCl₂)). We find that ionic Cu precursors offer much better control of Cu diffusion than the metallic Cu precursor, producing better front junction quality, lower back-barrier heights, and better bulk defect property than those fabricated using the metallic Cu source. Finally, outperforming power conversion efficiencies of 17.2 and 17.5% are obtained for devices with cadmium sulfide and zinc magnesium oxide as the front window layers, respectively which are among the highest reported CdTe solar cells efficiencies. Our results suggest that an ionic Cu precursor is preferred as the dopant to fabricate efficient CdTe thin-film solar cells and modules. The content of this chapter is based on a research paper published in ACS Materials and Interfaces2021 13(32), 38432-38440, entitled "Effect of Cu Precursor on the Performance of Efficient CdTe Solar Cells" and done by Sandip S Bista, Deng-Bing Li, Rasha A Awni, Zhaoning Song, Kamala K Subedi, Niraj Shrestha, Suman Rijal, Sabin Neupane, Corey R Grice, Adam B Phillips, Randy J Ellingson, Michael Heben, Jian V Li, and Yanfa Yan reprinted with permission ACS publication and Elsevier respectively.

3.1 Introduction

Cadmium Telluride (CdTe) solar cell technology has been attracting extensive attention due to its low cost and ideal bandgap for high-efficiency photovoltaics [54]. First Solar, LLC has reported the highest power conversion efficiencies (PCEs) of 22.1% for small area cells and 19% for modules, providing a competitive alternative for traditional silicon photovoltaics [55]. For the most efficient CdTe solar cells and modules, copper (Cu) is applied as a dopant to improve the p-type conductivity of the CdTe absorber and to reduce the Schottky-barrier height between the CdTe and the back contact [48, 56-58]. Cu incorporation is typically done via the post-deposition of a thin layer of Cu source material on CdCl₂-treated CdTe thin films. The Cu concentration ([59]) and distribution in the CdTe absorber layer can significantly influence the performance of CdTe solar cells. For example, excessive Cu incorporation can introduce interstitial defects (Cu_i) and other Cu related compensation complexes, e.g., Cu_i-Cu_{Cd}, [32] which would limit the hole density in CdTe films. Additionally, Cu_i ions can diffuse at high speed due to their high solubility at grain boundaries, [60-63] which adversely affects the long-term stability of CdTe solar cells [64-66]. More importantly, Cu at the front interfaces (e.g., the cadmium sulfide (CdS)/CdTe and zinc magnesium oxide (ZMO)/CdTe interfaces) has been thought to form recombination centers and shunting pathways, leading to the degradation of device performance [48, 67]. Therefore, the Cu dosage and distribution in CdTe films should be well controlled to minimize the nonradiative recombination related to Cu doping and maximize the device's performance and long-term stability.

In this regard, various Cu precursors have been used as the Cu source to fabricate CdTe thin-film solar cells. In general, two kinds of Cu precursors, namely, metallic Cu and Cu ions, have been used for Cu incorporation, including metallic Cu, [68] covalent Cu compounds, e.g., Cu_xTe, [69] Cu doped ZnTe, [70] and ionic Cu compounds, e.g., CuSCN,[71, 72] cuprous chloride (CuCl), [48, 57, 58] copper chloride (CuCl₂) [73, 74]. Among them, CuCl and CuCl₂ have attracted extensive attention due to its outstanding performance. Recently, CuCl₂ was incorporated in the CdTe absorber as the Cu precursor to eliminate the diffusion of Cu into the front junction, achieving a maximum PCE of ~16% [73]. Sites, Sampath, and coworkers have demonstrated a record PCE of 19.1% for CdSeTe solar cells using the CuCl precursor deposited by close space sublimation (CSS) [57, 75]. We previously reported a PCE of 17.5% for CdTe solar cells (no selenium) using a solution-processed CuCl treatment with a rapid thermal annealing process [48]. However, to date, comparative investigations on the impact of Cu precursors have rarely been reported.

Here, we report on a comparative study of the effects of Cu precursors on the performance of CdTe-based thin-film solar cells. Please note that no etching treatment is

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performed on the chlorinated CdTe film in this work. We fabricate CdTe thin film solar cells using a metallic Cu source (evaporated Cu) and ionic Cu sources (solution processed CuCl and CuCl₂). We find that the ionic Cu precursors offer much better control of Cu diffusion than the metallic Cu precursor. The statistical analysis of a large number of CdTe solar cells shows that the cells fabricated using the ionic Cu source show better front junction quality, lower back barrier heights, and better bulk defect property than the cells fabricated using the metallic Cu source. CuCl and CuCl₂, with different oxidation states of Cu, deliver almost the same performance for CdTe solar cells, which are much better than the cells used for the metallic Cu source. Our results show that the ionic Cu precursor plays a critical role in controlling the Cu dosage and establishing a desired Cu distribution profile.

3.2 Experimental Section

CdTe solar cells with two kinds of electron transport layers, i.e., CdS and ZMO, were fabricated. For the CdS/CdTe devices, fluorine doped tin oxide (FTO) coated glass (TEC 12D; NSG, US) with a 30 nm intrinsic SnO₂ layer was used as the substrate. First, an oxygenated cadmium sulfide (CdS:O) window layer with a thickness of 60 nm was deposited by radio-frequency (RF) magnetic sputtering using a 2-inch CdS target in a 2% oxygen and 98% argon environment at room temperature under 10 mTorr pressure and 50 W power. A 4-µm CdTe absorber was deposited by CSS at the source and substrate temperatures of 660 and 590 °C, respectively, at 10 Torr pressure, followed by a wet cadmium chloride (CdCl₂) treatment at 390 °C for 30 min in dry air.[25]

For the ZMO/CdTe devices, FTO coated glass (TEC 12; NSG, US) was used as the substrate according to our previous work.[48] A 80 nm ZMO window layer was deposited using a commercial ZMO target (8 wt% MgO) by RF sputtering with a flow gas of 16 sccm of pure argon and 24 sccm mixture gas of 95% argon and 5% oxygen. After a 10 min UV-ozone treatment for the as-deposited ZMO window layer, a $3.5 \mu m$ CdTe film was deposited by CSS with a source temperature of 560 °C and a substrate temperature of 495 °C under 1 Torr. Then, a CdCl₂ treatment was carried out at 420 °C for 20 min with a helium (He) flow (500 sccm) at 500 Torr.

After $CdCl_2$ treatment, the samples were rinsed with methanol to remove the residual CdCl₂ from the back surface. Then, three different Cu precursors were used to incorporate Cu for both CdS/CdTe and ZMO/CdTe devices. It is noted that no etching treatment was performed after $CdCl_2$ treatment for all the devices. The first Cu precursor was metallic Cu: a bilayer electrode of Cu (4 nm for CdS/CdTe and 3 nm for ZMO/CdTe devices) and Au (40 nm) was deposited by thermal evaporation with an individual cell area of 0.08 cm^2 , followed by an optimum activation treatment at 200 °C for 20 min. The second precursor was CuCl. First the CuCl solution is prepared by dissolving CuCl powders into 20 ml ethanol solvent followed by an ultrasonic treatment for 2 min. Note that CuCl should be oversaturated, as evidenced by the undissolved CuCl particles in the bottom of solution. The supernatant fluid was then used for the CuCl treatment. The Cu ion concentration in CuCl solution was 3.10 µg/mL, was measured by using inductively coupled plasma mass spectroscopy (ICP-MS). For the device with the CuCl treatment, different volumes of saturated CuCl solution were dropped onto the CdTe surface and annealing at different temperature to optimize the device performance. A saturated CuCl

volume of 100 μ L for CdS/CdTe and 80 μ L for ZMO/CdTe devices are optimum volume was used to drop and spread on a $1.5'' \times 1.5''$ CdTe surface and drying naturally and the sample were treated through short annealing time called rapid thermal annealing (RTA). After making series of the samples, RTA process is optimum at 200 °C for CdS/CdTe and 160 °C for ZMO/CdTe devices with a ramping speed ~60 °C/min without dwelling time in a 500 sccm He flow. The third precursor was CuCl₂: a CuCl₂ solution (with Cu a concentration of $3.10 \,\mu\text{g/mL}$ which is equivalent to the concentration of Cu in CuCl solution, 100 μ L for CdS/CdTe and 80 μ L for ZMO/CdTe devices) was used to drop and spread on a $1.5'' \times 1.5''$ CdTe surface. After drying naturally, the samples were treated through rapid thermal annealing (RTA) (at 200 °C for CdS/CdTe and 160 °C for ZMO/CdTe devices) with a ramping speed ~60 °C/min without dwelling time in a 500 sccm He flow. Here 80 μ L solution used on 1.5" ×1.5" CdTe surface has equivalent Cu atom concentration about 4.6 x 10¹⁷ cm⁻³ which has approximate thickness of 0.19 angstrom. After the Cu activation annealing treatment, a 40 nm Au layer was deposited on the back surface with an individual device area of 0.08 cm^2 . No further annealing treatment was taken after the Au deposition. Finally, a 120 nm magnesium fluoride (MgF₂) anti-reflective layer was deposited on the glass side of the FTO substrate in an ebeam evaporation system.

Hall effect measurements were performed for our as deposited, CdCl₂ treated and CuCl treated CdTe films (~3 μ m) deposited on soda lime glass using M91Fast Hall measurement system (LakeShore Cryotronics Advancing Science). All the as deposited, CdCl₂ treated and CuCl treated CdTe films show p-type conductivity with hole concentrations in the order of 10¹², 10¹², 10¹³ cm⁻³, respectively. Solar cell performance

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was characterized by measuring current density-voltage (J-V) curves under AM1.5G illumination using a solar simulator and a source meter (Keithley 2400) and the external quantum efficiency (EQE) spectra using an EQE system (PV Measurements Inc.). Dynamic secondary ion mass spectrometry (SIMS) was performed using Dynamic-SIMS5 from ION-TOF GmbH (Munster, Germany). The samples were analyzed in a dual beam profiling mode and the primary ion for analysis was 30 keV Bi^{3+} (Bi liquid metal ion source). This ion beam was applied over a 100 μ m ×100 μ m area at the center of the sputter crater (400 μ m × 400 μ m). The spectral data was acquired in a high massresolution mode. The energy of the sputtered ion was 1 keV Ar⁺ (Ar, electron impact ion source). Room temperature capacitance-voltage (C-V), temperature-dependent currentvoltage (J-V-T), thermal admittance spectroscopy (TAS), and impedance spectroscopy (IS) measurements were performed using a Solartron Modulab potentiostat equipped with a frequency response analyzer (Ametek Inc.). Photoluminescence (PL) characteristics were investigated utilizing steady-state and time-resolved PL. Steady-state PL measurement were performed by using 633 nm laser excitation at a power of ~ 5Wcm⁻² through the glass side. The PL signal were detected by a liquid nitrogen cooled symphony-II Si (CCD) detector after a Horiba iHR320 monochromator.

3.3 Results

After CdCl₂ treatment of CdS/CdTe solar cell devices at 390 °C for 30 min in dry air, 100 μ L CuCl solution was dripped on 1.5" × 1.5" CdTe sample followed with drying naturally and thermal activation of CuCl performed from 180 °C to 230 °C with 10 °C interval (Figure 3-1) without holding at peak temperatures called rapid thermal annealing (RTA). The devices annealed at 200 °C exhibit a maximum PCE with a higher V_{OC} and FF. At lower annealing temperature, e.g., 180 °C, the devices show significantly reduced average V_{OC} (828 mV vs 870 mV) and FF (68% vs 74%) due to the insufficient Cu diffusion, which resulted in lower hole density in CdTe and a higher back-barrier between CdTe and the back electrode. This can be confirmed from the significantly increased series resistance (R_S) and reduces shunt resistance (R_{SH}) at low annealing temperature. As the annealing temperature increases from 200 to 230 °C, again the device performance begins to degrade, especially V_{OC} and FF. This might be due to the over diffusion of Cu into the front interface between CdTe and CdS. A thermal activation of Cu through CuCl solution clearly shows V_{OC} and FF are directly affected by Cu diffusion on CdTe. At optimum conditions, the highest overall efficiency for the CdS-CdTe devices is 16.8%, with a V_{OC} of 0.870 V, a J_{SC} of 25.8mA/cm², and a FF of 75.0%, achieved at 200 °C annealing temperature and 100 µL CuCl solution. Further, to reduce the reflection loss a 125 nm magnesium fluoride (MgF_2) was deposited and obtained a PCE of 17.2%, with a V_{OC} 0.870 V, a J_{SC} 26.4 mA/cm² and a FF 75.1%, as shown in Figure 3- 3a.



Figure 3- 1 Statistical results of photovoltaic parameters of best 25 cells V_{OC} , FF, efficiency, J_{SC} , R_S and R_{SH} for CdS/CdTe solar cells with different CuCl annealing temperatures in RTA treatment.



Figure 3- 2 Statistical results of photovoltaic parameters of best 25 cells V_{OC}, J_{SC}, FF, and efficiency for ZMO/CdTe solar cells with different CuCl annealing temperatures and CuCl solutions volumes in RTA treatment. Reproduced with the permission from Elsevier Nao-Energy.

Further, CuCl volume and annealing temperature (RTA) are optimized for MZO/CdTe solar cells. Figure 3- 2 shows statistical results for MZO/CdTe solar cell performance with five different CuCl annealing temperatures (120 °C, 140 °C, 160 °C, 185 °C, and 210 °C) and CuCl solution. As shown in Figure 3- 2 V_{OC} increases gradually from around 0.750 to 0.870 V when the annealing temperature increases from 120 to 160 °C due to the adequate facilitated Cu diffusion by higher temperatures. However, when the annealing temperature is further increased to 210 °C, V_{OC} value decreases significantly to an average value of 0.825 V, which is due to the over diffusion of Cu. The highest FF of over 75% was observed when the annealing temperature is at 140 and 160 °C, indicating the performance of V_{OC} is dominated by the Cu concentration in CdTe bulk while the FF is dominated by the Cu concentration at CdTe back surface. Comparing with the pronounced variation in V_{OC} and FF, the maximum J_{SC} at different annealing temperatures varies insignificantly, with the peak J_{SC} value of 25.9 mA/cm² achieving at 160 °C. The changes in J_{SC} may be resulted from the proper concentration in CdTe bulk and at the back surface. The effect of CuCl solution volume on device performances also profound under different RTA temperature. At low RTA temperatures (120 °C, 140 °C, e.g.), more CuCl solution produces higher device performance, especially higher V_{OC}. At higher RTA temperatures (185 °C, 210 °C, e.g.), less CuCl solution is permitted for better device performances due to the high mobility of Cu at higher temperatures. The highest overall efficiency for the CuCl treated devices is 16.8%, with a V_{OC} of 0.860 V, a J_{SC} of 25.9mA/cm², and a FF of 75.4%, achieved at the conditions of 160 °C annealing temperature and 80 µL CuCl solution. After deposited a 125 nm magnesium fluoride (MgF₂) to reduce the reflectance and obtained a PCE of

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17.5%, with a V_{OC} 0.861 V, a J_{SC} 26.9 mA/cm² and a FF 75.4%, as shown in Figure 3- 3. With the MgF₂, the J_{SC} was improved by almost 1 mA/cm² with the highest quantum efficiency of around 90%.



Figure 3-3 (a, c) J-V curves and (b, d) EQE spectra of representative (a, b) CdS/CdTe and (c, d) ZMO/CdTe devices treated with different Cu precursors. Reproduced with the permission from ACS Publications.



Figure 3- 4 Statistical distribution of 25 best cells (a) V_{OC} , (b) J_{SC} , (c) FF, (d) R_S , (e) efficiency and (f) R_{SH} for CdS/CdTe solar cell devices with different Cu precursors. Reproduced with the permission from ACS Publications.



Figure 3- 5 Statistical distribution of 25 best cells (a) V_{OC} , (b) J_{SC} , (c) FF, (d) R_s, (e) efficiency and (f) R_{SH} for ZMO/CdTe solar cell devices with different Cu precursors. Reproduced with the permission from ACS Publications.

The representative device performance of CdTe solar cells with different Cu precursors (i.e., metallic Cu, CuCl, and CuCl₂, named CdTe-Cu, CdTe-CuCl, and CdTe-CuCl₂ hereafter, respectively) is shown in Figure 3- 3. A detailed statistical comparison of all the photovoltaic parameters for the CdS/CdTe and ZMO/CdTe devices are shown in Figure 3-4 and Figure 3-5 respectively. The best J-V parameters for each type of devices are tabulated in Table 3-1. For the devices with CdS as the front window layer (Figure 3-3 (a) and (b)), the best CdTe-Cu device shows a PCE of 15.20%, with a V_{OC} of 833 mV, a J_{SC} of 25.5 mA/cm², and a FF of 71.7%, while the CdTe-CuCl device demonstrates an overall improved performance with a Voc of 870 mV, a Jsc of 26.4 mA/cm², and a FF of 75.1%, yielding a PCE of 17.2%. The CdTe-CuCl₂ device exhibits a similar performance to the CdTe-CuCl device with a Voc of 854 mV, a Jsc of 26.3 mA/cm², and a FF of 74.3%, yielding a PCE of 16.7%. When comparing the EQE results, the CdS/CdTe-CuCl and CdS/CdTe-CuCl₂ devices show a significantly increased spectral response in the wavelength range from 350 to 550 nm with respect to the CdS/CdTe-Cu device (Figure 3- 3b) and deliver an integrated current density of 26.7 and 26.4 mA/cm², respectively, higher than that of the CdS/CdTe-Cu device (25.5 mA/cm²). The significant improvement of EQE in the whole wavelength range for the CuCl and CuCl₂ treated devices suggests better carrier separation and transport properties, especially at the front interface. This can be attributed to the reduced Cu diffusion to the front junction, which will be discussed later.

Samples	Voc	Jsc	FF	PCE	Rs	R _{SH}
	(V)	(mA/cm ²)	(%)	(%)	(Ω cm ²)	(Ω cm ²)
CdS-CdTe-Cu	0.833	25.5	71.7	15.2	3.8	1140
CdS-CdTe-CuCl	0.870	26.4	75.1	17.2	1.7	1421
CdS-CdTe-CuCl ₂	0.854	26.3	74.3	16.7	2.1	1209
ZMO-CdTe-Cu	0.837	25.9	61.8	13.4	9.8	1297
ZMO-CdTe-CuCl	0.862	26.9	75.5	17.5	1.7	1455
ZMO-CdTe-CuCl ₂	0.851	26.6	73.3	16.7	2.6	1548

Table 3- 1 Photovoltaic parameters for the best CdS/CdTe and ZMO/CdTe solar cell devices with different Cu precursors. Reproduced with the permission from ACS Publications.

The performance of ZMO/CdTe solar cells with CuCl and CuCl₂ (Figure 3- 3c) is also significantly improved compared with that of the metallic Cu-treated device (Figure 3- 3c). The devices treated with solution processed CuCl and CuCl₂ show higher quantum efficiencies of ~ 90% from 500 to 600 nm, yielding an integrated current of 26.2 and 25.9 mA/cm², respectively, which are higher than the J_{SC} of 25.5 mA/cm² in the ZMO/CdTe-Cu device (Figure 3- 3d). The statistical comparison in Figure 3- 4 and Figure 3- 5 also show the same improvements for the devices with the CdS and ZMO front window layers, especially the V_{OC} and FF, suggesting a better front main junction and a reduced back barrier height. Interestingly, the J_{SC} values in the CdS/CdTe devices are higher than those in the ZMO/CdTe devices although ZMO has larger bandgap than CdS. One reason is that the CdS film in this work is thinner (60 nm) than the ZMO film (80 nm), resulting in higher transmittance at the range of 300~380 nm. The other reason is the interdiffusion between CdS and CdTe at the front interface, resulting in the formation of CdS_xTe_{1-x} alloy, which has slightly smaller bandgap [76, 77]. Thereby, the light absorption of the CdS/CdTe device extended to longer wavelength at the range of 840~880 nm as shown in the EQE curves, Figure 3- 6.



Figure 3- 6 EQE compression between device having CdS and ZMO window layer. Reproduced with the permission from ACS Publications.



Figure 3- 7 Secondary ion mass spectroscopy depth profiles of the CdTe-Cu and CdTe-CuCl devices with ZMO as front buffer layer. Reproduced with the permission from ACS Publications.

Note that the J-V curves of the ZMO/CdTe device with Cu metal (Figure 3- 3c) shows clear distortion under a forward bias near V_{OC} (i.e., an S-kink), indicating poor heterojunction properties at the ZMO/CdTe interface. According to our SCAPS simulation results, [21] the S-kink can be attributed to the low ZMO film conductivity and the high acceptor-like defect trap concentration at the front interface, both of which are caused by the over diffusion of Cu. The diffusion of Cu into the ZMO film and the ZMO/CdTe interface can significantly decrease the ZMO conductivity [78-80] and form recombination centers at the front interface [48, 67]. The aggregation of Cu at the front interface and in the ZMO layer are identified by the dynamic-SIMS measurements (Figure 3-7). Note that in the CdTe-CuCl devices, the Cu activation can be performed by a RTA process at 160 °C with ~150 times less Cu dosage than the treatment using metallic Cu, as in our previous report [48]. The RTA process has also been tried for the devices with metallic Cu doping. However, the traditional Cu activation process (200 °C for 20 min) always shows higher device performance than that treated with the RTA process when metallic Cu is used as the Cu source. In comparison, the CdS/CdTe devices treated with metallic Cu show no S-kink. This is probably because CdS is not as sensitive to Cu as ZMO.

To further investigate the effect of different Cu precursors on the optoelectronic properties of CdTe films, a suite of characterizations was performed. Note that the CdTe-CuCl devices show similar performances with the CdTe-CuCl₂ devices, implying the nonessential effect of the oxidation state of Cu. Also, the devices treated with metallic Cu show much lower device performance than those with the solution processed CuCl and CuCl₂ treatments, suggesting more significant effect of the ionic versus metallic Cu

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sources. In addition, changing the front window layer, e.g., CdS and ZMO, does not affect the influence of different Cu precursors. Therefore, CdS/CdTe-CuCl was chosen as the representative of ionic Cu treatment to make comparison with the devices with metallic Cu in the characterization hereafter.



Figure 3- 8 (a) PL and (b) TRPL spectra for CdTe-Cu and CdTe-CuCl devices with CdS as the front window layer. For each sample, PL spectra were excited through the FTO glass side and CdTe film side with a 633 nm laser excitation. Reproduced with the permission from ACS Publications.



Figure 3- 9 Steady-state and time-resolved PL spectra of ZMO/CdTe devices with (a) Cu metal and (b) CuCl solution treatment. For each sample, PL spectra were excited through the FTO glass side and CdTe film side with 633 nm laser excitation. Reproduced with the permission from ACS Publications.

Figure 3-8 (a) shows the PL measurements of CdTe-Cu and CdTe-CuCl devices with CdS as the front window layer. Both samples show PL spectra with an emission

peak centered at 1.501 ± 0.003 eV when excited through the FTO glass side and at 1.537 ± 0.002 eV when excited from the film side but with different emission intensities. The variation of the emission peak is due to the interdiffusion of CdS and CdTe at the front interface [81]. Higher PL intensity generally suggests a lower nonradiative recombination rate and a higher carrier lifetime. For both glass and film side excitations, the CdTe-CuCl device shows higher PL intensities than the CdTe-Cu device, indicating lower recombination rates at the CdS/CdTe and CdTe/Au interfaces in the CdTe-CuCl device [21]. The TRPL results in Figure 3- 8 (b) further confirm this conclusion by showing a much higher carrier lifetime of 9.7 ns in the CdTe-CuCl device than that of 7.4 ns in the CdTe-Cu device when excited from the glass side. When excited from the film side, the same lifetime is obtained due to the severe recombination at the back surfaces and the equipment detection limit. The same PL and TRPL measurements were also carried out for ZMO/CdTe devices and similar trends observed with higher PL intensity and lifetime in the CuCl treated ZMO/CdTe films, as shown in Figure 3- 9 (a-b).



Figure 3- 10 (a) Mott-Schottky plots measured at room temperature for devices with Cu and CuCl treatment. Inset: Mott-Schottky plots measured from -3.0 to 1.0 V bias voltage. (b) The calculated carrier densities extracted from C-V measurements. Reproduced with the permission from ACS Publications. Reproduced with the permission from ACS Publications.
C-V measurement was used to investigate the apparent built-in potential (V_{bi}) at the front junction and extract the doping density in the CdTe absorber layer (Figure 3-10a). From the intercept of the linear fit of the Mott-Schottky plot ($1/C^2$ vs bias) with the bias axis, the V_{bi} across the depletion region formed by the CdS/CdTe junction was extracted. The CdTe-CuCl device shows a higher V_{bi} (0.58 V) than the CdTe-Cu device (0.42 V) (Figure 3- 10a). The improvement of V_{bi} suggests an improved front junction at the CdS and CdTe interface of the CdTe-CuCl device, which plays the most important role on V_{OC} and final device performance. The improvement of V_{bi} in the CdTe-CuCl device can be attributed to the improvement of hole density in the bulk CdTe absorber, the reduction of the interface trap state concentration and higher n-type conductivity of CdS film due to well-controlled Cu diffusion into the front interface and CdS film [82]. The apparent hole density N_A in the CdTe layer is calculated using the Mott Schottky plot according to the following equation:[68]

$$N_{A} = -\frac{2}{q\epsilon\epsilon_{0}A^{2}} \left[\frac{dC^{-2}(V)}{dV}\right]^{-1}$$

where ε is the relative dielectric constant of CdTe, ε_0 is the absolute permittivity of vacuum, A is the surface area of a cell, C is the junction capacitance, and V is the bias voltage. As shown in Figure 3- 10(b), the hole carrier concentration taken from the lowest point of its depth profile of CdTe-CuCl device is 5.33×10^{14} cm⁻³, which is higher than the carrier concentration in the CdTe-Cu device (8.63×10^{13} cm⁻³). C-V measurements for the ZMO-CdTe devices with varied Cu precursors were also performed and similar changes of the carrier concentration can be observed. The improvement of hole density in CdTe bulk is beneficial to the improvement of V_{bi} as discussed above and the reduction of the back-barrier height, which will be discussed later.



Figure 3- 11 Frequency vs. Capacitance spectra for (a) CdTe-Cu and (b) CdTe-CuCl devices, (c) and (d) differential capacitance spectra $(-\omega dC/d\omega)$ extracted from the capacitance spectra (a) and (b) respectively, (e) Arrhenius plots and (f) defects distribution in CdTe-Cu and CdTe-CuCl devices obtained from (c) and (d). The trap defect activation energies (E_A), defect capture cross-section (σ_t) and trap state densities (N_t) are tabulated in the inset. Reproduced with the permission from ACS Publications.



Figure 3- 12 Arrhenius plots that were used to calculate back-barrier height based on dark J-V-T measurement. Reproduced with the permission from ACS Publications.

Thermal admittance spectroscopy is an effective method to study the defect properties in CdTe solar cells [68, 83]. The capacitance spectra (C- ω) measured at various temperatures (T) for CdTe-Cu and CdTe-CuCl devices are shown in Figure 3- 10 (a) and (b). From the peaks of derivative of capacitance spectra (- ω dC/d ω), Figure 3-11(c) and (d), the defect characteristic frequencies as indicated by arrows were extracted and used to build the Arrhenius plots (Figure 3- 11e). From the linear fit of the Arrhenius plots, the trap defect states in the CdTe-Cu and CdTe-CuCl devices were calculated. Here, three characteristics activation energies, E_{A1} = 0.398 ± 0.006 eV, E_{A2} = 0.358 ± 0.011 eV, and E_{A3} = 0.354 ± 0.031 eV for CdTe-Cu devices and two activation energies, E_{A1} = 0.323 ± 0.016 eV, and E_{A3} = 0.306 ± 0.005 eV for CdTe-CuCl devices were detected. According to our previous investigation about the TAS measurements performed at various DC biases with constant AC modulation, [68] E_{A1} corresponds to the back contact barrier, while E_{A2} and E_{A3} are considered as deep acceptor-like trap states [42, 84, 85]. For the CdTe-Cu device, a back-barrier height of 0.398 ± 0.006 eV is obtained, which is higher than 0.323 ± 0.016 eV obtained in the CdTe-CuCl devices. This can be further demonstrated by the J-V-T measurements as shown in Figure 3-12. The reduction of back-barrier height is attributed to the improvement of hole density adjacent to the electrode as shown in the C-V measurement. Besides the improvement of backbarrier height, the CdTe-CuCl devices show much shallower defect levels than that in the CdTe-Cu devices. In the CdTe-Cu device, two defects with depth of $E_{A2} = 0.358 \pm 0.011$ eV, and $E_{A3} = 0.354 \pm 0.031$ eV are detected. While in the CdTe-CuCl devices, E_{A2} disappeared according to the change of the features in the differential capacitance spectra (Figure 3- 11c and d), and only one defect $E_{A3} = 0.306 \pm 0.005$ eV is obtained, which is shallower than the defects in the CdTe-Cu devices. The density (Nt) and capture crosssection (σ_t) of all the defects are also calculated as shown in Figure 3- 11(f) and the inset. The defect E_{A3} in the CdTe-CuCl device have much lower N_t (2.69×10¹⁴ cm⁻³) than that in the CdTe-Cu device $(6.45 \times 10^{14} \text{ cm}^{-3}, 8.78 \times 10^{14} \text{ cm}^{-3} \text{ for } \text{E}_{\text{A2}} \text{ and } \text{E}_{\text{A3}}, \text{ respectively})$. In addition, the defects with depth of EA2, which exists in CdTe-Cu but misses in the CdTe-CuCl device shows a much higher σ_t value of 4.83×10⁻¹⁶ cm⁻³, than the other two defects of 2.33×10⁻¹⁷ cm⁻³ and 8.34×10⁻¹⁷ cm⁻³, for CdTe-Cu and CdTe-CuCl devices, respectively. The eliminating of defects with high concentration and capture cross-section in the CdTe-CuCl device can reduce the nonradiative recombination loss and improve device performance.



Figure 3- 13 The degradation tests in ambient for 60 days for devices with different window layers and Cu precursors. Each group include 6 cells. The degradation of the (a) efficiency, (b) V_{OC}, and (c) FF were plotted individually. (d) Low-temperature steady-state PL measurement of CdTe-Cu and CdTe-CuCl devices excited from the back side at 9 K performed by a 532 nm laser at 25 mW/cm². Reproduced with the permission from ACS Publications.

It is well known that Cu ions in CdTe have a high migration rate, which is the culprit of the long-term stability issue for CdTe modules. It is worth mentioning that the CuCl treatment was performed using a RTA process owing to the ionic state of CuCl, which generated a desired Cu distribution profile, i.e., a high N_{Cu} at the back surface and a low N_{Cu} at the front interface [48]. At first glance, this kind of Cu distribution profile can be double edged, i.e., higher initial performance but lower long-term stability due to the gradient N_{Cu} profile that can promote the diffusion of Cu from the region with high

 N_{Cu} to the region with low N_{Cu} . To study the degradation induced by the different Cu distributions, a stability test (6 cells for each group) was carried out in ambient air for 60 days (Figure 3- 13). For the CdTe-Cu devices, the average V_{OC} decreases by 6-7%, and the average FF decreases by 5%, yielding an average PCE relative degradation by ~ 14% within 60 days. Whereas, the CdTe-CuCl devices show negligible degradation by ~ 1-2%. To confirm this result, the same degradation test was also performed for another CuCl-treated device with ZMO as the front window layer instead of CdS, which shows similar stability with the CdTe-CuCl devices with CdS as the front window layer. These results further indicate that the gradient of N_{Cu} does not lead to poor stability in the CdTe-CuCl devices, which results in a relatively low Cu_i concentration. Cu_i has been corelated to the fast Cu redistribution in the CdTe film and at the heterojunction, while the desired Cu_{Cd} and complexes have a relatively low diffusion rate.[86, 87]

This prediction can be further demonstrated by the PL measurement at a low temperature (Figure 3- 13 d) and the SIMS measurements (Figure 3- 7). The lowtemperature PL spectra of the CdTe-Cu and CdTe-CuCl devices show similar peaks, such as a free excitonic peak at 1.59 eV,[88] a donor-acceptor pair (DAP) peak at 1.55 eV (recombination of some donor state to V_{Cd} acceptor) and its phonon replicas, [89] and a 1.45 eV DAP peak (a DAP peak due to the recombination of Cl donor to Cu_{Cd} acceptor) and its phonon replicas at ~20 meV [90, 91]. The higher PL intensity at ~1.45 eV in the CdTe-CuCl device is the consequence of the presence of higher number of Cu_{Cd} acceptors at the back surface than that in the device treated with the thermally evaporated

Cu. It is worth mentioning that the SIMS results suggest a lower N_{Cu} at the back surface in the CdTe-CuCl device. The low N_{Cu} and high Cu_{Cd} acceptor concentration in the CdTe-CuCl device conjointly suggest a higher formation rate of desired Cu_{Cd} substitution and a lower formation rate of compensative interstitial (Cu_i), thereby enabling better long-term stability.

3.4 Discussions

According to the device performance and characterization of the devices with different Cu precursors, the following discussions are made to understand the importance of Cu precursor in fabricating efficient CdTe solar cells.

1) Cu diffusion. CdTe solar cells shows similar performances when CuCl and CuCl₂ are used as the Cu precursors, with either CdS or ZMO as the front window layers. This result implies that the oxidation state of Cu in CuCl and CuCl₂ shows a negligible effect on the Cu incorporation. In comparison, the device with metallic Cu shows much worse device performances. These results suggest that Cu diffusion from CuCl and CuCl₂ into the CdTe absorber have a similar diffusion behavior and defect properties in CdTe solar cells. This is because both the CuCl and CuCl₂ are ionic compounds and Cu ions exist naturally in these two materials, thus, no extra energy for Cu ionization is required for the Cu diffusion into CdTe. After the diffusion into the CdTe absorber, First-principles-based analysis indicates that Cu-related defects Cu_i^+ and Cu_{Cd}^- , both of which take Cu⁺ oxidation state, have relatively low formation energies [64, 87]. We assume Cu²⁺ would change to Cu⁺ and show the same diffusion rate. When metallic Cu is used as the Cu precursor, an oxidation process is needed, thus, extra energy is required to form

Cu ions that can subsequently diffuse into CdTe. We suspect that this is the reason why the CuCl treatment need lower annealing temperatures or shorter annealing duration than the metallic Cu treatment.

2) Cu dosage and distribution. The Cu ion concentrations in both CuCl and CuCl₂ solutions are identical (3.10 µg/ml). Due to the difference of the CdTe layer thickness (3.5 and 4 µm for the CdS/CdTe and ZMO/CdTe, respectively), 100 µL chloride solution is applied to $1.5'' \times 1.5''$ CdS/CdTe devices and 80 µL chloride solution is applied to $1.5'' \times 1.5''$ CdS/CdTe devices and 80 µL chloride solution is applied to $1.5'' \times 1.5''$ CdS/CdTe devices, which are equivalent to ~0.24 and 0.19 Å Cu layer, respectively. While, in the CdTe-Cu devices, the optimal Cu metal thicknesses applied in ZMO/CdTe and CdS/CdTe devices are 3 and 4 nm, respectively, which are much thicker than the equivalent Cu thickness in the CdTe-CuCl and CdTe-CuCl₂ devices. Nonetheless, the devices with the chloride treatment show a much higher carrier density than that with the metallic Cu treatment, suggesting that the Cu source in the chloride condition has a lower Cu dosage but a higher activation ratio (defined as the hole density relative to the incorporated dopant density) than metallic Cu.

3) Defect properties and long-term stability. Benefiting from the low Cu dosage, the devices treated with CuCl and CuCl₂ possess a higher carrier density, suppressed bulk defects with shallower levels and lower trap state capture cross section and smaller back barrier height and improved stability, simultaneously. This is because the device with a lower Cu dosage through the chloride treatment has more desired Cu_{Cd} acceptors while the device with higher Cu dosage through metallic Cu treatment has more detrimental Cu_i donors. When the Cu dosage increases, more Cu_{Cd} will be ionized, leading to the downshift of Fermi level towards the valence band maximum. In such a case, the

formation energy of the charged donor defect Cu_i^+ (a compensating donor) decreases linearly as a function of Fermi energy, [92] therefore, resulting in more shallow compensating Cu_i^+ donor and lower hole concentration. Due to the formation of compensating Cu_i^+ donor, the CdTe devices with thermal evaporated Cu treatment show a larger back-barrier and a more pronounced nonradiative recombination rate at the back interface. Thereby, the device performance, specifically V_{OC} and FF, are significantly limited. In addition, the formation of Cu_i^+ also introduces fast Cu ion migration throughout the CdTe film, which is the culprit of the long-term stability issue for CdTe production facilities.

4) Effect on the devices with different front window layer. Besides the effect at the absorber bulk and device back interface, the diffusion of copper into the front interface has been widely reported in CdTe devices, which can induce deep donor defect complexes at the front interface[84] and decrease the n-type conductivity of the front window layer [59, 67, 82, 84]. This effect became more notorious in CdTe solar cells with ZMO as front window layer due to its sensitivity to Cu (with several orders of magnitude reduction of window layer conductivity) [78-80]. In the devices with CdS as n-type window layer, the effect of Cu at CdS/CdTe interface is weaker than that in the ZMO/CdTe devices. The solution processed chlorine treatment successfully reduces the Cu penetration into the front interface and constructs the desired Cu distribution throughout the device, thus, the diode quality of the front main junction is improved.

3.5 Conclusions

A comparison among different Cu precursors (i.e., metallic Cu, CuCl, and CuCl₂ solutions) as the doping source is performed on CdTe solar cells. The similar performance of the devices with CuCl and CuCl₂ suggests that the oxidation states of Cu⁺ and Cu²⁺ show a negligible difference on device performance. Both of them show a significant improvement in device performance compared to the devices treated with the metallic Cu. The comparison of Cu activation temperature/time, dosage and device performance and characterization results concomitantly suggest that the solutionprocessed Cu treatment using a Cu ionic compound enables lower dopant diffusion and activation temperature/duration, less Cu dosage, more efficient Cu incorporation, and a desired gradient Cu profile in the CdTe film, resulting in improved electrical properties at both the front and back interfaces and the bulk of the absorber, leading to higher device performances than the conventical devices treated with metallic Cu doping. Finally, decent PCEs of 17.2% and 17.5% are obtained for the devices with CdS and ZMO as the front window layers, respectively, which are among the most efficient CdTe solar cells without Se incorporation.

Chapter 4

The Effect of CuSeO3 Hole Transfer layer on CdTe Solar Cells Performance

Solution-processed Cu doping with Cu contained hole transport layer (HTL) in CdTe solar cells has attracted great attention due to its low cost, ease of process, low-temperature activation, and facile Cu control advantages. Here, we introduced solution-processed copper selenate (CuSeO₃) as a Cu source and hole transport layer. Steady-state photoluminescence (PL) quenching effect and back-barrier height reduction together indicate efficient hole extraction from the bulk and suppressed carrier recombination at the back surface. As a result, a cell efficiency of 16.7% was demonstrated with a V_{OC} of 0.861 V and a fill factor of 76.65% for CdS/CdTe configuration and a power conversion efficiency of 18.5% after incorporating CdSe at the front interface to create CdSe_xTe_{1-x} gradient absorber at the interface.

This work is presented in IEEE photovoltaic special conference-PVSC49 with tittle "Solution-Processed Copper Selenium Oxide (CuSeO3) as Hole Trasport Layer for CdS/CdTe Solar Cells" by Sandip S Bista, Deng-Bing Li, Suman Rijal, Sabin Neupane, Manoj K Jamarkattel, Rasha A Awni, Zhaoning Song, Adam Phillips, Michael Heben, Randy J. Ellingson, and Yanfa Yan.

4.1 Introduction

CdTe is a leading thin-film technology, which produced a record power conversion efficiency (PCE) of 22.10 % for small cells and around 19 % for module productions [93]. These remarkable PCEs were achieved by introducing effective passivation and doping in the CdTe absorber layer. Traditionally, cadmium chloride (CdCl₂) is used for grain boundary passivation, and Cu is used for p-type doping in CdTe. It is also observed that Cu forms better Ohmic contact, although fast diffusion of Cu causes stability risk [49]. The low solubility and fast diffusivity of Cu in CdTe indicate that an optimum Cu incorporation is required to reduce the formation of undesired Curelated trap states and improve device stability [46, 47].

Recently, solution-processed Cu doping and Cu contained hole transfer layer (HTL) have attracted attention due to their low cost, easy process, low-temperature activation, and better Cu control characteristics. Our previous work suggests that ionic Cu (using CuCl and CuCl₂ solution) can give better Cu control by reducing the Cu dosage and forming gradient Cu distribution [15, 48]. Nonetheless, a suitable hole transport material with positive conduction band offset (CBO) and high work function is still required to further reduce the carrier recombination at the back surface. Therefore, it is believed that inserting a back buffer layer between CdTe and metal electrodes is expected to enhance carrier collection and the device performance.

CuSeO₃ has a large bandgap of 3.9 eV [94]. It can act as an alternative Cu source for p-type doping of CdTe with controllable Cu dosage and a hole transport material in CdTe solar cells. Here, we report the fabrication of efficient CdTe thin-film solar cells

using solution-processed CuSeO₃ as a hole transport material and a Cu source for p-type doping. Steady-state photoluminescence (PL) and temperature-dependent J-V measurements indicate an improved carrier collection efficiency between CdTe and CuSeO₃ and a reduced back-barrier height compared to Cu-metal treated devices.

4.2 Experimental Detail

All devices were fabricated on commercially available NSG TEC 12D soda-lime glass coated with fluorine-doped tin oxide (FTO) and 30 nm intrinsic SnO₂ provided by Pilkington, North America. First, the oxygenated cadmium sulfide (CdS:O) window layer was RF sputtered at room temperature under 10 mT pressure with a gas flow of 2% oxygen and 98% argon. A 4 µm cadmium telluride (CdTe) absorber layer was then deposited at 10 Torr using the closed space sublimation (CSS) method at a source temperature of 660 °C and a substrate temperature of 590 °C. CdCl₂ treatment was carried out at 390 °C for 30 minutes in dry air ambient. After cooling down, the sample was removed from the chamber and rinsed with methanol to remove chlorine and oxide residues. Subsequently, the CuSeO₃ was spin-coated on CdTe film using the solution method by dissolving $CuSeO_3$ •2 H_2O powder in ammonium hydroxide (28-30 wt.%) with a 2 mg/ml concentration. At optimum condition, 100 μ L solution was pipetted and spun at 6000 rpm for the 30 s on a $1.5^{"}\times 1.5^{"}$ sample surface. After spin coating, samples were post-annealed at different temperatures. Finally, devices were completed by thermally evaporating a 40 nm gold (Au) back metal electrode. Under a similar condition, the control devices were fabricated with a thermally evaporated 4 nm Cu and 40 nm Au bilayer followed with annealing at 200 °C for 20 minutes.

Further, CdSe/CdTe solar cells were fabricated on TEC 12D NSG-glass. The CdSe films with different thicknesses (0, 70, 130, 200, and 400 nm) were thermally evaporated at a source temperature of 680 °C under 1×10^{-7} Torr, while the substrate was kept at room temperature. CdTe film was deposited by closed space sublimation process at 660 °C source and 590 °C substrate temperatures under 10 Torr pressure. Afterward, the CdCl₂ residual was rinsed off with methanol. Then, CuSeO₃ back buffer layer was used for Cu doping as described above. Finally, the device was completed by thermally evaporating 40 nm gold via a shadow mask with a 0.08 cm² cell area.

AM1.5 illumination J-V and 0 V bias external quantum efficiency (EQE) measurements were conducted to evaluate the device performance. Steady-state photoluminescence (PL) measurement using a 532 nm laser excitation from the film side and temperature-dependent current-voltage (J-V-T) measurement (performed in a closed-cycle helium cryostat, where the temperature varied from 190 to 310 K, with a step size of 10 K) were conducted to understand the effect of CuSeO₃ back buffer layer in comparison with metallic Cu doped devices.

4.3 Results and Discussions



Figure 4-1 UV-Vis spectrum and Tauc plot of a CuSeO₃ thin film.

Figure 4- 1 shows the transmittance spectrum of CuSeO₃ thin film deposited on soda-lime glass using UV-Vis spectroscopy. From the Tauc plot, an energy band gap E_g = 3.75 eV is obtained, consistent with the literature report [94].



Figure 4- 2 Box plots of 25 best cells (a) V_{OC} (b) J_{SC} (c) efficiency (d) fill factor (FF), (e) series resistance (R_S), (f) shunt resistance (R_{SH}) of CdTe solar cells with Cu metal and CuSeO₃ back contact annealed at different temperatures.

We firstly optimized the thermal activation temperature of CuSeO₃ in CdTe solar cells. According to our previous experience on CdTe solar cells with CuSCN [8] as back contact, rapid thermal annealing process was used to activate CuSeO₃. We annealed CuSeO₃ coated CdTe solar cells in a CSS chamber at three different temperatures: 190, 210, and 230 °C without holding time. Figure 4- 2 shows the statistical distribution of

photovoltaic parameters under different annealing conditions and the comparison with standard Cu metal treated cells. CuSeO₃ processed cells annealed at 210 °C give the highest V_{OC} and FF. The high V_{OC}s might be due to a better doping profile. The enhancement in FF is due to the reduced series resistance (R_s) and increased shunt resistance (R_{SH}). The poor photovoltaic parameters for cells annealed at the lower temperature (190 °C) could be due to the insufficient Cu diffusion, while for the cells annealed at a higher temperature (230 °C), the lower device performance might be due to excessive diffusion of Cu to the front interface.

Figure 4- 3 (a-b) shows the J-V curves and EQE spectra of the champion cells. To understand the effect of CuSeO₃ thickness, we conducted a few experiments with a thicker CuSeO₃ back-buffer layer, as shown in Figure 4- 4. The thickness was controlled by increasing the concentration of CuSeO₃.2H₂O powder in NH₄OH solvent and reducing the spin-coating speed. We observed that thick CuSeO₃ was highly resistive, resulting in poorer device performance.

Table 4- 1 summarizes the photovoltaic parameters of the champion cells at different annealing temperatures. EQE spectra responsibility clearly shows the effect of annealing temperatures. The device annealed at 210 °C has a better spectral response at the longer wavelength regions (600 – 840 nm), suggesting reduced back-barrier height. All CdTe-CuSeO₃ devices show higher spectral response at short wavelength regions between 350 to 600 nm than Cu metal-doped devices, suggesting CuSeO₃ offers better control on Cu diffusion, leading to an improved front junction quality.



Figure 4- 3 (a) Current density-voltage (J-V) and (b) external quantum efficiency (EQE) spectra for the champion devices annealed at different temperatures for CdTe-CuSeO₃ and the reference cell.



Figure 4-4 (a) SEM image of a complete device (b) thick CuSeO₃ layer.

To understand the effect of CuSeO₃ thickness, we conducted a few experiments with a thicker CuSeO₃ back-buffer layer, as shown in Figure 4- 4. The thickness was controlled by increasing the concentration of CuSeO₃.2H₂O powder in NH₄OH solvent and reducing the spin-coating speed. We observed that thick CuSeO₃ was highly resistive, resulting in poorer device performance.

Process	Voc (mV)	Jsc (mA/cm ²)	FF (%)	PCE (%)	
Cu	841	24.6	68.47	14.17	
CuSeO ₃ -190 °C	840	24.85	68.84	14.37	
CuSeO ₃ -210 °C	861	25.27 76.65		16.7	
CuSeO ₃ -230 °C	851	25.01	74	15.75	

Table 4-1 Photovoltaic parameters of champion cells at different annealing temperatures.

Steady-state PL and temperature-dependent dark J-V measurements were carried out to understand the effects of CuSeO₃ on the device performance. As shown in Figure 4- 5(a), the CdTe-CuSeO₃ sample has a significantly lower PL intensity than the CdTe-Cu sample when the laser is illuminated from the film side, indicating a significant quenching effect. The PL quenching in CdTe-CuSeO₃ suggests that CdSeO₃ acts as an effective hole transfer layer with reduced back barrier height and extracts holes from CdTe into the CuSeO₃. Temperature-depended dark J-V measurements were used to quantify the back-barrier height. The device with metallic Cu shows a severer rollover at lower temperatures than the CuSeO₃/Au device, as shown in Figure 4- 5 (b-c). The presence of roll-over is directly related to the back-barrier height. Figure 4- 5 (d) shows the Arrhenius plots used to calculate the back-barrier heights. The calculated back-barrier heights for the devices with metallic Cu and CuSeO₃ are 0.325 eV and 0.266 eV, respectively. The reduced back barrier height is consistent with the improvement of device performance.



Figure 4- 5 (a) steady-state photoluminescence (PL) curves, (b-c) temperature-dependent dark J-V curves for devices containing CuSeO₃ and Cu metal back contact, respectively. (d) Arrhenius plots to calculate the of back-barrier heights for CuSeO₃ and Cu processed cells.

It is noted that the devices discussed above is based on CdS/CdTe stacks, and the efficiency of the device can be further improved by modifying the front interface. Here, we incorporate a low bandgap CdSe_xTe_{1-x} alloy in between CdTe and the commercially available TCO with SnO₂ buffer layer (T12D). Incorporating the right amount of Se and proper chlorination and copper activation play a vital role in increasing the device performance. In this work, the CdSe was deposited by thermally evaporated CdSe followed with CdTe sublimation. An efficient gradient CdSe_xTe_{1-x} absorber layer was created at the front interface through optimum wet CdCl₂ treatment.



Figure 4- 6 (a) J-V and (b) EQE measurements of CdSe/CdTe solar cells, with different CdSe thicknesses.

Table 4- 2 The champion and average cell photovoltaic performances with different CdSe thicknesses for 25 best dot cells.

CdSe (nm)		V _{OC} (mV)	J _{SC} (mA/cm ²)	FF (%)	PCE (%)
0	Best	0.763	25.29	62.14	11.99
	Average	724	24.78	60.02	11.17
70	Best	0.845	25.69	72.58	15.76
	Average	0.833	25.69	72.35	15.48
130	Best	0.84	28.77	76.82	18.56
	Average	0.838	28.52	76.48	18.29
200	Best	0.826	28.88	74.08	17.67
	Average	0.816	28.25	72.76	16.78
400	Best	0.836	20.59	72.09	12.41
	Average	0.828	19.78	71.17	11.65



Figure 4- 7 Statistical results of J-V performance parameters of best 25 CdSe/CdTe solar cells using different CdSe thicknesses.

Figures 4- 6 (a-b) show the J-V curves and EQE spectra corresponding to the varied CdSe thickness. Table 4- 2 summarizes the measured photovoltaic parameters of the best cells and an average of 25 cells for each device. It is observed that V_{OC} , J_{SC} , FF, and device efficiency directly depend on the Se in CdSe_xTe_{1-x} alloy, consistent with the literature report [39, 40]. The device with 130 nm CdSe gives optimum device performance with a V_{OC} of 840 mV, a J_{SC} of 28.77 mA/cm², a FF of 76.48%, and a power conversion efficiency of 18.56%. This improvement is solely due to the enhanced current collection in the longer wavelength region, which results from the formation of a low band gap CdSe_xTe_{1-x} alloy at the interface. The EQE curves clearly show the origin of J_{SC} loss. An increase in CdSe thickness increases the concentration of Se on CdSe_xTe_{1-x}

alloy, decreasing the ternary alloy's band gap and increasing J_{SC} up to 29 mA/cm². However, a 400 nm CdSe will generate a gradient bandgap out of optimum and inversely limit J_{SC} . Figure 4- 7 shows the statistical results of device parameters extracted from the J-V curves as a function of CdSe thickness.

4.4 Conclusion

A solution proceeds Cu doping, and Cu contained hole transfer layer (HTL) CuSeO₃ has been successfully adopted as a hole transport material in CdTe solar cells. Using a solution method, we achieved 16.70 % power conversion efficiency with an open-circuit voltage of 861 mV, a short circuit current of 25.27 mA/cm^{2,} and a fill factor of 76.65 % for the CdS/CdTe solar cell. T-J-V measurement shows that CuSeO₃ exhibits better Ohmic contact than copper metal doping, and steady-state PL confirms that CuSeO₃ is a hole transfer layer. Further, by modifying the front interface by incorporating a low band gap CdSe_xTe_{1-x} absorber layer, with the CuSeO₃ back buffer layer, we achieved a 18.56% power conversion efficiency.

Chapter 5

Lightweight and Flexible CdTe Solar Cells

Lightweight and flexible solar cells have significant advantages in their high specific power (kW/kg) and high feasibility during installation and transportation. Rigid CdTe solar cells have already achieved 22.1 % power conversion efficiency, using less material, due to which this technology is one of the cheapest among its competitors. However, about 5-10 µm rigid CdTe solar cells are grown on 3 mm thick glass, which substantially increases its production cost and reduced specific power. Here we fabricated the lightweight and flexible CdTe-based solar cell using a lift-off process and attached it to the substrate of interest. We achieved 12.6 % PCE in CdS/CdTe configuration and 13.35 % for CdS/CdSe/CdTe with a superior specific power. This chapter will explain three different lift-off techniques and the fabrication of lightweight and flexible CdTe solar cells.

5.1 Lightweight and Flexible CdTe Solar Cells via Water-Assisted Lift-Off Process

In this work, CdS/CdTe/Cu/Au film stacks grown on mica sheets were delaminated through a water-assisted lift-off process and transformed onto substrates of interest (aluminum foil, polymer) to fabricate flexible photovoltaics. Due to the high sensitivity of mica to solvent, a close-spaced sublimation cadmium chloride (CdCl₂) treatment was adopted for the CdTe film instead of a CdCl₂ methanol solution. Our results demonstrated that additional CdCl₂ treatment for the CdS film is critical to reducing the parasitic optical loss induced by CdS film and improving the crystallinity for both the CdS and CdTe films, resulting in a high-quality front junction and CdTe absorber with a significantly reduced non-radiative recombination. Finally, lightweight and flexible polycrystalline CdTe solar cells with a champion power conversion efficiency of 12.6 % were demonstrated.

5.1.1 Introduction

CdTe-based rigid solar cell technology is the most dominant thin-film technology, which has already achieved 22 % cell and 19 % module power conversion efficiencies (PCEs) [93]. Generally, the efficient CdTe solar cell is fabricated in superstrate configuration on a rigid glass substrate, where the actual functional layer is less than 10 μm, 300 times thinner than the rigid glass (~3mm). This dramatically increases the lightweight value and limits its potential application in space and other portable devices. Therefore, reducing the glass thickness or using flexible substrates makes devices costefficient with wide scenario applications. However, due to the necessity of high temperature to fabricate efficient CdTe solar cells, flexible CdTe solar cells are rarely investigated, and thereby their performance is far below their rigid counterparts [95, 96].

Delaminating devices from the rigid substrate has become a promising method to fabricate flexible CdTe solar cells, and various techniques have been developed, e.g., adding a scarification layer, [96-98] applying mechanical lift-off, [99, 100] thermomechanical stress, [101-103] or water-assisted lift-off [104-106]. Recently, Wen and coworkers reported the water-assisted lift-off technique to separate epitaxial CdTe film from a Muscovite mica (K₂O.Al₂O₃.SiO₂) substrate, demonstrating flexible CdTe solar cells with a power conversion efficiency (PCE) of 9.59 % with 687 mV open-circuit voltage (V_{OC}), [104] which is much lower than the record efficiencies of 16.4% fabricated on an ultrathin glass substrate, [107] 13.6% fabricated on metal foil, [95] and 15.5% fabricated using thermomechanical (i.e., using liquid nitrogen) lift-off process [108]. So far, the superstrate device is efficient in both flexible and rigid CdTe solar cells. However, superstrate configuration is limited to a specific, transparent substrate. Postgrowth processing like CdTe deposition, CdCl₂ treatment, and back contact processing significantly influence the hidden front interface, which is unreachable, despite providing freedom for back contact proceeding. Therefore, the fabrication processes or material deposition conditions need to be modified to better front interface engineering and control back contact processing.

In this work, the CdS and CdTe films are deposited sequentially on a mica sheet. Owing to the moisture sensitivity characteristic of mica, a CdCl₂ vapor treatment is introduced for the CdS and CdTe films. We find that an additional CdCl₂ vapor treatment for the CdS film before CdTe deposition helps improve the morphology of CdS and the afterward deposited CdTe absorber, enhancing PCE to 12.6%, which is 23.9% higher than previously reported PCE using mica as a mediate substrate.

5.1.2 Experimental Details

5.1.2.1 Fabrication of the CdS/CdTe film stacks on mica sheet:

Here freshly cleaved mica sheet is used as a mediator substrate for all flexible CdTe solar cell. A cadmium sulfide (CdS) buffer layer (100 nm) was thermally evaporated at room temperature under 4×10^{-7} Torr pressure, at a rate of 1.0 nm/s. The evaporating temperature of the crucible controls the deposition rate, and the quartz crystal monitor measured the thickness of the film. A 4µm CdTe absorber layer was deposited by the closed space sublimation (CSS) method with a source temperature of 580 °C and a substrate temperature of 520 °C in a 1% oxygen and 99% argon environment. Afterward, thermally evaporated CdCl₂ treatment was carried out in a closed space sublimation system with source temperature 385 °C and substrate temperatures at 390 °C for 30 mins. A film deposited on mica sheet is very sensitive to wet conditions, that prevents it to use any solution treatment. Therefore, dry $CdCl_2$ treatment is dispensed for all devices. Moreover, CdCl₂ treatment is taken as an optimizing parameter to fabricated efficient device. We fabricated two set of samples where, first set of samples with conventional CdCl₂ treated as define above and the second set of samples undergo twice CdCl₂ treatment one for CdS film at 400 °C for 5 mins in nitrogen and another conventional CdCl₂ treatment for CdTe. Subsequently, 3.5 nm copper (Cu) and 50 nm gold (Au) bilayer were thermally evaporated and annealed at 200 °C for 20 minutes in nitrogen ambient to facilitate Cu activation.

5.1.2.2 Peeling and completing device:

The film stacks were then peeled off from mica sheet through water-assisted liftoff process. To ease the lift-off process, epoxy and flexible sheet was attached on the film allow naturally dry. Then, the film stack with back sheet was immersed into DI water to facilitate the delamination process. Within a few minutes, mica sheet and the film stacks were separated. The separation is mainly attributed to a weak Van der Waal force between CdS film and mica, which is weaker than the force of surface tension exerted by water. The peeled film was dried by nitrogen jet and 150 nm transparent conduction oxide indium zinc oxide (IZO) layer was deposited as a front contact. In this whole process mica sheet serves only to grow CdS and CdTe film. After the delamination mica sheet is not a part of the solar cell.

5.1.2.3 Characterization of the device:

The morphology of film was characterized by high resolution field emission scanning electron microscopy (FE-SEM, Hitachi S-4800). The device power conversion efficiency was characterized by measuring current-voltage(J-V) curves under dark and AM1.5G (100 mW cm⁻²) illumination using a solar simulator and a source meter (keithley-2400. The external quantum efficiency (EQE) spectra were measured using a EQE system from PV Instrument. Both the J-V and EQE systems are calibrated with a standard Si solar cell. The capacitance-voltage (C-V) profiling were measured in a dark at room temperature with a contact AC frequency of 10 kHz and a DC bias voltage sweeping from -2.0 V to 1.0 V. The Steady-state photoluminescence (PL) and time resolved PL (TRPL) measurement were performed though the IZO side with 633 nm laser wavelength. Steady-state PL signal was detected by a symphony-II CCD detector from Horriba, and TRPL signal was collected via a hybrid APD/PMT module from Hamamatsu R10467U-50). A surface topography and potential are measured by D3100 AFM and home-made KPFM system based on D3100 AFM respectively.



5.1.3 Results and Discussions

Figure 5- 1 Schematic illustration of flexible CdS/CdTe device fabrication using waterassisted lift-off method. (a) As-fabricated device on mica sheet. (b) water assisted lift-off procedures. (c) complete flexible device. (d) photo image of flexible CdS/CdTe device.

As shown in the schematic diagram of the lift-off process (Figure 5- 1 a to c), the flexible CdTe solar cells were fabricated in three steps. 1) CdS, CdTe films with Cu/Au back electrode was deposited on mica sheet, adhered with a flexible substrate of interest (e.g., aluminum foil, polymer sheet, or SU-8 photoresist), CdCl₂ treatments were performed after CdS and CdTe deposition, respectively. 2) The CdS/CdTe/Au/flexible substrate stacks were lift-off from the mica sheet through water-assisted lift-off process. This delamination phenomenon has been successfully reported by Wen [104]. It could be

worth noting that, before dipping the film stacks into water, the edge of mica sheet with film stacks was slightly cut with scissor to promote water penetration into the CdS and mica interface. In addition, the lift-off time depends on the choice of adhesive. We observe that SU-8 photoresist epoxy produces delamination within a few seconds while Loctite EA 0151 adhesive takes 5 minutes to delaminate 1.5×1.5 inches film stacks. 3) 150 nm indium zinc oxide (IZO) front contact electrode was deposited on the delaminated surface to complete the device.



Figure 5- 2 Top view SEM images of CdS (a) w/o and (b) with CdCl₂ treatment, (c) their comparative grain size distribution, the back surface of CdTe film grown on CdS (d) w/o and (e) with CdCl₂ treatment, (f) their comparative grain size, and the back surface of CdCl₂ treated CdTe film grown on CdS (g) w/o and (h) with CdCl₂ treatment, (i) their comparative grain size.

Due to the moisture sensitivity of mica, vapor CdCl₂ treatment was introduced during the device fabrication to avoid the untimely film peel-off. However, we found that the vapor CdCl₂ treatment after CdTe deposition is insufficient for the CdTe film recrystallization and the grain boundary passivation. To solve this issue, an additional vapor CdCl₂ treatment for the CdS film before CdTe deposition is carried out to maximize the device performance (labeled as CdS with CdCl₂). To figure out the effect of CdCl₂ treatment for the CdS film annealed at the CdCl₂ treatment temperature but without the presence of CdCl₂ (labeled as CdS w/o CdCl₂) was used as a reference.



Figure 5- 3 Top view SEM images of peeled surface of CdS (a) w/o and (b) with CdCl₂ treatment, (c) grain size distribution of peeled surface of device stacks for CdS with CdCl₂.

Scanning electron microscopy (SEM) imaging was carried out to characterize the morphologies of the CdS films with and without the CdCl₂ treatment. It was observed that the CdS without CdCl₂ treatment (Figure 5- 2 a) shows an average grain size of 46 nm, which is much smaller than 118 nm in the CdS film treated with CdCl₂ (Figure 5- 2 b). The improvement of CdS grain size promises larger grain size of the lateral deposited CdTe film (Figure 5- 2 e) than that on the CdS without CdCl₂ treatment (Figure 5- 2 d).

This is further demonstrated from the morphology of the CdTe film after CdCl₂ treatment (after step 1, Figure 5- 2 g and h). The improvement of CdS/CdTe grain size can help reduce the nonradiative recombination at grain boundaries and facilitate higher build-in potential, thus, higher open circuited voltage. After step 2, We further investigated the morphology of the delaminated front interface of CdS/CdTe/Cu/Au/SU-8 stacks with CdS film exposing out. In the device with CdS without CdCl₂ treatment, the grain size of CdS on the delaminated surface (Figure 5- 3a) is much smaller than that as before CdTe deposition (Figure 5- 2a), indicating a gradient change of the CdS grain size from the CdS/mica interface to CdS/CdTe interface. This suggests that the CdCl₂ treatment for the mica/CdS/CdTe stack is not sufficient to facilitate the Cl diffusion to CdS/mica interface. By introducing the additional CdCl₂ treatment for the CdS film, the grain size of the CdS at mica/CdS interface and CdS/CdTe interface show similar grain size, remedying the insufficient CdCl₂ treatment for the mica/CdS/CdTe stacks. We believe that mica or rigid substrate will not affect the diffusion of Cl during the CdCl₂ treatment for the substrate/CdS/CdTe stacks.

X-ray diffraction (XRD) patterns were further carried out for the back and the delaminated surface of the CdS/CdTe stacks (Figure 5- 4) using CdS with and without the CdCl₂ treatment. The front interface of CdS w/o CdCl₂ film shows strong (002) and (101) crystal orientation for CdS with a hexagonal structure, while under CdCl₂ treatment of both CdS and CdTe, the CdS has intense (002), (101), (004), and (202) peaks. The XRD pattern for the CdTe back surface after final CdCl₂ treatment for both CdS w/o CdCl₂ and CdS with CdCl₂ remains the same. At the front surface, film stacks in CdS with CdCl₂ is more randomly oriented when compared with the film with air annealed CdS which is

due to grain growth and recrystallization introduced by additional CdCl₂ treatment of CdS window layer. Unlike the literature report, vacuum evaporated CdS on mica substrate are epitaxial.



Figure 5- 4 X-ray diffraction patterns of the back and delaminated front surfaces of CdS/CdTe using CdS with and without CdCl2 treatment (red colored indices are corresponding to CdS and dark indices are corresponding to CdTe).

Table 5-	1 SCAPS	input	parameters	used to	simulate	band	diagram	and J-V	curves of
	CdS/Cd7	ſe sola	r cells with	diffenrt	work fun	ction			

Parameters	IZO	CdS	CdTe
Thickness (nm)	150	100	4000
Band gap (eV)	3.5	2.42	1.5
Electron affinity (eV)	4.5	4.5	4.4
Dielectric constant	9.0	10	10
CB DOS N _C (cm ⁻³)	2.2 x 10 ⁺¹⁸	2.2 x 10 ⁺¹⁸	1.8 x 10 ⁺¹⁷
VB DOS N _D (cm ⁻³)	1.9 x 10 ⁺¹⁹	1.9 x 10 ⁺¹⁹	1.8 x 10 ⁺¹⁹
Electron mobility (cm ² /s)	100	100	320
Hole mobility (cm ² /s)	25	25	40
Shallow donor density Nd (cm ⁻³)	1.0 x 10 ⁺¹⁹	(vary)	
Shallow acceptor density Na (cm ⁻³)	-	-	1.0 x 10 ⁺¹⁴
Lifetime (ns)	0.1/0.1	0.001/0.001	20/20
Interfaces	S _n (cm/s)	S _p (cm/s)	
(CdTe/CdS)	1.0 x 10 ⁺⁶	1.0 x 10 ⁺⁶	
(CdS/IZO)	1.0 x 10 ⁺⁶	1.0 x 10 ⁺⁶	



Figure 5- 5 KPFM analysis of the peeled device, (a), AFM, (b) KPFM Potential (c) the corresponding roughness profile and surface potential for CdS without CdCl₂ treated film stacks (d), AFM, (e) KPFM Potential (f) the corresponding roughness profile and surface potential for CdS with CdCl₂ treated film stacks, (g) SCAPS-1D simulated band alignment and (h) simulated device performance.

The increase of grain size with CdCl₂ treated CdS can be further demonstrated from the atomic force microscopy (AFM) images, which clearly shows that CdS with CdCl₂ treatment has significant increased CdS grain size compared to that without the CdCl₂ treatment. Surface roughness also increase for CdS with CdCl₂ is consistence with grain growth and recrystallization as shown in Figure 5- 5 (c) and (f). Measured surface roughness is less around 1 nm, which is insignificant to effect overall device performance. Further, a kelvin probe force microscopy (KPFM) was used to analyze the surface potential of the delaminated CdS/CdTe front surfaces. It was found that the average surface contact potential for CdS with CdCl₂ surface is 300 mV higher than that using CdS w/o CdCl₂ treatment. Higher surface potential implies that work function of CdS was reduced by 300 mV. Work function depends on the position of Fermi level. We believe that CdCl₂ treatment oxidize CdS window layer and increase their conductivity due to which Fermi level shift up and reduced work function. A SCAPS simulation has been performed to understand the effect of work function on carrier density and their relations with solar cells device performance. Table 5- 1 are the input parameters for SCAPS simulation. Our SCAPS simulation shows that when work function is decreased by 2.3 eV the carrier concentration of CdS increase from $1 \times 10^{+14}$ to $1 \times 10^{+18}$ cm⁻³ introduced downward bend bending as shown in Figure 5- 5 (g), which significantly reduced the front interface recombination and enhanced the V_{OC} (Figure 5- 5 h). This simulated result is consistent with the experimental result.



Figure 5- 6 (a) J-V curve, (b) EQE spectra, and (c), (d), (e), (f) are statistic of photovoltaic parameters V_{OC}, J_{SC}, efficiency and FF.
CdCl ₂	Voc	Jsc	FF (%)	PCE	Rs	R _{SH}
treatment	(mV)	(mA/cm ²)		(%)	(Ω.cm ²)	(Ω.cm ²)
CdS with	829	23.64	64.30	12.60	5.3	499
CdCl ₂						
CdS w/o	788	23.36	60.34	11.11	7.0	434
CdCl ₂						

Table 5- 2 J-V Parameters of best flexible CdTe solar cells under single and double CdCl₂ treatment.

Figure 5-6 (a) shows the measured J-V curves of the best cells for CdS with CdCl₂, and CdS w/o CdCl₂ treated devices, and the best cells' performance was summarized in Table 5-2. As seen, CdS with CdCl₂ device demonstrates a maximum PCE of 12.60 % with an open-circuit voltage (V_{OC}) of 829 mV; a short-circuit current density (J_{SC}) of 23.64 mA/cm² and a fill factor (FF) of 64.30 %. However, CdS without CdCl₂ device has a maximum PCE is 11.11 % with a Voc of 788 mV, a J_{SC} of 23.36 mA/cm², and a FF of 60.34 %. The detailed photovoltaic parameters are tabulated in Table 5-2, and the statistics of 14 cells are shown in Figure 5-6 (c), (d), (e), and (f). A CdS with CdCl₂ device demonstrates better performance than CdS w/o CdCl₂ treated device. An overall improvement in the photovoltaic parameter is solely due to the CdCl₂ treatment of the CdS buffer layer. The improvements in V_{OC} and FF are attributed to the improved crystallinity, larger grain size, and passivated interface. SEM images clearly show that CdCl₂ treatment recrystallizes CdS grains and provides better grain growth for CdTe. We believe that the first CdCl₂ treatment might endorse CdTe grain growth and front interface passivation. However, measured V_{OC} and FF are slightly lower than the efficient superstrate device [15], mainly due to chloride and oxide residue remaining after CdCl₂ treatment. This residue leads to reduce R_S , and R_{SH} . It shows that, there is further room to enhance these device performances. Figure 5- 6 (b) displays the measured external quantum efficiency (EQE). CdS with CdCl₂ device has a slightly better spectral response at the shorter wavelength region. This might be due to a better front interface. Both devices show a similar spectral response at the longer wavelength region, mainly due to the parasitic absorption loss caused by the thick CdS window layer or the result of a broken interface. Further work is currently proceeding to improve the front interface. We believe, the shorter and longer wavelength response can be enhanced by the insertion of CdSe between CdS and CdTe. To further investigate the effect of inserting a thin CdCl₂ layer in between CdS and CdTe, some characterization was performed.

Additionally, steady state photoluminescence (PL) and time-resolved photoluminescence was used to understand the front interface. Figure 5- 7 (a), and (b) shows the PL and TRPL spectra measured from a glass side with 633 nm laser excitation. The PL intensity for CdS with CdCl₂ device has significantly higher than CdS without CdCl₂ device. A strong PL intensity is due to the higher radiative recombination or less non-radiative recombination, which suggests less recombination at the interface directed to higher carrier lifetime. Further TRPL measurement conforms that CdS with CdCl₂ device has longer carrier lifetime (69.2 vs. 15.3 ns).



Figure 5-7 (a) PL intensity, (b) carrier lifetime calculation from TRPL, (c) carrier density profiles, and (d) Mott-Schottky plot and calculation of build-in potential of CdS with CdCl₂ and CdS without (w/o) CdCl₂ devices.

Furthermore, a capacitance-voltage (C-V) measurement was performed to explore the build-in potential (V_{bi}) at the CdS/CdTe interface and hole carrier density in the CdTe absorber. The V_{bi} is determined from the Mott-Schottky plot ($1/C^2$ vs. Bias voltage) as shown in Figure. 6(c). CdS with CdCl₂ treated device has significantly higher V_{bi} than CdS without CdCl₂ treated device (0.68 vs 0.50 V). An increase in V_{bi} for a double CdCl₂ treated device is consistent with an increase in V_{OC} measured from J-V measurement (829 vs 788 mV). Further hole carrier density in the bulk absorber is extracted from the C-V carrier density profile [Figure 6(d)]. A single value of carrier density is the bottom point of the distinct U-shape carrier profile [42, 109]. The extracted hole carrier density is 1.66 x 10¹³ cm⁻³ and 2.45 x 10¹³ cm⁻³ for single and double CdCl₂ treated devices respectively. According to the following relation, a change in V_{OC} can also be expressed in terms of the doping concentrations [110].

$$\Delta V_{\rm OC} = \frac{K_{\rm B}T}{q} \ln\left(\frac{N_2}{N_1}\right)$$

Where, K_B is the Boltzmann's constant, T is the temperature, q is electric charge, and N₁ and N₂ are the carrier densities of CdS without CdCl₂ and CdS with CdCl₂ treated devices, respectively. By using the above relation, different in V_{OC} is only 10 mV which is much lower than the total change in V_{OC} obtained from J-V measurement. Therefore, we believe that improvement in V_{OC} is contribution of various factors like reduction of interface recombination, improvement in bulk carrier density or CdCl₂ might improve the conductivity of CdS buffer layer.

5.1.4 Conclusion

In conclusion, we used a water assisted lift-off technique to delaminate CdS-CdTe film from mica sheet and attached it to a flexible substrate of interest and fabricated ultrathin, lightweight, flexible CdTe solar cells with maximum efficiency 12.60%. The lift-off film is smooth, mirror like and free of any residue. We introduced effective dry CdCl₂ treatment method. The CdCl₂ treatment of CdS gives larger grains and better nucleation for CdTe growth. A second CdCl₂ treatment further enhances the grain growth and recrystallization and provides superior CdS-CdTe interface due to which it has intense PL spectra and longer carrier lifetime.

5.2 Lightweight and Flexible CdSe/CdTe Solar Cells via Mechanical Peeling

5.2.1 Introduction

A Se alloy minimizes the bandgap from 1.5 eV of CdTe to 1.4 for CdSe_xTe_{1-x} by optical bowing [35], allowing additional infrared photons to be absorbed, leading to an increased long-wavelength spectral response [39]. Further, it observed that Se alloy passivated the front interface due to which a carrier lifetime was improved [111]. So, the incorporation of CdSe_xTe_{1-x} is vital steps for every highly efficient CdTe based solar cells. In chapter 4, we demonstrated that incorporating Se at the front interface of CdTe solar cell devices improved longer wavelength photon response, which increases J_{SC} and the overall device performance. By knowing the advantage of a graded CdSe_xTe_{1-x} absorber, we introduced a thermally evaporated 130 nm CdSe between CdS and CdTe in a flexible CdTe solar cell device and create CdSe_xTe_{1-x} absorber through CdCl₂ treatment and our preliminary result shows that power conversion efficiency improved from 12.6 % of CdS/CdTe to 13.35 %.

5.2.2 Experimental Detail

First, 80 nm CdS and 130 nm CdSe film were thermally evaporated in a freshly cleaved mica sheet. $3.5 \ \mu m$ CdTe was deposited by the CSS method. CdCl₂ treatment was carried out by evaporation at 420 °C for 30 mins at 400 Torr pressure in a dry air using a CdCl₂ source plate. Finally, $3.5 \ nm$ Cu and 50 nm gold were evaporated and annealed in nitrogen ambient to activate the Cu. Further, about 50 μm SU-8 photoresist

was spun on the gold electrode side, is a flexible substrate for delaminated film stacks. As observed in the SEM image, CdS and CdSe completed dissolved which helped CdTe film stacks mechanically peeled off from the mica sheet. Sometimes a mica residue can remain on film stacks which can easily remove by using scotch tape. Finally, a flexible CdTe solar cell was constructed by sputtering 150 nm ITO.

5.2.3 Results and Discussions



Figure 5- 8 Top view SEM images of (a) cross-sectional SEM image of CdTe film stacks on mica sheet, (b) peeled surface, (c) rare CdTe surface after CdCl₂ treatment.



Figure 5-9 (a) J-V curve and (b) EQE curve for the best CdS/CdSe/CdTe solar cell.

One of the detrimental issues we encountered with the CdS/CdTe device was small voids observed in the delaminated front surface. We assumed a thin CdS film layer was damaged during lift-off create a void. For CdSe/CdTe device, a cross-section and delaminated surface SEM images show that CdS and CdSe completely diffused due to the high solubility of Se at the front interface by creating graded CdSSeTe and CdSeTe alloy with CdTe Figure 5- 8 (a-b). There is no interfacial layer remains between the mica sheet and remain film stacks, which helps to generate smooth, crack-free, and void-free mechanical peeling. Furthermore, Figure 5- 8 (c) shows CdTe's rare face morphology after CdCl₂ treatment having similar grain size to the front peeled surface which further confirm complete diffusion of CdS and CdSe on CdTe.

Figure 5- 9 (a) shows the J-V characterization result of the flexible CdS/CdSe/CdTe solar cell. A maximum power conversion efficiency of 13.35 % with a V_{OC} of 827 mV, a J_{SC} of 26 mA/cm², and a FF of 62.1% has been demonstrated. A promising V_{OC} measured from J-V is comparable to the V_{OC} reported on a superstrate CdSe/CdTe device fabricated on rigid glass. In comparison, the FF of the device is still lower than the average FF of a rigid CdSe/CdTe device. The inferior FF might be due to the CdCl₂ residue remaining after the thermally evaporated CdCl₂ treatment. Noted, there was no cleaning was done for the rare surface after CdCl₂ treatment. It is suggested that the higher FF can be achieved by annealing CdCl₂ treated film stacks in a vacuum, which might remove the residue that remains on the CdTe surface. Figure 5- 9 (b) shows the measured external quantum efficiency for the best CdSe_xTe_{1-x} cell. The increased EQE response in the longer wavelength region implies the formation of CdSe_xTe_{1-x} alloy, which has a lower bandgap than that of CdTe, which allows the additional infrared

photon to be absorbed and higher J_{SC} . The measured J_{SC} for rigid CdTe solar cells under a similar structure is around 29 mA/cm² which suggests that still there is much room to improve J_{SC} which requires careful optimization of the CdSe_xTe_{1-x} absorber layer. Here we used metallic Cu doping, our previous work suggest metallic Cu is not a superior method for doping in CdTe. Even knowing that we used metallic Cu because mica is sensitive to the moisture which prevent using any wet treatment. Therefore, thermal evaporation of CuCl might be a better choice for Cu doping to improve device performance further.

5.2.4 Conclusion

The incorporation of Se created a low band gap graded absorber layer $CdSe_xTe_{1-x}$ at the front interface that increases longer wavelength photon response and increases the current collection without affecting V_{OC} and improved PCE from 12.6 % of CdS/CdTe to 13.35 %. More importantly, graded film stacks generate a smooth, crack, and void-free peel-off from the mica sheet.

5.3 Thermal Stress Delamination of Rigid CdTe Solar Cells

5.3.1 Introduction

Delamination of CdTe solar cell devices from a rigid FTO coated glass substrate has enormous applications, from understanding buried window layers to fabricating lightweight and flexible CdTe solar cells in a substrate of interest having high specific power (W/kg). Recently McGott used the thermomechanical delamination approach to explain the impact of front interface quality in copper and arsenic doped $CdSe_xTe_{1-x}$ solar cells [103, 108]. We believe this approach is applicable for further understanding our efficient CdTe solar cell and the construction of flexible solar cell devices with high specific power (W/kg).



Figure 5- 10 (a) CdTe solar cell before delamination, (b) delamination procedure, and (C) photo image of reconstructed flexible CdTe solar cell.

5.3.2 Experimental Detail

First, rigid CdTe solar cell devices were fabricated in commercially available

T12D glass. 100 nm CdS and 130 nm CdSe layers were thermally evaporated on a NSG

T12D glass substrate. 3.5 µm CdTe was deposited in the CSS system at source

temperature 660 °C and substrate temperature 600 °C at 10 Torr pressure under a control

flow of 1000 sccm Argon and 10 sccm oxygen gas. Wet CdCl₂ treatment was carried out at 420 °C for 20 minutes under ambient dry air and the sample was cleaned to remove residues. CuSeO₃ back buffer layer spin-coated at 6000 rpm for 30 seconds and the sample was annealed in a CSS chamber at a peak temperature of 210 °C without holding time and allowed to cool down naturally. And finally, the rear contact 40 nm gold electrode was thermally evaporated, and the J-V curve was measured.

A second step was to coat a complete solar cell device with SU-8- 3500 epoxybased photoresists on a gold electrode. SU-8 photoresists act as a flexible substrate for a delaminated solar cell device. The thickness of the SU-8 photoresist was controlled by spin-coating speed, followed by soft baking at 100 °C for 10 mins and exposure to UV light for 2 minutes for hardening the SU-8 epoxy. After that, a CdTe solar cell device with a flexible substrate was dipped into liquid nitrogen. Within a few seconds, a film stacks were pop up (delaminated). We believe that delamination was by thermal stress generated by low-temperature liquid nitrogen between SnO₂-coated FTO glass and the CdSSeTe layer. Unfortunately, first set of delamination was not uniform and having some cracks. In a second set of devices where SU-8 photoresist was protected with duck-tap give more smooth delamination. After the delamination device was completed by depositing a 150 nm ITO front electrode via a shadow mask with a particular cell area of 0.09 cm².

5.3.3 Results and Discussions

The J-V curve of the newly reconstructed lightweight and flexible solar cell device was measured. Figure 5- 10 (a) shows a schematic diagram of a rigid CdTe solar

cell, Figure 5- 10 (b) thermal stress delamination through liquid nitrogen, and Figure 5- 10 (c) a photo image of the delaminated and reconstructed CdTe device. These are the preliminary results which show some cracks and a lack of 100 % delamination.



Figure 5- 11 (a) J-V curves and (b) EQE for CdTe solar cell device before delamination and after reconstruction.

Table 5-3 Device performance before delamination and after reconstruction of CdTe solar

cells.

Processing	Voc (V)	Jsc (mA/cm ²)	FF (%)	PCE (%)
Before delamination	0.834	26.8	75.1	16.8
After reconstruction	0.797	24.1	55.6	10.7

We compare the solar cell device performance before delamination and after reconstruction. Figure 5- 11 (a) and (b) shows the J-V curve and EQE of two solar cells before delamination and after reconstruction, respectively and Table 5- 3 summarizes their photovoltaic parameters. A reconstructed CdTe retains about 65 % of its before-

delaminated power conversion efficiency. We observed severe degradation in the current collection (26.8 vs. 24.1 mA/cm²) and fill factor (75.1 vs. 55.6%). According to EQE response, a reconstructed device has a poor shorter-wavelength response which might be due to a lack of window layer at the front interface, which further creates a bad front junction that also affects the fill factor of the device. I believe that device performance can be enhanced by introducing a suitable window layer.

Specific power is always a primary consideration parameter for lightweight and flexible solar cells. Specific power is the maximum power generated by solar cells per unit area mass density (W/kg). It can be calculated by knowing the maximum power generated by the solar cell and the total areal density of solar cell materials [112]. The maximum power generated by the solar cell is a product of solar cells' power conversion efficiency and incident power which is 1 W/m² (100 mW/cm²) under AM1.5, one sun irradiation.

Material	SLG	SnO ₂	CdS	CdSe	CdTe	Au	ITO	SU-8
Thickness	3 x	400	100	130	3500	50	150	5 x
(nm)	10+6							10^{+4}
Volume	2.5	6.95	4.82	5.81	5.85	19.3	7.14	1.15
Density								
(g/cm ³)								
Areal	7500	2.78	0.48	0.75	20.47	0.96	1.07	57.5
Density								
(g/m ²)								

Table 5-4 Calculate area mass density of respected solar cells materials.

Table 5- 4 summarizes the thickness and volume density of individual solar cell layers used to construct solar cell devices. The areal density of each layer was calculated by simply dividing volume density by their corresponding thickness. Since the thickness of the CuSeO₃ layer is less than 10 nm, their overall effective areal density is less than 0.05, so we neglected it. Power conversion efficiency (PCE) was 16.8 % for normal rigid CdTe solar cells, and its corresponding total area mass density is 7525 g/m². So, a rigid solar cell's calculated specific power density is about 22.3 W/kg. At the same time, in reconstructed lightweight and flexible solar cells with PCE 10.7 %, the areal mass density of 80.2 g/m² has a specific power density of 1330 W/kg, which is nearly 60 times higher than the rigid solar cells. It means a newly reconstructed solar cell has unique space application due to its flexibility, lightweight, and superior specific power (W/kg). If we achieve perfect delamination, the device performance might be further improved.

5.3.4 Conclusion

We delaminated a rigid CdTe solar cell device using thermal stress generated by liquid nitrogen and reconstructed a lightweight and flexible CdTe solar cell that retains nearly 65 % power conversion efficiency. A reconstructed flexible CdTe solar cell has a specific power of 1330 W/kg, nearly 60 times higher than the initial rigid CdTe device.

Chapter 6

Dissertation Summary and Work in Progress

6.1 Overall Summary

So far, Cu doping is one of the essential parts of rigid and flexible CdTe solar cells, which has pros and cons. Control Cu doping improves the CdTe doping density and reduces bulk defect and back-barrier height, while an excessive amount of Cu creates compensative effects. Currently, most CdTe research focuses on high-efficiency rigid CdTe devices. In contrast, flexible CdTe devices do not get much attention, although it has broader application, from incorporation in curve surface to space application. That motivates us to work on controlling Cu doping and flexible CdTe solar cells. Through the investigation in this dissertation, we supplied a deep understanding of the Cu doping mechanism, developed a new hole transport material for CdTe solar cells, and developed delamination and reconstruction methods to fabricate lightweight and flexible CdTe solar cells.

First, we studied the effect of metallic and ionic Cu doping on two sets of rigid CdTe solar cells with CdSO and ZMO as window layers. After careful optimization, we concluded that ionic Cu doping gives better Cu control. Due to this, we achieved better front junction quality, lower back-barrier heights, and better bulk defect properties. Further, we observed that the effect of excessive Cu is more notorious in CdTe solar cells with the ZMO as a window layer than with CdSO. Additionally, the sensitivity of ZMO window layer to the outer atmosphere brings reproducibility and stability risks. Therefore, CdSO is a strong n-type coupling partner as the window layer in CdTe solar cells, described in detail in chapter 3.

Chapter 4 introduced a wide band gap novel CuSeO₃ hole transfer material. CuSeO₃ has a dual application that provides Cu source and low barrier hole transfer layer. We fabricated CdS/CdTe/CuSeO₃ and CdSe/CdTe/CuSeO₃ solar cells on commercially available TEC12D glass and demonstrated 16.7% and 18.5% power conversion efficiencies, respectively.

The third part of the dissertation discussed lightweight and flexible CdTe solar cell devices fabricated using a water-assisted lift-off process. This study focused on the delamination of CdS/CdTe film stacks, transferring them into the substrate of interest. We demonstrated that additional CdCl₂ treatment for the CdS window layer can help to improve the conductivity of CdS, and better grain growth for CdS and CdTe, which suppress interfacial recombination; thereby, the device performance was improved. We also developed another two delamination methods. A mechanical peeling of CdS/CdSe/CdTe device. Since CdS and CdSe are completely diffuse in CdTe and create a graded alloy, there is no interfacial layer between mica and CdTe, making smooth mechanical peeling possible. Moreover, we also developed thermal stress delamination of a rigid CdTe device. Here, thermal stress generated by liquid nitrogen delaminated CdSe_xTe_{1-x}/CdTe device stacks from the substrate and provided a unique opportunity to

study the front interface. The reconstructed device was lightweight and flexible with a high specific power.

6.2 Work in Progress

6.2.1 CdSe as an Absorber Layer for Thin-Film Solar Cells

A cadmium selenide (CdSe) is a binary compound having a direct band gap of 1.7 eV which has great potential as top cell for tandem solar cells [113]. It has been theoretically demonstrated that a maximum efficiency of 44 % is achievable for tandem solar cells when 1.7 eV top cell is accompanied with commercial silicon solar cells. CdSe has been extensively used to create CdSeTe alloy by interdiffusion between CdSe and CdTe in the past decades. However, there is not much attention being paid to CdSe thinfilm solar cells with itself as absorber. Here, we did a preliminary investigation on this and achieved a 3.4% power conversion efficiency, indicating great application potential in photovoltaics.



Figure 6-1 (a) Schematic diagram of the CdSe solar cell and (b) cross-sectional SEM image.

CdSe solar cells were fabricated on commercial FTO coated glass (NSG_T12) substrate. $3 \mu m$ CdSe absorber layer was deposited by thermal evaporation method at

substrate temperature 200 °C. The thickness and deposition rate were controlled by evaporation temperature which was monitored by quartz crystal monitor. The distance between the source and substrate in our thermal evaporation system is about 1 foot due to which the deposition rate is low. After CdCl₂ treatment at 420 °C for 20 mins, PEDOT: PSS as a hole transfer layer was spun-coated at 2000 rpm for 30 second followed by annealing at 150 °C for 10 mins. Finally, device was completed by sputtering 150 nm ITO as electrode (Figure 6- 1).

SEM surface image reveals that the as-deposited CdSe film at 200 °C substrate temperature has less than 2 μ m grains (Figure 6- 2 a). Post annealing or CdCl₂ treatment shows substantial recrystallization and grain growth to 4 μ m (Figure 6- 2 b and c). In comparison to the anneal treatment without the application of CdCl₂, CdCl₂ treated film are smoother with intense XRD pattern (Figure 6- 2 d), suggesting that chlorination gives better recrystallization. XRD pattern analysis shows that thermally evaporated CdSe at 200 °C substrate temperature has a cubical phase (Jade #97-004-1528). After annealing or CdCl₂ treatment, it converted into hexagonal (Jade #97-004-1491) (Figure 6- 2 d).



Figure 6-2 (a-c) Top-view SEM image and (d) XRD pattern of CdSe film.



Figure 6- 3 (a) J-V curves, (b) EQE spectra, and (c-f) average statistical distribution of photovoltaic parameters of 20 best cells for each device.

We fabricated two sets of solar cell devices, one with CdCl₂ treated CdSe, another with CdSe annealed under identical conditions but without the presence of CdCl₂. As shown in Figure 6- 3 (a), CdCl₂ treated device has better V_{OC} (645 vs 576 mV), J_{SC} (13 vs 9.7 mA/cm²), FF (41.1 vs 37.1 %) and efficiency (3.4 vs 2.0%) in compared to the devices with annealed CdSe. Further, statistical distribution of photovoltaic parameters also shows that overall device performance was enhanced by CdCl₂ treatment (Figure 6-3 c-f). It was clear that CdSe annealed device has insufficient photon response over the long and short wavelength region in EQE spectrum (Figure 6- 3 b). This indicates that CdCl₂ treatment is essential to increase the photoactivity of CdSe, which might be the topic of further investigation. In this preliminary investigation, a CdSe solar cell efficiency of 3.4% is demonstrated, which is comparable to the reported high efficiency CdSe solar cells.

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Appendix A

List of Publications

- Rijal, S. Li, D.-B. Awni, R.A., Xiao, C. Bista, S.S. Jamarkattel, M.K. Heben, M.J. Jiang, C.-S.; Al-Jassim, M. Song, A. Yan, Y. Templated growth and passivation of vertically oriented antimony selenide thin films for high-efficiency solar cells in substrate configuration. *Advanced Functional Materials*, 2021, 2110032.
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