A Dissertation

entitled

Improving Performance in Cadmium Telluride Solar Cells: From Fabrication to Understanding the Pathway Towards 25% Efficiency

by

Geethika Kaushalya Liyanage

Submitted to the Graduate Faculty as partial fulfillment of the requirements for the

Doctor of Philosophy Degree in Physics

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December 2021

An Abstract of

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Polycrystalline Cadmium Telluride has been developed to be one of the most commercially successful materials for photovoltaic module production with power conversion efficiencies over 21% for research cells to over 18% for module efficiencies. However, little is known about these record devices architecture or the processing methods. Following conventional understanding of a CdTe solar cell operation, researchers have put extensive efforts over the years to improve the CdTe device performance through improved material quality and diode quality. While this have gained some benefit, performance limiting factors to these devices remains unchanged. Deviating from conventional concepts, better understanding of the device physics is needed in order to further improve these devices. This dissertation focusses on identifying these loss mechanisms and setting guidelines to fabricating high efficiency CdTe devices through both experimental and numerical simulation.

Experimental work discusses the details to construction and characterization of a CdTe deposition system and employing the new understanding of improving the CdTe device to achieve high performing CdTe devices. Here the traditional CdS window layer is

replaced by a wide bandgap $Mg_xZn_{1-x}O$ to increase the photocurrent generation with better band alignment. With optimum deposition and processing conditions, work demonstrates a device with power conversion efficiency >16%.

With a good front contact, performance of the device can be limited by the poor back contact. Expanding the understanding to front contact band alignment, characteristics of a back buffer layer suitable for CdTe back contact is also explored. Through 1D numerical simulation of the conduction and valence band offset, doping levels of the CdTe and back buffer layer material, this dissertation work sets the guideline to achieving CdTe device performance up to 25%.

This Dissertation is dedicated to…

My wonderful parents who gave everything to raised me

and

My wife who believed in me become the person I am today

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Finally, I would like to acknowledge my mother, my father and my wife Ning, and close friends for their constant support in the aspirations of my life. Without their support, this work would not be complete.

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List of Abbreviations

ABSG.....Aluminum Borosilicate Glass
AZO .....Aluminum Doped Zinc Oxide
BSRV .....Back Surface Recombination Velocity
CB .....Conduction Band
CBO/VBO.....Conduction/Valence band offset
$CdCl_2$.....Cadmium Chloride
CdS.....Cadmium Sulfide
CdTe.....Cadmium Telluride
CSS .....Closed Space Sublimation
CTO.....Cadmium Stannate (Cd_2SnO_4)
CZT .....Cadmium Zinc Telluride
DA.....Dry Air
E_F.....Fermi Level
EDS .....Energy Dispersive X-ray spectroscopy
EQE.....External Quantum Efficiency
FSRV .....Front Surface Recombination Velocity
FTO.....Fluorine dope Tin Oxide (SnO_2:F)
HRT.....High Resistive Transparent
HT .....Heat Treatment
IFLO.....Initial Fermi Level Offset
IR.....Infra-Red
MZO.....Magnesium Zinc Oxide
MZT .....Magnesium Zinc Telluride
PCE .....Photo-Conversion Efficiency
PV .....Photovoltaics
QNR .....Quasi-Neutral Region
SCR.....Space Charge Region
SEM .....Scanning Electron Microscope
SLG.....Soda Lime Glass
SRH.....Shockley-Reed-Hall
STEM.....Scanning Tunneling Electron Microscope
TCO.....Transparent Conducting Oxide
VB .....Valence Band
XRD .....X-Ray Diffraction

List of Symbols

θ.....Angle
η .....Device efficiency
χ .....Electron affinity
A.....Diode quality factor
E_A .....Electron Affinity
E_C .....Energy at conduction band minimum
E_V .....Energy at valence band maximum
FF .....Fill Factor
J_{Back} .....Back contact recombination current density
J_{Bulk}.....Bulk recombination current density
J_{Front} .....Front contact recombination current density
$J_{generated}$.....Generated current density
J_L .....Light generated current density
J_o.....Dark saturation current density
J_{Ph} .....Photon current density
$J_{Recombined}$ .....Recombination current density
J_{SC}.....Short Circuit Current Density
J-V.....Current Density-Voltage
MPP .....Maximum Power Point
q.....Charge of an electron
R_{Series} .....Series resistance
R_{Shunt}.....Shunt resistance
n.....electron concentration
N_C.....Effective density of states at the edge of conduction band
N_V.....Effective density of states at the edge of conduction band
p.....hole concentration
p_{CdTe}.....CdTe doping concentration
S_n/S_p .....Electron/Hole interface recombination velocity
T.....Temperature
V.....Applied voltage
V_{bi}.....Build-in-potential
V_{OC}.....Open Circuit Voltage
W.....Depletion width of a p-n junction
X_n .....Depletion width in n-doped region
X_p .....Depletion width in p-doped region

Chapter 1

Introduction

1.1 Background

Growing population and industrial expansions has pushed the world energy demand to new heights over the years. According to reports, primary energy consumption in US alone has reached 100.2 quadrillion Btu[1]. Statistical review of World energy shows that more than 80% of the energy consumption supplied by these fossil fuels such as petroleum, natural gas and coal in year 2020 [2]. When fossil fuels are burned in this proportion, a tremendous amount of stored carbon and greenhouse gases are released to atmosphere causing drastic changes to the Earth's climate; a trend raising significant environment and health risk to humans. Studies show that burning fossil fuels accounted for 74% of US greenhouse gas emission in 2019[3].

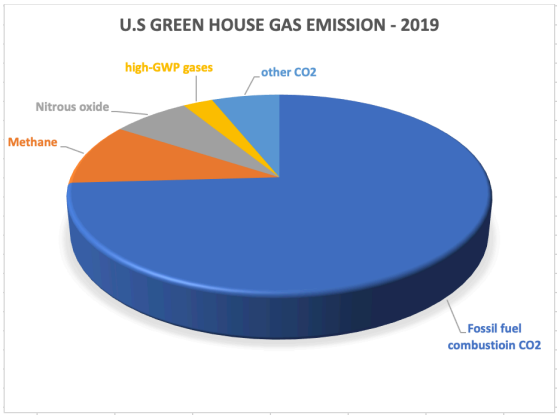

Figure 1.1 U.S Greenhouse gas emission by Gas in year 2019 [Data from Ref. [3]]

With increasing demand, limited supply of these fuel is being depleted and not renewed. Coupling with this, high environmental risk has forced people to move towards renewable energy sources to meet the energy demand. Several options exist to transition away from fossil fuel economy towards much cleaner sources of energy generation. Hydropower, geothermal, wind, and solar energy are few among these clean energy generation methods that shows the highest potential to compete with the traditional fossil fuels. As a result, implementation of renewable energy has been rapidly growing over the last decade, and energy produced from these renewables sources has grown almost 3 times compared to what was in 2000. It's expected that 2021 forecast sets the renewable electricity capacity additions closing to 200 GW[3].

1.2 Potential of Solar Energy & Photovoltaic Devices

Chief among the renewable energy sources, solar power stands out as one of the most cost-effective sustainable energy generation methods. According to the reports from International Energy Agency (IEA), solar power technology has become the "cheapest electricity in history" for projects with low cost financing and high quality resources[4]. While the favorable policy support and finance play a role to achieve this title, advancements to module performance and cost-effective processing method have been a tremendous aid to take the solar PV market to a record all-time high. IEA expects total of >250 GW addition from solar, making PV growth accounting for almost over 55% of all renewable energy expansions in the next two years[4].

The amount of sunlight striking the earth surface within a half an hour is sufficient to support the worlds energy need for an entire year[5]. The light from sun

arrives at earth surface as spectrum of discrete energy units called photons. Figure 1.2 shows the distribution of these photons incident on a surface various levels from earth's atmosphere. Light received at sea level provides us a normalized intensity of 1000 W/m^2 which is commonly used as the standard for characterizing the solar energy conversion.

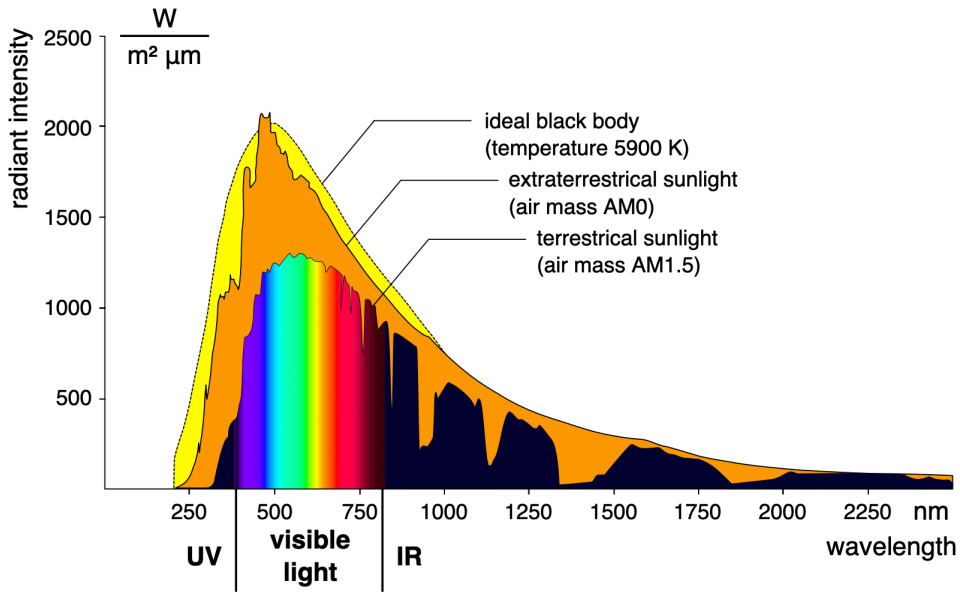

Figure 1.2 Spectrum of solar radiation at different levels from Sun to Earth's atmosphere [Adapted from Wikimedia Commons[6]]

A photovoltaic (PV) device can directly convert this energy into electrical energy. Fundamentally a PV device consists of one or more semiconductor materials tied with metal and transparent electrical contacts. Portion of the incident solar radiation is absorbed in a semiconductor layer to produce electrons and holes and these generated charges are extracted through the respective contacts. Currently, many semiconductors material are in use as absorbers. Table 1.1 list some of the most popular materials used in today's PVs and their corresponding band gap energy.

Table 1.1: Semiconducting photovoltaic materials with the corresponding band gap[7].

Semiconductor Material	Bandgap Energy (eV)
Si	1.11
GaAs	1.43
CdTe	1.5
CIGS	1.0
a-Si:H	1.55 -2.05

1.3 Solar Cell Basics

1.3.1 Semiconductors & Doping

Bandgap energy determines optical properties of a semiconductor material for its PV applications. For any material, energy bands are formed due to electronic states of the atoms closely spaced in energy and momentum. The bandgap energy is defined by the energy difference between the highest occupied energy state – Top of the Valence Band (E_V), and lowest unoccupied energy state – Bottom of the Conduction Band (E_C). *Fermi level* (E_F)is defined as the chemical potential of electrons at zero absolute temperature where there is a 50% probability of being filled with an electron. For a typical metal or semi-metal, the Fermi level lies inside one of these bands, allowing electrons to flow easily. In a semiconductor or an insulating material, Fermi level positioned between the bands requiring additional energy for any electrons to flow, with this energy >3 eV for a typical semiconductor. Materials used in PV devices, consist with bandgap energy just suitable to allow absorption of the photon energy from the solar spectrum.

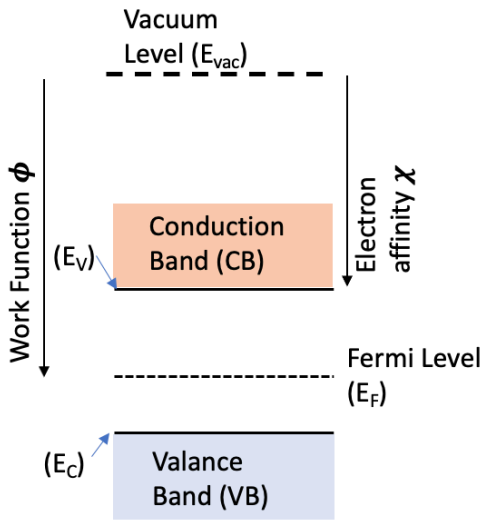

Figure 1.3 Filling of electronic states in an intrinsic semiconductor material where Fermi level is located at the middle. E_V and E_C mark the top/bottom of the Valence/Conduction band respectively.

At thermodynamic equilibrium, the relative concentration of electrons and holes in a particular material determines the probability of occupation. By solving the density of states as a function of energy, we can obtain the electron(n) and hole(p) concentration at respective CB and VB.

$$n = N_C \exp\left[-\frac{(E_C - E_F)}{kT}\right];\ p = N_V \exp\left[\frac{(E_V - E_F)}{kT}\right] \tag{1.1}$$

Where N_C and N_V represent the effective density of states at edge of E_C or E_V respectively. At a given temperature, the product of these two concentrations for a particular material is a constant which can be written as,

$$np = N_C N_V \exp\left[-\frac{E_g}{kT}\right] = n_i^2 \tag{1.2}$$

Where, E_g is the band gap of the material and n_i is the free electron and hole concentration in an intrinsic material. An intrinsic semiconductor is a pure defect free

crystal where at equilibrium, the electron and hole concentration are equal. In a typical material, the effective density of states at E_C or E_V are equal AND the effective masses of electrons and holes are equal, the Fermi level lies at the middle of the band gap of the material. Electron affinity of a material is also derived from E_F, which is the energy required to remove an electron denoted as χ in figure 1.3.

With increasing electron concentration in the CB over the intrinsic value, $n > p$, which will result an n-type semiconductor. Then, in order to hold equation 1.2 true, $E_C - E_F < E_F - E_V$, which would suggest that Fermi level is much closer to E_C than E_V. Similarly, with increasing hole concentration to obtain a p-type semiconductor, Fermi level sits much E_V than E_C. By introducing a small amount of impurities in an intrinsic material to donate or accept electrons, extrinsic or doped material can be formed.

1.3.2 Formation of a P-N Junction Diode

When an n-type and p-type material are placed in contact, a p-n junction is established. This is also referred as a diode. Due to the charge imbalance caused by the donor and acceptor ions in the n-type and p-type regions, majority charge carriers diffuse across the junction producing a diffusion current flow from the p-type region to the n-type region. Similarly, charges diffused in both sides, a built-in field will form in the opposite direction to the diffusion current producing a drift current. When these two currents find equilibrium, a *depletion region* or a *space-charge* region (SCR) of carriers will be formed at the junction with a potential difference called built-in potential in the value of:

$$V_{bi} = \frac{kT}{q} \ln \left(\frac{N_A N_D}{n_i^2}\right) \tag{1.3}$$

The width of the depletion region can be evaluated using the below formula:

$$W = [\frac{2\varepsilon kT}{qV_{bi}} (\frac{1}{N_A} + \frac{1}{N_D})]^{1/2} \quad (1.4)$$

Where the k if the Boltzmann constant, ε is the dielectric constant, q the electron charge, and N_A& N_D are acceptor and donor concentrations of a p-type and n-type semiconductor respectively.

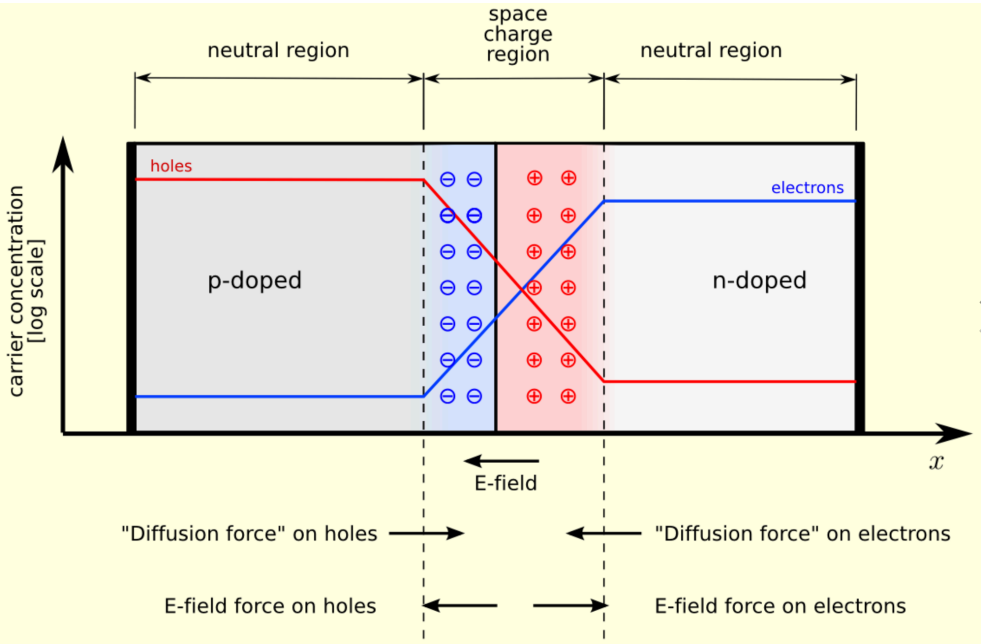

Figure 1.4 p-n junction at thermal equilibrium when no bias is applied. [Adapted from Wikimedia Commons[8]]

The region outside the SCR is called the *quasi-neutral* region (QNR) where with absence of an electric field, transport of the carriers will occur by diffusion. The extent of the depletion width into p- and n- regions depends on the dopant concentration of the n-type and p-type semiconductors respectively. And the depletion region in respective regions can be modified as,

$$X_n = \frac{WN_D}{N_{A+}N_D} \text{ and } X_p = \frac{WN_A}{N_{A+}N_D} \quad (1.5)$$

In forward bias, the electrostatic potential across the depletion region will be reduced by the applied voltage and the depletion width will be modified to be smaller than the original value and the current increases exponentially with increased forward bias. In reverse bias, the depletion width increases and the current flowing through the junction approaches the saturation current density, J_0. This diode type behavior can be explained using the below equation.

$$J = J_0[\exp\left(\frac{qV}{kT}\right) - 1] \tag{1.6}$$

When in dark, the current density-voltage characteristic of the junction behaves according to the equation 1.6 with an exponential dependance on voltage. When the solar cell is illuminated, photons are absorbed exciting the electrons from valence band to conduction band. With the built-in field, these charges are separated, driving the electrons to the n-type side and the holes to the p-type side of the junction. The generated current is exponentially increased with applied voltage and the current flow is shifted by the amount of light induced current. If an ideality factor of A and parasitic resistance behavior is assumed in the diode, the solar cell current-voltage curve can be re-written as equation 1.7 to account the loss mechanisms deviating from achieving the ideal performance.

$$J = J_0\left[\exp\left(\frac{q(V-R_{series}J)}{AkT}\right) - 1\right] - J_L + \frac{V}{R_{Shunt}} \tag{1.7}$$

1.3.3 Photoconversion Efficiency

In simple terms, the photo conversion efficiency of a solar cell can be put as,

$$Efficiency = \frac{Max\ Power\ generated\ Power\ from\ the\ solar\ cell}{Incident\ power} = \frac{P_{max}}{P_{in}} = \frac{V_{mp}\times J_{mp}}{P_{in}} \tag{1.8}$$

Where V_{mp} and J_{mp} is the voltage and current density at maximum power output of the solar cell.

In order to obtain the maximum power conversion efficiency, the generated photovoltage and the current at the maximum power point needs to be maximized. Figure 1.5 shows a typical current voltage characteristic of a solar cell illustrate using the modified diode equation in 1.7.

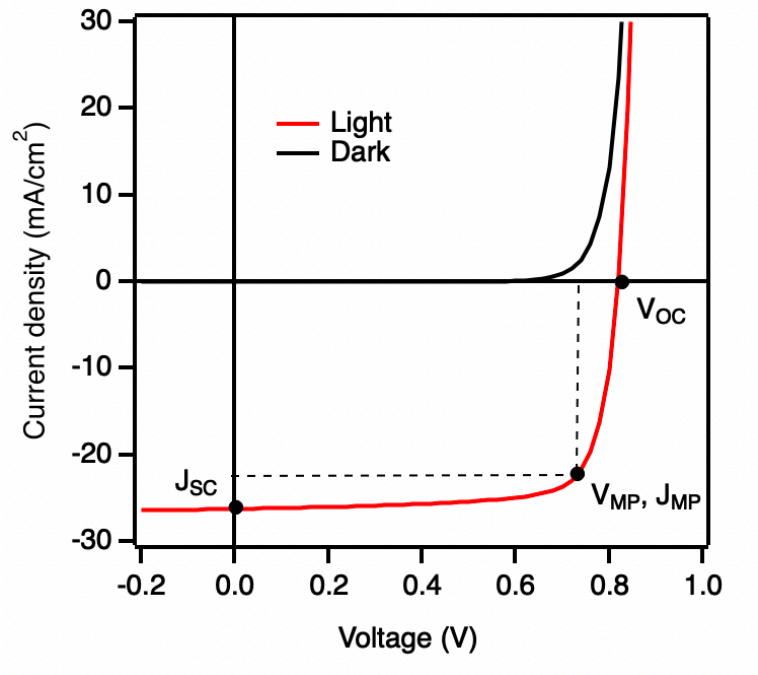

Figure 1.5 Typical Current density – Voltage characteristic in dark and light conditions. V_{OC} and J_{SC} points at each bias voltage. Maximum power point is used to determine the Fill factor of the device.

The current density at voltage zero is the short circuit current density (J_{SC}) and this approximately equate to the J_L for the devices. The open circuit voltage (V_{OC}) is defined where all the currents sum to zero and can be derived from equation 1.7 as,

$$V_{OC} = \frac{nkT}{q} \ln\left(\frac{J_L}{J_0} + 1\right) \quad (1.9)$$

Using these values, the conversion efficiency at Pmax can be re-written as,

$$\eta = \frac{V_{mp} \times J_{mp}}{P_{in}} = \frac{V_{OC} \times J_{SC} \times FF}{P_{in}} \quad (1.10)$$

Where FF measures the squareness of the J-V curve. A FF of 100% would mean that the J-V curve is rectangular and identifies as no parasitic losses like series or shunt resistance in the devices. However, the real-world devices, are consisted with all these loss mechanisms and in order to achieve maximum possible conversion efficiency, it's imperative to understand the behavior of the p-n junction model as well as understanding the loss mechanisms and the limitations of the material used.

1.4 CdTe Photovoltaics

Among all the PV technologies in hand, thin film CdTe solar cells show great potential populating solar market globally. Unlike the crystalline Si modules, where ~ 200 μm thick wafer is needed for full absorption of light due to low absorption coefficient and indirect bandgap, CdTe thin film PV modules need few micrometers of absorber material for the same task. Figure 1.6 shows absorption coefficient of different materials used in PV industry[9]. Clearly with the relatively large optical absorption coefficient, 1 μm thick CdTe layer can absorb 99% of the light above its bandgap.

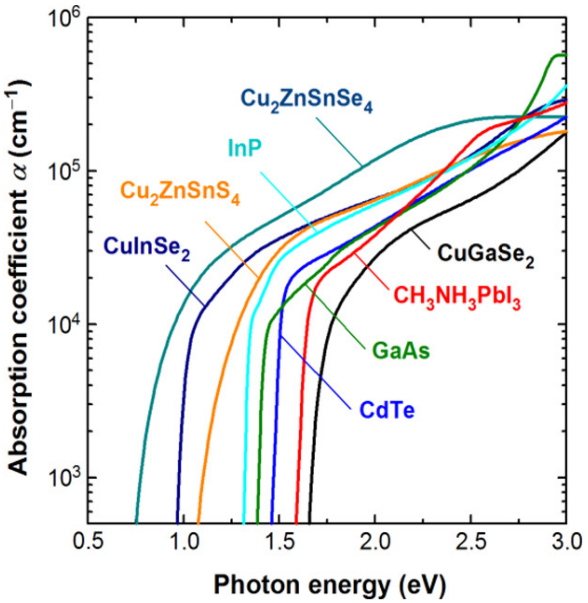

Figure 1.6 α spectra of various solar cell material as a function of the bandgap. [Reprinted with permission from Ref [9], copywrite (2018) Wiley with permission.]

Apart from these benefits, CdTe has attracted much attention due to its direct bandgap nature and nearly ideal bandgap energy for PV applications. Fabrication of CdTe devices have evolved over time with certified photoconversion efficiencies starting ~10%. While theoretical estimates for the maximum efficiencies up to 30% [10] for single junction CdTe cell, highest reported efficiency is 22.1%, a value that is comparative to record efficiencies of other materials.

1.5 Conventional Approach to CdTe Devices Improvements

Many techniques have been deployed for depositing CdTe material in both lab scale and manufacturing environment. Early CdTe devices consisted of having a CdTe absorber material, coupled with a n-type semiconductor such as CdS to form a p-n

junction. Devices were prepared in both substrate and superstrate configuration, shown in Figure 1.7, with superstrate being the favored of the community. CdS/CdTe stack was prepared with a transparent contact to allow the light to reach the absorber material and consisted with different semiconductor/metal back contact to extract holes. Device required a $CdCl_2$ activation step for recrystallization of the deposited material, to enhance the grain structure and reduce interface defects. Finally, doping with Copper (Cu) to lower the barrier during the back contact formation and introduce some p-type doping to the CdTe absorber layer.

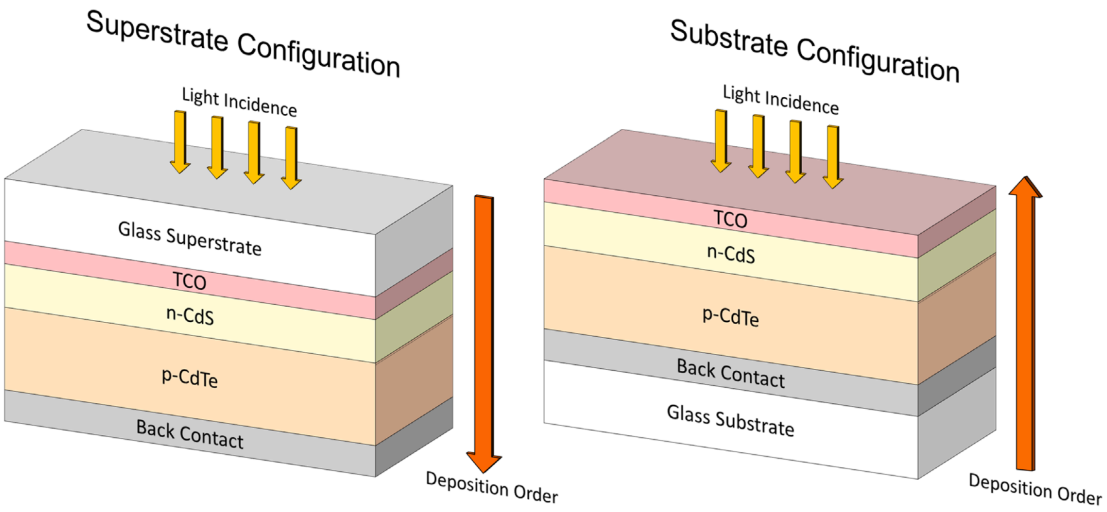

Figure 1.7 CdTe solar cell grown in superstrate (left) and substrate configuration(right). [Reprinted with permission from Ref. [11] Copyright (2016) Elsevier.]

With these device structures, CdTe device performance was stagnant ~16% for over a decade. Various strategies were deployed to improve, but these approaches were more compounded to conventional understanding of the CdTe solar cells. Below points highlights some of these strategies.

- Improve transparency in TCO [12-15]
- Reduce CdS layer or alternative material for window layer [12, 16-20]
- Obtain larger grains in CdTe through high temperature deposition techniques or post-processing [12, 18, 21-27]
- Managing barrier at the back with Cu doping [28]
- Employ back buffer layers like Te and employ electron reflector strategies [29, 30]

While these strategies do bring improvements to device performance, these approaches were insufficient to understand the real limiting factors of the device performance. Additional understanding of losses was required to further improve CdTe.

1.6 Improved Understanding for CdTe device physics

For a typical solar cell current density can be written as,

$$J_{Effective} = J_{Generated} - J_{Recombined} = J_{Ph} - J_{Front} - J_{Bulk} - J_{Back} \quad (1.11)$$

for all voltages and light intensities, where $J_{Generated}$ is the current density generated in the solar cell, and $J_{Recombined}$ is the recombination current density. Here for an optimum absorber, J_{Bulk} accounts for radiative recombination as well as Shockley-Read-Hall recombination, where the energy states created by the defects states within the bandgap can act as non-radiative recombination centers. J_{Front} and J_{Back} denotes the recombination currents at the front and the back interfaces of the devices.

Research have put extensive efforts to optimizing the CdTe device structure to improve performance over the years, but only in recent years, has the field as a whole moved towards understanding these loss mechanisms and engineering the device to reduce these losses. Through numerical simulation followed by experimental methods, the conventional device understanding has shifted to improve performance by,

- Reducing the losses due to defective front interfaces.
- Alloying the CdTe absorber to increase the photocurrent generation and improve material quality
- Managing the barriers to reduce the recombination at the back interface

Though it's not stated explicitly always, these strategies can be highlighted as factors leading to obtain superior performance for modern CdTe devices beyond 20%.

1.6.1 Reduce the Front Contact Recombination

For an effective contact of a solar cell, the most obvious role is to efficiently extract the photogenerated carries to be used in an external circuit. As the most photoexcited carries are generated at the front contact, it is critically important to suppress the recombination at the front interface to maximize the electron collection while allowing the generated holes to be transported to the back contact of the device.

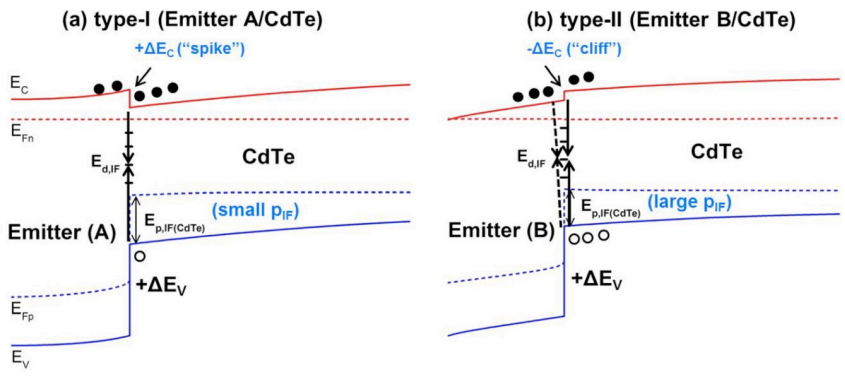

Figure 1.8 Band diagrams for two types of CdTe heterojunction, with interface defects, at 0.8 V bias under illumination, using the same ΔEC in both cases: (a) Type-I with positive ΔEC ("spike") and (b) Type-II with negative ΔEC ("cliff") [Reprinted with permission from Ref.[31] Copyright (2016) AIP Publishing].

For a non-degenerately doped window layer, if the conduction band is lower than that of the absorber layer ("Cliff" showed in Figure 1.8), the bending of the CdTe valence band maximum is much less allowing large number of holes to enter at the interface. This facilitates the interface recombination through defects present at the hetero interface.

On the other hand, if the conduction band of the window layer is above the conduction band of the absorber, there will be a barrier that electrons must overcome in order to be collected ("Spike" in Figure 1.8). When Fermi levels aligns at equilibrium, the CdTe conduction band minimum and valence band maximum near the interface bends downwards, reducing the effective hole concentration at the interface. Here, the Fermi level position of the emitter is a key factor to the degree of bending in the CdTe bands. With less effective holes at the interface, the recombination is suppressed enhancing the current collection at higher bias, thus increasing the V_{OC} and FF of the device. If the spike is too great, a barrier to the current flow will occur, losing effective current collection at the front contact.

Improved understanding of this front contact interface for the CdTe devices has inspired to use wide bandgap material[31-33] such as Magnesium Zinc Oxide (MZO), as a front contact buffer layer replacing the conventional CdS inferior window material.

Instead of a cliff as occur with a CdS window layer, fine tuning the bandgap of this MZO layer to form a narrow spike of $0.1\ eV \leq \Delta E_c \leq 0.3\ eV$, has allowed the modern-day research device performance to reach to higher baseline values.

1.6.2 Improved Current Generation and Reduced Bulk Recombination

As mentioned earlier in the text, CdS had been extensively used as the heterojunction partner for CdTe devices; however, due to its small band gap (2.4 eV), photons in shorter wavelengths are absorbed by the CdS, reducing the possible photo-generated current. To overcome this, various methods have been investigated, including reducing the thickness of the CdS layer[34, 35] incorporating oxygen to increase the bandgap of CdS[17, 19, 36] and using alternative wide bandgap window materials such ZnS[16]. But state-to-the-art devices has shown the most success of enhancing the current collection through band gap grading by incorporating Se in to the CdTe absorber. The first published work from Paudel and Yan[37] showed that using CdSe (bandgap ~ 1.7 eV) as the window material can lead to an enhancement of J_{SC} in both short and long wavelengths. The high solubility of Se in CdTe lead to the formation of a graded $CdTe_xSe_{1-x}$ layer during high temperature absorber preparation or post-deposition treatments (i.e., $CdCl_2$ treatment). Intermixed alloy layer exhibit high band bowing effect lowering the effective bandgap of the absorber layer compared to CdTe[38]. While the J_{SC} in long wavelength region is increased due to this, inter-diffusion of CdSe with the CdTe layer leads to the complete consumption of window layer, improving the photo response of the device in the short wavelength region. Figure 1.9 shows an external quantum efficiency illustrating the improvements to the current collection in the device that shows how tremendously J_{SC} can improve in long wavelength region.

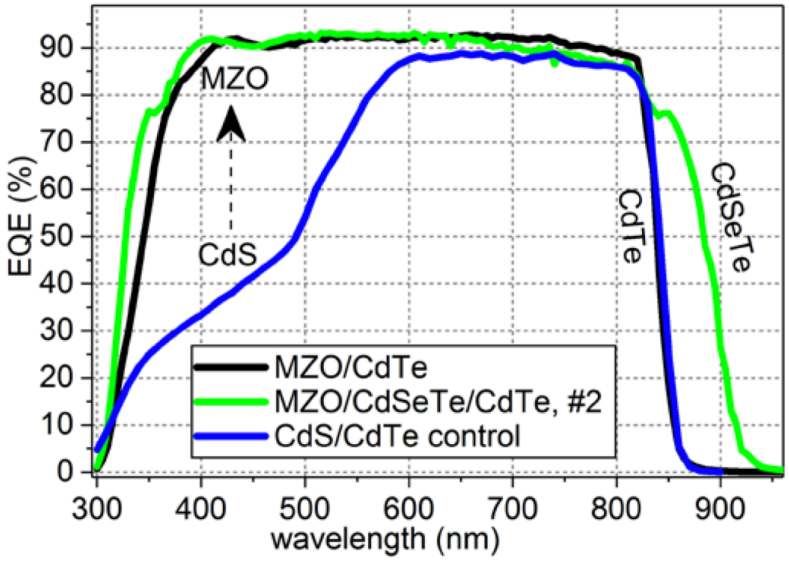

Figure 1.9 External quantum efficiency comparing devices with CdS window layer vs MZO. Devices with Selenium shows improved current collection in both short and long wavelengths compared to conventional CdS/CdTe device. [Reprinted (adapted) with permission from Ref.[39]Copyright (2018) American Chemical Society]

Loss of open circuit voltage (V_{OC}) and fill factor (FF) were observed in these $CdTe_xSe_{1-x}$ devices. While in earlier studies, a thin CdS layer was used to overcome this V_{OC} and FF loss[37], with new understanding for better front contact engineering, researchers have achieved significant device performance improvements using wide band gap MZO window layer with efficiencies reaching over 19%. Furthermore, recent studies show that with suppressing the front contact interfacial recombination, graded $CdTe_xSe_{1-x}$ absorber material can increase the minority carrier lifetimes 50 times greater compared to the CdTe absorber[40].

1.6.3 Improvements to Back contact

Recent Numerical modeling has set the path to achieving high performance front contacts for CdTe devices[32, 39, 41], suppressing the recombination at the front emitter/CdTe interface. These studies estimate that the minority carrier lifetime requirement for CdTe devices can be reduced to 25 ns in order to reach a PCE of 25%. However, all these studies have ignored the role of the back contact and assumed to have an ideal contact.

While the back contacts used today are not limiting the device performance, a good back contact is vital to achieving high efficiency CdTe devices. CdTe semiconductor material has a deep valence band energy (~ 5.95 eV)[42] because of its high electron affinity (χ = 4.5 eV) and the bandgap (1.45 eV), which would make it harder to form a suitable ohmic contact. Historically, doping the back surface of CdTe with copper (Cu) has been used to manage the barrier, but additional buffer layer material have been employed to achieve better performance. Although this was successful up to some extent, lack of understanding on the operation has been limitation to engineer superior back contact material stack for CdTe devices. Chapter 7 of this dissertation marks the first guidelines launched to select suitable back buffer material through numerical simulation. Analogous to the engineering work done at front contact emitter/absorber, this work investigates buffer layer conditions suitable for repelling the electrons to prevent back interface recombination while increasing the hole extractions. setting requirements to improve photoconversion efficiencies of the CdTe devices exceeding 25%[43].

1.7 Dissertation Overview

This dissertation focuses on improving the CdTe device performance. Work elaborated here will first describe establishing a new baseline for the CdTe devices, starting from constructing a deposition system. Adapting the new understanding, the deposition system is later modified to fabricate high efficiency CdTe devices and finally explore the requirements to reach superior performance beyond 25% through numerical simulation.

Chapter 2 contains the details to constructing the new automated closed space sublimation (CSS) system. The chapter also describes the deposition and characterization of the CdTe films using CdS as an n-type layer to obtain a baseline device performance.

Employing the new understanding of reducing the losses and improving the CdTe device performance, Chapter 3 elaborates the methods to incorporate wide bandgap MZO layer replacing CdS. Details to the characterization of MZO films and deposition system reconfiguration is included in this chapter. Finally, high efficiency MZO/CdTe devices fabricated on commercially available SnO_2:F/SnO_2 substrates is presented.

Chapter 4 and 5 presents the work done on improving the photogenerated current. Two chapters show how CdSe is produced by selenization of the CdS films as an alternative to form CdSe films as well enhancing the current generation by reducing the substrate thickness from 3.2 mm to 0.1 mm. Corning Willow © substrates were used for this study.

Following the new understanding of front contact alignment to increase device performance, Chapter 6 elaborates how the front transparent contact (TCO)-emitter alignment impact its device performance for wide bandgap absorbers. Numerical 1D

simulation show the need for TCO-Emitter alignment and use of MZO type wide bandgap emitter to increase FF and overall efficiency of the devices.

Chapter 7 explores how band alignment at the back interface of the device affects device performance. SCAPS 1D simulations done with this study introduces the concept of Initial Fermi Level Offset (IFLO) where positive IFLO coupled with increased doping concentrations in the CdTe could lead to 25% photoconversion efficiency with the currently known material. Applications to real world material is also discussed in this chapter.

Chapter 8 conclude the work in this dissertation with some potential future work that can apply benefit to improve CdTe solar cell device quality.

Chapter 2

Construction of a CdTe Deposition System and Obtaining Baseline Device Performance

Number of deposition methods have been employed to deposit CdTe solar cells and its semiconductor layers such as vapor transport deposition [44-46], magnetron sputtering[24, 47], close space sublimation[19, 48-50], thermal evaporation[51], Electro deposition [52, 53], spray deposition [54]. Chief among the deposition methods, closed space sublimation has been one of the most efficient and successful methods that can be used in a laboratory environment. Majority of this chapter is devoted on the details of constructing a closed space sublimation chamber. While this system is used for majority of the experimental work, this chapter elaborates the construction, characterization and achieving a baseline CdTe device with photoconversion efficiency <13%.

2.1 Closed Space Sublimation

Closed space sublimation (CSS) techniques attractive to researches due to it high deposition rates and ease of fabrication. During sublimation, CdTe exists as a stable binary compound without other phase which allows to deposit high quality material suitable for solar cell absorber. In such deposition systems, source CdTe material is

directly sublimated from material solid phase according to the below sublimation reaction [55].

$$CdTE\ (s) \rightleftharpoons 2Cd\ (g) + Te_2\ (g)$$

In order to achieve a uniform high deposition rate, the CdTe source and the intended substrate is maintained at a close distance (<10 mm). The sublimation of the material depends on several key parameters.

- Distance from the source to the substrate
- Temperature of the source and the substrate material
- Ambient condition: Type of gas and pressure

Growth rate has been shown to have inverse relation with the source to substrate distance due to divergence of the gas species. Work from other researches have been carried out with source to substrate distance varying from 1 to 11 mm[50]. Increasing the source temperature has also shown to increase the CdTe growth rate. Substrate temperature on the other hand, has shown slightly different characteristic, where the growth rate seemed to be constant up to certain substrate temperature and decreases as temperature is increased more due to re-sublimation of material [19, 50]. Growth rate also shows an affect from the ambient gas species in the environment with higher growth rates when Helium is used as the ambient gas compared to Ar and N_2 due to low molecular weight[50, 56]. Finally, increasing the ambient pressure tends to lead to large grain formation as the reduced mean free path of the sublimating species would reduce the density of stable nuclei formed on the substrate surface.

Typical high temperature deposition process like CSS are capable of generating material with larger grain structure that that increases the overall film quality. As the

temperature of the substrate increases, critical radius of forming a stable nuclei increases forming larger grains [57]. Similarly, by reducing the rate the species arrive at the substrate, reduces the density of stable nuclei formation thus increase the grain size.

2.2 Home Built Closed Space Sublimation System

CSS technique has been extensively investigated to deposit CdTe films on to foreign substrates. The coating process essentially is a physical vapor deposition. The substrate and the source are heated up to deposition temperatures ranging 500 °C – 650 °C while maintain the chamber ambient at a high pressure. Once the substrate and source reach the desired temperature, the pressure of the chamber is quickly reduced to allow the sublimation to occur. Due to the temperature difference maintained between the substrate and the source, the locally generated CdTe vapor is condensed on the colder substrate. High pressure back-fill is used to stop the deposition of the material on to the substrate and immediately cooled down. The hardware design of the system was adapted from common CSS system configuration seen illustrated in literature[19]. Figure 2.1 shows a schematic of the constructed system components.

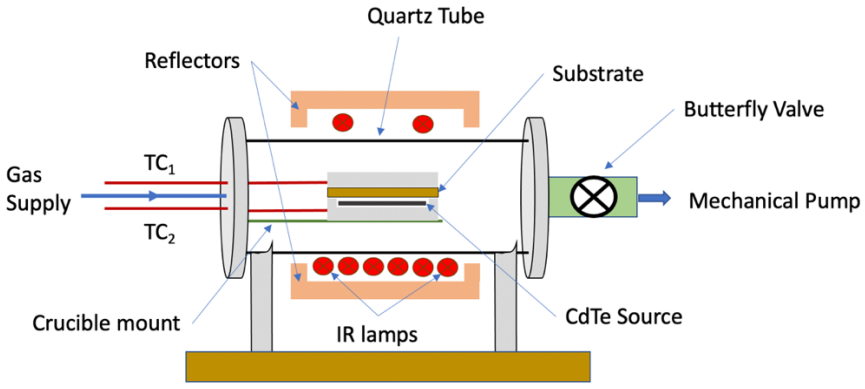

Figure 2.1 Schematic of closed space sublimation system

2.2.1 Hardware Setup

The chamber was constructed with a capability of depositing one sample at a time. A quartz tube was used for the deposition chamber with both ends self-sealing under vacuum. A SiC coated graphite susceptor with a carved pocket (2.75” x 2.75” x 0.25”) was used to hold the substrate, while solid block was used to sandwich the substrate glass between the source susceptor. This source/substrate blocks are placed at the center of the quartz tube. In order to heat the apparatus, 1000W Infra-Red (IR) lamps were used. Electron reflective material was used surrounding the deposition area in order to focus all the IR heat towards to the graphite susceptors. Since both top and bottom susceptors are heated from both top and bottom IR lamps, dimensions of these susceptors and the number of the Infrared lamps heating substrate and source was chosen to accommodate a temperature difference of ~50 °C. The susceptors are designed to hold 3”x3” glass substrates. Type K thermocouple inserted in the susceptors were used to monitor and control the temperature of the substrate and source. Figure 2.2 below is the constructed CSS system labeling all key operational components.

The chamber ambient gas and pressure are controlled by the inlet gas flow and a gas outlet connected to a mechanical pump through a throttle valve. The pressure of the chamber is measured by pressure gauges. The system was set up with a custom gas manifold consisting of pneumatic valves. The operating 24V signal for these valves were individually controlled with a binary signal supplied through a USB Data Acquisition (DAQ) system. These valves are used to feed N_2 gas to control various parts of the CSS system. The system can use up to four different gases with flows varying from 10 sccm to

2000 sccm. An additional N_2 gas connection with 15 psi is fed to the chamber gas line to purge and vent the chamber.

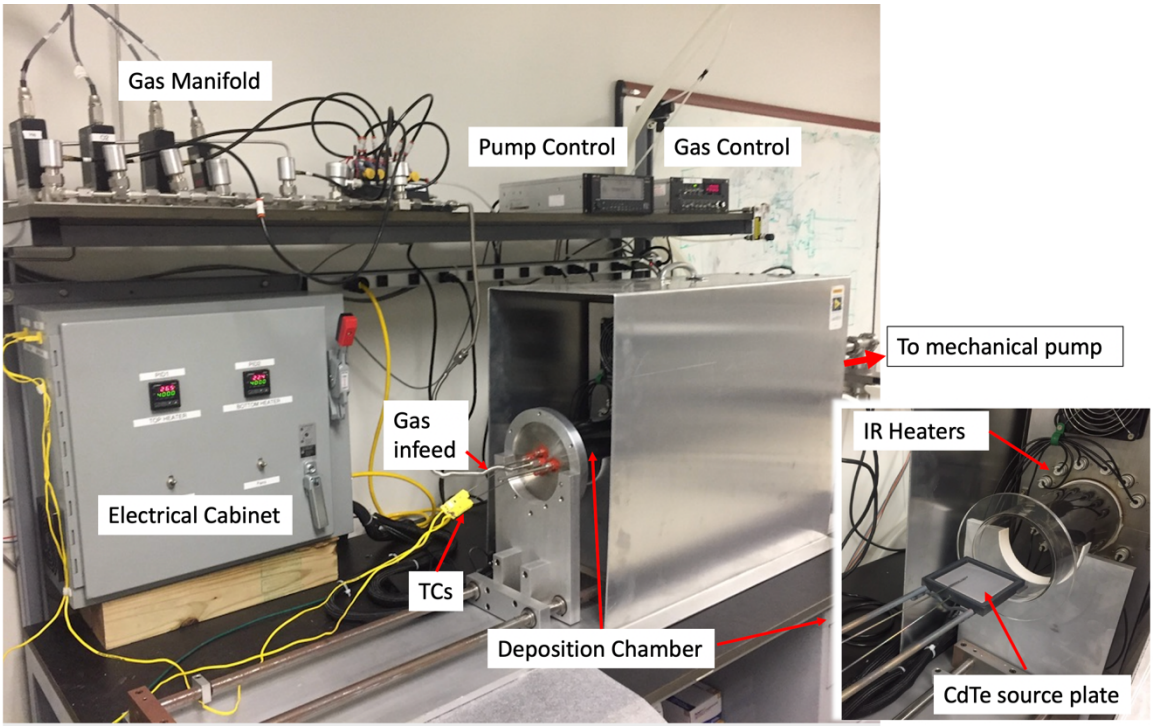

Figure 2.2 Hardware Set up for the newly constructed CSS system.

2.2.2 Automation through LabVIEW

The depositions were controlled using a custom LabVIEW program. The code communicates with all the mass flow controllers, pump controllers, temperature controllers and valves. The program was designed to operate the system in both fully automatic mode to carry out the CdTe deposition for any given set of parameters and manual mode where individual pump, heat and gas flow parameters control individually. The program was also set up to record all data associated with the deposition conditions. Figure 2.3 shows the LabVIEW program interface that enters the key processing inputs and as well as the key processing outputs during a deposition cycle.

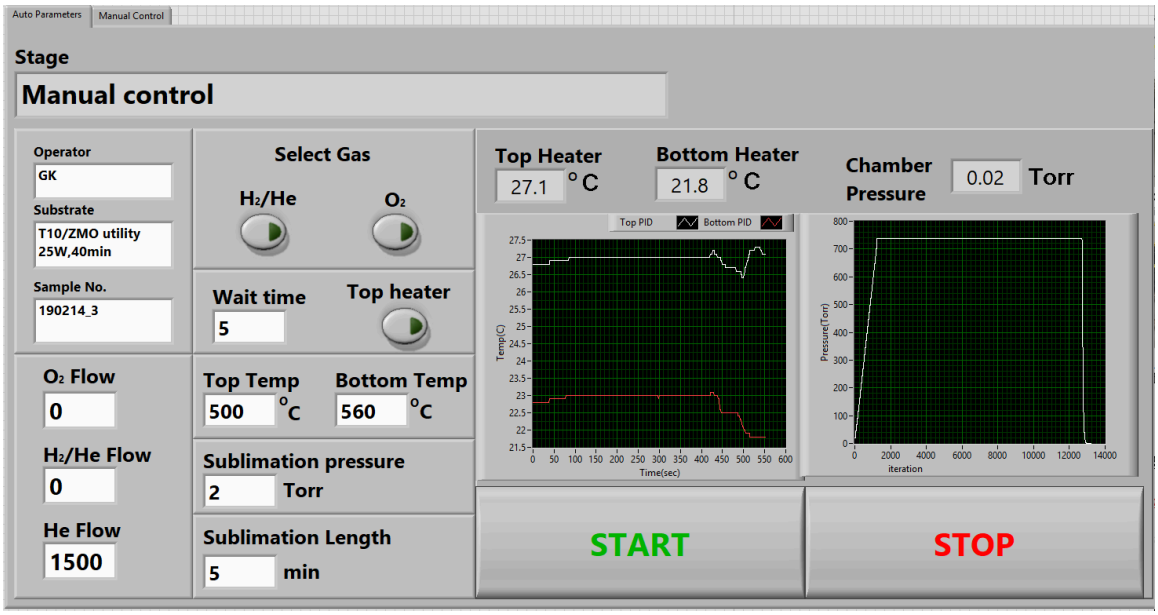

Figure 2.3 LabVIEW program interface controlling the CSS system

2.3 CdTe Device Fabrication using CSS System

2.3.1 Preparation of Source Material

The source material for the chamber was prepared in two different methods. One method is to sinter the high purity CdTe powder (99.999%) by placing it in an empty well of a graphite susceptor and heating up to 660 °C while the chamber pressure was maintained at 5 Torr of helium gas, which was flowing at 1500 sccm. This will be called a source plate from here in text. The second method is by preparing as CdTe source plates was to sublimated as a thick layer (~300 μm) of the high purity CdTe power onto a SiC coated graphite plate. Sublimation is carried out in a more aggressive manner where the source is maintained at 660 °C for ~60 min as opposed to a regular CdTe deposition where its only couple of minutes. Physical appearance to these two types of CdTe sources are shown in the below Figure 2.4.

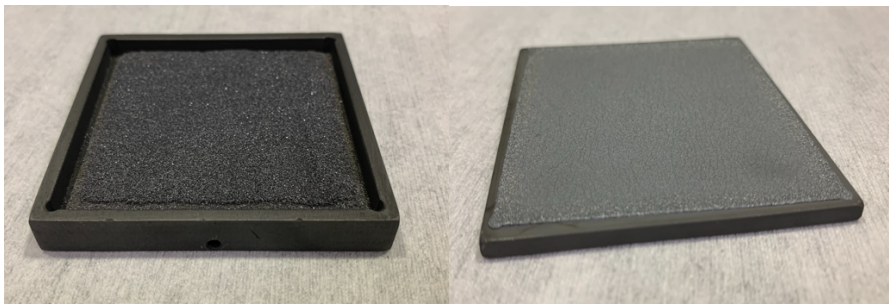

Figure 2.4 Source plates prepared by calcining the high purity CdTe powder (left) and sublimating the CdTe on to graphite susceptor (right).

2.3.2 Sublimation Process

Typically, the sublimation chamber is kept at vacuum when not in use to keep the chamber clean as possible. When in use, the source plate and substrate are loaded into the graphite susceptor and inserted into the chamber. The chamber is pumped down to 150 mTorr and purged with N_2 to 500 Torr. This process is repeated multiple cycles to stabilize the environment, and immediately after completion, the heating sequence begins. The start of the heating sequence also triggers cutting off the N_2 flow and start of the deposition gas of He or a gas mixture of He. Figure 2.5 below illustrates the temperature and pressures for a standard deposition from the system

Both substrate and source are heated rapidly to desired value and allow to stabilize. The start of the deposition begins as the pressure of the chamber is suddenly dropped to desired deposition pressure (typically between 1-100 Torr) and the deposition continues 1-5 mins. To stop the deposition, chamber pressure is rapidly raised back to 500 Torr with N_2 and the heating is turned off. The pressure is actively maintained at 500 Torr until the substrate and source temperature drops below 400 °C. Beyond this temperature, the vapor pressure of CdTe is negligible to have any active deposition[50].

At this point, the butterfly valve was completely closed and the N_2 gas is turned off allowing the source and substrate to cool down. Once both source and substrate temperatures dropped below 70 °C the chamber is vented with N_2 and the sample removed.

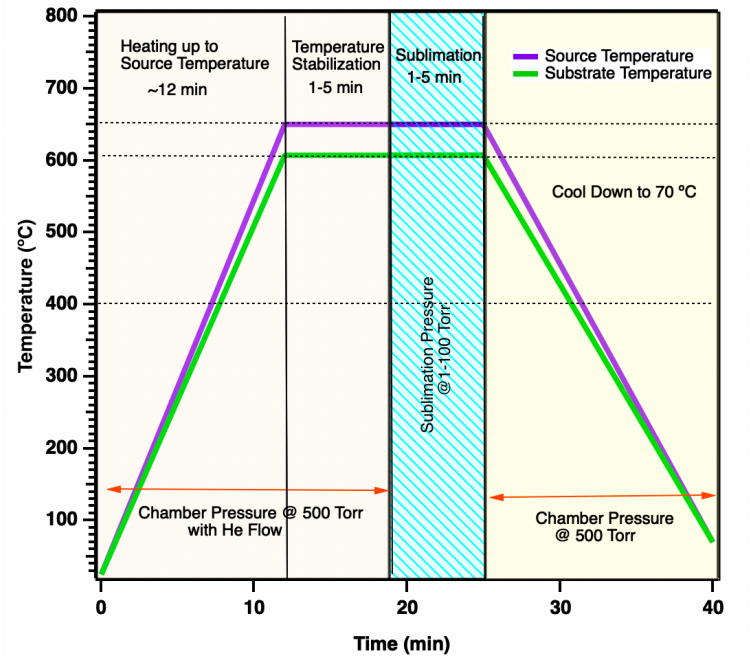

Figure 2.5 Typical temperature profile of a CdTe deposition from the CSS system.

2.3.3 CSS System Characteristics

To obtain the optimum deposition parameters, number of deposition conditions for CdTe absorber growth were tested using both source plate material and sintered CdTe powder source. All depositions were carried out on clean soda lime glass substrates (SLG). Substrate temperature was varied from 550 °C to 620 °C by targeting the bottom susceptor to values 600 °C to 670 °C, maintaining a ~50 °C difference between top and bottom susceptors. Maximum temperature for the substrate was kept at 620 °C to keep the glass substrates below softening point. To identify the affect from ambient to process,

deposition pressure was also varied from 1 Torr to 100 Torr with maintaining 1500 sccm Helium gas flow into the chamber. Duration of the deposition was adjusted to yield a ~3 μm CdTe film.

2.3.4 Effect of Source Temperature on Growth Rate and Morphology

As explained earlier in the text, the source and the substrate temperatures are coupled as the susceptors holding the source and substrate are in contact. Figure 2.6 shows how the CdTe growth rate change with the substrate/source temperature at a deposition pressure of 10 Torr He.

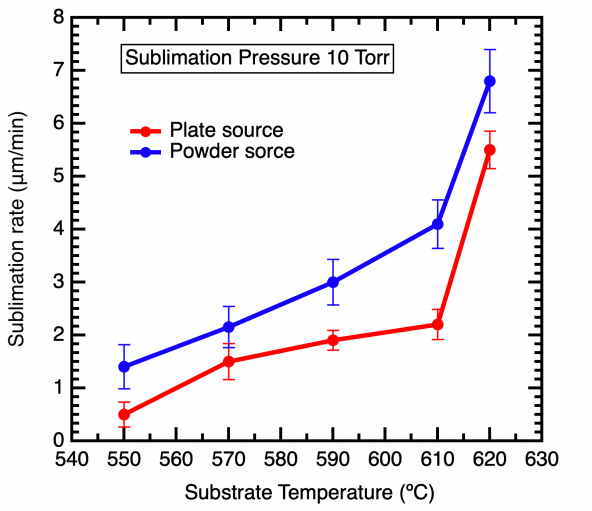

Figure 2.6 Film growth rate for substrate temperature changing from 550 °C to 620 °C when sublimated at 10 Torr for two different types of CdTe sources. Deposition was carried out for 2 min.

As shown in the figure, CdTe growth rate increase as the temperature of the source increases. Note that substrate temperature also proportionally went up as the source temp increased. Similar trend of increasing CdTe deposition rates were observed for both types of CdTe sources, except that with a sintered powdered source, the

deposition rate is lower than that of a source plate. This is most likely due to the lower thermal conductivity in the source material with a sintered powered source compared to a source plate. The uniformity of the surface of the source might also be another factor to the difference is the deposition rates.

Looking at the surface morphology of the films, the effect of source substrate temperature change can be clearly visible. As the scanning electron microscope (SEM) images shown in figure 2.7 shows, the average grain size of the films increased as the temperature of the source increased. The morphology changes align with the previous studies done using similar deposition system[19].

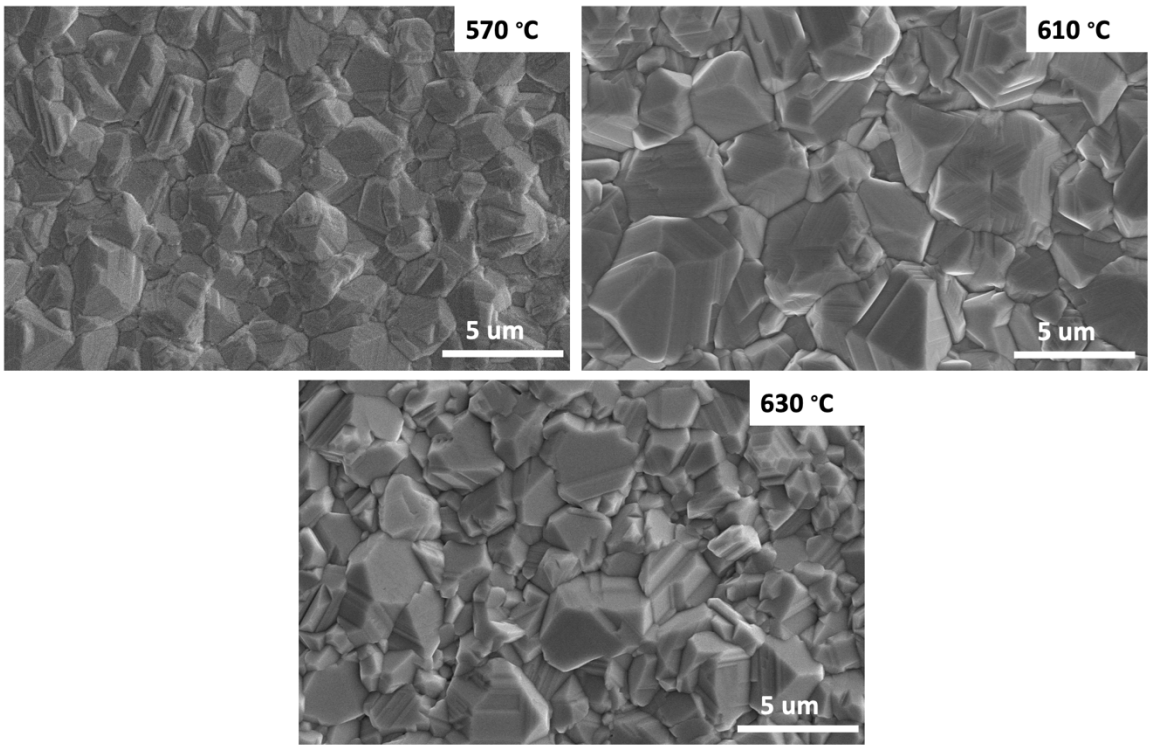

Figure 2.7 SEM Micrographs of CdTe films grown on SLG substrate with 570 °C, 610 °C, and 630 °C substrate temperature with 10 Torr pressure with 1500 sccm Helium gas flow.

2.3.5 Effect of Deposition Pressure on Growth Rate and Morphology

Pressure is another factor that can significantly affect the growth of the film. Sublimating at lower pressure allows the vapor species to easily nucleate on the substrate. When the pressure is increases, the deposition rate should drop. For these films, we observe that at higher pressures the deposition rates are lower (Figure 2.8). Similar behavior was reported other sources where CSS deposition technique was used for the CdTe deposition [19, 50]. For this work, CdTe was sublimated on SLG substrates at a source/substrate temperature of 610 °C and 660 °C respectively.

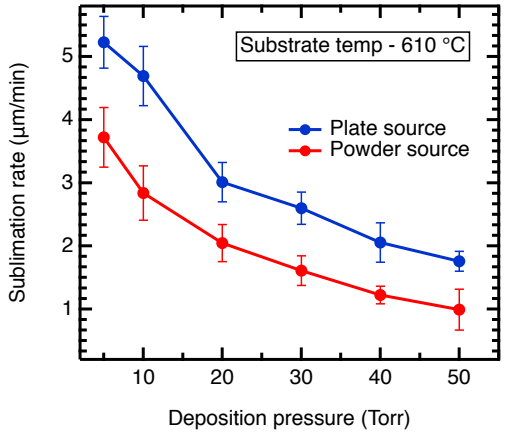

Figure 2.8 Film growth rates when deposition pressures ranging from 1 Torr to 50 Torr. Substrate and source temperature was kept at 610 °C and 660 °C for two different types of CdTe sources and duration of deposition was kept at 3 mins.

With increasing the sublimation pressure, number of small grains on the film increased. This is a very clear signature we see from the SEM micrographs in Figure 2.9. At higher pressure, transfer of CdTe vapor is interfered with increased gas species in the deposition environment, which allows to create additional nucleation instead of allowing

to grow larger grains. This causes the films grown at 1 Torr to have grain structures at the size of ~ 3-5 μm. We also see a variety of small grain sizes at lower pressures, most likely due to the increased deposition rates at low sublimation pressure.

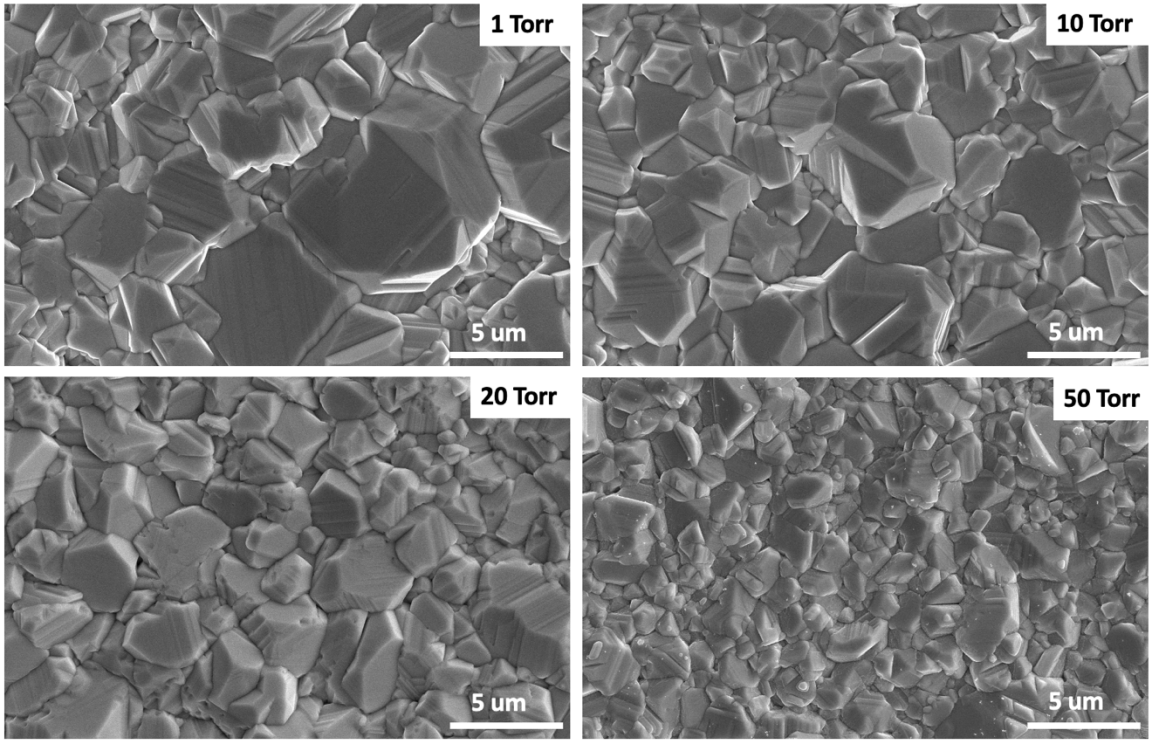

Figure 2.9 SEM images take of CdTe films grown on SLG substrate at sublimation pressures 1 Torr, 5 Torr, 10 Torr, and 50 Torr. Source and substrate temperature was held at 660 °C and 610 °C respectively with 1500 sccm Helium flow maintaining the pressure.

2.3.6 Effect of Oxygen in Ambient Gas

In most cases, adding O_2 during a physical vapor deposition is expected to lead to some reaction with the high energy species. With CdTe growth using CSS, adding some O_2 to the deposition environment is known to help with the material quality and passivation of the grain boundaries of the film[19, 50]. Looking at the deposition rate in

Figure 2.10, any O_2 in the gas mixture resulted a significant drop to the deposition rate. For this study, depositions were carried out at source and substrate temperatures at 660 °C and 610 °C with a sublimation pressure of 1 Torr.

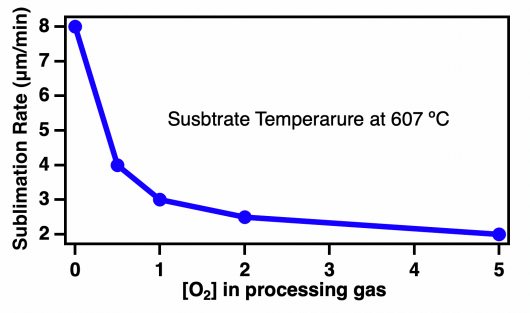

Figure 2.10 CdTe growth rate change with increase oxygen concentration in the processing gas. Oxygen was introduced as a gas mixture of He and CdTe source and substrate temperatures at 660 °C and 610 °C at a sublimation pressure of 1 Torr during deposition.

Films deposited in pure He shows sharp rough edges, while films made with a fraction of O_2 in the ambient resulted much smoother edges. Also, grains are much uniform when O_2 is incorporated (Figure 2.11). One added benefit to this is, with O_2 lowering the deposition rates and creating much uniform grains across, the deposition is more controllable.

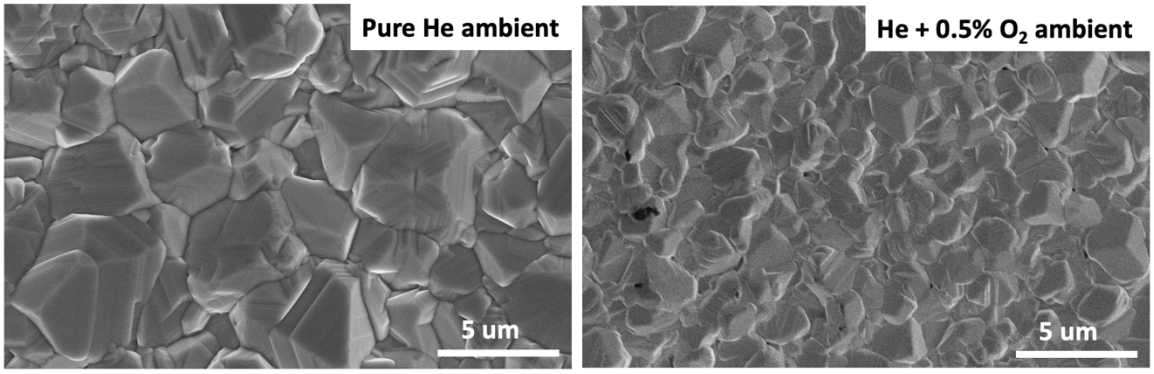

Figure 2.11 SEM images comparing the surface morphology of CdTe films grown on SLG substrates in pure Helium ambient vs gas mixture of 0.5% O2+Helium. The source and substrate temperatures were maintained at 660 °C and 610 °C respectively.

2.4 Fabrication of a Complete CdTe Solar Cell

Complete CdTe device were fabricated to determine the optimum deposition conditions for a high efficiency device. The CdTe solar cells were prepared in superstrate configuration with a film stack as shown in Figure 2.12. The CSS deposition parameters were adjusted to obtain a ~4-5 μm film thickness and devices were completed following the steps detailed in the sections below.

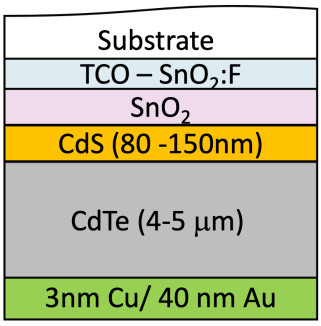

Figure 2.12 Baseline CdTe device structure from CSS system.

2.4.1 Substrate Preparation

Commercially available TEC 15M substrates were used as the substrate material. The substrate consisted of a SnO_2:F conductive layer with thin SnO_2 high resistive transparent layer (HRT). 3”x3” glass substrates were cleaned using diluted Micro-90 in an ultrasonic bath. Finally, the substrate was rinsed in de-ionized water for multiple cycles followed by high pressure N_2 flow to dry.

2.4.2 Semiconductor Layer Deposition

The complete CdTe device was fabricated with a CdS window layer deposited using RF-magnetron sputtering. Following the previous studies [58], ~80 nm CdS layer was deposited on to cleaned TEC 15M substrates at ~250 °C. The power density was maintained at 0.41 W/cm^2 during deposition, and the deposition carried out 15 mTorr chamber pressure with a 23 sccm Ar flow.

CdS deposited samples were transferred to the CSS deposition system immediately after taken out of the sputter system to minimize any contamination from the environment. CdTe depositions were carried out with substrate temperatures varying from 550 °C to 620 °C and for deposition pressures ranging from 1 Torr to 50 Torr. The duration of the deposition was adjusted to have CdTe film thickness of 4-5 μm. Deposition rate is slightly higher when depositing on CdS than on bare SLG.

2.4.3 $CdCl_2$ Heat Treatment

Deposited CdTe stacks were put through a post deposition $CdCl_2$ heat treatment in a system similar to CSS deposition system. For ease of treatment, the original 3”x3” sample was cut in to four equal pieces. This $CdCl_2$ heat treatment acts as an activation step and allows passivation of the CdTe absorber layer and grain growth improving the

performance of the device by increasing photogenerated current and the open circuit voltage[19, 21, 50]. For CdTe devices fabricated using low temperature growth techniques such as sputtering, $CdCl_2$ treat has shown to improve the crystallinity in the films and promote the grain growth[24, 59]. Although similar behavior was not reported for CdTe grown using high temperature deposition process like CSS[19], $CdCl_2$ activation step has shown passivate the grain boundaries due Cl diffusion through the grain boundaries. It has also shown the $CdCl_2$ treatment step promotes the interdiffusion at the CdS/CdTe interface, reducing defects due to lattice mismatch between CdS and CdTe layers[19, 21, 50].

Treatment is typically carried out in dry air (DA). Apart from grain growth and defect passivation from Cl, oxygen in the ambient environment helps to improve the crystalline quality of the CdTe layer. Studies have also showed that, oxygen helps to improve the p-type doping in the CdTe layer via acceptor-like shallow defects [60] [19, 21, 50, 61].

50 uL of saturated solution of $CdCl_2$ in methanol was drop casted on to the film and allowed it to try out. Then the substrate is heat treated at 390 °C for 30 min in a DA flowing environment and allowed to cool down to room temperatures. Excess $CdCl_2$ on the film was rinsed off using methanol and dried by blowing N_2.

2.4.4 Back Contact Processing and Device Completion

$CdCl_2$ treated samples were then transferred to the thermal evaporation system, where 3 nm Cu and 40 nm Au was evaporated on to the film. The device stack was then subjected to a post metal heat treatment at 200 °C for 25 min to allow the Cu to diffuse into the CdTe in order to make a back contact to the cell.

Prepared devices were laser scribed to define the cell area of 0.08 cm^2. In order to make and Ohmic contact to the front contact, Indium paste was used, and the completed devices were measured for current-voltage characteristic under AM 1.5 illumination. Figure 2.13 shows a completed CdTe solar cell.

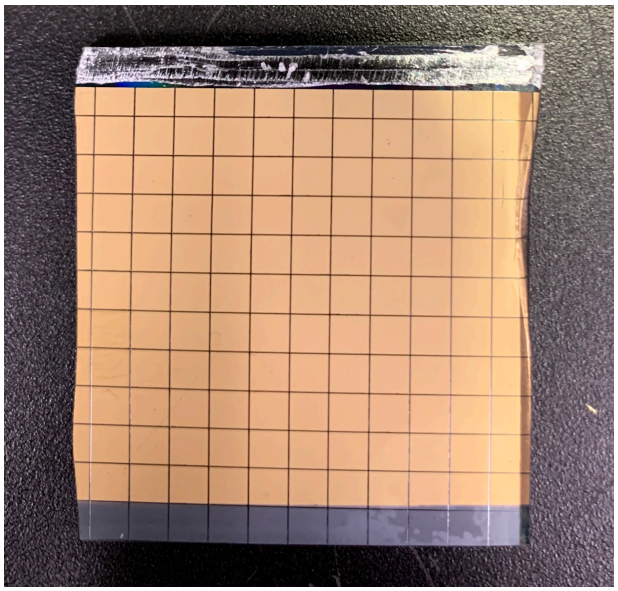

Figure 2.13 Completed CdTe device from CSS system

2.4.5 Baseline Device Performance from CSS System

Ability to grow high quality polycrystalline CdTe films is one of the key factors to high efficacy devices. Completed CdTe devices were fabricated in superstrate configuration in the structure described earlier in the text. With optimization of the device fabrication and post deposition treatments, an average photoconversion efficiency of 13% was achieved as a baseline from the CSS system.

Figure 2.14 shows the device performance of all the devices that were fabricated using the CSS system with a CdS window layer. All these devices were completed with a

$CdCl_2$ activation treatment, a back contact with 3 nm Cu and 40 nm Au followed by a post metal heat treatment. Device were measured under AM 1.5 illumination.

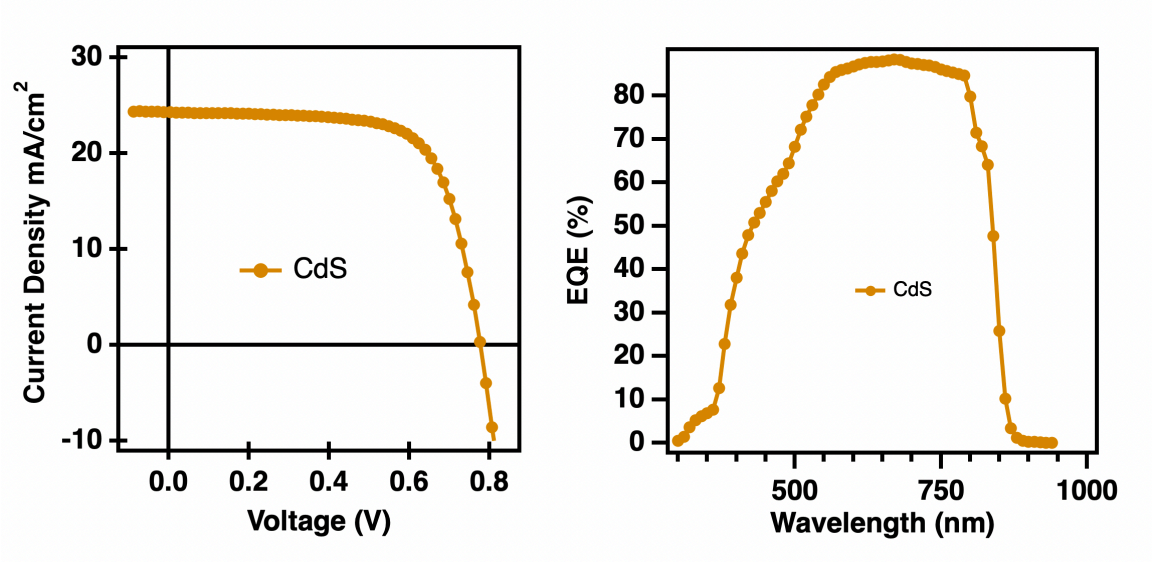

Figure 2.14 Best performing CdS/CdTe device fabricate on TEC 15M substrate. Device comprise of ~80 nm CdS layer deposited suing RF-Sputtering and CdTe layer was deposited at 660°C/610°C for source and substrate temperatures respectively at a deposition pressure of 20 Torr.

Figure 2.14 shows the J-V characteristics and external quantum efficiency (EQE) of the best performing device for the baseline device structure described above. The device shows a photoconversion efficiency of 13.15%, with a V_{OC} of 0.777V, J_{SC} of 23.88 mA/cm^2 and FF of 70.1%. Note the best performing devices for this structure shows lower Voc and FF compared to the devices reported in the literature[19, 50, 62] using similar deposition system. Optimization to the material stack and post processing is needed to improve the performance of the devices and will be described in later chapters in detail as paths to achieving high efficiency CdTe devices.

2.5 Conclusion

A closed space sublimation deposition system was constructed to deposit CdTe material. Equipment was automated using LabVIEW to carry out deposition for given source and substrate temperatures and sublimation pressure. Equipment characteristics were carried out to obtain high quality CdTe material. Upon characterization, completed CdTe solar cell devices were constructed on commercially available SnO_2:F substrates (TEC15M) with an ~80 nm CdS layer as the window layer. A number of parameters were tested out to fabricate baseline CdTe devices with an average photoconversion efficiency of 13% with the highest efficiency of 13.15%. Performance of the devices are below that of devices fabricate using similar type of systems reported in literature, and the improvements performance of these devices will be described in the coming chapters of this dissertation. There also will be discussions to improve the device performance of the baseline devices with increasing the current collection and open circuit voltage using alternative n-type window layer.

Chapter 3

Fabrication of High Efficiency CdTe solar cells via Closed Space Sublimation

The previous chapter described the construction of a new CSS deposition system and obtaining baseline device performance of 13%. The devices were constructed on a commercially available substrate with a SnO_2:F with a thin high resistive transparent layer of SnO_2 with a thin CdS window layer. This chapter focus on improvements to the device performance of the baseline device with state-of-the-art advancements to the CdTe device architecture. The original design to the constructed CSS deposition chamber was modified to fit the needs in improving high quality CdTe absorber layer and post processing options.

3.1 Introduction

Recent advancements to the CdTe solar cells show significant improvements to the short circuit current density (J_{SC}) and the open circuit voltage (V_{OC})[37, 39, 63-65]. A majority of these advancements are due to improved current collection in the long and short wavelength regions. Conventional understanding of the CdTe solar cell depicts a formation of a p-n junction that governs the performance of the device. While this is still valid, recent understanding of the device physics make us realize what is missing and

finding solutions to reduce the losses that impedes the device performance. A solar cell consists of an absorber with multiple contacts lined up to efficiently extract photogenerated carriers. As mentioned in the Chapter 1, the collected current in the solar cell can simply be put in as total photocurrent generated current minus the photocurrent recombined before extraction.

$$J = J_{generated} - J_{Recombined} = J_{Ph} - J_{Front} - J_{Bulk} - J_{Back} \quad (1.11)$$

Improving the photogenerated carriers, while reducing the detrimental recombination effects could significantly improve the device performance in CdTe devices.

3.1.1 Incorporating a Wide Bandgap Oxide as a Window/Emitter layer: Increase J_{Ph} and reduce J_{Front}

To improve the current collection in the CdTe devices, deviation from the conventional device structure is needed. As shown in Figure 1.9 from Ablekim *et al*.[39], if the conventional CdS layer was replaced with a suitable wide bandgap semiconductor like Magnesium Zinc Oxide (MZO), the additional current gain from the blue light is significant [32, 33, 39, 65].

In addition to the J_{SC} gain from blue light, numerical simulations have highlighted a tremendous V_{OC} gain reaching up to 1V from such window layer [39], by suppressing the front contact recombination with appropriate band (CB) alignment at the interface. Studies have attributed this performance gain to the band bending of CdTe at the emitter – CdTe interface due to creating a so-called CB "spike" (CB of emitter above CB of CdTe)[31, 32, 66], depriving holes and reducing the interface recombination. While the latter part is true, fundamentally, the reason for the band bending comes from the alignment of the Fermi levels in the materials. In n-

type doped material, if there is no change to the doping level, the Fermi energy level coupled with the CB edge and any change to the CB should result the Fermi level have the same effect. When the emitter is changed from a CB "Cliff" (CB of emitter below CB of CdTe) to form a CB "spike", the Fermi energy is driven up with the same amount. At equilibrium, this introduces more band bending to the CdTe bands, driving more holes from the interface. This reduces the front interface recombination, significantly improving the V_{OC} and FF of the device. While changing the CB to tune the emitter Fermi level is beneficial up to some extent, continuing to increase the height of the "spike" eventually would act as a barrier for the electrons to transfer to the front contact. Carefully tuning the CB location of the emitter is needed.

Lot of attention has been given to fabricate CdTe devices using Wide bandgap emitter material like MZO. While most not always successful, with proper processing conditions research groups have demonstrated expected benefits to V_{OC} and FF with MZO/CdTe device structure reaching PCE 18% and beyond [33, 67].

3.2 Wide Bandgap $Mg_xZn_{1-x}O$ (MZO) as an Emitter

Following these work, wide band gap MZO was incorporated as the emitter layer for the CdTe devices. The goal was to determine the optimum MZO properties using a range of compositions, starting from ZnO. Typical ZnO film has an electron affinity more negative compared to CdS[68], resulting conduction band minimum much lower with respect to CdTe. With a Fermi level in an unfavorable location, ZnO would induce much less band bending to CdTe bands at the ZnO-CdTe interface. This device will have much hole concentration at the front interface, limiting the device performance due to high recombination currents at the front interface.

Alloying MgO with ZnO is known to increase the bandgap of the material mainly through rise of CB, reducing the electron affinity of the material [31, 69, 70]. The bandgap in the alloy change according to,

$$E_g(x) \cong 3.3\ eV + 2.0x\ eV \quad (3.1)$$

,where x is the fraction of Mg in MZO and E_g is the resulting bandgap of the material. With CB rising, the Fermi level of the material should also increase, if there is no change to the doping concentration. Here, the change in the bandgap (or CB in this case) can also be used as a proxy to obtain the correct Fermi level alignments between the emitter and CdTe.

With this intent, we varied the Mg concentration in the film to obtain different bandgap MZO, hence different CB location in the emitter. For uniform deposition, RF-magnetron sputtering was used with home-made sputter targets with known Mg and Zn wt%. By using the equation 3.1, you can carefully choose your Mg concentration needed to obtain a specific bandgap.

3.2.1 MZO Target Preparation

MZO sputter targets were prepared in-house. MgO (99.99%, Sigma Aldrich) and Zn (99.9%, Alfa Aesar) powder was mixed in a roll mixer with different Mg:Zn ratios to obtain five different material compositions that would result in five different band gaps varying from 3.3 eV (pure Zn target) and 3.7 eV ($Zn_{0.8}Mg_{0.2}O$). The well mixed powder was then cold pressed into 2” sputter targets using a home-built die set. A 20 Ton force was applied for 30 min and the pressed pallet was transferred to the sputtering gun with a 2” Copper base plate for better contact. Figure 3.1 is showing a prepared target used for the MZO film deposition.

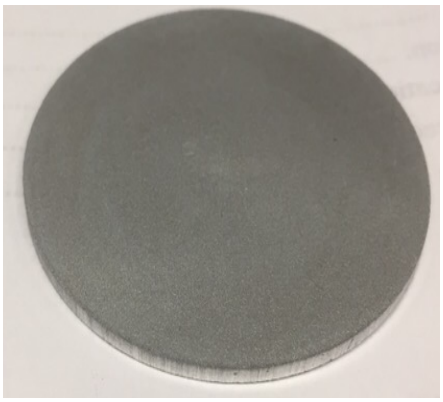

Figure 3.1 Inhouse prepared 2" diameter $Mg_xZn_{1-x}O$ target with bandgap estimating 3.6 eV.

3.2.2 RF- Sputtered MZO Film Characterization

Targets were broken in by sputtering for 1 hr at 10 mTorr deposition pressure with 5% O_2 mixed with argon. O_2 was required in the deposition as the targets contained mostly metal-Zn, and the optimum amount of O_2 in the gas mixture was determined by varying the gas mixture up to a point to obtain transparent films. The deposition power density was maintained at 0.616 Wcm^{-2}. Following the break-in of the newly pressed target, deposition was carried out on SLG substrate with all five different targets. The total deposition time was adjusted to deposit 300 nm MZO films, as the deposition rate decreased with the increasing Mg content in the target.

3.2.2.1 Bandgap Extrapolation of Deposited MZO Films

Transmission of the deposited films were measured using Perkin-Elmer Lambda 1050 spectrophotometer and bandgap values were extrapolated using the tauc plot method. Figure 3.2 shows the band gaps calculated from each of the MZO targets deposited on to the SLG substrates. It can be clearly seen that the band gap widens as the

amount on Mg increased. The extrapolated bandgap in the films matches the expected bandgap E_g derived from equation 3.1 based on the x value in $Mg_xZn_{1-x}O$.[32]

$$E_g = 3.3\ eV + 2.00x \qquad (3.1)$$

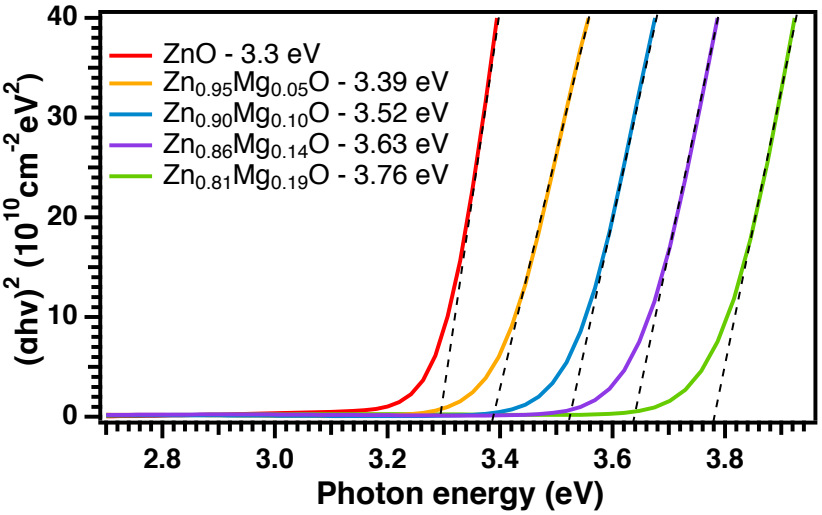

Figure 3.2 Bandgap extracted using the transmission spectra obtained from films sputtered at room temperature on to the 1 mm soda lime glass substrates.

It was hard to obtain a clear X-Ray diffraction pattern with thinner films deposited on amorphous SLG substrate. In order to validate the crystal structure, a MZO film with $Mg_{0.14}Zn_{0.86}O$ composition (most commonly used MZO composition for CdTe device fabrication) was used. Figure 3.3 shows the X-ray diffraction pattern obtained for a 1 µm film deposited on a commercially available TEC 15 (SnO_2:F) substrate at room temperature.

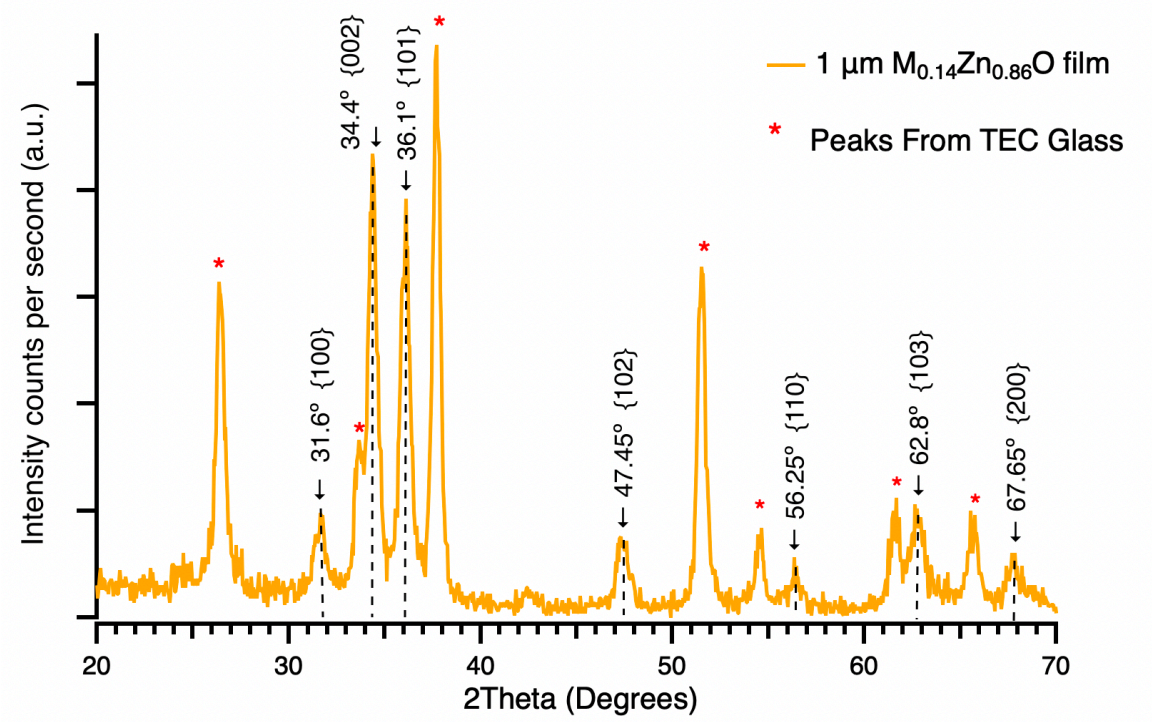

Figure 3.3 X-ray diffraction pattern of 1µm thick $Mg_{0.14}Zn_{0.86}O$ films deposited on TEC15 commercial substrate.

Even with the diffraction peak from underlying SnO2 peaks, deposited MZO film with bandgap ~3.63 eV shows clear diffraction peaks from hexagonal Wurtzite crystal structure as expected for this material. While dominating features of (002) and (101) plane diffractions are clearly visible in the spectrum, additional weekly diffracting attributes from (100), (102), (110), (103), and (200) are recognizable. Most likely, these features exist due to low temperature deposition conditions.

From this spectrum, the lattice constant, *c*, calculates to be 5.176 Å which is expected from incorporation of Mg into the lattice[71]. However, the lattice parameter *a* in the close-packing direction, seems to be slightly higher than that of ZnO, likely due to

the lattice strain in the film due to the difference in ionic radii of Mg2+ and Zn2+ ions and to the fact of thick MZO layer sputtered at room temperature[32, 71, 72]. Diffraction peaks from the TCO layer is also clearly visible, but these peaks have been excluded from the analysis. While Figure 3.3 only representing single MZO composition, collaborative studies done at University of Toledo,[73] shows that dominating (002) peaks shifts towards higher diffraction angles with increasing Mg content due to decrease in lattice parameters from Mg atoms substituting Zn atoms in the lattice.

3.3 Baseline Device Performance with MZO/CdTe Structure

Complete CdTe devices were constructed using the MZO as the window layer. For these devices, the CdS window layer has been replaced with ~80 nm of the different compositions of MZO layer sputtered onto commercially available SnO_2:F substrates. The CdTe deposition parameters were adjusted to grow 3 μm CdTe layer. In order to grow high quality pin hole free CdTe films, substrate the temperature was maintained at 550 °C while maintaining the source temperature at 600 °C. The deposition was carried out at 5 Torr sublimation pressure with flowing Helium gas (99.999%).

3.3.1 Device Performance with Varying MZO Bandgap

TEC15/MZO/CdTe devices were $CdCl_2$ treated by drop casting 50 uL saturated $CdCl_2$ in methanol and heat treating at 390 °C for 30 min. Treatment was carried out in a heat chamber with 5 ft^3/h dry air flow. These devices were finished with a thermally evaporated 3 nm Copper (Cu) and 40 nm Gold (Au) back contact followed by a post-metal-heat-treatment (PMHT) at 200 °C for 20 min. Figure 3.4 shows the current density-voltage (J-V) curves of the devices fabricated.

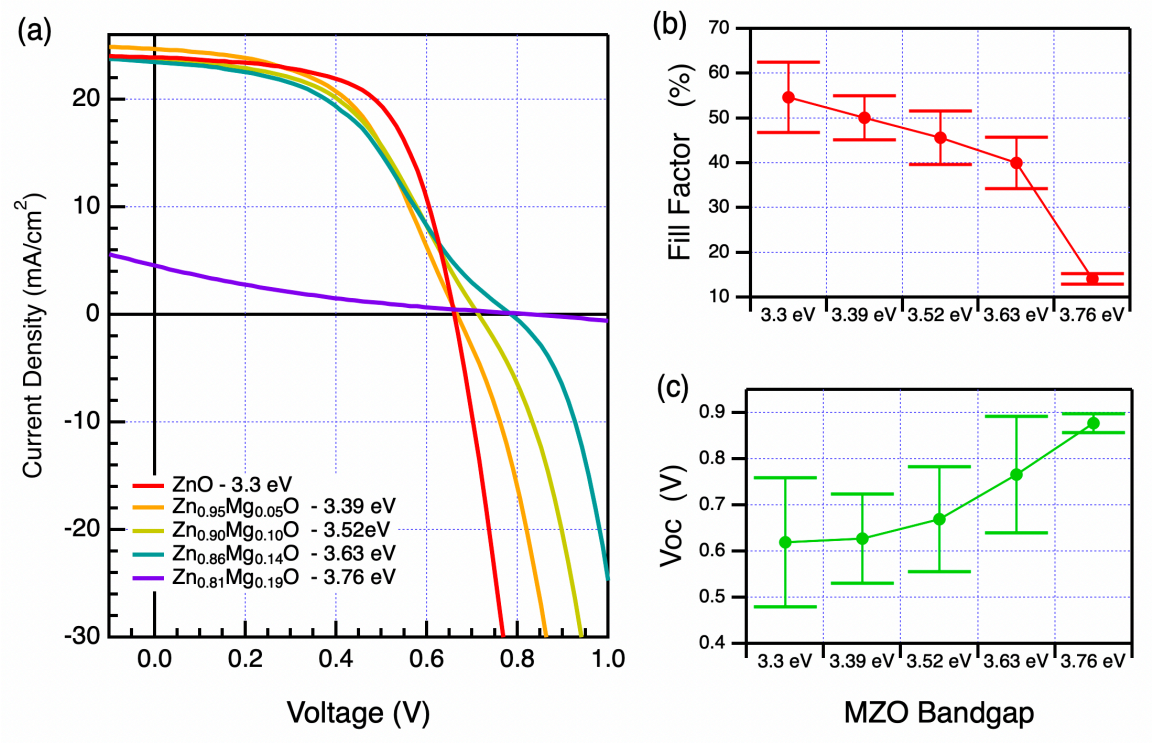

Figure 3.4 (a) J-V curve of the devices fabricated with different composition of the MZO bandgaps. Plots adjacent show the drop in (b) Fill Factor while the (c) V_{OC} increase with increasing the MZO bandgap.

For devices fabricated with ZnO emitter layer shows low Voc, but as the MZO layer bandgap widens with addition of Mg, the V_{OC} of the devices started to increase, reaching ~0.9V for the bandgap of 3.76 eV ZMO. On the other hand, FF of these device takes a drastic drop with increasing MZO bandgap, in a larger proportion than in crease in VOC. Looking at the J-V curves, a larger "S-kink" is formed as Mg is incorporated the emitter and gets worse with higher Mg content. What is striking is that, even for MZO bandgap 3.39 eV, where MZO CB is expected to be below that of CdTe forming a "cliff", an S-kink is evident. On another note, the J-V curve for most commonly used MZO

composition ($Mg_{0.2}Zn_{0.8}O$ with 3.76 eV) shows almost no current flow at short circuit, indicating a detrimental barrier to the charge flow in the device.

This phenomenon has been a common signature among many CdTe researches starting to use MZO. Devices exhibit low FF when MZO was used alone for the devices and regardless of the poor band alignment at the CdTe front interface, most groups have been forced to use a thin layer of CdS to maintain the performance, keeping MZO just as a high resistive transparent layer[74-76].

3.3.2 MZO Carrier Density vs Performance: 1D Numerical Modeling

To better understand the poor performance in these devices with MZO/CdTe, 1D SCAPS simulations were carried. Figure 3.5 shows the trends to the performance (Efficiency, V_{OC}, and FF) with respect to the CB offset between the MZO/CdTe interface and the doping concentration of the MZO layer. Here, the CB offset was varied by simultaneously changing the MZO layer bandgap and the electron affinity.

For negative CB offset between MZO/CdTe, Efficiency is driven by the changes to V_{OC}. Contour plot in Figure 3.5(c) shows that for MZO doping density below 10^{17} cm^{-3}, V_{OC} of the devices are getting impacted as the CB offset between MZO/CdTe turns to negative, with severe effects seen when the CB offset falls below -0.1 eV. Region with higher doping densities in MZO ($>10^{18}$ cm^{-3}) and negative CB offset seemed to less impact for V_{OC}, most likely slightly higher Fermi level in MZO still aids to create enough band bending in CdTe bands, reducing the interface recombination. While some V_{OC} gain may be observed in simulation, in reality, achieving such high donor concentrations ($>10^{18}$ cm^{-3}) in a MZO like oxides have proven to be difficult without additional impurity

dopants[71, 77]. V_{OC} plot also suggests that, as the CB offset becomes positive, V_{OC} improves.

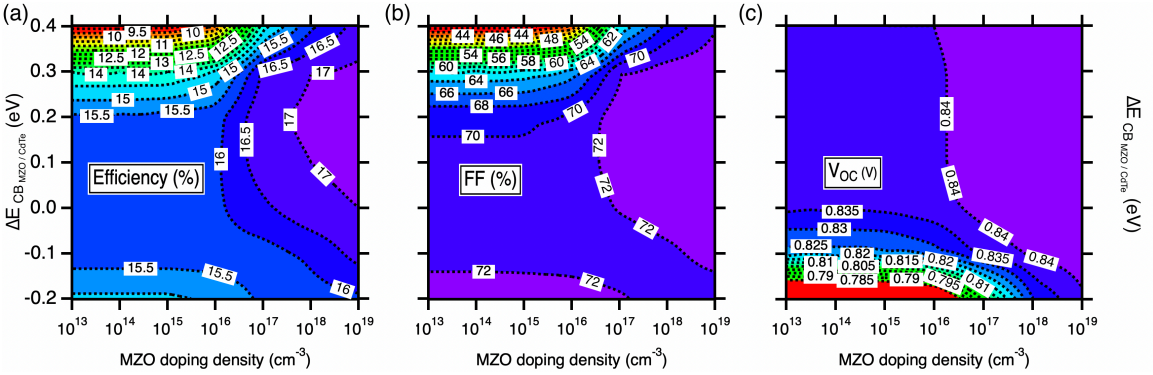

Figure 3.5 Simulated (a) Efficiency, (b) Fill factor, and (c) V_{OC} trends in MZO/CdTe devices at different CB offset values with varying MZO doping concentration. These devices were assumed to have 2ns bulk lifetime with mid-gap defect states at the interface and in the CdTe bulk.

With positive CB offsets, driver for Efficiency changes to FF. And the MZO doping density plays a key role in controlling FF, hence in overall efficiency. When the CB offset it negative, impact to FF seemed to negligible, but as the CB offset becomes positive, the FF drastically drops for MZO doping densities $<10^{17}$ cm^{-3}. While the absolute values for FF is not 1:1 match to with the simulations done here, the behavior of the FF drop is similar to what we have seen with the fabricated devices described in section 3.3.1. This suggest that, devices fabricated in the lab was largely impacted by the MZO doping density.

Looking at the band diagram for same device stack with two different carrier concentrations at 0.8 V (Figure 3.6), the device with an MZO with high carrier

concentration shows greater band bending in the CdTe near the front interface. With higher doping, the Fermi level of the MZO is much closer to the CB edge and would result a flat electron quasi-Fermi level through both the emitter and absorber. The case is different for devices with low carrier concentrations, where there the gap between the MZO CB edge and the Fermi level is larger. For the same bias voltage as with higher doping, electron quasi-Fermi level shows a barrier to electron flow in to MZO suggesting that photocurrent collection is impeded. This would explain the drop in the FF with moving the MZO bandgap at low carrier concentrations seen in Figure 3.5(b).

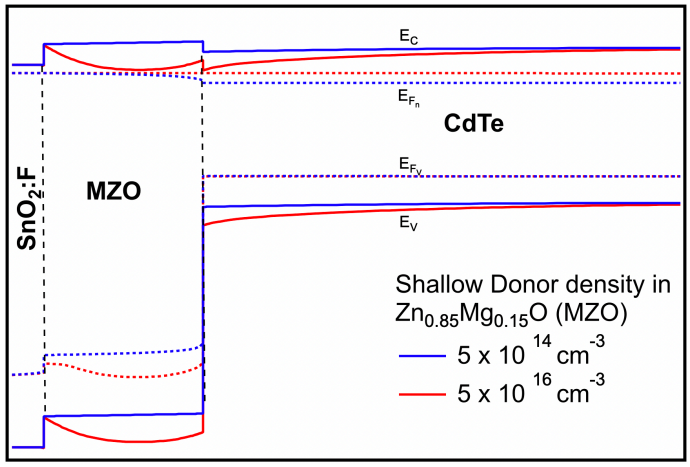

Figure 3.6 Simulated energy band diagram of MZO/CdTe device with two different donor densities in MZO layer. Values were obtained at 0.8 V under simulated AM 1.5 illumination.

While the practical capabilities were limited to measure the actual doping densities for the MZO layer fabricated in section 3.3.1, results from the simulation here clearly suggests that MZO doping density played a key role to the poor devices performance. With low doping concentrations in MZO, a large barrier to the electron transport would form and become worse as the MZO bandgap is increased. When the

doping concentration in MZO is increased, Fermi level sits much closer to CB edge, creating much less barrier to the electron flow from CdTe to front contact.

3.4 High Efficiency MZO/CdTe Films: Improving Carrier Concentration in MZO Layer & Improved Cu doping in CdTe

The n-type doping in ZnO, and its Mg-alloys comes mainly due to the oxygen vacancies[78]. It has been shown that during sputtering of ZnO and its alloys, the O_2 fraction in the sputter ambient can significantly impact the n-type doping and can even completely transformed to p-type doping, if sputtered in an environment with O_2 fraction> 50%.[79] Literature also shows that, as the Mg content in MZO increases beyond 35%, it's become difficult to maintain the intrinsic doping levels and more susceptible to varying doping concentrations in the film[79, 80]. With cold pressed mixed targets using Zn and MgO sputtered at 5% O_2 to maintain quality transparent of the films, alternative approaches are needed to increase the n-type doping in MZO films and reduce O_2 interaction at different stages in CdTe device processing.

3.4.1 Modifications to CdTe Deposition System

In order to reduce the O_2 in the deposition environment, the close spaced sublimation (CSS) system was modified. In addition to the mechanical pump system, turbo pump was added to the bring the system to higher vacuum.

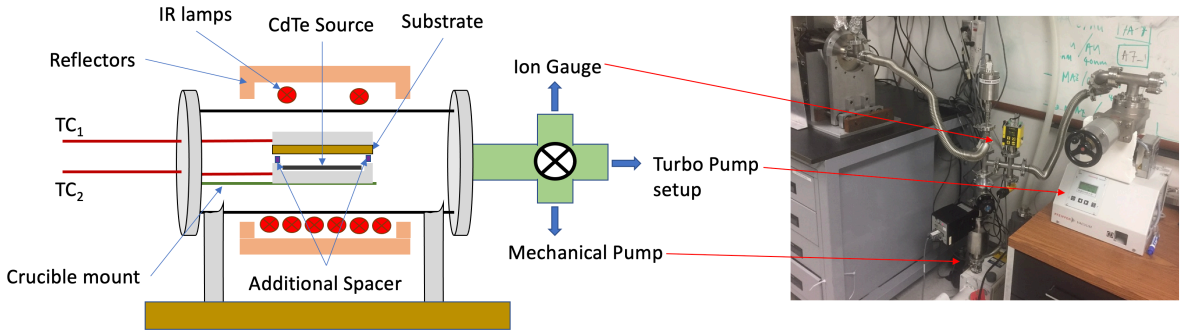

Figure 3.7 Schematic and snapshot of the modifications to the CSS system to reduce O_2 from the deposition ambient.

The gas manifold in the chamber was reconfigured to reach a base pressure of $1x10^{-7}$ Torr. Other than for loading the sample, the chamber was kept under vacuum. Previously, the crucible mount was set up to holding the source and the substrate in contact, and the temperature for both source and substrate was coupled and was not able to individually control. For better individual control and isolation of the source and the substrate, an additional 3 mm quartz spacer was added between the source and the substrate.

3.4.2 Additional Pre-heating Step to MZO Layer

In addition to this hardware and the software changes, additional heat treatment (referred as HT in the text hereafter) step was employed to the MZO layer pre-CdTe deposition. The aim is to induce more oxygen vacancies (V_O) in the MZO layer through thermal processing to promote n-type doping in MZO films. Assuming there is no Mg or Zn loss, the generation of the V_O in $Mg_xZn_{1-x}O$-like compounds can be written as,

$$Mg_xZn_{1-x}O = Mg_xZn_{1-x}V_O^{2+} + \frac{1}{2}O_2 + 2e^- \quad (3.11)$$

Apart from this, additional HT may result in better crystallinity and the MZO layer. Kuru and Narsat[81] showed a HT step up for MZO films would promote the optical and electrical properties of the film. As the films are processed in an ambient with less O_2 increases probability of generating more V_O as it depends on the partial pressure of the O_2[82].

To perform the HT prior to the CdTe deposition, MZO coated substrates were introduced to the modified chamber, and pumped down to 10^{-7} Torr and held for 30 mins. The automated deposition program was reconfigured with an additional heating step prior to CdTe deposition. Figure 3.8 shows the new temperature profile of the chamber after modifications.

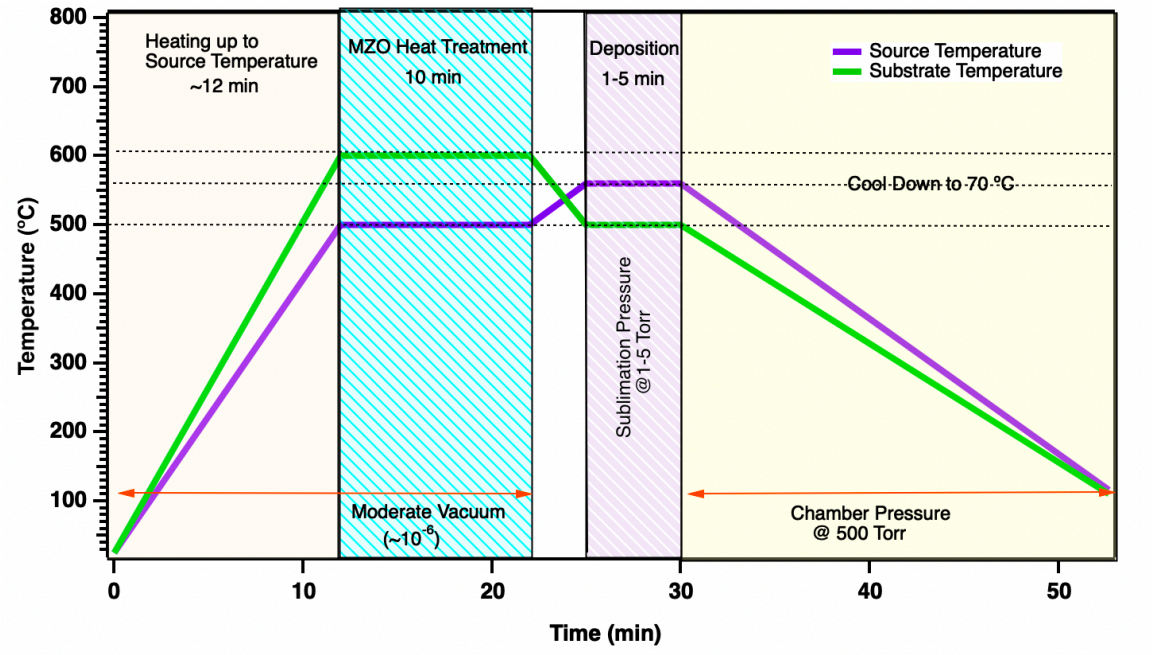

Figure 3.8 Modified CSS deposition profile for MZO/CdTe devices.

During the MZO HT, the substrate and source temperatures were maintained at 600 °C and 500 °C, respectively, in order to avoid any unwanted CdTe deposition on to

the substrate. After the HT for the MZO layer, Helium was introduced to the chamber to bring the ambient pressure up and simultaneously dropping the substrate temperature to 500 °C while increasing the source temperature to 560 °C. Deposition was carried out at 1-5 Torr and the duration of the deposition was adjusted to obtain 3 μm CdTe layer.

3.4.2.1 Effect of Heat Treatment on MZO: Film Composition

Upon investigating the composition, Auger depth profiles do not show any signs of Mg or Zn loss due to the HT MZO of the films prepared on TEC substrates. For simplicity, MZO with a bandgap of 3.64 eV was used and HT for different durations. Figure 3.9 shows Auger depth profiles obtained from Auger electron spectroscopy (Perkin-Elmer PHI600), comparing the Mg:Zn ratios. HT was carried out at 600 °C for 10, 20, 40 min on three different MZO thicknesses. Compositional profile suggests that the HT did not cause any changes to the Mg:Zn even HT duration up to 40 min.

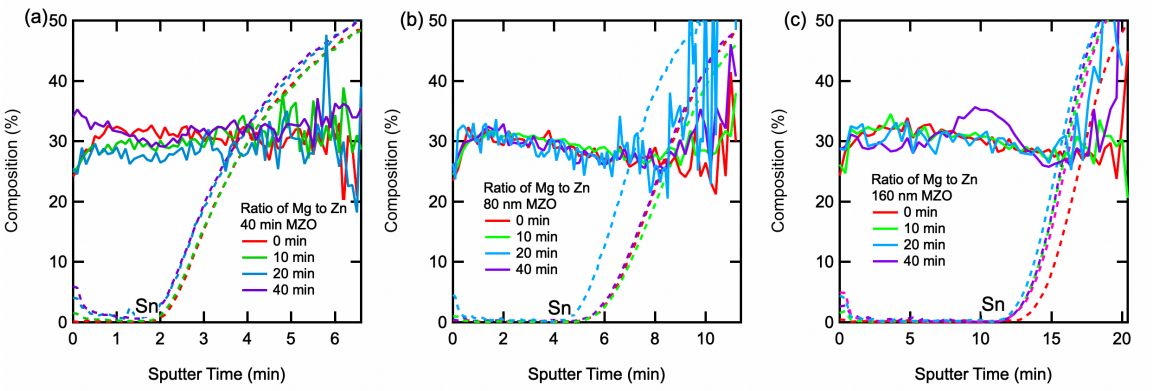

Figure 3.9 Auger depth profiles for MZO films with thicknesses (a) 40 nm, (b) 80 nm, and (c) 160 nm heat treated at 0, 10, 20, and 40 min at 600 °C under vacuum.

3.4.2.2 Effect of Heat Treatment on MZO: Crystal Structure

To test for any changes to crystalline structure in the MZO films, XRD patterns were obtain. Following similar method done for as deposited film, 1 μm thick MZO film deposited on TEC 15 substrate was used to obtain clear diffraction patten. The MZO film consisted with a bandgap of 3.64 eV and had been HT at 600 °C for 40 mins. Figure 3.10 shows the comparative XRD patterns for the as deposited and HT MZO films.

Both XRD patterns contains clear signatures from the underlying SnO_2 layer from the substrate, as marked in the figure. It's important to note that relative intensities from the diffraction peaks from SnO_2 are similar for both as deposited and HT films. Both as deposited and HT MZO films show strong orientation in hexagonal crystal system. One of sticking changes to notice is the reduction in the (101) diffraction peak at 36.1° and increase intensity of (002) diffraction peak at 34.4°, film has become more crystalline and strongly oriented in (002) direction due to HT. The resulted film also shows reduction in the weakly diffraction features from (110), (103), (200) and (102) compared to as deposited film due to increased crystallinity. Absence of any diffraction signatures from Mg^{2+} or MgO suggest the theory of no Mg or Zn loss, supporting the claim observed with Auger profile.

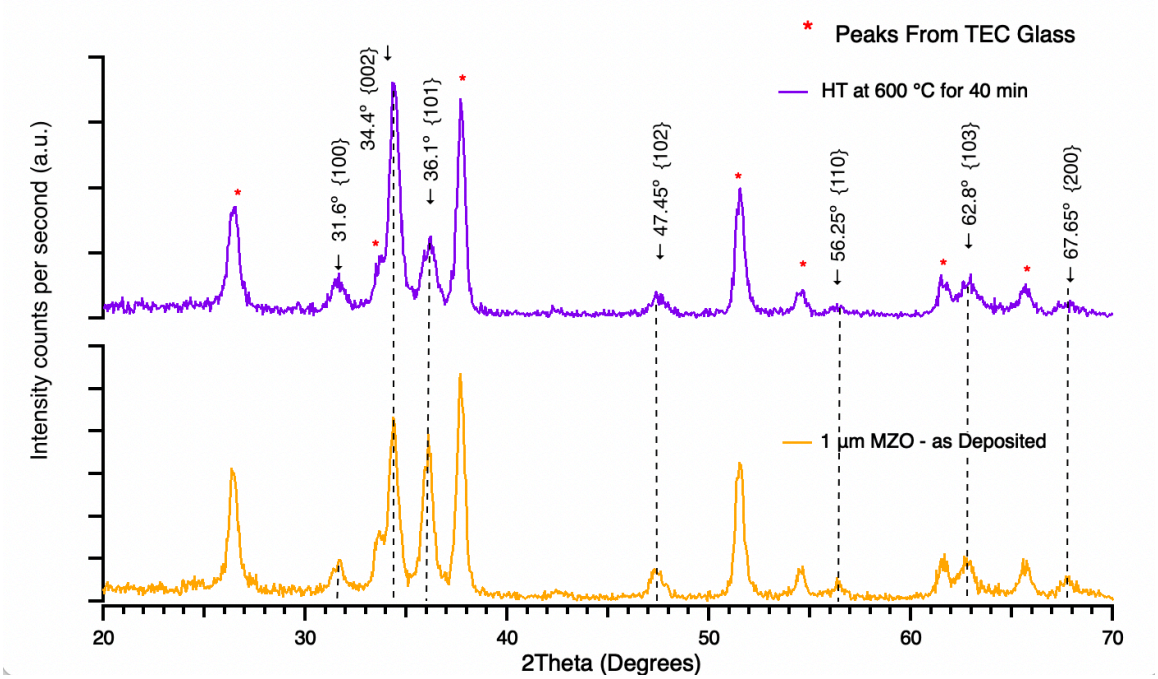

Figure 3.10 Comparison of X-ray diffraction patterns of 1µm thick $Mg_{0.14}Zn_{0.86}O$ films (3.64 eV) on TEC15 substrate, before and after putting through heat treatment at 600 °C for 40 min.

3.4.3 Oxygen Free $CdCl_2$ Treatment

Studies have shown how the oxygen in $CdCl_2$ heat treatment environment can penetrated almost ~3 µm CdTe interacting with the window layer[83]. This is beneficial to conventional CdS based CdTe device. However, having oxygen during $CdCl_2$ treatment would significantly affect the doping density in the MZO film. Interaction with O_2 significantly lower the O_2 vacancies in MZO, lowering the effecting doping concentration. Similar results have been published through collaborative effort from UT-PVIC, where the importance of O_2 free processing of the MZO/CdTe films to eliminate the S-kink issue[65].

$CdCl_2$ treatment was performed in an oxygen free chamber similar to CdTe deposition system in section 3.4.1. To ensure the chamber is free from oxygen, a turbo-pump stack was used to obtain a base pressure of 10^{-6} Torr prior to the treatment. 100 μL of saturated $CdCl_2$ solution in anhydrous methanol (99.99%) was applied by drop casting, and the sample was treated in N_2 flowing environment. Samples were heated to 420 °C and treatment was carried out for 20 min.

Without oxygen in treatment ambient, this treatment method does not have the same benefit as a traditional $CdCl_2$ treatment where oxygen would help to passivate the defects. Therefore, slightly aggressive heat treatment was employed in order to aid the recrystallization process. Having MZO allow for more aggressive $CdCl_2$ treatments compared to CdS/CdTe devices. Excess CdCl2 was removed with a methanol rinse and used for back contact processing.

3.4.4 Back Contact Processing

Incorporation of Cu for CdTe device processing has been of the key factors to obtain good device performance. Though with degrading effects, Cu is historically known to improve carried concentration at the CdTe back surface and reduce the barrier for the hole transportation. Many approaches have been used to add Cu to CdTe back contact processing, Cu_xTe[20], Cu doped ZnTe[84], Te/Cu[85] although, careful control of the amount added has been a challenge.

Recently Li et al.[86] showed wet chemical method to incorporate Cu for back contact processing and achieving high efficiency device performance for ZMO/CdTe devices. Using cuprous chloride (CuCl) as the source of Cu needed for back contact, and use of a rapid thermal annealing process, the group showed a better control of supplying

the needed Cu for the device. Studies done on CdTe back contact processing have also shown high temperature post treatment to be beneficial to form Cu_xTe like complexes that helps to reduce the back contact barrier and improve device performance.[20, 85]

Adapting this work, CuCl was used to facilitate needed Cu. By controlling the concentration dissolved in anhydrous ethanol and controlling the amount added for the treatment, the amount of Cu introduced was controlled. 50 uL of 5 mmol/L CuCl was added to the sample via spin-coating followed by heat treatment at 220 °C for 12 mins in an oxygen free atmosphere. The treatment chamber was purged with 5 scfm N2 flow to ensure the chamber environment if oxygen free and the treatment was carried out with 5 scfh flow.

3.5 Device Performance with Improved Fabrication/Processing Conditions to MZO/CdTe

Deploying modifications discussed earlier, CdTe devices were fabricated with MZO/CdTe. Devices were $CdCl_2$ treated in an oxygen free environment followed by the CuCl back contact processing. With these improvements, the s-kink seen in the earlier devices was suppressed and significant improvement to the FF and J_{SC} was observed in the devices. In addition to this, high temperature CuCl treatment has significantly aided to improve the V_{OC} compared to the devices fabricated using the CSS system.

With further optimization of these process parameters, a highest PCE of 16.1% was observed with a Voc of 0.861 V and J_{SC} of 25.47 mA/cm^2 and FF of 73.1%. Above figure 3.11 shows the best performing device produced from the from the CSS system with MZO/CdTe during my work. Here, the through processing, the optimum MZO layer thickness was found to be ~80 nm with HT of 20 min at 600 °C.

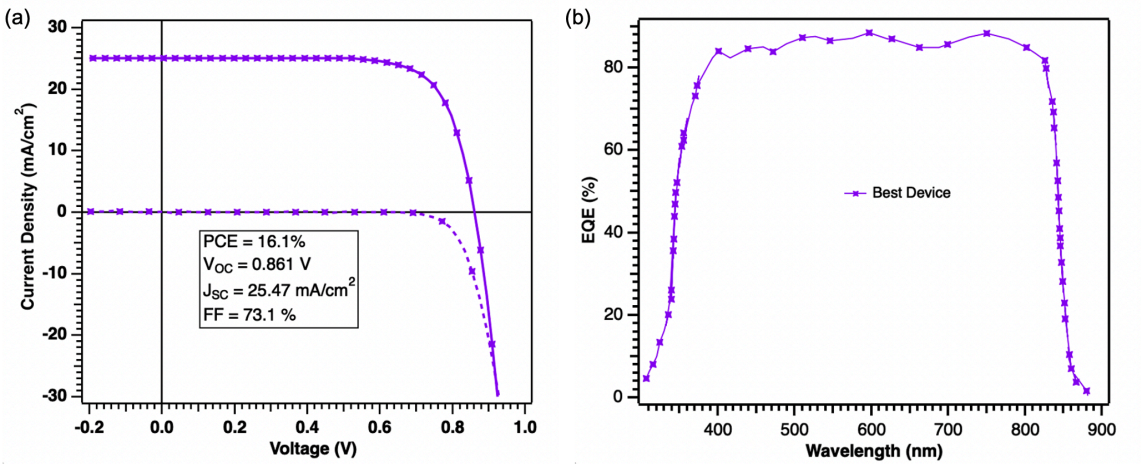

Figure 3.11 (a) J-V curve and (b) EQE of the best performing device with MZO/CdTe. 80MZO layer is 80 nm thick and was put through HT for 20 min at 600 °C. $CdCl_2$ treatment for the device was done in an O_2 free environment and device was finished with CuCl back contact processing with Au back electrode.

3.6 Conclusion

This chapter discuss the step-by-step evolution to the fabricating high efficiency CdTe device using wide bandgap MZO emitter layer. Initial devices show a large s-kink in the J-V curve from poor front contact alignment between MZO/CdTe interface due to low doping concentration in MZO layer. Modifications were made to convert the CSS system to a high vacuum evaporation system with an additional heat treatment step prior to CdTe deposition to improve the n-type doping in the MZO films. Coupled with this, oxygen was eliminated from the post processing environment to preserve high electrical conductivity in the MZO layer. With these modifications, an MZO/CdTe device with 16% was achieved.

Chapter 4

RF-Sputtered Cadmium Stannate for Flexible Glass CdTe Solar Cells

As mentioned in the earlier text, keys to improving the performance of CdTe is by increase the photocurrent generation while reducing the loss mechanism in the photovoltaic cell. While the work described in this chapter pre-dates the improved understanding to produce high performing CdTe devices, concept will help to gain an additional benefit to photo-current generation through improving incident light to the device. The study focus using thinner substrate to increased transparency in front contact. An ultra-thin Corning® Willow® substrate was used with cadmium stannate (CTO) transparent conducting oxide (TCO) to fabricate CdTe devices.

The complete device stack consisted with traditional CdS emitter material as a benefit of thermally processing of CTO via proximity annealing method described in literature [12, 87]. Substrate/CTO/CdS stack was thermally processed using closed space sublimation system to obtain desired optical and electrical properties and fabricate CdTe devices with photoconversion efficiency of 14.4%. The results in this chapter have been published in Liyanage et al., 2016 [88], © IEEE. Printed with permission, from Geethika K. Liyanage, Corey R. Grice, Adam B. Phillips, Zhaoning Song, Suneth C. Watthage, Nichholas D. Franzer, Sean Garner, Yanfa Yan, and Michael J. Heben, RF-sputtered Cd2SnO4 for

flexible glass CdTe solar cells, 2016 IEEE 43rd Photovoltaic Specialist Conference (PVSC), and June. 2016.

4.1 Introduction

Transparent conducting oxides (TCOs) are electrically conductive materials with low absorption of visible and near infra-red (NIR) light. Besides commonly used materials such as fluorine doped tin oxide, indium tin oxide, and aluminum-doped zinc oxide, cadmium stannate (CTO) is of interest due to excellent compatibility with CdTe device processing [17]. The low resistivity (~1.5 $\times 10^{-4}$ Ω-cm) [12] of CTO arises from the high mobility (up to 100 $cm^2/V\text{-}s$) [89] and high carrier concentration (~10^{20} cm^{-3}). The high transmission (>85%) across the visible and NIR portions of the optical spectrum is due to relatively low free carrier absorption and a wide band gap.

Studies show that RF-sputtering typically results in the best quality CTO films for implementation in photovoltaic (PV) devices [17, 90, 91]. However, as-deposited CTO films are amorphous and highly resistive. A high temperature post-deposition annealing at 600 - 660 °C with the sample covered with either a CdS-coated or a bare piece of glass (i.e. “contact annealing”) [17, 87, 89-91] is often required to promote crystallization and develop high conductivity and transparency. This high temperature treatment limits the commercial deployment of CTO. Here we investigate the application of an alternative route [17] for processing amorphous RF-sputtered CTO films into high performance TCOs for PV devices. The approach uses the thermal energy of the CSS process, avoids a separate high temperature annealing step, and can be applied to fabrication of PV devices on flexible glass substrates. Recently, CdTe devices constructed on fluorine

doped tin oxide coated flexible Corning® Willow® Glass substrates yielded solar to electric power conversion efficiencies as large as 16.4%[48]. The use of CTO as the transparent conducting material may allow the power conversion efficiency to be pushed to higher values.

4.2 Experimental Details

CTO films were deposited by RF-sputtering using a 2-inch diameter target prepared in-house. CdO (Sigma-Aldrich, 99.5%) and SnO_2 (Sigma-Aldrich, 99.99%) powders were mixed in a molar ratio of 2:1 and calcined at 1100 °C for 6 h [90]. The resulting powder was ground with a mortar and pestle and pressed into sputter targets using 12 tons of force for 20 - 30 minutes at room temperature. CTO films were sputtered at 50 W for 1 h on 3.0 mm thick soda lime glass (SLG), 1.1 mm thick aluminum borosilicate glass (ABSG), and 0.2 mm thick Corning® Willow® Glass substrates, each heated to 300 °C. The chamber was dynamically pumped to maintain a pressure of 10 mTorr while Ar/O_2 mixtures were introduced at a flow rate of 30 sccm. Energy dispersive x-ray spectroscopy (EDS) was used to determine the stoichiometry of the film. The film thicknesses were determined by cross sectional imaging using a Hitachi S-4800 UHR-Scanning Electron Microscope.

Device stacks consisted of the CTO film, ~100 nm of RF-sputtered intrinsic zinc oxide (i-ZnO) as a high resistivity transparent layer (HRT), ~85 nm of RF-sputtered CdS:O, and 4 - 5 μm of CSS CdTe. The CdS:O was deposited by RF-magnetron sputtering (50 W, 10 mTorr) at room temperature. Oxygen was incorporated by flowing 2 vol% O_2 in Ar at 40 sccm. CdTe thin films with thicknesses of 4 – 5 μm were grown in

0.5 vol% O_2 in He at 50 mTorr in a homebuilt CSS system. The source and substrate temperatures were 660 °C and ~607 °C, respectively [19]. As-grown CdTe films were treated with $CdCl_2$ at 387 °C for 30 min in dry air. After removing the excess $CdCl_2$ by rinsing with methanol, 3 nm of Cu and 40 nm of Au were sequentially deposited by thermal evaporation without a vacuum break. Device stacks were finished by heating at 150 °C in air for 45 min. The prepared devices were laser scribed to define a cell area of 0.08 cm^2. Current-Voltage (J-V) characteristics were measured under simulated AM1.5 illumination.

To investigate the optical properties of the CTO layer after device fabrication by CSS deposition, the CdTe and CdS layers were removed from the best performing devices made on SLG by soaking (10 min) in a solution that was prepared by mixing 10.0 g citric acid monohydrate (Sigma Aldrich, 99%) and 10 ml of 6% H_2O_2 in 90 ml of deionized water. CTO films with and without i-ZnO were also processed through the CSS temperature profile without deposition of either CdS or CdTe to investigate how the presence of the HRT layer affected the CTO film. Additionally, samples were prepared by contact annealing using a bare piece of ABSG glass to cover the CTO samples while annealing at 600 °C - 660 °C for 30 min in air. The optical transmittance of the films was measured using a Perkin-Elmer Lambda 1050 spectrophotometer. Electron mobility and carrier density were measured using an MMR Technologies Hall measurement system. Contacts for Hall studies were made using indium. X-ray diffraction (XRD) patterns were obtained using a Rigaku Ultima III X-ray diffractometer.

4.3 Device Fabrication on CTO Films: Results and Discussion

4.3.1 CdTe Devices Prepared on Soda Lime Substrates

In order to develop a process for Corning® Willow® Glass, initial optimization work was done on SLG. To study the effect of oxygen during sputtering, CTO films were sputtered onto SLG at different oxygen partial pressures. When CTO was deposited in a pure Ar environment, the films were found to be Cd poor by EDS. As the O_2 pressure was increased, the composition also increased toward the ideal 2:1 (Cd:Sn) ratio and became constant for O_2 partial pressures of 20% and above. The sputtering rate of CTO, though, decreased as the O_2 pressure increased.

To determine how the stoichiometry of the CTO film affects the device performance, sputtered CdTe devices were prepared following our previous work[92] on CTO films deposited using O_2 partial pressures ranging from 0% to 50%. Performances of these devices are shown in Figure 4.1.

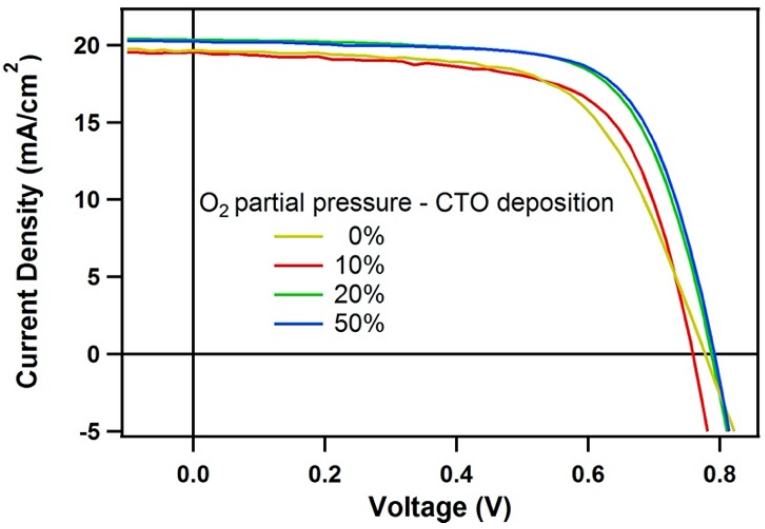

Figure 4.1 J-V curves of sputtered CdTe devices prepared on CTO films on SLG that were deposited with different O_2 partial pressure.

The thickness of the CTO layer in these films was held constant at ~300 nm, and the films underwent the high temperature contact annealing before additional semiconductor layers were deposited. The performance of the devices improved as the O_2 content increased from 0% to 20%. Higher oxygen contents yielded no additional improvement. The poor performance (low fill factor and V_{OC}) of devices made on CTO deposited at less than 20% O_2 is attributed to nonstoichiometric composition in the CTO layer. The V_{OC} and fill factor values improved as the partial pressure of the O_2 in CTO deposition increased to 20%, at which point, the power conversion efficiencies was greater than 11% under AM 1.5 illumination.

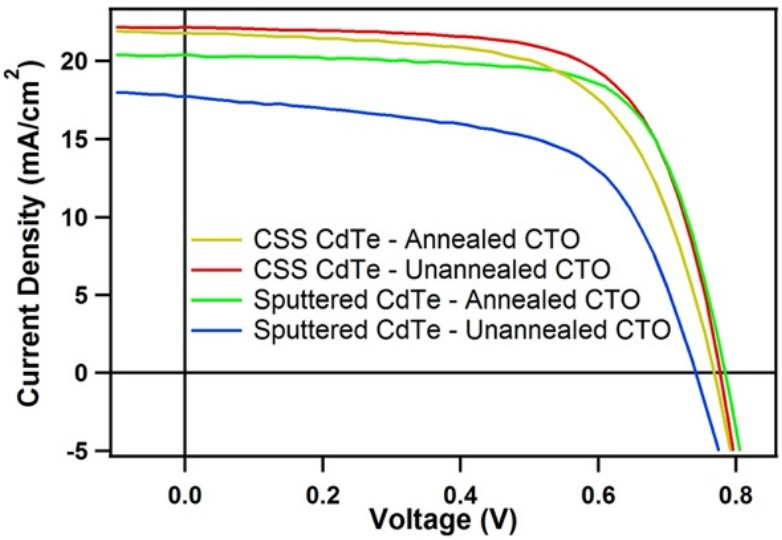

Figure 4.2 J-V curves of CdTe devices prepared by CSS and sputtering on SLG Glass, with and without contact annealing. The CTO layers were deposited in a 20% O_2 environment.

To study the effect of the CSS process on the CTO layer, CdTe was deposited at high temperature on CTO films prepared at 20% O_2 partial pressure. One CTO film underwent the high temperature contact annealing step before CdTe deposition while the other did not. The temperature excursion during CSS deposition consisted of a ramp to ~607 °C over ~10 min and a hold at that temperature for ~7 min. Figure 4.2 and Table I compare the J-V curves and device parameters for both CSS and sputtered CdTe devices prepared on CTO/SLG.

Sputtered CdTe devices prepared on unannealed CTO showed poor device performance, as expected. Apart from the lower current density due to the reduced thickness of the sputtered CdTe layer (4-5 μm versus 2.1 μm), devices from both CdTe deposition methods prepared on heat-treated CTO showed similar J-V characteristics. In comparison, the CdTe device prepared by CSS on the unannealed CTO also demonstrated high performance. The high efficiency of the CSS CdTe on the unannealed CTO is a clear indication that the use of a high temperature deposition technique can directly produce high performance CTO without an additional heat treatment. Interestingly, Grazing Incident-XRD measurements show that even the highly conductive CTO layers have poor crystallinity.

Table 4.1: Comparison of CSS and Sputtered CdTe Devices Prepared on SLG

Device	V_{OC} (V)	J_{SC} (mA/cm^2)	FF (%)	Eff. (%)
CSS CdTe - annealed CTO	0.769	21.9	64.2	10.8
CSS CdTe - unannealed CTO	0.778	22.2	67.8	11.7
Sputtered CdTe - annealed CTO	0.784	20.4	70.0	11.2
Sputtered - unannealed CTO	0.742	16.3	58.7	7.1

4.3.2 Changes to Optical Properties with Thermal Processing

To explore the changes in the optical properties of the CTO after the CSS CdTe deposition, we stripped the devices to the CTO layer and measured the optical transmittance of the films. In addition, to investigate the effect of the HRT layer, CTO films with and without i-ZnO were processed through the CSS temperature profile without deposition of either CdS or CdTe. These measurements were compared to the data for the as-deposited and contact annealed films and are shown in Figure 4.3.

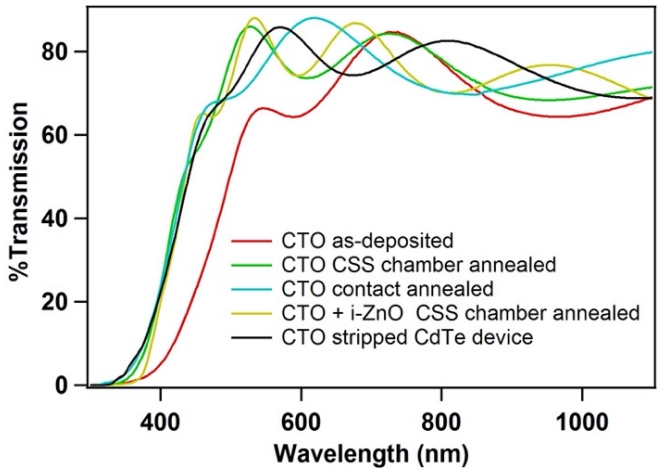

Figure 4.3 Optical transmittance of CTO films on SLG substrates.

As-deposited CTO films showed poor transmittance across the visible and near IR portions of the spectrum, and an optical band gap of ~2.8 eV, which is less than expected for crystalline CTO [3-5]. The changes to the transparency is also clear visible that as

deposited films show yellowish color and the thermal processing transform them to more transparent films (Figure 4.4). The CSS process dramatically increased the transparency of the films and increased the optical band gap to ~3.5 eV. A similar change in the band gap was observed when contact annealing was used.

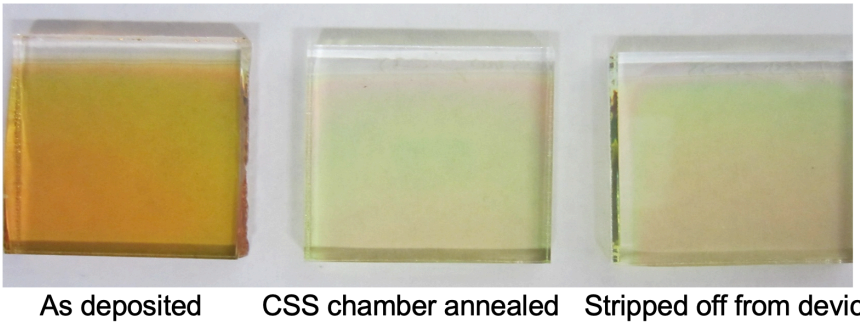

Figure 4.4 Physical appearance of the CTO films at different processing conditions.

Significant improvements were also observed in the electrical properties. Table 4.2 shows the band gap, sheet resistance, mobility, and carrier concentration for CTO samples deposited with 20% O_2. As-deposited films were highly resistive with low mobility and low carrier concentration of 12.7 $cm^2/V\text{-}s$ and 3.28 x 10^{18} cm^{-3}, respectively. After the CSS process, these values increased to ~50 $cm^2/V\text{-}s$ and ~10^{20} cm^{-3}. Similar improvements in the electrical properties were observed after contact annealing of CTO films, which is consistent with observations by others[17, 87, 89-91].

4.3.3 Role of i-ZnO (HRT) Layer

Results in Figure 4.3 and Table 4.2 show that high temperature deposition of CdTe improves the optical and electrical properties of the as-deposited films. Previous studies concluded that the CTO layer had to be covered to prevent Cd loss during the high temperature annealing [87, 91].

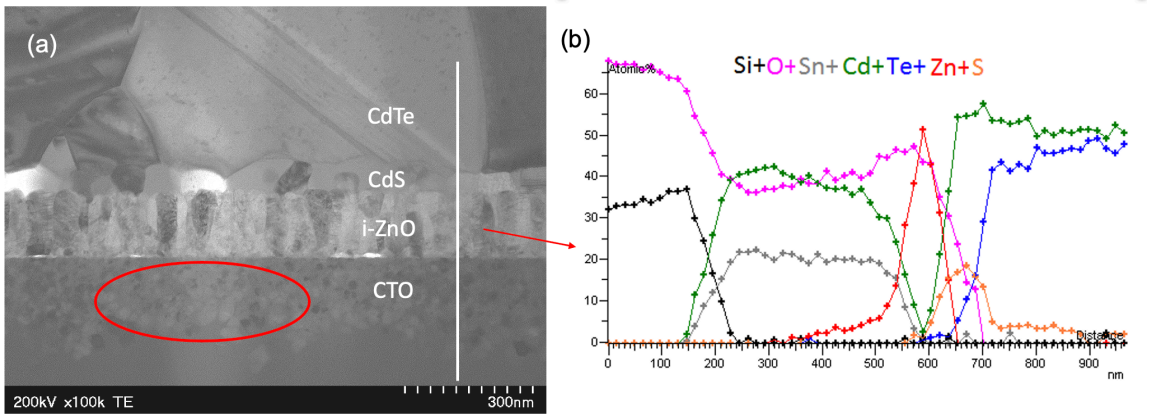

Figure 4.5 (a) STEM image and (b) STEM EDS compositional line profile of a complete CdTe device prepared by CSS on CTO/i-ZnO/CdS:O stack.

Table 4.2 shows that even a thin HRT layer can play this role. While the optical improvements for CTO with and without i-ZnO are similar after experiencing the CSS temperature profile, the sheet resistance for the CTO film annealed with i-ZnO was 20% lower than that of the film without i-ZnO. High resolution Scanning Transmission Electron Microscopic (STEM) images shown in Figure 4.5 shows increased crystallinity in the CTO layer and compositional line scan across the stack shows, signs of diffuse Zn into the CTO layer. Correlated to these findings, the CTO from the stripped device shows significantly better electrical properties than those of any other film. Diffusion of Zn and during the thermal processing may have helped significantly to improves the CTO film quality at thermal processing as a device.

Table 4.2: Electrical Properties of CTO Films on SLG

CTO ~300 nm	Bandgap (eV)	R_{sheet} (Ω/□)	Mobility (cm^2/V-s)	Carrier Conc. (cm^{-3})
As deposited	2.95	1896	12.7	3.3×10^{18}
Contact annealed	3.66	23.4	33.5	9.8×10^{19}
CSS chamber annealed	3.57	25.1	34.4	2.4×10^{20}
CTO + i-ZnO CSS chamber annealed	3.48	21.0	33.4	3.0×10^{20}
Stripped CdTe device	3.60	8.7	52.7	4.5×10^{20}

4.4 Best Performing Devices with CTO: Comparison with Different Substrates

The optimized parameters for CTO preparation that were determined from depositions on ABSG and SLG substrates were used to fabricate CdTe devices on thin Corning® Willow® Glass substrates using the CSS technique. Figure 4.6 shows a comparison of the J-V curves for the best performing devices fabricated on 1.1 mm ABSG, 3.0 mm SLG substrates, and 0.2 mm Corning® Willow® Glass. The CTO layers in these devices were sputtered in 20% O_2 and were ~300 nm thick. The best device efficiencies for the SLG, ABSG, and Corning® Willow® Glass substrates were 11.7%, 13.4%, and 14.4%, respectively.

Devices made on both Corning® Willow® Glass and ABSG samples showed a greater J_{SC} value than devices on SLG, presumably due to the higher transmittance of these glasses. Figure 4.6 also shows that the devices all have different V_{OC} values. This could be due to differences in the effect of the $CdCl_2$ treatment since all three underwent

a treatment that was optimized for 3.2 mm glass substrates. Higher performance for Corning® Willow® Glass is expected with further optimization.

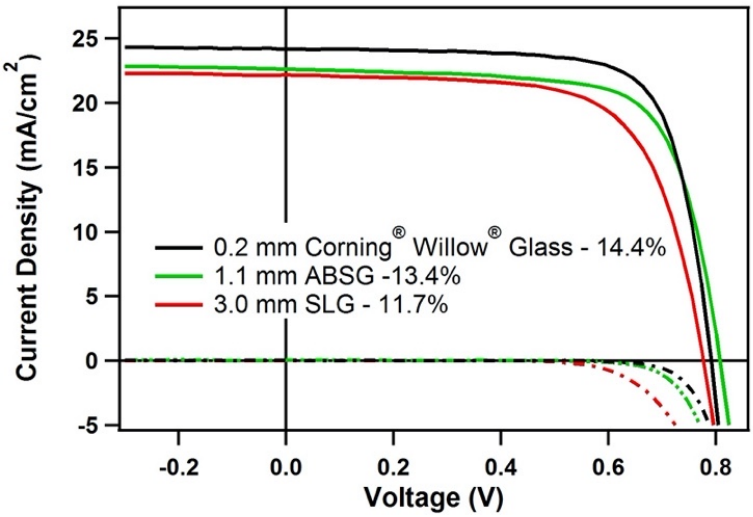

Figure 4.6 J-V Characteristics of the best CdTe devices fabricated on 200 μm Corning® Willow® Glass, 1.1 mm ABSG, and 3.0 mm SLG. The CTO layers were deposited in 20% O_2 ambient.

Alternative materials could also be used as the HRT layer in these CSS deposited CdTe devices, and new materials may affect the optical and electrical properties of the final CTO layer. These investigations need to be the subject of future work.

4.5 Conclusions

In summary, we prepared amorphous CTO films by RF-sputtering and investigated the effect of O_2 partial pressure during the CTO deposition on the performance of CdTe solar cells. We showed that the high temperature CSS deposition process used to fabricate CdTe solar cells improves the electrical and optical properties of the CTO layer. This

shows that the CSS process converts the as-deposited CTO film into a high performance TCO without the need for an intermediate annealing step. The optimized CTO films were used to fabricate CdTe devices on different glass substrates, and a best efficiency of 14.4% was achieved with a flexible Corning® Willow® Glass substrate. With further optimization of the material stack and post deposition processing, higher device performance is expected.

Chapter 5

Improved Short-Circuit Current Density in CdTe Solar cells: Incorporating Se to Window layer

This chapter focuses on further attempts to improve the photogenerated current density in the CdTe solar cells by incorporating CdSe as a window material. Traditional CdSe based devices required a thin layer of CdS layer at the transparent conducting oxide layer interface to preserve the high open circuit voltage. Instead of preparing a conventional CdS/CdSe bilayer where each layer is deposited through physical vapor methods, here we investigate chemically converting a pure CdS layer to form a $CdS_{1-x}Se_x$ film. Preparation of the $CdS_{1-x}Se_x$ film was done by heat treating a pure CdS films with a Se vapor, converting a fraction of the CdS to CdSe through an exchange reaction. The degree of conversion increased as the selenization time increased. The resultant films showed a mixture of CdSe and CdS phases at short times, and the formation of $CdS_{1-x}Se_x$ phases at longer times. To study the effect of the selenized window on device performance, sputtered CdTe films were prepared, and devices were finished. Current-voltage characteristics and external quantum efficiency measurements showed that the selenized CdS did not perform as well as either sputtered CdS or sputtered CdSe

windows. Better control of the intermixing with CdTe and the defect physics could lead to higher performance devices in the future. Results in this chapter have been published in Liyanage et al., 2017[93], © IEEE. Printed with permission, from Geethika K. Liyanage, Adam B. Phillips, Zhaoning Song, Suneth C. Watthage, Ramez H. Ahangharnejhad, and Michael J. Heben, $CdS_{1-x}Se_x$ Window Layer for CdTe Prepared by the Exchange of S with Se in CdS Films, 2017 IEEE 44th Photovoltaic Specialist Conference (PVSC), and June. 2017.

5.1 Introduction

CdTe is a promising absorber material for thin film photovoltaics (PV) due to its direct band gap and high optical absorption coefficient [17]. The record efficiency of CdTe has been dramatically increased over the past five years, reaching a power conversion efficiency (PCE) of 22.1% for research scale devices [94]. Recent increases in the record PCE are mainly due to the increases in the short circuit current density (J_{SC}) which has been achieved by increasing the current collection in both the short- and long-wavelength regions.

CdS has been extensively used as the heterojunction partner for CdTe devices. However, photons absorbed in the CdS generally do not contribute to the photogenerated current and, due to its band gap (2.4 eV), the lost current density can be substantial. To overcome this, various methods have been investigated, including reducing the thickness of the CdS layer[34, 35] and using wide band gap window layers such as CdS:O[17, 19, 36] and ZnS[16].

Recently, Paudel and Yan[37] showed that using CdSe (bandgap ~ 1.7 eV) as the window material can lead to an enhancement of J_{SC} in both short and long wavelengths. The high solubility of Se in CdTe lead to the formation of a graded $CdTe_{1-x}Se_x$ layer during high temperature absorber preparation or post-deposition treatments, reducing the effective bandgap of the absorber layer[37, 95]. While this enhances the current collection from long wavelength photons, the complete interdiffusion of CdSe into the CdTe layer improves the photo response of the device in the short wavelength region. The loss of open circuit voltage (V_{OC}) and fill factor (FF) observed in these CdSe/CdTe devices was attributed to the lower carrier lifetime in the intermixed $CdTe_{1-x}Se_x$ layer [95]. By incorporating a CdS/CdSe bilayer, the values of these parameters were recovered while retaining the high J_{SC}[37].

All of these studies with a CdS/CdSe window used layer-by-layer deposition of CdS and CdSe by sputtering [37, 95] or pulsed laser deposition [96, 97]. In the present study, $CdS_{1-x}Se_x$ thin films were prepared by an exchange reaction of S with Se in CdS thin films prior to completing the CdTe devices. This was accomplished by heating CdS thin films with Se vapor for various periods of time. Se exchanged films were analyzed for their optical properties as well as the elemental compositions and crystal structures. Finally, these films were used as the window layer in CdTe PV devices.

5.2 Experimental Details

100 and 10 nm thick CdS thin films were prepared on commercially available TEC 15M (SnO_2:F/SnO_2; Pilkington NA) substrates by sputtering at a substrate temperature of 250 °C, (0.41 W/cm^2, 15 mTorr and 23 sccm of Ar). An aluminum box

with inner dimensions of 50 mm × 50 mm × 5 mm was used to perform the Se exchange. The CdS samples and Se powder (Sigma Aldrich, 99.99%) were loaded into the box in a glove box and sealed with a graphite gasket. Films were heated to 350 °C for 30 min, 60 min, 90 min, 120 min, or 300 min. After cooling to the room temperature, the films were rinsed with methanol to remove any Se residue.

The optical transmittance of these films was measured using a Perkin-Elmer Lambda 1050 spectrophotometer. Surface images of these films were acquired using a Hitachi S-4800 UHR-Scanning Electron Microscope (SEM), and the composition analysis was done using the energy dispersive x-ray spectroscopy (EDS). To examine the structure of these films, x-ray diffraction patterns were obtained using a Rigaku Ultima III X-ray diffractometer in parallel beam mode with a fixed angle of 1° .

To fabricate CdTe solar cells, 2.1 μm thick CdTe films were deposited by sputtering on the prepared $CdS_{1-x}Se_x$ films at a substrate temperature of 250 °C, (0.41W/cm^2, 10 mTorr and 23 sccm of Ar). As-grown CdTe devices were activated by heat treating with $CdCl_2$ at 387 °C for 30 min in dry air. $CdCl_2$ activation for a longer duration (up to 45 min) were also performed on similar films to investigate the intermixing of the graded $CdS_{1-x}Se_x$ with CdTe. After removing the excess $CdCl_2$ with methanol, a standard back contact processing was performed by evaporating 3 nm of Cu and 40 nm of Au followed by a heat treatment at 150 °C in air for 30 min. The prepared devices were laser scribed to define a cell area of 0.08 cm^2. Current density-voltage (J-V) characteristics were measured under simulated AM1.5 illumination. Behavior of the photocurrent generation in these devices was characterized by external quantum efficiency (EQE).

5.3 Results and Discussion

5.3.1 Optical Properties of the Selenized CdS films

The evolution of the optical properties was examined by measuring the transmittance spectra. As shown in Figure 5.1(a), as-deposited CdS films shows a clear absorption edge at the wavelength of ~ 512 nm corresponding to a 2.42 eV band gap. As the selenization time increases, the absorption feature at 512 nm decreases. At the same time, there is an increase in absorption over the range of 520 to 710 nm, likely due to the formation of a CdSe layer on the film surface with a Se gradient in to the CdS layer. The thickness of this graded layer likely increased with selenization time as more Se diffused into the CdS, reducing the thickness of the pure CdS layer.

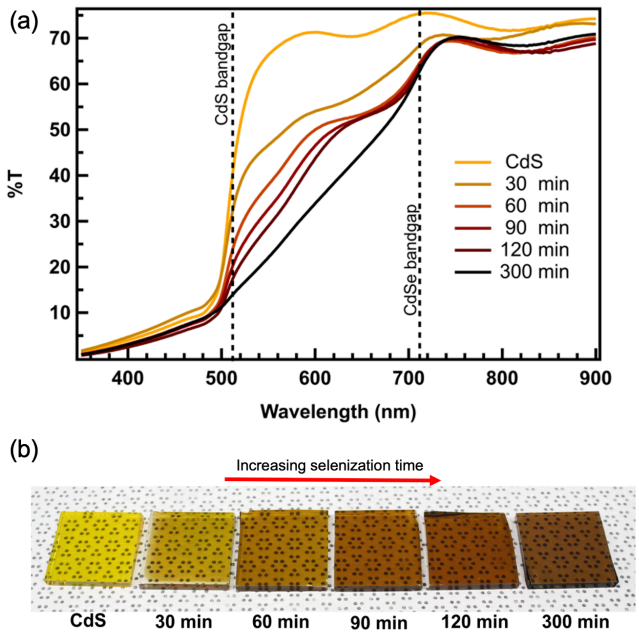

Figure 5.1 (a) Optical transmittance spectra, and (b) optical images of the $CdS_{1-x}Se_x$ films with different selenization times.

For selenization times up to 120 min, a visible absorption edge at the CdS bandgap indicates that there is still a pure CdS region at the SnO_2 interface. For the sample treated at the longest time (300 min), there is no evidence of a clear band edge at the CdS absorption wavelength, indicating that pure CdS layer no longer exists. Rather the film consists of a CdSe surface at the front and a CdS surface at the back with a graded composition between the two.

Figure 5.1(b) shows the evolution of the physical appearance of the selenized samples. The color of these films changed from light yellow (CdS) to reddish-brown (expected for CdSe) with increasing selenization time as expected for Se incorporation into CdS films.

5.3.2 Surface Morphology and Compositional Changes from Selenization

To investigate the compositional variation of the $CdS_{1-x}Se_x$ films as a function of the selenization time, the S and Se content of the films was probed by EDS (Figure 5.2(a)). The molar ratio of Se to S increased with increasing selenization time, which is consistent with the evolution of the optical properties of the films. After 120 minutes of selenization, the Se:S ratio was close to 1:1. Further, or even complete, conversion of CdS into CdSe is expected with the increasing exposure time to Se vapor.

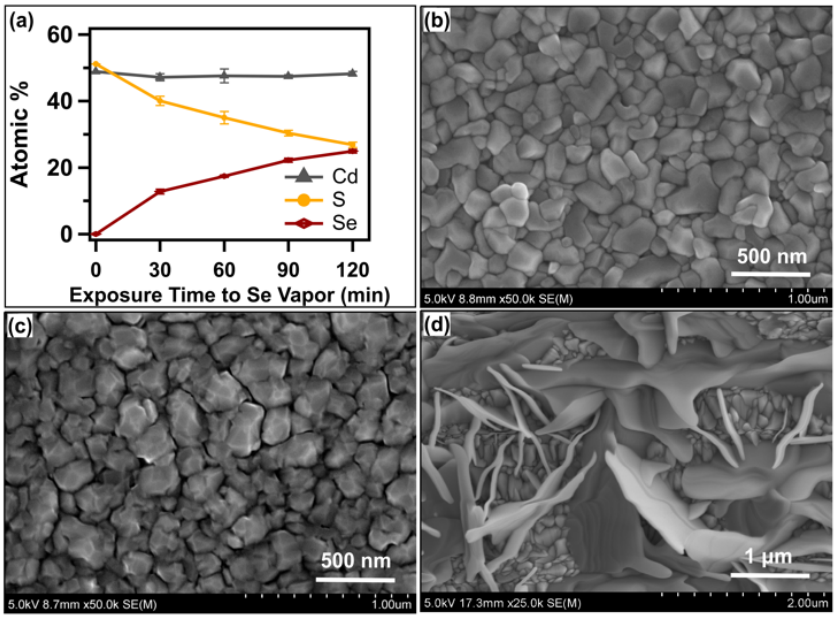

Figure 5.2 (a) Compositional variation of $CdS_{1-x}Se_x$ film with time, SEM images of (b) prepared $CdS_{1-x}Se_x$ film by selenization at 350 °C for 120 min, (c) an as-deposited CdS film, and (d) a clean TEC 15M glass after selenization at 350 °C for 120 min.

The surface morphology changes due to selenization were investigated by imaging prepared films using SEM. Figure 5.2 (b) and (c) shows SEM images of a $CdS_{1-x}Se_x$ film and an as-deposited CdS film. These images show that the $CdS_{1-x}Se_x$ film has smaller grains with smoother edges as compared to the as-deposited CdS film. No Se particles were found on the surface of the selenized samples even after a 120 min heat treatment in Se vapor, while Se flakes were condensed onto the bare SnO_2 surface when CdS was not present (Figure 5.2(d)). Thus, the color change for the treated films (Figure 5.1(b)) is clearly not due to deposition of Se on top of the CdS film.

5.3.3 Changes to the Crystal Structure with Increasing Selenization Time

XRD patterns were obtained for the $CdS_{1-x}Se_x$ films in an effort to fully understand the details of the selenization phase (Figure 5.3). As-deposited CdS shows the characteristic peaks for the hexagonal wurtzite structure (h-CdS). After 30 min of selenization diffraction intensities associated with the h-CdS phase decreased, while peaks belonging to the wurtzite CdSe (h-CdSe) started to appear. This change is most clearly seen in the range of 2θ from 45° to 49° where there is no overlapping with the SnO_2 signals (inset of Figure 5.3). After 30 min of selenization time, two distinct peaks at 2θ = 45.9° and 2θ = 47.8° associated with diffractions from (103) planes belonging to h-CdSe and h-CdS, respectively, were visible. This indicated that interaction with Se vapor for this relatively short time period resulted in a structurally distinct CdSe phase rather than a $CdS_{1-x}Se_x$ alloy. This is consistent with Se vapor readily interacting with the high-energy surfaces of CdS grains (Fig. 2d) and the formation of a CdSe shell on the exterior of the grain. This process could lead to the smoother grain surfaces seen in Figure 5.2(c). The (103) diffraction intensity for h-CdS further decreased with increasing selenization time while the intensity of the companion peak belonging to h-CdSe increased with no shift in the peak position. At the same time, diffraction intensity between 2θ = 45.9° and 2θ = 47.8° increased, suggesting the formation of intermediate $CdS_{1-x}Se_x$ phases. For longer selenization times (300 min), the (103) diffraction for h-CdSe was prominent while the companion peak from CdS was absent. However, there was still a significant shoulder on the high 2θ side, indicating the presence of $CdS_{1-x}Se_x$ phases. Note that the diffraction

intensities from the SnO_2 layer were unchanged during the selenization, indicating that the structure of the SnO_2 film was not significantly changed.

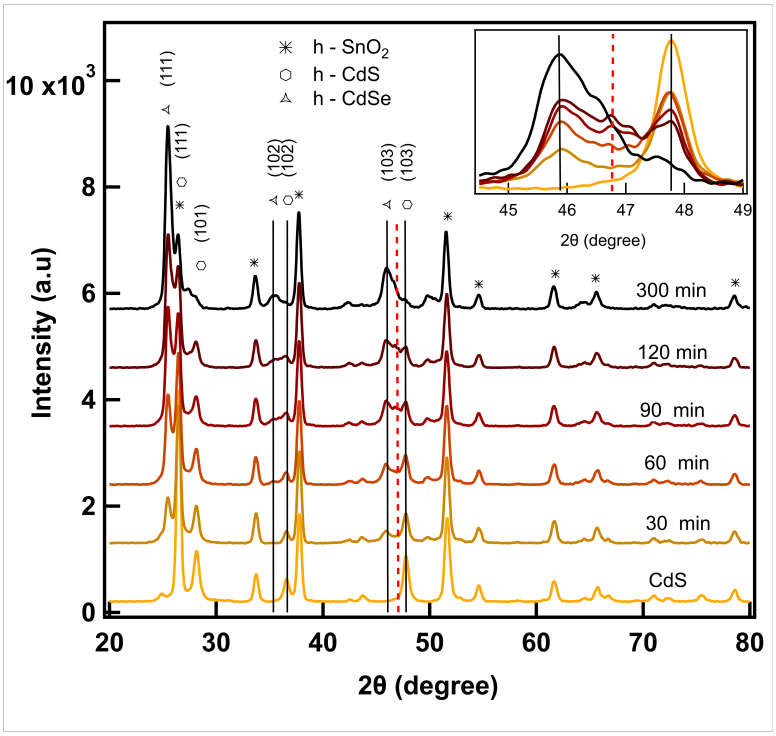

Figure 5.3 XRD pattern data for CdS films after Se exchange for different exposure times to Se vapor.

5.4 CdTe device Fabrication with Selenized $CdS_{1-x}Se_x$ Films

To test the photovoltaic performance of thin film solar cells prepared with the selenized CdS window layer, we deposited CdTe layers by sputtering and finished the devices with back contacts, as described above. Two control devices, one with 100 nm CdS and one with 100 nm CdSe, were also fabricated for comparison. Figure 5.4 shows the J-V characteristics and EQE of several devices.

The PV performance (Figure 5.4(a)) of the devices prepared with the $CdS_{1-x}Se_x$ window layers was worse than that of either of the control devices. The losses in V_{OC},

J_{SC}, and FF increased as the selenization time was increased. The EQE (Figure 5.4(b)) showed an increase response in the long wavelength region (>850 nm) when Se was present. This is consistent with a reduction in the CdTe band gap with Se incorporation[38]. For longer selenization times, increase in the wavelength at which a photo-response occur is consistent with further Se diffusion into the grains. While the device made with sputtered CdSe shows an enhanced photocurrent generation in both short and long wavelength regions, as well a flat generation profile across the intermediate wavelengths, devices made with a selenized layer show improved long wavelength response but poor response in the 350 to 700 nm regions.

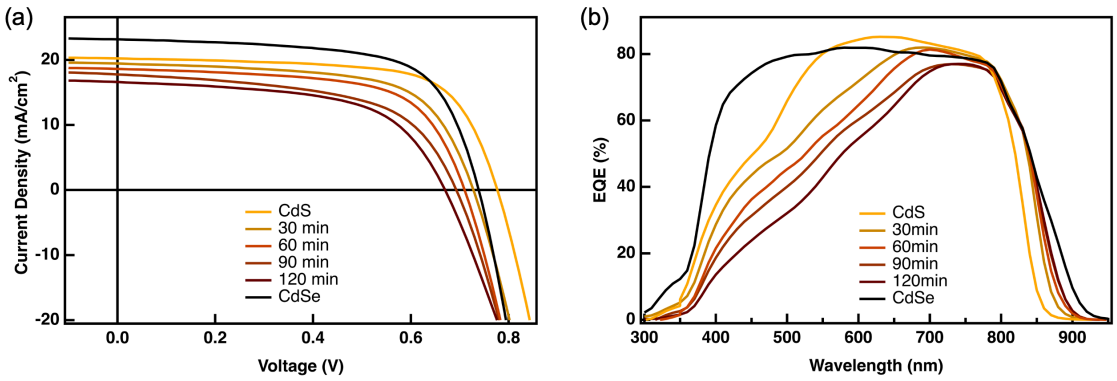

Figure 5.4 (a) J-V characteristics and (b) EQE measurements of CdTe devices made on window layer comprised with 30 min, 60 min, 90 min, and 120 min Se exchange compared to CdTe devices made on 100 nm CdS (control CdS), and 100 nm CdSe (control CdSe).

The devices fabricated with the control CdSe and $CdS_{1-x}Se_x$ window layers showed a lower V_{OC} and FF as compared to the control CdS device, with the values for the $CdS_{1-x}Se_x$ layers being below those for the control CdSe device and being worse with

increasing selenization time. Poplawsky *et al.* [95] attributed the loss in V_{OC} with Se incorporation to lower carrier lifetimes that arise from the intermixing of Se with CdTe during the high temperature deposition/post-deposition processes used in that work. The evolution of the EQE with selenization time and the inflection point around 500 nm suggests the presence of CdS for both 30 and 60 min of selenization time, consistent with the XRD data. At longer selenization times the shape of the EQE curve becomes more triangular, with very little response on the short wavelength side. At the longest selenization time the EQE data resembles the data found for the 400 nm thick sputtered CdSe layer in the work of Poplawsky *et al*.[95]. In that work, the relatively thick 400 nm CdSe layer produced a wurtzite CdTe-CdSe alloy that was photo-inactive, while thinner CdSe layers led to Se-poor zincblende CdTe-CdSe alloys that were photoactive. We note that our highest processing temperature (387 °C) occurred during the $CdCl_2$ treatment while Poplawsky *et al*. [95] grew the CdTe layer by closed space sublimation at 610 °C. Therefore, the degree of intermixing of Se and Te in the CdTe is likely to be different despite the similarity between the EQE data.

5.4.1 Role of Se exchange in $CdS_{1-x}Se_x$ with Te in CdTe devices

To fully investigate the role of Se exchange with Te in CdTe, we varied the $CdCl_2$ treatment time. Experiments were performed on CdTe devices prepared with 100 nm thick CdS samples that had been selenized for 60 min. Figure 5.5(a) shows that the V_{OC} and J_{SC} were adversely impacted, suggesting that the devices were in fact over-treated, perhaps even at after 30 min. Consistently, the EQE data (Figure 5.5(b)) shows loss in current generation across the range 400 – 700 nm with increased treatment time,

indicating increasing recombination losses for light absorbed near the junction. It is interesting to note that the long wavelength response was not effected.

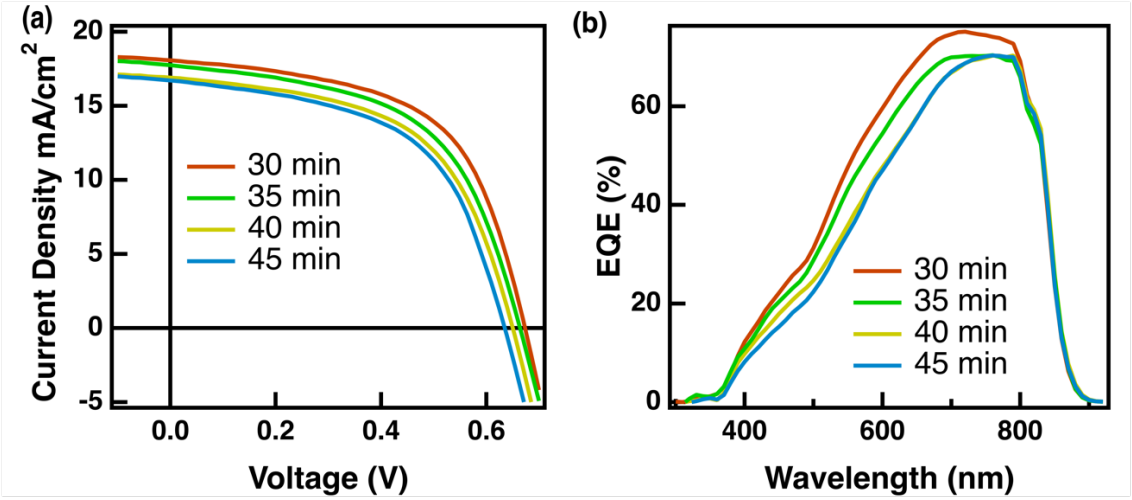

Figure 5.5 (a) J-V characteristics and (b) EQE measurements of CdTe devices prepared on $CdS_{1-x}Se_x$ (60 min selenization time at 350 °C) finished with different $CdCl_2$ activation times.

We orginally anticipated that a fully selenized CdS layer could perform as well as a sputtered CdSe layer and, if some CdS was retained, it might be possible to obtain the short circuit current enhancements while maintinaing a high V_{OC}. However, the selenized CdS samples, in all cases, lead to poorer performance than sputtered CdS alone or pure sputtered CdSe. In another approach, we sputtered a 10 nm CdS film on TEC15M and selenized it for 60 min at 350 °C to prepare a thin $CdS_{1-x}Se_x$ film. From the transmission and EDS data presented earlier we concluded that 60 min would be sufficient to nearly fully selenized the thin CdS layer to produce a CdSe layer with a small S content. After selenization, 90 nm of CdSe was subsequently sputtered on top.

This stack and two other stacks, comprised of 100 nm CdS and 100 nm CdSe layers on TEC15M, were finished into devices by sputtering 2.1 μm of CdTe, performing a $CdCl_2$ treatment (30 min at 387 °C), followed by standard back contact processing. Figure 5.6 shows the J-V and EQE performance of these devices. Once again, we see characteristic beahavior for the CdS and CdSe devices.

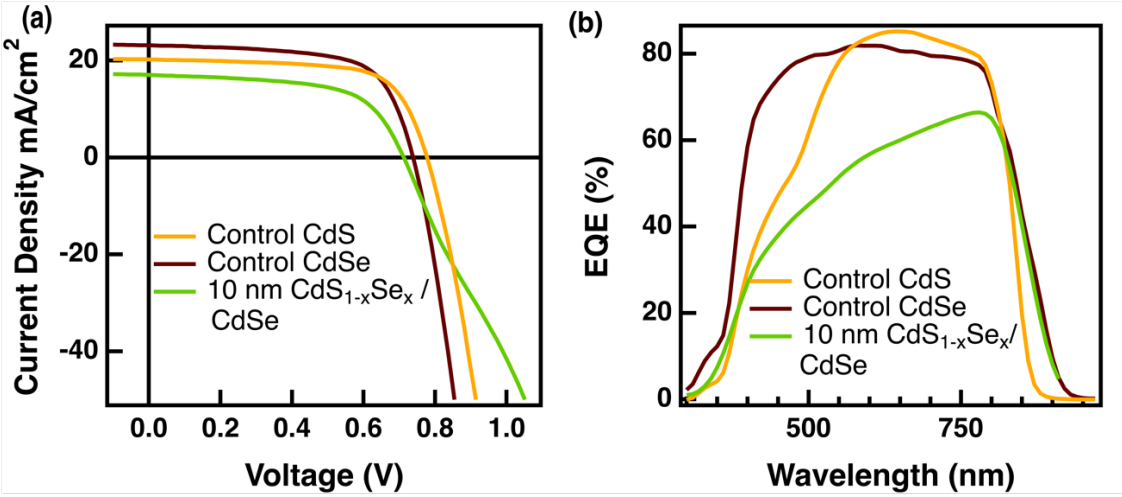

Figure 5.6 (a) J-V characteristics and (b) EQE measurements of CdTe devices made on 100 nm CdS (control-CdS), 100 nm CdSe (control-CdSe), and 10 nm selenized CdS (60 min selenization time) with additional 90 nm CdSe.

The J-V data shows a higher V_{OC} and lower J_{SC} for the CdS device, while the reverse is true for the CdSe device. Turning to the EQE, the CdS device shows a notch associated with absorption at wavelengths < 500 nm that does not contribute to the photocurrent, while the CdSe device has a broader, flatter response that extends to longer wavelengths. The device with the $CdS_{1-x}Se_x$/CdSe bilayer has V_{OC} and J_{SC} values that are smaller than those of the control devices. The J-V curves also shows roll-over in forward

bias, which suggests the formation of an additional junction in the device, perhaps at the $CdS_{1-x}Se_x$/CdSe interface.

In this device configuration the Se-Te interdiffusion is expected to be governed by the properties of the CdSe/CdTe interface. Consequently, it is somewhat surprising that the inclusion of a thin, nearly fully selenized $CdS_{1-x}Se_x$ layer could introduce such significant losses in the EQE. Evidently, the defect distribution within the $CdS_{1-x}Se_x$ layer and its structure is significantly different from that of the sputtered CdSe film. We note that the EQE data for the $CdS_{1-x}Se_x$/CdSe bilayer and the CdSe devices overlaps in the long wavelength region indicating that the photocurrent generation and collection mechanisms are the same at these wavelengths. In contrast, the EQE at shorter wavelengths is severely impacted. The data suggests that the recombination rates are much higher for carriers that are generated near, or can diffuse in to, the $CdS_{1-x}Se_x$ layer.

The poor performance of devices with $CdS_{1-x}Se_x$ layers is most likely due to the defect structure in the layers. Additionally, the XRD data indicated that the selenization does not proceed in a homogeneous fashion, particularly when the as-deposited CdS layer consists of small grain material. Even in the limit of long-time selenization there is still evidence of S content and the grain structure suggests that the S is not uniformly distributed. This lack of homogeneity is very likely translated to the Se-Te exchange that has been shown to be beneficial at the CdSe/CdTe interface. For example, one can imagine a situation where CdSe on grain surfaces in the initial window layer may intermix with the CdTe during the $CdCl_2$ activation, while S and Se content in elsewhere in the heterogeneous layer may not participate in the intermixing. These issues have been highlighted by Grice *et a*l.[98] where it was determined that CdSe/CdTe interface mixing

of low temperature sputtered devices occurs only during the $CdCl_2$ activation step while, in contrast, significant intermixing occurs during a high temperature deposition processes such as closed space sublimation. A similar approach may promote intermixing in these $CdS_{1-x}Se_x$/CdTe devices to obtain a better junction quality.

5.5 Conclusions

$CdS_{1-x}Se_x$ thin films were prepared by selenization of CdS films in a closed aluminum box. The degree of selenization was controlled by adjusting the exposure time to Se vapor at 350 °C. X-ray diffraction data indicates that films produced with 30 min of selenization consist of grains with a CdSe shell CdS interior. Increasing selenization time resulted in the further diffusion of Se into the grains and a more complete conversion to CdSe. The $CdS_{1-x}Se_x$ films were used as a window layer in sputtered CdTe devices. Prepared devices showed poor performance compared to standard CdTe devices fabricated on either CdS or CdSe. EQE results show a significant photocurrent loss in the 400-700 nm range in these devices due to poor intermixing of the $CdS_{1-x}Se_x$ with CdTe. A high temperature absorber preparation method could be used to promote this intermixing to obtain better junction quality.

Chapter 6

Advancements to the Front Contact: Role of Band Alignment at the Transparent Front Contact/Emitter Interface in the Performance of Wide Bandgap Thin Film Solar Cells

Moving forward with experimental work completed in the laboratory environment, it was crucial to establish methods to increase the performance of these CdTe devices. Following the research done both numerical modeling and experimental work, further studies on numerical modeling was carried out to investigate a suitable front contact combination to obtain high performance CdTe solar cells.

Even though researches have highlighted the importance of appropriate band alignment between the emitter and the absorber for high performing CdTe devices, impact of the band alignment between the TCO and the emitter interface has not been thoroughly investigated. This chapter will focus on the role of the TCO/Emitter interface alignment and the importance of maintaining a proper alignment when moving to wide bandgap absorber. In this work it was identified that, in order to obtain an optimum device performance from any wide bandgap absorber we should maintain at most 0.3 eV offset between the TCO and the emitter. Results also suggest that solar cells with wide bandgap absorbers and poor TCO/emitter band alignment, a blocking layer will be

formed resulting in an s-kink in the current density-voltage curve and poor performance due to low FF in the devices. This work has been published in Liyanage et al., 2018[99] reproduced from APL Materials, Vol 6(10), Geethika K. Liyanage, Adam B. Phillips, and Michael J. Heben, Role of band alignment at the transparent front contact/emitter interface in the performance of wide bandgap thin film solar cells, Pages 101-104, with permission from AIP Publishing.

6.1 Introduction

Recently, researchers at Colorado State University fabricated high efficiency CdTe devices by replacing the CdS emitter with Mg-doped ZnO ($Mg_{1-x}Zn_xO$, or MZO).[33] Because the MZO used for these devices had a bandgap (E_G) of ~3.7 eV (x = 0.23), the short wavelength response of the quantum efficiency (QE) showed no significant losses at energies below the E_G of the transparent conducting oxide (TCO). The QE data closely resembled the data for record CdTe cells,[100] suggesting that MZO or another large E_G emitter may have been employed in First Solar's devices.

While the increase in current collection due to lack of absorption in CdS certainly improves the device performance, much of the improvement was due to appropriate conduction band (CB) alignment at the MZO/CdTe interface.[31, 32] When CdS is the emitter, the emitter/absorber CB offset ($E_{CB}^{em} - E_{CB}^{abs} = \Delta E_{CB}^{em/abs}$) is negative and a cliff is formed at the CdS/CdTe interface. This gives rise to CdTe energy bands that are nearly flat near open circuit voltage (V_{OC}), high concentrations of both electrons and holes near the interface, and, thus, high front surface recombination rates. By replacing the CdS with MZO, which has a higher energy CB, a spike ($\Delta E_{CB}^{em/abs} > 0$) can be formed. The spike

increases the band bending in the CdTe and reduces the concentration of holes at the interface by orders of magnitude. Too large of a spike, however, can block the flow of minority carriers. The spike for CdTe is optimized when $\Delta E_{CB}^{em/abs}$ is ~0.2 eV.[31, 32] Correct band alignment at the emitter/absorber interface increases both the V_{OC} and the fill factor (FF).

Wide E_G absorbers for top cells in tandem devices can be developed by alloying CdTe with either ZnTe[101] or MgTe[102]. However, the highest reported efficiencies for polycrystalline $Cd_{1-x}Zn_xTe$ (CZT; 11.5 %)[103] and $Cd_{1-x}Mg_xTe$ (CMT; 9.3 %)[104] are still too low for use in tandems.[105, 106] Because these devices have evolved from CdTe devices, CdS is typically the window layer.[101, 104, 107, 108] The low efficiencies achieved to date may be expected due to the presence of a cliff at the emitter/absorber interface. Indeed, increasing E_G in CZT alloys is dominated by an upward movement of the CB, while the formation of CMT results in both the conduction and valence bands moving to higher and lower energies, respectively.[109] Thus, the cliff at CdS/CZT and CdS/CMT interfaces should be larger than the one at a CdS/CdTe interface.

We recently performed simulations of the current density-voltage (JV) characteristics of wide bandgap CZT and CMT absorbers.[110] While modeling the performance of a 1.7 eV absorber, with MZO as the emitter and several TCOs, we determined that the band alignment at the TCO/emitter interface is also very important, especially within the context of recent emitter/absorber interface engineering. In this contribution, we focus on the role of the TCO/emitter band offset and explore the performance of devices fabricated with wide E_G absorbers when the emitter/absorber

spike is kept constant at an optimum value. We also investigate and compare the relative importance of barriers at the front and back contacts. We conclude that proper band alignment at the TCO/emitter interface is essential for producing high efficiency thin film solar cells.

6.2 Details to the 1D Numerical Model

Simulations were carried out using the SCAPS-1D software developed at the University of Gent.[111] Devices were built in the superstrate structure with a 500 nm thick highly doped ($5x10^{20}$ cm^{-3}) transparent front contact, a 50 nm MZO emitter layer, and a 2 μm thick absorber. The valence band (VB) energy for the absorber was fixed at the value for CdTe, -5.9 eV. As E_G for the absorber was changed, the CB moved to higher energy, as expected for increasing the Zn content in CZT. The emitter E_G was changed in concert to maintain a 0.2 eV CB spike at the emitter/absorber interface. The changes in E_G for the emitter correspond to changes in the Mg content in MZO. Gaussian mid-gap defects states were assumed in the absorber with a lifetime of 1 ns for both holes and electrons. Except where noted, an Ohmic back contact was forced in the simulation to avoid the formation of a potential barrier at the back of the device. Other key modeling parameters were obtained from previous CdTe SCAPS simulations[32, 112, 113] (Listed in Table 6.1).

Table 6.1. Parameters Used for SCAPS 1D Simulation

Parameter	TCO	Emitter-MZO	Absorber
Thickness (nm)	500	50	2000
Band gap (eV)	vary	vary	Vary
χ (eV)	vary	vary	vary
Relative dielectric constant	9	10	9.4
N_C (cm^{-3})	2.2×10^{18}	2.2×10^{18}	8.0×10^{17}
N_V (cm^{-3})	1.8×10^{19}	1.8×10^{19}	1.8×10^{19}
Mobility e/h (cm^2/Vs)	100/25	100/25	320/40
Lifetime e/h (ns)	0.1/0.1	$1/10^{-3}$	1
Doping density (cm^{-3})	n: 5×10^{20}	n: 1×10^{17}	p: 1×10^{15}
Interfaces	**TCO/MZO**	**MZO/CdTe**	
S_n, S_p (cm/s)	N.A.	10^5	

6.3 Results and Discussion

6.3.1 Current Stands to the Device Performance for Wide Bandgap Semiconductor Solar Cells

Figure 6.1(a) shows the simulated JV curves for devices with absorber (emitter) E_G of 1.5 (3.6) eV, 1.7 (3.8) eV, and 2.0 (4.1) eV. The TCO was Al-doped ZnO (AZO; E_A = 4.5 eV, E_G = 3.3 eV).[112] The V_{OC} increased as the absorber E_G increased, nearly in a 1:1 ratio. At the same time, the current decreased due to reduced overlap with the solar spectrum. However, the major impact to the performance was associated with a large reduction in FF. The effects on the JV response can be readily understood by considering the band diagrams (Figure 6.1(b)). The potential variation of the CB across the front of the device is different for each of the three E_G, with the MZO layer being more fully depleted in the large E_G case. For the 1.5 eV absorber, the spike height is comparable to the band bending, creating an overall profile which is close to optimal. In

the case of the 2.0 eV absorber, in contrast, the barrier height to minority carrier flow is effectively increased and the bands are flatter. As a result, "rollover" around V_{OC}, like that seen for poor back contacts,[28, 34, 114, 115] degrades the FF.

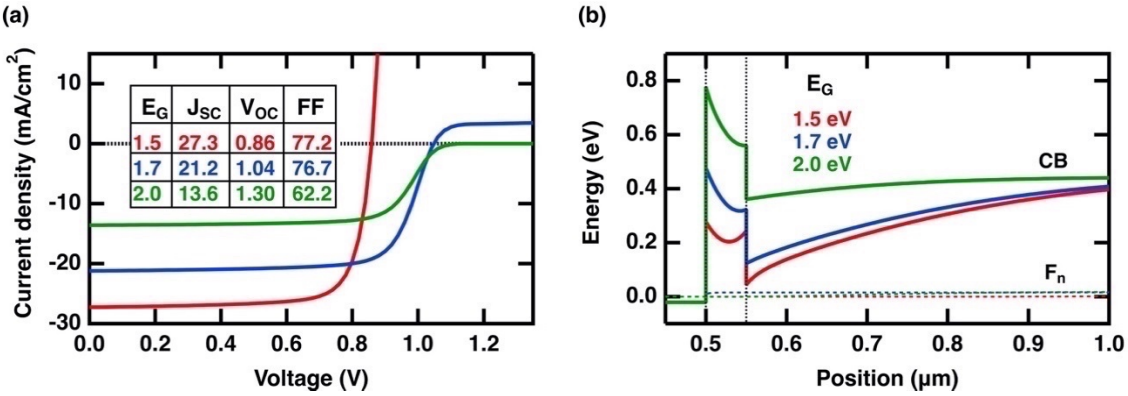

Figure 6.1 (a) Simulated current density-voltage (JV) curves for devices with absorber bandgaps of 1.5 eV, 1.7 eV, and 2.0 eV and (b) conduction band portion of the band diagrams at V_{OC} condition under AM1.5G illumination. A spike of 0.2 eV was maintained at the emitter/absorber interface in all simulations.

6.3.2 Effect from Front Contact Alignment vs Back Contact Alignment to Device Performance

To better understand the role of the energetics at the TCO/emitter interface we compared the 2.0 eV device of Fig. 1 which has "bad" front band alignment ($E_{CB}^{TCO} - E_{CB}^{em} = \Delta E_{CB}^{TCO/em}$= -0.8 eV) to one in which the TCO/emitter CB offset was "good" ($\Delta E_{CB}^{TCO/em}$ = -0.4 eV). Note that we are assuming that the Fermi level in the TCO is at the conduction band energy. Figure 6.2(a) shows the CB portion of the band diagrams for the two devices at short circuit. When the TCO/emitter (front) alignment is bad, the

emitter and absorber CBs near the front of the device remain at a higher energy. The amount of band bending in the emitter and the absorber is a function of the doping level and thickness of the emitter. In the present case, the total number of free carriers in the emitter is low, and the charge transfer that occurs during equilibration causes the depletion region to extend into the absorber layer. When the front alignment is good the quasi-Fermi level for electrons at the front of the device lines up with the Fermi level in the TCO.

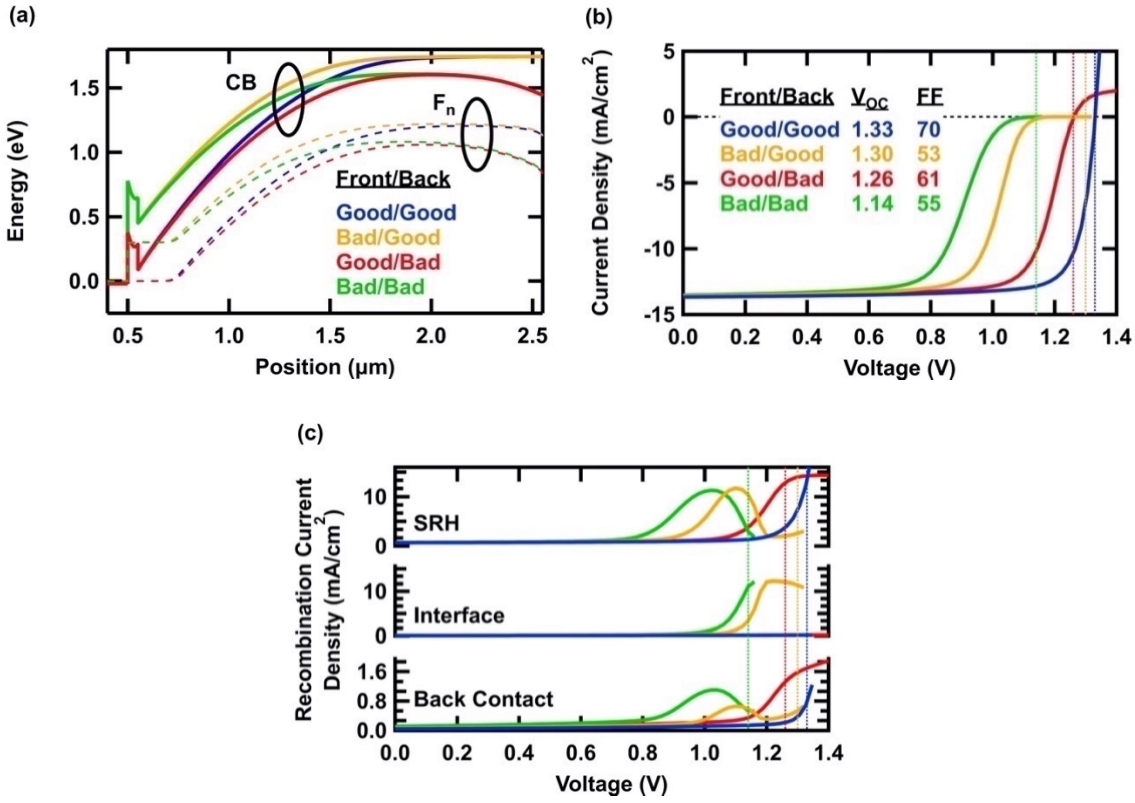

Figure 6.2 (a) Conduction band portion of the band diagram of 2.0 eV devices taken under illumination at 0 V. (b) Simulated JV response and (c) recombination current densities observed in these devices. The vertical dotted lines indicate the V_{OC} for each device.

Figure 6.2(b) and (c) show how the difference in alignment at the TCO/emitter interface affects the JV curve and recombination current density in the device, respectively. For a device with good front alignment and a good (i.e., Ohmic) rear contact (a so-called good/good device) there is negligible interface recombination across all voltages examined, and the Shockley-Reed-Hall (SRH) and back contact recombination currents begin to rise only as a V_{OC} is approached. This is a typical behavior for devices that exhibit a high FF. When the TCO/emitter interface cliff is increased by 0.4 eV to produce a blocking front contact (a "bad/good" device) the carriers are more effectively confined at earlier voltages and the onset of SRH recombination shifts by a corresponding amount, ~0.4 V. This happens because the bands begin to flatten before V_{OC}. As V_{OC} is approached the bands flatten further such that minority carriers are no longer effectively swept from the front surface, and interface recombination begins to dominate. These two effects work in concert to produce the rollover in the JV response and a substantially reduced FF in this bad/good device (Figure 6.2).

The simulation of the bad/good device shows that a barrier at the front of the device can produce effects similar to those produced by a back contact barrier. To determine the relative importance of front and back barriers we modeled two additional 2.0 eV devices. The first was a "good/bad" device that had good alignment at the TCO/emitter interface ($\Delta E_{CB}^{TCO/em}$ = -0.4 eV) but bad VB alignment ($\Delta E_{VB}^{back/abs}$ = -0.30 eV) at the rear contact. This latter value may be compared to the measured barrier height of ~0.4 eV for a CdTe device with a copper-free Au back contact.[116, 117] The second additional device that was modeled was "bad/bad", i.e. with bad alignment at both the TCO/emitter interface ($\Delta E_{CB}^{TCO/em}$= -0.8 eV) and the back contact ($\Delta E_{VB}^{back/abs}$ = -0.30

eV). The introduction of the back barrier introduces a potential drop at the rear contact and a downward bending electron Fermi level. The SRH recombination currents become active at even lower voltages due to the additional carrier containment, as do the back contact recombination currents. In general, the front and back barriers are seen to impede the flow of carriers out of the device in an identical fashion. The back barrier impedes majority carrier holes while the front barrier impedes minority carrier electrons. Carrier build-up at the interfaces and band flattening due to voltage drops at the contacts increases SRH and interface recombination at voltages earlier than V_{OC}. The effects sum to generate stronger rollover in the JV. The impact on the FF is much greater than the impact on V_{OC}.

6.3.3 TCO/Emitter Requirements with Increasing Absorber Bandgap

To determine when "good" alignment at the TCO/emitter interface actually occurs, the performance of devices made with varying absorber E_G was investigated as a function of the TCO electron affinity (E_A^{TCO}). As before, a constant spike ($\Delta E_{CB}^{em/abs}$= 0.2 eV) was maintained at the emitter/absorber interface, and the back contact was Ohmic. Figure 6.3 shows the contour plots of the photovoltaic (PV) parameters. Results were simulated with E_A^{TCO} varying from 4.5 eV to 4.0 eV with a constant doping density of 5 x 10^{20} cm^{-3}. Unfortunately, lowering the doping density or increasing the E_A^{TCO} beyond the values used here resulted in simulations that failed to converge. The dotted line is a reference where $\Delta E_{CB}^{TCO/em}$ equals -0.3 eV, and the lower right-hand corner corresponds to the 2 eV simulation of Figure 6.1 ($E_A^{TCO} = 4.5$ eV, $\Delta E_{CB}^{TCO/em}$ = -0.8 eV).

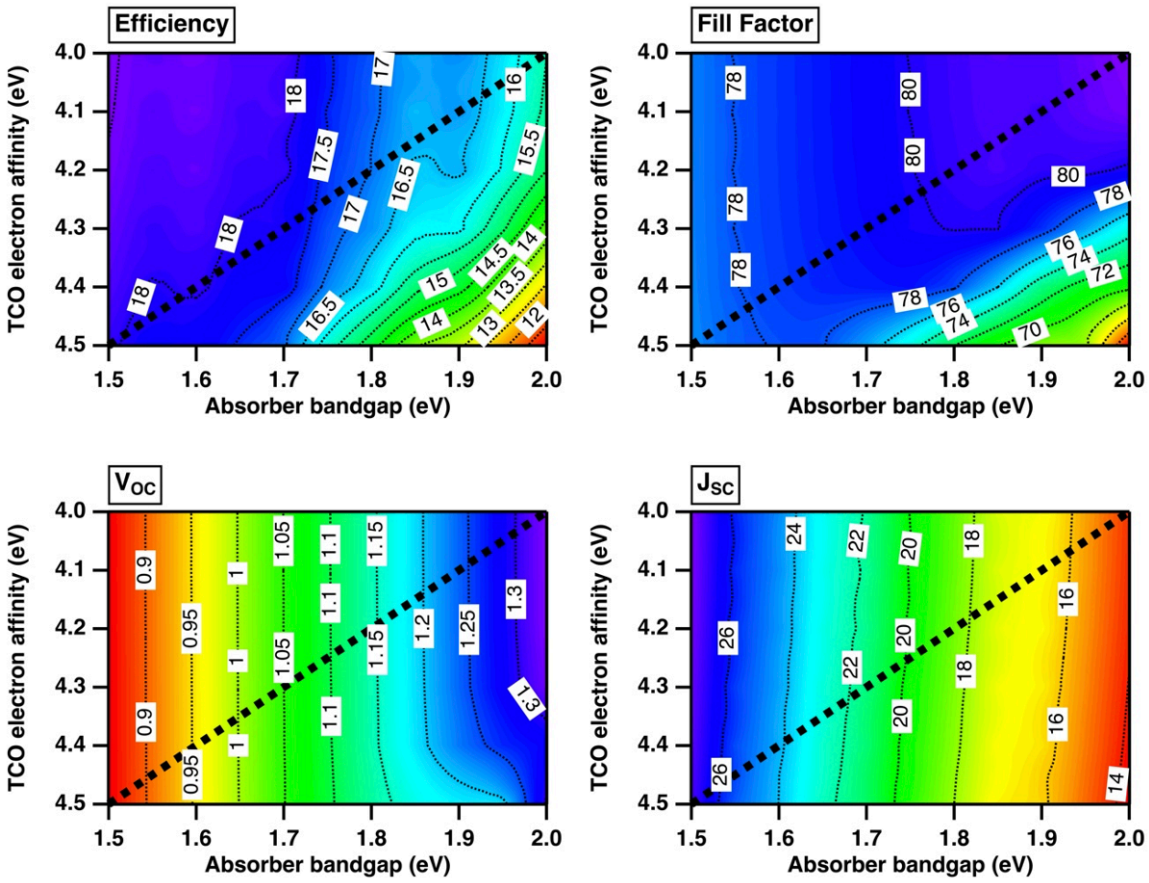

Figure 6.3 Variation of the PV performance with changing absorber bandgap vs TCO electron affinity. For all simulations, the emitter/absorber offset was maintained at +0.2 eV. The dotted line is a guide for the eye that indicates where the conduction band of the TCO is 0.3 eV below the conduction band of the emitter.

As may be expected, J_{SC} is nearly independent of the E_A^{TCO} across the range studied here. V_{OC} is also independent of E_A^{TCO} for absorber E_G below approximately 1.8 eV, and only weakly varying at higher values. The variations in the efficiency can be nearly completed traced to variations in the FF, which show the most sensitivity in the

high E_A^{TCO} high E_G portion of the contour plot. In this portion of the plot, where the magnitude of the $\Delta E_{CB}^{TCO/em}$ cliff varies from -0.3 to -0.8 eV, the constant FF lines are perpendicular to changing $\Delta E_{CB}^{TCO/em}$, indicating that the device performance is nearly completely controlled by the magnitude of the TCO/emitter cliff in this region.

From a practical point of view, it is difficult to determine how our findings relate to published experimental results. The reported E_A and doping density values for SnO_2:F (FTO), a commonly used TCO for CdTe solar cells, range from 5.3 to 4.5 eV and 1 x 10^{19} to 5 x 10^{20} cm^{-3}, respectively. [3,][32, 118] While the largest E_A^{TCO} we used, 4.5 eV, as well as the doping density of 5 x 10^{20} cm^{-3}, are in these ranges, this exact combination we used may not be commonly available. The E_A of a material, in particular, can be a strong function of the crystalline facets and electric dipoles present on the specific local surfaces. With this degree of sensitivity, the actual E_A of a particular TCO will be dependent on the production and handling methods. However, with E_A values for FTO being 4.5 eV and larger, and with the clear trends shown in Figure 6.3, as $\Delta E_{CB}^{TCO/em}$ is made even more negative with larger values of E_A^{TCO}, poor values of FF can be expected for devices with smaller E_G, too. In fact, extrapolation of the data presented in Figure 6.3 suggests that even CdTe devices may be sensitive to TCO selection when E_A^{TCO} is substantially greater than 4.5 eV. This may explain the inflection in the JV curve observed by Kephart *et al*.[32] for MZO/CdTe devices with a 0.2 eV spike at the interface. In fact, the importance of band alignment at the TCO/MZO interface in CdTe solar cells was recently mentioned as a potentially limiting factor.[74]

It is also interesting to consider the recently reported 6.5% device which was fabricated with an MZO emitter and Se as the absorber.[119] In that work, the conduction

band offset at the emitter/Se interface was varied by adjusting the MZO composition. Surprisingly, the highest efficiency device had a cliff at the MZO/Se interface, rather than spike. As the size of the cliff was decreased the V_{OC} increased, but not as quickly as the FF decreased. Our results suggest that the poor device performance, specifically the low FF, is due to poor TCO/MZO alignment. FTO was used as the TCO in that work, possibly resulting in a TCO/emitter barrier that would dominate the device performance. For higher efficiency devices with Se, the TCO would need to be replaced by one with an E_A at least 0.5 eV lower, possibly a Mg-doped AZO.[120]

6.4 Conclusions

This study shows that the CB offset at the TCO/emitter becomes increasingly important as the absorber E_G increases. In addition, we showed that with poor band alignment at the front, rollover behavior emerges, which introduces an s-kink in the JV curve at voltages below V_{OC}. A barrier at either the front or the back of the device can introduce similar behavior, which may be difficult to diagnose. For good TCO/emitter alignment, the TCO CB edge cannot be more than 0.3 eV below the emitter CB edge.

Chapter 7

The Role of Back Buffer Layers and Absorber Properties for >25% Efficient CdTe Solar Cells

Previous chapters focused on improving the quality of the absorber layer and the front contact alignment in CdTe solar cells. With these improvements to the front end of the device, understanding minority carrier recombination at the back contact is crucial in achieving the high performance CdTe devices. This chapter presents the results of numerical simulations performed to understand how the band alignment in the back contact of CdTe devices effect the devices performance. In particular, results illustrates how valence and conduction band offsets and the doping level in the CdTe and a back buffer layer would impact the device performance. Simulations extends to finding the needed properties for a back buffer layer that would facilitate 25% PCE in CdTe devices. The results in this chapter have been published in Liyanage et al.,[121] and reprinted (adapted) with permission from Geethika K. Liyanage, Adam B. Phillips, Fadhil K. Alfadhili, Randy J. Ellingson, and Michael J. Heben, The Role of Back buffer Layers and Absorber Properties for >25% Efficient CdTe Solar Cells, Vol 2, Issue 8, Pages 5419-5426, Copyright (2019) American Chemical Society.

7.1 Introduction

For over a decade, the record photoconversion efficiency (PCE) for CdTe devices stood at 16.5%.[17] Starting in 2011, this record was broken eight times in rapid succession by GE Solar and First Solar. It currently sits at 22.1%[100] and appears to be at a technological roadblock. Kanevce et al. employed numerical modeling to determine routes for improving device efficiency to higher values.[122] They determined that increasing the absorber doping density and carrier lifetime is necessary to improve the device efficiency. However, as these values improve, front surface interface recombination becomes more significant and can limit device performance. With this in mind, they reported that a minority carrier lifetime (τ_e) > 100 ns, a front surface recombination velocity (FSRV) < 100 cm-s^{-1}, and a CdTe free-hole density (p_{CdTe}) > 2 x 10^{16} cm^{-3} would be simultaneously required to reach 25% efficiency.[122]

Experimental work to increase both the minority carrier lifetime and hole density in the absorber has begun. Minority carrier lifetimes determined from photoluminescence decay curves[123] greater than 25 ns have been reported for polycrystalline CdTe films,[124],[125] while lifetimes longer than 100 ns have been measured for CdTe and $CdSe_xTe_{1-x}$ in Al_2O_3 double heterostructures.[40, 126] Separately, a recent report demonstrated that the hole density in polycrystalline CdTe could be modified through the incorporation of dopants in the gas stream during vapor transport deposition.[127] Dopant densities on the order of 1 x 10^{16} cm^{-3} were reported without a reduction in the carrier lifetime.[127]

Very little is publicly known about the characteristics of the materials and interfaces in the current record CdTe device. To date, the highest PCE presented in the

open literature with detailed fabrication instructions is 19.1%.[33].[64] A key advance in that work was the development of a wide bandgap emitter layer, $Mg_XZn_{1-X}O$ (MZO),[32] which allows the emitter/CdTe band alignment at the front of the device to be controlled through variation in the Mg concentration. With optimized band alignment, the near surface band bending could be controlled to reduce the hole density at the front interface.[31] This effect was reported as being responsible for developing a higher open circuit voltage (V_{OC}), fill factor (FF), and efficiency.

The experimental progress on front surface interface engineering prompted additional simulations to reassess the requirements for PCEs > 25%.[128] With optimized band alignment and band bending at the front of the device, the front surface recombination can be suppressed even when the FSRV is high ($1x10^5$ cm-s^{-1}). Under these conditions the carrier lifetime requirement to reach 25% PCE can be relaxed from 100 ns to 25 ns. The hole density requirement, though, remains unchanged at $p_{CdTe} > 2 \times 10^{16}$ cm^{-3}. Front contact engineering simulations have been extended to wider bandgap II-VI alloy devices with similar conclusions.[99, 129] The common finding in these studies is that a well-designed front emitter/absorber interface must repel holes but still allow electrons to flow.[31, 99, 128, 129]However, the studies focusing on optimization of the emitter/absorber interface largely ignored the role of the back contact, and assumed flat band conditions and a back surface recombination velocity (BSRV) of 1×10^5 cm-s^{-1}.

While today's back contacts are not likely performance limiting, back barrier heights for ZnTe, which is the commercial contact,[130] was reported to be between 0.3 and 0.5 eV.[131, 132] Efforts to use other so-called back buffer layers[84, 92, 113, 133-138] have resulted in values ranging from 0.15 – 0.3 eV,[131, 132, 135] but the

understanding of how these back buffer layers actually operate is quite limited.[113, 139] Here, we investigate the operation of the absorber/back buffer interface and explore designs to minimize recombination at the back of the device, in a manner that is analogous to the engineering that was done to optimize the emitter/absorber interface.[31, 99, 128, 129]

7.2 Model Description

Simulations were carried out using the SCAPS-1D software developed at the University of Gent.[140] Devices consisted of a 300 nm n-type transparent F-doped SnO_2 front contact, a 100 nm MZO emitter layer, a 2 μm CdTe absorber, and a 100 nm back buffer layer. A 2 μm absorber thickness was chosen because it absorbs 98% of the above bandgap AM1.5 spectrum while minimizing the amount of CdTe in the device to reduce costs. To isolate the role of the absorber/back buffer interface, flat band conditions between the back buffer and back contact were assumed, and the surface recombination velocity at this interface was set to 1 x 10^5 cm-s^{-1}. The key material parameters, except where noted, were obtained from the literature, and are presented Table 7.1.

Table 7.1: Material parameters Used for SCAPS 1D Simulation

Parameter	**TCO**	**Emitter-MZO**	**CdTe**	**Back-buffer**
Thickness (nm)	300	100	2000	100
Band gap (eV)	3.6	3.7	1.5	vary
χ (eV)	4.45	4.2	4.4	vary
Relative dielectric constant	9	10	9.4	9.4
N_C (cm^{-3})	2.2 x 10^{18}	2.2 x 10^{18}	8.0 x 10^{17}	8.0 x 10^{17}
N_V (cm^{-3})	1.8 x 10^{19}	1.8 x 10^{19}	1.8 x 10^{19}	1.8 x 10^{19}
Mobility e/h (cm^2/Vs)	50/25	100/25	320/40	320/40
Lifetime e/h (ns)	0.1/0.1	1/10^{-3}	25	0.1/0.1
Doping density (cm^{-3})	n: 5x10^{20}	n: 1x10^{17}	p: 2x10^{14} - 2x10^{16}	p: 2x10^{14} - 1x10^{21}
Interfaces	**TCO/MZO**	**MZO/CdTe**	**CdTe/Back-buffer**	
S_n, S_p (cm/s)	N.A.	10^5	10^0 – 10^5	

The 3.7 eV band gap of the MZO layer was chosen to provide a +0.2 eV CBO, and the FSRV was 1 x 10^5 cm-s^{-1}, both consistent with front surface optimizations performed by others.[31, 128] Following this earlier work, we also assumed Gaussian type mid-gap defects states. A lifetime of 25 ns for both holes and electrons in the absorber was assumed, in good agreement with measured values for CdTe.[40, 124, 125] We initially fixed the BSRV at the absorber/back buffer interface to 1 x 10^5 cm-s^{-1}, but this value was also varied where noted. Except for the relative conduction and valence band positions and the hole density values, material parameters for the back buffer layer were set to those used for CdTe, including the introduction of mid-gap defect states. We note that the trends presented here are generally true for other lifetimes, and data for a lifetime of 1 ns is presented in the Supporting Information.

For ease of discussion, consider the non-interacting band diagram in Figure 7.1. We use a sign convention for the absorber/back buffer interface that defines a positive band offset as meaning that carriers (both holes and electrons) moving in their respective band must go to higher potential energy to exit the absorber and enter the back buffer. Therefore, a positive conduction band offset (CBO) indicates that the conduction band of the back buffer is higher in energy than the conduction band of the CdTe, while a positive valence band offset (VBO) indicates that the valence band of the back buffer is lower in energy than the valence band of the CdTe. Likewise, we can consider that the Fermi levels in the CdTe and the back buffer may be at different energies before the materials are brought into contact. If the Fermi level in the back buffer is initially below the Fermi level in the CdTe absorber, the initial Fermi level offset (IFLO) is defined to be positive. Note that this definition is consistent with the idea that majority carrier holes must move

to higher energy to flow out the back of the device. For purposes of simulation, we assume that the positions of the conduction and valence bands and the doping level in the back buffer can be arbitrarily adjusted.

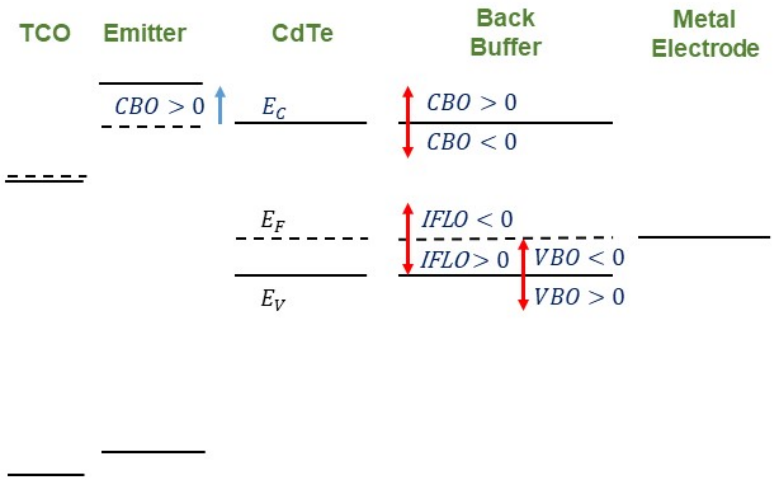

Figure 7.1 Sign convention describing the band alignments for the non-interacting layers in the device structure. The conduction and valence band offsets at the CdTe/back buffer interface (CBO and VBO, respectively) are defined to be positive when holes in the valence band or electrons in the conduction band experience a potential energy barrier in moving from the CdTe into the back buffer. The initial Fermi level offset (IFLO) follows the same convention from the perspective of the majority carrier holes. A positive IFLO means that the Fermi level in the back buffer is initially more negative than that of the CdTe. At the front of the device, the CBO emitter/absorber interface is considered to be optimized with a +0.2 eV barrier for electrons.

7.3 Results and Discussion

7.3.1 Role of Conduction and Valence Band Offsets

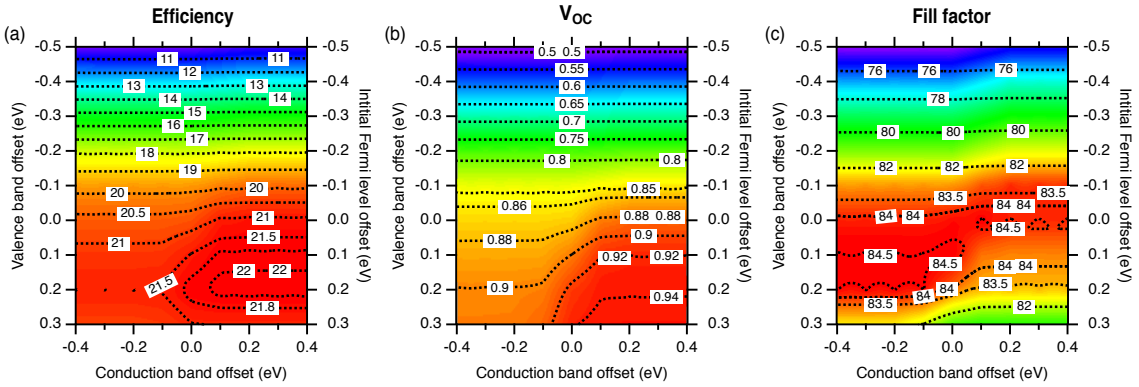

Figure 7.2 Contour plots of the photovoltaic (PV) parameters, (a) efficiency, (b) open circuit voltage (V_{OC}), and (c) fill factor as a function of the conduction and valence band offsets between CdTe and the back buffer. The right-hand axes show the initial Fermi level offset (IFLO) between the CdTe and buffer phases prior to equilibration. The doping in the buffer layer was fixed at p = 2 x 10^{14} cm^{-3}; the CdTe lifetime was set to 25 ns, and the BSRV at the absorber/back buffer interface was set to 1 x 10^{5} cm-s^{-1}.

To test our simulations, we start by determining how the CBO and VBO at the absorber/back buffer interface affect the device performance. Figure 2 shows the contour plots for V_{OC}, FF, and PCE as a function of the VBO and CBO at the CdTe/back buffer interface. The V_{OC} increases in a 1:1 fashion as the VBO becomes less negative independent of the value of the CBO until a value of approximately -0.2 eV is reached. The findings are similar to work by others where the VBO dependency was calculated with a fixed CBO.[114, 141] The V_{OC} begins to exhibit a dependency on the CBO when

VBO is greater than -0.1 eV, but the dependence is weak. This conflicts with other studies[30, 41, 142] that reported a stronger CBO dependence with a fixed VBO value. This discrepancy can be resolved by considering that the CdTe hole density we used is 2 x 10^{14} cm^{-3}, which is consistent with the value used in most simulations,[31, 68, 143] while reports of a strong CBO dependence used a much lower hole density, which leads to more strongly tilted energy bands (*vide infra*). Note that these conclusions are not significantly altered if a carrier lifetime of 1 ns is assumed (Figure 7.3).

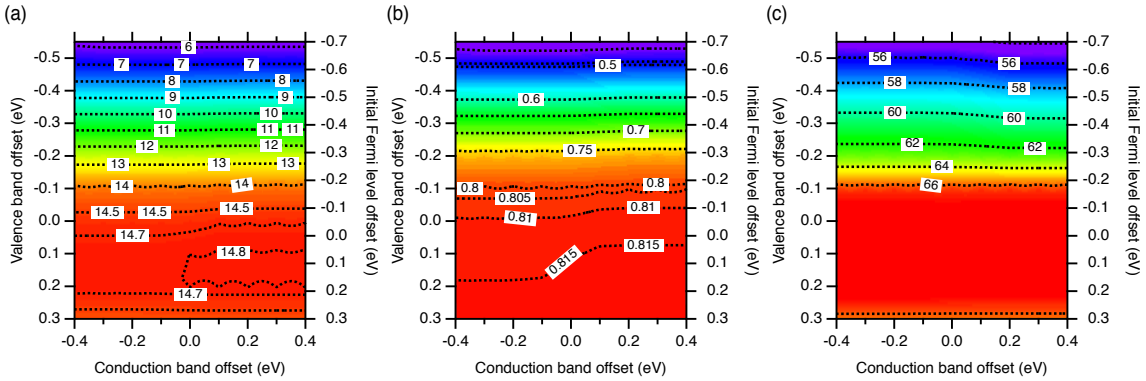

Figure 7.3 Contour plots of the photovoltaic (PV) parameters, (a) efficiency, (b) open circuit voltage (V_{OC}), and (c) fill factor, as a function of the conduction and valence band offsets between CdTe and the buffer layer with CdTe carrier lifetime of 1 ns.

Qualitatively, the findings can be understood by recognizing that there is a barrier to holes moving towards the interface even when the VBO is negative because of the local band bending in the absorber. The band bending that impedes holes from reaching the interface is decreased as the VBO moves toward zero. As the VBO becomes positive the slope of the band bending changes sign and holes are more efficiently transported to the back surface. Upward band bending continues to have a beneficial impact on V_{OC}

even when a valence band barrier at the interface is created. Positive VBOs start to block hole exit, which leads to poor transport and lower FF values. At an optimized VBO of +0.2 eV, a positive CBO further improves the V_{OC} due to the production of a barrier that assists in electron reflection. The FF also improves as the VBO becomes more positive until a large barrier for hole transport forms around 0.1 eV. The related physics will be discussed in more detail below. The PCE improves with both V_{OC} and FF, and values of 22.0% are achieved in the lower right portion of the figure.

7.3.2 Role of Back Buffer Doping and Initial Fermi Level Offset

In the previous example, the back buffer and absorber hole densities were the same, $p = 2 \times 10^{14}$ cm^{-3}. Because we assumed the same effective valence band density of states for both materials, the Fermi levels are at the same energy relative to their respective valence bands. For this special case, the initial Fermi level offset (IFLO) between the back buffer and CdTe phases is equal to the VBO. Figure 7.4 addresses the case of how the IFLO affects the device performance separately from the VBO. Here we examined three different IFLO cases (-0.2, 0.0, and +0.2 eV) with a fixed VBO of -0.2 eV (Figures 7.4(a) and (c)), and three different VBOs cases (-0.2, 0.0, and +0.2 eV) with a fixed IFLO of +0.2 eV (Figures 7.4(b) and (d)) . The IFLOs were set by adjusting the hole density in the back buffer (see Table 7.2).

Table 7.2: Hole density in the back buffer layer used to maintain initial Fermi level offsets (IFLOs) as indicated with $p_{CdTe} = 2 \times 10^{14}$ cm^{-3} for different valence band offsets.

Back buffer layer hole density (cm^{-3})			
	VBO = -0.2 eV	VBO = 0.0 eV	VBO = +0.2 eV
IFLO = -0.2 eV	2.0 x 10^{14}	-	-
IFLO = 0.0 eV	4.5 x10^{17}	-	-
IFLO = +0.2 eV	1.0 x10^{21}	4.5 x10^{17}	2.0 x 10^{14}

The CBO at the absorber/back buffer interface was fixed at +0.2 eV to ensure that the devices could access the highest efficiency region of Figure 7.2, which includes the possibility of forming an electron reflector. The front emitter/absorber interface was fixed in an optimized configuration, as described above. The simulated current density (J-V) and recombination current density (J_R-V) versus voltage curves, as well as the band diagrams at the maximum power point (MPP), are shown in Figure 7.4. We focus first on the case where the IFLO is varied for a fixed VBO of -0.2 eV (Figures 7.4(a) and (c)). Previous guidance suggested that a VBO of -0.2 eV on its own would yield high performance devices, but the possible role of doping in the back buffer and the resulting IFLO was not considered.[114, 141]

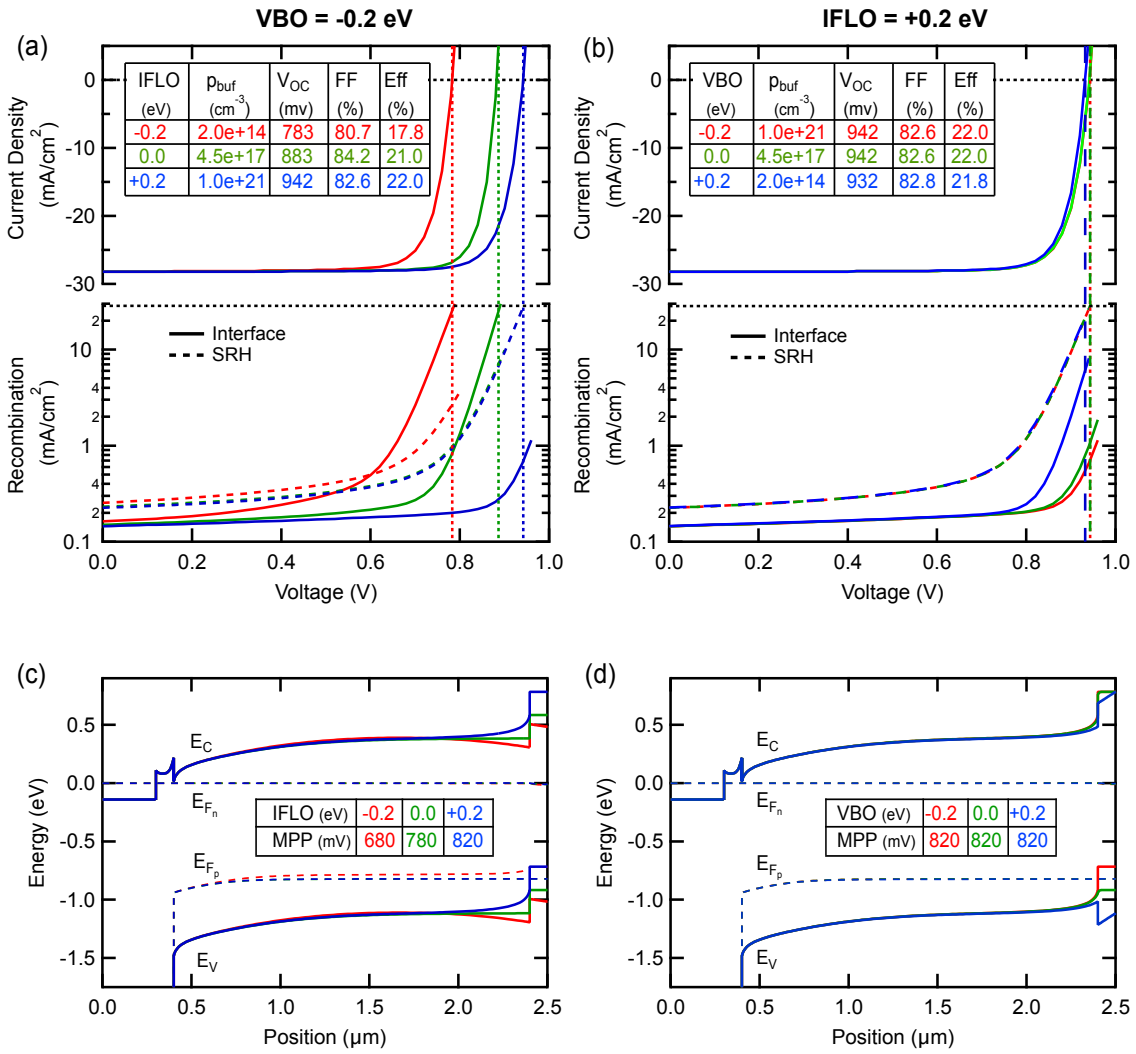

Figure 7.4 (a & b) Simulated J-V and J_R-V for CdTe devices where (a) VBO and CBO equal to -0.2 eV and +0.2 eV, respectively, and the back buffer layer hole densities were changed to produce IFLOs as indicated, and (b) both the CBO and the IFLO were fixed at +0.2 eV, but the VBO was adjusted by changing the back buffer hole density as indicated (see Table 1). (c & d) Band diagrams corresponding to (a) and (b), respectively, obtained at the maximum power point. The CdTe hole density was 2 x 10^{14} cm^{-3}, and the carrier lifetime was 25 ns.

As Figure 7.4 shows, the doping in the buffer and the resultant IFLO can have a significant effect on the device performance even when the CBO and VBO are fixed at values that have been reported to be near optimal. When the IFLO is -0.2 eV, the back buffer Fermi level is above the Fermi level in the CdTe prior to equilibration. Afterwards, band bending is created in both the CdTe and the back buffer. At the MPP, the CdTe valence and conduction bands bend downward in the region close to the back buffer interface. This local downward bending causes electrons to be attracted toward the interface and leads to an early turn-on of interface recombination as the bias is increased and the bands are flattened. This downward band bending also produces a barrier for holes moving in the band to exit the CdTe layer, which increases SRH recombination. The balance is such that the interface recombination turns on more rapidly with increasing bias, and thus it is the dominant recombination mechanism that limits V_{OC}.

When the IFLO is changed to be 0.0 eV or +0.2 eV, the bands are flat and upward bending, respectively, near the CdTe/back buffer interface at the MPP. For the case of IFLO = 0.0 eV, the onset of interface recombination is pushed to higher bias voltage and does not begin to increase significantly until a bias of ~0.7 V. The global band bending begins to flatten at about the same bias, which causes the SRH current to increase. At V_{OC} the interface recombination current is still ~3 times larger than the SRH current, so it still limits the V_{OC}, but at a significantly higher value. When IFLO = +0.2 eV the upward band bending at the back interface suppresses the interface recombination further, and the V_{OC} becomes limited by SRH recombination. These findings underscore the importance of back buffer doping and the IFLO and make it clear that the back contact can be limiting even when the VBO is -0.2 eV. Thus, the design of a high-performance back

contact is not simply a function of the valence or conduction band offsets, but strongly depends on the IFLO, which is a function of the doping level in the back buffer.

The data in Figure 7.4(b) and (d) illustrate the role that varying VBO can have when the IFLO is maintained at +0.2 eV. There is very little difference in the band bending in the CdTe at the back of the device, and the device performance of ~22% is nearly unaffected by the choice of VBO. With a positive VBO there is slightly less upward band bending at the interface, and a blocking barrier in the valence band landscape at the absorber/back buffer interface. This barrier leads to increased interface recombination current, but the V_{OC} values are all limited by SRH recombination. Interestingly, if the minority carrier lifetime is increased to 100 ns, all of these devices are still SRH-limited, but at an efficiency value of ~24% (Figure 7.5).

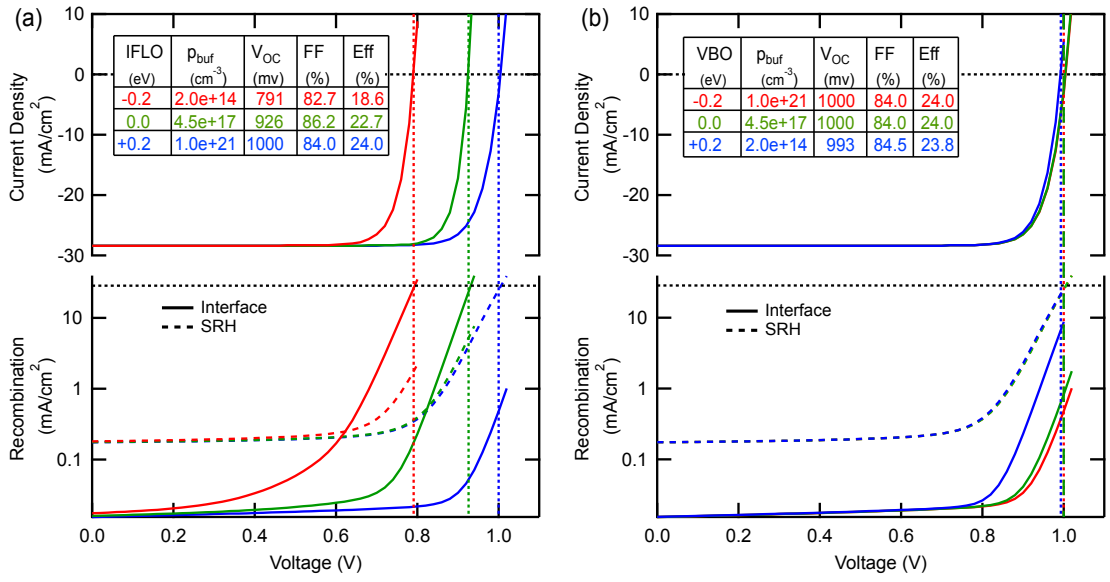

Figure 7.5 Simulated J-V and J_R-V for CdTe devices where (a) VBO and CBO = -0.2 eV and +0.2 eV, respectively, and the buffer layer hole densities were changed to produce IFLOs as indicate, and (b) both the CBO and the IFLO

were fixed at +0.2 eV, but the VBO was adjusted by changing the buffer hole density as indicated. The CdTe hole density was 2 x 10^{14} cm^{-3}, and the carrier lifetime was 100 ns.

Before moving on, we note that the short circuit current density (J_{SC}) is ~28.5 mA-cm^{-2} for all cases simulated here. While SCAPS is not set up to handle reflection losses and, thus, the calculation of J_{SC} with high accuracy, we note that an experimental J_{SC} value of 27 mA-cm^{-2} has been reported for a CdTe device with an antireflection coating.[33] This value is 95% of the simulated value, so our calculate PCEs, and the trends, are likely to be relevant to experimental devices.

7.3.3 Role of Absorber Doping

We next consider how an increase in the CdTe hole density will affect the IFLO and the device performance. CdTe hole densities of 2 x 10^{14}, 2 x 10^{15}, and 2 x 10^{16} cm^{-3} were chosen, and the hole densities in the buffer (p_{buf}) were chosen to be 2 x 10^{14} to yield negative IFLO values (Figures 7.6(a) and (c)) and 1 x 10^{21} cm^{-3} to yield positive IFLO values (Figures 7.6(b) and (d)). Note that increasing the p_{CdTe} for a fixed p_{buf} decreases the IFLO. The CBO and VBO values at the absorber/back buffer interface were fixed at +0.2 and -0.2 eV, respectively.

Figure 7.6 shows the resulting J-V and J_R-V curves as well as the band diagrams at the MPP for the negative (Figures 7.6(a) and (c)) and positive IFLO values (Figures 7.6(b) and (d)). Figure 7.6(a) shows large increases in the V_{OC} as the CdTe hole density is increased. Going from p_{CdTe} of 2 x 10^{14} cm^{-3} to 2 x 10^{15} cm^{-3} results in a V_{OC} increase of 148 mV, and another 66 mV is found when p_{CdTe} = 2 x 10^{16} cm^{-3}. The depletion region width at the CdTe/back buffer interface shrinks as p_{CdTe} is increased (Figure 7.6(c)),

which reduces the volume over which the minority carrier electrons are driven towards the back surface. This in turn reduces the np product near the interface and delays the onset of the interface recombination current to larger bias voltages. As shown in the J-V and J_R-V curves (Figure 7.6(a)), the downward band bending towards the interface produces devices that are performance-limited by interface recombination.

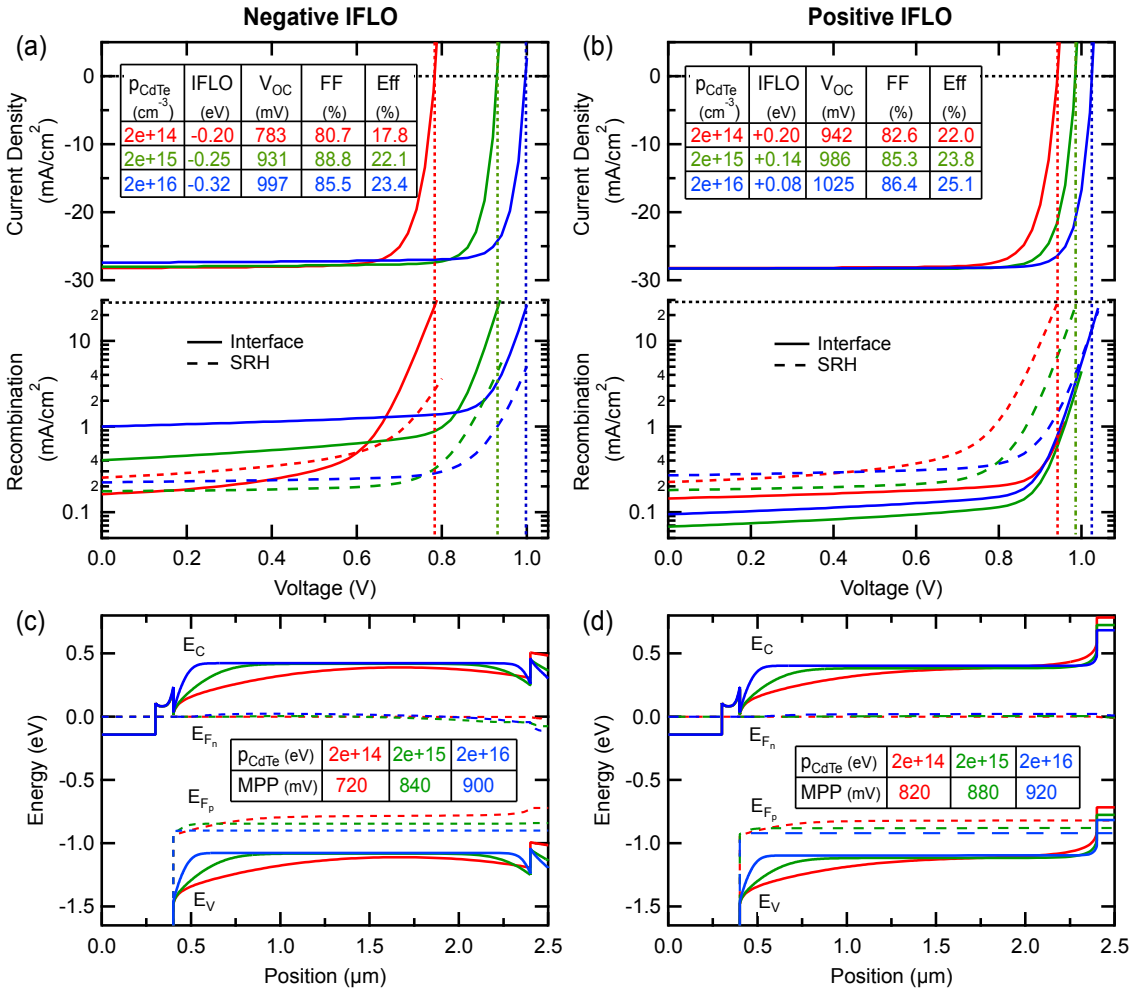

Figure 7.6 (a) & (b) Simulated J-V and J_R-V for CdTe devices where (a) the back buffer hole density is 2 x 10^{14} cm^{-3} ($E_{F,Buf}$ = -5.40 eV) and the absorber layer hole densities were changed to produce IFLOs as indicated, and (b), similar to (a), where the back buffer hole density is 1 x 10^{21} cm^{-3} ($E_{F,Buf}$ = -5.80 eV). (c)&

(d) Band diagrams corresponding to (a) and (b), respectively, obtained at maximum power point. The carrier lifetime is 25 ns and the VBO and CBO are fixed at -0.2 eV and +0.2 eV, respectively.

For positive IFLO values (Figures 7.6(b) and (d)), the bands slope upward near the CdTe/back buffer interface. Here, increasing p_{CdTe} from 2 x 10^{14} cm^{-3} to 2 x 10^{15} cm^{-3} leads to V_{OC} improvements on the order of only 40 mV, but the V_{OC} starts 159 mV higher when the IFLO is positive. The combination of a positive IFLO and an increasing CdTe hole density pushes the interface recombination current out to even larger biases. The photocurrent output of the device collapses very rapidly with bias as SRH recombination turns on abruptly when the bands are flattened. Note that the case where IFLO equals +0.08 eV approximates the flat band condition that was used to simulate 25% device efficiency by others.[122, 128]

7.3.4 Role of Back Surface Recombination Velocity

Investigations on front surface interface engineering have shown that the dependence of device performance on FSRV can be reduced when the band alignment at the emitter/absorber interface is optimized.[31, 128] To explore whether a similar statement can be made for the back interface we fixed the CBO and VBO at +0.2 and -0.2 eV, respectively, and varied the IFLO through adjustment of p_{buf} for three different values of p_{CdTe}. The BSRV was also varied to yield the efficiency contour plots shown in Figure 7.6.

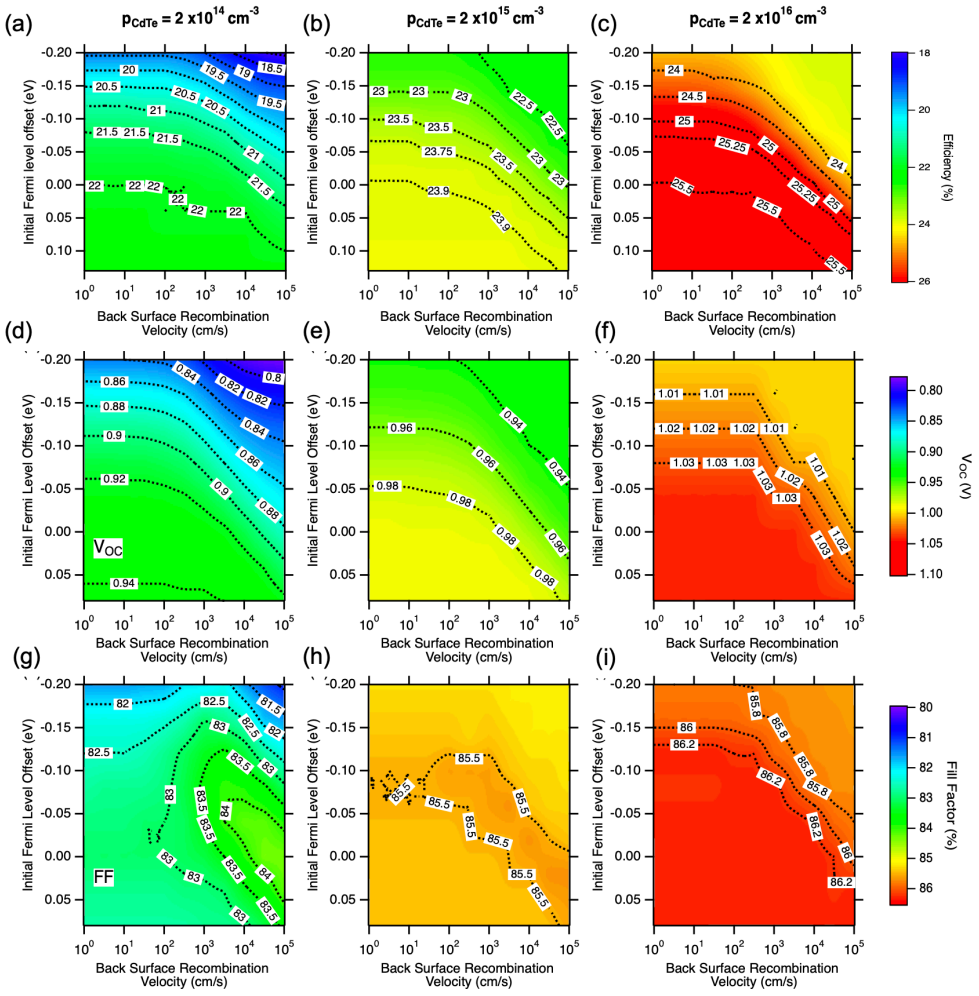

Figure 7.7 Contour plots of simulated device efficiency, V_{OC} and FF as a function of the IFLO between the CdTe and back buffer layers and the interface recombination velocity with p_{CdTe} equal to (a), (d), (g) 2 x 10^{14} cm^{-3}, (b), (e),(h) 2 x 10^{15} cm^{-3}, and (c),(f),(i) 2 x 10^{16} cm^{-3} .

For each value of p_{CdTe}, the highest efficiency portion of the plot is in the lower left corner. In general, the BSRV becomes less important as the initial Fermi level offset becomes more positive. As p_{CdTe} is increased the efficiency values increase, and, when p_{CdTe} is 2 x 10^{16} cm^{-3}, PCEs greater than 25% can be achieved with BSRVs as high as 1 x

10^5 cm-s^{-1} with an IFLO greater than 0.05 eV. This is because the higher hole densities in the absorber give rise to a collapsed space charge region and more band bending near the interface, as seen in Figure 7.6(d). Thus, management of the local band bending allows the back surface to become less sensitive to the BSRV values. Put differently, simply preventing the electrons from getting to the back surface reduces the need for a low BSRV, in direct analogy to findings for the front interface.[31, 128]

7.3.5 Relevance of Simulations to Actual Buffers

The simulations allow the properties of the optimized back buffer materials to be specified. For example, for the case of a CBO of +0.2 eV, which is sufficient to produce electron reflecting behavior for a positive IFLO, we can consider that an IFLO > 0.05 eV and VBOs ranging from -0.2 to +0.2 eV will result in devices that are SRH-limited and insensitive to the BSRV up to values of 1 x 10^5 cm-s^{-1}. In this case, the bandgap and hole density of the target buffer material can be determined using Figure 7.8.

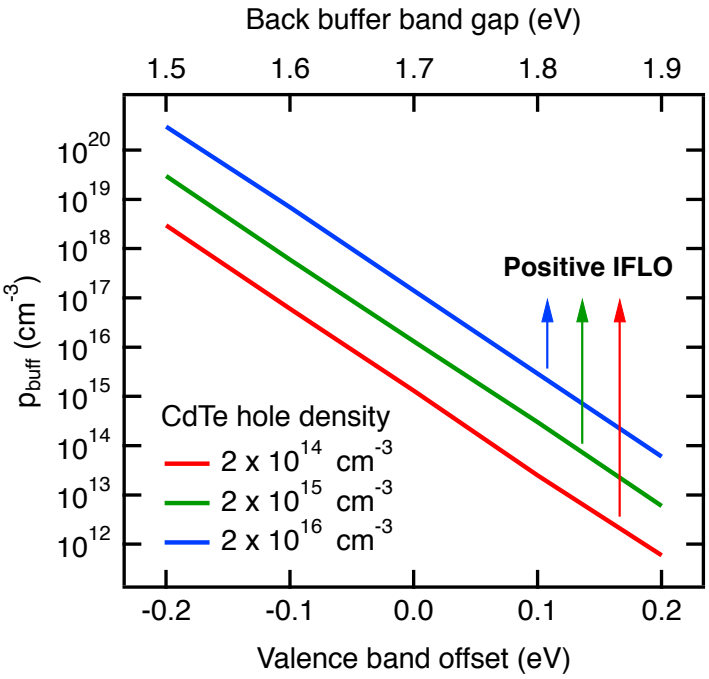

Figure 7.8 Conditions for forming a device with IFLO = 0.05 eV. The back buffer hole density is plotted as a function of VBO for CdTe hole densities of 2 x 10^{14}, 2 x 10^{15}, and 2 x10^{16} cm^{-3} with a fixed CBO of +0.2 eV. Points above the lines result in devices with IFLO > 0.05 eV. The top axis shows the corresponding band gap for each VBO value.

With Figure 7.8 as a guide, we can consider how the properties of real world materials compare to the desired values. Tellurium is a low bandgap materials that has been used as the back buffer in the highest efficiency devices reported in the academic literature.[64, 144] The hole concentration in Te is on the order of 10^{18} cm^{-3}, and the VBO between CdTe and Te is ~-0.3 eV.[113, 139] For p_{CdTe} = 2 x 10^{14} cm^{-3} these Te values result in an IFLO of approximately -0.15 eV. From Figure 7.2, we would expect an efficiency for this IFLO value to be ~19%, which is consistent with the highest

efficiency for a device with a Te buffer and a pure CdTe absorber, 18.3%.[144] The data in Figure 7.7 suggests that the device performance is most likely limited by absorber/back buffer interface recombination if the minority carrier lifetime was indeed relatively long (i.e., ~ 25 ns). To increase the device efficiency, the IFLO would need to be increased. Figure 7.8 suggests that the Te hole density would need to be on the order of 10^{20} cm^{-3} for the IFLO to be ~0.05 eV. Alternatively, the IFLO could be increased by decreasing the CdTe hole density. Neither option is likely. Additionally, as shown in Figure 7.2, the highest efficiencies in are inaccessible due to the negative CBO. The conclusions would be similar for other small bandgap materials that have been proposed, including SWCNTs[137, 138] and SnTe.[133] However, these materials could be employed to form a contact between a more suitable buffer layer and a metal.[135]

As Figure 7.9 shows, just adding the buffer layer improves device performance compared to when the metal directly contacts the CdTe layer. When the work function of the metal is 5.1 eV and the back buffer is included, the V_{OC} of the device increases by 211 mV, and the addition of the Te layer increases it by an additional 132 mV. When there is no buffer layer in this case, the bands bend downward, leading to a barrier to hole exit and attracting electrons towards the back of the device.

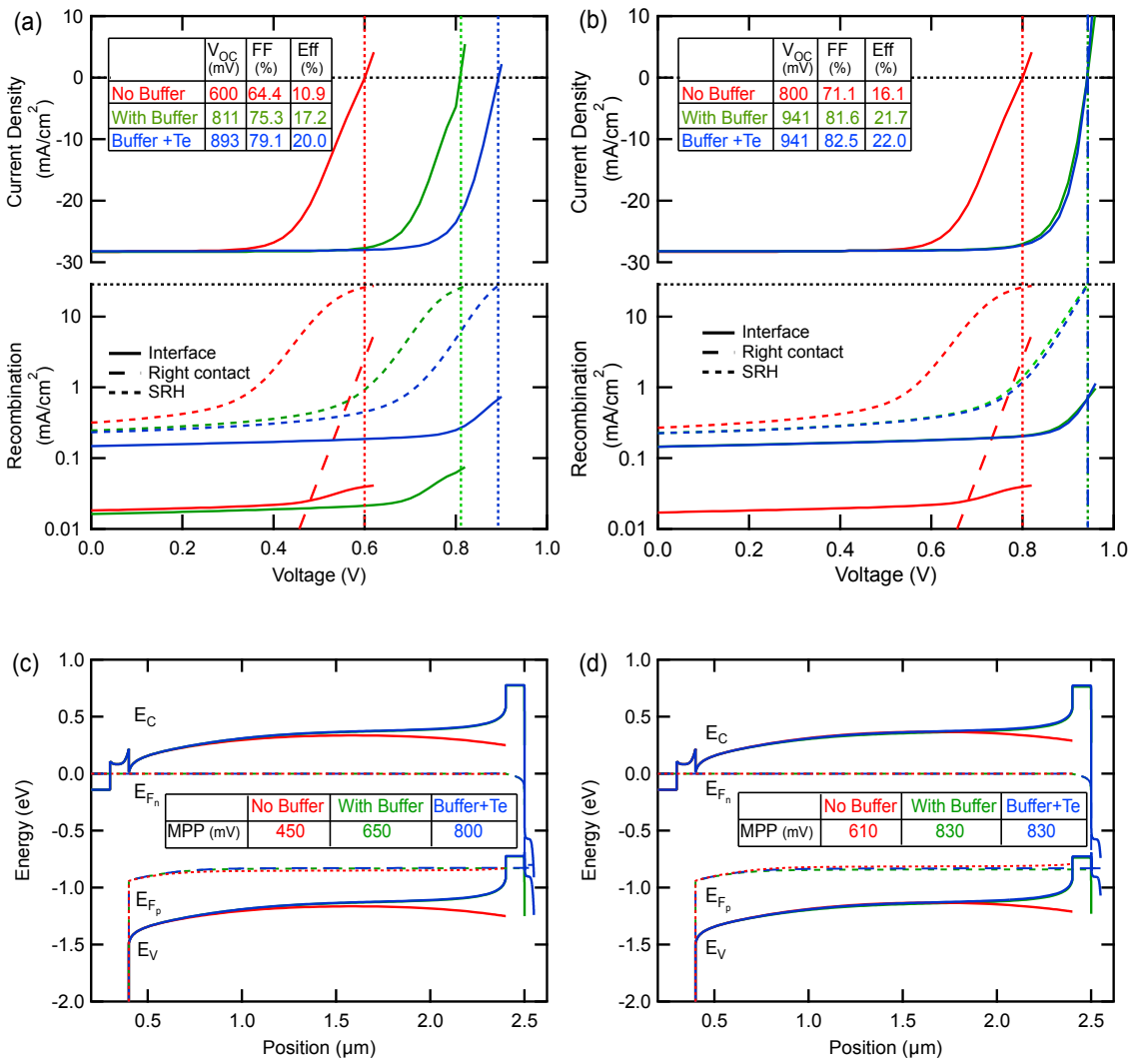

Figure 7.9 Simulated J-V and J_R-V for CdTe devices where the VBO and CBO = -0.2 eV and +0.2 eV, respectively, the buffer layer hole densities were fixed at 1 x 10^{21} cm^{-3} to produce an IFLO of +0.2 eV and the work function of the back metal is (a) 5.1 eV or (b) 5.3 eV. Each graph includes the same data when metal is in direct contact to the CdTe and when a Te buffer is used between the back buffer and the metal. The CdTe hole density was 2 x 10^{14} cm^{-3}, and the carrier lifetime was 25 ns.

These result in early onset of SRH recombination and significant recombination in the back contact, respectively. Combined, the leads to a low V_{OC}. When a single buffer is added, the band bending in the CdTe is now upward, allowing holes to flow into the buffer and repelling electrons. However, a large barrier exists between the buffer layer and the back contact, which leads to a sharp turn on of the SRH recombination at ~0.6 V. By adding the second buffer with a valence band edge and noninteracting Fermi level closer to the work function of the back electrode, the large barrier that formed between the buffer and the metal is divided over two interfaces. Two lower barriers pushes the onset of SRH recombination to higher bias voltages and increased device performance.[58] The same general results hold true when the metal work function is 5.3 eV. In this case, though, the band bending and barriers to hole flow are reduced, leading to better device performance.

ZnTe, on the other hand, has a 2.25 eV bandgap, forms a positive CBO with CdTe, and the valence band is thought to be close to that of CdTe.[84, 145, 146] It has been reported as a commercial buffer layer by First Solar.[130] However, recent experimental results measure a forward bias barrier height of at least 0.3 eV,[84, 131] suggesting a VBO of -0.3 eV. If this is the case, Figure 6 indicates that buffer hole densities on the order of 10^{19}, 10^{20} and 10^{21} cm^{-3} would be required to achieve an IFLO of +0.05 eV with $p_{CdTe} = 2 \times 10^{14}$, 2×10^{15}, and 2×10^{16} cm^{-3}, respectively. While ZnTe hole densities on the order of 10^{19} cm^{-3} may be achieved, which would yield a device with PCE near the current record value of 22.1%,[100] it is unreasonable to consider that the higher hole density values needed to reach higher PCEs could be realized. Thus, alternatives to ZnTe may be required to achieve 25% PCE.

Organo-metal halide perovskite layers have also been proposed as a back buffer layer and early results are promising.[136],[58] With a positive CBO and the ability to vary the bandgap predominantly through reduction of the valence band energy, this material system would appear to be an ideal candidate to fabricate the entire buffer layer stack. However, perovskite materials currently suffer from low doping densities[147-149] and material instability.[150]

Clearly, there are tremendous synthetic challenges associated with the development of the actual materials and, once developed, a next concern would be the maintenance/creation of the correct interface characteristics during, i.e., thermal processing. More research is needed in this important area.

7.4 Conclusions

We have performed simulations to comprehensively investigate the properties that would be needed for back buffer layers to facilitate reaching 25% PCE. Building on earlier work,[31, 122, 128] we considered incorporation of a back buffer layer and investigated the interplay between buffer and absorber doping and the conduction and valence band offsets. When the initial Fermi level of the buffer is below that of the CdTe the IFLO is positive and the conduction and valence bands of the CdTe bend upward towards the interface when the phases are equilibrated. This effect alone repels electrons and greatly reduces the interface recombination such that SRH-limited performance can be achieved. A positive CBO only becomes significant when the IFLO is positive and, together, these requirements enable devices to operate with >25% efficiency. These findings should be helpful in developing the next generation of high efficiency back contacts.

Chapter 8

Dissertation Summary and Future Work

8.1 Overall Summary

Work elaborated here consist of both experimental and numerical simulation that would set guidelines to fabricating high efficiency CdTe devices. Experimental work done here mainly uses closed space sublimation (CSS) as the deposition technique for the CdTe device fabrication. Deviating from the conventional understanding, dissertation focus on improving the device performance through increasing the solar cell photocurrent and reducing the loss mechanism that impedes the device performance.

Experimental work done in this dissertation first details the construction of a new CSS system that can be controlled using custom build LabVIEW program, characterization of the deposition parameters and finally achieving baseline device performance. Adapting the new understanding, wide bandgap MZO had been employed to the CdTe devices replacing the conventional CdS emitter. The goal was to suppress the interface recombination at the emitter-absorber interface through proper band alignment between the CdTe and MZO. Although the first attempt to fabricating the MZO/CdTe devices results poor performance, through 1D numerical simulation, work illustrates causes for degrading effects with the MZO/CdTe device structure and highlights the

significance of the material properties of MZO in order to achieve the full benefit of using such emitter. With lower carrier concentration in MZO, the detrimental effects to the FF was significantly impacting the device performance as the unfavorable Fermi level location in MZO causing a greater barrier to the electron transfer from CdTe to the front contact. Chapter3 focus on actions to mitigate this and improve the conductivity in the MZO layer, adapt new back contact processing to achieve PCE > 16% for MZO/CdTe devices.

In addition to achieving this device performance, the dissertation also explores methods to increase the photo-current generation through incorporating more transparent front contact such as cadmium stannate (CTO) on ultra-thin substrate. Later in the chapter5, dissertation explore the options to incorporate CdSe into device stack to increase the photocurrent generation, through selenization of CdS films.

Final two chapter in the dissertation focus on 1D numerical simulations to further improve the device performance. Extending some work done in literature, chapter 6 highlights the importance of TCO-emitter alignment for CdTe base devices. While this is not detrimental to current CdTe devices with existing TCO material, the CB location becomes extremely important to achieve high performance when the absorbers exceed 1.5 eV. Simulation highlights the range of properties for TCO that can be used in such devices and identifies that TCO CB edge should be not more than 0.3 eV.

While the first chapters focus on improvements to current collection and suppressing the front contact recombination, chapter 7 sets the guidelines to identifying a proper back contact stack for CdTe devices through simulation. The study explores the conduction and valence band offset between the CdTe and a back buffer layer and the

doping density requirements to achieve superior performance. Study also highlights the importance of the Fermi energy location and its alignment to reduce the barrier at the back contact. Results shows that, with CdTe doping $>10^{16}$ cm^{-3} and a buffer layer with Fermi level below the CdTe Fermi level could suppress the interface recombination at the back contact and device performance>25% can be achieved. While there are factors to consider for on difference between the theoretical 1D simulations and the real-world devices, this sets a guide to identifying back buffer layer materials that can be used to achieve high efficiency CdTe devices.

8.2 Future Considerations

This dissertation sets the path to several interesting future work that can easily be adapted and tested out.

8.2.1 Incorporation of CdSe to MZO/CdTe devices

The work in this thesis, extends only up to fabricating a 16% device using MZO/CdTe with a current density (J_{SC}) ~25 mA/cm^2. As described in several points in this thesis, incorporation of Se to CdTe absorber improves the current collection in the long wavelength region. With MZO as an emitter, adding Se to the absorbe would significantly increase the JSC further pushing the device performance to match higher the current best performing cells in field. This work would require to carefully optimizing the MZO bandgap that suits the $CdSe_xTe_{1-x}$ absorber at the front interface.

8.2.2 Cd_2SnO_4 as TCO for Wide Bandgap Absorber Devices

Following the simulation work done on TCO – emitter alignment, it would be interesting to apply this to practical use. Cd_2SnO_4 is shown to have an electron affinity of 4.2 eV[129, 151] and certainly would fit to make an excellent TCO material for absorbers like $Cd_{1-x}Zn_xTe$ or $Cd_{1-x}Mg_xTe$. Coupled with proper MZO bandgap should provide the means to fabricate devices that can be used as top cell for Tandem devices.

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Appendix A

List of Publications

1. Alaani, Mohammed A Razooqi; Koirala, Prakash; Phillips, Adam B; **Liyanage, Geethika K**; Awni, Rasha A; Sapkota, Dhurba R; Ramanujam, Balaji; Heben, Michael J; O'Leary, Stephen K; Podraza, Nikolas J; ,Optical Properties of Magnesium-Zinc Oxide for Thin Film Photovoltaics,Materials,14,19,5649,2021,Multidisciplinary Digital Publishing Institute
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8. Phillips, Adam B; **Liyanage, Geethika K**; Alfadhili, Fadhil K; Heben, Michael J; ,Understanding CdTe Performance with Engineered Front and Back Interfaces,2019 IEEE 46th Photovoltaic Specialists Conference (PVSC),0777-0782,2019,IEEE
9. Awni, Rasha A; Li, Deng-Bing; Song, Zhaoning; Bista, Sandip S; Razooqi, Mohammed A; Grice, Corey R; Chen, Lei; **Liyanage, Geethika K**; Li, Chongwen; Phillips, Adam B; ,Effects of Fabrication Atmosphere on Bulk and Back Interface Defects of CdTe Solar Cells with CdS and MgZnO Buffers,2019 IEEE 46th Photovoltaic Specialists Conference (PVSC),,,0177-0181,2019,IEEE
10. Alfadhili, Fadhil K; Phillips, Adam B; Jamarkattel, Manoj K; Snyder, Austin J; Gibbs, Jacob M; **Liyanage, Geethika K; Heben**, Michael J; ,Potential of CdZnTe Thin Film Back Buffer Layer for CdTe Solar Cells,2019 IEEE 46th Photovoltaic Specialists Conference (PVSC),0140-0143,2019,IEEE
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