A Thesis

entitled

Circuit Modeling and Performance Evaluation of GaN Power HEMT in DC-DC Converters

By

Krushal S Shah

Submitted to the Graduate Faculty as partial fulfillment of the requirements for the Master of Science Degree in Electrical Engineering

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An Abstract of

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The power generated by renewable sources such as solar photo-voltaic (PV) arrays and wind turbines is time varying and unpredictable. In order to minimize the wastage of power obtained from such sources, there is a great need of efficient power converters which are compact and can effectively manage power in Smart Grid applications. The design of such power converters would require the use of new semiconductor materials, novel device structures, improved switching and control circuits, and advanced packaging technologies. Wide bandgap materials are promising for RF/microwave and power switching electronics. Among these materials, III-V Nitrides - especially Gallium Nitride (GaN), and Silicon Carbide (SiC) are heavily investigated by industry because of their superior electrical and thermal properties, and improved radiation hardness compared to the standard semiconductor material -silicon.

A smart DC microgrid suitable for high-penetration in commercial applications and that efficiently utilizes energy available from distributed, renewable generators is described. GaN HEMTs based converters should be incorporated in the DC microgrid. It

is shown that the proposed DC power distribution system can produce savings in excess of 10-15% over the current approach that uses inverters.

Performance evaluation between silicon MOSFET and GaN HEMT is presented for chip-scale and maximum peak power tracking DC-DC power converter applications. The current circuit model available for GaN HEMTs does not converge for converter topology. Thus circuit calculations are based on improved circuit model for the FET with accurate description of capacitances and thermal on-resistance. It is shown that GaN power HEMTs used in a synchronous buck converter topology (for a $19/1.2V_{DC}$, 7.2W) can potentially lead to nearly 77 % power conversion efficiency at 25°C when switched at 5 MHz. However, results show that the current formulation for loss calculation in the topology described is erroneous and so there is a need of new loss formulation and device selection criteria based on circuit dynamics and device parameters.

Similarly simulations were carried out for a DC-DC boost converter topology ($200/380V_{DC}$, 10kW) and it has been shown to have 93 % power conversion efficiency at 25°C when switched at 1 MHz. But using new semiconductors materials like GaN HEMT and SiC in this case causes high *dv/dt* stress on switch and diode during switching which may cause failure of device.

Dedicated to all my Family members

Acknowledgements

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Moreover I am indebted to my parents and siblings whose love and confidence in me helped me complete Graduate studies with relative ease.

I would also like to thank Nextek Power system esp. Laing Downey and John Jahshan for providing valuable information about DC microgrid and DC ballast for testing.

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List of Abbreviations

EPRI.....Electric Power Research Institute
FET .....Field effect transistor
GaN.....Gallium Nitride
HEMT .....High electron mobility transistor
MOSFET.....Metal oxide semiconductor field effect transistor
NREL .....National Renewable Energy Laboratory
PHEV .....Plug In Hybrid Electric Vehicles
POL.....Point of load
Si .....Silicon
SiC.....Silicon Carbide

List of Symbols

C_{DSO} ..... Zero bias drain to source capacitance,
C_{GDO} ..... Zero bias gate to drain capacitance,
C_{ISS} ..... Input Capacitance at Zero Bias for FET
C_{JO} ..... Juntion Capacitance at zero Bias for diode
C_{OSS} ..... Output Capacitance at Zero Bias for FET
C_{RSS} ..... Transfer Capacitance at Zero Bias for FET
D..... Duty cycle
f_s ..... Power switching frequency
I_D ..... Drain current,
I_O ..... Output current,
m ..... Grading coefficient
PB ..... Built-in voltage
Pcon..... FET conduction loss,
Pgd ..... Gate drive loss
Poss ..... FET output switching loss
Psw..... Input switching loss,
Q_{GS} ..... Gate to Source charge before the FET turns on
Q_{oss} ..... Output charge
$R_{DS(ON)}$..... ON-resistance between drain to source
R_L ..... Load resistance
R_{NOM} ..... normal resistance at room temperature T_{NOM} (25^0C)
R_s..... Series Resistance for diode
T_{C1} ..... Temperature coefficient 1
T_{C2} ..... Temperature coefficient 2
t_{off} ..... FET turn-off time
t_{on} ..... FET turn-on time
V_{BR} ..... Reverse Breakdown Voltage
V_{DS} ..... Drain to Source Voltage
V_F ..... Forward Voltage Drop for diode
V_{GD} ..... Gate to drain voltage,
V_{in}..... Supply voltage

V_o ..... Output voltage
V_{TH} ..... Threshold Voltage
ΔV_o ..... Output ripple voltage

Preface

In Chapter 1, smart, low-cost and efficient DC microgrid ideally suited for local utilization of electricity generated from renewable energy sources such as the solar photovoltaics (PV) arrays and wind turbines. The proposed DC power distribution architecture is easily scalable to residential, commercial and community-level applications; and simple, first-order calculations are presented to estimate the energy and cost savings feasible when distributing energy generated from a 50 kW solar PV array to power typical residential and commercial DC-compatible loads. It is shown that more than 10% energy may be saved by replacing the current inverter-based solar PV utilization approach with the proposed DC power distribution system. Since there is no inverter involved, the DC power system also results in significant cost savings with improved reliability. Further improvements in energy efficiency and reliability are feasible by embedding sensor-based control and power management.

In Chapter 2, performance enhancement possible for point of load converters based on GaN HEMT device is presented. Circuit model for GaN HEMT and silicon MOSFET is developed to compare the performance of devices in DC-DC converter topology. All the factors affecting the device performance in converter is discussed in detail.

In Chapter 3, efficiency improvements feasible from advanced DC-DC power converters based on emerging GaN HEMTs is presented; circuit simulations of a

200/380V_{DC}, 10 kW boost converter have yielded an efficiency of 93% using emerging GaN power FETs. Further improvement in efficiency is feasible with more improved GaN power FET designs and power control techniques. The thesis concludes with specific recommendations on new challenges that need to be addressed and new technologies that need to be developed in order to render the proposed DC micro-grid.

Chapter 1

Introduction

The established US electrical utility infrastructure was conceived more than 100 years ago and is vulnerable and relatively inefficient when compared to distributed generation [1]. Distributed generation avoids both the vulnerability of transmission and distribution links and nodes and the 6.5% transmission and distribution losses. The advent of semiconductor electronics and the recent rapid growth of renewable energy technologies, such as solar photovoltaic (PV) and wind turbines, are dramatically changing the nature of transmission, distribution and utilization of electrical energy. Most of today's electrical loads—lighting, adjustable-speed motors, brushless DC motors, and computing and communication equipment—are more compatible with DC power [2]. Most distributed renewable energy generators (DREGs)—including solar PV, wind, fuel cell, rectified high-frequency alternator outputs on micro turbines or flywheels, batteries, and ultra-capacitors— produce DC voltage. Thus DC power has great potential for increased compatibility with high-penetration, distribution-connected solar PV and other DREGs. Today's solid-state switching DC-DC converters that transform DC from one

voltage level to another have power conversion efficiency in the range of 95%. At the point of use, converter or rectifier losses are avoided by using DC power, averaging approximately 30% savings across all internal and external power supplies [3]. Thus, the two primary factors that gave AC the advantage over DC 100 years ago have been eliminated. As a result, new opportunities and challenges are presented for efficient and low-cost local utilization of renewable energy using a DC power distribution system.

Large electrical grids are based on AC for two important reasons. First, changing voltage is simple and cheap; this allows energy to be transported over long distances at high efficiency and relatively low cost. Second, AC motors and generators are more cost-effective than DC counterparts. However, for a localized application such as residential or commercial usage with a large DC power source such as a solar PV array, it is actually more cost-effective to use a local DC power distribution system for DC loads such as lighting and a local AC grid for the remaining AC loads [2]. This is because changing DC to AC is relatively expensive and inefficient, while regulating DC or changing AC to DC is both cheap and efficient. Inverters for converting DC to AC are quite complex; DC regulators for DC-to-DC conversion are relatively simple; and AC-to-DC rectifiers are extremely simple. Therefore, it is quite easy to import both DC and AC power into a DC power distribution system but relatively difficult to import DC power into an AC grid.

Tremendous improvements have been made during the past decade in the efficiency and cost effectiveness of solar PV technology, but relatively little advancement has occurred in methods for converting PV electricity into a usable form [4]. Instead of taking a fresh look at the best ways to utilize distributed PV energy, most applications simply force it to conform to a system that was designed for centralized generation. For

example, inverters are invariably used to convert the DC energy from the PV to AC energy before it is applied to the load. Unfortunately, DC-to-AC inversion is an inherently complex and expensive process, and the efficiency can range as low as 85%. Furthermore, overall system reliability is significantly affected and is often limited by the inverter. Voltage inversion is also totally unnecessary if a large DC load is in close proximity to the PV installation. There are several examples where this is the case, three of the most prevalent being lighting, HVAC, and computing/ communication used in residential and commercial buildings.

1.1 DC loads

Since the introduction of semiconductor in consumer products, electronics devices have become integral part of lifestyles of masses. There is growth in appliances having computing and internet connectivity which is all DC powered after processing. There is also growth in DC LEDS lighting in place of incandescent lights [3].

1.1.1 DC lighting (LEDs lights v/s incandescent bulbs) and DC Fans

The LEDs light are gaining popularity day by day and promoted by companies like GE etc. LED lights have advantages over incandescent lights in terms of operational life, cost and energy saving. The operational life of current white LED lamps is 100,000 hours in contrast to the average life of incandescent light which is approximately 5000 hours. Thus LEDs can be installed at places which not easily accessible, and can avoid routine bulb replacement

The true cost associated with lighting includes the cost of installation and replacement of the bulb. The overall cost of LEDs comes to significantly lesser than incandescent bulbs.

The key strength of LED lighting is reduced power consumption. When designed properly, an LED circuit will approach 80% efficiency, which means 80% of the electrical energy is converted to light energy. The remaining 20% is lost as heat energy. Compare that with incandescent bulbs which operate at 20% efficiency while 80% of the electrical energy is lost as heat [5].

DC powered fans developed are powered by 12/24 V_{DC} and can be easily interfaced DC distribution [6].

1.1.2 DC Powered Datacenters (Servers) and Power Supply Unit

Another important commercial and residential load is the IT based equipment's like personal computers, laptops, SMART phones, etc. and servers to provide world wide web to store data. The Lawrence Berkeley National Laboratory (LBNL) has estimated that the total amount of energy flowing into external power supplies for electronic devices in the U.S. is about 290 TWh/year [7]. Out of these around 13 % of power was consumed by servers in datacenters excluding power requirement for cooling. Thus a significant amount of power is required by datacenters. The current AC distribution deployed commercially is less efficient and thus generates lots of heat. The U.S. Environmental Protection Agency (EPA) and the DOE's Energy Star program estimates that one-third to one-half of the power sent to these devices is lost as heat. This ultimately

means that around 100-150 TWh/year are currently being lost in these conversions. Thus it is essential to efficiently utilize this power. Figure 1-1 shows the AC configuration to represent the typical set-up found in today's data center, taking $480V_{AC}$ from the utility feed, and stepping it down to $208/120V_{AC}$ for input to AC-powered servers. UPS used here to condition the input signal and provide constant AC output to servers. Battery bank is also connected to provide uninterrupted power source to load. To integrate the power from renewable sources inverter is used to convert the DC power generated into AC; to power servers. The overall efficiency of existing system would be around 61%; whereas using best in class UPS and power supply unit increases efficiency to about 79%.

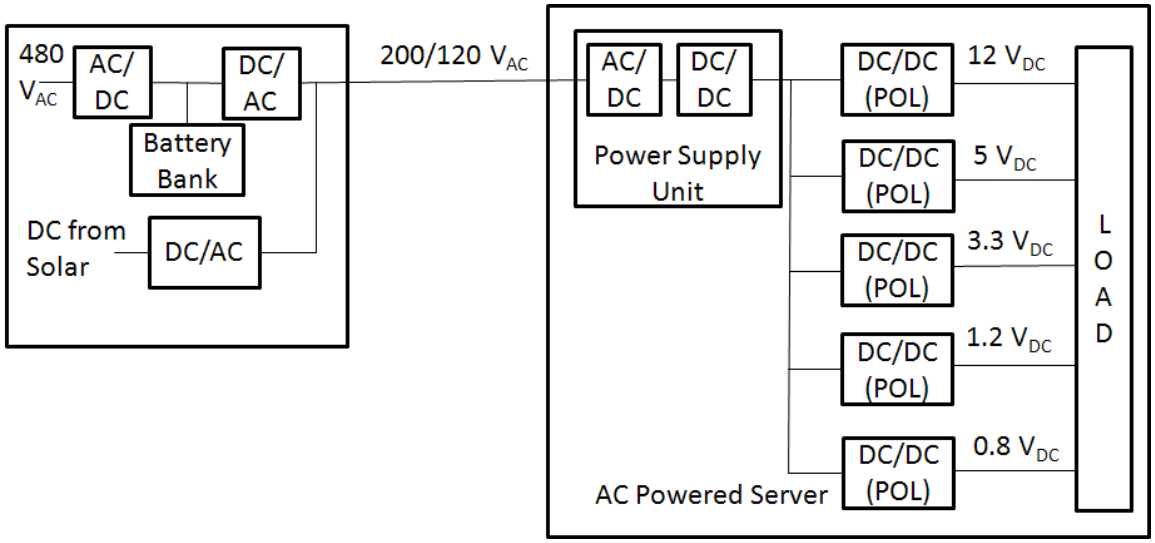


Figure 1-1: Current AC based data center set-up, delivering 208/120VAC input to AC-powered servers.

Figure 1-2 shows DC Distribution system implemented by LBNL in which DC distribution was used instead of AC. The input voltage was converted into DC using UPS (Rectifier) to 380 V_{DC} to power DC- powered servers. In this layout the only power conversion before the server takes place through one rectifier. Inside the server power supply, only one DC/DC conversion occurs. In addition to the reduction in losses, this arrangement is inherently simpler, which will should lead to lower equipment cost, lower installation cost, and higher system reliability due to lower parts count. The measured efficiency of such system came out to be around 87 %; which means 26% improvement in system efficiency in comparison with existing data centers layout. And around 8% gain in system efficiency in comparison with the best in class AC system. The integration of renewable energy can be more efficient using DC/DC converter in comparison with inverter. Thus DC system is more efficient and cost effective in comparison with AC system in case of powering servers in data centers. Even the device-like computer, laptops, mobile phones, etc. require DC at point of load in power supplies. Thus directly powering them DC in contrast to AC would reduce the conversion steps and improve system efficiency [7].

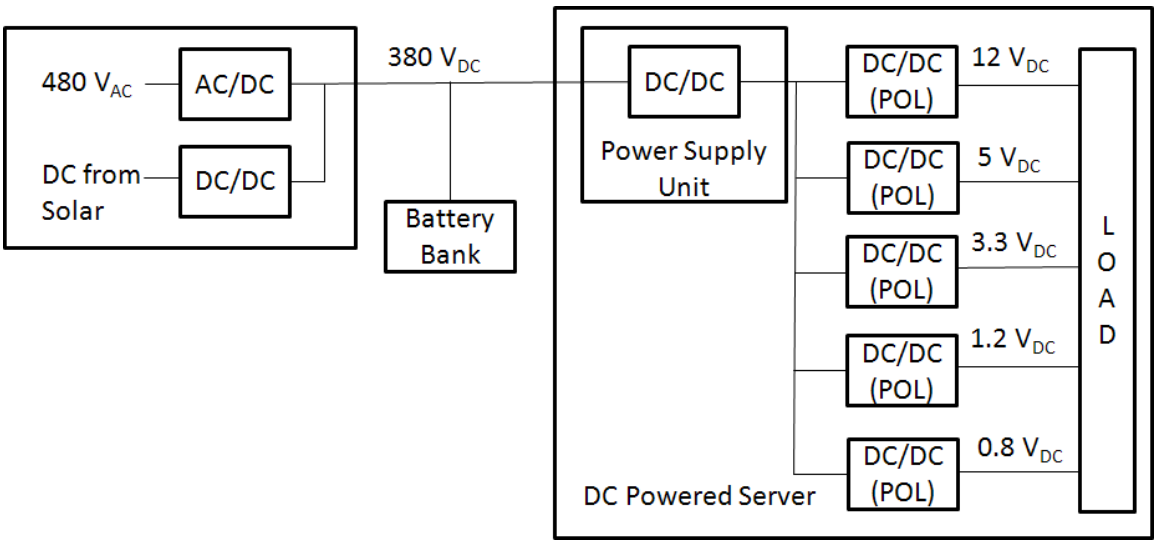


Figure 1-2: DC based data center set-up, delivering 380VDC input to DC-powered servers.

1.2 AC Distribution for Microgrid

The existing AC power system is meant for distributing utility-scale AC power generated at a remote site for household, commercial, and industrial applications. However, energy generated from renewable sources such as solar PV and wind is generally DC and can be made available locally at the application site [4]. Figure 1-3 illustrates today's power distribution system employed for local utilization of DC electricity generated from a 50 kW solar PV array to power electrical loads including a computer server and building loads such as ceiling fans, lighting, laptops, desktops, HVAC, and others. A maximum peak power tracker (MPPT) with an efficiency as high as 97% is used to optimally extract electricity generated from the solar PV panel; it is then inverted and used to power local AC loads. Excess solar PV energy, if any, is fed back to the utility AC grid. As shown in Figure 1-1, the computing server uses $240V_{AC}$, and hence requires AC-DC-AC conversion

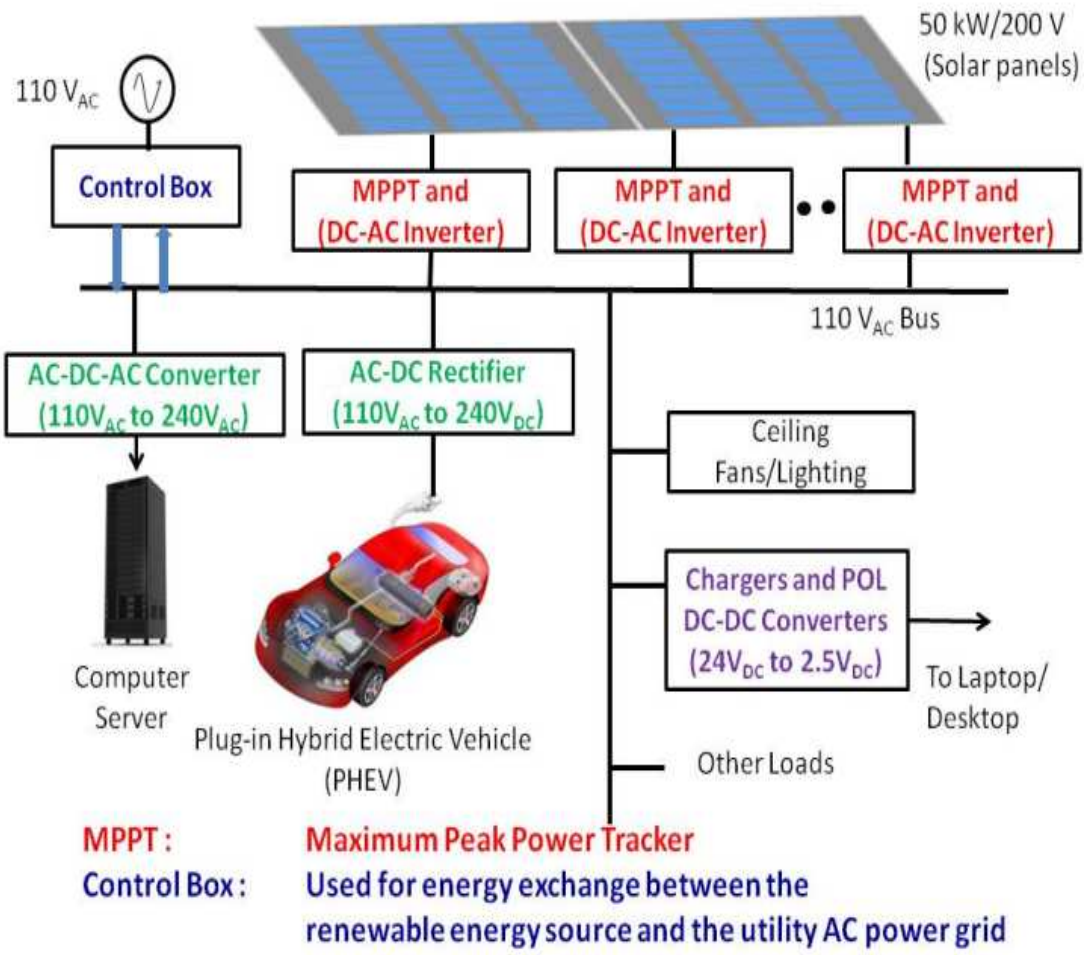


Figure 1-3: Schematic representation of current distributed energy integration approach using inverters.

Likewise, a high-voltage AC-DC rectifier is used to deliver 240V_{DC} power to charge plug-in hybrid electric vehicles (PHEVs). Within the building, AC-DC battery chargers are used to deliver point-of-load (POL) DC power to low-voltage loads such as laptops, desktops, and cell phones [8][9][10][11]. The battery chargers used in mobile OEM devices, the so-called "vampires," are power-hungry and, typically have an efficiency in the range of 65% to 80% [12]. A simple calculation suggests that the power system shown in Figure 1-3 results in about 70% to 75% efficient usage of electricity generated from the 50 kW solar PV array for local utilization; the rest of the electrical

energy is lost in various power conversion stages. The efficiency calculations are tabulated in Table 1-1 using the best commercially available silicon-based rectifiers, inverters, and DC-DC converters [13][14][15][16][17].

1.3 DC Distribution for Microgrid

Several new approaches are being developed for direct DC utilization of electricity generated from renewable energy sources [18][19][20][21]. In one approach, AC power from the utility grid is rectified and integrated with the DC electricity produced from renewable energy sources [18]. In another approach $380V_{DC}$ electricity is first developed from the renewable energy source and is used to power internet data center servers and PHEVs [7][19][20]. Figure 1-4 illustrates our proposed smart DC power distribution system for direct DC utilization of the electricity generated from the same 50 kW solar PV array. In the proposed DC power system, a $300V_{DC}$ power bus is first developed and is used to provide continuous DC power to the computer server; a $380V/240V_{DC}$ DC-DC converter charges the PHEV when needed. A $24V_{DC}$ power distribution line is developed to provide DC power to loads such as fans, lighting, computers, and other DC-compatible loads. To minimize the distribution power loss, loads will have to be located within 10 meters from the point of generation of $24V_{DC}$. As a result, multiple $380V/24V_{DC}$ DC-DC converters are needed in order to generate a number of $24V_{DC}$ buses. As shown in Figure 1-5 the proposed DC power distribution system results in about 85% to 87% efficient usage of electricity generated from the 50 kW solar PV array for local utilization when the solar PV energy is directly utilized to power local DC-compatible electrical loads. The total power was categorized as 70% residential use, 20 % PHEVs and 10% data

servers and the saving was calculated using off the shelf converters performance. Efficiency of these individual DC-DC converters is shown in Figure 1-5. Based on the calculated efficiency for GaN HEMT based converters (3-4% more than commercial silicon based converters), saving with advanced converters was proposed. Table 1-1. shows the energy and cost saving using DC system. It also shows additional saving of energy using advanced converters designed using GaN FET. As before, in estimating this efficiency improvement, we have used data based on the best commercially available silicon-based MPPTs and DC-DC converters [21]. Figure 1-5 shows comparison of energy saving by using GaN HEMTs based converters. The 24-volt DC standard is actively promoted by the EMerge Alliance [22]. The state-of-the-art DC-DC power converters are hybrid, bulky, costly, and very inefficient. In order to meet the stringent requirements (efficiency, cost and reliability) of emerging DC Grid applications, in this study GaN HEMT based converters are evaluated.

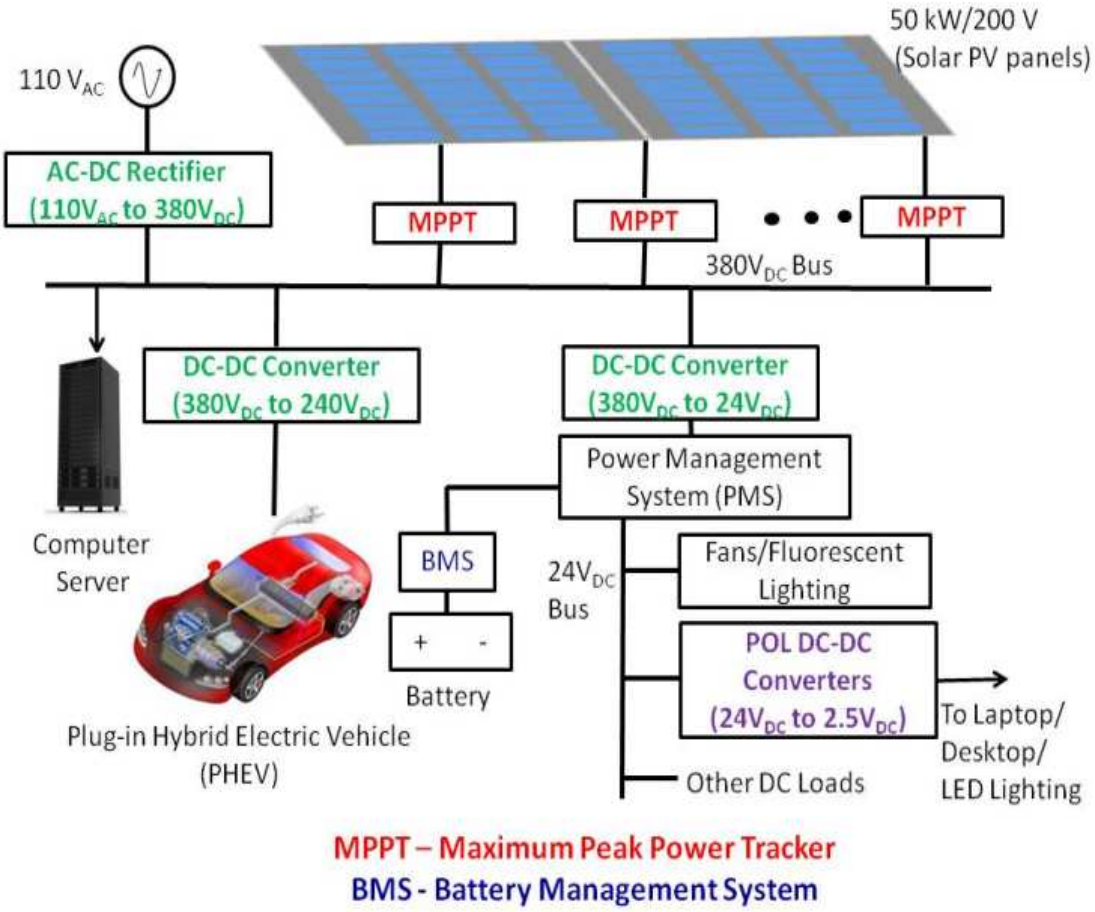
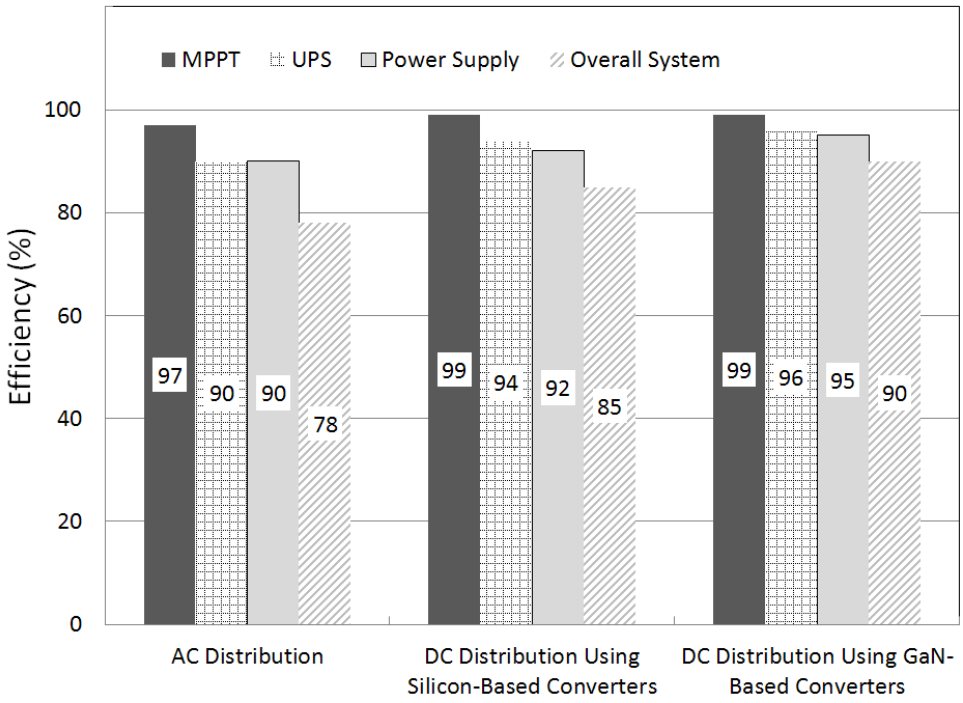


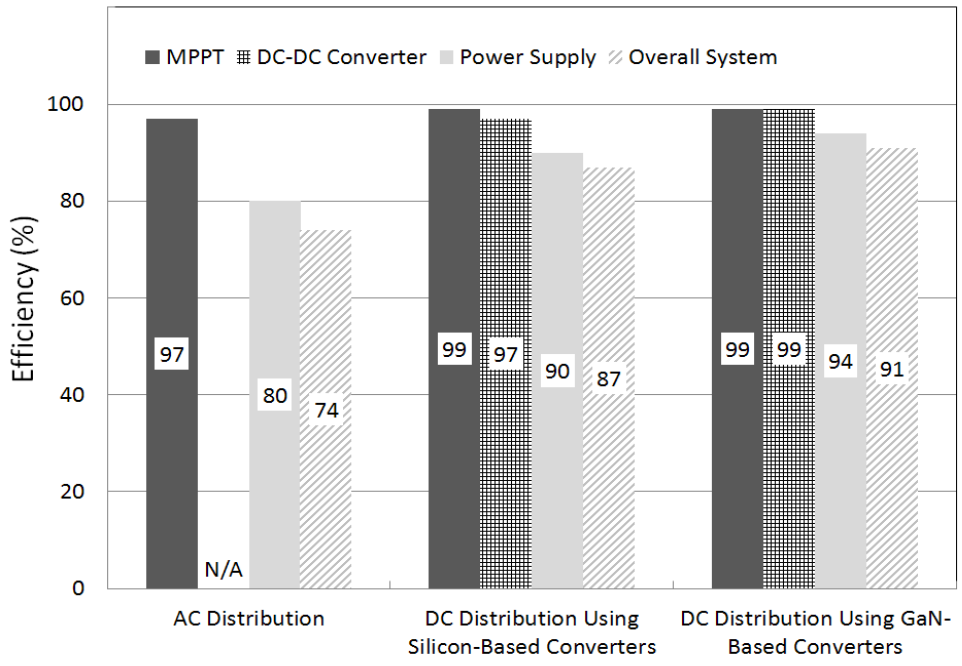
Figure1-4: Schematic representation of the proposed smart DC power distribution system for efficient local utilization of the electricity generated from the solar PV array

Table 1.1: Overall power savings in the proposed 50 kilo-watt dc power grid shown in Figure 1-4 using commercial silicon power converters and proposed advanced Gallium Nitride FET-based power converters

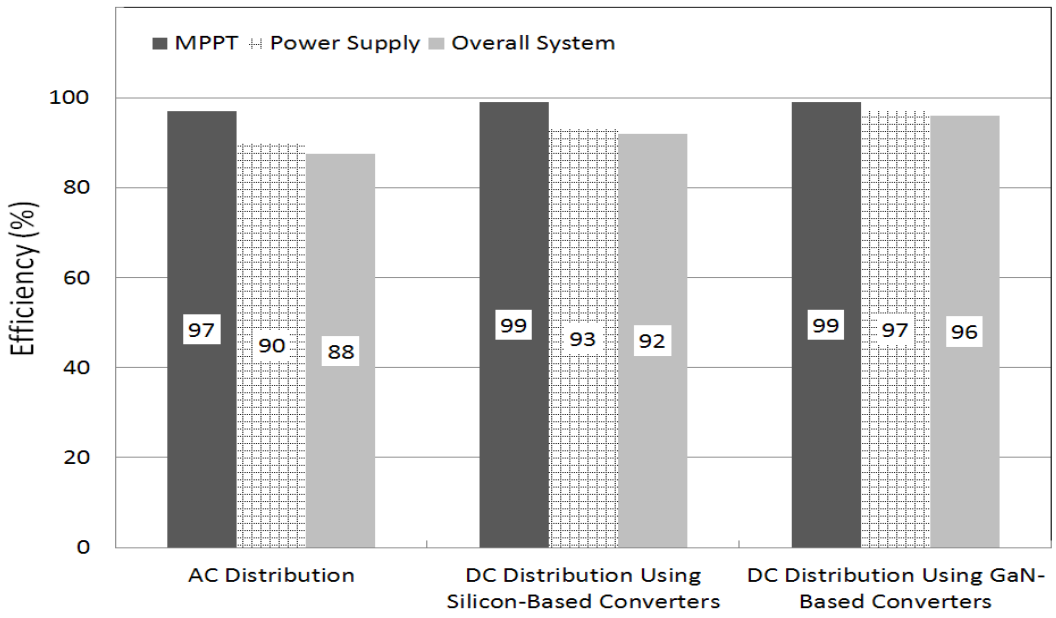
Electrical Load	**Power Usage (kW)**	**Energy Saving Using Commercial Silicon Power Converters (kW)**	**Cost Saving using DC Distribution and by Using Commercial Silicon Power Converters ($)**	**Energy Saving Using Proposed GaN-based Power Converters (kW)**
Building Electrical Loads	35	5.25	5,000	6.65
PHEVs and other loads	10	0.45	1,000	0.85
Computer Server	5	0.35	800	0.60


MPPT
UPS
Power Supply
Overall System
Efficiency (%)
100
80
60
40
20
0
97
90
90
78
99
94
92
85
99
96
95
90
AC Distribution
DC Distribution Using Silicon-Based Converters
DC Distribution Using GaN-Based Converters

(a)


MPPT
DC-DC Converter
Power Supply
Overall System
Efficiency (%)
100
80
60
40
20
0
97
N/A
80
74
99
97
90
87
99
99
94
91
AC Distribution
DC Distribution Using Silicon-Based Converters
DC Distribution Using GaN-Based Converters

(b)



(c)

Figure 1-5: Calculated Efficiency of various components and overall Power Grid for different kind of loads such as (a) Computer Servers (b) Laptop/Desktop (c) PHEVs as well as other loads.

1.4 Need of advanced DC-DC Converters

The DC microgrid discussed here and energy calculations are based on 50 kW system. The same approach can be used for individual small houses where load requirement is quite less (around 2-3KW). To integrate solar into such system less number of DC-DC converters would be required. Since the space in such houses would be limited such converters needs to be compact and efficient. The state-of-the-art DC-DC power converters are hybrid, bulky, costly, and very inefficient [4]. In order to meet the stringent requirements (efficiency, cost and reliability) of emerging Smart Grid applications, there is a critical need for chip-scale efficient DC-DC power convertersand compact converters for MPPT tracking. Miniaturization of DC-DC power converters can

be accomplished by high-frequency (> 1 MHz) switching of power semiconductor devices so that magnetics and capacitors can be integrated with the semiconductor power switch and control/switching circuitry. However, high-frequency power-switching results in increased power loss and degraded reliability, and often requires application of advanced cooling and thermal management technologies with diminishing returns. Besides, conventional silicon power devices have reached material limits in performance and reliability. Thus there is a need for integrated power converters which are built using efficient GaN power FETs. In Chapter 2 and Chapter 3 two DC-DC converters(Buck and Boost) are discussed in detail.

Chapter 2

Evaluation of Synchronous Buck DC-DC Converter

Typical low-voltage electrical loads include desktops, laptops, phones, digital cameras, and other OEM devices [10]. Battery chargers are used to charge mobile devices; efficiency of 12-19V_{DC} battery chargers is typically in the range of 70% to 80%. One recent study conducted estimates that in California alone, these so-called "vampires" consume nearly 20% of the electricity used; consequently, new regulations on battery charger efficiency are mandated [12]. Several POL converters are used inside the OEM device to provide power to low-voltage microchips [10]. The efficiency of these POL converters ranges from 50% (for a low dropout regulator or LDO) to 90% (for a hybrid switch-mode power converter or SMPC); the POL converters provide regulated low-voltage (1V_{DC} to 5V_{DC}) power from the 12-19V_{DC} battery. For example, in a high-end cell phone, nearly 30% of the device cost and size arise from the battery power management circuitry; and, nearly 30% of the battery energy is wasted in the power management circuitry. Further miniaturization and efficiency improvement of battery power management circuitry are of paramount importance.

In this Chapter GaN based high electron mobility transistor (HEMT) devices are studied in terms of performance improvement compared to state of art silicon devices in

synchronous buck DC-DC converter topology [23][24][25]. In order to perform first hand calculations and analyze the device performance in circuit before building it; circuit simulations are required. Since GaN HEMTs are fairly new in industry; not much work is carried out towards accurate and simple circuit simulation models of FETs. The desirable feature of a circuit simulation model is its simplicity and ease with which the model parameters can be extracted. The total number of components that constitute the model must be kept to a minimum to improve the simulation efficiency of complex systems.

The available circuit model from EPC is built using complex curve fitting equations for current-voltage and capacitance-voltage characteristics of HEMTs [26]. When this model was used for simple synchronous DC-DC converter and boost converter, there were convergence problems. The model cannot be used for studying effect of FET on circuit dynamics. Thus there is need of simple circuit model for studying effect of GaN HEMTs in circuits at higher frequency.

2.1 Synchronous DC-DC Buck converter Test Circuit

We have chosen a synchronous buck converter topology for this study to provide regulated power from a $19V_{DC}$ battery to a $1.2V_{DC}$ load as it applies to a wide range of POL converters. The synchronous buck converter circuit shown in Figure 2-1 offers the highest conversion efficiency for a non-transformer isolated DC-DC converter at the power level considered; this circuit is also easily scalable for chip-scale integration [26][27][28][29].

In this circuit, the high-side switch Q_1 charges the inductor (L) when it is turned on; the low-side switch Q_2 provides the freewheeling path for the inductor when the high-side switch is turned off. The low-side FET switch Q_2 is operated as a diode in the third quadrant (a synchronously switched rectifier); gate drive is optimized to provide zero deadtime so that freewheeling diode is not required [30].

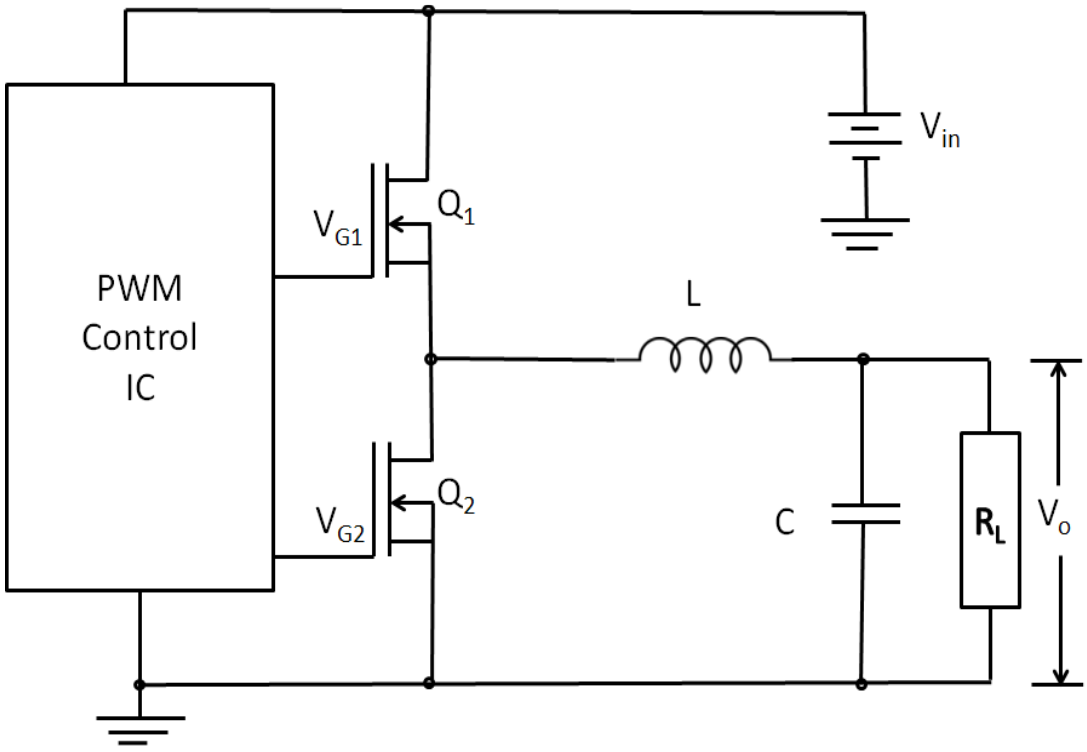


Figure 2-1: Circuit schematic of a synchronously switched DC-DC buck converter

The minimum inductor value needed to maintain continuous current conduction as a function of switching frequency, and a corresponding capacitor value for the desired output ripple are calculated using standard closed form expressions (2.1) and (2.2) [31] [32]:

$$L_{min} = \frac{D.(V_{in}-V_o)}{2.I_o.f_s} \quad (2.1)$$

$$C = \frac{(1-D)}{8.f_s^2.L.(\Delta V_o/V_o)} \quad (2.2)$$

In this study, the semiconductor switches, PWM control IC, and the inductor are assumed to be the only elements in the circuit with losses. The circuit and packaging, parasitic, and stored charge in semiconductors are neglected. The duty cycle is slightly adjusted to obtain the desired converter performance.

2.2 Tradeoff between Gallium Nitride (GaN) Power HEMT structure and Silicon Vertical Structure

Different Silicon and GaN HEMTs devices were used as high and low FET in synchronous buck converter.The Silcion and GaN HEMT structure studied are shown in Figure 2-2 and Figure 2-3. The Silicon MOSFETs are mostly vertical device and current conducts through the bulk region[33]. Whereas GaN HEMTs are basic GaN-on-Si based device, based on the presence of a two-dimensional electron gas (2DEG) spontaneously formed by the intimacy of a thin layer of AlGaN on a high quality GaN surface as shown in Figure 2-3. This device is basically a field-effect transistor (FET) with an induced high electron mobility channel between the drain and source electrodes; this device can be made to conduct current in the absence of any applied voltage to the gate electrode ("normally ON") or by the application of a gate voltage ("normally OFF") by careful engineering of material layers using the principle of bandgap engineering [23][24].

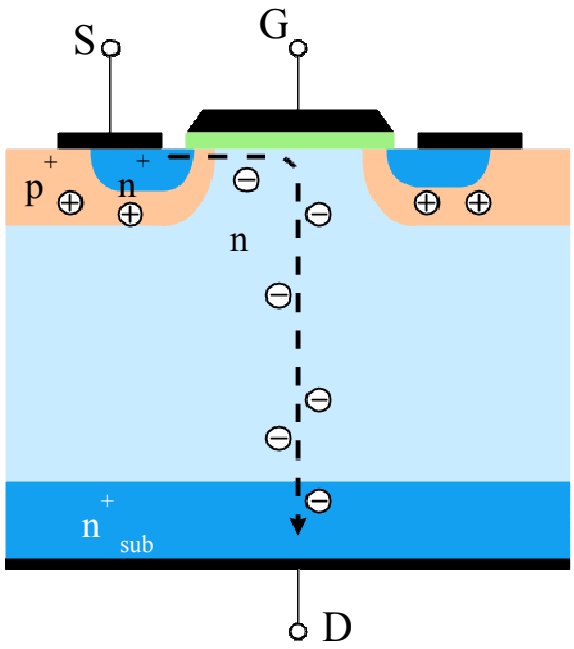


Figure 2-2: Schematic cross section of a Silicon MOSFET

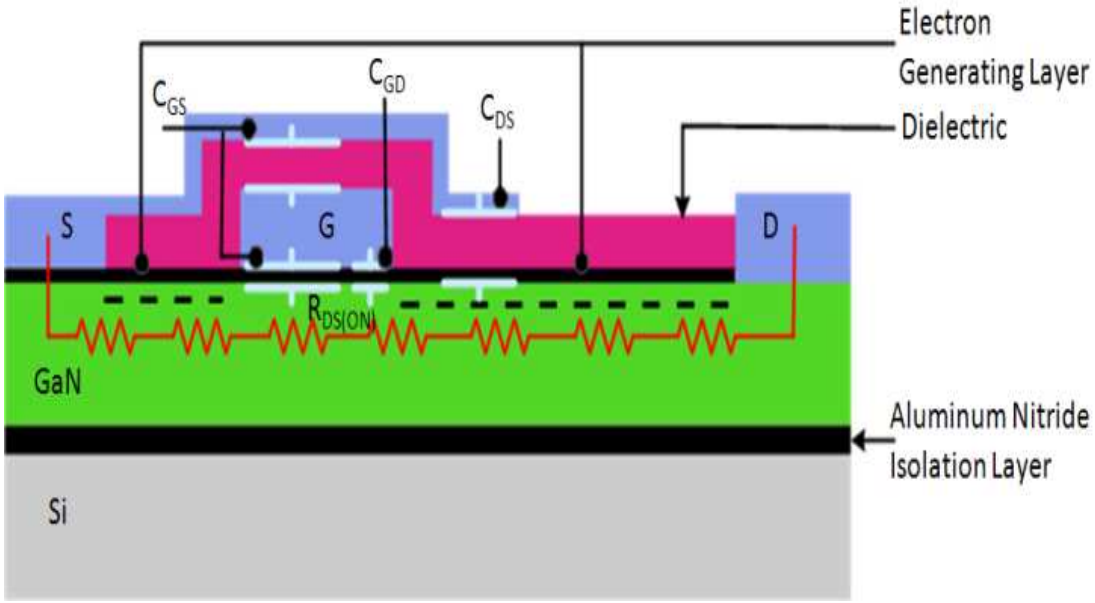


Figure 2-3: Schematic cross section of a GaN power HEMT

The main advantage of using GaN HEMT is there is body didoe associated with it and gate charge is very less as compare to silicon MOSFET. The Capacitances and resistances associated with GaN HEMT are less than silicon power MOSFET as shown in Table 2-1. Thus GaN HEMT based converters can be switched at higher frequency.

2.2.1 Dynamic on resistance problem in GaN HEMTS

In GaN HEMT there is problem of electron getting trapped near channel region and it may cause decrease in drain current and increase in on resistance. These Dynamic on-resistance also known as “current collapse”, causes degradation of device performance. The magnitude of “current collapse” is strongly dependent on the electric field at the gate-edge where electrons can be accelerated. A virtual gate electrode is formed by electrons trapped in the AlGaN/dielectric interface where they charge up the surface states. This can result in a reversible degradation of drain current. Electrons can also be trapped in the AlGaN barrier layer itself or in the GaN buffer layer below [34] .

The device design improvements using gate and source field plates are an effective way to reduce the electric field thereby suppressing the increase in on-state resistance as well as gate leakage degradation. In addition, better confinement of electrons in the potential well and overall improvement in the material quality of AlGaN/GaN epitaxial layers are important to combat dynamic on resistance. EPC has taken steps in material growth, device design, and process optimization to minimize the potential device degradation mechanisms. Thus the devices used in study has been tested for dynamic on resistance in field [34].

2.2.2 Comparison of Parameters of Commercial Silicon MOSFET and GaN HEMTs

Table 2-1 lists the FET parameters used for the design of a 19V/1.2V, 7.2W SB DC-DC power converter for GaN HEMT and Silicon MOSFET. These parameters for the best commercial devices were extracted from the data in order to fit the circuit models. The commercial devices were selected such that the design was optimize to provide better performance for high side and low side FETs. The high side FET used in case of GaN HEMT was rated 40V/10A, whereas in case of silicon MOSFET from Vishay [35][36]. Since the duty ratio of converter is very low (less than 7%), low side switch is conducting most of time. To reduce the conduction loss, FET with high die area was used. Thus GaN HEMT with rating 40V/33A was used and in case of silicon, MOSFET from Infineon was used for simulations[37][38]. The circuit arrangement ensures that the body diode of the silicon power MOSFET is never turned ON.

Table 2.1: Comparison of important FET parameters used in design of 19/1.2V_{DC}, 7.2 W SB DC-DC converter

Device	V_{BR} (V)	V_{TH} (V)	I_D (A)	$R_{DS(on)}$ (mΩ)	C_{ISS} (nF)	C_{OSS} (nF)	C_{RSS} (nF)	Q_G (nC)
Best Commercial Silicon MOSFET (High Side)	40	1.2	20	22	0.75	0.57	0.22	4.9
GaN HEMT (High Side)	40	1.4	10	16	0.32	0.3	0.06	3
Best Commercial Silicon MOSFET (Low Side)	30	1.6	40	4.3	5.1	4	0.8	27
GaN HEMT (Low Side)	40	1.4	33	4	1.3	1.2	0.22	11.6

2.2.3 Size of Magnetics and Capacitors

The sizes of magnetic components and capacitors in the circuit vary inversely with frequency; hence higher switching frequency is desired for converter miniaturization. The main advantage of using the GaN FET for power switching is that switching frequency can be kept high (>5 MHz) while still maintaining lower conduction power loss (compared to a silicon power MOSFET with identical rating); this can reduce capacitor and inductor values exponentially as shown in Figure 2-4. Thus, by using wide band gap materials converters can be made more compact, hence facilitating chip-scale power integration at increased power ratings [27].

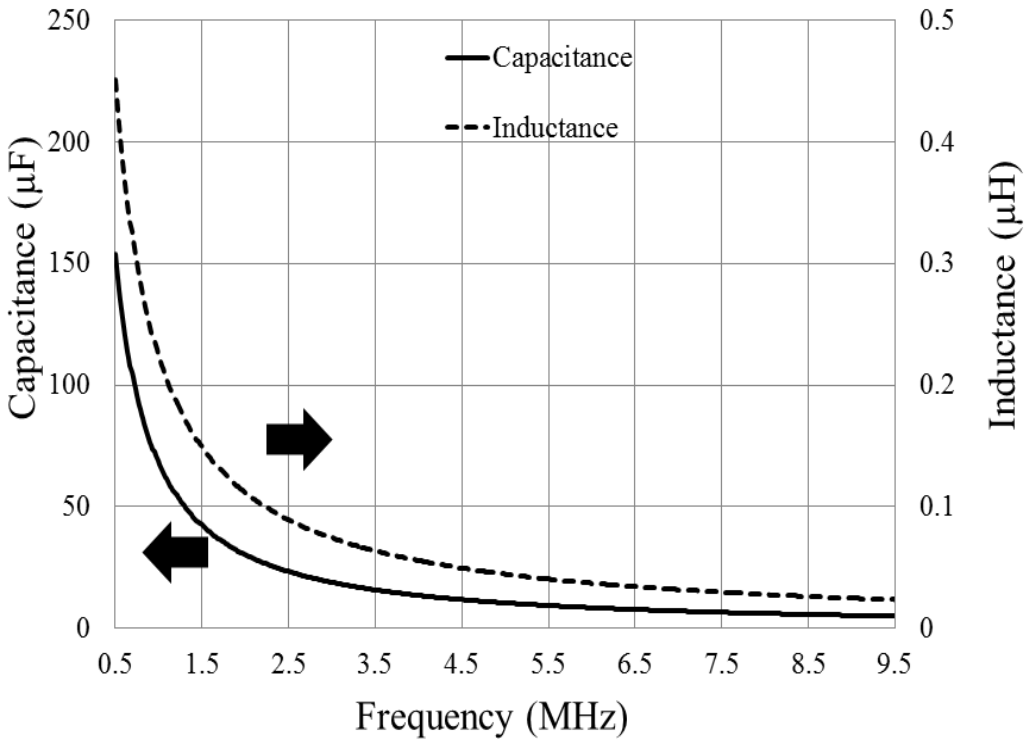


Figure 2-4: A plot of calculated Inductor and Capacitor values vs. Frequency for a 19V/1.2VDC, 7.2W synchronously switched DC-DC buck converter

2.3 Circuit Model for Silicon MOSFET and GaN Power HEMT

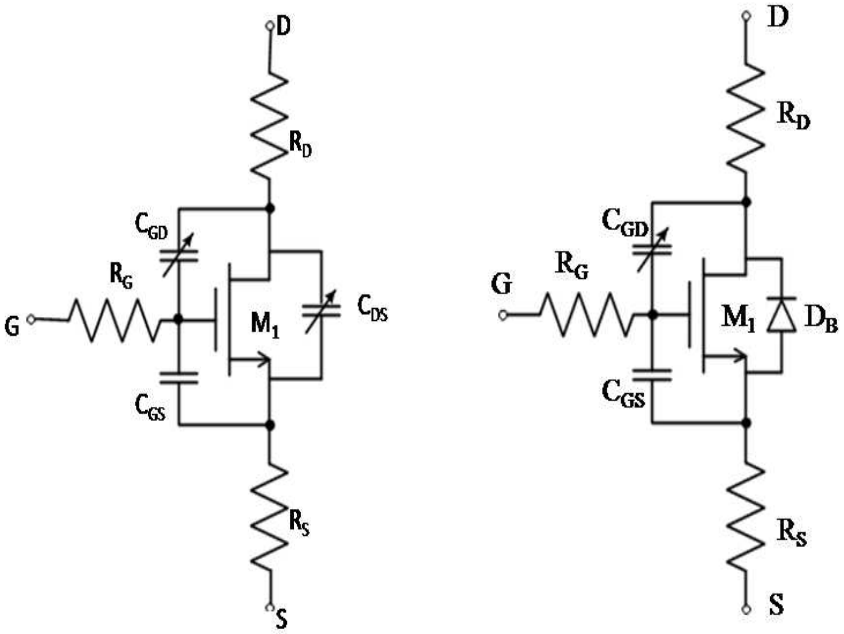


Figure 2-5: Shenai's circuit model for (a) GaN HEMTs (b) Si MOSFETs

2.3.1 Static forward Current-Voltage Characteristic Modeling

A simple FET circuit model, first proposed by Shenai, is used in this study; this model is applicable to both GaN power HEMT as well as silicon power MOSFET[39]. The model is built around MOSFET M1 and other parasitic resistor and capacitor are connected externally as shown in Figure 2.5. A SPICE Level 3 built-in model was used as intrinsic power MOSFET M1. The important specified model parameters included are gate threshold voltage V_{TH}, transconductance parameter K and channel length modulation λ

Figure 2-6 shows the comparison of forward IV characteristic for from datasheets and simulations results for GaN HEMT. It clearly shows that there is good agreement between the measured and simulated characteristics. Similar measurements were made for other GaN HEMT and silicon device used in converters as shown in appendix A. Table 2-2 lists values of important parameters that are extracted from measured data from datasheet for modeling of IV characteristics for GaN HEMT and silicon MOSFET.

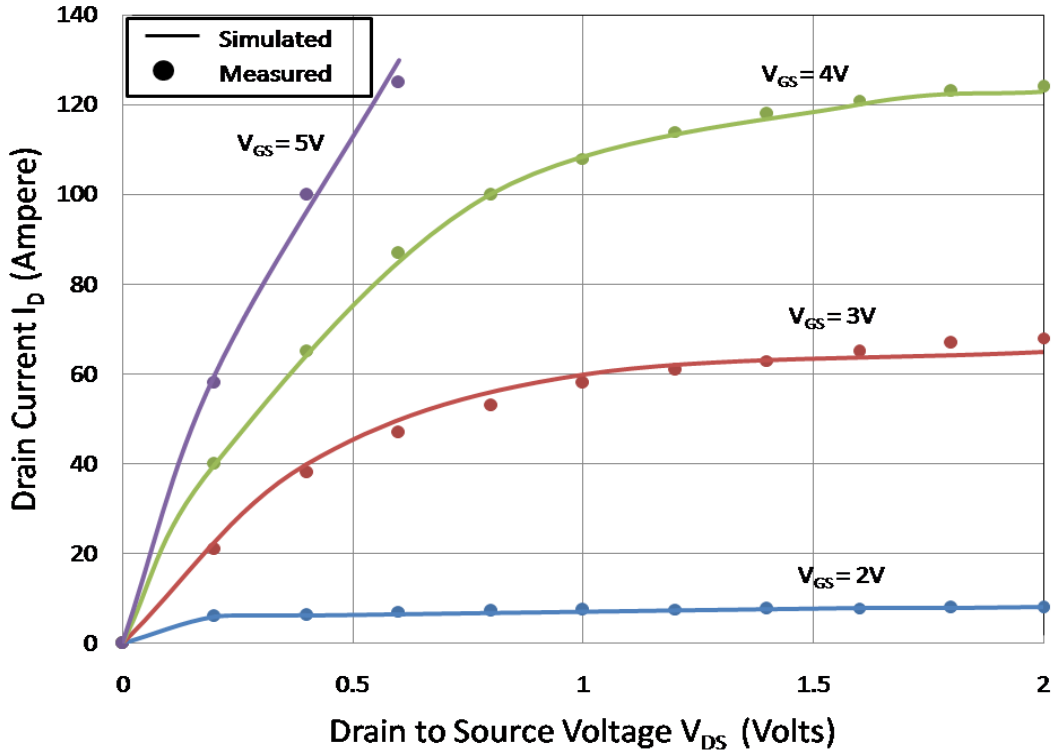


Figure 2-6: Simulated and measured plot of drain current v/s drain to source voltage for varying gate to source voltage measured at room temperature (25 ^{0}C) for GaN HEMT (EPC 1015)

2.3.2 Temperature Dependent ON-Resistance Modeling

All resistances and capacitances of the main FET are connected externally with the body diode (D_B) in case of Silicon based MOSFET as shown in Figure 2-5(b) , and since GaN power HEMT devices doesn't have any diode between drain and source a variable voltage dependent capacitor is connected shown in Figure 2-5(b).As shown in Figure 2-5 source, drain and gate resistances R_S, R_D and R_G were introduced to represent parasitic resistances. The values of R_S and R_D each corresponded to half of the measured on-resistance $R_{DS(ON)}$.

In order to accurately estimate the converter performance vs. temperature, accurate temperature dependence of the on-resistance $R_{DS(ON)}$ was used in the circuit model. In this study, we have used a temperature-dependent model for the on-resistance (2.3). The Level 3 model currently available in SPICE for a power FET does not take into account the temperature dependence of the on-resistance; and, hence, leads to inaccurate representation of the conduction power loss vs. temperature;

$$R_{DS(ON)} = R_{NOM} * (1 + T_{C1}(T - T_{NOM}) + T_{C2}(T - T_{NOM})^2) \quad (2.3)$$

T_{C1} and T_{C2} are adjusted to fit the curve from datasheet for normalized on resistance v/s temperature shown in Figure 2-5.

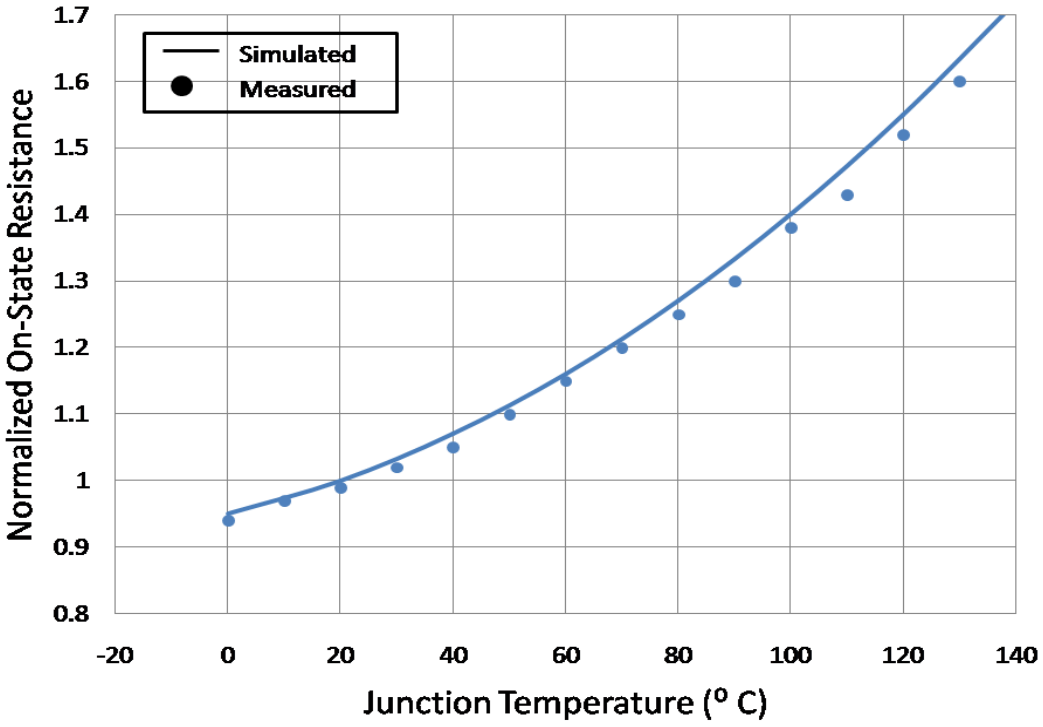


Figure 2-7: Simulated and measured plot of normalized ON-resistance v/s junction temperature for GaN power HEMT (EPC 1015)

Table 2.2: Comparison of important level-3 SPICE model for MOSFET M1 and temperature dependent on resistance used in design of 19/1.2V_{DC}, 7.2 W SB DC-DC converter

Device	**Normalized on resistance parameters**			**Level 3 MOSFET SPICE important parameters**			
	R_{NOM} (Ω)	**T_{C1}**	**T_{C2}**	**V_{TH} (V)**	**K (A/V^2)**	**λ (V^{-1})**	**R_G (Ω)**
Best Commercial Silicon MOSFET (High Side)	22	8.56e-3	1.58e-5	1.2	1.04e-6	0.02	1
GaN HEMT (High Side)	16	6e-3	5e-5	1.4	2e-6	0.02	1
Best Commercial Silicon MOSFET (Low Side)	4.3	1.23e-2	1.8e-5	1.6	3e-6	0.01	1
GaN HEMT (Low Side)	4	6e-3	5e-5	1.4	2e-6	0.01	1

2.3.3 Voltage Dependent Capacitance Modeling

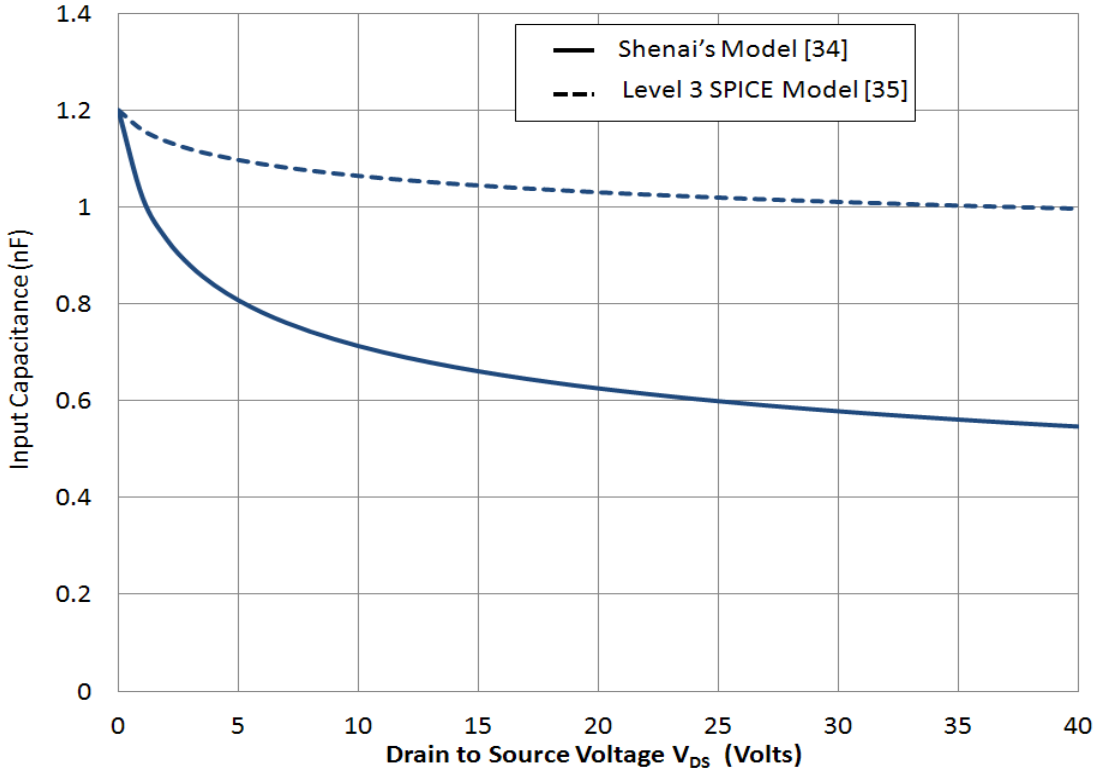


Figure 2-8: Comparison of input capacitance modeled using Shenai's model [34] and the SPICE-based model [35]

It should be further noted that Shenai's model correctly simulates the voltage-dependent input capacitance and is in agreement with the datasheets. The level 3 SPICE model for capacitance does not accurately simulate this capacitance as shown in Figure 2-8 [40]. The SPICE model underestimates the capacitance values, and hence the switching power loss, especially at increased drain-to-source bias voltage.

The built-in MOSFET capacitance was not used and interelectrode capacitances were externally connected as shown in Figure 2-5. The measured gate-source capacitance was relatively independent of the potentials applied to the three electrodes. Thus a constant measured capacitance C_{GS} was used in sub circuit model.

The second and most important capacitive component C_{GD} is gate to drain capacitance and was modeled. This capacitance charges and discharges during switching. Accurate voltage dependent capacitance was modeled in SPICE using an analytical expression given by (2.4). The capacitance of reverse biased drain-source junction body diode was modeled as (2.5).

$$C_{DS} = \frac{C_{DS0}}{\left(1-\frac{V_{DS}}{PB}\right)^{m}} \tag{2.4}$$

$$C_{GD} = \frac{C_{GD0}}{\left(1-\frac{V_{GD}}{PB}\right)^{m}} \tag{2.5}$$

The parameters built-in voltage PB and grading coefficient m are adjusted to obtain desirable characteristic with the measured values. A plot of measured and simulated capacitance values is shown in Figure 2-9. The in-built SPICE diode model is used for body diode D_B in case of Silicon MOSFET. It can be seen that there is some error in measurement of output capacitance (C_{OSS}) in the 0-15 V_{DC} range. This error is mainly due to the model of C_{DS}; this needs to be addressed in future works. But it does not have significant effect on accurate FET performance in circuit. Table 2-3 lists important parameters used in this capacitance model for all different FETs used in the converter.

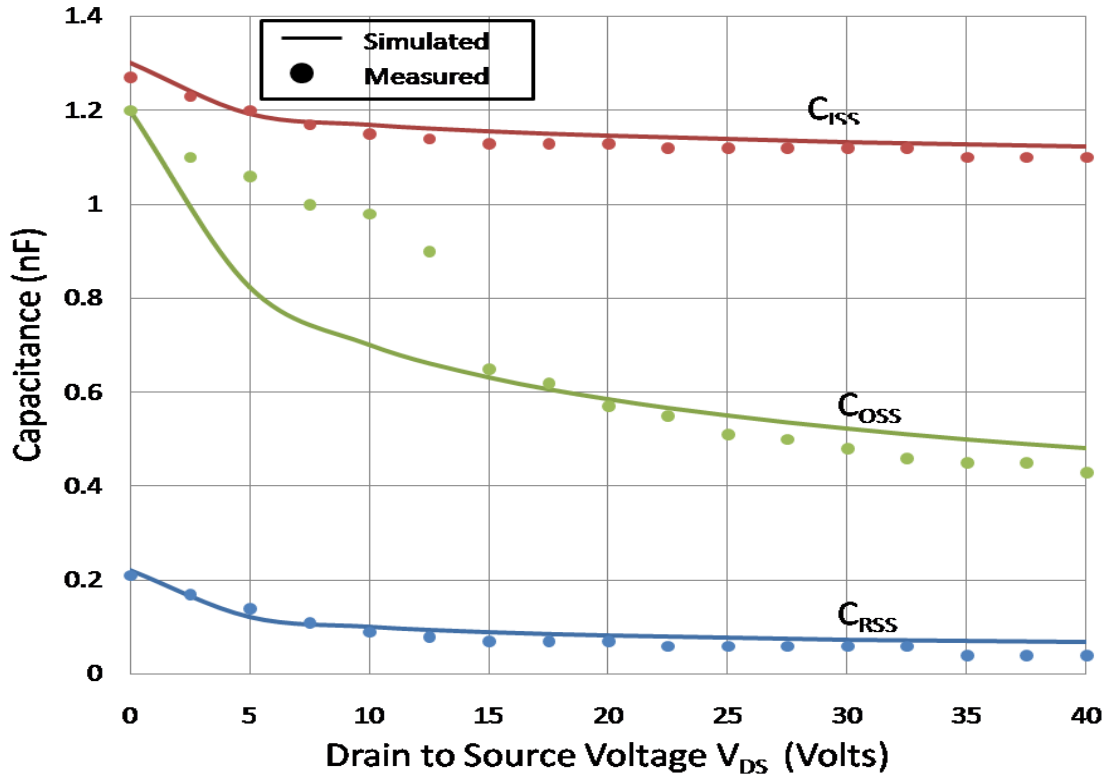


Figure 2-9: Simulated and measured plot of various capacitance v/s drain to source voltage measured at room temperature (25 ^{0}C) for GaN HEMT (EPC 1015).

Table 2.3: Comparison of important voltage dependent capacitance model used in design of 19V/1.2V_{DC}, 7.2 W SB DC-DC converters

Device	**C_{GS} (nF)**	**C_{DS}**			**C_{GD}**		
		C_{JO} (nF)	**PB (V)**	**m**	**C_{JO} (nF)**	**PB (V)**	**m**
Best Commercial Silicon MOSFET (High Side)	0.53	0.35	0.12	0.7	0.22	0.7	0.6
GaN HEMT (High Side)	0.26	0.24	0.9	0.25	0.06	0.8	0.3
Best Commercial Silicon MOSFET (Low Side)	4.3	3.2	0.55	0.34	0.8	0.8	0.7
GaN HEMT (Low Side)	1.1	1	0.9	0.25	0.22	0.8	0.3

2.4 Power Inductor Model

Figure 2-10 shows the lumped element SPICE circuit model for the power inductor L in Figure 2-3. The model takes into account frequency dependence of the inductance and power loss

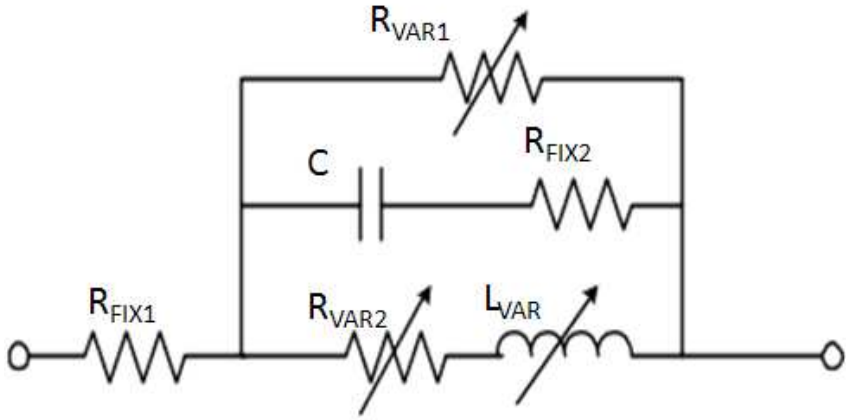


Figure 2-10: Model for Inductor used in SB DC-DC Converter

Equations (2.6) and (2.7) represents the frequency dependence of series resistance in inductor and l_1, l_2 are variable coefficient to fit the curve of the resistance. The Equation (2.8) represents the frequency dependence in value of power inductor and in equation l_3 l_4 and l_5 are adjusting coefficient to fit the curve of inductor [41]

$$R_{VAR1} = l_1 * \sqrt{f_s} \tag{2.6}$$

$$\mathrm{R_{VAR2}} = \mathrm{l_2} * \sqrt{\mathrm{f_s}} \tag{2.7}$$

$$L_{VAR} = l_3 - l_4 * \log(l_5 * f_s) \tag{2.8}$$

2.5 Loss Modeling and FET Optimization

The main components in the converter with losses are the FETs and inductor. Hence, it is important to accurately analyze the various losses occurring in the two FETs [43][44]. The total loss FET loss is

$$P_{total} = P_{sw} + P_{con} + P_{gd} + P_{oss} \tag{2.9}$$

These losses are calculated using:

$$P_{con} = D.I_D^2 * R_{DS(ON)} \tag{2.10}$$

$$P_{gd} = Q_{GS} * V_{GS} * f_s \tag{2.11}$$

$$P_{sw} = V_{in} I_D \left(t_{on} + t_{off}\right) * f_s \tag{2.12}$$

$$P_{oss} = \frac{1}{2} * V_{in} * Q_{oss} * f_s \tag{2.13}$$

The total switching loss is the sum of P_{sw} and P_{oss}. Figure 2-11 illustrates the shortcomings of switching loss calculations using this formulations; accurate FET switching losses calculated from SPICE circuit simulations (and validated using converter measurements) are also plotted for comparison. This large discrepancy primarily results from incorrect assumptions made in estimating the switching losses. Accurate modeling of FET voltage and current waveforms are needed during switching in order to correctly estimate the switching losses.

To evaluate performance of GaN based HEMTs switched at high frequency (<5 MHz) in the circuit, a new Figure of Merit (FOM) is needed. Shenai first proposed the input technology factor, $k = R_{DS(ON)} C_{iss}$ *(or* $R_{DS(ON)} Q_g$*)* as the FOM for evaluating the potential of a given power semiconductor switch technology in high-frequency power-switching applications[45]; however, this FOM only accounts for the on-state and input switching power losses, and does not account for output switching losses. Although this FOM has

remained to-date as the industry-standard, there is need of new device selection criteria which accounts for output switching loss as well for the converters operating at high frequency. It was observed that input capacitance for high side FETs and output capacitance for low side FETs have highest impact on switching loss of switch in synchronous Buck DC-DC converter. The parameters affecting the FET performance are die area, duty cycle, temperature, frequency etc. [46].

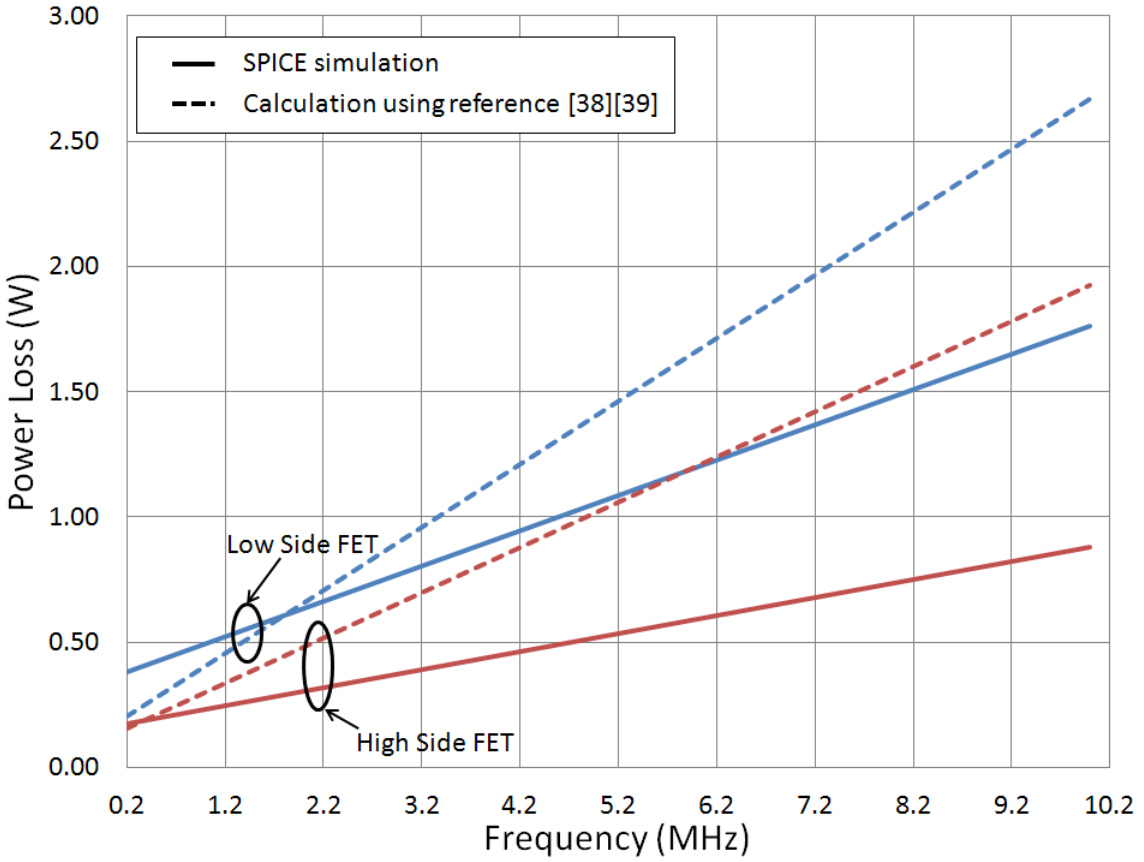


Figure 2-11: Comparison of switching losses in GaN power HEMTs obatined from improved SPICE simulations and conventional formulation [38][39] for a 19/1.2V_{DC},7.2W SB DC-DC power converter operating at at room temperature (25 ^{0}C)

2.5.1 Effect of Die size

Configuration 1: To evaluate the effect of die size of FET used in low side and high side switch in synchronous buck converter, detailed loss calculation were performed in both switches for different frequencies. Initially FET 1 with specification 40V/10 A were used as per requirement of the design of converter 19/1.2V_{DC}, 7.2W. The GaN HEMT from EPC was selected for both high side and low side switch [35]. Figure 2-12 shows variation of switching loss, conduction loss and total loss in high side and low side switch with frequency. At lower frequency (below 5 MHz), the conduction loss accounts for more than 50% of total loss, thus overall loss is very high in low side FET, thus reducing efficiency at lower frequency.

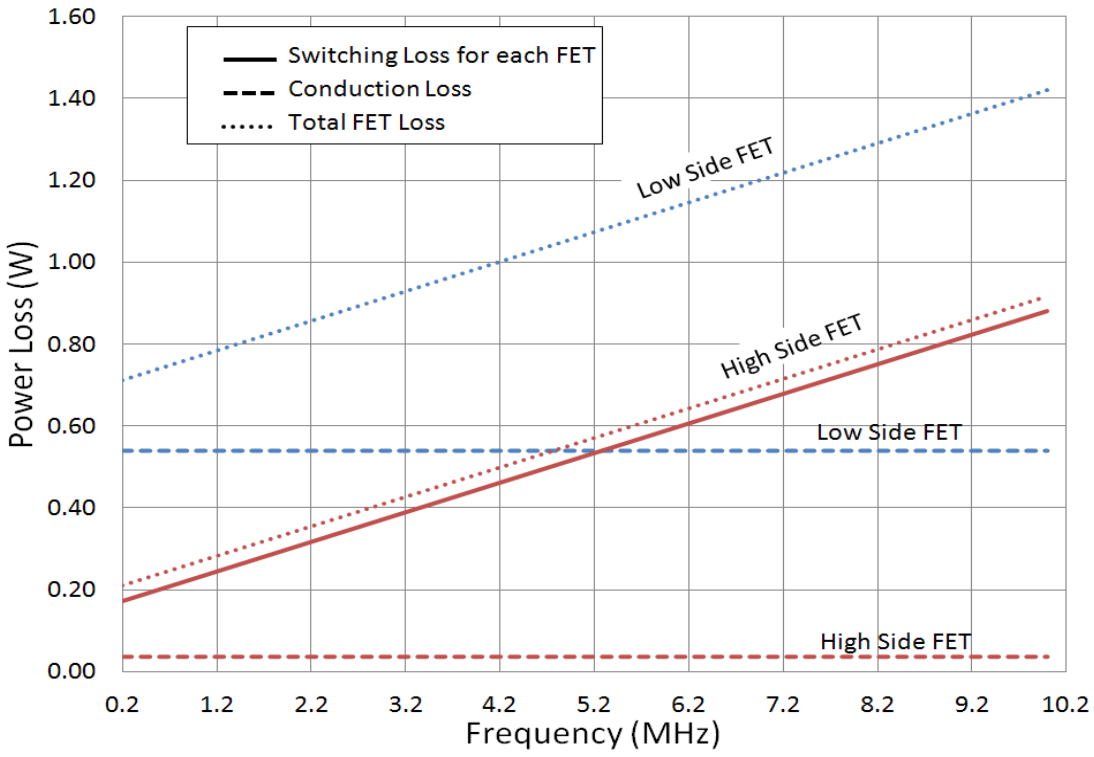


Figure 2-12: Simulated plot of various losses for GaN HEMT for Configuration 1

Configuration 2: To reduce conduction loss, die area of switch was increased. According to (2.14) ON-resistance is inversely proportional to die area, thus increase in die area will decrease the ON resistance. But increase in die Area will also increase the parasitic capacitance as shown (2.15). GaN HEMT with larger die area was used; 40V/33A was used as switch (FET 2) in both high side and low side switch. Since this GaN HEMT has higher current rating; it has low on resistance and higher parasitic capacitances as compare to other device used. Figure 2-13 shows variation of switching loss, conduction loss and total loss in high side and low side switch with frequency. Since ON-resistance is very less as compared to FET 1, the conduction loss is reduced considerably and it accounts for less than 40 % of total loss in total loss. The Switching loss in this device is much higher as compare to FET 1 because of increased capacitance. At higher frequency (above 5 MHz) the switching loss dominates total loss and this will degrade the performance of converter. Thus this configuration is good only for very low frequency.

$$R_{DS(ON)} = {}^{R_{sp}}/_{Die\ Area} \tag{2.14}$$

$$C = C * Die\ Area \tag{2.15}$$

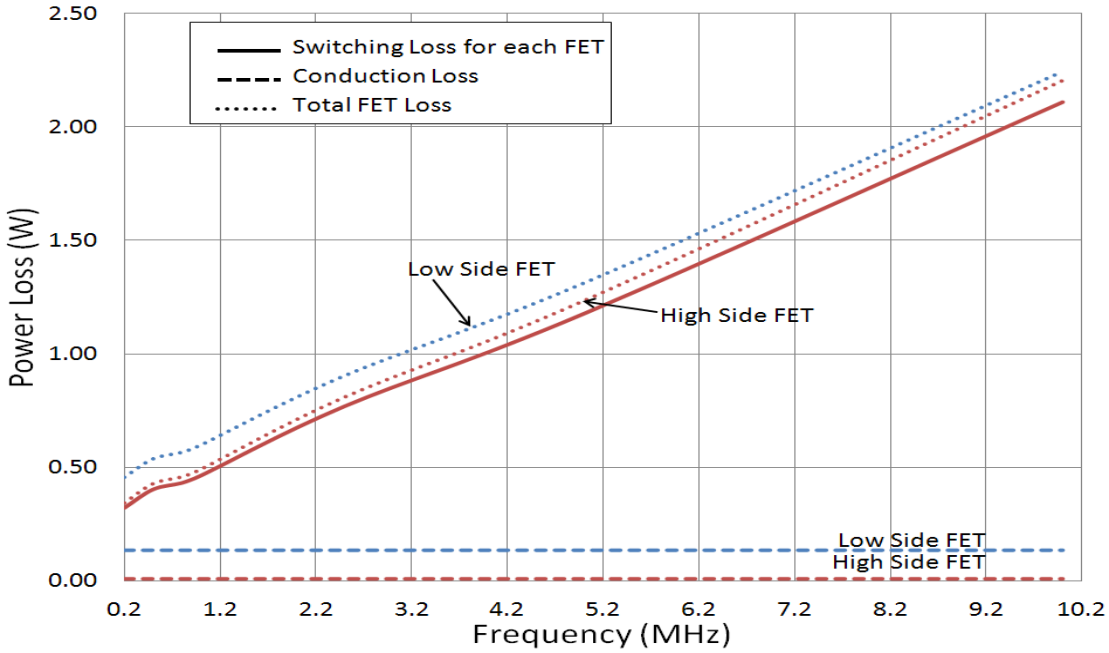


Figure 2-13: Simulated plot of various losses for GaN HEMT for Configuration 2

Configuration 3: The step ratio ($19/1.2V_{DC}$) is very high, which means low side FET is conducting most of the time; thus conduction loss dominates the total loss in low side switch. Whereas the high side FET is conducting for very less time (~0.06) of total time, thus switching loss dominates the total FET loss. So taking this into consideration high side switch with rating (40V/10A) and low side switch with rating (40V/33A) were used in simulations. These resulted in reduction of conduction loss in low side switch and switching loss in high side switch. Figure 2-14 shows variation of switching loss, conduction loss and total loss in high side and low side switch with frequency. This configuration ensured lower losses in switches as compared to other configuration at lower frequency. However at higher frequency switching loss accounts for more than 50% of total loss and thus FETs have more losses than configuration 1.

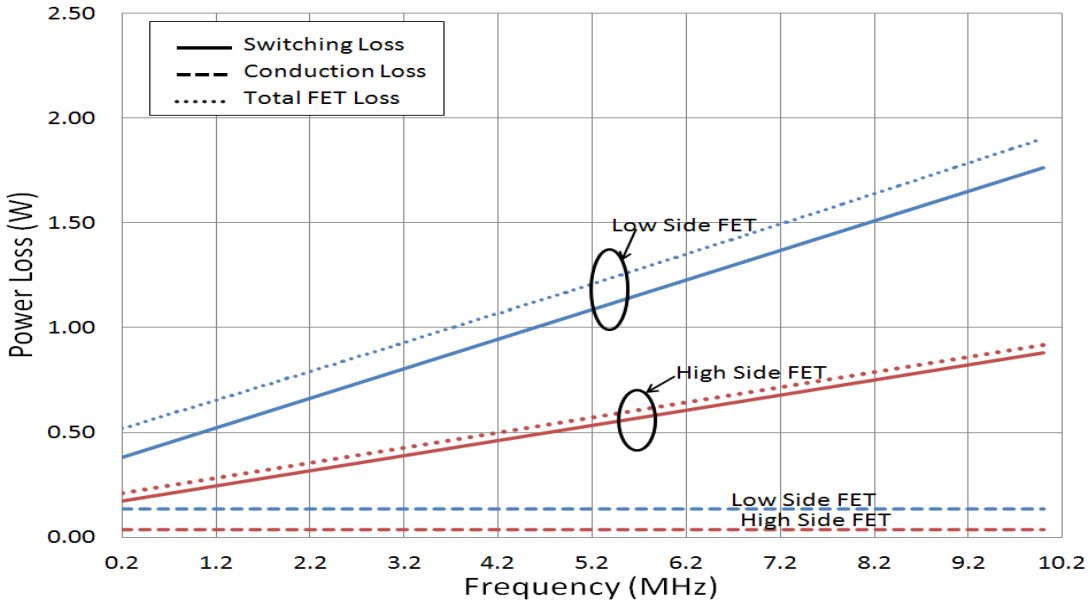


Figure 2-14: Simulated plot of various losses for GaN HEMT for Configuration 3

Table 2-4 shows the simulated results for efficiency measured for 19/1.2V, 7.2W synchronously switched DC-DC buck converter for different frequency with low side and high side switch having different ratings. It clearly shows that configuration 3 is good for low frequency, because of its optimized switch used for low side. But at higher frequency the switching loss is dominating over conduction loss, thus switch with least switching loss is desirable. Thus configuration 1 has 2% higher efficiency for frequency over 2.5 MHz as compared to other configuration. Figure 2-13 shows total losses in both switch for different combination of GaN HEMT device used in 19/1.2V, 7.2W for different frequency measured at room temperature (25 °C). The graph shows that at frequency greater than 3 MHz , the total FET losses is lower in case of configuration 1 in comparison of any other configuration. However at lower frequency scaling of device is useful and has lower losses in comparison with other configuration, thus higher efficiency..

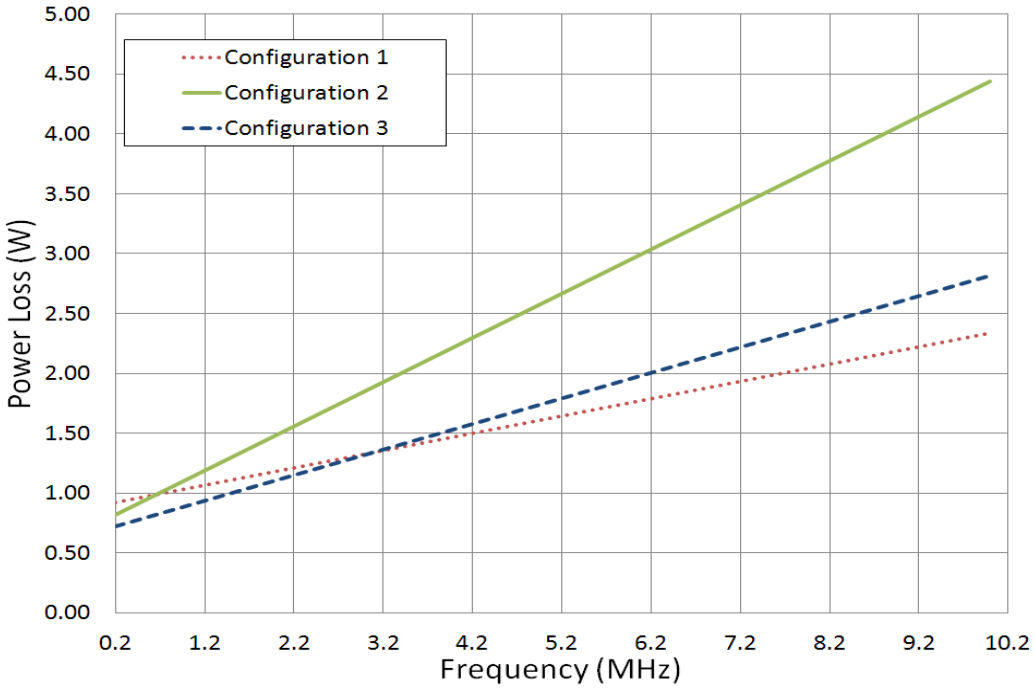


Figure 2-15: A plot of total losses in both FETs measured using simulations v/s frequency for 19/1.2 V, 7.2 W SB DC-DC converter

Table 2.4: Comparison of Efficiency for different

Frequency (MHz)	**Efficiency (%)**		
	Configuration 1	**Configuration 2**	**Configuration 3**
0.2	88	89	91
0.5	86	87	89
0.8	85.5	86	87
1	84	83	86
2.5	83	79	83
5	82	72	80
10	72	60	69

2.5.2 Effect of Duty Cycle

Then the efficiency was calculated using simulations results from varying duty cycle and thus power at frequency 5 MHz. The current was kept constant at 6A for all varying voltage by adjusting load resistance. Figure 2-14 shows the efficiency of the 19V-6A DC-DC power converter as a function of duty cycle; measurement was performed at a room temperature of 25°C. The Figure 2-18 clearly shows that efficiency increases with duty cycle. This increase is largely due to decrease in switching loss in switch used. The load in servers require voltage in range of 1.2V to 5V, thus having higher duty cycle will increase the number of conversion steps require to achieve the load voltage. Eventually the efficiency of overall system will decrease. Hence converter with lower duty cycle is used to decrease conversion steps required.

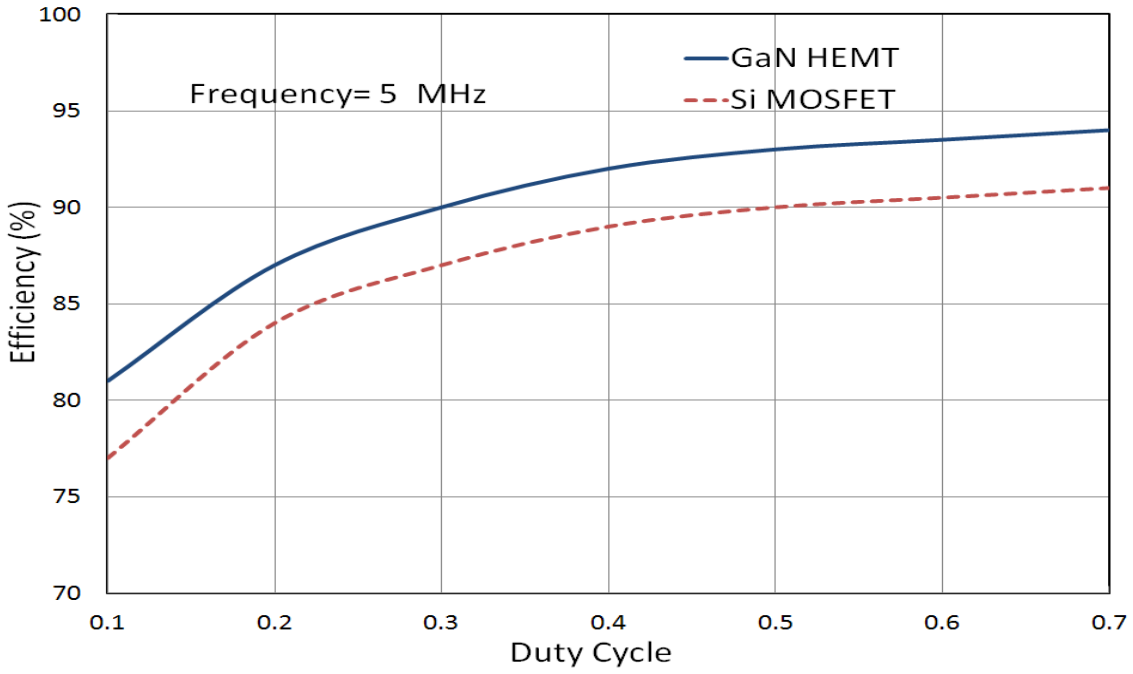


Figure 2-16: A plot of total losses in both FETs measured using simulations v/s Duty Cycle for 19/1.2 V, 7.2 W SB DC-DC converter

2.6 Results and Discussion

Figure 2-17 shows the simulation results for the 19/1.2V_{DC}, 7.2W DC-DC power converter at various temperatures for an output ripple of 1%. These results suggest that there is about 3% - 4% drop in efficiency as the temperature is increased from -55°C to 150°C at a power conversion frequency f_s = 5 MHz. This variation in efficiency is primarily due to variation in the on-state resistance with temperature; this on-resistance dependence on temperature is accurately modeled in the improved FET model.

Simulations were also performed at various frequencies and at room temperature. Figure 2-17 shows the simulation results for the 19V/1.2V_{DC}, 7.2W DC-DC power converter at room temperature for an output voltage ripple of 1%. These results suggest that an efficiency η = 78% can be achieved at a power conversion frequency f_s = 5 MHz. The efficiency gain for GaN HEMT-based power converter is more than 3% compared to the silicon power MOSFET converter. The enhanced performance of GaN HEMT-based converter is largely due to reduced device capacitances compared to the state-of-the-art commercial silicon power MOSFETs; a smaller input capacitance results in reduced gate charge, and hence, the switching loss is reduced.

Table 2-5 and Table 2-6 provides insight into various power losses occurring in the circuit components of the DC-DC converters. Table 2-6 shows that the FET losses in case of silicon MOSFE is more than the GaN HEMT by 3-4 %. The conduction loss for both high side and low side switch remains almost constant for full range of frequency. Since the step ratio for voltage is very less (around 0.06), low side switch is ON most of time, thus conduction loss in case of low side is more as compare to high side switch. As switching loss is function of switching frequency, it increases with switching frequency.

Switch with high die area was used for low side to decrease ON resistance, it meant increase in capacitances. Thus the switching loss is higher in low side as compare to high side switch. Since series inductor resistance is function of frequency, inductor loss increases with frequency.

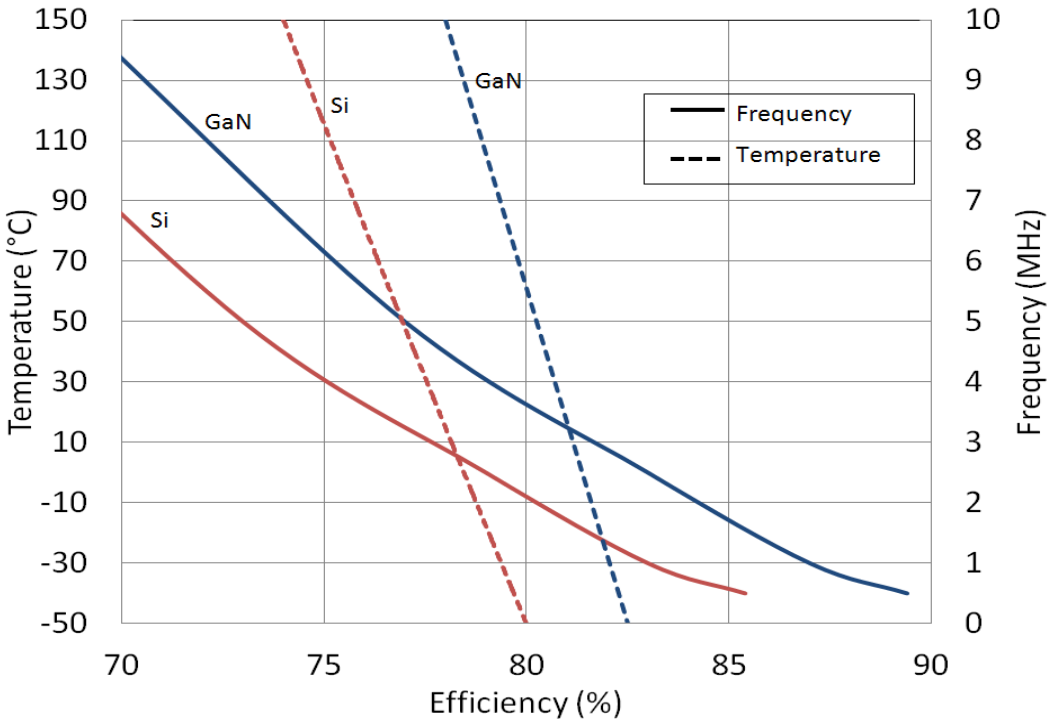


Figure 2-17: Simulation results showing Efficiency vs. temperature (at 5 MHz) and frequency (at a room temperature of 25°C) for a 19/1.2V_{DC}, 7.2W SB DC-DC converters

Table 2.5: Power losses in GaN HEMTS and power inductor for a 19V/1.2V, 7.2W DC-DC SB converter measured at room temperature (25°C) as a function of frequency

Frequency (MHz)	Output Power (W)	Input Power (W)	High Side FET Conduction Loss (W)	Low Side FET Conduction Loss (W)	High Side FET Switching Loss (W)	Low Side FET Switching Loss (W)	Inductor Loss (W)	Efficiency (%)
0.2	7.2	7.91	0.04	0.13	0.11	0.34	0.09	91
0.5	7.2	8.09	0.04	0.13	0.19	0.41	0.11	89
0.8	7.2	8.28	0.04	0.13	0.22	0.53	0.15	87
1	7.2	8.37	0.04	0.13	0.36	0.46	0.18	86
2.5	7.2	8.67	0.04	0.13	0.35	0.75	0.20	83
5	7.2	9.00	0.04	0.13	0.38	1.00	0.25	80
10	7.2	10.43	0.04	0.13	0.94	1.78	0.35	69

Table 2.6: Power losses in Silicon MOSFET and power inductor for a 19V/1.2V_{DC}, 7.2W DC-DC SB converter measured at room temperature (25°C) as a function of frequency

Frequency (MHz)	Output Power (W)	Input Power (W)	High Side FET Conduction Loss (W)	Low Side FET Conduction Loss (W)	High Side FET Switching Loss (W)	Low Side FET Switching Loss (W)	Inductor Loss (W)	Efficiency (%)
0.2	7.2	8.28	0.05	0.15	0.13	0.66	0.09	87
0.5	7.2	8.47	0.05	0.15	0.21	0.76	0.11	85
0.8	7.2	8.67	0.05	0.15	0.25	0.88	0.15	83
1	7.2	8.78	0.05	0.15	0.40	0.81	0.18	82
2.5	7.2	9.00	0.05	0.15	0.46	0.94	0.20	80
5	7.2	9.35	0.05	0.15	0.55	1.15	0.25	77
10	7.2	11.08	0.05	0.15	1.35	1.98	0.35	65

Then the efficiency was calculated using simulations results from varying load at a constant frequency 800 kHz. The measured data was collected from EPC [42]. Figure 2-18 shows the efficiency of the 19/1.2V_{DC} DC-DC power converter as a function of load

current; measurements were performed at a room temperature of 25°C. Since the values of inductor and capacitor affects the energy storage of current and voltage. The value of magnetics was increased 10 times the calculated value in order to get constant efficiency over wide range of load. The results clearly show that efficiency changes with load current and that there is about 3% improvement in peak efficiency for the GaN FET-based converter compared to the converter using silicon MOSFET. Table 2-7 and Table 2-8 show clearly that both conduction and switching losses in switch increases with increase in current. The losses in silicon switches are more than GaN HEMT devices by 3-4%. Since inductor losses in series resistance are function of current, it increases with current.

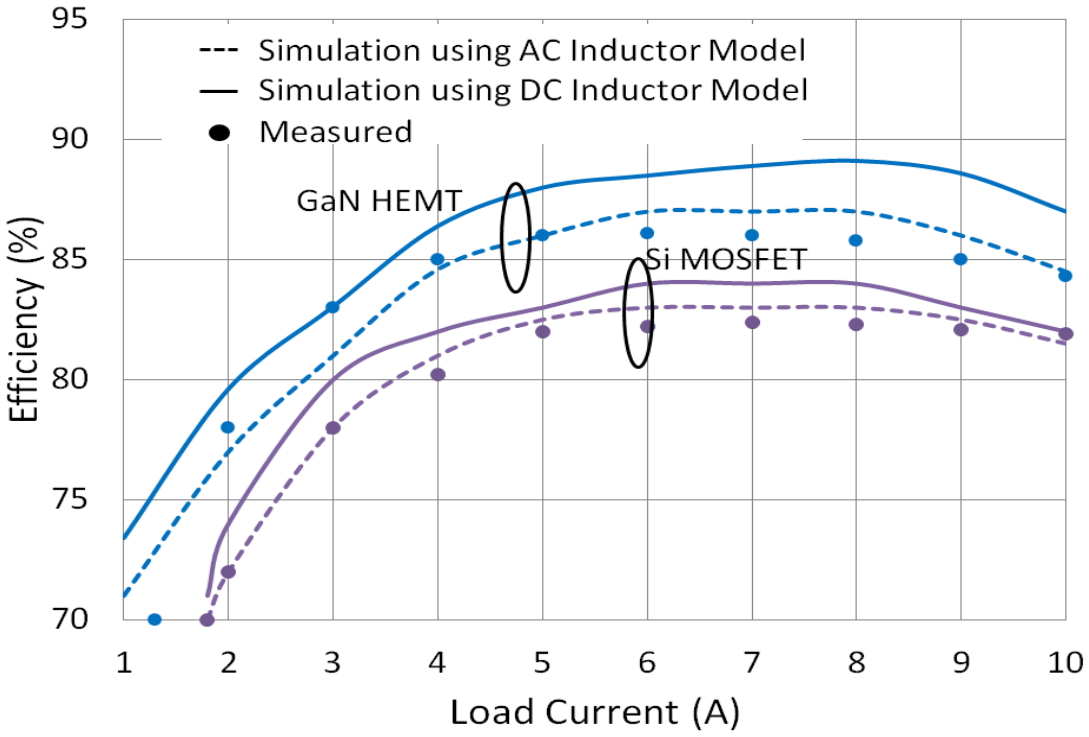


Figure 2-18: A plot of simulation and measured efficiency vs load current for 19/1.2V_{DC} SB DC-DC converter at a switching frequency of 800 kHz (at a room temperature of 25°C)

Table 2.7: Power losses in GaN HEMTS and power inductor for a 19/1.2V_{DC} DC-DC SB converter for varying load measured at a switching frequency of 800 khz and room temperature (25°C)

Output Current (A)	Output Power (W)	Input Power (W)	High Side FET Conduction Loss (W)	Low Side FET Conduction Loss (W)	High Side FET Switching Loss (W)	Low Side FET Switching Loss (W)	Inductor Loss (W)	Efficiency (%)
1	1.2	1.69	0.00	0.00	0.12	0.36	0.00	71
2	2.4	3.12	0.00	0.01	0.17	0.51	0.02	77
3	3.6	4.44	0.01	0.03	0.19	0.57	0.04	81
4	4.8	5.67	0.02	0.06	0.19	0.54	0.06	84.6
5	6	6.98	0.03	0.09	0.21	0.55	0.10	86
6	7.2	8.28	0.04	0.13	0.22	0.54	0.14	87
7	8.4	9.66	0.05	0.18	0.25	0.57	0.20	87
8	9.6	11.03	0.06	0.24	0.28	0.59	0.26	87
9	10.8	12.56	0.08	0.30	0.34	0.70	0.32	86
10	12	14.20	0.10	0.37	0.43	0.89	0.40	84.5

Table 2.8: Power losses in Silicon MOSFETs and power inductor for a 19/1.2V_{DC} DC-DC SB converter for varying load measured at a switching frequency of 800 khz and room temperature (25°C)

Output Current (A)	Output Power (W)	Input Power (W)	High Side FET Conduction Loss (W)	Low Side FET Conduction Loss (W)	High Side FET Switching Loss (W)	Low Side FET Switching Loss (W)	Inductor Loss (W)	Efficiency (%)
1	1.2	3.09	0.00	0.01	0.17	0.72	0.01	70
2	2.4	3.33	0.01	0.02	0.17	0.72	0.02	72
3	3.6	4.62	0.01	0.04	0.18	0.75	0.04	78
4	4.8	5.93	0.02	0.06	0.20	0.78	0.06	81
5	6	7.27	0.03	0.10	0.22	0.82	0.10	82.5
6	7.2	8.67	0.05	0.15	0.25	0.89	0.14	83
7	8.4	10.12	0.07	0.20	0.29	0.97	0.20	83
8	9.6	11.57	0.09	0.26	0.32	1.04	0.26	83
9	10.8	13.09	0.11	0.33	0.37	1.16	0.32	82.5
10	12	14.72	0.14	0.40	0.44	1.35	0.40	81.5

Chapter 3

DC-DC Boost Converter and *dv/dt* stress

It has been well known for more than two decades that power devices made from wide bandgap semiconductors such as Silicon Carbide (SiC) and Gallium Nitride (GaN) offer much lower on-state resistance ($R_{DS(on)}$) than silicon power devices because of their superior electrical conductivity and breakdown field compared to silicon [47]. However, only recently, GaN power high electron mobility transistors (HEMTs) are being made available in samples by select commercial vendors [23].

SiC diodes has zero reverse recovery time and low forward voltage drop as compare to commercial silicon diodes. As described in this chapter; using SiC diodes can improve converter efficiency by 4-5 %. Since SiC has zero reverse recovery time it can reduce voltage stress on switch used in boost DC-DC converter [48].

Switching the device at higher frequency and with advent of wide band gap materials based FETs having low capacitance; high *dv/dt* across switch and diode is observed during switching in DC-DC boost converter. K. Acharya et al. showed that SiC diode fail at values of 55-60 V/ns [49].

3.1 DC-DC Boost Converter Test Circuit

The electricity produced from the solar panel is time-varying and fluctuating in nature. Hence, MPPT is used to extract optimum electricity from the solar PV energy conversion process. The same boost converter can also be used to perform the MPPT function [31][32]. The boost converter circuit shown in Figure 3-1 has been chosen to evaluate the efficiency gains possible from emerging GaN power HEMTs; the results are compared to the best commercially available silicon CoolMOS power devices [51].

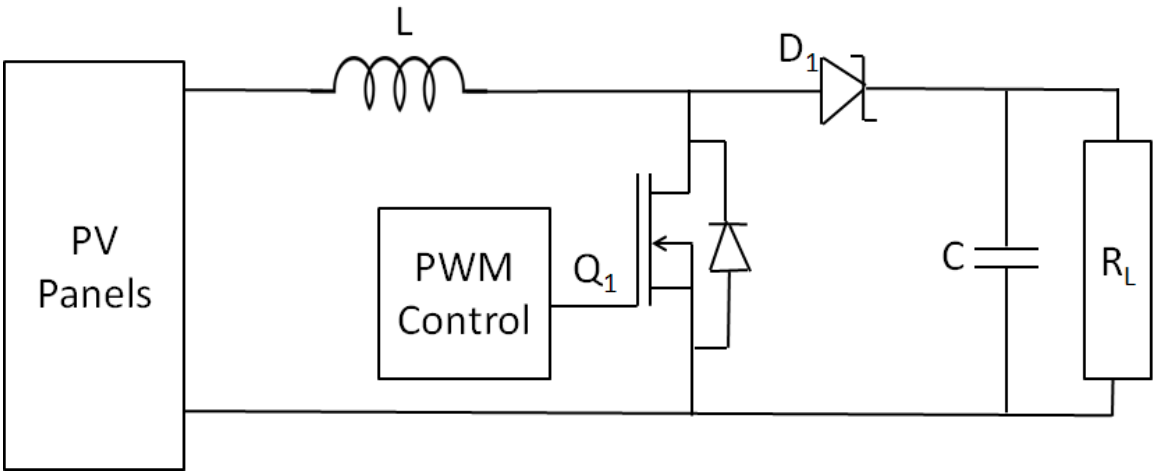


Figure 3-1: Circuit schematic of a DC-DC Boost Converter

In the boost converter circuit shown in Figure3-1, when switch Q_1 is turned, inductor is charged by the solar PV electricity. During this time, diode D_1 is reverse-biased. In order to avoid a voltage spike at the drain of Q_1, the reverse recovery of diode D_1 must be negligible. When switch Q_1 is turned off, and when the solar power is available, the output capacitor C_2 is charged from the energy stored in the inductor as well as by the electricity produced from the solar PV source. When solar power is not available, appropriate provision is made for the circuit to operate in the boost mode.

The minimum inductor value needed to maintain continuous current conduction as a function of switching frequency, and a corresponding capacitor value for the desired output ripple are calculated using standard closed form expression[31][32]:

$$L_{min} = \frac{D.(1-D)^2(V_o)}{2.I_o.f_s} \tag{3.1}$$

$$C = \frac{D}{f_S.R.(\Delta V_o/V_o)} \tag{3.2}$$

The sizes of magnetic components and capacitors in the circuit vary inversely with frequency; hence, higher switching frequency is desired for reducing the converter size and cost. The main advantage of using the GaN FET for power switching is that switching frequency can be kept high (>1 MHz) while still maintaining lower conduction power loss (compared to a silicon power MOSFET with identical rating); higher switching frequency can reduce capacitor and inductor values exponentially as shown in Figure 3-2.

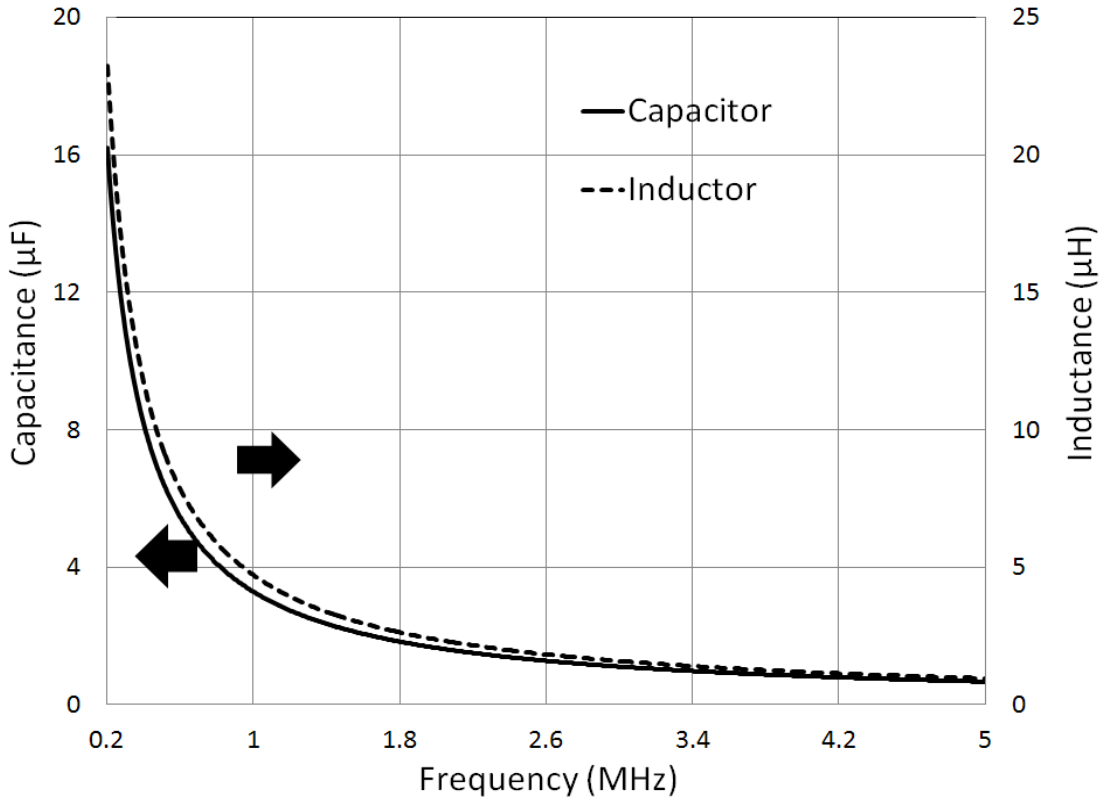


Figure 3-2: A plot of calculated inductor and capacitor values vs. frequency in the 200/380V_{DC}, 10kW DC-DC boost converter.

The best available 600V/30A commercial silicon CoolMOS data was used in converter; the 600V/30A GaN HEMT circuit model parameters were estimated by scaling the results commercially available GaN HEMTs from EPC [51][52][53][54][55].Initially to meet the specification of boost converter design, the commercial device (100 V and 200V) was scaled to current specification of 30A. The parasitic resistances and capacitance was calculated and plotted. Then after using the slope of the plot shown in Figure 3-3 and Figure 3-4 for 100V and 200V, the resistance and capacitances was estimated for 600V to compare it with commercial Silicon device. Table 3-1 lists the comparison of various FET parameters used in DC-DC boost converter (200V/380V_{DC}, 10kW).

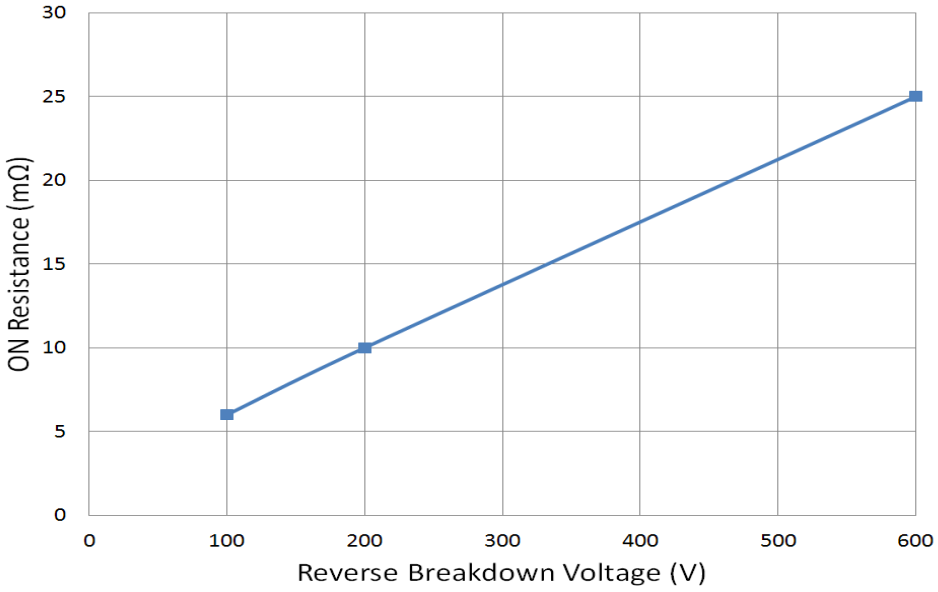


Figure 3-3: A plot of scaled values of ON resistance v/s reverse breakdown voltage from commercially available GaN HEMT device (30 A devices)

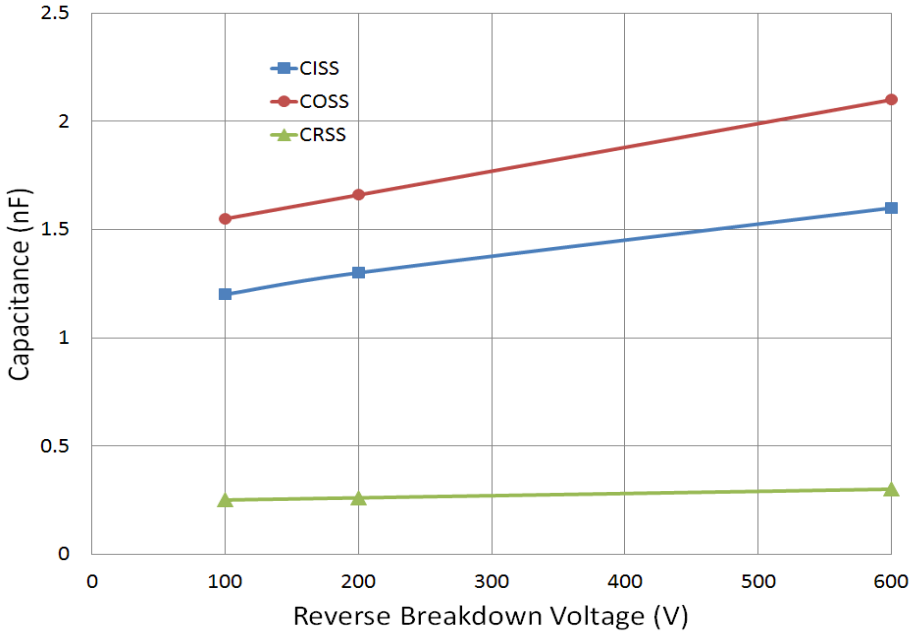


Figure 3-4: A plot of scaled value of all parasitic capacitance (at zero bias) v/s reverse breakdown voltage from commercially available GaN HEMT device (30 A devices)

In order to evaluate the performance of SiC diode with commercial diode , various combination of switch and diode was tested.

Configuration 1: In configuration 1 GaN HEMT was used as switch and SiC diode for D_1[56]. When these configuration is used, as it offers the lowest forward voltage drop with negligible reverse recovery amongst commercially available diodes in this rating..

Configuration 2: In this configuration GaN HEMT was replaced by silicon MOSFET and SiC diode was used. This configuration was used to compare performance of silicon MOSFET with Gan HEMT for frequency, temperature and current variations.

Configuration 3: In this one Silicon MOSFET was used as switch, while SiC diode was replaced by best commercial silicon diode [57].

Configuration 4: In this one GaN HEMT was as switch, with silicon diode.

Table 3.1: Comparison of important FET parameters used in design of 200/380V_{DC}, 10kW Boost DC-DC converter [45]

Device	**V_{BR} (V)**	**V_{TH} (V)**	**$R_{DS(on)}$ (mΩ)**	**C_{ISS} (nF)**	**C_{OSS} (nF)**	**C_{RSS} (nF)**	***dv/dt* (V/ns)**
Best Commercial Silicon MOSFET	600	3	0.099	4.5 n	20 n	1.8 n	50
GaN HEMT	600	1.4	0.025	1.6 n	2.1 n	0.3 n	-

Table 3.2: Comparison of important diode parameters used in design of 200/380V_{DC}, 10kW Boost DC-DC converter [50][51]

Device	**V_{BR} (V)**	**C_{JO} (V)**	**(V_F)**	**R_S (mΩ)**	**T_{rr} (ns)**
Best Commercial SiC Diode	600	480	1.8	40	0
Best Commercial Si Diode	600	61	2.6	60	30

3.2 Circuit Simulation Model for Power FET

A simple FET circuit model, first proposed by Shenai, is used in this study; this model is applicable to both GaN power HEMT as well as silicon power MOSFET [39]. The model described in Chapter 2 is used for modeling of switch in boost converter

3.3 Results and Discussion

A behavioral gate switching waveform was used to determine the optimum switching frequency and timing sequence so as to achieve the highest power conversion efficiency.

3.3.1 Effect of Load, Frequency and Temperature variation on performance of boost converter

Since load is never constant in practical implementation, simulations at different load currents and at a constant frequency of 1MHz were performed. Figure 3-5 shows the efficiency of the 200V/380V_{DC} DC-DC power converter as a function of load current; calculations were performed at a room temperature of 25°C. Since the values of inductor and capacitor affects the energy storage of current and voltage. The values of magnetics were increased 10 times the calculated value in order to get constant efficiency over wide range of load. The results clearly show that efficiency changes with load current and that there is about 3% improvement in peak efficiency for the GaN power HEMT based converter compared to the converter using silicon CoolMOS.

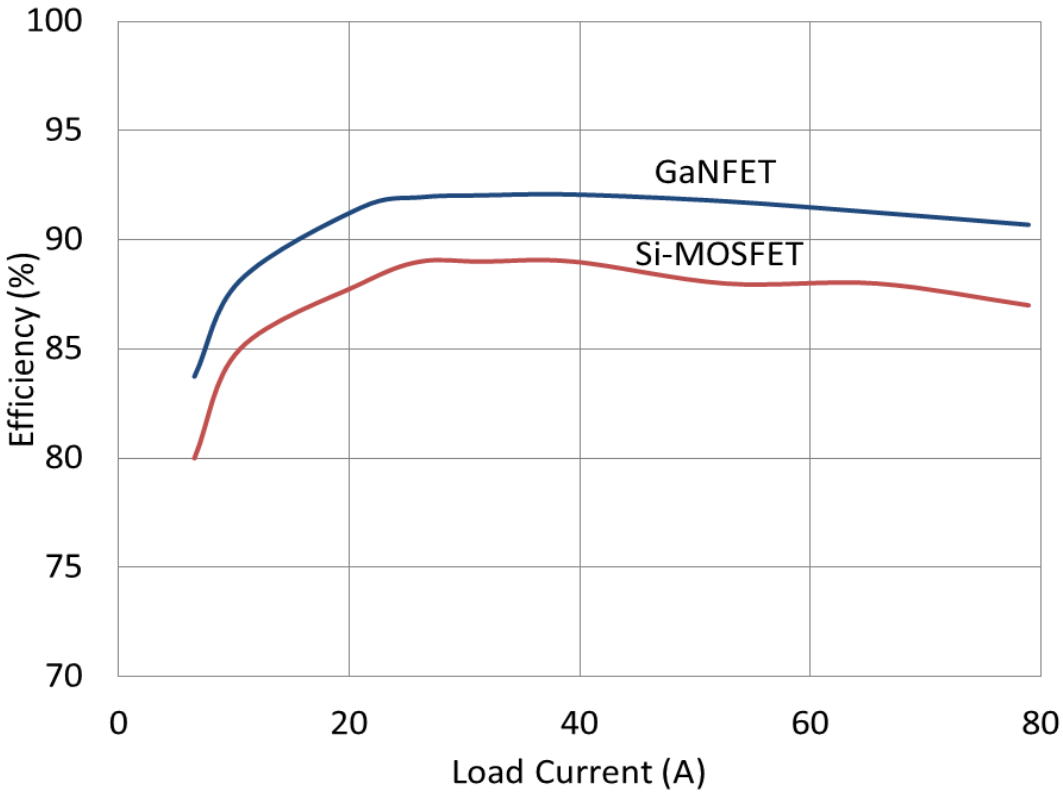


Figure 3-5: A plot of calculated efficiency vs. load current for 200V/380V DC-DC boost converter at a switching frequency of 1MHz and room temperature (25°C).

The converter simulations were also performed at various temperatures and frequency. Figure 3-6 shows the simulation results for the converter where the efficiency is plotted vs. frequency (at a room temperature of 25°C) and temperature (at 1MHz) for an output ripple of 1%. These results suggest that there is about a 4% drop in efficiency as the temperature is increased from -55°C to 150°C. This variation in efficiency is primarily due to change in the on-state resistance of power FETs with temperature. These results also suggest that a room-temperature efficiency η = 93% can be achieved at a power conversion frequency f_s = 1 MHz using the GaN power HEMT. The efficiency gain for GaN HEMT-based power converter is about 3% compared to the converter with the best commercially available silicon CoolMOS. The enhanced performance of a GaN

HEMT-based converter is largely due to reduced device capacitances compared to state-of-the-art commercial silicon power MOSFETs; a smaller input capacitance results in reduced gate charge, and hence, the switching loss is reduced.

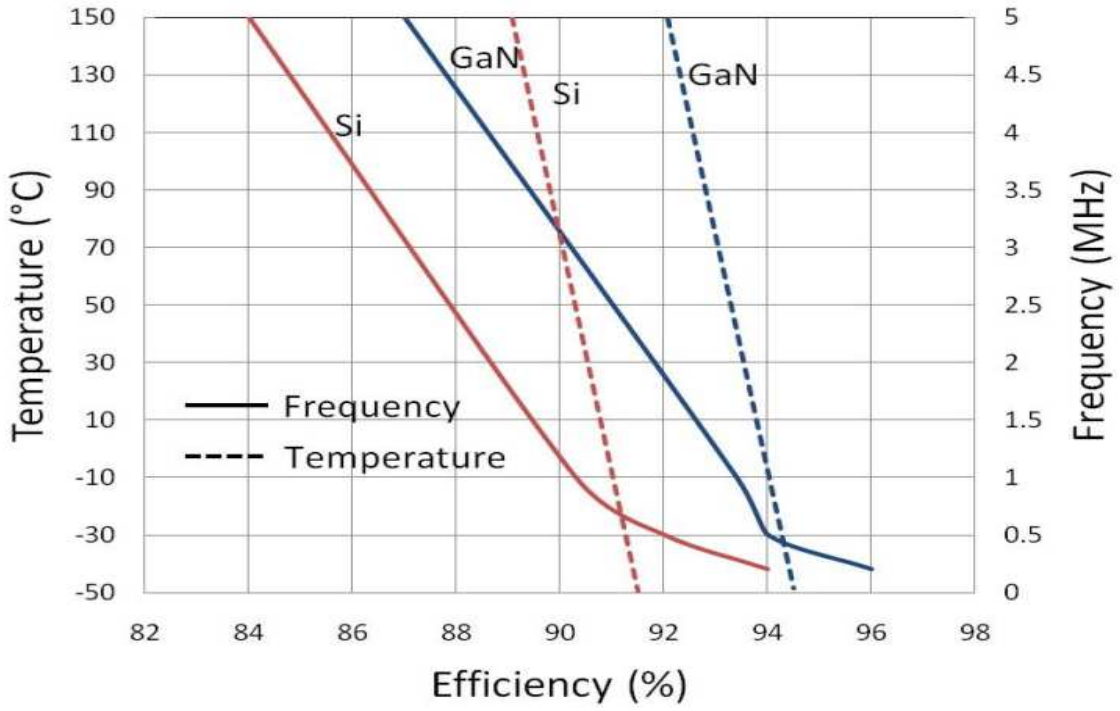


Figure 3-6: Simulation results showing efficiency vs. temperature (at 1MHz) and frequency (at a room temperature of 25°C) for a 200/380V_{DC}, 10kW DC-DC boost converter.

3.3.2 Effects of *dv/dt* stress on performance of device

dv/dt is important parameter for ruggedness of power semiconductor device(high voltage). There are two mechanism of dv/dt turn on in power MOSFET due to high *dv/dt* as shown in Figure 3-7. When voltage across gate source terminal exceeds the threshold voltage of device it gets turn on and it goes into current conduction mode. It may cause failure if device. The current flowing through transfer capacitance is proportional to *dv/dt*

across drain to source terminals as shown in (3.3).Thus higher *dv/dt* causes higher causes gate to source voltage exceed the value of threshold.

$$\frac{dv}{dt} = \frac{V_{TH}}{R_G C_{GD}} \tag{3.3}$$

In other mechanism of *dv/dt* induced turn on, higher values of *dv/dt* causes the d the parasitic bipolar transistor can turn ON. This *dv/dt* inducted turn on of device causes catastrophic failure of device. Thus *dv/dt* rating is important for high voltage devices [58].

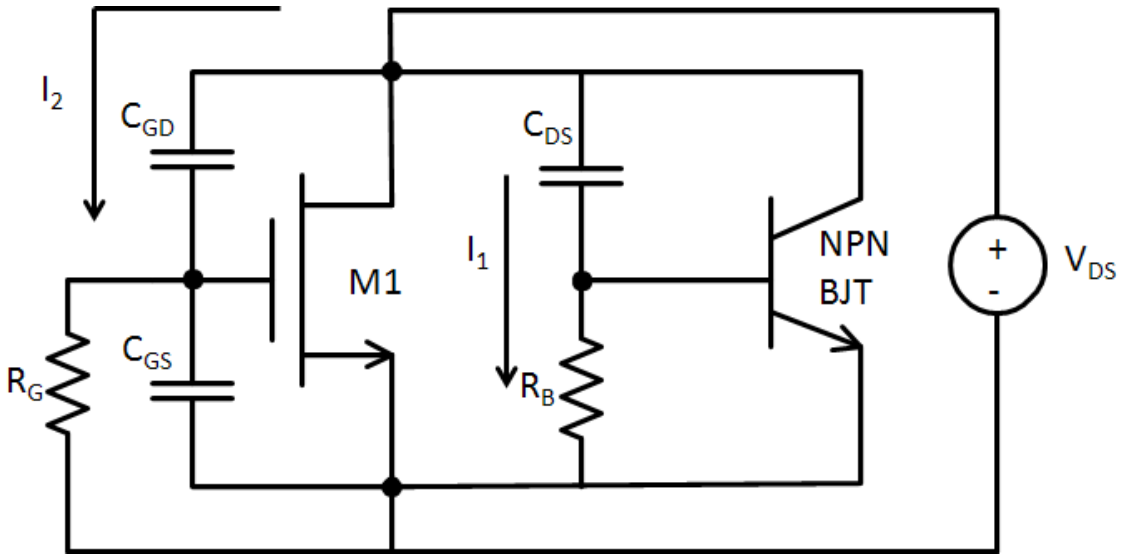


Figure 3-7: Two possible mechanism of *dv/dt* induced turn on in power MOSFETs

Table 3-3 shows the comparison of efficiency measured for various configurations of 200V/380 V, 2 kW DC-DC boost converter. It can be clearly seen that converter built using devices made of advanced new wide band semiconductor materials like SiC and GaN; has highest efficiency of 90% at 1 MHz switching frequency. The use of advanced materials like GaN and SiC has made possible to have high switching frequency for DC-DC boost converter. But the use of high switching frequency increases the *dv/dt* stress across the diode and switch as shown in Figure 3-8, Figure 3-9 Figure 3-10 and Figure 3-

11.Figure 3-8 shows *dv/dt* stress observed across diode and switch during switching for various configuration described in section 2 for DC-DC boost converter 200/380V_{DC}, 2kW measured at 1 MHz and 5 MHz for room temperature(25°C) and high temperature (150°C).

Since the gate to drain capacitance is less in GaN HEMT as compare to silicon MOSFET ; it clearly shows in the Figure 3-12 that the *dv/dt* stress across GaN HEMT is more as compare to silicon MOSFET. The threshold voltage has negative temperature coefficient and hence *dv/dt* stress reduces with temperature. The junction capacitance of silicon is less than the SiC diodes and thus it has higher *dv/dt*. During turn-on of switch after second cycle onwards the stored charge from diode is discharged into switch, this reverse stored charge causes very high voltage and *dv/dt* stress across switch. Higher *dv/dt* causes under certain conditions a catastrophic failure of device [58].

Table 3.3: Comparison of efficiency for different configuration for 200/380V_{DC}, 2kW DC-DC Boost converter

Switching Frequency (MHz)	**Efficiency of different Configuration**			
	1 (%)	**2 (%)**	**3 (%)**	**4 (%)**
1	90	85	80	86
5	83	79	74	80

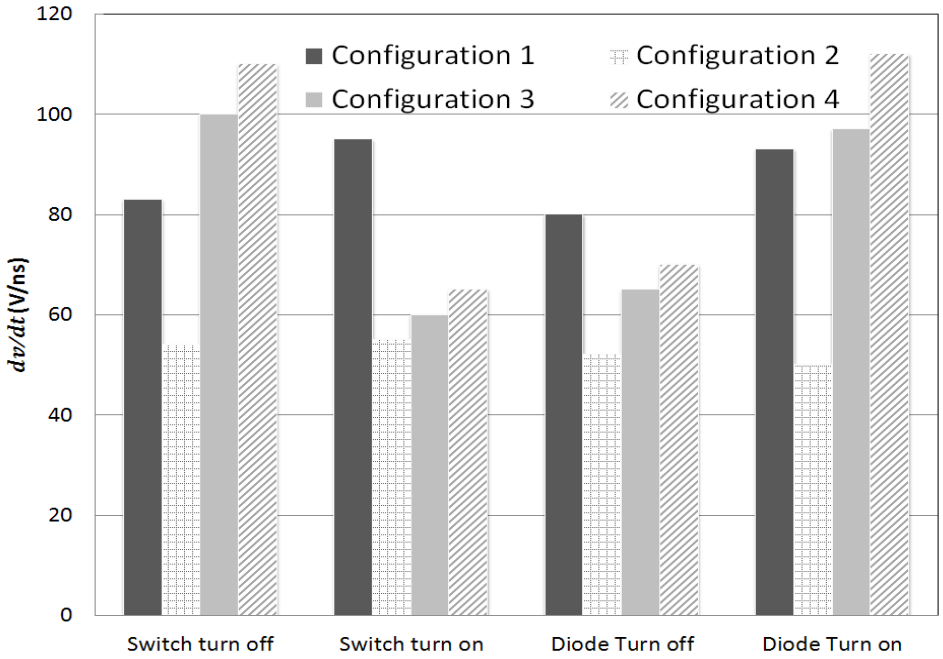


Figure 3-8: Simulation results for *dv/dt* across switch and diode during switching for various configurations of DC-DC boost converter 200/380V_{DC}, 2kW measured at 5 MHz frequency and room temperature (25°C)

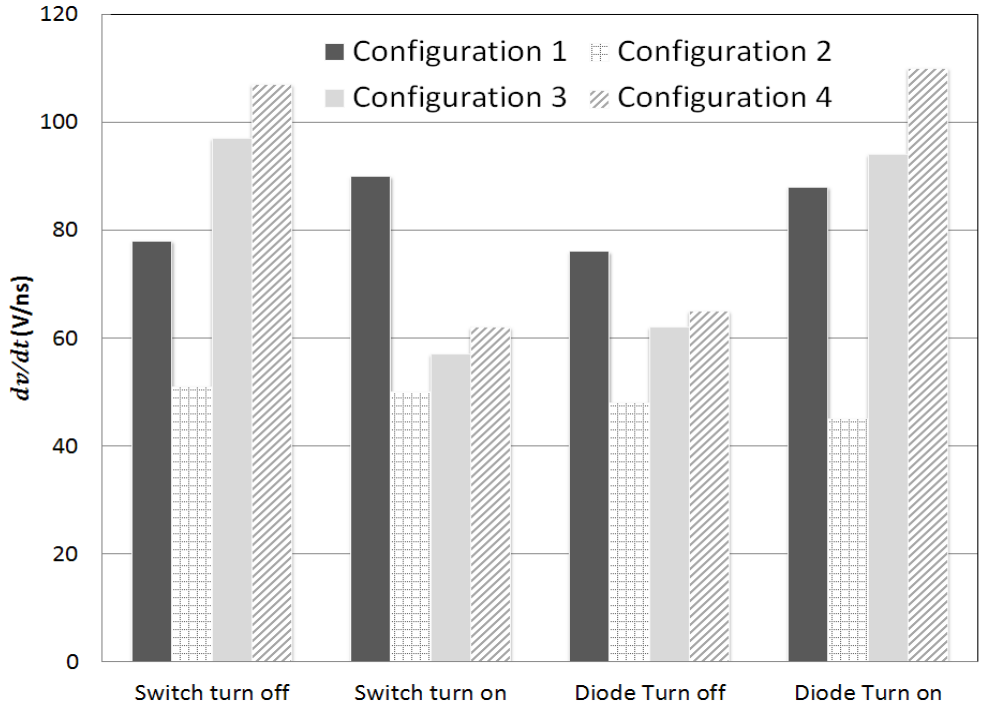


Figure 3-9: Simulation results for *dv/dt* across switch and diode during switching for various configurations of DC-DC boost converter 200/380V_{DC}, 2kW measured at 5 MHz frequency and high temperature (150°C)

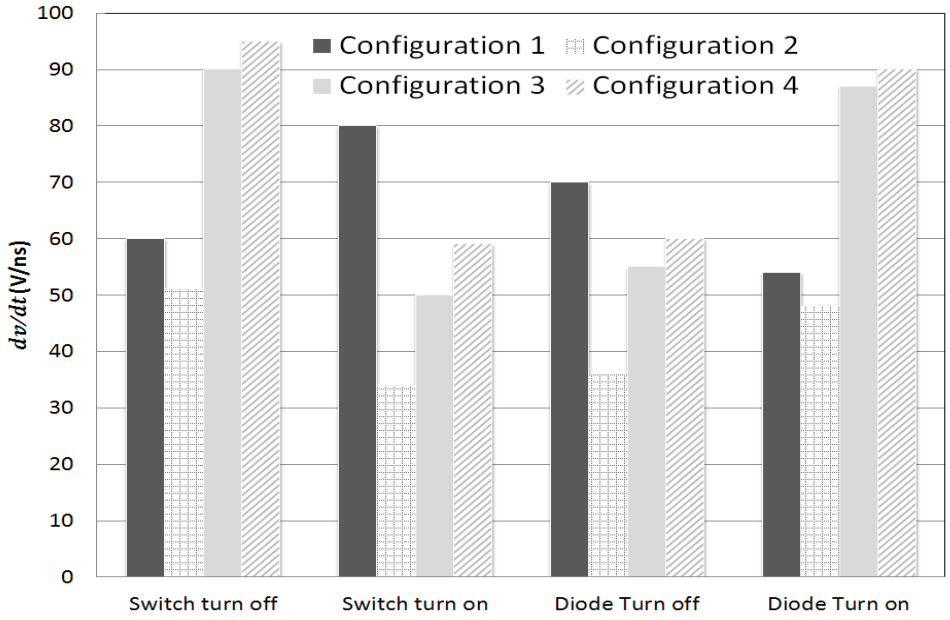


Figure 3-10: Simulation results for *dv/dt* across switch and diode during switching for various configurations of DC-DC boost converter 200/380V_{DC}, 2kW measured at 1 MHz frequency and room temperature (25°C).

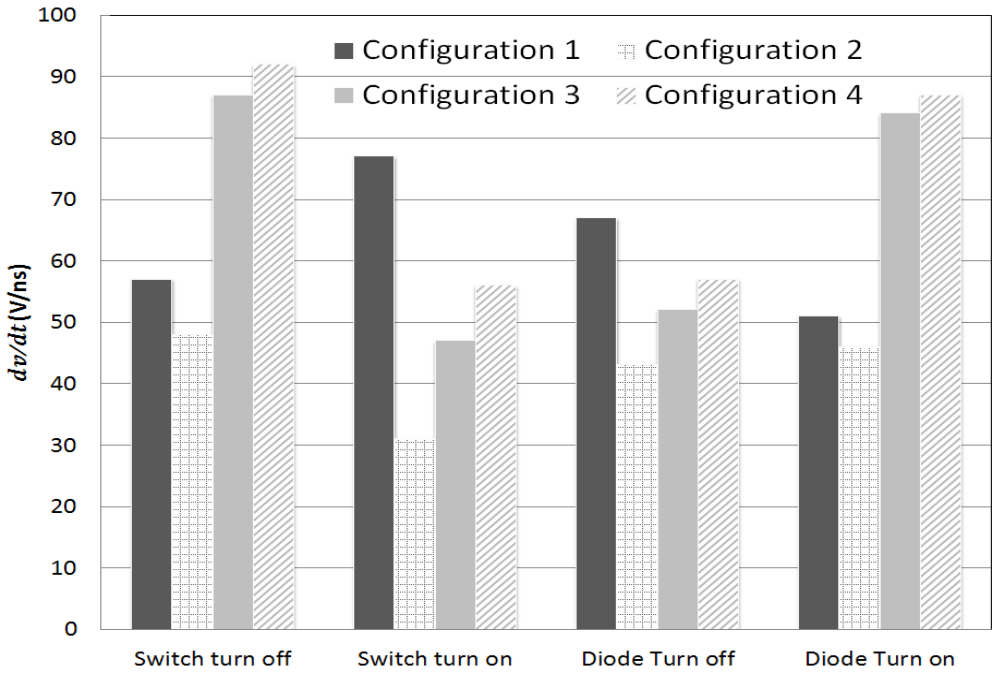


Figure 3-11: Simulation results for *dv/dt* across switch and diode during switching for various configurations of DC-DC boost converter 200/380V_{DC}, 2kW measured at 1 MHz frequency and high temperature (150°C)

Chapter 4

Conclusion and Future Work

4.1 Conclusion

A smart, DC power distribution system architecture is proposed in which available energy from renewable generators is optimally utilized to power local DC-compatible electrical loads. The proposed DC system allows for low-cost design of distributed renewable energy generators (DREGs); and is easily scalable to different power levels suitable for rapid, high-penetration of DREGs.

First-order efficiency and cost calculations are presented for a 50 kW solar PV system delivering DC power to typical building loads in addition to powering a $380V_{DC}$ computer server and plug-in hybrid electric vehicles (PHEVs). It is shown that savings of more than 10% in energy generated by the solar PV array and significant cost reduction can be accomplished using the proposed DC power distribution system compared to the conventional approach using inverters. When the current state-of-the-art silicon power converters are replaced with new and emerging GaN FET-based DC-DC power converters, further energy savings in excess of 4% can be achieved using the proposed

smart DC power distribution system. These results are based on design calculations performed for a 200V/380V, 10kW DC-DC power converter.

A simple and accurate physics based GaN HEMT circuit simulation model is reported. The parameters used here can be easily extracted from different characteristics of commercial datasheets. The model takes into account various voltage dependent capacitances and parasitic temperature dependent source and drain resistances of HEMTs and are in agreement with measured data.

The optimization of FET for buck converter topology is reported and for higher frequency FET with lowest die area for both high and low side has the lowest losses. Simulations for frequency, load and temperature variations were performed. The efficiency gain for GaN HEMTs based converter was reported approximately 3-4 % better than Silicon MOSFET converter. The calculated converter performance, however, represents a dramatic advancement towards heterogeneous chip-scale power integration in emerging Smart Grid applications.

Different configurations for boost converter were tested and it is shown that converter with GaN HEMT and SiC diode had the highest efficiency gain in comparison of other ones. It was also reported that high *dv/dt* stress of switch and diode is observed during switching for different configuration at high switching frequency. The SiC diode is bound to fail at such high *dv/dt*

4.2 Future Work

It must be noted that smart wireless sensors and controls can be incorporated within the proposed DC power system in order to further enhance energy efficiency and improve reliability. This approach is also needed to render the proposed DC power system suitable for high-penetration scenarios.

In calculating these results, we have used conservative first-order estimates for GaN FET and inductor circuit model parameters. Further efficiency improvement can be achieved when thermal management and cooling are considered; improved gate switching and *dv/dt* reduction techniques are employed. A more accurate, physics-based model for GaN HEMT is required for reliability testing and circuit simulation. The converters need to be built and tested at high frequency to validate the simulations results.

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Appendix A

Simulation and Measured Data for Si MOSFET and GaN HEMT in Circuit Model

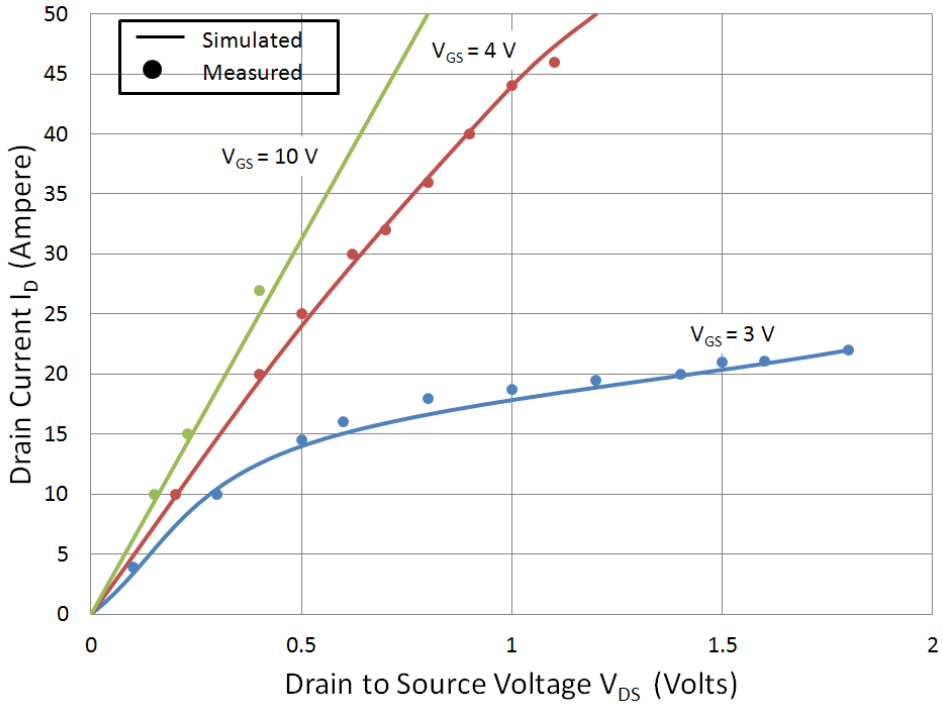

Figure A-1: Simulated and measured plot of drain current v/s drain to source voltage for varying gate to source voltage measured at room temperature (25 ^{0}C) for Si MOSFET (Si2788dp)

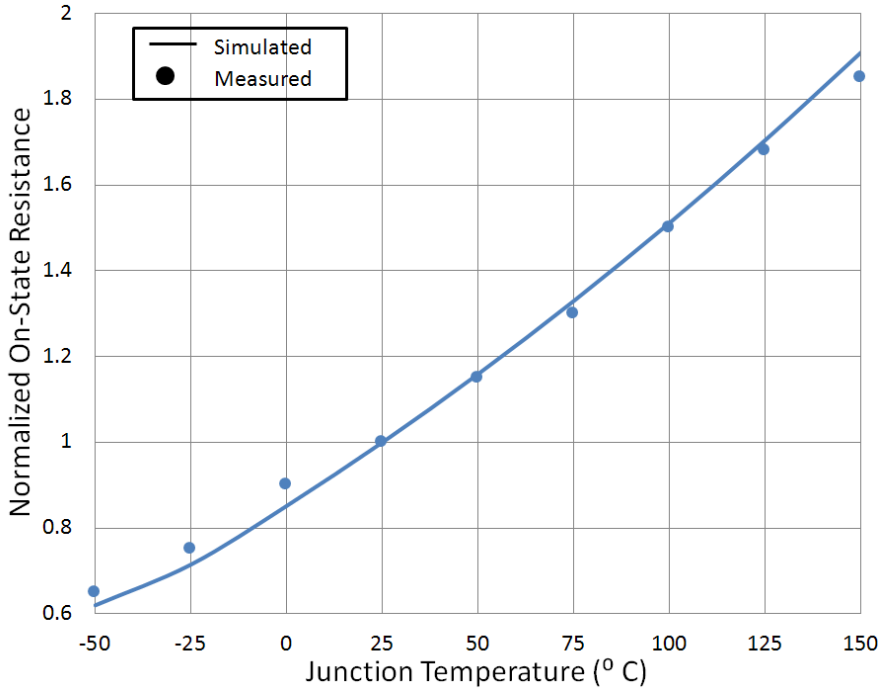

Figure A-2: Simulated and measured plot of normalized on-resistance v/s junction temperature for Si power MOSFET (Si2788dp)

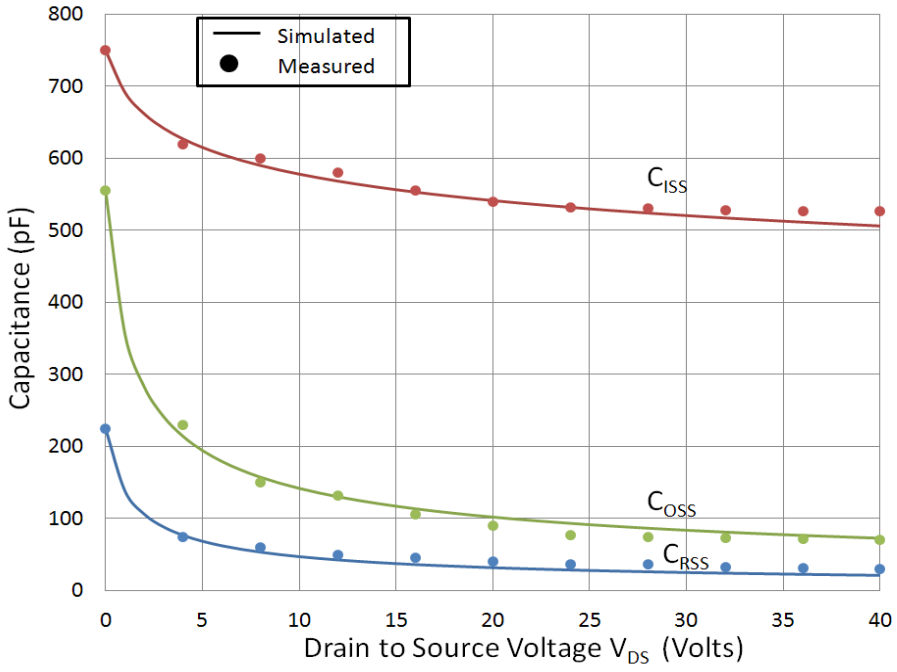

Figure A-3: Simulated and measured plot of various capacitance v/s drain to source voltage measured at room temperature (25 ^{0}C) for Si power MOSFET (Si2788dp)

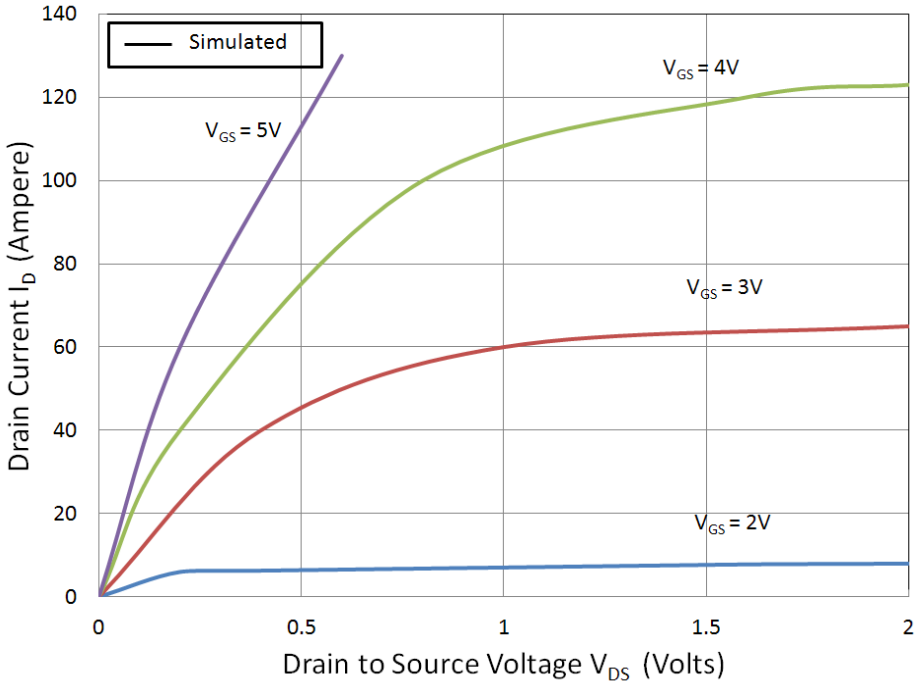

Figure A-4: Simulated and measured plot of drain current v/s drain to source voltage for varying gate to source voltage measured at room temperature (25 ^{0}C) for 600V/30A GaN HEMT

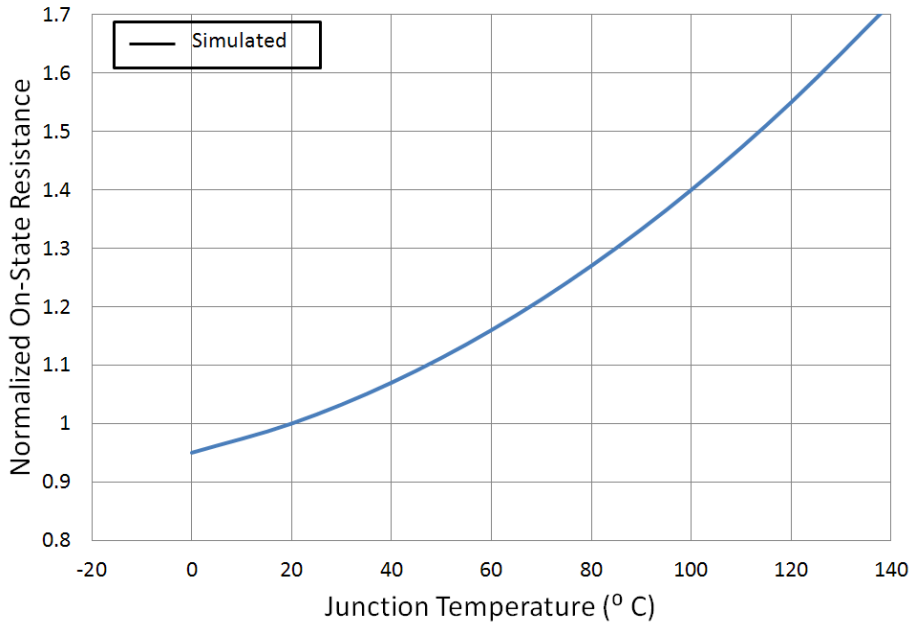

Figure A-5: Simulated plot of normalized on-resistance v/s junction temperature for 600V/30A GaN HEMT

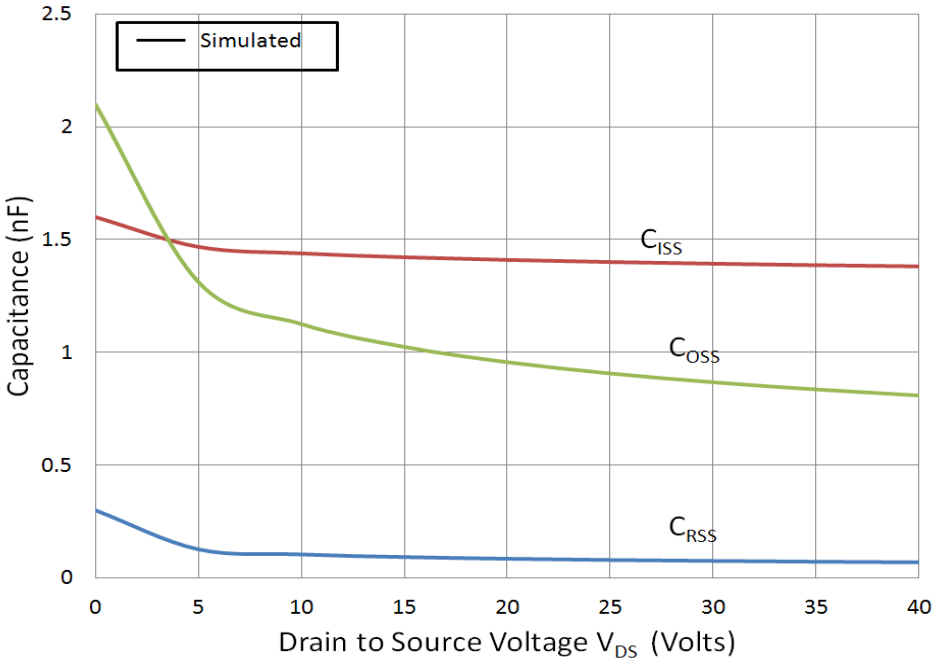

Figure A-6: Simulated plot of various capacitance v/s drain to source volatge measured at room temperature (25 ^{0}C) for 600V/30A GaN HEMT

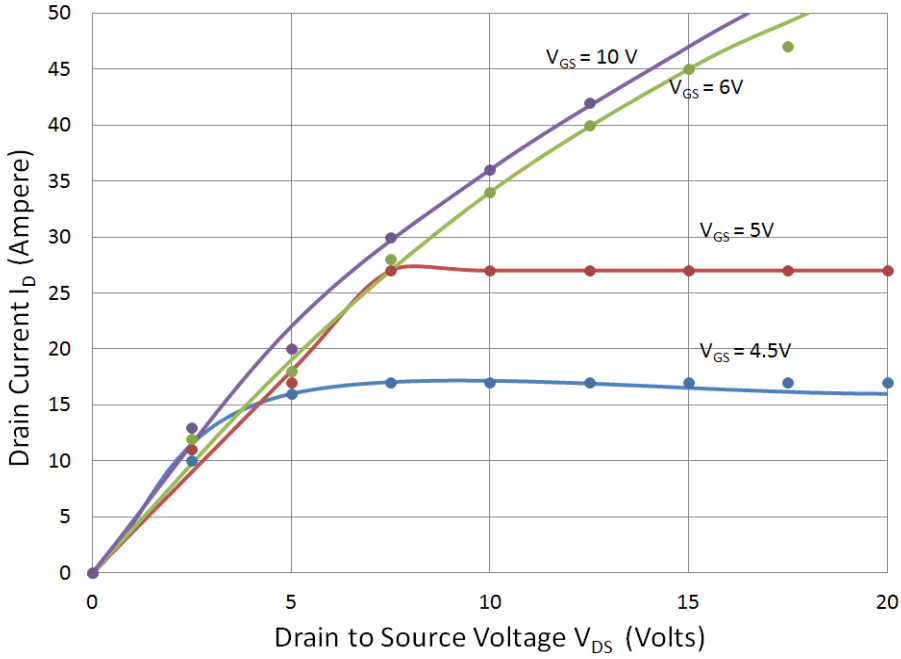

Figure A-7: Simulated and measured plot of drain current v/s drain to source voltage for varying gate to source voltage measured at room temperature (25 ^{0}C) for Si MOSFET (IPB60R099CP)

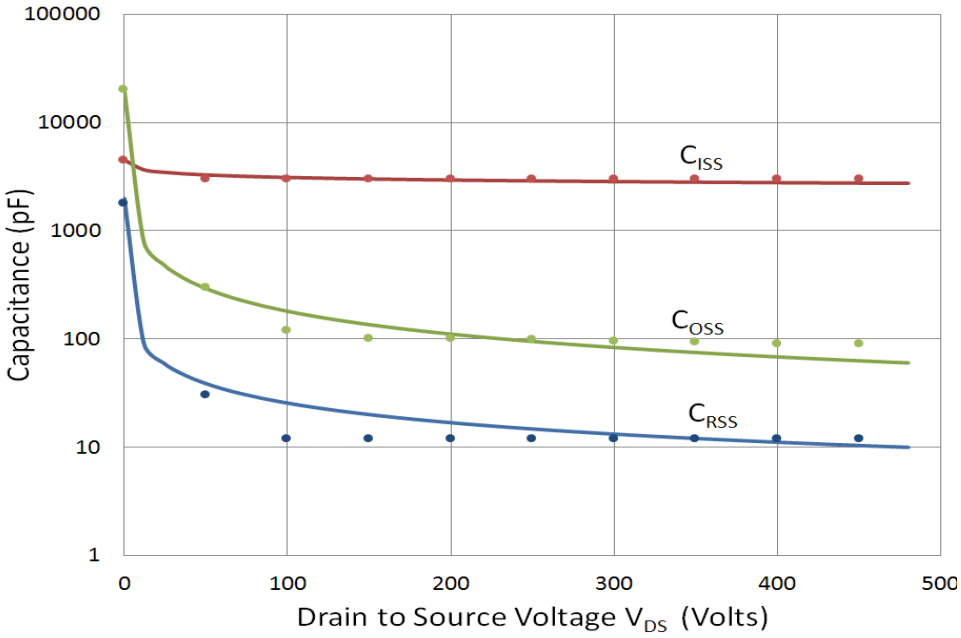

Figure A-8: Simulated and measured plot of various capacitance v/s drain to source voltage measured at room temperature (25 ^{0}C) for Si MOSFET (IPB60R099CP)

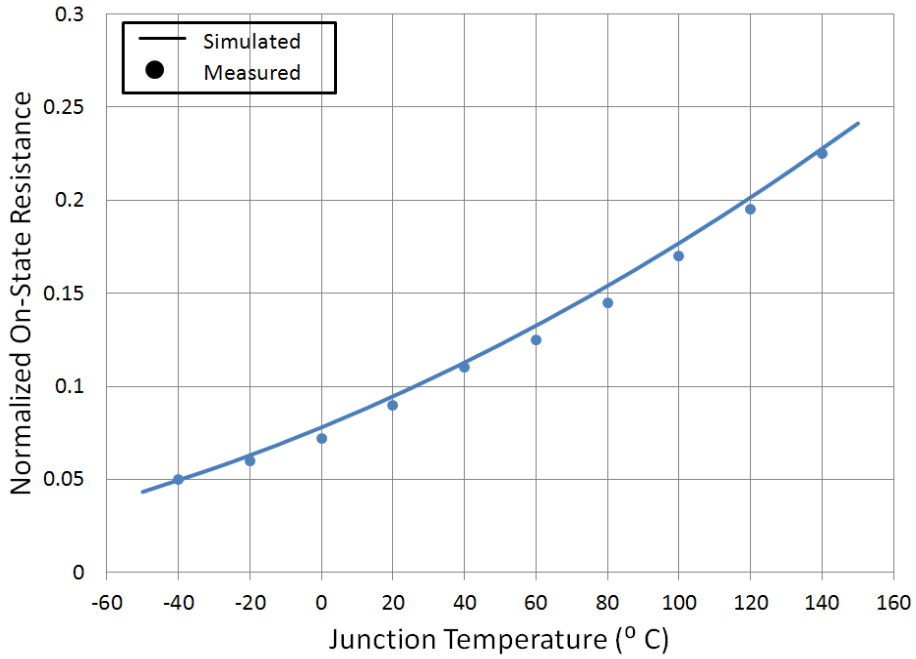

Figure A-9: Simulated and measured plot of normalized on-resistance v/s junction temperature for Si MOSFET (IPB60R099CP)