A High Speed Digital Receiver for an Instrumentation Radar System

A Thesis

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By

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ABSTRACT

Wireless communication systems have enjoyed explosive growth over the past few years. As demands for increased capacity and quality grow, improved interface with high speed and flexibility must be implemented. The use of newly-developed analog, digital and DSP hardware make it possible to meet these needs. With proper hardware and software interface between those components, one can actually build up a versatile system which can be used to communicate with many devices with different protocols, to form a simple measurement instrument or the front end of the software radio system, etc. This thesis describes a new wireless receiver that has been interfaced to compact range radar system at the ElectroSeience Laboratory of the Ohio State University. It also describes how the software and hardware system are used to interface the radar with the computer system in order to control the radar system and collect the data.

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To my family

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Team effort make this hardware system development possible. Special thanks to Gary Winchell for making those print circuit boards and giving me technical advices, and to Willie Theunissen for his patience and programming effort throughout the system testing.

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CHAPTER 1

INTRODUCTION

1.1 Motivation

The Compact Range measurement system at the Electro-Science Laboratory of the Ohio State University has recently been upgraded [1,2]. For the hardware system, the transmitter and receiver have been replaced by a completely redesigned transceiver system for greater dynamic range, better stability, greater precision and shorter data acquisition time. As for the software system , it had been completely redesigned to be able to control all the hardware function for data collection. It also provides a user friendliness, self-test and maintenance features. Recently, part of the radar system has been upgraded again in order to simplify the hardware architecture , increase the speed for data acquisition, enhance data processing and provide a more user friendly graphical interface. In particular, the IBM PC and workstation have been replaced by a single Pentium III 750MHz PC. And the old DSP hardware(A/D Converter, Digital Downconverters ,accumulators) has also been replaced by a newly-developed AD and DDC board, plus a new DSP board for faster data output and lower cost. In addition, a high speed PIO board has been added into the system for faster data acquisition. Finally, the system software has been ported from ASYST and Assembly Language

to Delphi to provide a nice graphical interface and software integration. This thesis provides the brief overview of the compact range principles and the measurement system, introduces how the measurement system functions and details the hardware and software design of the new data acquisition hardware and software systems.

1.2 Objective and Outline of Thesis

The aim of this thesis is twofold. The first aim is to provide an overview of the hardware of the radar system that was done previously and how it operates. Secondly, this thesis details the development of the new data acquisition system (DAS) and some basic changes that have been made in the measurement system architecture.

The thesis is organized into six chapters. Chapter 2 provides an overview of the compact range principles , the radar system layout and the basic operation of the radar system. Chapter 3 covers the overview of the new DAS system architecture and how it fits into the overall radar system. The basic architecture and performance specifications of each component are also included. Chapter 4 gives the flow diagrams of the programs used to generate the control words of Digital Down Converter (DDC) and the one that controls the DAS board. It also gives a detailed description about how the DAS provides the interface between the DDC and the high speed PIO board. Chapter 5 includes the performance analysis of the entire DAS and the performance test of the entire radar system. Chapter 6 concludes with a summary of the requirements of the radar system, the design of the DAS and its performance.

1.3 Contribution

Author's contribution to this project is to design the architecture of the DAS system, optimize the system performance, solve the interface problems among the components of the system, DSP programming and perform the system testing all together with the instrumentation radar system.

CHAPTER 2

COMPACT RANGE PRINCIPLES AND SYSTEM OVERVIEW

Compact range radar cross-section (RCS) measurement system has been used at the ElectroScienceLaboratory for years. This chapter provides a brief introduction to this system in terms of its basic layout and operation.

It very helpful to do the time domain analysis of radar target signature in terms of understanding the scattering characteristics of a target. Since it is easier to do the measurement in the frequency domain than in the time domain, a better approach is to apply an inverse Fourier transform to the data in frequency domain to get the time domain data samples. This method is known as a RCS frequency scan. A block diagram of a RCS measurement system is shown in Figure 2.2. It consists of several components including a swept-frequency transmitter, an antenna system, a receiver, a recording and processing system and a target pedestal which can be used to hold and rotate the target. The signal from transmitter is routed to a T/R switch which connects the transmit pulse with the feed antenna. This illuminates the target and creates a scattered field. This scattered signal from the target is received by the feed antenna and routed by the same T/R switch to the receiver where it is sampled for further processing. To make a valid RCS measurement, the radar target must be

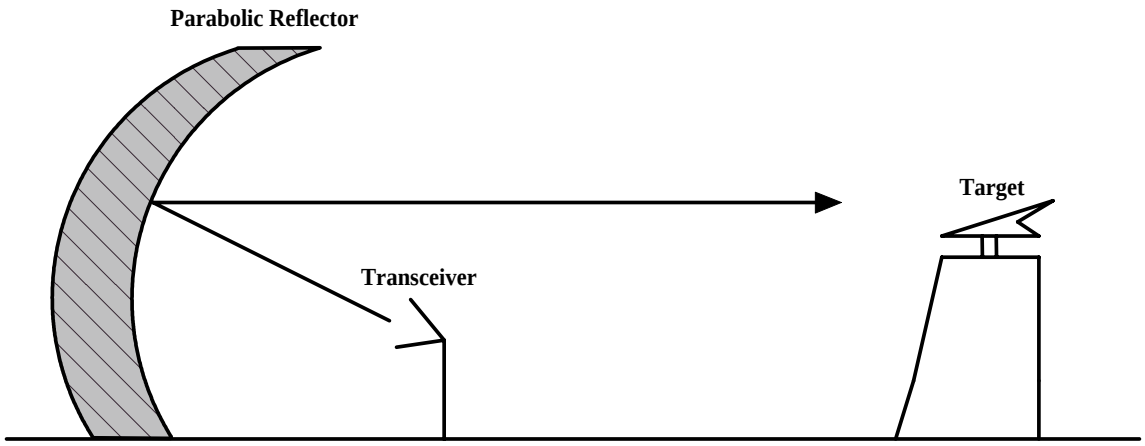


Figure 2.1: A compact RCS measurement range

in the far field which means that it takes a lot of space to build the system. One solution to this requirement is to use a parabolic reflector and place the feed antenna at the focus of the reflector as shown in Figure 2.1. This system is called the Compact Range RCS measurement system. With this type of range, a lot of space can be saved and the measurement can be performed indoors. Even though the parabolic reflector creates the desired plane wave illumination of the target, a few error terms are shown in the Figure 2.2. To minimize the interference terms, one must apply various types of solutions. Some specific examples are presented here.

2.1 Range Gating

The stray signals from different scatters arrive at different times since the distance between the transceiver and each of those scatters are different. By having high speed pin diodes switches in the transmit and receive paths as shown in Figure 2.3, one can gate out many of the undesired error terms. However, some of the error terms can be

used as the reference to calibrate the measured signals. Data referencing in the next section provides a good example of this concept. A timing diagram of the received signal is shown in Figure 2.4.

2.2 Data Referencing

To improve the accuracy of the measurement, drift in the system components must be removed effectively. It is implemented by putting a reference target at a different range from the desired target and gating the receiver alternatively between the desired target and the reference target. Every time a data sample is taken , the system collects the response from both the desired target and the reference target. Then the desired target data is divided by the reference target data so that the drift in the system is minimized. In some cases, the scattered signal from the parabolic reflector is used as the reference terms in the OSU compact range system.

2.3 Background Subtraction

With range gating, one can only get rid of the interference signals outside the target range gate.Thus, the target data is still corrupted by the interference at the same range as the target(i.e. the target support pedestal.). Thus, a background subtraction technique is implemented to remove some of the target/pedestal interaction errors by subtracting the no-target data from the target measurement . Note that data referencing is applied during both measurements.

2.4 Calibration

Calibration of the measured target data is implemented by dividing the measured target data by a measured calibration target data set and multipling by the exact

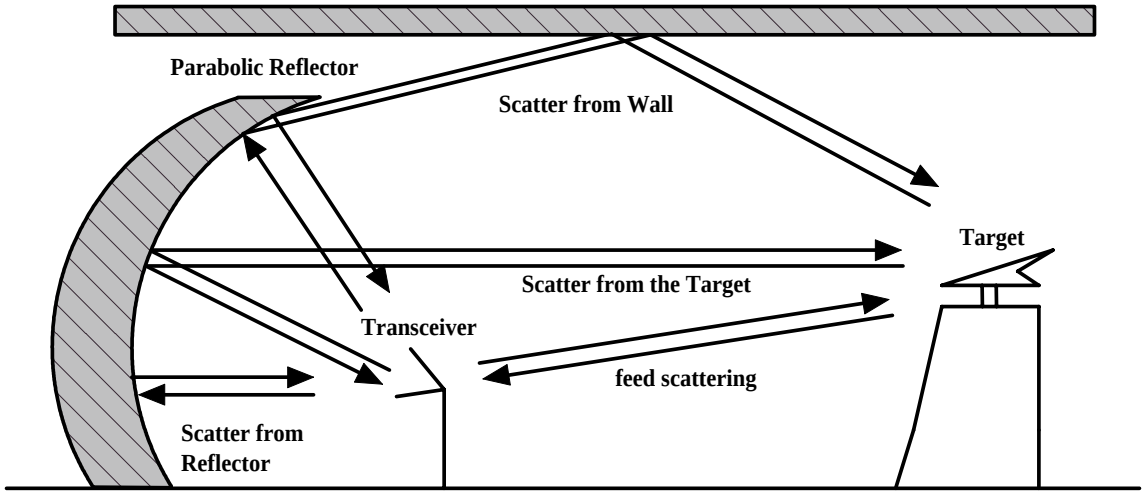


Figure 2.2: Multiple Scatterers in compact range system

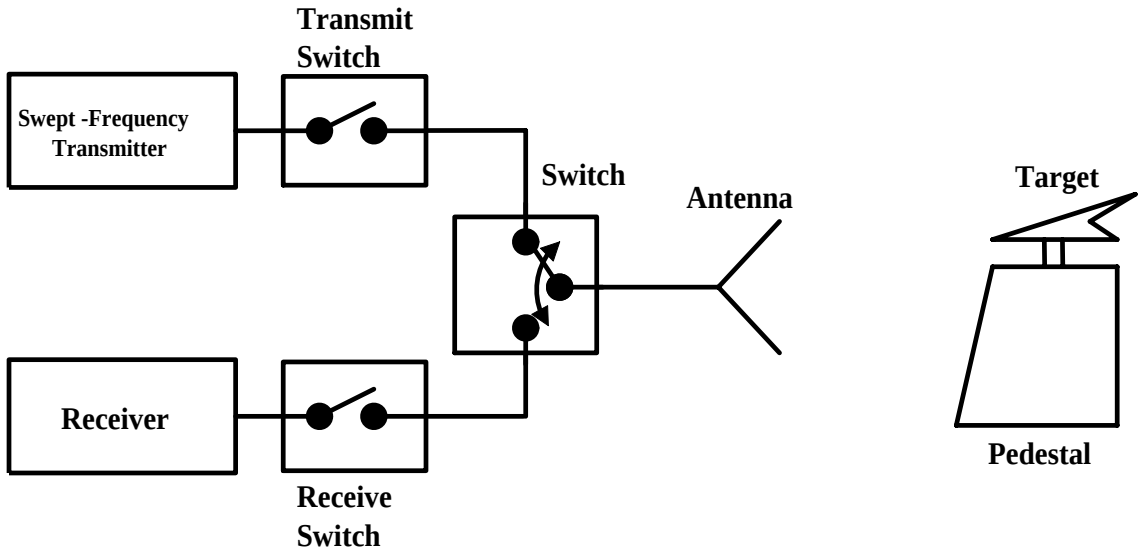


Figure 2.3: A pulsed RCS measurement system

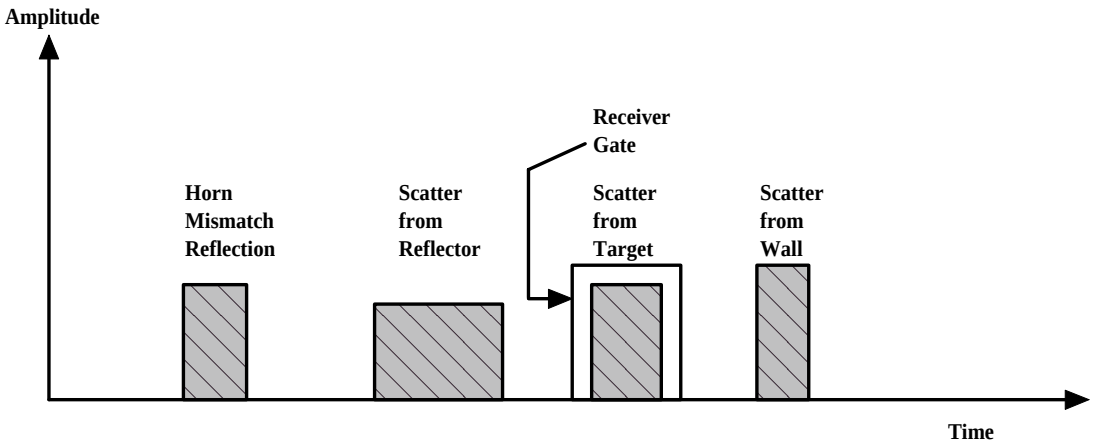


Figure 2.4: Compact range system timing diagram

calibration target solution. The complete calibration equation is given by

$$T_c = \left(\frac{T - B_t}{C - B_c} \right) E \tag{2.1}$$

where

T =target measured data

B_t =target background

C =calibration target measured data

B_c =calibration target background, and

E =exact solution for calibration target

2.5 Basic Radar Layout and Operation

The radar system is composed of the transceiver, the frequency synthesizer and the pedestal controller as shown in Figure 2.5. The operation and the layout of these subsystems are briefly discussed in the following sections.

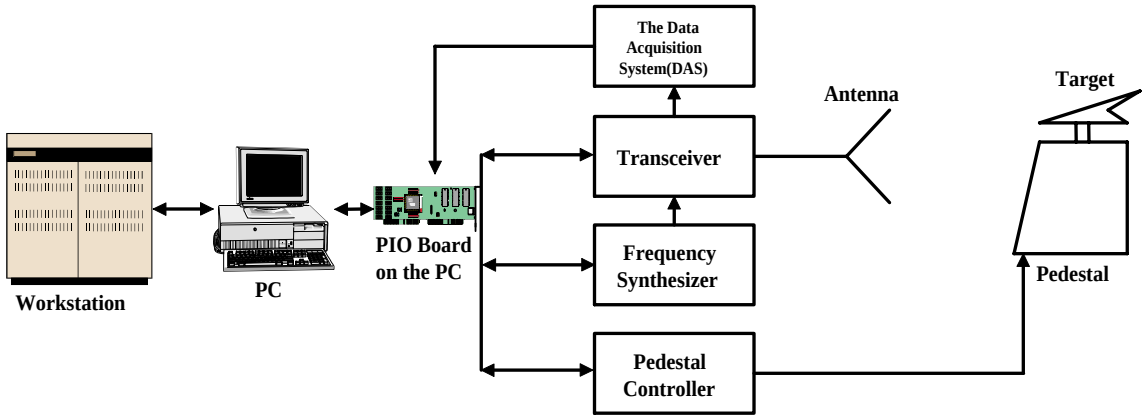


Figure 2.5: The Radar System Diagram

2.5.1 Transceiver

The transceiver can operate in several different frequency bands. They are separated hardware sections that function from 0.3 to 1 GHz, 2 to 18GHz, 27 to 36GHz and 90 to 100GHz. These frequency ranges are divided into bands because broadband components working across the entire frequency band is not possible. For the transmitter, two PIN diode switches are used to provide the pulsed CW transmission. A simplified layout is shown in Figures 2.6 and 2.7. It should be noticed that the frequency synthesizer which is controlled by the computer serves as the first LO. And the other two mixers with intermediate frequencies at 1.5GHz and 11.7MHz serve

as the second and third LO. They are all used in both the transmitter and receiver sections to downconvert and upconvert the signal to the desired frequences. Besides, all of the attenuators and YIG filters are controlled by the system computer to provide desired signal level and filter characteristics. The power information which is monitored by detectors, D1-D5, and can be read by the computer through auxiliary AD converters. The auxiliary AD converter is composed of a 12-bit AD converter and an 8 channel multiplexor. That means up to 8 detectors can be used to monitor the system information. Finally, switches in the transreceiver are used to select signal paths for loop back tests, multiple band control and time gating. A highly stable clock signal serves as the frequency reference for the overall radar system.

2.5.2 Frequency Synthesizer

The frequency synthesizer serves as the first LO and is able to synthesize a single frequency ranging from 2GHz to 18GHz. It takes about 200 micro seconds to lock the frequency when it performs a frequency scan with a 20MHz increment. It is controlled by the system computer through a PIO compatible interface.

2.5.3 Pedestal Controller

The pedestal controller is used to set up the azimuth angle of the target and how fast it rotates. The angle can be set ranging from 0 to 359.99 degrees. Its minimum angular increment is 0.01 degree. As for the speed, it can be set from 0 to 4095 units using acceleration unit that can be set from 0 to 7. It is also controlled by the system computer through the PIO bus with secondary addresses 6 and 7.

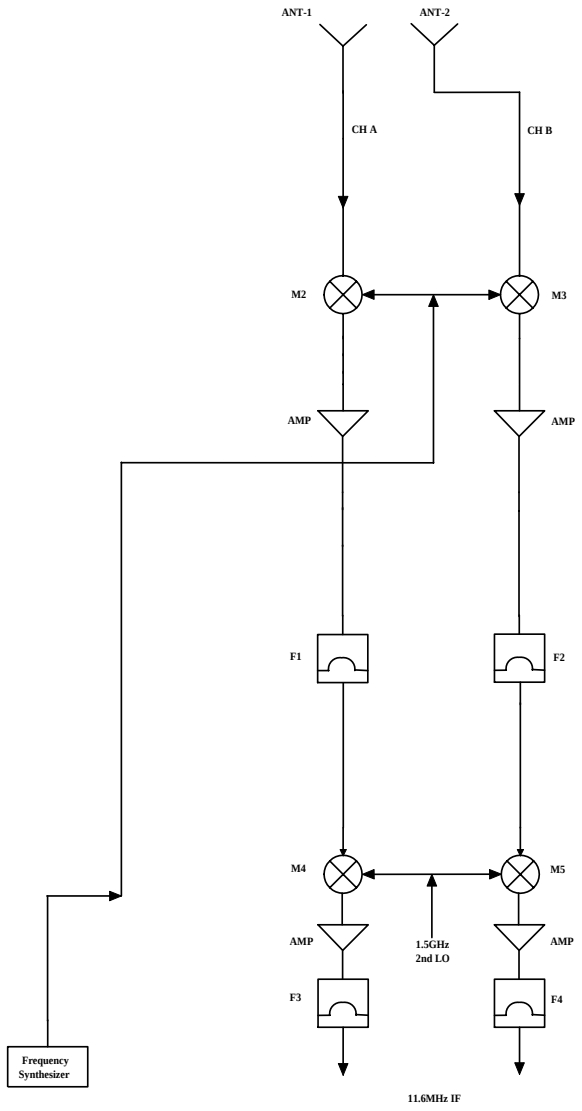


Figure 2.6: The Radar System Diagram of the RF Section (Simplified)

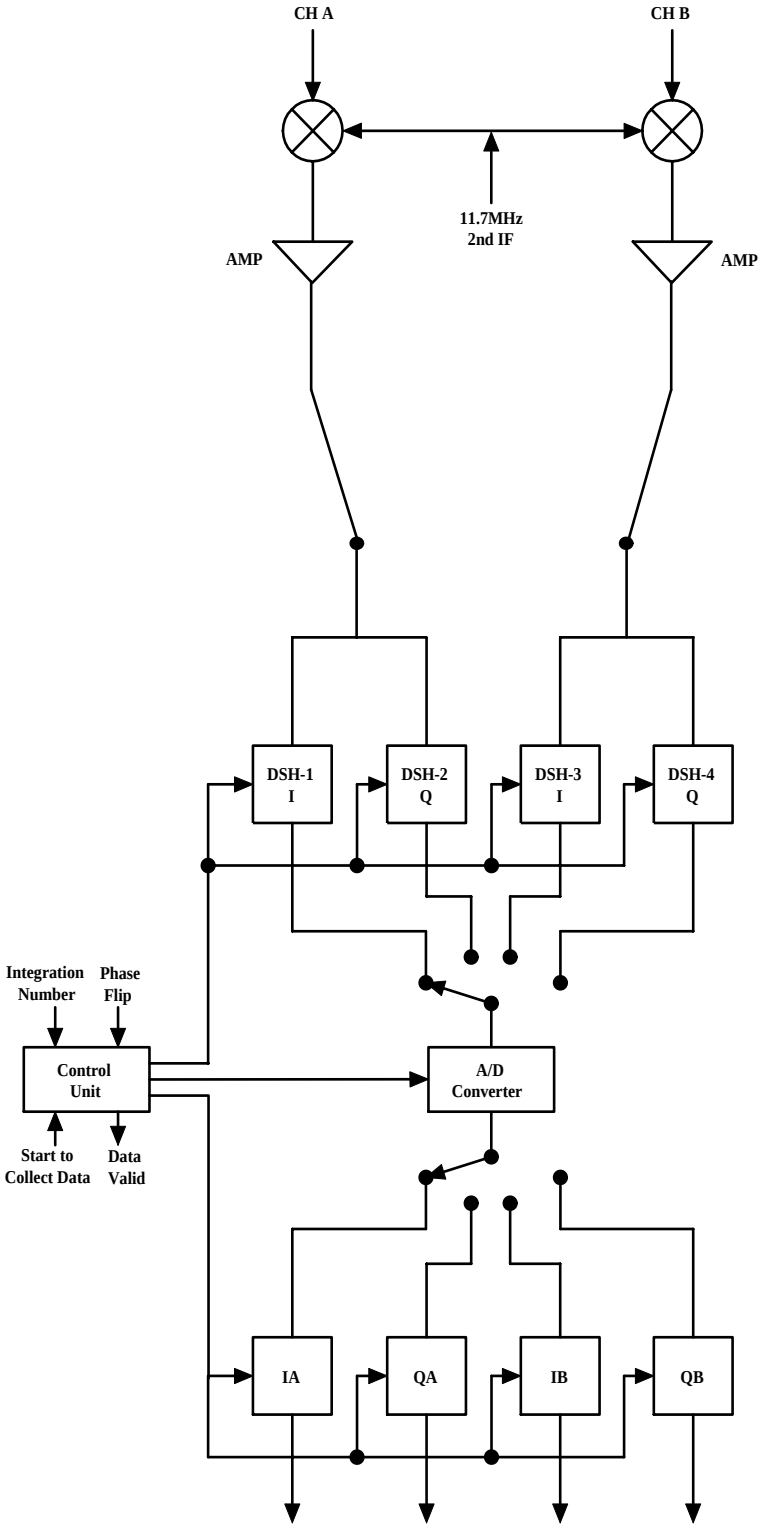


Figure 2.7: The Radar System of the IF Section (Simplified)

2.5.4 The Data Acquisition System (DAS)

The DAS system is the composed of the 3rd LO, phase shifters, sample and hold circuits, a 16-bit AD converter and a set of 24-bit accumulators. (24-bit accumulators are needed because the maximum integration number of the system is 256.)

A few steps are taken during the digitization process. First, the signal is mixed with 11.7MHz IF reference to downconvert the signal to the 100KHz. The signals are subsquently sent to the in-phase and quadrature synchronous detectors and the sample and hold circuit, DSH-1 and DSH-2 which are controlled by the system computer through the control unit. Then the output of the detectors goes to a 16-bit AD converter for digitalization. The output of AD converter goes to the 24-bit accumulator for accumulation. It should be noted that during the system initialization process, the intergration number(Address 0)is sent to the control unit and the phase flip is disabled. Then a trigger signal is sent to the control unit and the DAS begins to take the specific number of samples and add them up in the accumulators. Once the computation is complete, the data valid line is set to high and the computer reads the output of the accumulators.

The "phase-flip" mechanism is implemented in order to get rid of the DC offset in the A/D converter. When it is enabled, the 100KHz references are shifted 180 degree out of phase so that the DC offset of the analog circuits are subtracted from the accumulator. Usually the measurement result with and without phase flipping are taken in turns. And they are added together so that the DC offset is minimized in the final result.

2.5.5 The Parallel I/O Control System through Secondary Address

The Parallel I/O (PIO) Control system is composed of a 24-bit digital PIO board and the system computer. The 24-bit I/O bus is divided into 3 8-bit ports, A (data output),B(data input) and C(address output). The secondary addresses are assigned to each controller of the system. Every time the computer needs to control a device, it sends the specific address to port C. Then the commands are sent through port A and the response or data from the devices are received through port B. The most significant bit of port C is used to send the data strobe signal.

For devices other than the pulse timing unit, input or output is performed by following steps below:

1. Send 128 plus the secondary address to port C through the PIO.
2. Send the secondary address to port C through the PIO.
3. Send the command to port B throught the PIO or collect the data from the other devices at port A.
4. Send 128 to port C through the PIO (end of session).

For timing units, commands are sent by following steps below:

1. Send 128 plus the secondary address to port C through the PIO.
2. Send the command to port B through the PIO.
3. Send the secondary address to port C through the PIO.
4. Send 128 plus the secondary address to port C through the PIO.
5. Send 128 to port C through the PIO (end of session).

The Secondary Addresses for various transceiver components and their functions are shown in Table 2.1. It should be noted that the new digital receiver does not exactly follow the steps mentioned on the last page. It goes as follows.

For the DDC board, sending the control sequence is performed by the following steps:

1. Send 128 plus the secondary address (1) to port C through the PIO.
2. Send the secondary address (1) to port C through the PIO.
3. Send the control words of from port B to the DDC throught the PIO.
4. Send 128 to port C through the PIO (end of session).

For the DSP board, sending the instructions is performed by the following steps:

1. Send 128 plus the secondary address (1) to port C through the PIO.
2. Send the secondary address (1) to port C through the PIO.
3. Send the instructions from port C to the DSP board throught the PIO.
4. Send 128 to port C through the PIO (end of session).

It should be noted that the Secondary Address Schemes for the DSP and the DDC board are different from those of the other devices. First, for the DDC, control words are sent through Port B only during the system initialization process. And for the DSP board, instructions are sent through Port C which is normally used as a address port.

The control words sending to the DDC is generated by the control word generator described in Section 4.1. And the instruction set is detailed in Section 4.2.2. The connection between the secondary address board and the DDC board is detailed in Table A.1 (Appendix). And the detailed description of the Secondary Addresses is shown in Table B.1 (Appendix).

2.6 Summary

A RCS measurement compact-range radar system is used to provide an easier way to probe the scattering characteristics of a target without using a lot of space. To get rid of the problems come with a compact range measurement system, range gating, data referencing, background subtraction and calibration techniques are applied.

To be able to control several devices of the radar system using a PC, a unique secondary address and a set of the secondary board is assigned to each device to avoid data or instruction conflict. It should be noted that the secondary address schemes of the DDC and the DSP board are differnt from those of the other devices.

CHAPTER 3

HARDWARE DESIGN AND PERFORMANCE

This chapter describes in detail the design of the new Data Acquisition System (DAS). It includes the system overview, how the new DAS fits into the existing radar system and a brief description about the architecture and performance of each of the key components in the system. To better illustrate how the interface works between the DSP and fast PIO works, it is discussed in terms of a low-level signal flow diagram in the next chapter. The software will also be presented in Chapter 4.

3.1 System Overview

The system block diagram which highlights the signal flow is shown in Figure 3.1. First, the 11.6 MHz IF signal from the radar system is connected directly to the AD converter as the analog input signal. And the 11.6MHz reference signal from radar is multiplied by four in frequency to avoid aliasing and serves as the AD converter clock signal. The output of the AD is a 12-bit digital signal that is directly connected to the digital down converter(DDC). Since the DDC can accept up to 16-bit input, the input for the 4 lower bits of the DDC are grounded to match the output of the AD converter. This provides a additional processing gain to the system. The DDC is programmable and the control words are sent during the system initialization

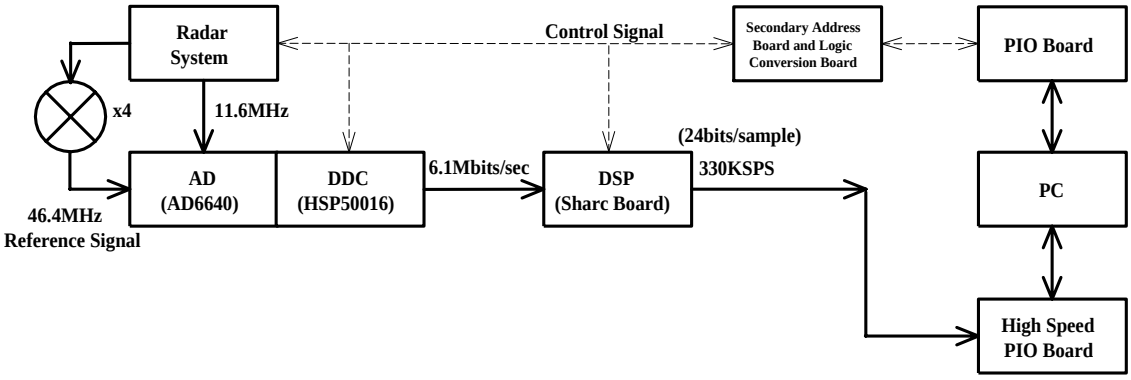


Figure 3.1: DAS System Diagram

process to the DDC using a PIO interface which is controlled by PC. This provides flexibility to change the central frequency(equivalent to the 3rd LO frequency in the old system) and the bandwidth of DDC for system optimization. Thus, the user can control all these parameters including the decimation factor. With a smaller decimation factor, both the bandwidth of the LPF in the DDC and output data rate increase. And with a higher clock frequency, the bandwidth of the LPF, central frequency and output data rate of the DDC increase. To ensure that the system can work properly, the decimation factor should be chosen with care. That means that the physical limitation of the DSP and PIO board, such as maximum input and output data rate, processing speed of DSP board, etc. need to be taken into consideration. In this system, the desired bandwidth is 100KHz, the desired central downconverting frequency is 11.6MHz and the decimation factor is chosen to be 64 to meet the bandwidth requirement. Thus, the output rate of the DDC is set to be 6.1Mbits/sec.

The DSP board is used to reformat the serial data input from the DDC to a 24-bit parallel data output word that is sent to the high-speed PIO board. The serial input data is received by the SPORT1 on the DSP board, accumulated several times according to the integration number initialized by the system PC and then sends the resulting output data to the external port of the DSP board. The maximum input rate of the SPORT1 is suppose to be 40Mbits/sec, but to provide sufficient time for the DSP to process the data, an input data rate lower than 20Mbits/sec is recommanded. The maximum output rate of the external port on the DSP is 2.7MSPS(with a 32-bit word width).

Since the external port on the DSP board can easily be damaged if instructions are sent to it when it attempts to write out the data, the external port is configured in a way such that the data is sent via the address port and the data port is only used to read instructions to ensure the external port is always safe from damage.

The high-speed PIO board is then used for data collection. The maximum input data rate for this PIO is 3.1MSPS (24-bit channel width) in level-ACK mode (level-acknowledge mode for asynchronous signal). This data goes through the DMA channel to the PC so that CPU time is saved and can be used for more intensive data processing tasks.

The PIO board is used to control several components of the radar system , to send instructions to the DSP board and to send control words to the DDC chip during the system initialization process. It should be noted that a Secondary Address scheme is used every time the PIO sends or receives data to avoid conflicts among the several devices controlled by this PIO interface.

3.2 Comparison between the old and new Data Acqusition System (DAS)

The old and new Data Acqusition System diagrams are shown respectively in Figures 3.2 and 3.3. It can be seen from these figure that the new DAS has a much simpler architecture than the old one. One may wonder if the new system trades the performance for simplicity, but actually the new system is faster, more reliable, accurate and less expensive than the old one. A few reasons about why the new system is better are briefly discussed in the following paragraphs.

1)The IF signal is downconverted digitally. Basically, analog downconversion produces image and linearity problems. These problems are elimiated by digital downconversion.

2)The I and Q channels are separated digitally. One should note that the old analog generated I and Q channels tend to have bias errors which means that they are not orthogonal or of equal amplitude. This can result in distortion and spurious components in the center of passband(DC). With the I and Q channels sythesized digitally, the I/Q balance is very nearly perfect.

3)The new AD works much faster than the old one. Based on the old system, a new sample is obtained every 200 micro seconds (when integration number is equal to 1). The new system takes only about 6 micro seconds to complete the same task (about 33 times faster) .

4)The output data from DSP is always valid. In the old DAS, the output of the accumulators is always present even before the calculation is done. Thus, a data valid line is needed to tell the PC that the accumulation is done and that the data result is ready. In the new system, the raw data is accumulated in the DSP board.

And the DSP board is programmed in a way such that the result is only sent after the calculation is completed. So, the data valid line is no longer needed in the new system.

5)The DSP board provides a more flexible structure. The DSP is capable of receiving, refomating and then sending data at a very high data rate. So users have more freedom to chose the communication port and protocol to maximize system performance. By using several high speed switches, one can easily expand the system to handle multiple channels.

3.3 AD Converter

The AD converter used in the system is an Analog Device AD6640 locked at 46.4MHz (4x11.6MHz). Its functional block diagram is shown in Figure 3.4[3]. Although the maximum sample rate allowed with the AD6640 is 65MSPS, the maximum sample rate can be up to 70 MSPS.

The 11.6MHz IF signal in the system is oversampled at 46.4MSPS. This oversampling gives a processing gain because the faster the signal digitized, the wider the distribution of noise. And since the noise power must remain constant, the actual noise floor is lowered by 3dB each time the sample rate is doubled.

The maximum analog input frequency is 300 MHz. This makes the AD6640 capable of doing bandpass sampling where the bandpass signal is aliased down to the baseband in the same manner that a mixer down-converts a bandpass signal. There are a couple of benefits for doing this. First, it is very useful to eliminate the complete mixer stage including amplifiers, filters and other components, reducing cost and power dissipation. With a 46.4MHz clock , the ADC typically is used

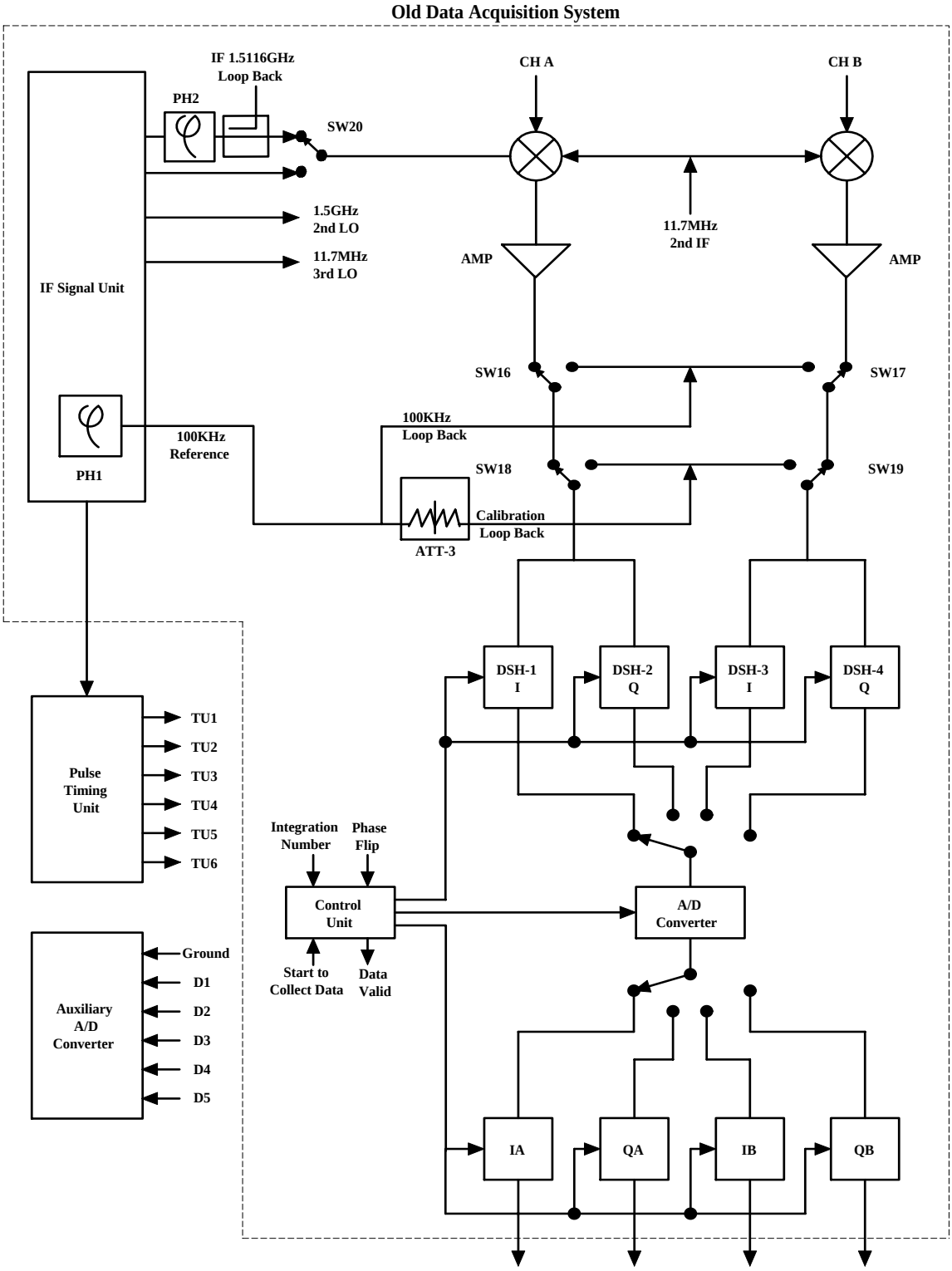


Figure 3.2: The old DAS System Diagram

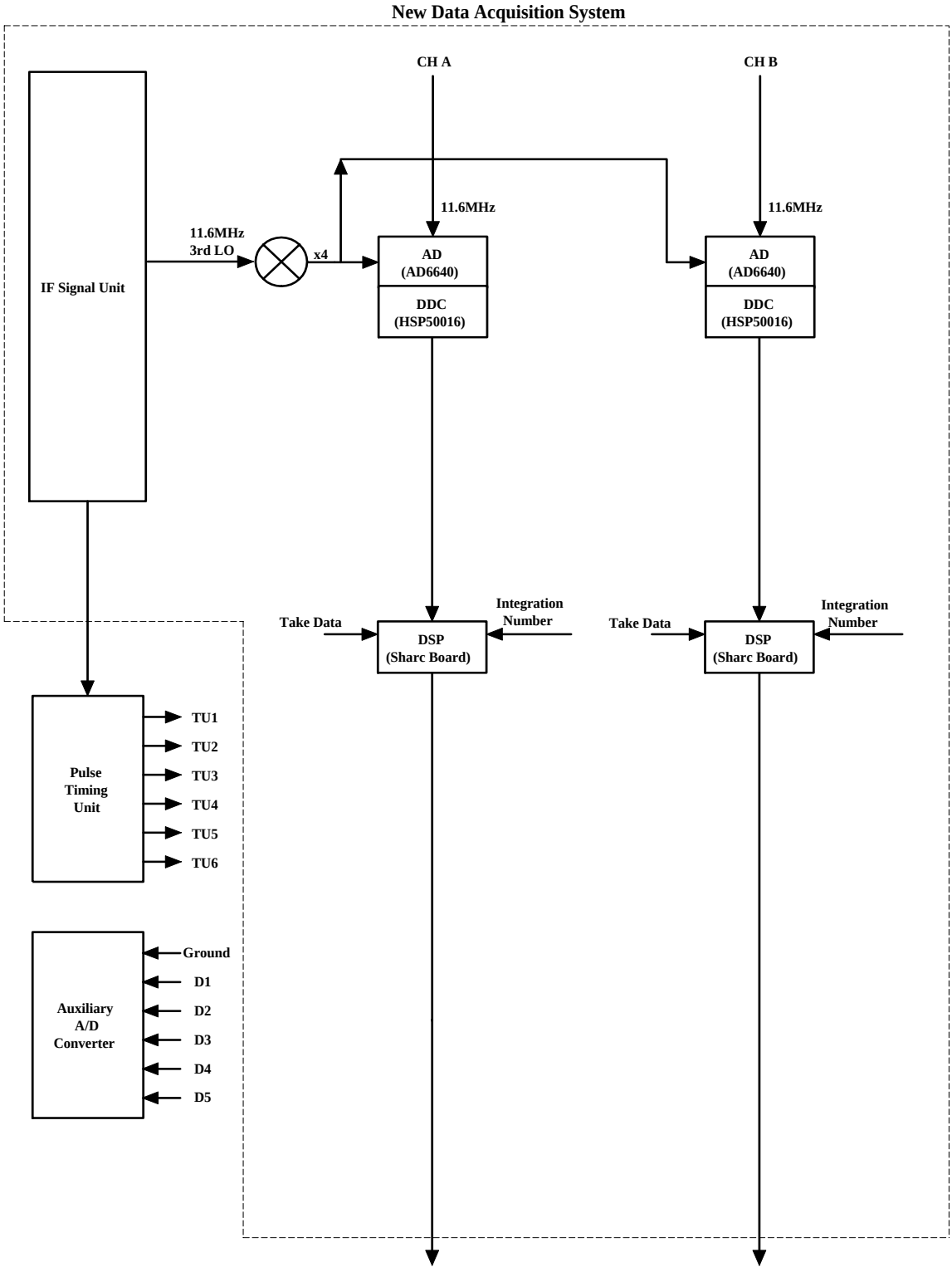


Figure 3.3: The new DAS System Diagram

to digitize frequencies from 0 to 23.2MHz(the first Nyquist zone) or 23.2MHz to 46.4MHz(the second Nyquist zone). Using bandpass sampling techniques, the ADC can capture the band from 46.4MHz to 69.6MHz(the third Nyquist zone) or 69.6MHz to 92.8MHz (the fourth Nyquist zone) using the first image produced during the sampling process. Theoretically, there is no limitation about the order of images that

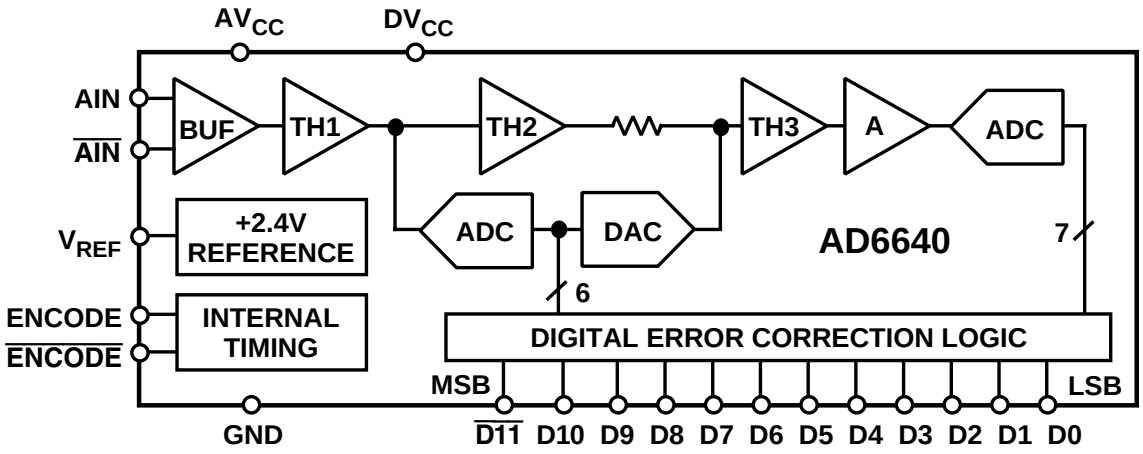


Figure 3.4: The Functional Block Diagram of AD6640

can be used to digitize the bandpass signal if an impulse train with infinitely short pulse width is used to take the samples. However, since it is impossible to do that, a Sinc distribution overlaid is introduced on the sampling impulse train in the frequency domain. Because of that, high order images will be mixed to the first Nyquist zone but will be attenuated by the Sinc distribution. The fourth order image was not found to be significantly attenuated by this kind of distortion.

3.4 Digital Downconverter (DDC)

3.4.1 Circuit Design

The schematics of the DDC are shown in Figures 3.5 and 3.6. While sending the control words to the DDC chip, its very important to make sure that the RESET and IQSTRT lines are stable through out the process. To minimize the interference from the other data lines, a interface circuit was designed in such a way that these control sequence have two paths to the DDC chip. One of the pathes uses the RESET and IQSTRT sequence; while the other path is for the rest of the control sequence. Two-level registers are used to arrange the data loading in the sequence.

Part of the circuit serves as a clock signal generator for the second-level registers while the other part is designed just to hold the data and make sure that there is enough time for the signals on the data lines to be stable before they are sent to the DDC.

The timing signals, PCWR0 and PCWR1 as shown in Figure 3.7, are used to provide the clock signals to the first-level register, U2 and the clock generator, U1 and U3. It should be noticed that those clock signals are sent in sequence. At the falling edge of PCWR1, data is sent from U2 to the second-level registers. Then in the following two clock periods, clock signals are generated by U3 so that data at the input end of U4 and U5 are sent to the DDC in turn.

3.4.2 Quadrature Digital Downconversion

The DDC chip used in the system is an Intersil HSP50016 and its functional block diagram is shown in Figure 3.8[4]. It provides quadrature digital downconversion for the digital output of the AD converter before it goes to the DSP board.

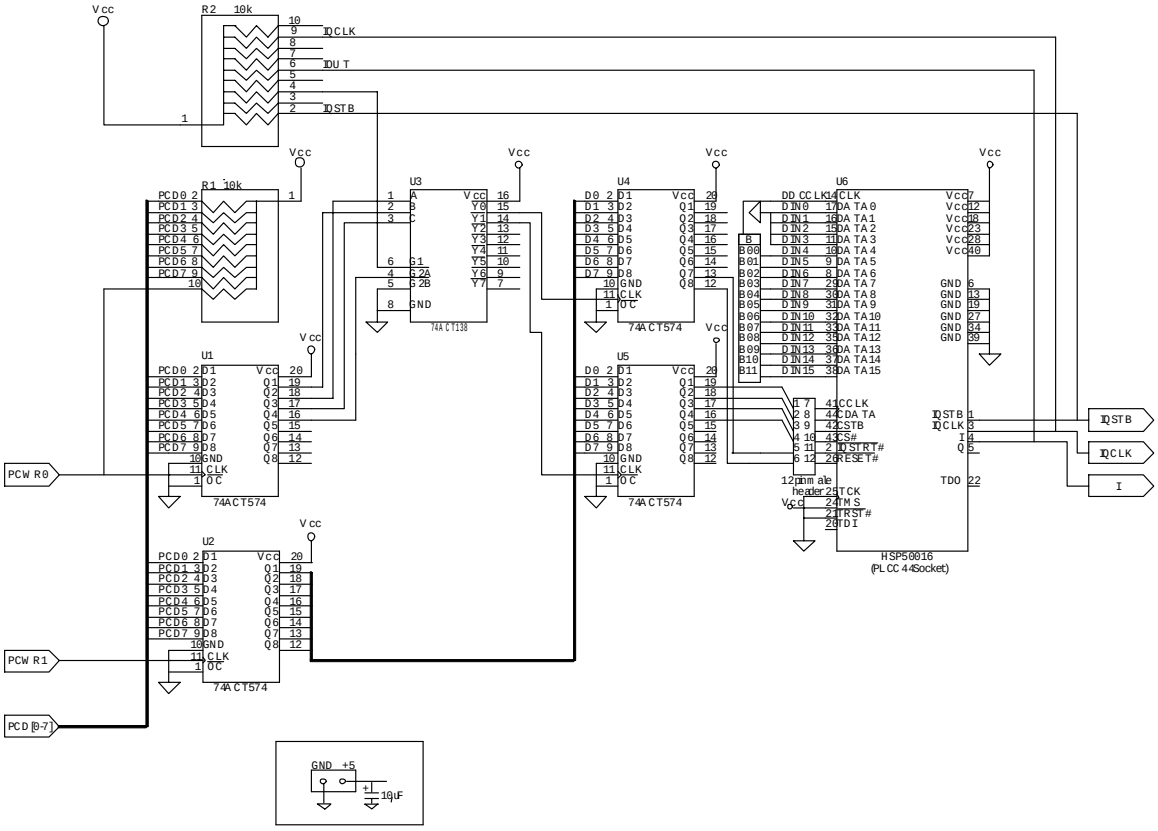


Figure 3.5: Schematic 1

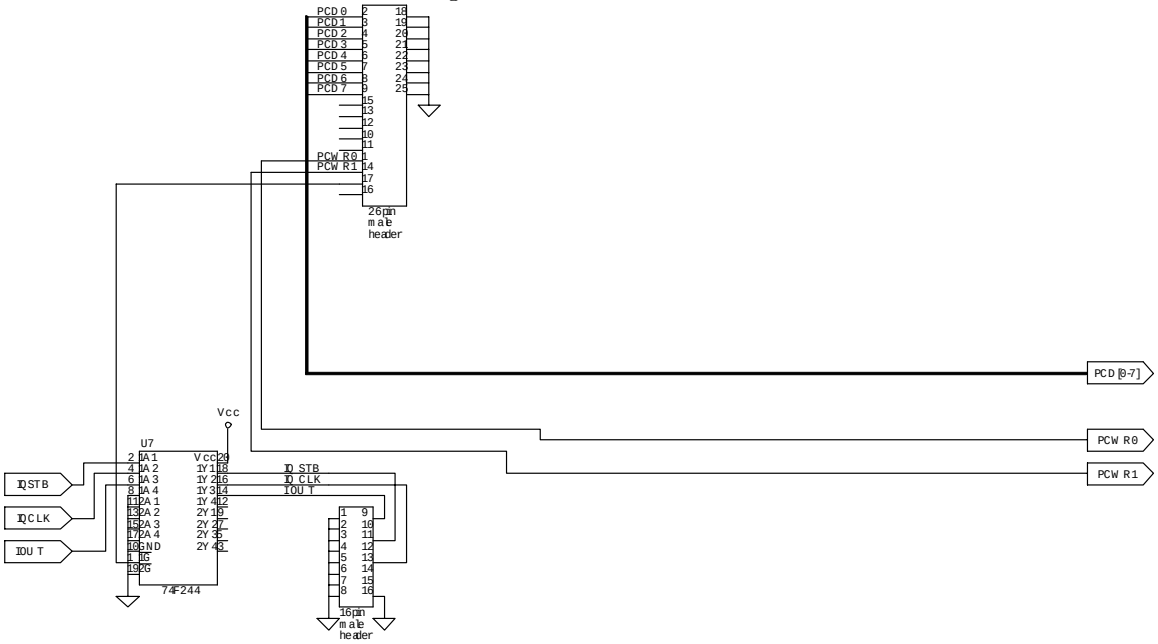


Figure 3.6: Schematic 2

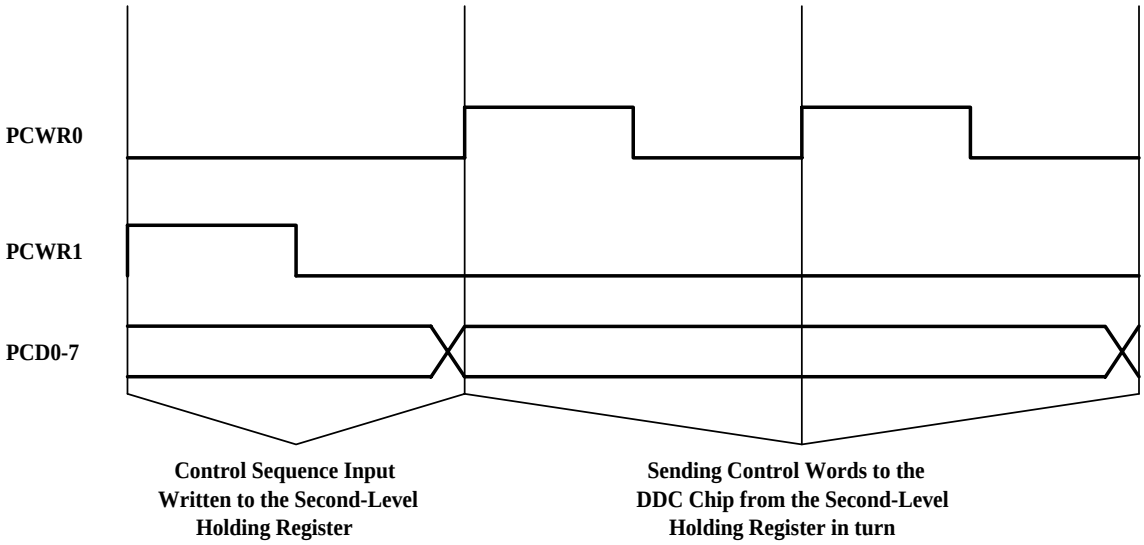


Figure 3.7: Timing Diagram for Loading the Control Words into the DDC Chip

The DDC is composed of a quardrature sine and cosine mixer, a complex sinusoidal generator, high decimation filters, fixed coefficient FIR filters and an output formatter. The mixers have two digital multipliers, one of them is for inphase and the other is for the quadrature channel. The LO signal for each channel is generated by the complex sinusoidal generator which uses a 33 bit register and its resolution in frequency can be calculated using the following formula : $DDCresolution(infrequency) = F_{clk}/2^N$

where N is the number of bits of the register. At the maximum clock rate, the frequency resolution is $52MHz/2^{33}$ which is equal to 0.006Hz. The outputs of I and Q multipliers are symmetrically rounded to 17 bits. This guarantees 102dB spurious free dynamic range (SFDR).

The high decimation filter(HDF)is composed of cascaded integration and comb filters. This structure is commonly used for high sample rate decimation filtering

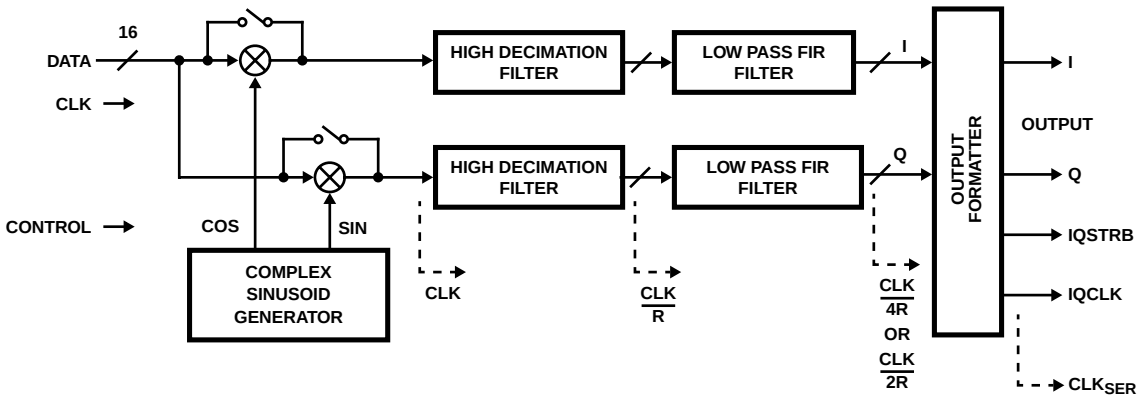


Figure 3.8: Digital Downconverter Functional Diagram

since the integration filter can perform accumulation but no multiplication. The frequency response of the decimation filter is given by:

$$H(f) = \left(\frac{\sin(\pi f)}{\sin(\pi f/R)}\right)^5 \left(\frac{1}{R}\right)^5 \tag{3.1}$$

where R is the decimation rate. The range of R is from 16 to 16384. Since the signal is further decimated by 4 through the FIR filter, the overall decimation rate range is from 64 to 65536.

The FIR filtering stage is used to perform aliasing attenuation, passband roll off compensation , transition band shaping and final stage decimation. It is functionally equivalent to two identical 121-tap low pass FIR filters. The filters are comprised of a single real multiplier, a sum of products accumulator and a table it can refer to for corresponding control parameters. The passband ripple(through HDF and FIR filter)is less than 0.04dB. As for the filter bandwidth, it can be calculated by the

following formulas:

$$BW_{DS(-3dB)} = 0.1375F_s/R, and \quad (3.2)$$

$$BW_{DS(-120dB)} = 0.2002F_s/R \quad (3.3)$$

where F_s=clock rate ;R=HDF decimation factor(16<R<16384). Since R is chosen to be 64 in this system, its corresponding -3dB and -120dB bandwidths are 99.6875KHz and 145.145KHz.

3.5 DSP board

The DSP board used in the system is a Sharc EZ-Kit Lite with ADSP21061 and its system block diagram is shown in Figure 3.9[5]. It provides the interface between the DDC and fast PIO board. The output of the DDC is fed to its serial port (SPORT), being accumulated and sent out through its external port. The maximum input data rate of the serial port is 40Mbits/sec. And the maximum data rate for the external port (both read and write) is 2.7MSPS(32bits/sample). The external port is programmed to have read and write functions through data and address port separately so that it can also be used to receive instructions as integration number and take data from the PIO board. The software aspects of this system are detailed in Chapter 4. And a brief description about the serial poart and the external port will be given in the following sections.

3.5.1 Serial Port (SPORT)

The Sharc board has two serial ports[6], SPORT0 and SPORT1, with a range of clock and frame synchronization options. It allows several communication protocols and can provide interface to many industry-standard data converters and CODECs.

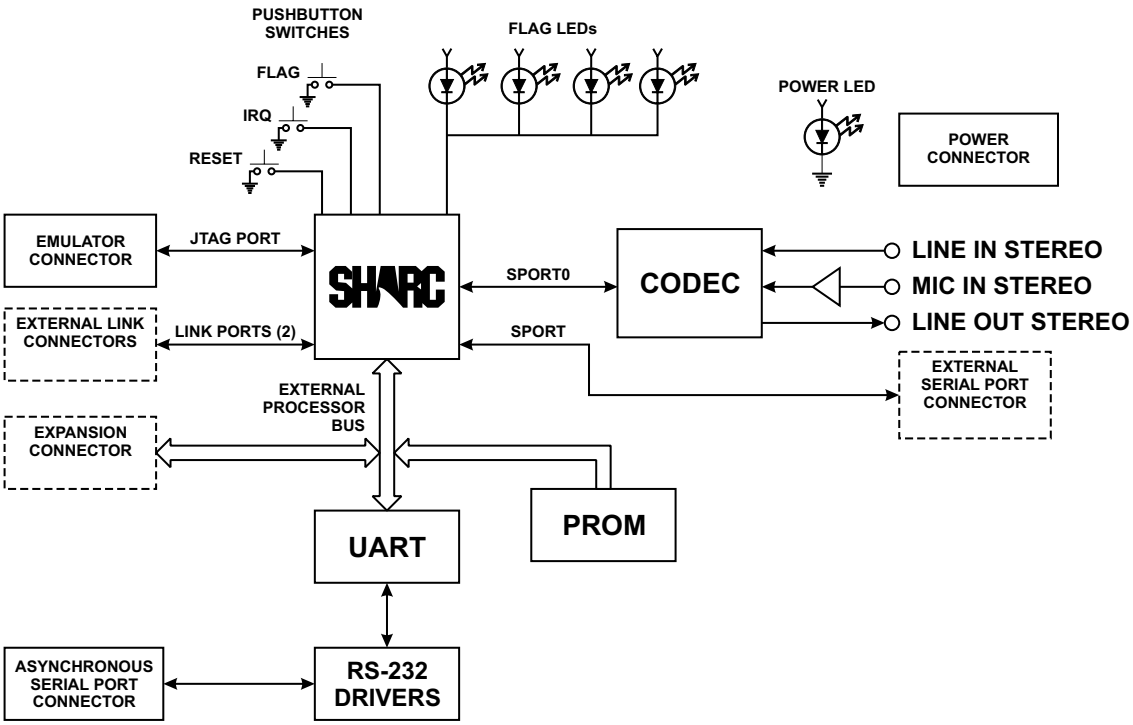


Figure 3.9: Sharc Board System Block Diagram

Each of them has its own set of shift registers, hardware companding units, data buffers and serial port control units as shown in Figure 3.10. And two channels are used in each port so that both transmitting and receiving tasks can be performed independently. SPORT1 is used in the system to receive data from the DDC. The RX buffers has two data registers and one input shift register. It's like a three-location FIFO and two 32-bit words can be stored when the third word is shifted in. Overflow occurs when the third word overwrite the second word if the first word has not been read out. When that happens, the receive overflow status bit (ROVF) will be set in the receive control register. The ROVF status can only be cleared when the SPORT is disabled.

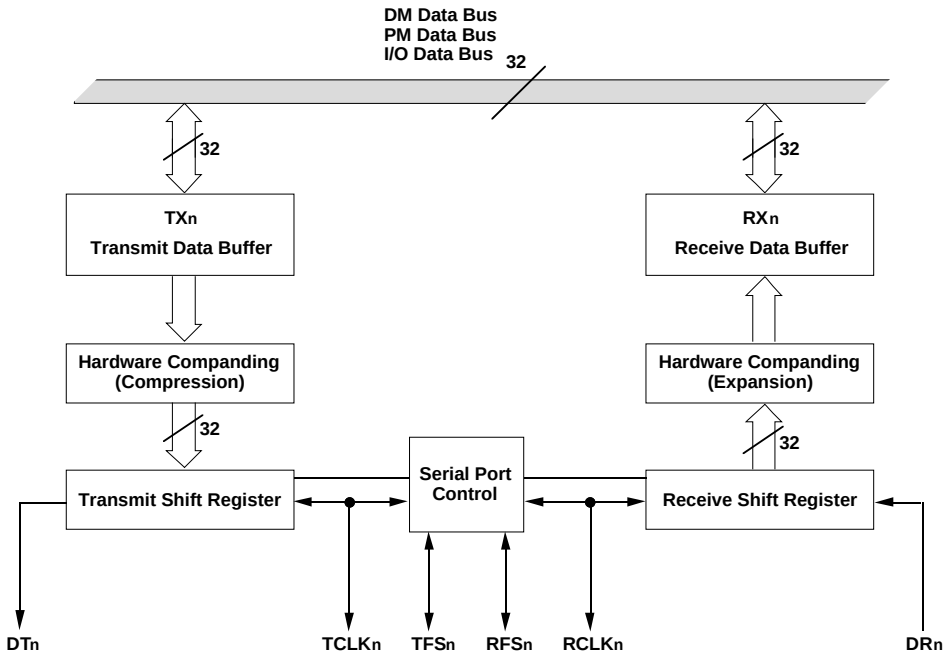


Figure 3.10: Serial Port Block Diagram

3.5.2 External Port

The external port on Sharc board is designed for external memory interfacing. It provides up to 4 gigawords addressing for off-chip memory. It allows direct connection with fast static RAM devices. Memory-mapped peripherals and slower memory devices are also supported with programmable wait states and hardware acknowledge signals. The external port provides a 48-bit data bus, a 32-bit address bus, read strobe line, write strobe line and bank select line to communicate with external devices. The data and address bus diagram is shown in Figure 3.11. In the system, it is used to send 24-bit accumulated output data to the fast PIO board.

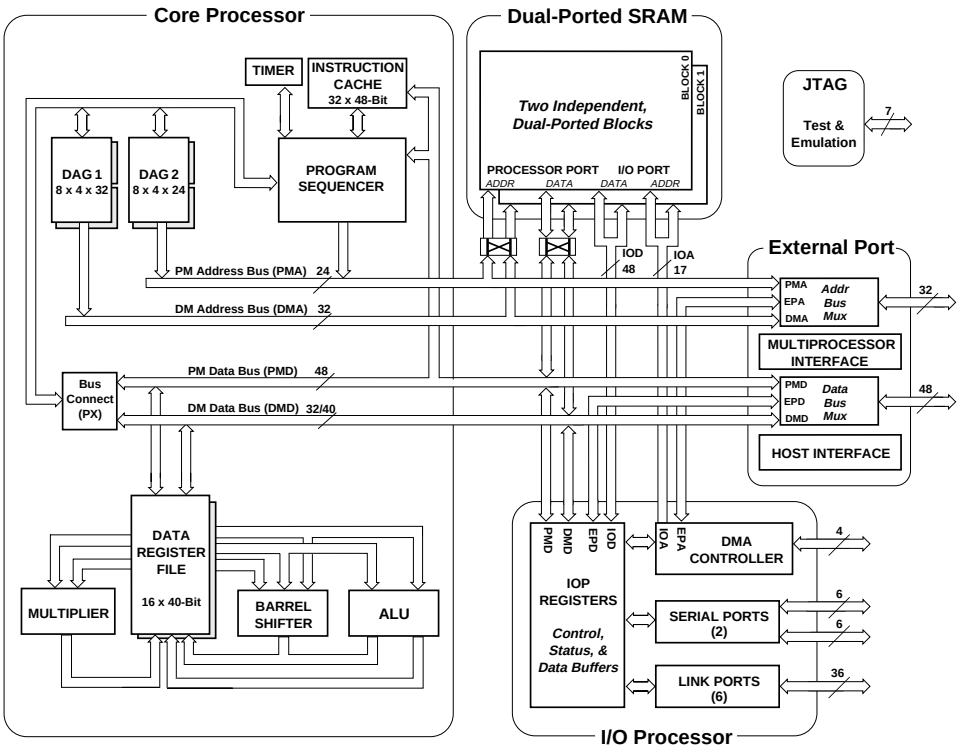


Figure 3.11: ADSP-21061 Data and Address Bus Block Diagram

3.6 Parallel I/O Board

3.6.1 PIO board

The PIO board, ComputerBoards PCI-DIO24, is composed of 82C55 parallel I/O chips[7]. It has three data registers and one control register which occupy 4 consecutive I/O locations that are used to provide 3 ports(A,B,C). Each port has 8 bits and can be programmed to perform direct I/O reads or writes. In the system, the PIO board is used to control serveral devices of the radar system and send the control word sequence to the DDC during the system initialization. All of the 3 ports(Port

A for data input, Port B for data output , Port C for address output)read and write according to the secondary address scheme, which is given in Section 2.5.5.

3.6.2 Fast PIO board

The fast PIO board used in the system is a National Instrument PCI-DIO-32HS and its functional block diagram is shown in Figure 3.12[8]. It has 32 digital I/O lines that can be divided into four 8-bit ports and is able to perform single-point I/O, pattern I/O and high-speed data transfer using several handshaking protocols. The speed of handshaking I/O is up to 76Mbytes/sec. And the maximum data rate varied with the handshaking mode and cable length used in the system as shown in Figure 3.13. Two DMA channels are provided to reduce the CPU loading during data transfer. In the system, the fast PIO board is used to receive the 24-bit data from the DSP board.

3.7 Logic Conversion and Secondary Address Boards

The logic conversion and secondary address boards are composed of several simple logic circuits and registers. The logic conversion board is used to convert the TTL signal (+5V 0V) to a +12V and -12V signal so that the logic levels (Low, High) can still be identified correctly after the voltage drops caused by the long line lengths. The secondary address board is used to gate out those data or instruction flows intended for other devices. Each secondary address board has its own unique address. And it is enabled only if it received the same address from the port C. Secondary address scheme is detailed in Section 2.5.5.

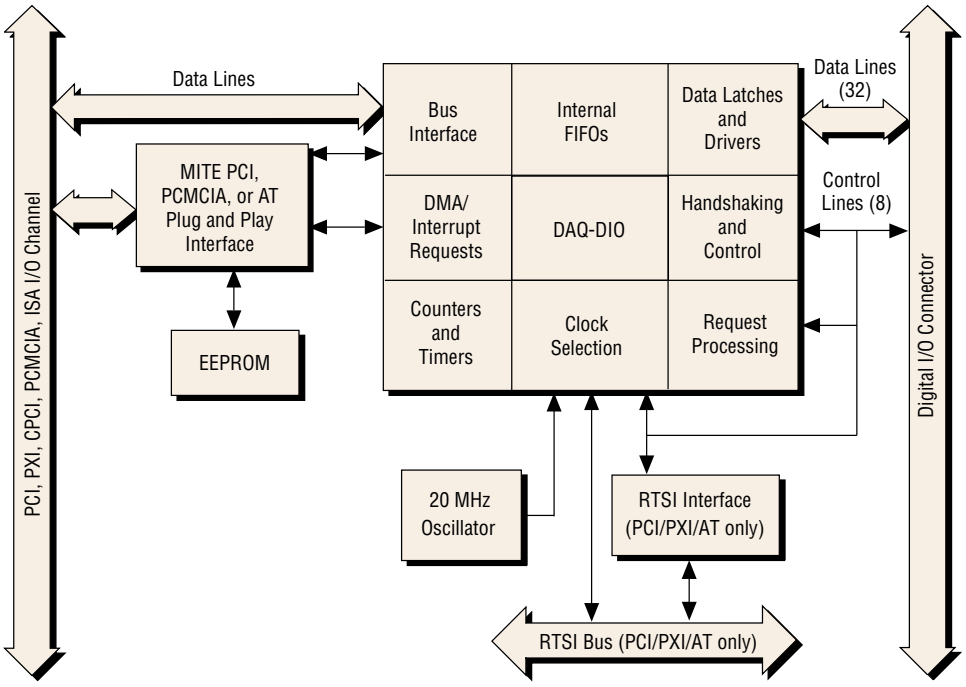


Figure 3.12: PCI-DIO-32HS Block Diagram

Protocol	Peak Rates (Mwords/s) by Cable Length 1 m	2 m	5 m	REQ and ACK Polarity	REQ Edge-mode	Programmable Delay	Complementary Protocols
8255 Emulation	6.67	4	4	Active-low	Trailing	Between transfers	Leading-Edge
Level ACK	3.33	2.5	2.5	Programmable	Leading	Before ACK and between transfers	Level-ACK
Leading-Edge Pulse	3.33	2.5	2.5	Programmable	Leading	Before ACK and between transfers	Leading-Edge Pulse
Long Pulse	3.33	2.5	2.5	Programmable	Leading	For pulsewidth and between transfers, DIO-96, 8255, 82C55	Long Pulse, 8255-Emulation, DIO-24, DIO-96, 8255, 82C55
Trailing-Edge Pulse	1.8	1.5	1.5	Programmable	Trailing	For pulsewidth and between transfers	Trailing-Edge Pulse
Burst	20	10	10	Programmable	Neither; uses level REQ	For clock speed	Burst

Figure 3.13: PCI-DIO-32HS Handshaking Protocols

3.8 Summary

The new DAS system is composed of an 12-bit A/D converter whose typical SNR is 68dB, a 16-bit DDC with spurious dynamic range as 102dB, a 40MHz Sharc DSP board with maximum output rate as 2.75 Mbytes/sec, a high-speed PIO card with maximum input rate as 3.1Mbytes/sec , logic conversion board and secondary address board.

The main difference between the old receiver and the new one is that the down-conver and IQ separation is done digitally so that it is free from linearity and image problems and has perfect IQ balance. Also, it offers a much faster processing speed and a better handshaking scheme.

CHAPTER 4

SOFTWARE IMPLEMENTATION

This chapter describes in detail the software control of the Digital Down-Converter (DDC) and the design of the DSP program. It includes how the control words of the DDC in the system are derived, a flow diagram of the control word generator, how the control sequence are sent through the PIO board and a brief description about how the Sharc DSP board works as an interface between the DDC and the fast PIO board in terms of the DSP software design. A signal flow diagram is also shown to provide a clear illustation of the data format and flags used during the data transfer and its related port configuration.

4.1 Control Sequence Generation

4.1.1 Derivation of the Control Words

In this section, the steps taken to derive the control words of the DDC are briefly described. It should be noticed that the DDC was not used to access the chirp mode and the multi-channel mode in the system. Thus, the related control words 2 and 3 are set to 0 to disable these features. Likewise, the test enable bit in control word 1 is always set to 0 to disable the test features.

In the system, the downconveting frequency is designed to be 11.6Mhz . Since the clock frequency for the DDC is 46.4MHz and the bandwidth of the analog signal is 100kHz, optimum decimation rate can be calculated as follows:

$$BW_{DS(-3dB)} = 0.1375F_s/R. \tag{4.1}$$

Once the decimation rate is decided several important parameters such as minimum phase increment, scaling multiplier gain, and IQ clock rate can be calculated accordingly.

In CW mode minimum phase increment is subtracted from the output of the phase register on every CLK and the difference become the new phase register value as shown in Figure 4.1. It is given by

$$phase\ increment = INT(f_c/f_s)2^{33}Hex. \tag{4.2}$$

By substituting the value of f_c and f_s into this equation, one obtains that

$$phase\ increment = INT\left(\frac{11.6 \times 10^6}{46.4 \times 10^6}\right) \times 2^{33} = 80000000(Hex) \tag{4.3}$$

As shown in Figure 3.8, the output of the mixers goes to the HDF. And since the gain of each HDF is dependent on the decimation rate, there is a need to compensate for it. The scale factor used to do the compensation is given by

$$Scale\ factor = 32768 \times 2^{CEILING(5log_2(R))}/R^5. \tag{4.4}$$

By substituting the value of R into this equation, one finds that

$$Scale\ factor = 32768 \times 2^{CEILING(5log_2(64))}/64^5 = 8000(Hex). \tag{4.5}$$

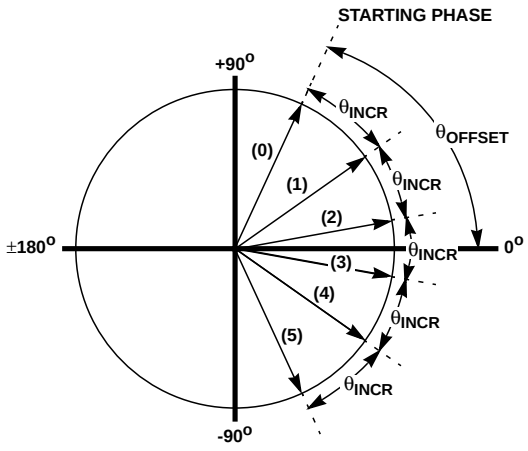


Figure 4.1: Phase Word Parameters for the CW Case

It should be noticed that the HDF and FIR filter serve as one optimized composite filter. A diagram of the frequency response of the composite filter for R=16 is shown in Figure 4.2 to better illustrate the concept.

Finally, the IQCLK rate is given by

$$IQCLK\ frequency = Floor\left[\frac{R \times 4}{Length_{min}}\right] \tag{4.6}$$

where

$$\begin{aligned} Length_{min} &= [(NumberofOutputBits + 2) \times Mode] + 1 \\ or Length_{min} &= [(16 + 2) \times 2] + 1 = 37 \end{aligned} \tag{4.7}$$

where Mode=2 since the DDC is in I followed by Q Mode.

By substituting the value of R and $Length_{min}$ into these equations, one obtains that

$$IQCLK\ frequency = Floor\left[\frac{64 \times 4}{37}\right] = 0101(binary). \tag{4.8}$$

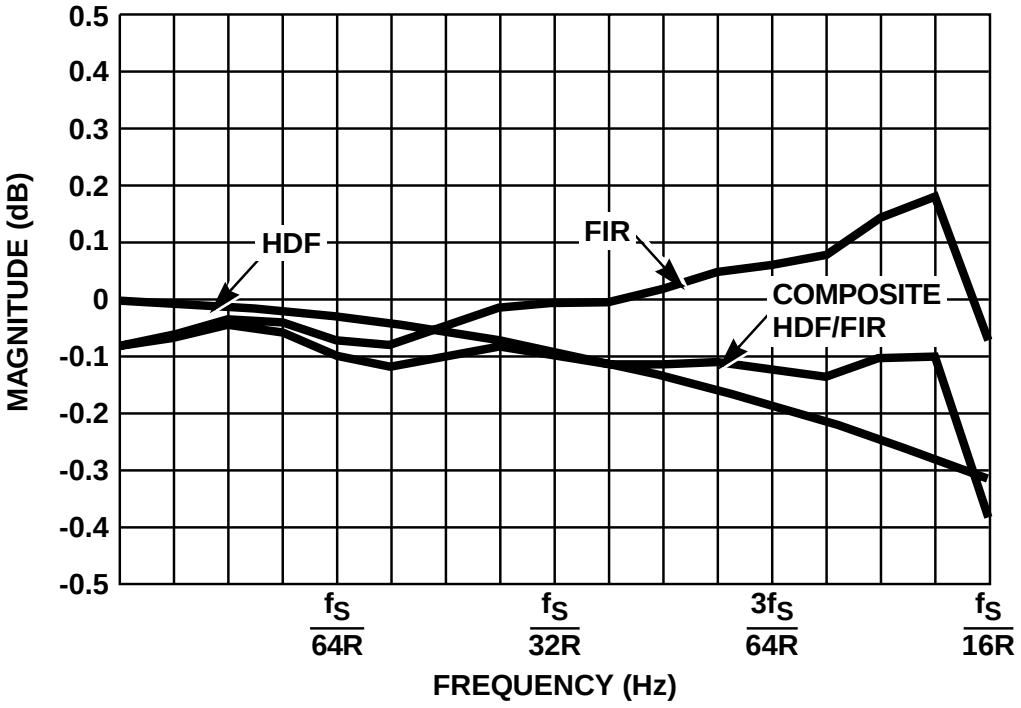


Figure 4.2: Frequency Response of the Composite Filter for R=16

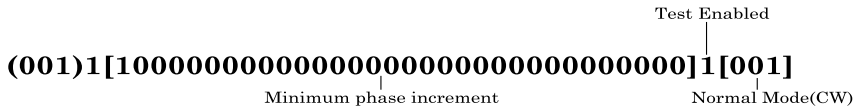
As for the rest of the parameters and their corresponding functionality, they are illustrated in Figure 4.3. And the detail information about the setting of the control words is shown in Table C.1-C.6 (Appendix).

4.1.2 Control Word Generator

As explained in Section 3.4.1, two-level registors are used to insure that the control lines connected to the DDC chip are always stable. Because of the fact that the logic circuit and registors share the same data lines in a time-division manner, there is a need to blend the control words into those control sequence for the logic circuit in a

WORD1

3800000009



WORD2

5000000000

(010)10000000000000000000000000000000000000

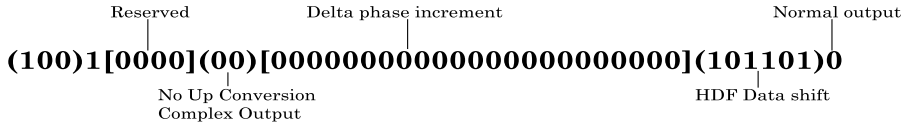
WORD3

7000000000

(011)10000000000000000000000000000000000000

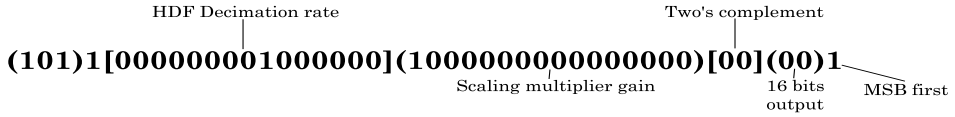
WORD4

900000005a



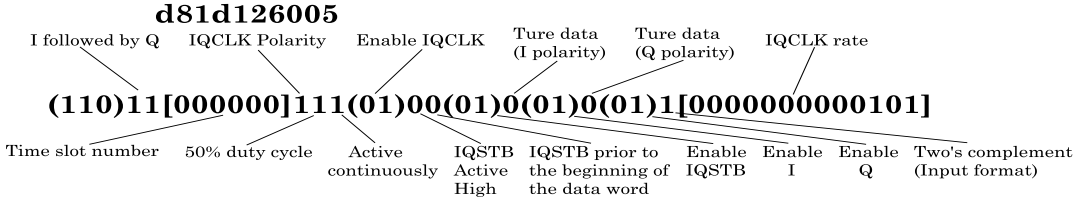
WORD5

b008100001



WORD6

d81d126005



WORD7

f000000002

(111)10000000000000000000000000000000000010

Figure 4.3: Control word sequence

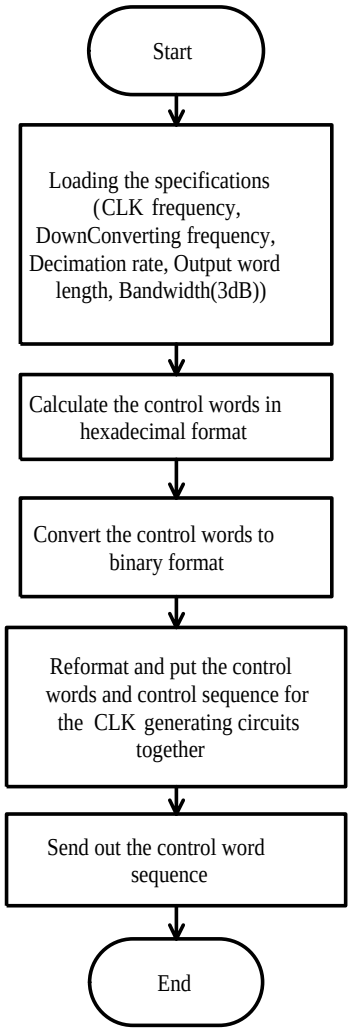


Figure 4.4: Flow Diagram of the Control Word Generator

proper way. Also, there is a need to generate associated CLK signals and status line signals for the registors according to the timing specifications.

To address this tasks, a program was implemented to calculated the control words, and to generate all control signals needed for the logic circuits and registors. A flow diagram of this program is shown in Figure 4.4.

4.2 DSP Programming

An assembly routine is programmed for the DSP board to perform accumulation and reformating tasks. In this section, the port configuration, the instruction set, the data flow of the I and Q words, and the data processing are briefly discussed. A flow diagram of the program is shown in Figure 4.6.

4.2.1 The Port Configuration

For the Sharc DSP board, the serial port 1 (SPORT1) is used to receive the 16-bits I and Q words from the DDC output. An interrupt driven scheme for SPORT1 is used so that the processor core can handle other tasks while new data is being received.

The external port on the Sharc DSP board has 32bits(bit16-bit47) available for data and 32bits available for addresses as shown in figure 4.5. In the system, 24bits(bit1-bit24) of the address port are used to send out the 24-bits accumulated I and Q words to the fast PIO board while three bits of the address port serve as indicators and clock generator. Note that 4bits of the data port are used to receive the instructions such as integration number and take data from the PIO board.

The bit25 of the address port is used to generate the clock signal for the I and Q words because its more stable than the read strobe signal from the external port. In fact, it's a tradeoff between maximum data rate and stability of the clock signal. The maximum data rate is 1.35MSPS instead of 2.7MSPS if the clock signal used is generated by the address port.

Bit26 of the address port serves as the indicator of I and Q words. Since the data port is synchronised with the address port, any bit of the address port can be used

to put 'mark' on the I and Q words. When bit1 is high the data port has sent out an I word and when it is low it has sent out the Q word.

Bit27 of the address port serves as the timing indicator for I and Q words. And bit28 of the address port serves as the data valid indicator for I and Q words.

The main problem associated with the serial I and Q word transfer is that it is very difficult to know which word is actually the I or Q data.

In this design, serial I and Q words from the DDC chip into the DSP board the first word being the I word. But the first word out of the DDC output is not alway I. If the DSP board takes Q words as I words then the spectrum flips. And if the I words are paired up with the Q words having different timing index then there will be a phase shift in the frequency domain.

Similar problems occur when the accumulated I and Q words are sent to the fast PIO board. The use of bit26-27 of the address port provide correct information for the PC to know whether the word received is I or Q and how to pair I and Q with the same timing index if the first word received by DSP is an I word.

In the system, the bit27 is set to 1 for the first pair of I and Q words and then set to 0 for the second pair of I and Q and so on. As for how to handle the situation when the DSP board makes a wrong judgement on the I and Q input, a program for testing is implemented in the host program on the PC. The program actually compares the I and Q words with the values stored in the computer to identify which word is I or Q during the system initialization process so that the measurement can be made without this problem.

For the fast PIO card, its port is configured as one 32-bit port for reading(24bits for the data, 4bits for the indicators and the other 4bits are reserved). Since the

output data of the DSP board is transfered to the fast PIO card in a asynchronized manner, the port is configured to received data in Level ACK mode.

4.2.2 Instruction Set

In the system, bits45, 41, 40 and 38 of the data port on the DSP board are connected to C6, C5, C4 and C3 of the PIO board, respectively through the Logic Conversion and the Secondary Address board. And two types of instructions, integration number and take data are sent to the DSP board. For the take data command, it is sent to get one frequency or angular point during the frequency or the angular scan by sending 8 (take data) and then 1(delay) through port C on the PIO board. For the integration number, two values in sequence are sent to the DSP board. The first value is sent to pick the group of the integration number(low, mid and high), and the second number sets the real value of the integration number, as shown in Table 4.1.

First Value	Second Value	Corresponding Integration Number
16	8	1
16	32	2
16	64	4
32	8	8
32	16	16
32	64	32
48	8	64

Table 4.1: Values needed to send to change the integration number

4.2.3 Data Manipulation

The main task for the DSP board is to do the accumulation. The 16-bit I and Q words are recognized as fix-point positive numbers and stored in the on-board memory in two's complement format. If a small positive value in two's complement is added by a small negative number in two's complement, sometimes it ends up with a big positive or negative value which is incorrect. What's implemented in the DSP program is that it first converts the number into sign-extented values so that the DSP board can differentiate positive numbers from negative ones. The DSP then does addition and converts the answer into two's complement format with proper length according to the integration number.

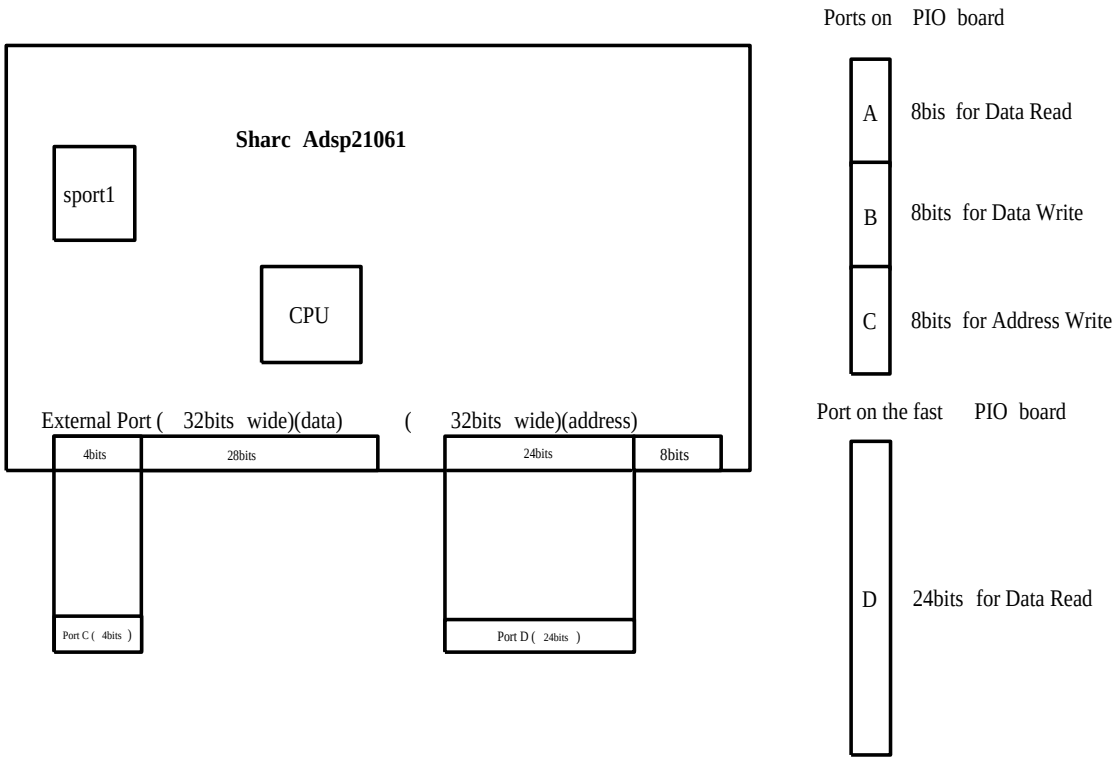


Figure 4.5: The DSP Port Diagram

4.3 Summary

A control word generator was implemented to convert the desired specs into the data streams which can be directly sent to the control word feeding circuit.

The serial ouput of the DDC goes to the SPORT1 on the DSP board and the accumulation result is sent through the external address port to the PC while the external data port is used to receive instructions from the PC. The DSP board can process instructions such as take data and integration number.

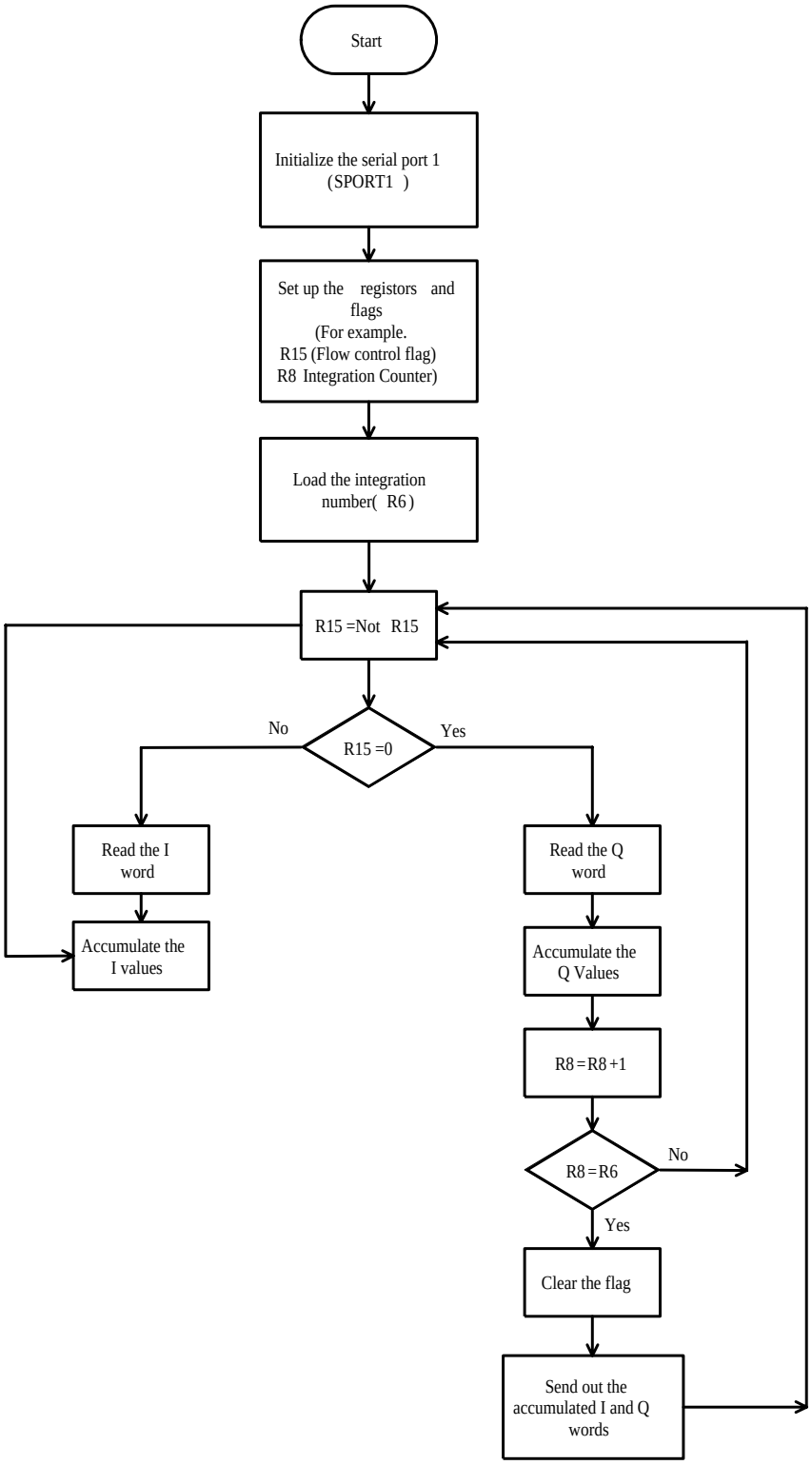


Figure 4.6: Flow Diagram of the DSP Assembly Routine

CHAPTER 5

DIGITAL RECEIVER EVALUATION

This chapter presents a complete set of performance results for the digital receiver. The testing was performed to verify first that the components met the manufacturer specifications and secondly that the circuit of the digital receiver system can seamlessly work with ESL's existing instrumentation radar system.

The evaluation procedure consisted of testing the control word feeding circuit , measuring the noise power out of the chain with a 50 ohm termination on the input for AD board, testing the linearity and noise performance of the AD board, measuring the noise power and the dynamic range of the digital receiver, testing the accumulation function of the DSP board and its effect to reducing the noise level and testing its acquisition speed.

5.1 DDC Board Testing

Since the HSP50016 is a highly programmable DDC chip and offers various functions, it's necessary to check the DDC control words input and output to see if the control sequence generator and its associated control word feeding circuits work as designed and if the DDC can follow the instructions correctly. A simple system setup

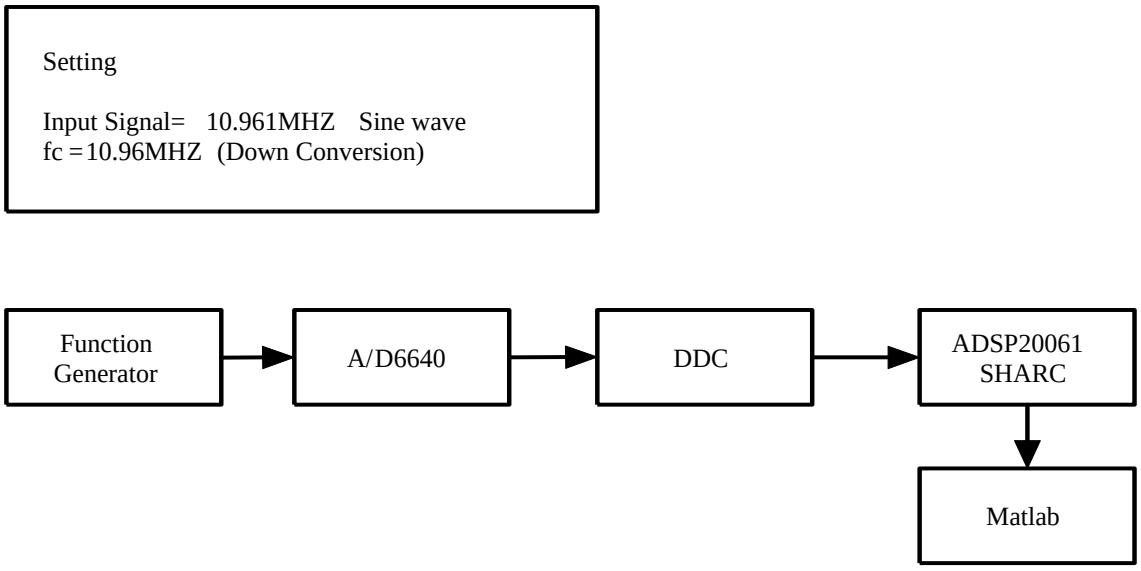


Figure 5.1: The setting of the testing system

Control Word	*Nibble9*	*Nibbles0-8*
0	1	000000000
1	3	385c000009
2	5	000000000
3	7	000000000
4	9	00000004c
5	b	012bdeb81
6	d	81d12600f
7	f	000000000

Table 5.1: Control Words for the testing

was developed to do the testing as shown in Figure 5.1. The control words used during the testing are shown in Table 5.1.

The first step of the testing is to make sure that the control words received by the DDC chip are the same as those specified in the control word generator. Since there are only 6 lines connected from the control word feeding circuit to the DDC chip (CCLK: Control Clock, CDATA:Control Data, CSTB: Control Strobe, CS:Chip select, IQSTRT and RESET) and the control sequence is not very long, the best way to do the test is to use HP Logic Analyzer to monitor these 6 lines and make comparison of the desired control words and the received control words. It was found that the control word feeding circuit was not very noisy and functioned properly during the testing. The control sequence captured by the Logic Analyzer during initialization and transmission are shown in Figures 5.2 and 5.3.

The next step was to make sure that the DDC functions according to the control words. As shown in Figure 4.3, there are 27 parameters that can be specified to make DDC work in several different ways. Most of them can be verified by doing time-domain and frequency-domain analysis of the DDC output, while the others can be verified simply by taking a look at the waveform of the DDC output. For example, the decimation rate specified in the testing system is 149 in control word 5. And its corresponding IQCLK frequency is 2.47MHz. Since the IQCLK frequency shown on the Logic Analyzer is also 2.47MHz, one then knows that the DDC received the decimation rate correctly. It should be noticed that the parameters other than the 27 stated earlier are set to be 0 because the testing features on the chip are disabled. The waveform of the DDC output (CLK, STROBE and DATA) is shown in Figure 5.4.

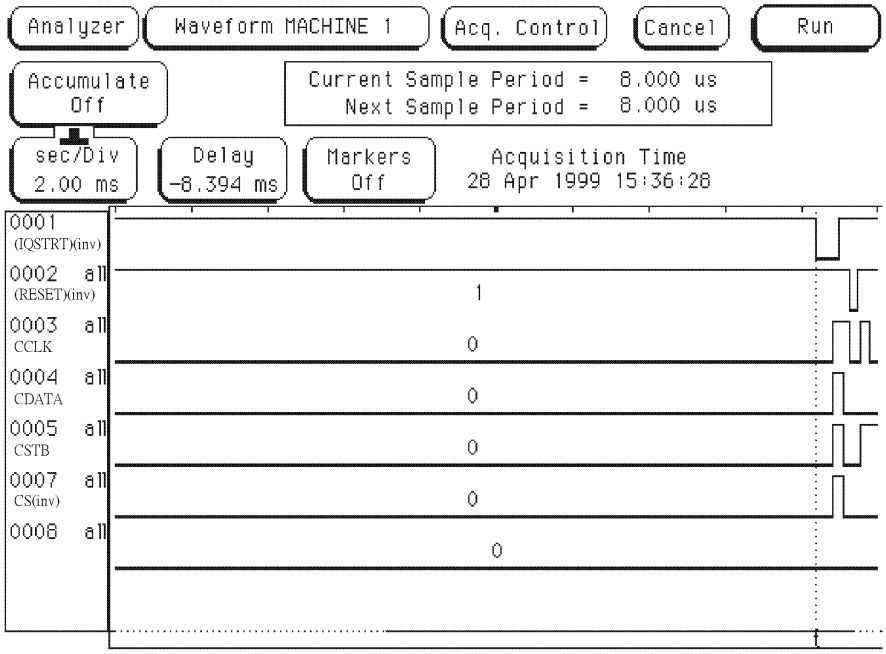


Figure 5.2: Initial State of the Control Sequence

5.2 AD Board Testing

The AD board is the most important part of the system. It mainly sets the dynamic range, linearity, noise performance and the minimum signal level of the digital receiver. In the testing system, a 1-Volt peak-to-peak sinusoidal wave with a 1000Hz offset compared to the down-converting frequency is used for the analog input and a 40.96MHz clock signal is used as the clock for the AD board. The reason for using a 1-V sinusoidal signal is to access the full dynamic range of the AD to measure the signal-to-noise ratio and to check the linearity of the AD. Using a signal with a small frequency offset makes it easy to check the I, Q phase difference in the time-domain and gives one an intuitive idea of the linearity of the AD. In addition if

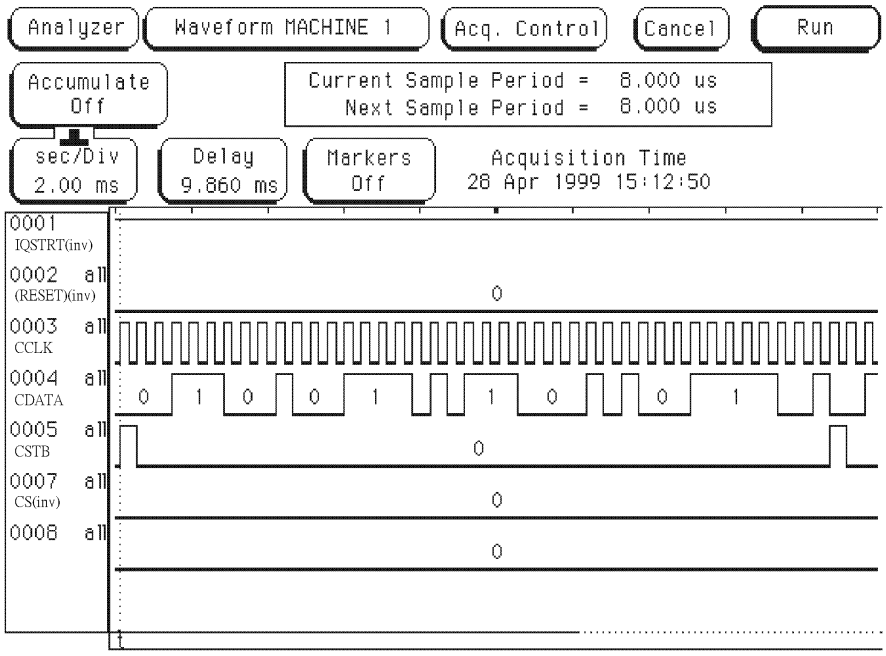


Figure 5.3: Control Words during Transmission

the result of the time-domain and frequency-domain analysis is consistent with the expected results, it helps one to verify the functionality of the whole digital receiver.

Figures 5.5 and 5.6 show the time-domain waveform of the I and Q channel after conversion and its corresponding spectrum, respectively. It can be seen from Figure 5.5 that the I and Q sinusoidal waveforms have the same amplitude and a 90 degree phase difference to each other which implies a single tone in the time-domain. In addition, no glitch and IQ flipping problem was found. As can be seen from Figure 5.6 that the difference between the peak level of the signal and the level of the noise floor is about 110 dB. Since the plot shows the spectrum from the result of a 4096 point FFT which reduces the noise power by 36 dB and assuming that the processing gain due to oversampling and filtering is 5 dB, the actual dynamic range is about 68 dB

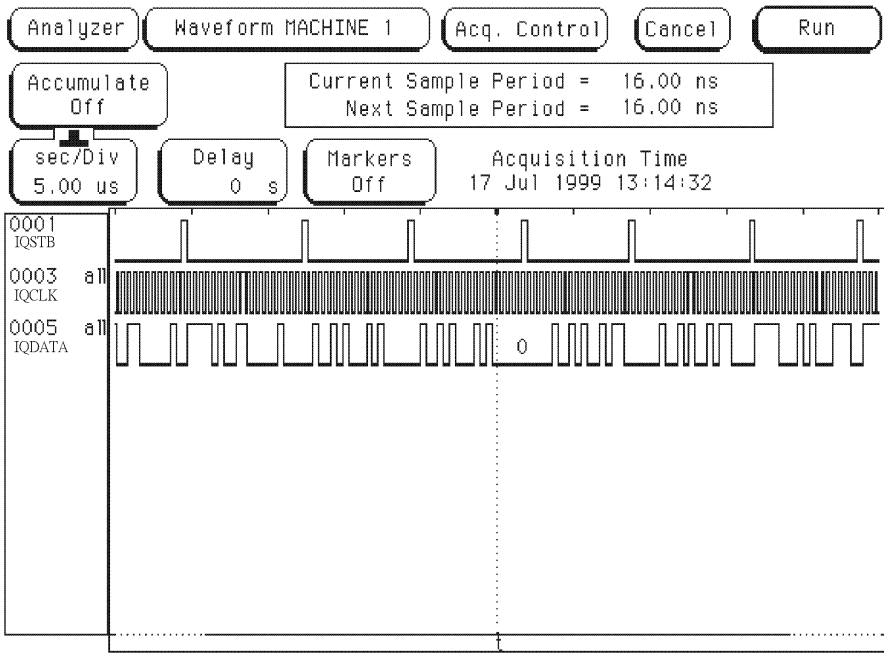


Figure 5.4: Output of the DDC

which is about the same as the typical signal-to-noise ratio indicated on the datasheet of the Analog Device AD6640 board. It should be noticed that the bandwidth is programmed to be about 37 KHz. It's also shown in the Figure 5.6 that there is about a 1 kHz frequency offset for the tone compared to the origin which is correct since the sinusoidal wave feed into the AD board has a 1KHz frequency offset compare to the programmed down-converting frequency. At this point, these results show that each board of the digital receiver is in working properly and provides the expected results.

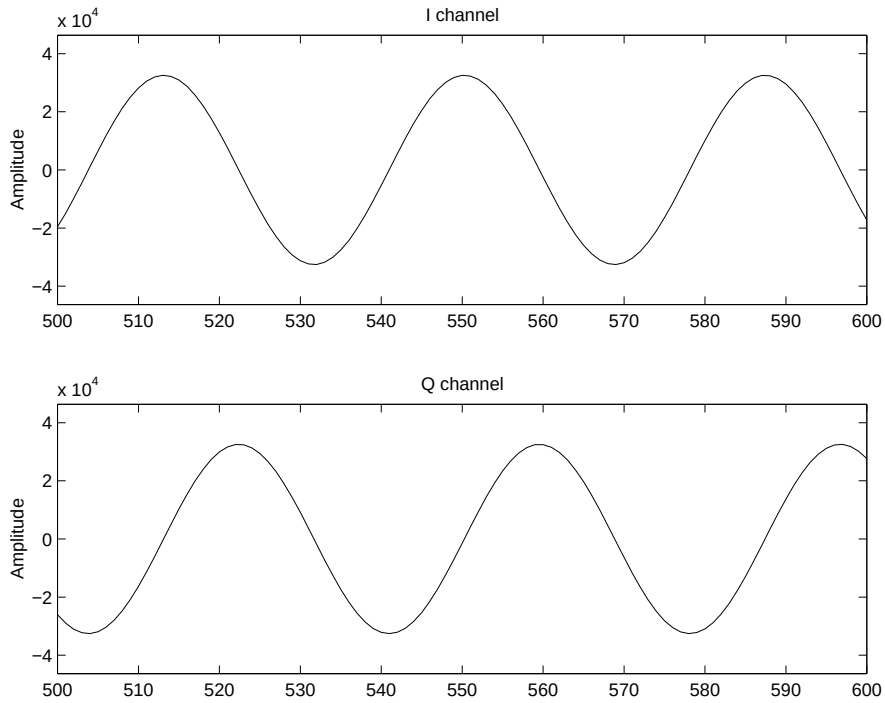


Figure 5.5: Waveform of the I and Q Channel after Downconversion

5.3 Digital Receiver Radar Testing

The final stage of the testing is to interface the digital receiver with the existing instrumentation radar system and evaluate its performance. The system setup is shown in Figure 3.1. For testing, the radar is set to 1.5GHz RF Loop Mode during the test.

5.3.1 Noise Level

The first step of the testing is to measure the noise level of the digital receiver. To do this test, a 50 Ohm matched load is connected to the front end of the receiver and the receiver is commanded to collect two sets of data. The DC level is removed by

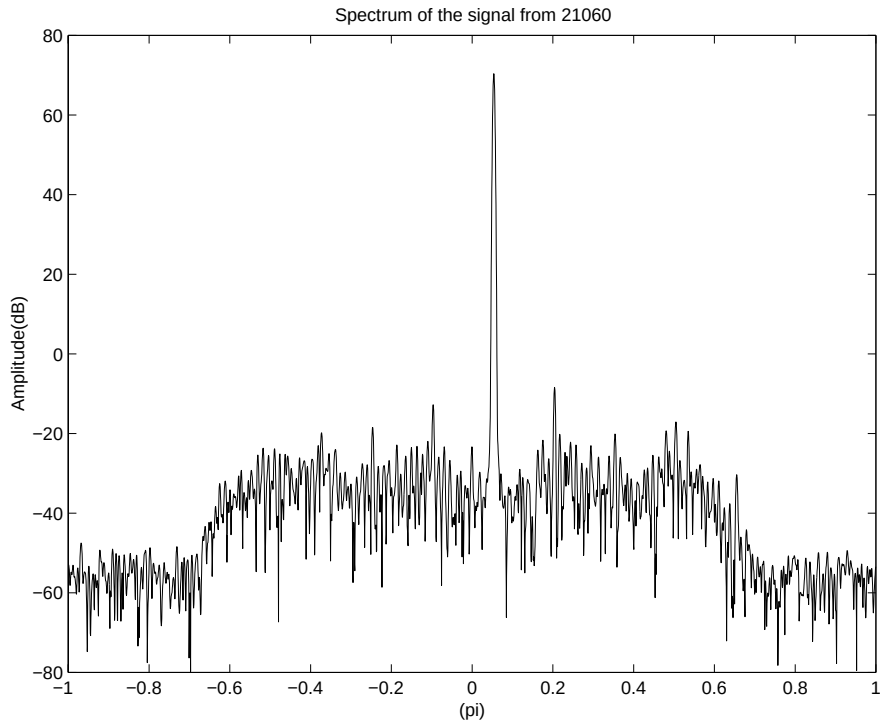


Figure 5.6: Specturm of the signal after Downconversion

subtracting the first measured values from the second one; in which case, the noise power is divided every time the integration number is doubled. Using this approach, the measured noise level is shown with different integration numbers (N=1) and (N=8) in Figures 5.7 and 5.8, respectively. Note that the noise level is about 5 dB for N=1 and less than 0 dB for N=8.

5.3.2 Dynamic Range

The next step is to measure the dynamic range of the digital receiver. A test signal is generated by amplifying a reference signal to saturate the receiver. Every time the measurement is made, more pads are connected to provide attenuation between the

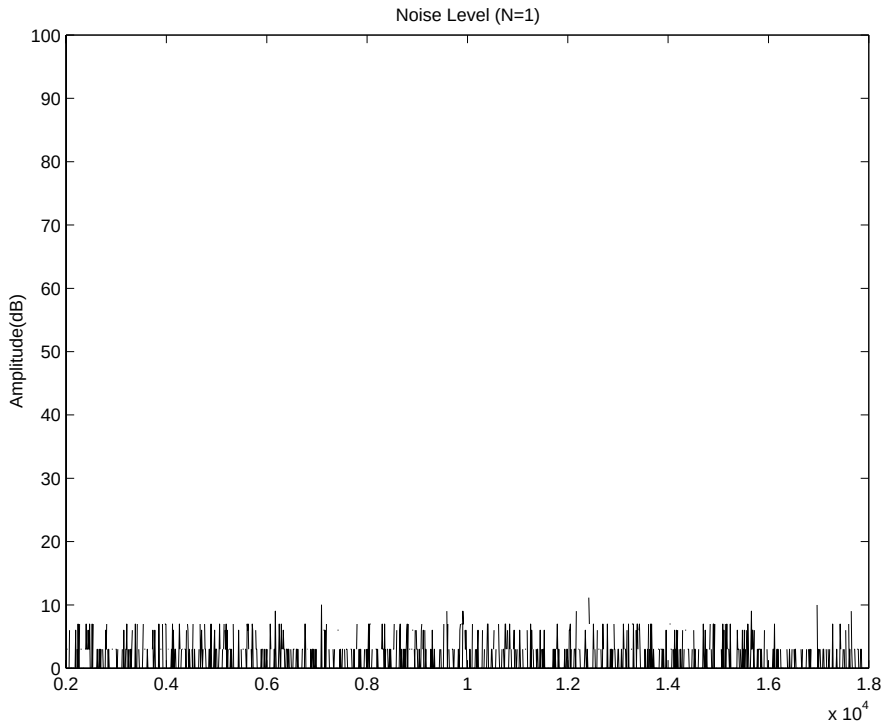


Figure 5.7: Noise Level of the Digital Receiver (N=1)

test signal source and AD analog input. As can be seen from Figure 5.9, the dynamic range of the receiver is about 80 dB.

5.3.3 Speed

To measure the speed of the digital receiver. The the HP Logic Analyzer is set up to probe the take data pin and associated data output pins on the DSP board. Roughly speaking, this is the time it takes to generate a pair of I and Q. This speed for different integration number can be calculated as follows:

$Time\ spend\ to\ get\ a\ pair\ of\ I\ and\ Q = 40\mu s + 6\mu s * integration\ number$

The first term, $40\mu s$, indicates the pulse width of the take data command. And the 6

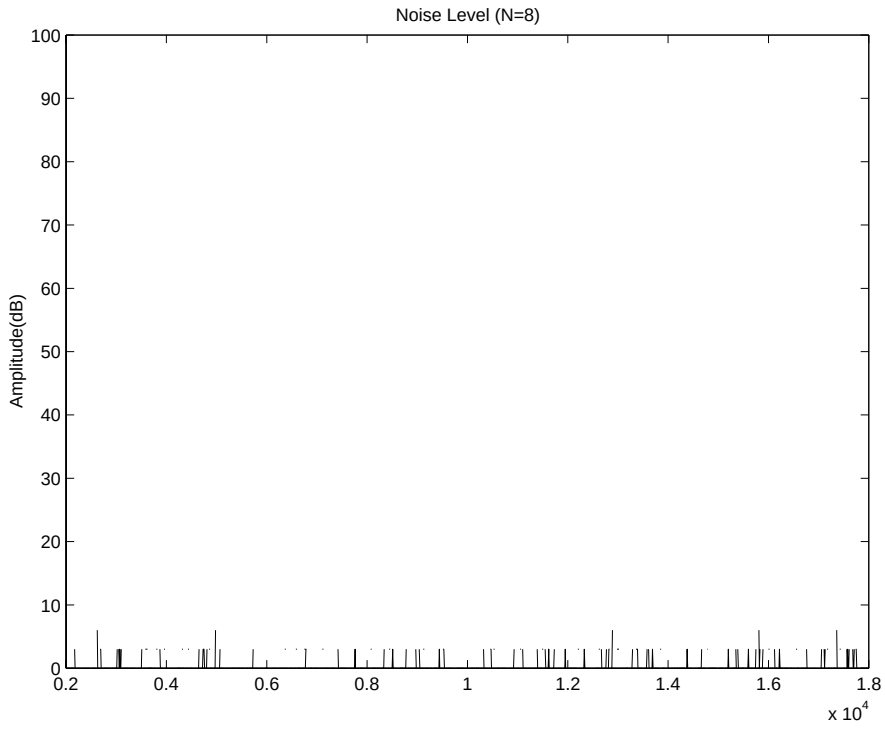


Figure 5.8: Noise Level of the Digital Receiver (N=8)

μs indicates the time needed to get one sample when the integration number is equal to 1.

Table 5.2:Speed Test of the Digital Receiver

Integration Number	Time needed to get a pair of I and Q (in microseconds)
1	46
2	52
4	66
8	88
16	136
32	232
64	424
128	808
256	1576

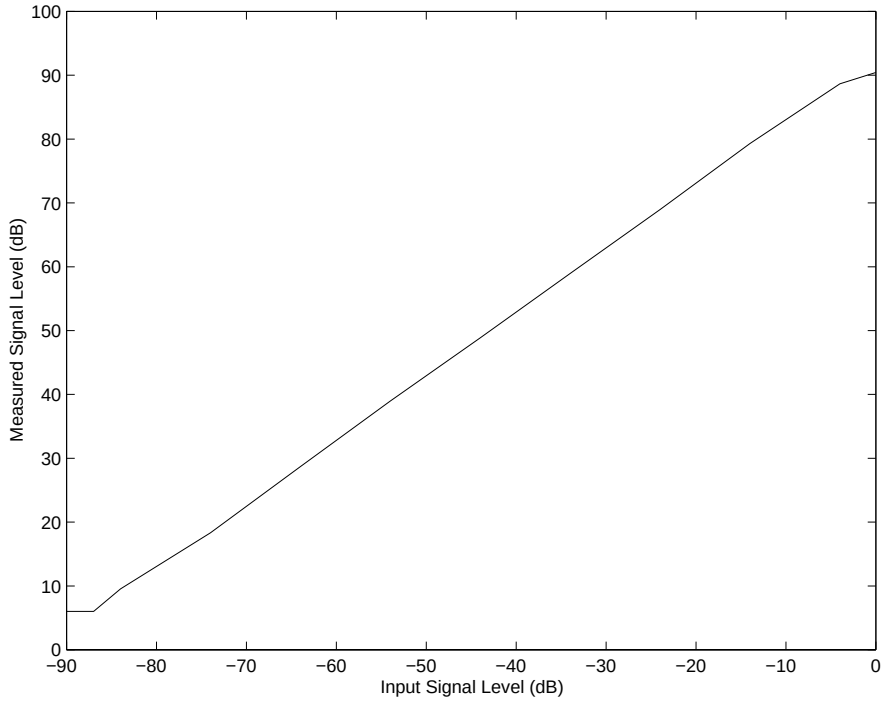


Figure 5.9: Test of the Dynamic Range of the Receiver (N=8)

The processing time for different integration numbers is shown in Table 5.2.

5.3.4 Signal Level and Noise Performance

In the 1.5 GHz RF Loop mode, the signal level was found to be 70 dB. And it actually represent a -25 dB signal level relative to a millivolt according to the measurement result from the spectrum analyzer. To measure the noise level, two sets of data are collected by the receiver. And then the first one is subtracted from the second one. It should be noticed that as the integration number increase by a factor of 8, the noise level is expected to drop by 9 dB. But during the measurement the noise level goes down only by 4 dB as the integration number increases from N=1 to N=8. This is because the noise present is not only white noise. By using the

spectrum analyzer, it can be seen that there are harmonics at frequencies other that at 11.6 MHz. A very narrow band bandpass filter is expected to get rid of other type of noise so that the noise level can be lower down as expected. The signal level for N=1 and N=8 integration numbers are shown in Figures 5.10 and 5.11.

5.4 Summary

A simple way to verify the functionality of the digital receiver is to feed a single frequency sinusoidal wave with a small frequency offset compared to the Down-Converting frequency as the analog input of the receiver, collect the data and plot it in time domain and frequency domain and check if the frequency offset and the SNR are as expected.

The noise level of the digital receiver is about 5dB (N=1). The dynamic range is around 80 dB and it takes 46μs (N=1) to get a pair of I and Q.

A very narrow band filter at 11.6MHz is needed to get rid of the interference from the harmonics so that the noise floor can be reduced efficiently as the integration number increases.

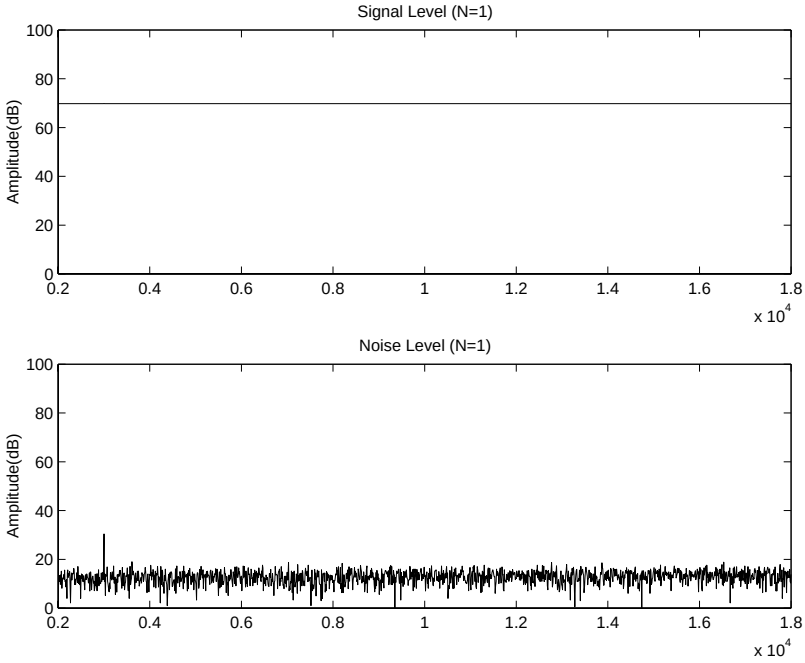


Figure 5.10: Signal and Noise Level (N=1)

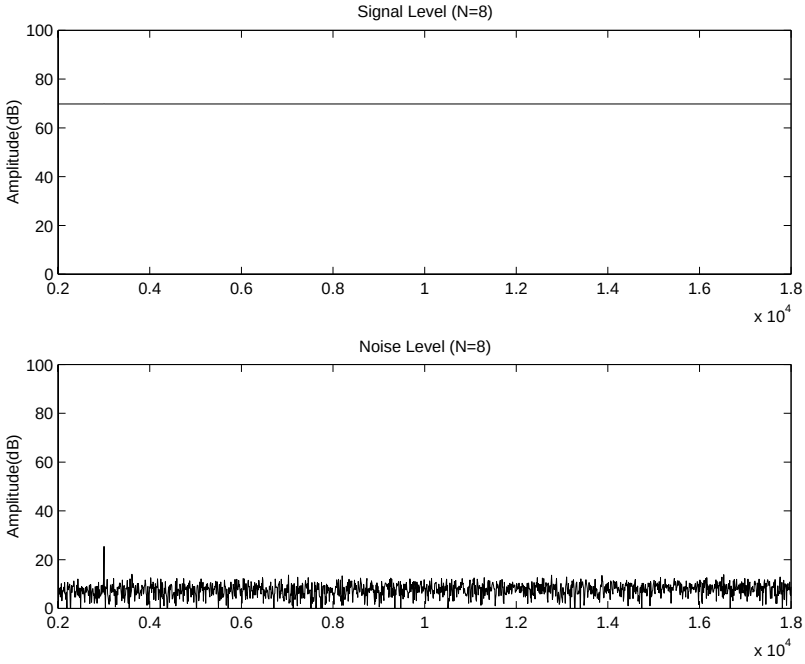


Figure 5.11: Signal and Noise Level (N=8)

CHAPTER 6

CONCLUSION

6.1 Conclusion

The new digital receiver for the compact range radar system has been described in this thesis. It has been designed to allow the user to efficiently configure the system parameters, to collect the desired measured data and to modify the structure for easy upgrade (muilti-channel system). This has been accomplished by using high-performance A/D, DDC, DSP and PIO boards. The major functions of the system are to oversample the 11.6 MHz signal to increase the SNR performance , downconvert and separate the I and Q channel digitally to the complex baseband to elimiate image and linearity problems, perform data format conversion and accumulation using the DSP board to lower down the noise level, and interface the DSP with the PC using a high-speed data acquisition card with build-in DMA channels to minimize the CPU load during the measurements.

The hardware and software associated with this new digital receiver has been coordinated so that data can be obtained in a most efficient manner. For example , it takes only 88 μs to get a pair of I and Q for an integration number of 8 while the old receiver need to take 1.6 ms to get it. Further speed improvement can be achieved by

using a faster PIO, DSP board and reprogram the DDC. The overall radar SNR set by the RF components is around 80 dB. The noise level of the new digital receiver is seen to be much lower than the old one (about 10 dB lower). Thus, the new receiver achieves a 60 dB SNR without integration. However, if one wishes to further reduce the noise floor efficiently by increaing the number of integration, one must add a very narrow band bandpass filter with center frequency of 11.6 MHz. Across this narrow filter, the noise should be white and the integration number should provide improved performance as expected.

6.2 Future Work

There are a few important tasks left to complete in the hardware development. First, since the radar system used has two channels, another receiver need to be built and data from the DDC into the DSP need to be feed in a TDM fashion. Second, for this system, the speed of the receiver is limited by the processing speed of the DSP , it would be desirable to upgrade the DSP board with the one with higher CPU processing power. Third, the minimum pulse width that generated by the PIO board is about 20μs , that cause time waste when sending the instructions to the DSP. It would be desirable to replace the PIO board with the one that is able to generate a minimum pulse width about 3μs so that the data acquisition speed can be further improved. At last, as mentioned in the previous section, a very narrow-band filter need to be added to get rid of the interference caused by the other harmonics.

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APPENDIX A

A.1 Connection Detail

Table A.1 Connection Diagram

Pin Name	Output Pin Number the DDC board	Data Flow	Pin Name	Output Pin Number of the Secondary Address Board
$\overline{PCWR1}$	14	$\leftarrow$	B0	10
$\overline{PCWR0}$	1	$\leftarrow$	B1	9
PCD0	2	$\leftarrow$	B2	8
PCD1	3	$\leftarrow$	B3	7
PCD2	4	$\leftarrow$	B4	6
PCD6	8	$\leftarrow$	B5	5
PCD7	9	$\leftarrow$	B6	4
$\overline{G1}$	17	$\leftarrow$	B7	3

APPENDIX B

B.1 Secondary Address

Secondary Address	Device Name and Control
1	Integration number (output). This indicates the number of samples to be accumulated in the 24-bit accumulators. 256 minus the integration number is sent to the control unit.
2	Trigger to start data collection(output). Sets by sending 0.
3	Data valid line(input). Ready to read from accumulator if the first bit is 0.
4	High byte for the I word of the channel A (input).
5	Middle byte for the I word of the channel A(input).
6	Low byte for the I word of the channel A(input).
7	Loop mode switch(output). Bit 0 is used to set SW14 for IF 1.5GHz loop back test of channel A. Bit 1 is used to set SW14 for IF 1.5GHz loop back test of channel B. Bit 2 is used to set SW16 for IF 100KHz loop back test of channel A. Bit 3 is used to set SW17 for IF 100KHz loop back test of channel B. Bit 4 is used to set SW5 and SW20 for 18 to 36 GHz(KA band) operation. For each bit, 1 means enable and 0 means disable.
8	High byte for the Q word of the channel A(input).
9	Middle byte for the Q word of the channel A(input).
10	Low byte for the Q word of the channel A(input).
11	RF loop back test switch and feed horn switch(output). Bit 0 is used to set SW8 for RF loop back test. Bit 1 is used to set SW13 for RF 1.5GHz loop back test. Bits 2 to 7 are for feed horn switches (for future expansion). For each bit, 1 means enable and 0 means disable.
12	High byte for the I word of the channel B(input).

Table B.1 Secondary Address for various transceiver components

Secondary Address	Device Name and Control
13	Middle byte for the I word of the channel B(input).
14	Low byte for the I word of the channel B(input).
15	Band selction switch(output)(controls SW2, SW6 and SW9). The high band(6-18 GHz) is selected if Bit 0 is 1. The low band(2-6 GHz) is selected if Bit 0 is 0.
16	High byte for the Q word of the channel B(input).
17	Middle byte for the Q word of the channel B(input).
18	Low byte for the Q word of the channel B(input).
19	Calibrator phase shifter(output)(PH1). The output range from 0 to 39 for a phase shift from 0 to 351 degrees. (Phase increment is 9 degrees)
20	Calibrator attenuator(output)(ATT-3). The output range from 0 to 128.(8 units represent 3dB attenuation)
21	Calibrator board selector(output). Calibrator is enabled by SW8 if output is 15. Calibrator is disabled by SW8 if output is 0.
22	IF reference phase shifter(output)(PH2). The output range from 0 to 128. The phase shift range from 0 to 357.1875 degrees. Ouput should be A*128/360 if a phase shift A is desired.
23	Phase flip(output). Enabled if bit 0 is 0. Disabled if bit 0 is 1.
24	6LSB is the parameter for the transmit frequency YIG filter(output).
25	6MSB is also the parameter for the transmit frequency YIG filter(output).
26	YIG lock ready line (input). YIG-1 is locked if bit 0 is 0.
27	YIG track or hold control(output). Track mode is selected if bit 0 is 0. Hold mode is selected if the output is 128.
32	Channel selecation of the auxiliary AD converter(output). Output 0 selects the ground reference. Output 1 selects the LO level(D1). Output 2 selects the TX1 level(D2). Output 3 selects the TX2 level(D3). Output 4 selects the RX1 level(D4). Output 5 selects the RX2 level(D5).
33	Data ready line for the auxiliary AD converter(input). Ouput 1 means data is ready.
34	8MSBs from the auxiliary AD converter(input).
35	4LSBs from the auxiliary AD converter(input).

Secondary Address	Device Name and Control
36	RF attenuation level(output)(ATT-2). The attenuation level range from 0 to 50dB. The attenuation level is X dB if the output is 5xX.
37	LO attenuation level(output)(ATT-1). The attenuation level range from 0 to 50dB. The attenuation level is X dB if the output is 5xX.
67	Pulse timing unit repetition interval(PRI)(output). The interval range from 30 to 2500 ns. The interval is 10xX ns if the output is X with the nibbles reversed.
68-71	Reserved.
72	Pulse trailing edge position'units'(output)(TU1). I can be set from 0 to 9 ns. Sending 128 turns the TU1 "on" and let the signal go through without modification.
73	Pulse trailing edge position'tens'(output)(TU1). The pulse trailing position is set to (10x'tens' value + 'units' value). Its value can not be greater than (PRI - 21) or than the leading edge position.
74	Pulse leading edge position'units'(output)(TU1). Sending 128 turns the TU1 "off" and let no signal go through.
75	Pulse leading edge position'tens'(output)(TU1). The pulse leading position is set to (10x'tens' value + 'units' value). It value can not be smaller than the trailing edge position.
76-79	Reserved.
80	Pulse trailing edge position'units'(output)(TU2). Sending 128 turns the TU2 "on".
81	Pulse trailing edge position'tens'(output)(TU2).
82	Pulse leading edge position'units'(output)(TU2). Sending 128 turns the TU2 "off".
83	Pulse leading edge position'tens'(output)(TU2).
84-87	Reserved.
88	Pulse trailing edge position'units'(output)(TU3). Sending 128 turns the TU3 "on".
89	Pulse trailing edge position'tens'(output)(TU3).
90	Pulse leading edge position'units'(output)(TU3). Sending 128 turns the TU3 "off".
91	Pulse leading edge position'tens'(output)(TU3).
92-95	Reserved.
96	Pulse trailing edge position'units'(output)(TU4). Sending 128 turns the TU4 "on".
97	Pulse trailing edge position'tens'(output)(TU4).

Secondary Address	Device Name and Control
98	Pulse leading edge position'units'(output)(TU4). Sending 128 turns the TU4 "off".
99	Pulse leading edge position'tens'(output)(TU4).
100-103	Reserved.
104	Pulse trailing edge position'units'(output)(TU5). Sending 128 turns the TU5 "on".
105	Pulse trailing edge position'tens'(output)(TU5).
106	Pulse leading edge position'units'(output)(TU5). Sending 128 turns the TU5 "off".
107	Pulse leading edge position'tens'(output)(TU5).
108-111	Reserved.
112	Pulse trailing edge position'units'(output)(TU6). Sending 128 turns the TU6 "on".
113	Pulse trailing edge position'tens'(output)(TU6).
114	Pulse leading edge position'units'(output)(TU6). Sending 128 turns the TU6 "off".
115	Pulse leading edge position'tens'(output)(TU6).
116-119	Reserved.

APPENDIX C

C.1 DDC Control Word Format

DESTINATION ADDRESS = 0

BIT POSITION	FUNCTION	DESCRIPTION
39-37	Address	000 = Control Word 0
36	Update	0 = Update Only This Control Register 1 = Update All Control Registers
35-32	Reserved	All Zeroes

PHASE GENERATOR/TEST ENABLE/OUTPUT REGISTER

DESTINATION ADDRESS = 1		
BIT POSITION	**FUNCTION**	**DESCRIPTION**
39-37	Address	001 = Control Word 1
36	Update	0 = Update Only This Control Register 1 = Update All Control Registers
35-4	Minimum Phase Increment	Bits 35-4 = $2^{31}...2^{0}$. Range: 0 < Minimum Phase Increment < π $(1\text{-}2^{-32})$ radians. In the CW mode this is the phase increment of the NCO which is added to the NCO intitial phase offset state. The desired Sin/Cos generator (local oscillator) frequency is set by the equation: **$f_C = (\text{phase increment}) f_S 2^{-33}$**; where f_C is the desired local oscillator frequency, f_S is the input sampling frequency, and phase increment is the control word value in hexidecimal. To calculate the value to be programmed into this field, use this equation: **phase increment = INT[f_C / f_S)2^{33}]hex** Some examples of phase increments and local oscillator frequencies: `00000000`h: f_C = zero frequency `00000001`h: $f_C = f_S / 2^{33}$ - lowest frequency (75MHz x 2^{-33} = 8.73mHz) `10000000`h: $f_C = f_S$ /32 `20000000`h: $f_C = f_S$ /16 `40000000`h: $f_C = f_S$ /8 `80000000`h: $f_C = f_S$ /4 `ffffffff`h: $f_C = (0.49999) f_S$ - highest frequency (75MHz x 2^{-33} = 37.49MHz) In the CHIRP modes, this is the smallest allowable phase increment. In the Filter Only mode, this parameter should be set to 0.
3	Test Enable	0 = Test Features Disabled 1 = Test Features Enabled
2-0	Phase Generator Mode	000 = Filter Only 001 = Normal Mode (CW) 010 = Reserved 011 = Up Chirp 100 = Reserved 101 = Down Chirp 110 = Reserved 111 = Up/Down Chirp ***Note that the lsb sets the gain through the DDC as follows:*** ***0 = Gain is1*** ***1 = Gain is 2***

Table C.1: Control Word Format

PHASE GENERATOR REGISTER

DESTINATION ADDRESS = 2		
BIT POSITION	**FUNCTION**	**DESCRIPTION**
39-37	Address	010 = Control Word 2
36	Update	0 = Update Only This Control Register 1 = Update All Control Registers
35-32	Reserved	All Zeroes
31-0	Maximum Phase Increment	Bits 31-0 = 2^{31}... 2^{0}. Range: is 0 < Maximum Phase Increment < $\pi(1-2^{-32})$ radians. This parameter is only used in the CHIRP modes, and this is the largest allowable phase increment. Set to 0 in the Filter Only and CW modes.

PHASE GENERATOR/OUTPUT TIME SLOT REGISTER

DESTINATION ADDRESS = 3		
BIT POSITION	**FUNCTION**	**DESCRIPTION**
39-37	Address	011 = Control Word 3
36	Update	0 = Update Only This Control Register 1 = Update All Control Registers
35-32	Reserved	All Zeroes
31-18	Time Slot Length	Time Slot Length in IQCLK Periods; Bits 31-18 = 2^{13}... 2^{0}. Range is (19,25, 33, 37, 39, 49, 65 and 77) The equation for calculating the value for this field is: **TSL = [[(Number of Output Bits + 2)Mode] + 1]Hex**; where mode is 2 if the DDC is in either the real or I followed by Q mode. Mode is 1 for all other DDC operational modes. Allowable Minimum Time Slot Lengths: (18)1 + 1 = 19 (13 hexidecimal) (18)2 + 1 = 37 (25 hexidecimal); Real Output or I followed by Q (24)1 + 1 = 25 (19 hexidecimal) (24)2 + 1 = 49 (31 hexidecimal); Real Output or I followed by Q (32)1 + 1 = 33 (21 hexidecimal) (32)2 + 1 = 65 (41 hexidecimal); Real Output or I followed by Q (38)1 + 1 = 39 (27 hexidecimal) (38)2 + 1 = 77 (4d hexidecimal); Real Output or I followed by Q
17-0	Phase Offset	Starting Phase Angle of Phase Accumulator; Range = 0 to 2π. Bits 17-0 = 2^{32}... 2^{15}. Some example phase offset hexidecimal values : `0000` - 0 `1000` - $\pi/2$ `2000` - π `3000` - $3\pi/2$ `3fff` - 2π

Table C.2: Control Word Format(Continued)

PHASE GENERATION/HDF.OUTPUT REGISTER

DESTINATION ADDRESS = 4		
BIT POSITION	**FUNCTION**	**DESCRIPTION**
39-37	Address	100 = Control Word 4
36	Update	0 = Update Only This Control Register 1 = Update All Control Registers
35-33	Reserved	All Zeroes
32-31	Output Spectrum	00 = No Up Conversion,Complex Output 01 = Up Convert by f"/4, Real Output 10 = Up Convert by f"/2,Complex Output 11 = Reserved Mode
30-7	Delta Phase Increment	24-Bit Delta Phase Increment. Bits 30-7 = 2^{23}... 2^{0}. Range: 0 < Delta Phase Increment < π (2^{-8}-2^{-32})
6-1	HDF Data Shift (Shift Factor)	16-Bit HDF Gain Compensation Number - the shift portion. HDF Input Data Shift (Towards LSB). Bits 6-1 = 2^{5}...2^{0}. Range: 0 ≤ Shift Factor ≤ 55 decimal; Range: [0 ≤ Shift Factor ≤ 37]hex Calculate the value for this field using this equation: **HDF Data Shift = [75 - Ceiing(5 $\log_2$(R))]hex** Note: $\log_2(x) = (3.32)\log(x)$
0	Spectral Reverse	0 = Normal Output 1 = Spectrally Reversed Output

HDF/OUTPUT REGISTER

DESTINATION ADDRESS = 5		
BIT POSITION	**FUNCTION**	**DESCRIPTION**
39-37	Address	101 = Control Word 5
36	Update	0 = Update Only This Control Register 1 = Update All Control Registers
35-21	HDF Decimation Counter Preload (HDF DCP)	HDF Decimation Counter Preload. Range: 15 < HDF Decimation Counter Preload < 32,767 Calculate the value for this feild using this equation: **HDF DCP = R - 1;** where R is the HDF decimation (rate change) factor. Common HDF decimation (rate change) factors and associated hexidecimal HDF DCP values: `000f`: R = 16 `00ff`: R = 128 `01ff`: R = 512 `03ff`: R = 1,024 `07ff`: R = 2,048 `0fff`: R = 4,096 `1fff`: R = 8,192 `3fff`: R = 16,384 `7fff`: R = 32,768

Table C.3: Control Word Format(Continued)

HDF/OUTPUT REGISTER (Continued)

<table>
<tr><th colspan="3">DESTINATION ADDRESS = 5</th></tr>
<tr><th>BIT POSITION</th><th>FUNCTION</th><th>DESCRIPTION</th></tr>
<tr><td>20-5</td><td>Scaling Multiplier Gain (Scale Factor)</td><td>16-Bit HDF Gain Compensation Number - the multiplier portion.
Range: 1 ≤ Scale Factor < 2,
Field Format = $2^0.2^{-1}...2^{-15}$.
Calculate the value for this field using this equation:
Scale Factor = $2^{CEILING(5log_2(R))}/(R)^5$, where R is the HDF decimation (rate change) factor and CEILING(x) is equal to x for integer values, otherwise is equal to the next higher integer.
Common HDF decimation factors (R), decimation counter preload (DCP) and Scale Factors (SF) values:

<table>
<tr><th>R</th><th>DCP(dec)</th><th>DCP(hex)</th><th>SF(dec)</th><th>SF(hex)</th></tr>
<tr><td>16</td><td>15</td><td>000f</td><td>1.000</td><td>8000</td></tr>
<tr><td>128</td><td>127</td><td>007f</td><td>1.000</td><td>8000</td></tr>
<tr><td>512</td><td>511</td><td>01ff</td><td>1.00</td><td>8000</td></tr>
<tr><td>1,024</td><td>1,023</td><td>03ff</td><td>1.000</td><td>8000</td></tr>
<tr><td>2,048</td><td>2,047</td><td>07ff</td><td>1.000</td><td>8000</td></tr>
<tr><td>4,096</td><td>4,095</td><td>0fff</td><td>1.000</td><td>8000</td></tr>
<tr><td>8,192</td><td>8,191</td><td>1fff</td><td>1.00</td><td>8000</td></tr>
<tr><td>16,384</td><td>16,382</td><td>3fff</td><td>1.00</td><td>8000</td></tr>
<tr><td>32,768</td><td>32,768</td><td>7fff</td><td>1.000</td><td>8000</td></tr>
</table>

Note that the Scale Factor is 1 (8000hex) for power of 2 decimation factors.
The compensation for the HDF gain is performed with a shifter and a multiplier. Thus to program the HDF Gain compensation, there is an associated Shift Factor and the Scale Factor. As the Decimation Factor increases, the multiplier moves away from the value 1 and approaches the value 2. When the calculated value for the multiplier equals or exceeds 2, the shifter is incremented and the multiplier returns to 1 and increases towards 2 again as the Decimation Factor increases.

As an example, the table below details the values of Scale Factor for values of R from 16 to 32:

<table>
<tr><th>R</th><th>DCP(dec)</th><th>DCP(hex)</th><th>SF(dec)</th><th>SF(hex)</th></tr>
<tr><td>16</td><td>15</td><td>000f</td><td>1.000000000</td><td>8000</td></tr>
<tr><td>17</td><td>16</td><td>0010</td><td>1.477013647</td><td>BD0E</td></tr>
<tr><td>18</td><td>17</td><td>0011</td><td>1.109857915</td><td>8E0F</td></tr>
<tr><td>19</td><td>18</td><td>0012</td><td>1.693916116</td><td>D8D2</td></tr>
<tr><td>20</td><td>19</td><td>0013</td><td>1.310720000</td><td>A7C5</td></tr>
<tr><td>21</td><td>20</td><td>0014</td><td>1.026983417</td><td>8374</td></tr>
<tr><td>22</td><td>21</td><td>0015</td><td>1.627707993</td><td>D058</td></tr>
<tr><td>23</td><td>22</td><td>0016</td><td>1.303318981</td><td>A6D3</td></tr>
<tr><td>24</td><td>23</td><td>0017</td><td>1.053497942</td><td>86D9</td></tr>
<tr><td>25</td><td>24</td><td>0018</td><td>1.717986918</td><td>DBE6</td></tr>
<tr><td>26</td><td>25</td><td>0019</td><td>1.412060017</td><td>B4BE</td></tr>
<tr><td>27</td><td>26</td><td>001a</td><td>1.169233029</td><td>95A9</td></tr>
<tr><td>28</td><td>27</td><td>001b</td><td>1.949663831</td><td>F98E</td></tr>
<tr><td>29</td><td>28</td><td>001c</td><td>1.635911864</td><td>D165</td></tr>
<tr><td>30</td><td>29</td><td>001d</td><td>1.380840823</td><td>B0BF</td></tr>
<tr><td>31</td><td>30</td><td>001e</td><td>1.172037271</td><td>9605</td></tr>
<tr><td>32</td><td>31</td><td>001f</td><td>1.000000000</td><td>8000</td></tr>
</table>
</td></tr>
<tr><td>4-3</td><td>Output Format</td><td>00 = Two’s Complement
01 = Offset Binary
10 = Sign Magnitude
11 = Single Precision Floating Point Format</td></tr>
</table>

Table C.4: Control Word Format(Continued)

HDF/OUTPUT REGISTER (Continued)

DESTINATION ADDRESS = 5		
BIT POSITION	**FUNCTION**	**DESCRIPTION**
2-1	Number Of Output Bits	00 = 16 Bits 01 = 24 Bits 10 = 32 Bits 11 = 38 Bits
0	Output Sense	0 = LSB First 1 = MSB First

INPUT AND OUTPUT FORMAT REGISTER

DESTINATION ADDRESS = 6		
BIT POSITION	**FUNCTION**	**DESCRIPTION**
39-37	Address	110 = Control Word 6
36	Update	0 = Update Only This Control Register 1 = Update All Control Registers
35	I followed by Q	0 = I and Q Output Separately 1 = I and Q Data Output on I Pin
34-29	Time Slot Number	Bits 34-29 = $2^5 \ldots 2^0$. Range: 0 < Time Slot Number < 63. This implies that 64 different channels may be mutliplexed, assigning one time slot per channel.
28	IQCLK Polarity	0 = Output Data Stable On Rising Edge Of IQCLK; IQCLK High between I or Q Bit Periods when IQCLK Duration = 0. 1 = Output Data Stable on Falling Edge of IQCLK; IQCLK Low between I or Q Bit Periods when IQCLK Duration = 0.
27	IQCLK Duty Cycle	0 = IQCLK Active Time = CLK Period. 1 = 50% Duty Cycle
26	IQCLK Duration	0 = Active During I or Q Output Periods Only 1 = Active Continuously
25-24	IQCLK Three-State Control	00 = Three-State IQCLK 01 = Enable IQCLK 1x = Auto-Three-State Enable IQCLK (during time slot)
23	IQSTB Polarity	0 = Active High 1 = Active Low
22	IQSTB Location	0 = IQSTB Prior to the Beginning of the Data Word. 1 = IQSTB During the Data Word.
21-20	IQSTB Three-State Control	00 = Three-State IQSTB 01 = Enable IQSTB 1x = Auto Three-State Enable IQSTB (during time slot)
19	I Polarity	0 = True Data 1 = Inverted Data
18-17	I Three-State Control	00 = Three-State I 01 = Enable I 1x = Auto Three-State Enable I (during time slot)
16	Q Polarity	0 = True Data 1 = Inverted Data

Table C.5: Control Word Format(Continued)

INPUT AND OUTPUT FORMAT REGISTER (Continued)

DESTINATION ADDRESS = 6		
BIT POSITION	**FUNCTION**	**DESCRIPTION**
15-14	Q Three-State Control	00 = Three-State Q 01 = Enable Q 1x = Auto Three-State Enable Q (during time slot)
13	Input Format	0 = Offset Binary 1 = Two's Complement
12-0	IQCLK Rate Counter Preload	I/QCLK Rate Counter Preload, Bits 12-0 = $2^{12} \cdots 2^{0}$. Range: 2 ≤ IQCLK Rate Counter Preload ≤ 1701. To calculate the value in this field use this equation: **IQCLK Rate Counter Preload = [FLOOR[(HDF Decimation Factor x 4)/TSL] - 1]hex**; where FLOOR(x) represents the integer part of x, and TSL is the decimal value of Control Word 3, bit 31-18.

PHASE OFFSET REGISTER

DESTINATION ADDRESS = 7		
BIT POSITION	**FUNCTION**	**DESCRIPTION**
39-37	Address	111 = Control Word 7
36	Update	0 = Update Only This Control Register 1 = Update All Control Registers
35-14	Reserved	All Zeroes
13	Data	0 = Normal Data Input 1 = Force Input Data to 8000 Hex.
12-11	FIR Accumulator Control	00 = Normal Accumulation - The accumulator is reset on every FIR cycle. 01 = No Accumulation -The accumulator is disabled. 10 = Continuous Accumulation -The accumulator is not reset on every FIR cycle. This test mode was created to allow the user to perform the equivilent of a check sum test. A very long term test could be run and an accumulated output would yeild a specific numeric value. If the answer differed, the part is not functioning properly. 11 = Reserved
10	Q Strobe on Roll Over	0 = Q carries Normal Data 1 = Q Strobes When Phase Generator Rolls Over
9	Force Outputs	0 = Normal Output Response 1 = Force Outputs
8	IQCLK Forced Data	If Bit 9 = 1, Force IQCLK = Bit 8; Else Normal
7	IQSTB Forced Data	If Bit 9 = 1, Force IQSTB = Bit 7; Else Normal.
6	I Forced Data	If Bit 9 = 1, Force I = Bit 6; Else Normal.
5	Q Forced Data	If Bit 9 = 1, Force Q = Bit 5; Else Normal.
4	Sin/Cos Generator Bypass	0 = Sin Cos Generator Normal, 1 = Bypass Sin Cos Generator; Sin = Cos = 0.fffff (approximately 1)
3	Scaling Multiplier Bypass	0 = Scaling Multiplier Normal, 1 = Scale Factor = 1.
2	Reserved	Must be Zero for Proper Operation while Test Features are Enabled.
1	Wait For RAM Full	If Bit = 0, DDC will Output Data Normally after a Reset, which will Include Unpredictable Data in Data RAMs. If Bit = 1, No Chip Output will Occur until Sufficient Data RAM Locations are Written.
0	Disable Overflow Protection	0 = Normal Operation 1 = Disable Overflow Protection

Table C.6: Control Word Format(Continued)