Statistical Yield Optimization of Analog MOS Integrated Circuits

A THESIS

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By

Hua Su, B.S., M.S.,

* * * * *

The Ohio State University

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Master's Examination Committee:

Dr. Mohammed Ismail

Dr. Patrick Roblin

Approved by

Adviser

Department of Electrical Engineerir

To my parents

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VITA

November 11, 1966 ..... Born – Beijing, China

June, 1987 ..... B.S. in Physics,
Peking University,
Beijing, China

1987-1988 ..... Teaching Associate,
Physics Department,
City University of New York,
New York, New York

1988-1992 ..... Teaching Associate,
Physics Department,
The Ohio State University,
Columbus, Ohio

September, 1990 ..... M.S. in Physics,
The Ohio State University,
Columbus, Ohio

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Statistical Modeling and Optimization of Analog MOS Circuits

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CHAPTER I

Introduction

1.1 Background

For analog MOS integrated circuit design, the variation in circuit performance arising from device parameter variations should be evaluated. Especially, when all MOS devices are scaled to meet increasingly demanding circuit specifications, process variances including both inter - and intra - die variations significantly affect the reliability of the circuit performance. To produce integrated circuits with acceptable yields, the effect of these random process variations should be included in the design phase.

SMOS (Statistical MOS) [1, 2, 3] is a statistical device model which includes the effects of random parameter variationas on both interdie (die - die) and intradie (parameter mismatch on each die). It has been successfully incorporated into two existing circuit simulators, SPICE [4] and APLAC [5, 6]. The parameter mismatch in NMOS as well as PMOS transistors have been tested and implemented in the circuit simulators. SMOS model has been used to examine the effects of process variation on both analog and digital circuits [7, 8, 9].

With the aid of this SMOS (Statistical MOS) model, it is presently possible to simulate the effects of device dimensions, bias, and circuit layout on the variability

of circuit performance. Therefore, optimization of all factors under the control of the circuit designer is possible. In contrast, previous studies in statistical circuit design and optimization did not account for two key factors contributing to device mismatch: device size and layout.

1.2 Research Focus

The core of this research is to develop a practical optimization algorithm which, together with the SMOS model, can create a practical CAD environment for integrated circuits [3, 7]. The investigation and comparison of different optimization algorithms is required to determine which is most suitable for this application. In this thesis, we are going to investigate two different optimization algorithms, which are steepest-descent method and experimental design method. The goal of these optimizations may be for the user to determine the best circuit modification (change in device dimension or bias condition) to achieve a user specified functional yield. Previously, this form of optimization was unrealizable, since the models employed did not include the effect of device size on circuit variances. To perform the statistical circuit optimization, the other basic optimization techniques such as design centering etc. will also be needed. The demand for more complex integrated circuits has continue to force a decrease in device geometries and minimum feature size. This signifies the necessity of the optimal design of the device size while to achieve the yield specifications. A major difficulty faced by various approach to statistical circuit design has been prohibitively high computational cost and as a result their practical application has been limited to relatively small circuits. Thus, the affordable computational cost

(or the simulation time) has to be considered.

1.3 Organization of Thesis

The organization of this thesis is as following. Chapter II reviews some important issues of the Statistical MOS (SMOS) Model and describes the CAD implementation of the model to the APLAC (originally Analysis Program for Linear Active Circuits) simulator.As a part of the study of the APLAC, a nominal circuit optimization example will also be discussd. Chapter III and IV investigate two different optimizaion algorithms which are conventional steepest-descent method and statistical experiment design method with the aid of SMOS model and APLAC simulator. Two basic analog building circuits, current mirror and Miller-compensated operational amplifier, will be examined with the steepest-descent method. A review of the experiment design method and its applications will be discussed in Chapter IV and also the Miller compensated operational amplifier circuit will be examined. Finally, Chapter V provides the conclusions of this project, a comparison of the above mentioned two algorithms will be discussed. In addition, it gives some suggestions for the future work in this area.

CHAPTER II

Statistical MOS Model and CAD Implementation

2.1 Statistical MOS Model

2.1.1 Survey of statistical modeling

As the minimum feature size in MOS analog circuits has been reduced due to more ambitious performance requirements, the statistical variation of device characteristics can be very significant. An accurate statistical model which includes the effect of parameters, such as device geometries and circuit layout is required in order to perform the statistical simulation of the analog integrated circuits. Generally, the Monte Carlo techniques should be employed and the model should be incorporated into any exsiting circuit simulator [2, 3].

The statistical variations can be classified as intradie and interdie fluctuations [2, 9, 10]. Interdie variations mainly arise from the wafer to wafer process while the intradie device mismatch caused by the similarly designed transistors under the same biasing conditions. The interdie variability is normally much larger than the intra device mismatch and is taken into account on the performance of the digital circuits. However, device mismatch contributes significantly to the variances of the circuit performance of the analog circuits. Therefore, a statistical model which counts for

the device mismatch is necessary for the analog circuits.

Previous research in this area can be summerized as following. Shyu *et al.* [11] investigated the random errors of current sources and capacitors. All tansistor variances are derived in terms of their effect on the current matching in a current mirror. The most important random error process (which is dependent of the transistor areas) for the large capacitors is due to the oxide variarions and for small values the edge variations which are explained by the channel length and width mismatch dominate. Lakshmikumar *et al.* [12] futhered Shyu's work by seperating the area dependence of transistor mismatch into the variance model and described MOS transistor matching by means of the two parameters which are the threshold voltage (V_T) and the current factor (β). Pelgrom *et al.* [13] improved the previous work by including substrate factor and adding a spacing dependent term to the parameter variance model. The general parameter is characterized as:

$$\sigma^2(\Delta P) = \frac{a_p}{WL} + {s_p}^2 {D_{12}}^2 \tag{2.1}$$

where a_p and s_p are the fitting constants relating the parameter variance to the device area (WL) and seperation distance (D_{12}), respectively.

Though the previous three studies on the mismatsh of the MOS transitors determined the functionality of the device mismatch, the mismatch variance equations do not provide a method to calculate the actual parameter and have failed to incorporate to the circuit simulator. A new improved statistical model will be introduced and it resolves the above mentioned problems.

2.1.2 SMOS model

SMOS (Statistical MOS) model, a general CAD compatible parameter level statistical model was originally developed at the Ohio State University [2, 8, 1]. This model comprehends the effect of device area, transistor bias and circuit layout on the variance of the MOS integrated circuits. The parameter mismatch variance is based on the Pelgrom's work. To calculate a statistically significant value for parameter P, the following equation is employed:

$$P = \mu_p + \sigma_p R \tag{2.2}$$

where μ_p is the mean of P, σ_p is the standard deviation of P and the R is a random variable which is sampled by the Monte Carlo technique and has the same distribution as P. Since the correlation between model parameters inherent to device models has to be preserved and the variance of these parameters across the die has to be considered, the statistical PCA (Principle Component Analysis) and σ-Space Analysis (σSA) were employed. The PCA and σSA are used to preserve parameter correlations and the seperation distance dependence of the parameter variance, respectively. Therefore, for a given circuit layout, the coefficient matrix of PCA and σSA will be calculated through the parameter extraction of the devices with varying dimensions and seperation distances. Appendix A listed a sample model file calculated by the SMOS model. SMOS model is also very general in nature and has been implemented into the SPICE and APLAC circuit simulator. The accuracy of this model has been verified by simulation results as well as the experimental testing.

2.2 CAD Implementation of SMOS Model

2.2.1 Introduction of APLAC

APLAC (Analysis Program for Linear Active Circuit) has been developed in the Helsinki University of Technology since 1972 [5, 6]. It provides the user an extremely flexible environment to do the circuit analysis. APLAC is capable of carrying out dc, ac, noise, transient, oscillator and multitone harmonic steady-state analysis. Monte Carlo analysis is available in all basic analysis modes and sensitivity analysis is available in dc and ac modes. The MOSFET models included in APLAC are exactly the same as those in SPICE [4]. APLAC has some advantages over SPICE in the area of simulation flexibility. In addition, the circuit simulations can be performed much faster in APLAC implementation than in SPICE. More importantly, APLAC is an object-oriented program and is realized by creating C-macros which take into account specific needs of circuit simulation, essentially, simplify modeling. Some more advanced tasks, such as nominal optimization and microwave s-parameter analysis etc., are also available in APLAC. APLAC contains five different optimization methods: conjugate gradient, minmax, random, manual tuning and design centering. Any parameter in the design program can be used as an optimization variable and any user-defined function may act as an optimization objective.

2.2.2 APLAC Implementation of SMOS Model

Since APLAC is an object-oriented program capable of performing circuit simulation in a C-language programming environment, the SMOS model has been implemented

as an object file called *smos.c*. In another word, SMOS is incorporated as a subroutine within the APLAC source code. As an example of the use of SMOS, a typical SMOS statement of three transistor circuit is shown as following [7, 2]:

SMOS nstat FILE chip.st NPCA 6 NTRAN 3 NPAR 16

+ XY

+ 0 0

+ 0 5

+ 0 10

Once the above command is read, the APLAC calls SMOS and transfers to it the identifier values. The fixed part after SMOS is the name of the model only. FILE is followed by a string "chip.st" which the name of the model file. The rest part of the first line indicates the number of PCA coefficients (which is 6), the number of transistors (which is 3) and the number of statistically varying model parameters in the model file (which is 16) in the example respectively. The subsequent lines contain the layout information. The coordiantes of each transistor follow the XY identifier. Each time model calculations for a group of transistors described by a given "SMOS" are desired, an SME function is called. An example of the SME call is as following [7, 3]:

Call SME(nstat, "calculation flag")

SME function calls the model calculation routine which includes the model name (the same as in SMOS line) and a calculation flag. The possible calculation flags are:

"A"which tells the model calculation routine to calculate the layout dependent variance terms; "P" which signals the routine to use the previous layout information; and "N" which is used for the nominal circuit simulation. Any further developement work on SMOS requires only working with C-language object file smos.c which includes the code of the SME access function and the SMOS definition routine.

2.2.3 Nominal Circuit Optimization Example with APLAC

Circuit Description

As a study of the advanced task in APLAC, a nominal circuit optimization example will be discussed as following. Figure 1 shows a linear all-MOS floating resistor circuit using MOSFETs in the saturation region. The nodes V_X and V_Y are the two terminals of the resistor and $I_{IN} = I_{OUT}$ is the current that flows through the resistor [14]. One of the major advantages of this CMOS floating resistor circuit is that it has a reasonable big tuning capability. In another words, the resistance range is fairly wide. The resistance of this CMOS floating resistor is :

$$R = \frac{1}{4K_1(V_c - V_{ss})} \tag{2.3}$$

where

$$K_1 = \frac{1}{2}\frac{W_1}{L_1}\mu_o C_{ox} \tag{2.4}$$

which is inversely proportional to V_c-V_{ss}, that is the resistance will be increased as we increase the absolute value of the control voltage V_c. Considering the different applications of this CMOS floating resistor circuit, we would like to optimize the

resistance range and the swing of the input voltage by changing the device sizes in order to achieve the target total harmonic distortion value of one percent. The optimization variables will be the device sizes and the optimization objective is the total harmonic distortion. The APLAC language program is shown in APPENDIX B.

Resistance Range Optimization

Before the optimization, the total harmonic distortion simulation of the circuit has been done with the original designed device sizes. This simulation was done as the amplitude of the input voltage was set at 1.0V which was also for the optimization. The simulation results show that the total harmonic distortion has a minimum when the control voltage is equal to -3.1V. The THD vs. control voltage(V_c) curve is as a bell shape(referring to Figure 2). We also notice that the total harmonic distortion value is greater than one percent when the control voltage is beyond the range of -2.5V and -3.8V. Therefore, for each control voltage beyond that range, we optimize the circuit in order to achieve the target total harmonic distortion value of one percent. We found that the target vaule can be achieved only at $V_c = -3.8V$ and $V_c = -2.5V$. With the optimized devices sizes, we simulated the total harmonic distorion value vs. the control voltage and the results are presented in Table 1 and Table 2.

Input Voltage Swing Optimization

The simulation of the THD value vs. the amplitude of the input voltage have aslo been done before the optimization. The control volatge was set at -3.1V at which the

THD value is minium for a specific input voltage. From the simulaton results, we found that the total harmonic distortion increases as the input voltage increases and it is greater than one percent when the amplitude of the input voltage is greater than 1.5V(referring to Figure 3). Similar to what we have done in the first optimization, we optimize the circuit for input voltages greater than 1.5V in order to achieve the THD goal less than one percent. The results which were presented in Table 3 and Table 4 show that this goal can be achieved as the amplitude of the input volatge increased to 1.7V.

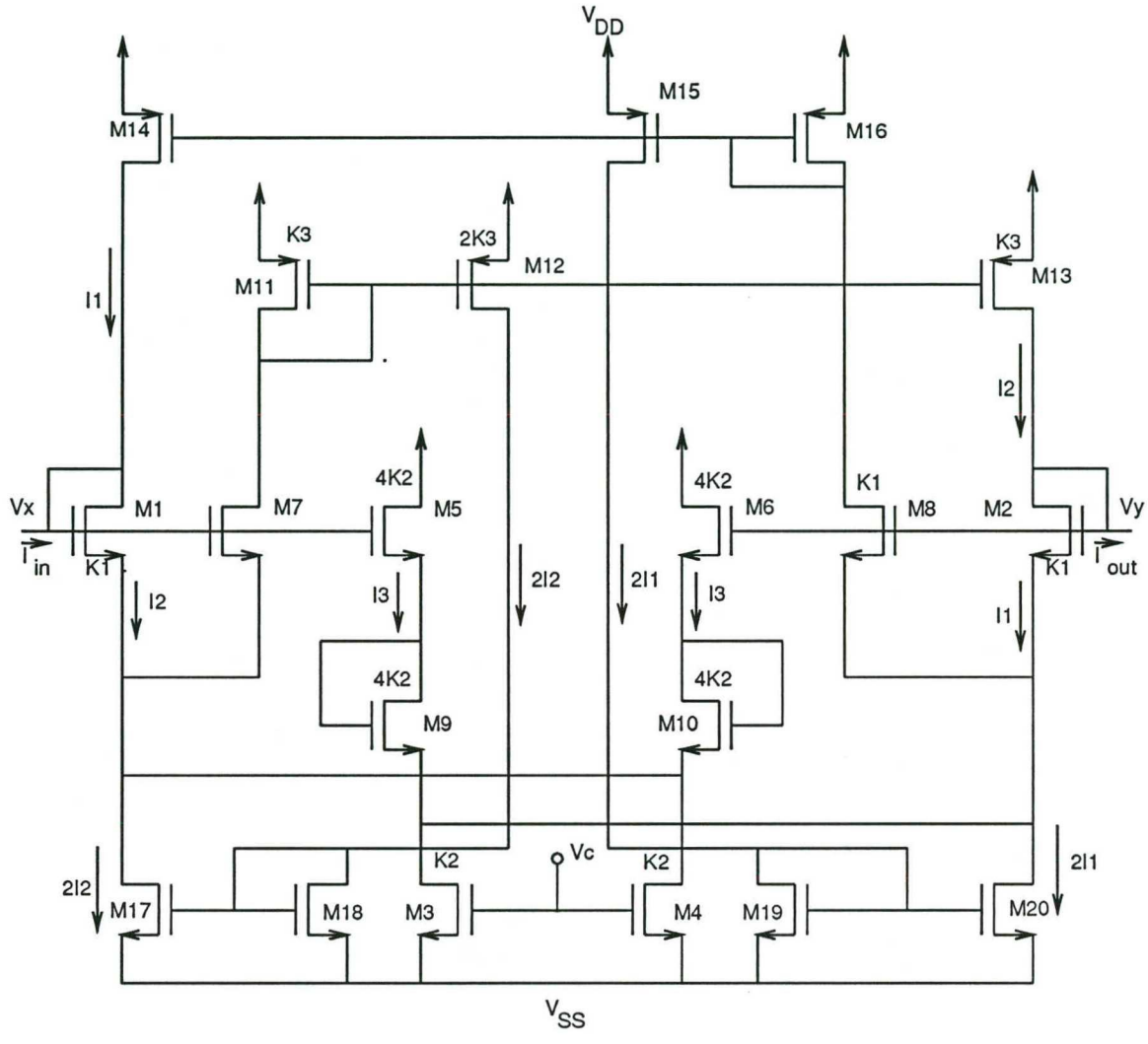

Figure 1: CMOS Floating Resistor Circuit

Table 1: Nominal circuit optimization of CMOS floating resistor circuit. The results of the optimized sizes for 1.0V input voltage.

Device Sizes	Original Values	Optimized Values
$a_1(\mathrm{nm}^2)$	1.70	1.48
$L_2(\mu\mathrm{m})$	5.00	7.81
$W_3(\mu\mathrm{m})$	10.00	13.20
$W_4(\mu\mathrm{m})$	5.00	4.00

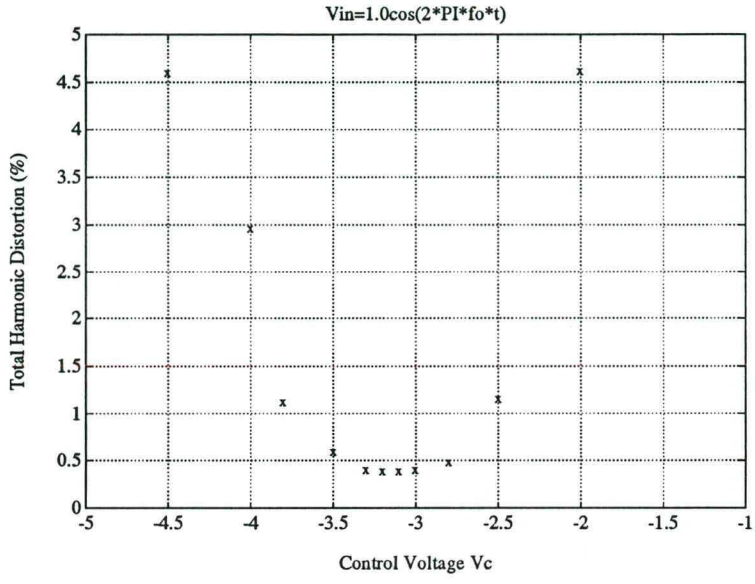

Figure 2: Total harmonic distortion vs. the control voltage of the CMOS floating resistor circuit.

Table 2: Nominal circuit optimization of CMOS floating resistor circuit. The results of the optimized THD values for 1.0V input voltage.

Control Voltage(Vc)	Original THD(%)	Optimized THD(%)
-4.0V	4.59	2.08
-3.8V	1.12	966.51m
-3.5V	591.73m	453.68m
-3.3V	398.59m	213.53m
-3.2V	384.09m	196.76m
-3.1V	383.92m	196.62m
-3.0V	385.17m	207.36m
-2.8V	476.38m	298.85m
-2.5V	1.15	971.37m
-2.0V	4.61	3.92

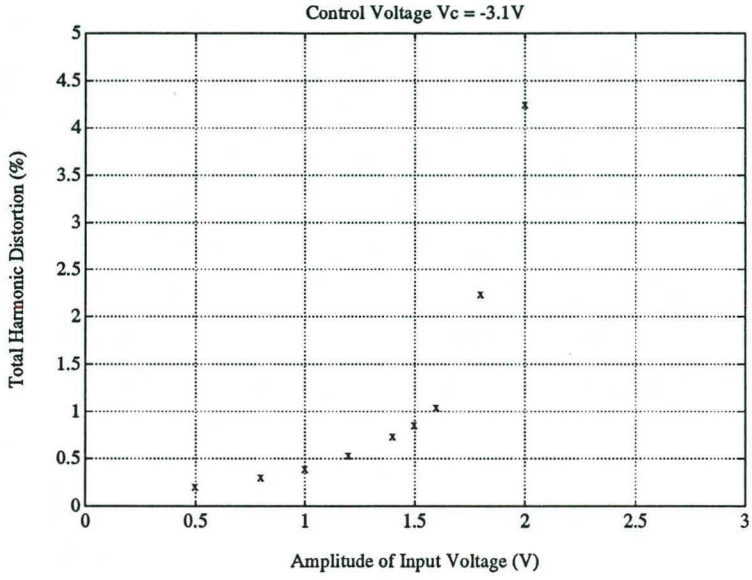

Figure 3: Total harmonic distortion vs. the amplitude of the input voltage of the CMOS floating resistor circuit.

Table 3: Nominal circuit optimization of the CMOS floating resistor circuit. The results of the optimized device sizes for the -3.1V control voltage.

Device Sizes	Original Values	Optimized Values
$a_1(\mathrm{n}m^2)$	1.70	1.84
$L_2(\mu\mathrm{m})$	5.00	7.16
$W_3(\mu\mathrm{m})$	10.00	17.17
$W_4(\mu\mathrm{m})$	5.00	5.69

Table 4: Nominal circuit optimization of the CMOS floating resistor circuit. The results of the optimized THD values for the -3.1V control voltage.

Input Voltage(V_{in})	Original THD(%)	Optimized THD(%)
0.5V	194.01m	163.59m
0.8V	293.35m	253.98m
1.0V	383.92m	322.13m
1.2V	526.40m	429.45m
1.4V	729.62m	599.64m
1.5V	851.33m	707.70m
1.6V	1.04	828.54m
1.7V	1.48	998.32m
1.8V	2.23	1.31
2.0V	4.24	2.89

CHAPTER III

Statistical Circuit Optimization: Steepest-Descent Method

In this chapter, we are going to develop a statistical circuit optimization method with the aid of the SMOS model and the APLAC circuit simulator. This method will result in the achievement of the nominal circuit specifications as well as a desired functional circuit yield. In general, the circuit performance variations are caused by the device mismatch the inter-die process variations. However, the effect of the inter-die process variations can be reduced by using the external bias controls or automatic tuning techniques. Therefore, device mismatch is the only process variation which we will consider in our circuit optimization. A general and successful model for MOS parameter mismatch variance was first presented by Pelgrom [13]. To decrease the standard deviation of a circuit performance criterion, or to increase functional circuit yield, the device areas must be increased, resulting in a reduction in the magnitude of device mismatch. Since the circuit performance is dependent on the channel length and the aspect ratio, that is the performance mean shifts as the device area changes, increased the device area does not necessarily result in the increased circuit yield. Hence the design centering technique has to be included in the yield optimization.

3.1 Optimization Methodology

3.1.1 Steepest-Descent Methodology

As we mentioned earlier, the circuit performance mean shifts as the device area increases. In our optimization procedure, we have to include the nominal optimization loop, the Monte Carlo loop as well as the statistical optimization loop(referring to Figure 4). Basically, the nominal optimization loop, which employs the standard min-max optimization method implemented in APLAC, centers the design to user desired circuit performance specifications by adjusting the aspect ratios of the devices. The Monte Carlo loop which accurately accounts for the effect of the device mismatch on circuit performance is used to calculate the yield of the present circuit design. Finally, the statistical optimizatoin loop alters the device areas or some of the device areas to achieve the target functional yield. The areas were changed using the steepest descent method [7, 9]. The principle of this method is to alter the device area which is most sensitive to the functional yield, thereby increasing the yield. A guess of each device area were inputed to this circuit optimizer initially. The area of the device which has the greatest value of: $\partial YIELD/\partial Area(i)$ will be changed to:

$$Area(i)_{new} = Area(i)_{initial} + \frac{\partial YIELD}{\partial Area(i)}(YIELD_{target} - YIELD_{initial}) \qquad (3.1)$$

This new device area along with the other unchanged device areas were inputed again to the circuit optimizer and the functional yield was recalculated. Repeating this technique, the target yield will be achieved while all the device sizes are determined.

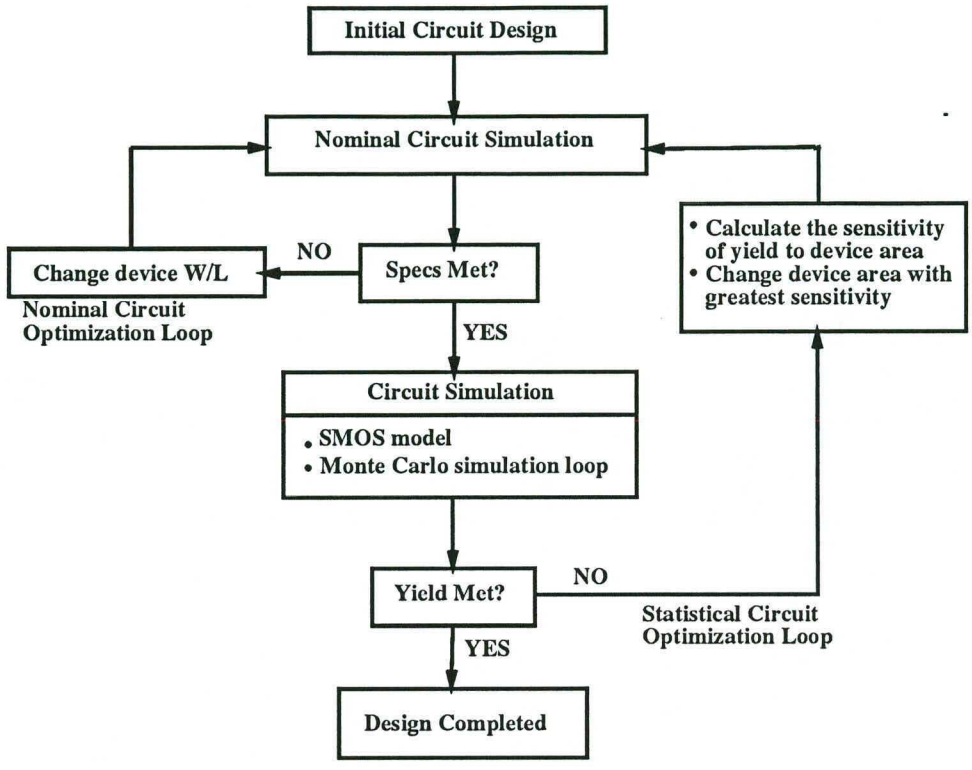

Figure 4: Flow chart of the statistical yield optimization with the steepest-descent method.

3.1.2 Computational Cost

A major problem faced by various approaches to statistical circuit design is the high computational cost or the simulation time. In order to achieve a high yield in the statistical circuit optimization, the affordable simulation time has to be considered. In our optimization procedure, the simulation time is mainly dependent on the time of each Monte Carlo loop. The output of the Monte Carlo loop is the yield of the circuit design. Therefore, the running time of each yield calculation is proportional to the number of Monte Carlo simulations. In the previous applications of the SMOS

model, the number of Monte Carlo simulations was chosen to be 1000. It is our purpose to reduce the number of Monte Carlo simulations to a certain value which will not affect the accuracy of the yield calculation.

The results of the functional yield mean and standard deviation vs. different number of Monte Carlo simulations for current mirror(referring to Figure 9) and Miller-compensated operational amplifier(referring to Figure 10) were shown in Table 5 or Figure 5 and Table 7 or Figure 7 respectively. The results of the running time of each yield calculation vs. different number of Monte Carlo simulations for those two circuit building blocks were shown in Table 6 or Figure 6 and Table 8 or Figure 8 respectively.

From these results, we have found that the running time of each yield calculation is proportional to the number of Monte Carlo simulations as we expected for both circuits. And the standard deviation of the yield does not increase dramatically while the number of Monte Carlo simulations changes from 1000 to 500. However the running time is reduced almost 50%. We will set the number of Monte Carlo simulations to 500 in our optimization.

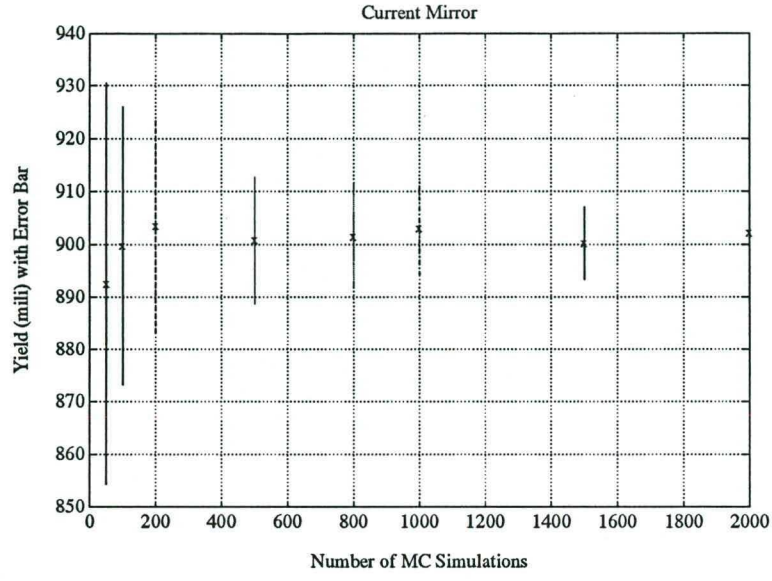

Figure 5: The results of functional yield mean and standard deviation vs. different number of Monte Carlo simulations for current mirror. It is based on the 50 yield calculations for each particular number of MC simulations.

3.2 Statistical Circuit Optimization Examples

3.2.1 Optimization Schemes

The developed optimization method will be examined on two basic analog circuits. They are the current mirror [15] which is shown in Figure 9 and the Miller-compensated operational amplifier [16] which is shown in Figure 10.

We have tried two different optimization schemes which differ from the defined transistor geometry. In the first optimization scheme, the transistor geometry is as following [7]:

$$W = (W/L) * (a) * (4\mu m) \tag{3.2}$$

$$L = (a) * (4\mu m) \tag{3.3}$$

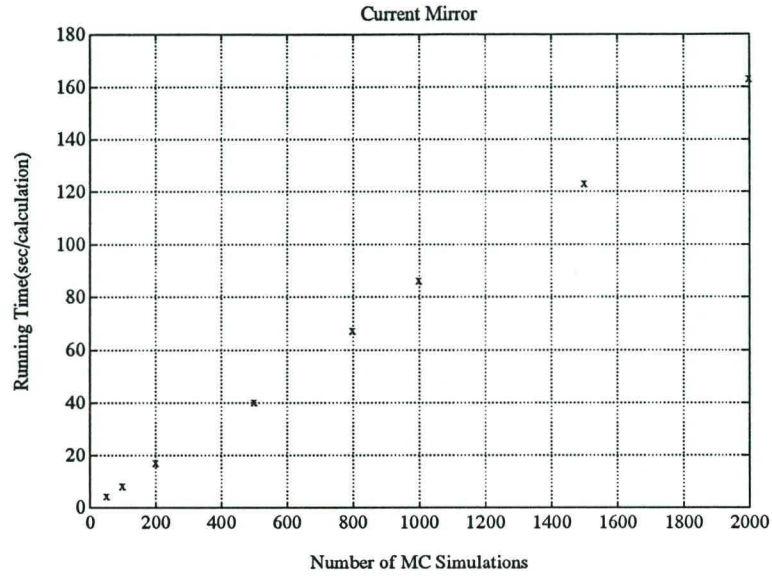

Figure 6: The results of running time of each yield calculation vs. different number of Monte Carlo simulations for current mirror.

and

$$Area = (W/L) * (a)^2 * (16\mu m^2) \tag{3.4}$$

where (W/L) and (a) are the aspect ratio and the area coefficient respectively. In the second(or improved) scheme, the transistor geometry has been redefined:

$$W = ((a) * (W/L))^{1/2} * (4\mu m) \tag{3.5}$$

$$L = ((a)/(W/L))^{1/2} * (4\mu m) \tag{3.6}$$

and

$$Area = (a) * (16\mu m^2) \tag{3.7}$$

where the (W/L) and (a) are the aspect ratio and the area coefficient respectively. Obviously, the area coefficient means differently from the previous definition. In both

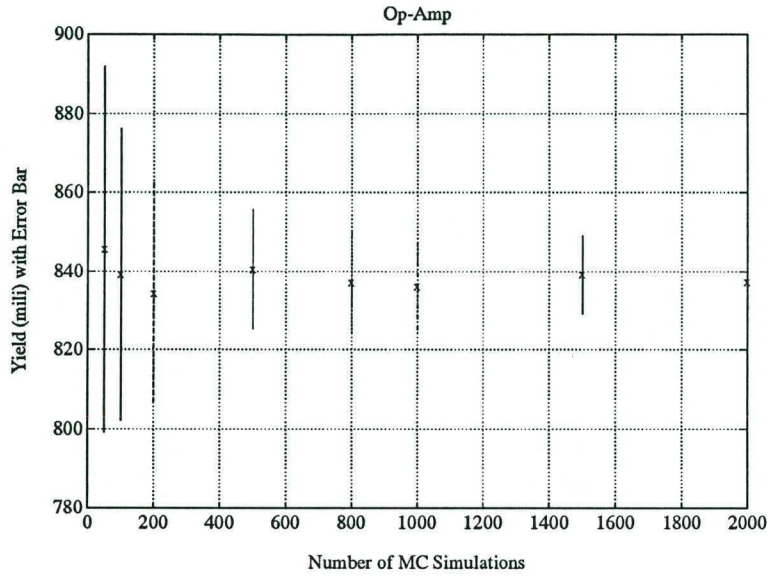

Figure 7: The results of functional yield mean and standard deviation vs. different number of Monte Carlo simulations for Miller-compensated operational amplifier. It is based on the 50 yield calculations for each particular number of MC simulations.

optimization schemes, the desired functional yield is set to 90%. A comparison of these two schemes will be discussed in the two circuits.

3.2.2 Current Mirror Optimization

Current mirror is one basic circuit building block which is universally employed to generate dc currents [15]. It consists of two enhancement MOSFETs, M_1 and M_2, having equal threshold voltage V_t, but different (W/L) ratios. Since M_1 is connected in parallel with M_2, they have the same V_{GS}, therefore:

$$I_O = I_{REF} * \frac{K_2}{K_1} \tag{3.8}$$

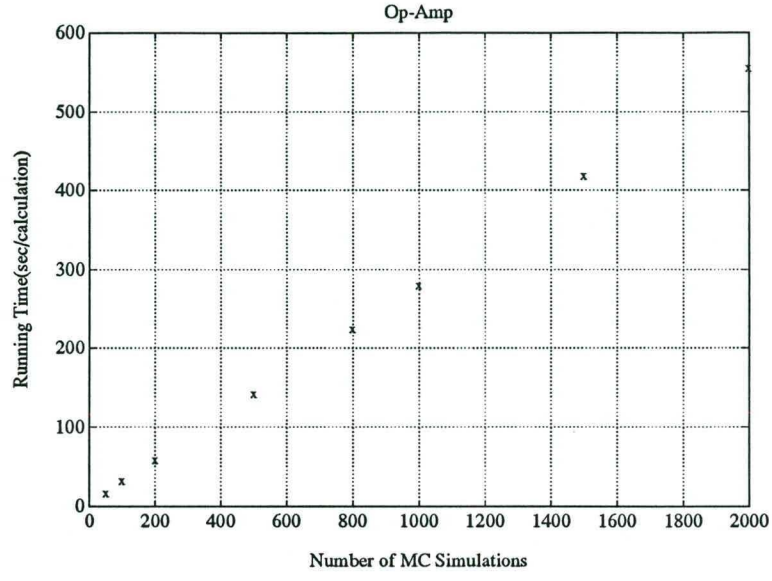

Figure 8: The results of running time of each yield calculation vs. different number of Monte Carlo simulations for Miller-compensated operational amplifier.

Expressing K_1 and K_2 in terms of the devices' (W/L) ratios gives :

$$I_O = I_{REF} * \frac{(W/L)_2}{(W/L)_1} \tag{3.9}$$

In our simulation, I_{REF} is chosen to be $10\mu A$ and the aspect ratios of two MOSFETs are $(W/L)_1 = 10$ and $(W/L)_2 = 5$ respectively. The nominal optimization or centering loop centers the I_O to $5.00 \pm 0.01\mu A$. The statistical optimization loop achieves the desired circuit yield for I_O to be within $5.0 \pm 0.1\mu A$. The statistical optimization results of two different schemes are listed in Table 9 which provides both the the optimized aspect ratios and area coefficients.

For the optimization results, the number of nominal optimization loop is less than 20, the number of Monte Carlo simulations was set to 500 as we discussed earlier,

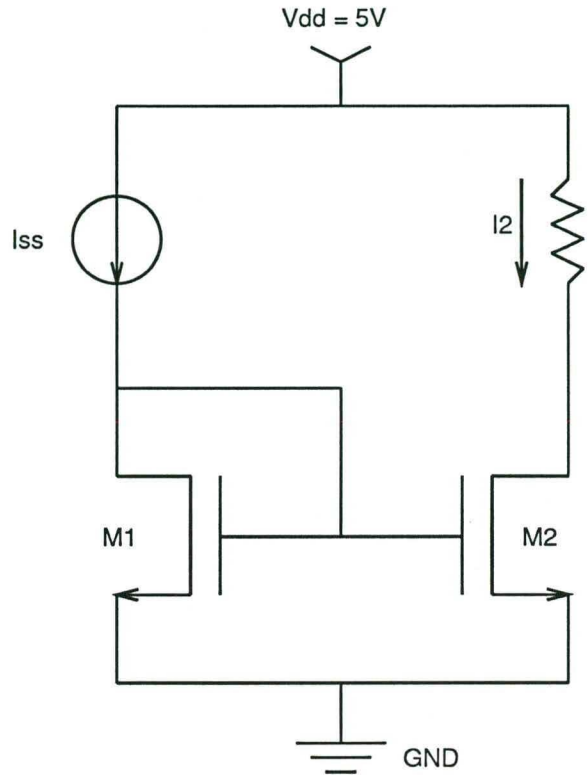

Figure 9: Current Mirror Circuit

and a typical number of statistical optimization loops was 5. All the device lengths are greater than $2\mu m$. With the second(or improved) optimization scheme, the total device area was greatly reduced to half of that of the first optimization scheme.

3.2.3 Operational Amplifier Optimization

Another example of statistical circuit optimization is performed on the basic, Miller-compensated operational amplifier [16]. In our simulations, a common-centroid layout for two transistor pairs, (M_1, M_2) and (M_3, M_4), was assumed. The device seperation distances were set to reasonable values based on the transistor geometry. The aspect

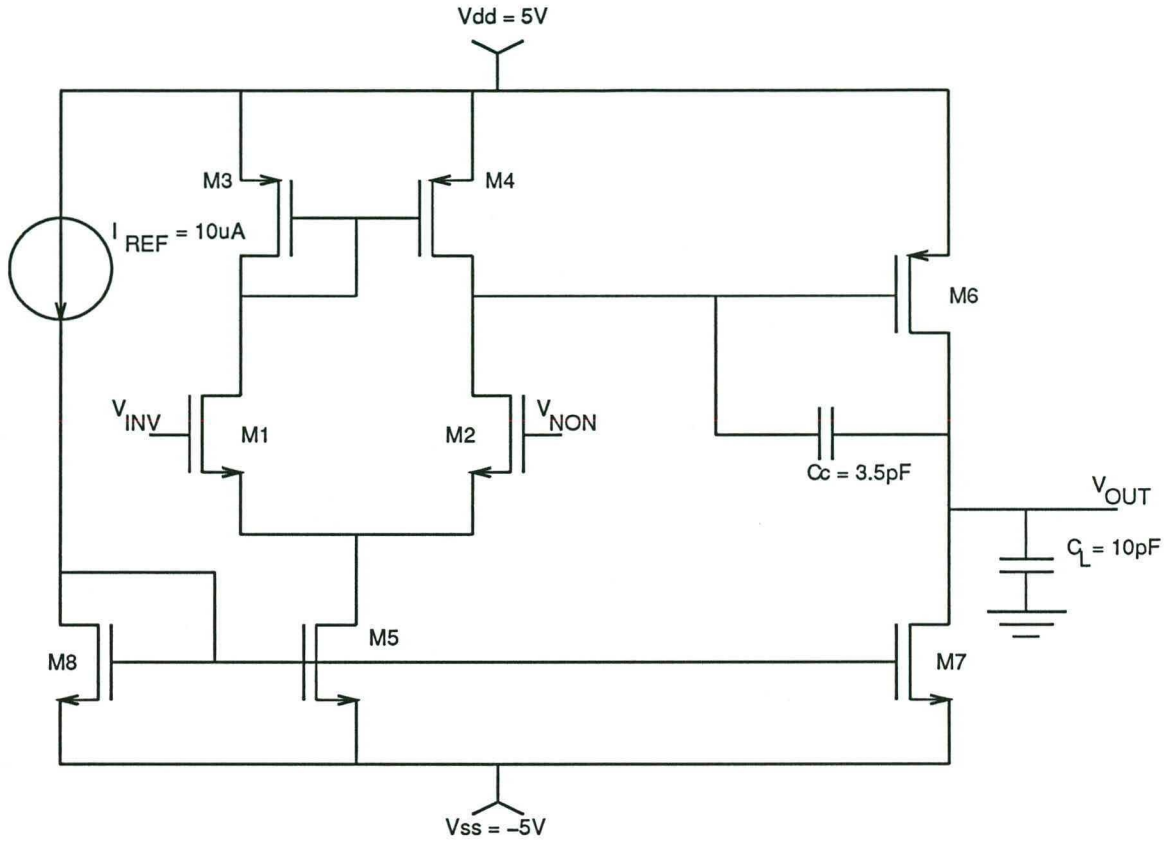

Figure 10: Miller Compensated Operational Amplifier Circuit

ratio of transistor M_8 was held constant at 2.

Six circuit performance criteria have been chosen for the nominal circuit optimization. In general, each performance criterion shows a decrease in standard deviation, i.e. an increase in functional yield, as the device area is increased. As an example, we simulated the yield as a funtion of two increased device areas with the design centering which is shown in Table 10. Previous research have shown, among the six performance criteria for this op-amp, only the offset voltage is sensitive to the device mismatch [2]. The standard deviations of the rest five performance criteria are neg-

ligibly small even for small transistor areas. Therefore, the offset voltage is the only performance criterion for which the device sizes have to be statistically optimized. Other performance criteria need only be centered to their desired values. The statistical circuit optimizations were then performed on four different offset voltage acceptability ranges. The results of both optimization schemes were provided in Table 11, Table 12 , Table 13 and Table 14. In general, the total device area decreases as the offset voltage tolerance increases. And also the total device area of the improved optimization scheme was greatly reduced in contrast to the first optimization scheme. However, for the improved optimization scheme, certain device lengths were less than $2\mu m$ which is restricted by the used fabrication process. In order to solve this problem, we noticed that in the length equation:

$$L = ((a)/(W/L))^{1/2} * (4\mu m) \tag{3.10}$$

By using simple algebra, we worked out that the ratio of (a) and (W/L) needed to be greater than 0.25 in order to keep the minimun value of the device lengh to be $2\mu m$. Therefore, an extra statistical optimization loop is needed for this modified area coefficient. Nevertheless, the total device area is still less than that of the first optimiztion scheme. For these optimizations, the number of the nominal optimization loops ranged from 10-60 and the typical number of statistical optimization loops was 30.

3.3 Conclusions

A CAD tool capable of performing statistical circuit optimization has been developed. In this tool, SMOS model which includes the effects of device geometry, circuit layout and transistor bias on the parameter variance was incorporated into the circuit simulator APLAC. With the use of the classic steepest-descent optimization method, the basic analog circuits, such as current mirror and Miller-compensated operational amplifier, are able to be optimized to meet the functional yield goals in an efficient, area-minimizing manner. The computational cost, or the simulation time, has also been investigated. It is a trade off of the desired accuracy.

However, with this tool, we were unable to find the optimum value of the total circuit area while optimizing the circuits to achieve the target yield. This goal will be achieved with the experimental design methodology [18, 19] which will be discussed in the next chapter.

Table 5: The results of functional yield mean and standard deviation vs . different number of Monte-Carlo simulations for current mirror. It is based on 50 yield calculations for each particular number of MC simulation. The area of each transistor is $320\mu m^2$ and $640\mu m^2$. The tolerence of output current is 0.1μA.

nsim	50	100	200	500	800	1000	1500	2000
Yield Mean (m)	892.40	899.60	903.40	900.68	901.40	902.90	900.17	902.10
Yield Stdev (m)	38.13	26.38	20.38	11.98	9.77	8.75	6.83	5.42

Table 6: The results of running time of each yield calculation vs. different number of Monte-Carlo simulations for current mirror. The area of each transistor is $320\mu m^2$ and $640\mu m^2$. The tolerence of output current is 0.1μA.

nsim	50	100	200	500	800	1000	1500	2000
CPU Time(sec)	4	8	17	40	67	86	123	163

Table 7: The results of functional yield mean and standard deviation vs . different number of Monte-Carlo simulations for Op-amp. It is based on 50 yield calculations for each particular number of MC simulation. The area of each transistor is $800\mu m^2$ and the tolerence of offset voltage is 2.0mv.

nsim	50	100	200	500	800	1000	1500	2000
Yield Mean (m)	845.60	839.20	834.30	840.48	836.97	836.06	839.17	837.13
Yield Stdev (m)	46.31	37.09	28.05	15.17	12.86	12.43	9.85	7.95

Table 8: The results of running time of each yield calculation vs. different number of Monte-Carlo simulations for Op-amp. The area of each transistor is $800\mu m^2$ and the tolerence of offset voltage is 2.0mv.

nsim	50	100	200	500	800	1000	1500	2000
CPU Time(sec)	15	31	58	141	223	279	418	564

Table 9: Current mirror statistical optimization results. Optimized values for output current, area coefficients, aspect ratios, device lengths and total areas for two different optimization schemes. The tolerance of the output current is 0.1μA and the functional yield is 90%.

Optimized Values		First Opt. Scheme	Improved Opt. Scheme
Output Current (μA)	I_O	5.0009	4.9944
Area Coefficients	a(1)	1.50	20.00
	a(2)	4.23	48.57
Aspect Ratios	W/L(1)	10.32	8.59
	W/L(2)	6.26	4.81
Transistor Lengths	L(1)(μm)	6.00	6.10
	L(2)(μm)	16.92	12.71
Total Areas (μm^2)		2164.12	1097.12

Table 10: The results of functional yield vs. two increased device areas with design centering of the Op-amp. The number of Monte-Carlo simulation is 500. The area of all the other transistor is $160\mu m^2$ and the tolerence of offset voltage is 2.0mv.

Yield (mili)	136	306	546	758	808	854
Area[1,2] (μm^2)	160	240	320	400	480	560

Table 11: Op-amp statistical optimization results. Optimized values for circuit performance, area coefficients, aspect ratios, device lengths and total areas for two different optimization schemes. The offset voltage tolerance is 1.5mv and the functional yield is 90%.

Optimized Values		First Optimization Scheme	Improved Opt. Scheme	
			Original Results	Final Results
Circuit Performance	Gain-BW (MHz)	5.03	5.12	5.16
	Slew Rate (V/μs)	15.5	5.20	7.01
	Gain Margin (dB)	27.2	23.2	21.7
	Phase Margin (deg)	55.1	65.2	67.5
	DC Gain (dB)	71.8	82.3	75.0
Area Coefficients	a(1,2)	1.75	80.34	80.34
	a(3,4)	5.50	16.74	16.74
	a(5)	1.00	10.00	10.00
	a(6)	1.00	10.00	94.00**
	a(7)	1.00	10.00	10.00
	a(8)	1.00	10.00	10.00
Aspect Ratios	W/L(1,2)	28.75	61.75	24.71
	W/L(3,4)	3.25	3.49	6.87
	W/L(5)	6.25	2.39	3.09
	W/L(6)	273.50	373.39	364.81
	W/L(7)	208.00	34.04	34.89
	W/L(8)	2.00	2.00	2.00
Transistor Lengths	L(1,2)(μm)	7.00	4.56	7.21
	L(3,4)(μm)	22.00	8.76	6.24
	L(5)(μm)	4.00	8.18	7.20
	L(6)(μm)	4.00	0.66 *	2.03
	L(7)(μm)	4.00	2.17	2.14
	L(8)(μm)	4.00	8.94	8.94
Total Areas (μm^2)		13799.52	3746.66	5090.66

*: device length is less than 2μm.

**: modified area coefficient.

Table 12: Op-amp statistical optimization results. Optimized values for circuit performance, area coefficients, aspect ratios, device lengths and total areas for two different optimization schemes. The offset voltage tolerance is 2.0mv and the functional yield is 90%.

Optimized Values		First Optimization Scheme	Improved Opt. Scheme	
			Original Results	Final Results
Circuit Performance	Gain-BW (MHz)	5.08	5.23	5.02
	Slew Rate (V/μs)	11.1	5.18	8.41
	Gain Margin (dB)	24.3	22.4	20.2
	Phase Margin (deg)	55.4	73.7	71.1
	DC Gain (dB)	70.8	76.6	70.2
Area Coefficients	a(1,2)	2.00	39.85	39.85
	a(3,4)	4.00	10.00	10.00
	a(5)	1.00	10.00	10.00
	a(6)	1.00	10.00	83.00**
	a(7)	1.00	10.00	10.00
	a(8)	1.00	19.84	19.84
Aspect Ratios	W/L(1,2)	32.00	41.47	15.38
	W/L(3,4)	1.00	12.10	11.67
	W/L(5)	4.50	2.30	2.98
	W/L(6)	126.25	352.90	261.35
	W/L(7)	207.00	39.53	21.54
	W/L(8)	2.00	2.00	2.00
Transistor Lengths	L(1,2)(μm)	8.00	3.92	6.44
	L(3,4)(μm)	16.00	3.64	3.70
	L(5)(μm)	4.00	8.34	7.33
	L(6)(μm)	4.00	0.67 *	2.25
	L(7)(μm)	4.00	2.01	2.73
	L(8)(μm)	4.00	12.60	12.60
Total Areas (μm^2)		10048.00	2392.64	3560.64

*: device length is less than 2μm.

**: modified area coefficient.

Table 13: Op-amp statistical optimization results. Optimized values for circuit performance, area coefficients, aspect ratios, device lengths and total areas for two different optimization schemes. The offset voltage tolerance is 2.5mv and the functional yield is 90%.

Optimized Values		First Optimization Scheme	Improved Opt. Scheme	
			Original Results	Final Results
Circuit Performance	Gain-BW (MHz)	5.12	5.17	4.99
	Slew Rate (V/μs)	10.1	5.77	8.82
	Gain Margin (dB)	24.6	22.6	19.9
	Phase Margin (deg)	59.0	73.0	70.0
	DC Gain (dB)	73.1	72.2	69.9
Area Coefficients	a(1,2)	1.50	36.14	36.14
	a(3,4)	2.75	10.00	10.00
	a(5)	1.00	10.00	10.00
	a(6)	1.00	10.00	72.00**
	a(7)	1.00	10.00	11.00**
	a(8)	1.00	16.82	16.82
Aspect Ratios	W/L(1,2)	22.00	31.49	13.74
	W/L(3,4)	3.00	8.24	8.29
	W/L(5)	4.00	2.54	3.15
	W/L(6)	204.00	285.88	257.93
	W/L(7)	134.50	42.33	19.29
	W/L(8)	2.00	2.00	2.00
Transistor Lengths	L(1,2)(μm)	6.00	4.28	6.49
	L(3,4)(μm)	11.00	4.41	4.39
	L(5)(μm)	4.00	7.39	7.13
	L(6)(μm)	4.00	0.75 *	2.11
	L(7)(μm)	4.00	1.94 *	3.02
	L(8)(μm)	4.00	11.60	11.60
Total Areas (μm^2)		7821.76	2225.60	3233.60

*: device length is less than 2μm.

**: modified area coefficient.

Table 14: Op-amp statistical optimization results. Optimized values for circuit performance, area coefficients, aspect ratios, device lengths and total areas for two different optimization schemes. The offset voltage tolerance is 3.0mv and the functional yield is 90%.

Optimized Values		First Optimization Scheme	Improved Opt. Scheme	
			Original Results	Final Results
Circuit Performance	Gain-BW (MHz)	5.16	5.25	4.98
	Slew Rate (V/μs)	11.5	5.27	8.67
	Gain Margin (dB)	22.8	22.5	19.8
	Phase Margin (deg)	58.6	71.9	70.1
	DC Gain (dB)	72.2	76.5	69.8
Area Coefficients	a(1,2)	1.00	30.64	30.64
	a(3,4)	2.25	10.00	10.00
	a(5)	1.00	13.65	13.65
	a(6)	1.00	10.00	73.00**
	a(7)	1.00	10.00	11.00
	a(8)	1.00	10.00	10.00
Aspect Ratios	W/L(1,2)	13.75	39.91	13.84
	W/L(3,4)	5.50	7.04	9.26
	W/L(5)	4.75	2.45	3.33
	W/L(6)	247.25	290.96	255.34
	W/L(7)	91.00	43.22	19.58
	W/L(8)	2.00	2.00	2.00
Transistor Lengths	L(1,2)(μm)	4.00	3.50	5.95
	L(3,4)(μm)	9.00	4.77	4.16
	L(5)(μm)	4.00	9.45	8.10
	L(6)(μm)	4.00	0.74 *	2.14
	L(7)(μm)	4.00	1.92 *	3.00
	L(8)(μm)	4.00	8.94	8.94
Total Areas (μm^2)		6850.88	1998.88	3022.88

*: device length is less than 2μm.

**: modified area coefficient.

CHAPTER IV

Statistical Circuit Optimization: Experiment Design Method

4.1 Introduction

Experiments are carried out by investigators in all fields of study either to discover something about a particular process or to compare the effect of several factors on some phonomena. The three basic principles of experimental design are replication, randomization, and blocking [20, 21]. By replication, we mean a repetition of the basic experiment. This allows the experimenter to obtain an estimate of the experimental error. Randomization is the cornerstone underlying the use of statistical methods in the experiment design. This implies that both the allocation of the experiment material and the order in which the individual runs or trials of the experiment are to be performed are randomly determined. Blocking involves making comparisons among the conditions of interest in the experiment within each block.

4.1.1 Role of Experiment Design

If an experiment is to be performed most efficiently, then the scientific approach to planning the experiment must be employed. To use the statistical approach in designing and analyzing an experiment, the following three tasks have to be performed

in an organized manner: to decide the objective of research, to consider the method by which to achieve the objective, and to evaluate the method [21, 18, 20]. The suggested procedure is shown in the flow chart of Figure 11. A clear statement of the problem often contributes substantially to a better understanding of the phenomena and the final solution of the problem. The experimenter must select the independent variables or factors to be investegated in the experiment. And also the ranges over which these factors are to be varied and the number of levels at which runs are to be made. In choosing a response or dependent variable, it has to be certain that the response to be measured really provides information about the problem under study. The choice of experimental design is of primary importance in the whole procedure. The experimenter should determine the order in which the data will be collected and the method of randomization to be employed. It is always necessary to maintain a balance between the statistical accuracy and cost. Once the design method is selected, the experimenter should carefully monitor the progress of the experiment to ensure that it is proceeding according to the plan. Statistical methods should be employed in analyzing the data from the experiment. In recent years the computer has played a ever-increasing role in the data analysis. Graphical techniques are particular helpful in data analysis. The conclusions about the results will be drawn after the data has been analyzed and the recommendations which may include a further round experiment will be made as well.

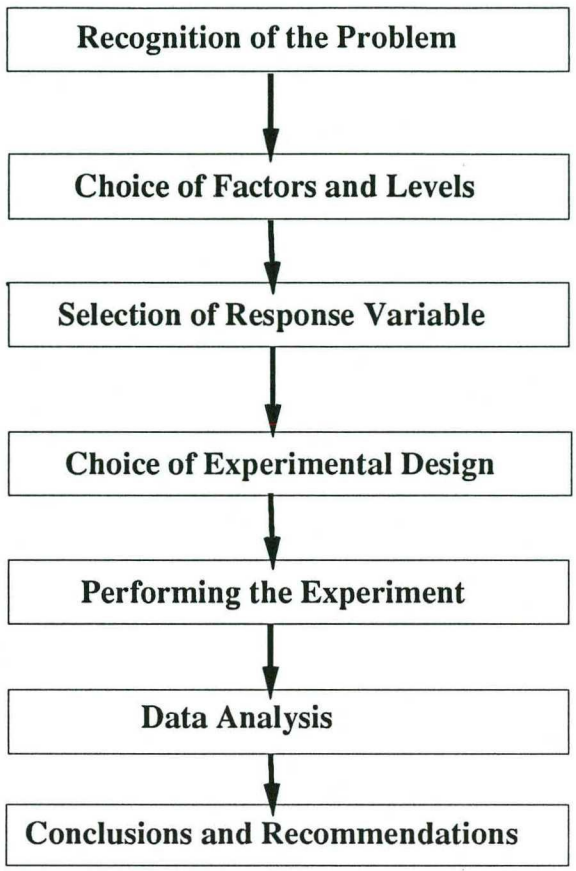

Figure 11: Flow chart of the experiment design

4.1.2 Areas of Application of Experiment Design

The experiment design method has been widely used in the engineering and industrial research. The major applications come from the following three areas [21, 18, 19, 20]:

- The functional relationship $y = f(A, B, ...)$ is known. This is a problem that often appears in design calculations and planning calculations. For example, in seeking to determine how one should choose the circuit constants such as L, C, and R in a circuit design so that the output y will become a target value.

When variables such as circuit constants are numerous, calculation for every combination is difficult, and calculations at a few values of A, B, ... that are selected by using the orthogonal arrays becomes very useful.

- In the functional relationship $y = f(A, B, ...)$, the functional form f is unclear or not well understood in a certain range of the factors, A, B, ... In this case, we decide the levels for the variables in the range we wish to study and express the functional relationship by equations and graphs obtained by experiments.

- Although expectations and assumptions exit about the form of the function $y = f(A, B, ...)$, it contains parameters and one wishes to estimate them. We have to create the theoretical equations and formulars that well express relationship in this type of problem.

4.2 Optimization Methodology

4.2.1 Experiment Design Method

As an application of the experiment design in the statistical circuit optimization, we would like to find the optimal device areas in order to achieve a target functional circuit yield which is obviously the objective of our research. Using this statistical technique, the effects on circuit performance of individual circuit components in the circuit can be seperated. It also provides a more accurate estimation of the circuit performance variance simultaneously and requires a much smaller number of circuit simulations.

Among all different experimental design methods, such as combination design,

Latin square design, orthogonal array design and factorial design etc., the orthogonal array is selected to accomplish the objective of our research. The orthogonal arrays were originally used for expressing functions and assigning experiments. It was then improved by Dr. Taguchi [18, 19] to optimize the design of products and production process in a cost-effective manner representing one of the major advances in the history of manufacturing industries. His use of orthogonal arrays enables a rapid search through millions of design options to find the design that is furthest away from all potential problems.

4.2.2 Orthogonal Arrays

Table 15 shows a typical orthogonal distribution array L_8 (2^7)or simple orthogonal array L_8 [18]. The number of each row is called the experiment number or assignment number, and it runs from 1 to 8. The vertical alignments are termed the columns of the orthogonal array, and every column consists four each of the numerals 1 and 2. Since the combinations of the numerals of any column and those of any other column are made up of the numerals 1 and 2, there are four possible combinations. When each of two columns consists of the numerals 1 and 2 and the four combinations (1, 1), (1, 2), (2, 1), and (2, 2) appear with the same frequency, we say that these two columns are balanced, or orthogonal. In this example, the number of factors is seven and each factor has two levels representing by 1 and 2 respectively. Normally, the choice of factors and levels should be decided by the experimenter before the assignment of the orthogonal array table.

As a comparison with other experiment design methods, Table 16 lists the assign-

ment by combination design [18]. When the experiment is performed, we get by with changing only the level of one factor in each run of the experiment. In this method, when comparing the two levels of any one factor, the other factors were all fixed at a specific level. Usually, the difference between the two levels is obtained with very good precision if the experiment is done this way. But in comparing the two levels by an assignment that will yield the average effect (so-called the main effect) of these two levels with varied combinations of levels of the other factors are very importnant. In finding the effects of the two levels, by an orthogonal array, we compare the mean of the data from four runs of the experiment. Although the precision of each experimental run may be poor, the comparison of the mean of data of four runs each time which the precision is not necessarily as bad as the comparison of two levels only. On the other hand, the difference effect estimated in the combination design is correct for the case when the other factors are at their fixed levels, there is no guarantee that the effect will exist consistently if other factor conditions change. Specifically, we are really seeking the averaged effect when the levels of the factors are varied.

The other commonly used experiment design method is factorial design [20, 22, 23]. In this method, all possible combinations of the levels of the factors are investigated in each complete trial or replication of the experiment. One of the advantages of the factorial design is that interactions between the factors is taken into account which will avoid the misleading of the conclusions. But the cost of the experiment is more expensive, the number of running the experiment is much higher than that of the orthogonal design. Use the same example as we discussed earlier, for a seven factors with each has two levels, the numnber of runs (or assignments) is 2^7 (128). Even with

the so-called fractional factorial design [20, 21] in which the high order interactions are negligible and the information on main effects and the low order interactions may obtained by running only a fraction of the complete factorail design, the cost of the experiment is still expensive. On the other hand, the interactions of the factors will be cancelled when we perform the experiments on the main effects in the orthogonal array design. It is with the aforementioned goal, a balance between the statistical accuracy and cost, the orthogonal array design has been selected.

4.3 Statistical Circuit Optimization Example

4.3.1 Operational Amplifier Optimizaion

As an example of the statistical circuit optimization with the experiment design method, the Miller compensated operational amplifier [16] which has been used in the previous chapter will be examined. Figure 12 is the flow chart of the optimization algorithm. The offset voltage which is primarily sensitive to the device parameter mismatch [7] is the performance criterion for which the device sizes have to be statistically optimized. The other nominal specifications such as open loop gain, phase margin etc. must be met within the nominal optimization loop by adjusting the device W/L ratios. Therefore the device areas are the input variables for each yield calculation. Based on the results from the previous chapter, the ranges of the tansistor areas except for $A[4]$ will be from 10 to 50 and the range of $A[4]$ is between 50 and 90. Each area factor has five levels with the equal interval 10. The actual orthogonal array assignments and yield results are shown in Table 3.

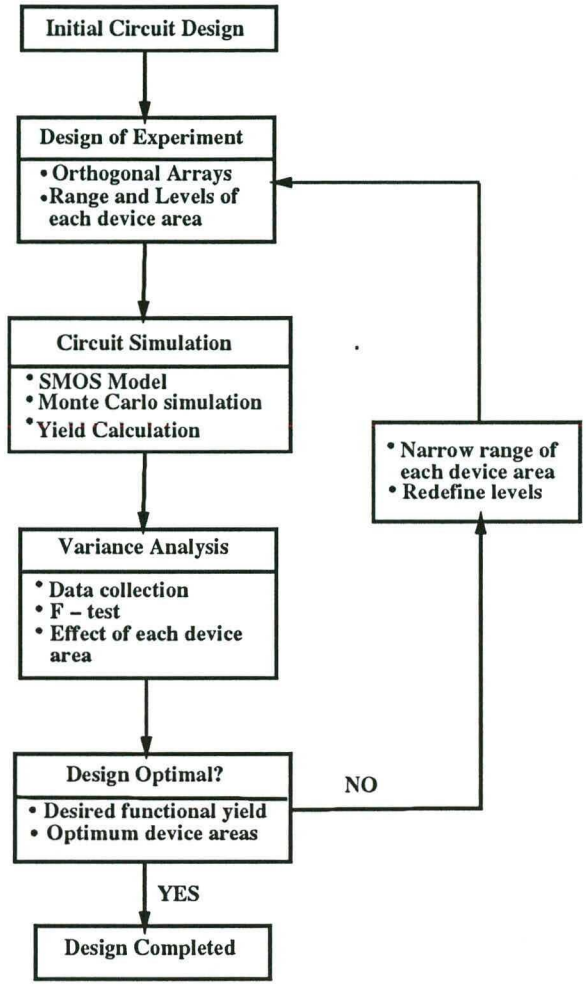

Figure 12: Flow chart of the statistical yield optimization with experiment design method.

4.3.2 Statistical variance analysis

Before the statistical variance analysis, we would like to introduce the following terminologies [24, 18, 19]:

$$d.f. = degrees\ of\ freedom \tag{4.1}$$

which is normally equal to the number of pieces of information minus one. (To understand this terminology, let us look sample variances of n pieces of information. The number of sample variances is n in this case, but they are not independent since the sum must be zero. Hence, if we know any $(n-1)$ of them, we can calculate the other one from the first $(n-1)$. The independent $(n-1)$ are called the degrees of freedom.) and

$$T = Total\ Sum\ of\ Yield \tag{4.2}$$

and

$$CF = Correlation\ Factor = \frac{(T)^2}{Number\ of\ Observations} \tag{4.3}$$

and

$$SS_T = Total\ Sum\ of\ Squares(of\ Each\ Observation) - CF \tag{4.4}$$

and

$$SS_{A_i} = \frac{Sum\ of\ Squares\ of\ A'_{ij}s}{No.\ of\ Observations\ of\ Each\ Level} - CF \tag{4.5}$$

where,

$$A_{ij} = Value\ in\ Supplementary\ Table\ for\ Level\ j\ of\ A_i,\ \ j = 1...5;\ \ i = 1...6; \tag{4.6}$$

and

$$SS_e = SS_T - SS_{A_1} - SS_{A_2} - SS_{A_3} - SS_{A_4} - SS_{A_5} \tag{4.7}$$

From the experimental yield results, we calculated the above mentioned statistical variances which are listed in the supplementary Table 18 and the ANOVA (ANalysis Of VAriance) Table 4.In the supplementary Table 18, the effect of each area factor at each level A_{ij} to the yield has been estimated. Obviously, the sum of the effect of

all five levels should be equal for each area factor. And the value R is the difference between the greatest effect and the least effect of each area factor.

The significance of the effect of each area factor will be determined by performing a hypothesis test [24, 25, 26]. F - test which is based on the F - distribution (the probability density function (p.d.f) is F distribution) has been widely used in the statistical analysis. Basically, it is a ratio of two χ^2 distribution divided by its degrees of freedom respectively. In our experiment, we assumed that both yield and its variation obey the normal distribution. Therefore, the SS values obey the χ^2 distribution. Usually, the statistic or the ratio of F - test indicates the sources of variations. The denominator often stands for the variation in the experimental yield caused by the randomization (or noise) of the experiment and the numerator is the variation caused by the deviation of the factors we want to test. Intuitively, if this ratio is large, it means that the variation associated with the specific factor is much larger than that of the randomization. We would conclude that this testing factor has an significant effect on the experimental yield, or at least it is more important than the pure randomization. Otherwise, if the ratio is small, we would say it is not so important to the yield since its impact is no more than that of the noise. This ratio, the statistic, obeys the $F(a, b)$ distribution with a and b are the degrees of freedom of the numerator and denominator respectively. When we actually perform the F - test, two other important statistical terminologies which are "p - value" and "at d% level" have to be introduced [24, 26]. The p - value of a positive number A is the cumulative density function (c.d.f) of $F(a, b)$ at A and it can be illustrated as the

following integral:

$$p = \int_{-\infty}^{A} F(a,b)dx \tag{4.8}$$

The experiment is normally tested "at $d\%$ level". This means that we choose a number K and the p - value associated with this number K is $1-d\%$. The significance of each factor will then be evaluated by comparing the corresponding ratio to the number K. If the ratio is larger, then the factor is significant and vice versa. The smaller the $d\%$ level is, the more accurate the evaluation is. Once the $d\%$ level has been selected, the number K can be found from the statistical table [24]. In our experiment, we noticed that the error terms for both the degrees of freedom and the SS value were zero. Therefore, we take the average of the two smallest SS's to be the denominator for the F - test and the testing distribution function is: $F(4,4)$. The p -values of all the area factors are calculated by using SAS (Statistical Analysis Software) and are listed in the ANOVA Table I. It is then obvious that $A[1]$ and $A[5]$ are more significant. This is also consistent with the results from the supplementary table in which both $A[1]$ and $A[5]$ have a relative wide variation to yield within the selected range. In another word, the ranges should be narrowed in order to find more optimal design. And also there is only one observation with the yield greater than 85%. We conclude that the second round experiment is necessary.

The results from the supplementary table have been plotted in Figure 13, 14, 15, 16, 17 and 18. From these figures, we can briefly determine the trend of the effect of different area factors. The new ranges (referring to Table 20) of the area factors will be selected around the peaks which associated with relative small areas. In order to preserve the randomization, the order of the assignment has been rearranged. The

experimental yield of the second round experiment are shown in Table 21.

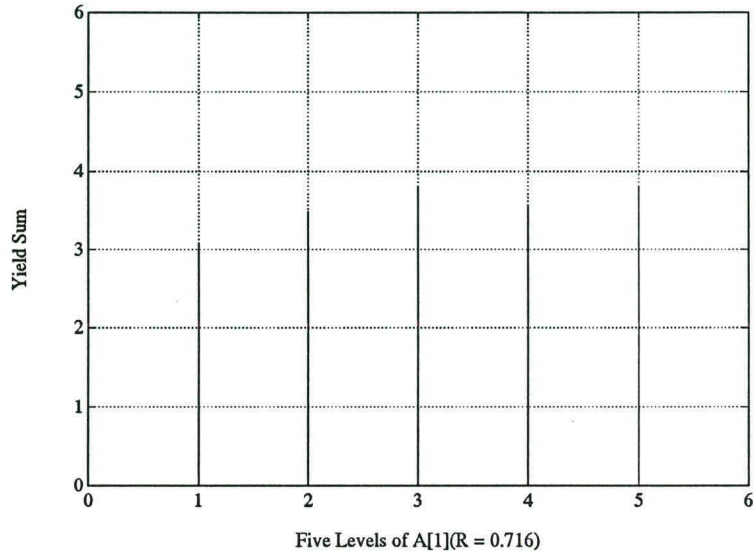

Figure 13: Estimation of the effect of the device area A[1] of the first run experiment.

Apparently, the second round experiment is improved since all the yield results are high and quite close to the target functional yield except for a very few cases. Similar to the variance analysis performed for the first round experiment, we listed all the statistical terms in the supplementary Table 22 as well as the ANOVA Table 23. The greatest p - value is 0.72. Statistically speaking, no factor is significant even at 20% level. It is not necessary to perform the further experiment since the design is already optimal. From the five observations which have the yield more than 85%, we can determine the combination with the minimum total area of the circuit. The optimal total device area is $3808\mu m^2$ and it is comparable to what we got from the other optimization algorithm.

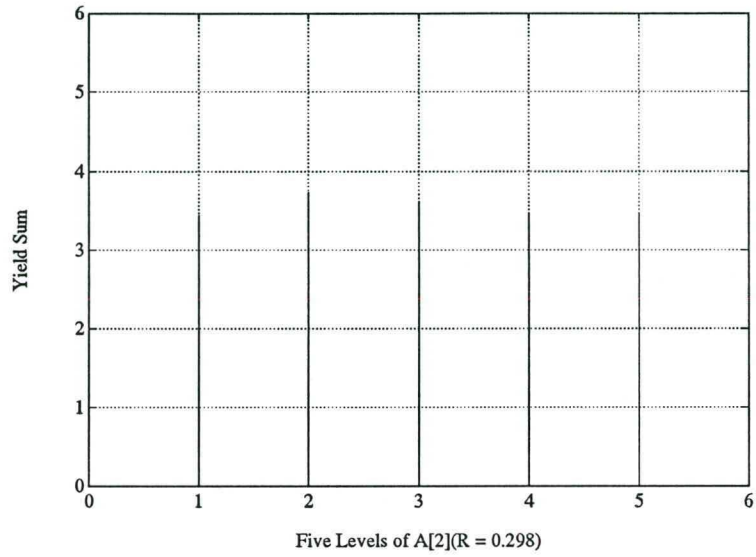

Figure 14: Estimation of the effect of the device area A[2] of the first run experiment.

Table 15: Orthogonal Array L_8

Col. ⇒ No. ⇓	1	2	3	4	5	6	7
1	1	1	1	1	1	1	1
2	1	1	1	2	2	2	2
3	1	2	2	1	1	2	2
4	1	2	2	2	2	1	1
5	2	1	2	1	2	1	2
6	2	1	2	2	1	2	1
7	2	2	1	1	2	2	1
8	2	2	1	2	1	1	2

Table 16: Example of Assignment by Combination Design

Factor ⇒ No. ⇓	1	2	3	4	5	6	7
1	1	1	1	1	1	1	1
2	2	1	1	1	1	1	1
3	2	2	1	1	1	1	1
4	2	2	2	1	1	1	1
5	2	2	2	2	1	1	1
6	2	2	2	2	2	1	1
7	2	2	2	2	2	2	1
8	2	2	2	2	2	2	2

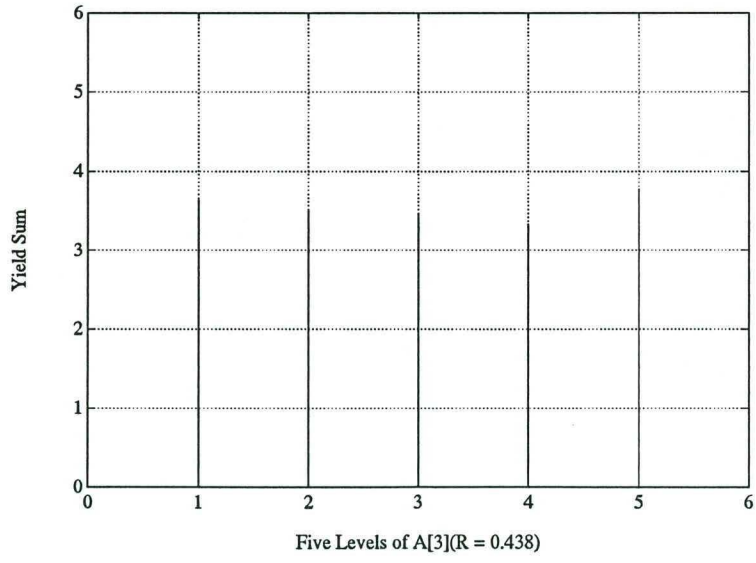

Figure 15: Estimation of the effect of the device area A[3] of the first run experiment.

Table 17: Actual assignment and experiment data of first run experiment.

Factor ⇒	Device Areas						Yield
No. ⇓	A[1]	A[2]	A[3]	A[4]	A[5]	A[6]	%
1	1	1	1	1	1	1	54.4
2	1	2	2	2	2	2	58.0
3	1	3	3	3	3	3	64.8
4	1	4	4	4	4	4	61.0
5	1	5	5	5	5	5	70.6
6	2	1	2	3	4	5	70.0
7	2	2	3	4	5	1	75.8
8	2	3	4	5	1	2	61.2
9	2	4	5	1	2	3	69.2
10	2	5	1	2	3	4	72.8
11	3	1	3	5	2	4	74.8
12	3	2	4	1	3	5	78.4
13	3	3	5	2	4	1	81.4
14	3	4	1	3	5	2	81.0
15	3	5	2	4	1	3	64.2
16	4	1	4	2	5	3	64.0
17	4	2	5	3	1	4	75.8
18	4	3	1	4	2	5	70.6
19	4	4	2	5	3	1	75.0
20	4	5	3	1	4	2	70.4
21	5	1	5	4	3	2	80.4
22	5	2	1	5	4	3	85.4
23	5	3	2	1	5	4	84.4
24	5	4	3	2	1	5	61.2
25	5	5	4	3	2	1	69.0

Table 18: Supplementary Table I. Estimation of effects of the first run experiment.

Levels ⇒	Yield Sum					T	R =
Factors ⇓	level1	level2	level3	level4	level5		Max-Min
A[1]	3.088	3.490	3.798	3.558	3.804	17.738	0.716
A[2]	3.436	3.734	3.624	3.474	3.470	17.738	0.298
A[3]	3.642	3.516	3.470	3.336	3.774	17.738	0.438
A[4]	3.568	3.374	3.606	3.520	3.670	17.738	0.296
A[5]	3.168	3.416	3.714	3.682	3.758	17.738	0.590
A[6]	3.556	3.510	3.476	3.688	3.506	17.738	0.212

Table 19: ANOVA Table I. Analysis of variance of the first run experiment.

Source	d.f.	SS	Ratio	P-value
A[1]	4	0.0686	8.85	0.97
A[2]	4	0.0129	1.66	0.68
A[3]	4	0.0224	2.88	0.84
A[4]	4	0.0099		
A[5]	4	0.0503	6.49	0.95
A[6]	4	0.0056		
error	0	0		
Total	24	0.1697		

Table 20: Levels of the area factors of the second run experiment.

	level1	level2	level3	level4	level5
A[1]	32	36	40	44	48
A[2]	28	24	20	16	12
A[3]	10	10	10	10	10
A[4]	88	84	80	76	72
A[5]	50	40	30	20	10
A[6]	20	17.5	15	12.5	10

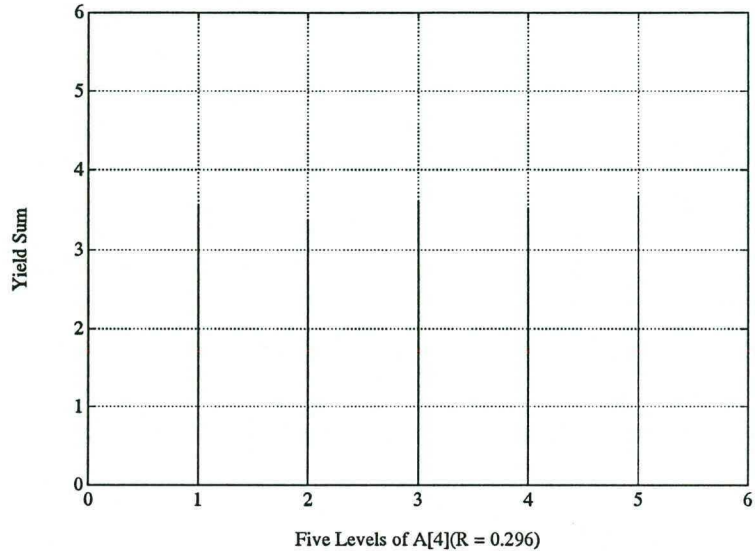

Figure 16: Estimation of the effect of the device area A[4] of the first run experiment.

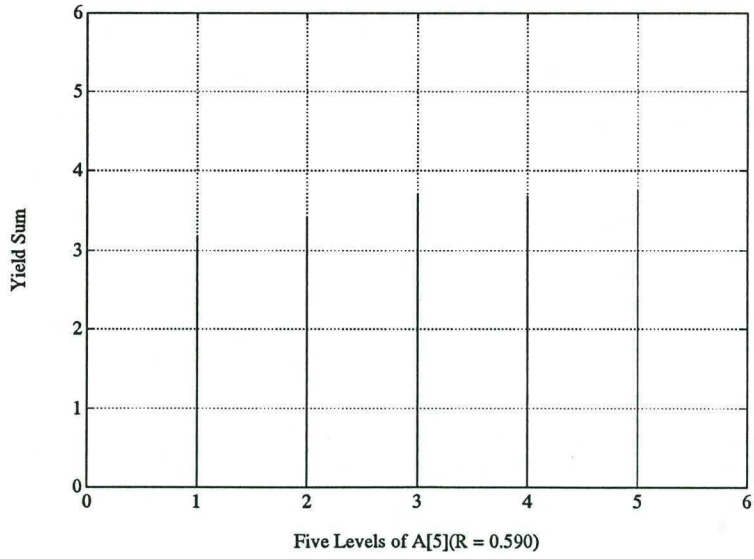

Figure 17: Estimation of the effect of the device area A[5] of the first run experiment.

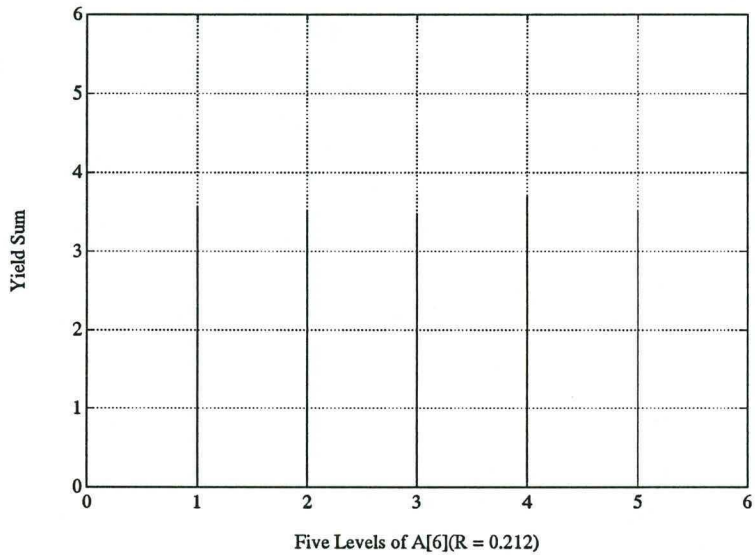

Figure 18: Estimation of the effect of the device area A[6] of the first run experiment.

Table 21: Actual assignment and experiment data of second run experiment.

Factor ⇒	Device Areas						Yield
No. ⇓	A[2]	A[6]	A[5]	A[3]	A[1]	A[4]	%
1	1	1	1	1	1	1	88.0
2	1	2	2	2	2	2	80.4
3	1	3	3	3	3	3	86.6
4	1	4	4	4	4	4	73.8
5	1	5	5	5	5	5	80.0
6	2	1	2	3	4	5	84.0
7	2	2	3	4	5	1	88.0
8	2	3	4	5	1	2	66.2
9	2	4	5	1	2	3	76.6
10	2	5	1	2	3	4	82.6
11	3	1	3	5	2	4	86.4
12	3	2	4	1	3	5	78.0
13	3	3	5	2	4	1	79.8
14	3	4	1	3	5	2	85.0
15	3	5	2	4	1	3	81.0
16	4	1	4	2	5	3	84.2
17	4	2	5	3	1	4	70.0
18	4	3	1	4	2	5	79.4
19	4	4	2	5	3	1	79.8
20	4	5	3	1	4	2	83.6
21	5	1	5	4	3	2	80.0
22	5	2	1	5	4	3	66.4
23	5	3	2	1	5	4	81.2
24	5	4	3	2	1	5	78.8
25	5	5	4	3	2	1	80.4

Table 22: Supplementary Table II. Estimation of effects of the second run experiment.

Levels ⇒	Yield Sum					T	R =
Factors ⇓	level1	level2	level3	level4	level5		Max-Min
A[1]	3.840	4.032	4.070	3.876	4.182	20.000	0.342
A[2]	4.088	3.974	4.102	3.968	3.868	20.000	0.234
A[3]	4.074	4.056	4.060	4.022	3.788	20.000	0.286
A[4]	4.160	3.952	3.946	3.940	4.002	20.000	0.220
A[5]	4.014	4.064	4.234	3.824	3.864	20.000	0.410
A[6]	4.224	3.828	3.932	3.940	4.076	20.000	0.396

Table 23: ANOVA Table II. Analysis of variance of the second run experiment.

Source	d.f.	SS	Ratio	P-value
A[1]	4	0.0162	1.38	0.62
A[2]	4	0.0074	0.63	0.33
A[3]				
A[4]	4	0.0068	0.58	0.31
A[5]	4	0.0216	1.85	0.72
A[6]	4	0.0189	1.62	0.68
error	4	0.0116		
Total	24	0.0825		

CHAPTER V

Summary and Future Work

5.1 Summary

With the implementation of the SMOS model in the APLAC simulator, it enables the user to do a variety of statistical circuit analysis, especially the statistical circuit optimization. One of the major applications of the SMOS model is to aid in the optimal design of analog CMOS circuits. APLAC contains optimization routines capable of performing the nominal circuit optimizations and it provides the optimizor a very flexible CAD environment.

In this thesis, we have investigated two different optimization algorithms, which are the conventional steepest - descent method and the experimental design method. The nuclei of these statistical optimization algorithms are the SMOS model and the APLAC simulator. All the random process variations are generated and characterized by Monte Carlo simulations. Therefore, the number of Monte Carlo simulations plays a important role in the computational cost. Previous work used 1000 Monte Carlo simulations for each yield calculation. With our investigation, we improved it to 500 Monte Carlo simulations. The computational cost has been reduced to one half without affecting the accuracy of the yield calculation.

The principle of the steepest -descent method is to alter the device area which

is most sensitive to the functional yield, thereby increasing the yield. A nominal circuit optimization is also included for each yield calculation in order to achieve all the nominal circuit specifications. With this method, we are able to optimize the circuit to meet the yield goal in a fairly efficient manner. However, there are two main disadvantages of this method. First, it is difficult to determine the optimal (or minimum) value of the total device area while optimizing the circuit. Thus, while the circuit meets the functional yield requirements in a fairly efficient manner, the final circuit design may not be optimal. Second, the computational cost may be too expensive for more complicated circuits, since we believe the number of optimization loops (or the number of yield calculations) will be dramatically increased and it is nondeterministic.

The experiment design method in conjunction with the statistical variance analysis has been widely used in the statistical circuit design and analysis. With this technique, the effects of the significance on circuit performance of individual circuit components in the circuit can be seperated and estimated.The core of this method is the selection of the design method. We have shown that the orthogonal array design has a great balance between the statistical accuracy and the computational cost. Even for the large analog integrated circuits, the method is very efficient since the number of simulations can be determined. In addition, by performing the statistical variance analysis, we are able to find the final optimal circuit design. That is the total circuit area can be optimized.

Both developed optimization algorithms have been examined on the basic Miller compensated operational amplifier and all the original goals have been accomplished.

5.2 Future work

The investigation of the statistical optimization algorithms in this thesis illustrates the possible applications of the SMOS model. The SMOS model which comprehends the dependence of the device area, circuit layout and transistor bias on the parameter variance can be incorporated as part of the statistical circuit design and optimization cycle. The recommendations for the future work in this statistical optimization area are following:

- The SMOS model implemented in the developed statistical optimization algorithms only models the mismatch in NMOS transistors [8, 1]. Later work expands the SMOS model by measuring and testing the mismatch in PMOS transistors and the interdie variations of both NMOS and PMOS parameters. The CAD implementation of the SMOS has also been updated with the interdie variations [9]. It will be interesting to see if the optimization techniques still work when the interdie variations are included.

- For the second optimization algorithm investigated in this thesis, the experiment design method was incorporated. In order to determine the optimal circuit design, the statistical hypothesis testing technique was introduced for the variances analysis. The optimal design can also be accomplished with different statistical analysis approaches. For example, the response surface methodology (RSM) may be investigated [27, 28, 29]. With the construction of the response surface (or yield body) in the design space, this should enable the optimizor to determine the optimal circuit design as well. The circuit optimizor will need to

have the solid knowledge of statistics and existing statistical CAD tools such as SAS (Statistical Analysis Software).

- Other optimization algorithms, such as the simulated annealing, should be investigated. Simulated annealing is based on the physical fact that a particle placed in a given potential and with Brownian motion is diffused into the global minimum of the given potential profile [30]. It can be used to solve the multiminimal optimization problem on multidimensional continuous design space and also is less sensitive to being trapped in a local minima.

The eventual goal of the future reseach in this statistical circuit optimization area is to develop a complete CAD tool to aid in the design automation of high performance and high yield analog integrated circuits.

Appendix A

SMOS Intradie Process File for NMOS Transistors

```
 VFB  -0.7923   0.1596   -0.2149  0.0632  73.3E-6
P  0.6978  0.4069 -0.4593  0.0894 -0.2617  0.1873
 K1   1.0631    -0.3540  0.6939   0.0714  45.3E-6
P -0.6734 -0.0643  0.6136 -0.3218  0.2236 -0.1287
 K2   0.1297    0.1116   0.0565   0.0178  7.00E-6
P -0.5059  0.3363  0.6646 -0.3308  0.1605 -0.1308
 ETA  -0.0290   0.0993   -0.0321  0.00541 4.38E-6
P  0.8557  0.3103  0.0248  0.2247  0.1898 -0.0982
 MUZ  611.91    437.9    -107.5   27.91    0.0399
P -0.0527  0.7673 -0.0901  0.3321  0.4877  0.1258
 U0   0.0478    0.0764   -0.0632  0.00625 5.13E-6
P  0.4109  0.1562  0.6864  0.0032  0.0404  0.5163
 U1   0.2972    0.7812   -0.0720  0.0714  46.7E-6
P -0.6792  0.2479 -0.6611 -0.0143  0.0077 -0.1356
 X2MZ -3.063    -1.052   104.5    4.545   1.93E-3
P  0.0778  0.9278  0.2304 -0.1235 -0.2002 -0.0772
 X2E  -0.00504  0.0269   -0.0172  8.89E-4 0.67E-6
P -0.7571 -0.0761  0.4429  0.4327 -0.0670 -0.0086
 X3E  0.00393   -0.00543 2.54E-4  0.00109 0.43E-6
P -0.7048 -0.2639 -0.0817 -0.3399 -0.0675  0.4564
 X2U0 0.000506  -0.00693 0.0395   0.00178 1.07E-6
P  0.4250  0.7921  0.1654 -0.3487 -0.1651 -0.0411
 X2U1 -0.1009   0.2365   -0.1449  0.0267   6.2E-6
P -0.6890 -0.1813  0.4523  0.4725 -0.2146  0.0141
 MUS  763.56    1160     -145.8   87.00    0.0645
P -0.6923  0.5493 -0.3713  0.0936  0.1824  0.1529
 X2MS -64.43    159.5    61.69    14.11   9.33E-4
P -0.4722  0.6385  0.4656  0.1935 -0.3140 -0.0585
 X3MS 30.30     239.8    -26.61   19.51    0.0131
P -0.8145  0.2912 -0.4228 -0.0065 -0.0012  0.0968
```

```
 X3U1 0.1502    0        -0.00388 0.0194  14.7E-6
P -0.7682  0.1775 -0.5631 -0.1171 -0.1079 -0.0107
 PHI  0.7500    0        0        0       0
P  0       0       0       0       0       0
 TOX  0.04      0        0        0       0
P  0       0       0       0       0       0
 VDD  5         0        0        0       0
P  0       0       0       0       0       0
 DL   0         0        0        0       0
P  0       0       0       0       0       0
 DW   0         0        0        0       0
P  0       0       0       0       0       0
 CGD0 3.41E-10  0        0        0       0
P  0       0       0       0       0       0
 CGS0 3.41E-10  0        0        0       0
P  0       0       0       0       0       0
 CGB0 5.51E-10  0        0        0       0
P  0       0       0       0       0       0
```

Appendix B

Nominal Circuit Optimization Program of APLAC

```
*resistor  Vc:-2.7 to -3.8 :no Vt in the eqn.
*apr,90
*R:40k 80k

**********************************
********** THD ANALYSIS **********
**********************************
#ver

#define nharm 4
#define f0 1k
*
Prepare SS nharm

OptimMethod MinMax

Declare IAPLACVAR
+ b1=0.17
+ W2=30u
+ L3=3u
+ L4=20u

Declare VECTOR eff REAL nharm
+       APLACVAR time THD

**********************************
***** OPTIMIZATION VARIABLES *****
**********************************

APLACVAR a1 1840p OPT
```

```
APLACVAR L2 7.16u OPT
APLACVAR W3 17.17u OPT
APLACVAR W4 5.69u OPT

*********************************
******** MODEL DEFINITIONS *******
*********************************

.MODEL NM NMOS (LEVEL=2 KP=5.018000E-05 VTO=1.0 GAMMA=1.024 PHI=.60
+ TOX=411.00E-10 LD=.243906U NSUB=2.230E+16 UO=597.303
+ UEXP=.142861
+ UCRIT=89159.5
+ DELTA=1.38386 VMAX=71683.1 XJ=.25U NFS=7.32701E+11 NEFF=1.0 NSS=1.0E+12
+ TPG=1.0 RSH=23.6 CGDO=3.073878E-10 CGSO=3.073878E-10 CGBO=6.56424E-10
+ CJ=4.04E-04
+ MJ=.457 CJSW=5.02E-10 MJSW=.369 PB=.8)
*
.MODEL PM PMOS (LEVEL=2 KP=2.007E-05 VTO=-.73 GAMMA=.5039 PHI=.60
+ TOX=411E-10 LD=.25U NSUB=5.4E+15 UO=238.92
+ UEXP=.215244
+ UCRIT=21917.9
+ DELTA=1.01034 VMAX=41620.5 XJ=.25U NFS=1.191843E+12 NEFF=1.001 NSS=1.0E+12
+ TPG=-1.0 RSH=70.1 CGDO=3.150679E-10 CGSO=3.150679E-10 CGBO=6.56424E-10
+ CJ=2.08E-04
+ MJ=.466 CJSW=2.23E-10 MJSW=.127 PB=.7)

*********************************
******* CIRCUIT DEFINITIONS ******
*********************************

Mosfet M1 4 4 7 7 MODEL NM W (a1*b1)^(1/2) L (a1/b1)^(1/2)
Mosfet M2 5 5 6 6 MODEL NM W (a1*b1)^(1/2) L (a1/b1)^(1/2)
Mosfet M7 11 4 7 7 MODEL NM W (a1*b1)^(1/2) L (a1/b1)^(1/2)
Mosfet M8 10 5 6 6 MODEL NM W (a1*b1)^(1/2) L (a1/b1)^(1/2)
Mosfet M5 1 4 21 21 MODEL NM W 4*W3 L L3
Mosfet M6 1 5 20 20 MODEL NM W 4*W3 L L3
Mosfet M3 6 3 2 2 MODEL NM W W3 L L3
Mosfet M4 7 3 2 2 MODEL NM W W3 L L3
Mosfet M17 7 8 2 2 MODEL NM W W2 L L2
Mosfet M18 8 8 2 2 MODEL NM W W2 L L2
Mosfet M20 6 9 2 2 MODEL NM W W2 L L2
Mosfet M19 9 9 2 2 MODEL NM W W2 L L2
```

```
Mosfet M11 11 11 1 1 MODEL PM W W4 L L4 PUBLIC
Mosfet M12 8 11 1 1 MODEL PM W 2*W4 L L4 PUBLIC
Mosfet M16 10 10 1 1 MODEL PM W W4 L L4 PUBLIC
Mosfet M15 9 10 1 1 MODEL PM W 2*W4 L L4 PUBLIC
Mosfet M14 4 10 1 1 MODEL PM W W4 L L4 PUBLIC
Mosfet M13 5 11 1 1 MODEL PM W W4 L L4 PUBLIC
Mosfet M10 20 20 7 7 MODEL  NM W 4*W3 L L3
Mosfet M9 21 21 6 6 MODEL  NM W 4*W3 L L3

**********************************
******** SUPPLY VOLTAGES *********
**********************************

Volt VDD 1 0 DC 5
Volt VSS 2 0 DC -5

**********************************
******* CONTROLING VOLTAGES ******
**********************************

Volt VC1 3 0 DC -3.1

**********************************
********** THD ANALYSIS **********
**********************************

Volt Vtr 40 0 SS 1 1.7
Volt VM1 4 40 DC 0
Res R3 5 99 1.0
*
Model OpModel ROUT 0
Opamp op1 0 5 99 0
+ AV 1e12
+ Model opModel
*

Function THDIST Distortion(99,0)
Sweep "ss analysis"
+ SS_ANALYSIS
+ F0 f0
+ X "frequency" "Hz" 0.0 nharm*f0
+ Y "Uout" "V" 0.0 0.35
```

```
*+ PLOTTER "res5.hp"
*
  Call eff=mag(RMSSpectrum(99))
*
  Call THD=THDIST

  Goal THD LT 0.80
  Display VECTOR nharm
  + X "f" HarmFreq
  + Y "Uout" eff
  + DRAW_STYLE SPECTRUM
EndSweep
*
Print LF LF
+ S "Harmonic Distortion " REAL Distortion(99,0) S "%" LF
+ S "DC level    " REAL eff[0] LF
+ S "1*f0 level " REAL eff[1] LF
+ S "2*f0 level " REAL eff[2] LF
+ S "3*f0 level " REAL eff[3] LF
*+ S "Area(M1,M2,M7,M8): " REAL a1 LF
*+ S "Area(M17,M18,M19,M20): " REAL a2 LF
*+ S "Area(M3,M4): " REAL a3 LF
*+ S "Area(M5,M6,M9,M10): " REAL 4*a3 LF
*+ S "Area(M11,M13,M14,M16): " REAL a4 LF
*+ S "Area(M12,M15): " REAL 2*a4 LF
*+ S "W/L(M1,M2,M7,M8): " REAL W1/L1 LF
*+ S "W/L(M17,M18,M19,M20): " REAL W2/L2 LF
*+ S "W/L(M3,M4): " REAL W3/L3  LF
*+ S "W/L(M5,M6,M9,M10): " REAL 4*(W3/L3) LF
*+ S "W/L(M11,M13,M14,M16): " REAL W4/L4 LF
*+ S "W/L(M12,M15): " REAL 2*(W4/L4) LF
*+ S "W(M1,M2,M7,M8): " REAL W1 LF
*+ S "W(M17,M18,M19,M20): " REAL W2 LF
*+ S "W(M3,M4): " REAL W3  LF
*+ S "W(M5,M6,M9,M10): " REAL 4*W3 LF
*+ S "W(M11,M13,M14,M16): " REAL W4 LF
*+ S "W(M12,M15): " REAL 2*W4 LF LF
*
Print OPT_VAR

OpenFile A "OPT.dat"
Print OPT_VAR FILE "OPT_VAR
```

```
CloseFile "OPT.dat"

OpenFile A "OPT.dat"
Print FILE "OPT.dat" DATE LF
+ S "Harmonic Distortion " REAL Distortion(99,0) S "%" LF
+ S "DC level    " REAL eff[0] LF
+ S "1*f0 level " REAL eff[1] LF
+ S "2*f0 level " REAL eff[2] LF
+ S "3*f0 level " REAL eff[3] LF LF
*+ S "Area(M1,M2,M7,M8): " REAL W1*L1 LF
*+ S "Area(M17,M18,M19,M20): " REAL W2*L2 LF
*+ S "Area(M3,M4): " REAL W3*L3  LF
*+ S "Area(M5,M6,M9,M10): " REAL 4*(W3*L3) LF
*+ S "Area(M11,M13,M14,M16): " REAL W4*L4  LF
*+ S "Area(M12,M15): " REAL 2*(W4*L4) LF LF
*+ S "W/L(M1,M2,M7,M8): " REAL W1/L1 LF
*+ S "W/L(M17,M18,M19,M20): " REAL W2/L2 LF
*+ S "W/L(M3,M4): " REAL W3/L3  LF
*+ S "W/L(M5,M6,M9,M10): " REAL 4*(W3/L3) LF
*+ S "W/L(M11,M13,M14,M16): " REAL W4/L4 LF
*+ S "W/L(M12,M15): " REAL 2*(W4/L4) LF LF
*+ S "W(M1,M2,M7,M8): " REAL W1 LF
*+ S "W(M17,M18,M19,M20): " REAL W2 LF
*+ S "W(M3,M4): " REAL W3  LF
*+ S "W(M5,M6,M9,M10): " REAL 4*W3 LF
*+ S "W(M11,M13,M14,M16): " REAL W4 LF
*+ S "W(M12,M15): " REAL 2*W4 LF LF
*+ S "L(M1,M2,M7,M8): " REAL L1 LF
*+ S "L(M17,M18,M19,M20): " REAL L2 LF
*+ S "L(M3,M4): " REAL L3  LF
*+ S "L(M5,M6,M9,M10): " REAL L3 LF
*+ S "L(M11,M13,M14,M16): " REAL L4 LF
*+ S "L(M12,M15): " REAL L4 LF LF
CloseFile "OPT.dat"

**********
**********
```

Appendix C

Statistical Circuit Optimization Program of APLAC

```
*****************************************
#define LN 4u

#define LP 4u

Prepare OPT MINMAX

Declare IAPLACVAR
+ nsim=500      $ number of Monte Carlo simulations
+ tol=2.0e-3      $ tolerance of offset voltage
+ yldtarg=0.90
+ k=0 n=0
+ b8=2

Declare APLACVAR add i j min dmin

Declare VECTOR
+  PM REAL nsim     $ phase margin
+  AV REAL nsim     $ DC gain
+  GB REAL nsim     $ gain-bandwidth
+  GM REAL nsim     $ gain margin
+  SR REAL nsim     $ slew rate
+  VOFF REAL nsim   $ offset voltage
+  A REAL 6
+  d REAL 6
+  al REAL 6
+  al2 REAL 6
+  YIELD REAL 50
*
*************************************
```

```
*  Optimization variables for centering - W/L ratios
APLACVAR b3 8.5 OPT
APLACVAR b6 152 OPT
APLACVAR b1 8 OPT
APLACVAR b5 8 OPT
APLACVAR b7 65 OPT
*APLACVAR b8 2 OPT
*
**************************************
*  SMOS model definition
SMOS nstat FILE chip2.st NPCA 6 NTRAN 5 NPAR 16
+ XY -3-LN*1e6   0
+    3-LN*1e6    0
+    0           4+LN*1e6*9.5
+    5*LN*1e6+25 0
+    -3-LN*1e6   4+LN*1e6*9.5

SMOS pstat FILE chip2p.st NPCA 6 NTRAN 3 NPAR 16
+ XY -3-LP*1e6   10+LP*1e6*4+LN*1e6*4.5
+    3+LP*1e6    10+LP*1e6*4+LN*1e6*4.5
+    6*LP*1e6+25 10+LP*1e6*4+LN*1e6*4.5
*
**************************************
*  Constant model parameters
Model npar TOX=0.04 VDD=5 DL0=0 DW0=0 PHI0=0.75 AD=0
+      PD=0 AS=0 PS=0 CGD0=3.4E-10 CGS0=3.4E-10 CGB0=5.5E-10
+      N0=1 NB0=0 ND0=0 RSH=0 CJ=0 CJW=0 DS=0 WDF=0 XPART=1
+      IJS=0 JSW=0 PJ=0.7 PJW=0.7 MJ=0 MJW=0

Model ppar TOX=0.04 VDD=5 DL0=0 DW0=0 PHI0=0.69 AD=0
+      PD=0 AS=0 PS=0 CGD0=3.8E-10 CGS0=3.8E-10 CGB0=6.5E-10
+      N0=1 NB0=0 ND0=0 RSH=0 CJ=0 CJW=0 DS=0 WDF=0 XPART=1
+      IJS=0 JSW=0 PJ=0.7 PJW=0.7 MJ=0 MJW=0
*
**********************************************
*  Op-Amp Circuit
Bsim m3  5  5 1 1  PUBLIC MODEL ppar MODEL pstat
+    L=(A[2]/b3)^(1/2)*LP W=(A[2]*b3)^(1/2)*LP P
Bsim m4  6  5 1 1  PUBLIC MODEL ppar MODEL pstat
+    L=(A[2]/b3)^(1/2)*LP W=(A[2]*b3)^(1/2)*LP P
Bsim m6  8  6 1 1  PUBLIC MODEL ppar MODEL pstat
+    L=(A[4]/b6)^(1/2)*LP W=(A[4]*b6)^(1/2)*LP P
```

```
Bsim m1  5  3 7 7  PUBLIC MODEL npar MODEL nstat
+    L=(A[1]/b1)^(1/2)*LN W=(A[1]*b1)^(1/2)*LN
Bsim m2  6  4 7 7  PUBLIC MODEL npar MODEL nstat
+    L=(A[1]/b1)^(1/2)*LN W=(A[1]*b1)^(1/2)*LN
Bsim m5  7 10 2 2  PUBLIC MODEL npar MODEL nstat
+    L=(A[3]/b5)^(1/2)*LN W=(A[3]*b5)^(1/2)*LN
Bsim m7  8 10 2 2  PUBLIC MODEL npar MODEL nstat
+    L=(A[5]/b7)^(1/2)*LN W=(A[5]*b7)^(1/2)*LN
Bsim m8 10 10 2 2  PUBLIC MODEL npar MODEL nstat
+    L=(A[6]/b8)^(1/2)*LN W=(A[6]*b8)^(1/2)*LN

Cap  CC 8 6 3.5p
Cap  CL 8 0 10p
Curr IB 1 10 DC 10u
Res  RB 1 10 10meg
Res  RO 11 12 1meg
Cap  CO 11 0  1.0
CSource voff 12 0 8 0 1.0 VCVS
Volt VDD 1 0 DC 5
Volt VSS 2 0 DC -5
Volt Vnon 4 0 DC 0 AC 1.0
Volt Vinv 3 11 DC 0
*
Function AVgain magdB(vac(8))
For i 1 6
  Call A[i]=10
EndFor

While (n!=2)
  Call SME(nstat,N)
  Call SME(pstat,N)
  Call j=0
*
****************************************
*  Begin centering loop
  Sweep "Open Loop Frequency Response"
  + OPT_XTOL 1m
  + LOOP 51 FREQ LOG 10 100MEG

      If NewLoop
         Call AV[1]=AVgain
         Analyze DC
```

```
      Call VOFF[1]=vdc(8)
    EndIf

    IF (LOOPINDEX == 50)
      Calc
        SolveF(5MEG, AVgain)
        GB[1]=f
        PM[1]=180+pha(vac(8))
        SR[1]=Ref(m5,IDS)/3p
        SolveF(GB[1], pha(-vac(8)))
        GM[1]=-AVgain
        j=j+1
      EndCalc
    EndIf

    Goal GB[1] GT 5.1MEG UNIT 0.1MEG
    Goal AV[1] GT 71 UNIT 1
    Goal PM[1] GT 56 UNIT 1
    Goal GM[1] GT 21 UNIT 1
    Goal SR[1] GT 12.7 UNIT 0.2
    Goal VOFF[1] BETWEEN -5e-4 5e-4 UNIT 1e-4

  EndSweep
*
*  End centering loop
*******************************************
*
  OpenFile A opt3n.out
  Print FILE opt3n.out DATE LF
  +     S "OPT NUM = " R "%#6.4e" j LF
  +     S "W/L (1,2) = " R "%#6.4e" b1 LF
  +     S "W/L (3,4) = " R "%#6.4e" b3 LF
  +     S "W/L (5) = " R "%#6.4e" b5 LF
  +     S "W/L (6) = " R "%#6.4e" b6 LF
  +     S "W/L (7) = " R "%#6.4e" b7 LF
  +     S "W/L (8) = " R "%#6.4e" b8 LF LF
  +     S "a1= " REAL A[1] S "   a3= " REAL A[2] LF
  +     S "a5= " REAL A[3] S "   a6= " REAL A[4] LF
  +     S "a7= " REAL A[5] S "   a8= " REAL A[6] LF LF
  +     S "GB    = " R "%#6.4e" GB[1] LF
  +     S "SR    = " R "%#6.4e" SR[1] LF
  +     S "GM    = " R "%#6.4e" GM[1] LF
```

```
  +     S "PM    = " R "%#6.4e" PM[1] LF
  +     S "AV    = " R "%#6.4e" AV[1] LF
  +     S "VOFF  = " R "%#6.4e" VOFF[1] LF LF
  CloseFile opt3n.out

*
*********************************************
*  Begin Monte Carlo loop
  For i 1 nsim
    Call SME(nstat,A)
    Call SME(pstat,A)
    Analyze DC
    Call VOFF[i]=vdc(8)
  EndFor
*  End Monte Carlo loop
*********************************************
*  Calculate yield
  Call add=0
  For i 1 nsim
    If ((VOFF[i]>-tol)*(VOFF[i]<tol)) then
      Call add=add+1
    EndIf
  Endfor
  Call k=k+1
  Call YIELD[k]=add/nsim

  OpenFile A opt3n.out
  Print FILE opt3n.out DATE LF
  +     S "YIELD = " REAL YIELD[k] LF LF
  CloseFile opt3n.out
*
*  Modify device areas
  If (k == 1)
    Call a[1]=2*a[1]
  EndIf
  If ((k>1)*(k<7))
    Call a[k-1]=a[k-1]/2
    Call a[k]=2*a[k]
    Call d[k-1]=a[k-1]/(YIELD[k]-YIELD[1])
  EndIf
  If (k == 7)
    Call a[6]=a[6]/2
```

```
    Call d[6]=a[6]/(YIELD[7]-YIELD[1])
    Call min=1
    Call dmin=d[1]
    For i 2 6
      If (abs(d[i])<abs(dmin)) then
        Call min=i
        Call dmin=d[min]
      EndIf
    EndFor
    Call al[min]=a[min]
    Call a[min]=a[min]+d[min]*(yldtarg-YIELD[1])
  EndIf
  If (k > 7)
    If ((YIELD[k]>0.85)*(YIELD[k]<0.95)) then
      If (n == 1) then
        Call n=2
      Else
        Call n=1
      EndIf
    Else
      Call k=0
    EndIf
  EndIf
*  End of device area modifications
*****************************************
*
EndWhile
*  End statistical optimization loop
*****************************************
```

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