Antimonide-Based Avalanche Photodiodes on InP Substrates for Short-Wave Infrared Applications

Dissertation

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Abstract

Infrared detection is crucial for many applications including remote sensing, light detection and ranging (LiDAR), chemical and gas detection, topographic mapping, optical communication, among other commercial, military and research applications[1-4]. To target the infrared spectral range, notably the short-wave infrared (SWIR) range, avalanche photodiodes (APDs) are attractive as they can provided the much-needed sensitivity and responsivity that is required for low photon environments due to their inherent amplification process of multiplication via carriers impact ionizing. This, in turn, enables APDs to improve the signal to noise ratio (SNR) of an optical receiver system. To achieve high performance via high SNR of an APD, it is necessary to maximize gain and quantum efficiency, while considering methods of reducing the dark current and the excess noise, which contribute to high noise, thereby lowering the SNR. To achieve high sensitivity, many materials have been investigated for APDs. Recently, III-V Sb-based material systems have been on the forefront for the research and development of APDs, particularly on InP substrates, which provide lower costs for future large-scale manufacturing of the technology. While one material may meet some of the key figures of merit to achieve high performance for infrared applications, significant challenges arise with meeting all of them, which has motivated the work of more complex heterostructure APD designs known as separate, absorption, charge, and multiplication (SACM) APDs. In an SACM design,

different material systems and compositions are selected for each layer, to limit the tunneling dark current, achieve high multiplication gain, and low excess noise, especially when operating at high temperatures without cryogenic cooling. To achieve high performance and push operation to large enough reverse biases to leverage gain via impact ionization, heavy emphasis in investigations has been on reducing the dark current and its components stemming from either growth (bulk dark current) or fabrication processing (surface leakage dark current). While much work has centered around optimizing designs of complex III-V SACM APDs, much less has been investigated surface dark current reductions as another method to inhibit the dark current a device experience overall.

The contribution of this work is to improve Sb-based III-V SACM APDs for high performance via four investigations that were completed. The contributions of this dissertation are as follows.

1. Two Sb-based materials have been of interest as multiplier materials for complex SACM APDs targeting the SWIR due to their potential to promote sufficient impact ionization of carrier for maximizing gains. These two multipliers are AlGaAsSb and AlInAsSb and have been demonstrated on InP substrates as p-i-n devices with low dark current and low excess noise behavior[43,44,46]. When implemented into more complex SACM designs, it is essential to fully understand the material to properly design the electric field profile under high biases. One significant detail to understand about the

material to optimize SACM performance is to determine the background doping and unintentionally doped (UID) polarity of the material. In this section, the doping polarity of random alloy AlGaAsSb and AlInAsSb via a double mesa device architecture and capacitance-voltages measurements across several temperatures and voltages of interest was investigated. Through this investigation, future complex SACM designs implementing these two Sb-based multipliers will be improved to realize higher performance.

2. AlInAsSb has demonstrated high potential as a multiplier material for SACM APDs but has never been investigated previously in an SACM design with InGaAs absorber on InP substrates. In this investigation, the first InGaAs/AlInAsSb SACM APD on InP substrates has been evaluated for its behavior across a variety of temperatures and displaying high temperature stability over other reported APDs.
3. AlGaAsSb has been investigated in both a p-i-n and as part of an SACM, employing different growth techniques and UID layer thicknesses, to reduce the bulk dark current. Very little has been reported about reducing the surface dark current via alternative fabrication processing of the material. In this contribution, a Zn-diffused AlGaAsSb p-i-ns were investigated as a step towards fully planar Zn-diffused AlGaAsSb APDs, that have the potential to mitigate surface leakage dark current, delay breakdown and subsequently achieve high gains.

4. AlGaAsSb has been employed in SACM APDs for 1550 nm detection using a GaAsSb absorber on InP substrates and have demonstrated ultra-high gain, but no work has investigated the GaAsSb/AlGaAsSb as a planar architecture. In this contribution a Zn-diffused GaAsSb/AlGaAsSb SACM APD was investigated with the implementation of guard rings to further improve performance.

With the contributions outlined from this work, further improvements in high performing Sb-based APDs for short-wave infrared detection can be achieved. This can be accomplished via further optimization of the heterostructure SACM design and engineering and considering alternative fabrication processing to reduce the dark current, thereby lowering SWaP-C overall.

Dedication

I dedicate my dissertation to my family. Thank you for all the support.

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Fields of Study

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Chapter 1. Background and Motivation

The infrared spectral range is a component of the electromagnetic spectrum that spans wavelengths of 0.7 μm to 25 μm and is comprised of smaller regimes called the near-infrared (NIR, 0.7 - 1.0 μm), short-wave infrared (SWIR, 1.0 – 3.0 μm), mid-wave infrared (MWIR, 3.0 – 5.0 μm), long-wave infrared (LWIR, 8.0 – 14.0 μm), and the very long-wave infrared (VLWIR, 14.0 – 25.0 μm). There is significant interest in the development and implementation of infrared detectors that can image wavelengths within the infrared spectral range, notably for applications including remote sensing, light detection and ranging (LiDAR), chemical and gas detection, topographic mapping, optical communication, and other commercial, military and research applications[1-4]. Infrared detectors and systems have been employed for these applications since the 1950's, when the first-generation infrared systems were developed through the implementation of single pixels and linear arrays[5-6]. Since their infancy, infrared detectors and systems have undergone an iterative transformation, with second (2D staring array implementation, and single color), third (high operating temperature, multicolor capabilities, large format arrays), and present-day fourth generation systems implementing focal plane arrays (FPAs) from photonic material systems and read-out integrated circuits (ROICs)[5]. The FPA is responsible for converting radiation into current by detecting photons at a given wavelength and the ROIC reads the current signal. To ensure successful detection, the

optical receiver system requires a photodetector, which is an optoelectronic device that absorbs the received optical energy and converts it to electrical energy, typically in the form of photocurrent[7]. One popular type of photodetector implemented for infrared detectors, especially in photon-starved applications, is an Avalanche Photodiode (APD), which is scalable as the number of pixels increases in FPAs[8]. APDs are suitable for these detection applications because they are highly sensitive and can amplify weak inputted signals due to an internal gain process. This internal gain process results from carrier multiplication via impact ionization. Impact ionization of carriers is a stochastic process in which an electron (or hole) acquires sufficient energy in a high electric field region that enables it to collide with other carriers. During this process, an electron-hole pair is generated. This multiplication process continues and produces the internal gain for the APD. Figure 1 depicts this process of carriers impact ionizing in an APD, whereby $\frac{1}{\alpha}$ is the average distance an electron will travel before impact ionizing and $\frac{1}{\beta}$ is the average distance a hole will travel before impact ionizing. With the mechanism of impact ionization, APDs can increase the signal-to-noise ratio (SNR) of a detector's receiver system, thereby providing an attractive photodetector choice for a variety of applications across the various infrared wavelength regimes.

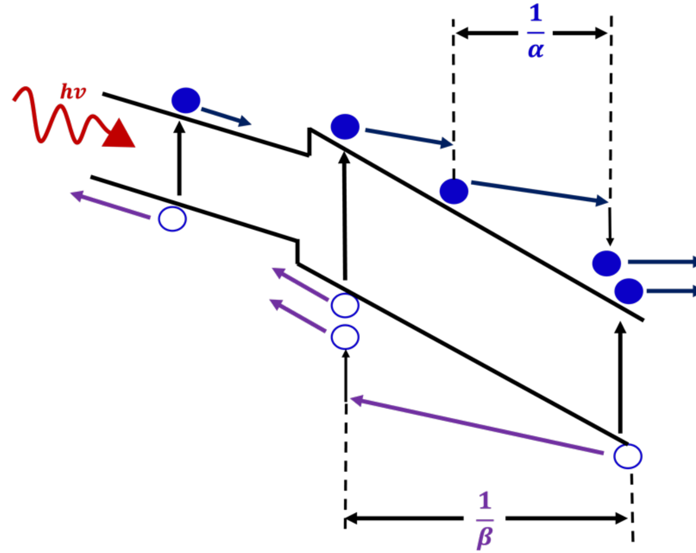

Figure 1. Impact Ionization Process for electrons and holes in avalanche photodiodes

1.1 Avalanche Photodiodes for Short Wave Infrared (SWIR) Applications

The SWIR regime, which spans 1.0 – 3.0 μm, is attractive for a variety of applications, including the detection of greenhouse gases, in particular methane and carbon dioxide, 3-D mapping of urban infrastructure and implementation into autonomous vehicles, and a variety of additional defense and commercial LiDAR applications[9-11]. 1.55 – 2.0 μm is of notable interest for these applications as lasers may be considered eye safe at these wavelengths under reasonable power conditions[12,13]. Although Si is a common choice for many applications, this wavelength range is not satisfied using Si based APDs, due Si's cut-off wavelength being approximately 1.1 μm. As a result, alternative APDs have been investigated for these SWIR applications. Another APD choice that is implemented for the SWIR is HgCdTe. While HgCdTe APDs are a common choice

because they can achieve high performance due to high gain and excess noise close to unity, they suffer from instability that arises from material nonuniformity and low fabrication yields[14-17]. Furthermore, the low noise that HgCdTe can demonstrate is only realized at compositions close to $Hg_{0.5}Cd_{0.5}Te$, where the bandgap is narrow, enabling tunneling to occur easily. With a low bandgap energy, dark current is high for HgCdTe APDs at high operating temperatures (HOT) and thus limits the operation of these devices to ~ 77 K[16]. The high dark current for HgCdeTe at higher temperatures introduces noise interferences into the detector device that has a significant detriment to overall detection performance. With this, cryogenic cooling is required for detector systems employing HgCdeTe, bringing with it a significant increase in cost. This is unfavorable for a variety of applications where a driving motivator is to maintain low SWaP-C (Size, Weight, Power, and Cost) for the overall detector system, especially as many applications continue to move towards smaller platforms. This motivates the exploration, development, and implementation of III-V APDs.

At present, In_xGa_{1-x} As APDs have been at the forefront of commercially available III-V APDs for SWIR detection, notably for 1.55 µm applications, due to their favorable bandgap energy of ~ 0.73 eV (for $In_{0.53}Ga_{0.47}As$), low noise, high demonstrated responsivity and fast rise and fall times, stable operation at higher temperatures, and lattice matching ability to InP substrates[18]. $In_xGa_{1-x}As$ also provides tunability to other wavelengths within the SWIR and beyond, namely between 0.85 and 3.6 µm, by adjusting the composition of indium and gallium[19-21]. While InGaAs/InP APDs are commercially

available for SWIR detection, InGaAs has a k-value of ~ 0.4 - 05 and an absorption coefficient of ~10^4 cm^{-1} which results in an undesirable increase in excess noise and speed limitations[22-25]. This has motivated the development of novel III-V APDs for SWIR with the implementation of Sb-based materials, which will be the focus of this work.

1.2 Figures of Merit for SWIR Avalanche Photodiodes

Before discussing the figures of merit, it is first necessary to discuss the types of APDs that exist. There are two main types of APDs that are investigated: linear mode APDs and Geiger mode APDs. As mentioned at the beginning of this chapter, APDs are attractive for a variety of infrared detection applications due to the impact ionization mechanism and the resulting gain that amplifies weak detected signals. While this is beneficial, the impact ionization process also multiplies dark current, results in excess noise, and limits the gain-bandwidth of the APD, all of which must be carefully considered[26-29]. For linear mode APDs, the photocurrent is multiplied from the impact ionization process and it proportional to the primary photocurrent and the multiplication gain denoted as M[30]. Excess noise factor, $F(M)$, also arises from impact ionization and has a relationship with gain for the linear mode APDs. Geiger mode APDs are unique from linear mode APDs are they can temporarily overbias the APD over its breakdown voltage to detect a signal in a process known as quenching[31,32]. Figure 2 illustrates the differences in current-voltage characteristics for PIN photodiodes, linear mode APDs and Geiger mode APDs within the reverse bias regime. While Geiger mode APDs provide interesting capabilities for detection, they have different figures of merit than linear mode APDs that must be

considered. Research efforts in this dissertation have focused on the development of linear mode APDs.

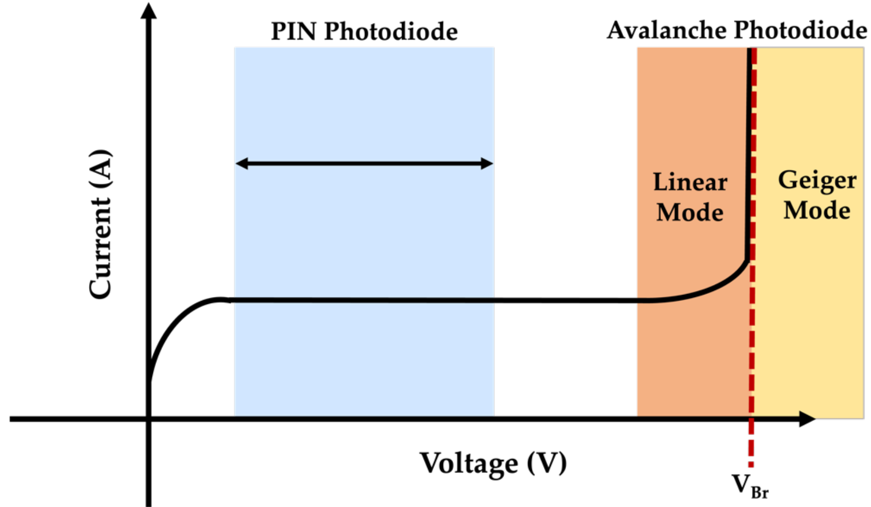

Figure 2. Current-Voltage characteristics of PIN photodiodes, linear mode APDs, and Geiger mode APDs within the reverse bias regime. V_{Br} represents the voltage at which the device experiences breakdown.

When designing and developing high performance linear mode APDs, there are several figures of merit to consider. High performance linear mode APDs require high gain, high quantum efficiency, low excess noise factor, low dark current to produce a high signal-to-noise ratio (SNR). Within an APD, multiplication gain is calculated from the photocurrent and the dark current over the operating voltages. Multiplication gain of an APD can be expressed as

$$M(V) = \frac{I_{photo}(V)}{I_{photo,M=1}} = \frac{I_{light}(V) - I_{dark}(V)}{I_{light,M=1} - I_{dark,M=1}} \qquad (1)$$

where $I_{photo}(V)$ is the measured photocurrent at a given voltage, $I_{photo,M=1}$ is the measured photocurrent at the unity gain voltage, whereby $M = 1$, $I_{light}(V)$ is the total current under illuminated conditions for a given voltage, $I_{dark}(V)$ is the dark current for a given voltage, and $I_{light,M=1}$ and $I_{dark,M=1}$ are the total current and dark current, at the unity gain point, respectively[31].

For infrared detector systems, the quantum efficiency is defined as the number of outputted electrons for the total number of incident photons and is dependent upon the selected optical signal's wavelength for the APD[31]. For high performing APDs, the quantum efficiency must be as high as possible for the targeted wavelength of interest.

The next figure of merit to consider for a high performing APD is the excess noise factor, *F(M)*. According to McIntyre's local field theory model for APDs, the excess noise factor is defined as

$$F(M) = k \cdot M + (1-k) \cdot \left(2 - \frac{1}{M}\right) \qquad (2)$$

$$k = \frac{\beta}{\alpha} \qquad (3)$$

In Eq. 2, *F(M)* is the excess factor, and k is the ratio of the hole ionization coefficient, β, to the electron ionization coefficient, α for electron APDs[27]. Excess noise factor has a relationship between the multiplication gain, the ratio of both carrier types of impact ionizing and is dependent upon the material selected for the APD as well as the

architecture of the device. The excess noise factor is a component of the SNR and contributed to the overall noise of the detector. Because of this, it is necessary to drive the excess noise factor down to as low as possible, while also keeping high M to leverage the gain achievable with APDs. This is accomplished by targeting an excess noise factor as close to 2 as possible through the implementation of materials that demonstrate low k-values. Low k-value materials occur when one carrier type dominates the impact ionization over the other carrier type. While the McIntyre model provides an elegant representation of carrier's impact ionizing in an APD, actual transport, scattering, the impact ionization process, and the increase in noise within an APD as a function of the gain, a more sophisticated model may be required in the future.

The next critical figure of merit for APDs is the dark current. Dark current can be defined as the current an APD exhibits in the absence of an illumination source. The total overarching dark current of a device can be differentiated into two components: bulk dark current and surface dark current. The total dark current can be expressed as

$$I_{dark} = I_{bulk}M + I_{surface} \qquad (4)$$

where I_{dark} is the total dark current, I_{bulk} is the bulk-derived dark current, $I_{surface}$ is the surface-derived dark current. The bulk-derived dark current is introduced into the APD via defects or nonuniformities that occur within the crystalline structure and occur during the growth process. The surface-derived dark current is introduced to the APD

during the fabrication processing of the epitaxial material to delineate individual devices for characterization. Based on Eq. 4, it can be noted that the multiplication gain also impacts the total dark current but multiplies with the bulk component only.

The final figure of merit that will be discussed for the linear mode APD is the SNR. SNR can be considered as the "cleanliness" of a signal pattern, and it is necessary to limit the noise components that hinder the signal detection and subsequently decreases detector sensitivity. SNR for an APD that is coupled to an amplifier circuit can be illustrated as

$$SNR = \frac{q\eta\phi M}{\sqrt{< i_{shot}^2 > + \sigma_{circuit}^2}} \qquad (5)$$

In Eq. 5, q is the electron charge, η is the quantum efficiency at the unity gain point, ϕ is the photon flux in photons/sec, $< i_{shot}^2 >$ is the shot noise, and $\sigma_{circuit}^2$ is the circuit noise in amperes[33]. To achieve high SNR, it is imperative that the shot noise is limited and to enable the noise to be dominated only by circuit components. Shot noise originates from the statistical nature of the generation-recombination process of carriers and can be expressed by

$$< i_{shot}^2 > = 2qB\left[q\eta\phi M^2 + I_{bulk}M^2F(M) + I_{surface}\right] \qquad (6)$$

Where B is the bandwidth. It can be noted that when $< i_{shot}^2 >$ is replaced in the SNR equation, a more in-depth SNR equation can be written as Eq. 7 below. It is evident from the equation that to achieve high SNR, it is necessary to reduce dark current, limit excess noise factor, while encouraging the gain to remain high.

$$SNR = \frac{q\eta\phi M}{\sqrt{2qB\left[q\eta\phi M^2 + I_{bulk} M^2 F(M) + I_{surface}\right] + \sigma_{circuit}^2}} \qquad (7)$$

It should be noted that while it is ideal to have APD that meets all the selected figures of merit, additional considerations may be required for the specific application of the detector system. Several additional constraints that may be necessary to account for include the operating temperature, operating voltage, and size, weight, and power (SWaP-C) associated with the system and its platform. For each individual application, some tradeoffs will be required to produce a successful APD.

1.3 PIN and SACM Avalanche Photodiodes

To achieve a high performing APD that meet or exceeds the required specifications for a given application, one must first consider the design and structure. Considerations must be undertaken for the structure and what methods may be useful to mitigate dark current. Dark current is a critical component to limit for APDs, especially when high performance is required at high voltage biases to achieve the maximum gain. Dark current arising from band-to-band tunneling (BTB) or trap assisted tunneling (TAT) can dominate

the dark current at high biases where there is a large electric field[34]. In a PIN structure APD, one material is selected for the APD, and it is difficult to implement a narrow bandgap material that can both detect the wavelength of interest, maximize gain via impact ionization and not suffer from excessive dark current from tunneling and subsequently high noise. To combat this, a more complex heterostructure design called a separate absorption, multiplication, and charge layer (SACM) APD can be utilized. In an SACM APD, each layer of the heterostructure is independently optimized for its specific purpose to maximize the APD's performance overall. The absorber layer's material and thickness is selected intentionally to enable absorption for the intended wavelength and encourage a high quantum efficiency. The multiplier layer is responsible for impact ionization in the APD, whereby a large gain be achieved and is also designed to consider achieve a low excess noise factor via material selection. In between the absorber layer and the multiplier layer is the charge and/or grading layer of the SACM. The grading layer is essential for ramping up the electric field sufficiently to ease electron transport through the structure. This is pertinent to the SACM as the absorber is designed to have a low electric field for reducing the tunneling dark current when voltage is applied, and the multiplier layer is designed to have a uniform high electric field for sufficient impact ionization to achieve maximum gain. Finally, the charge layer serves as a block to the electron transport until the electric field threshold has been reached. This staves off tunneling of carriers prematurely. One of the key design rules when designing a novel SACM APD is that the electric field across the absorber should be less than the tunneling threshold. In many SACM designs, a grading layer is also incorporated between the absorber and the multiplier to smooth band offsets

that occur with varying material compositions and assists with efficient electron transport from the narrow bandgap absorber to the wider bandgap multiplier. Each of the layers are fine-tuned using changes in composition of materials, thicknesses in the layers and doping concentrations for their respective roles in the SACM overall. Figure 3 shows the representative SACM heterostructure and the magnitudes of the electric fields within each respective layer.

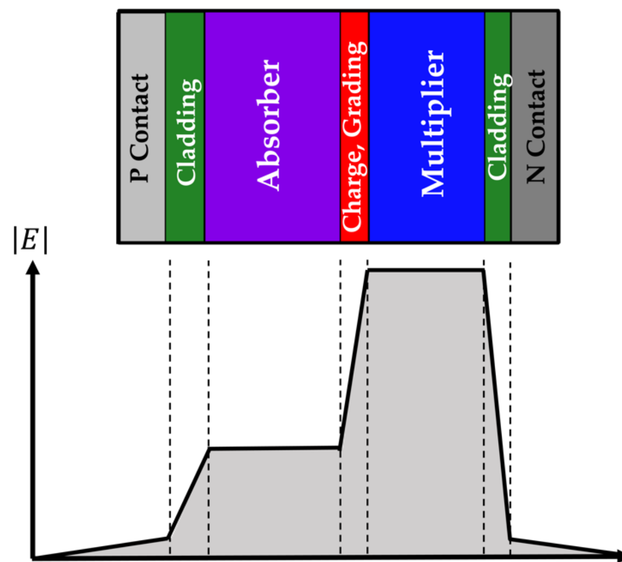

Figure 3. Representative heterostructure for an SACM APD and the magnitudes of the electric field through the APD.

1.4 Mesa and Planar Architecture Avalanche Photodiodes

Once a heterostructure design has been finalized and grown, the sample is then fabricated to realize individual devices that will undergo characterization to determine

performance. When processing the material via fabrication, there are typically two device architectures that are considered: mesa and planar. Figure 4 illustrates the two device architectures and their differences for a SACM APD. Mesa architecture devices are formed through a wet or chemical etching process whereby some of the epitaxial grown material is removed. Planar architecture devices are not delineated through etching but rather through a patterning process. For both types of architectures, there are challenges that arise with the fabrication processing that must be addressed to achieve high performance. Mesa APDs introduce unsatisfied dangling chemical bonds at the surface of the etched material that makes the susceptible to generation-recombination (G-R) dark current at the sidewalls. The presence of unwanted G-R dark current at the sidewalls can be mitigated through passivation techniques and can protect the structure from the surrounding environment that may degrade the material over time. Mesa APDs may can also experience premature breakdown because of notches that are produced during the etching process[35]. To circumvent the processing challenges of mesa devices, careful considerations of etching techniques and chemistries are required and are dependent upon the materials in the heterostructure.

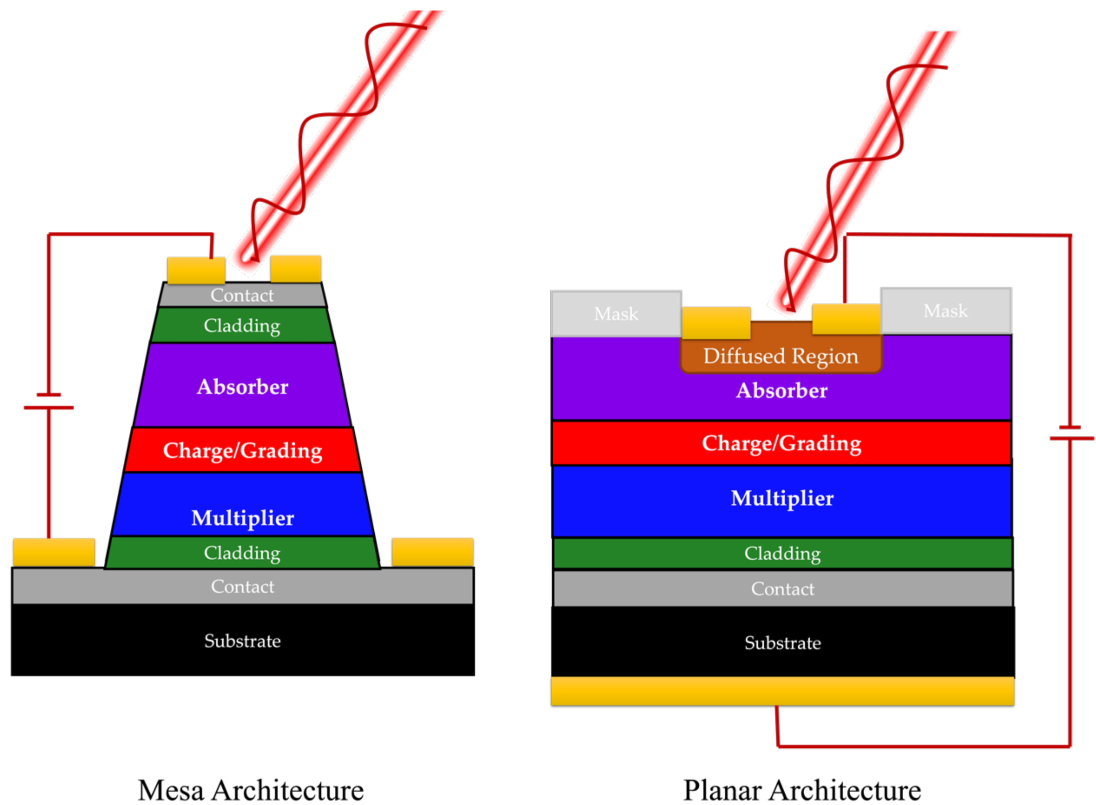

Figure 4. Representative SACM APD architectures produced during the fabrication processing.

Planar APDs have recently gained more interest for novel III-V materials due to the potential mitigation of premature breakdown and lower dark current that is introduced during the etching process of the device sidewalls during mesa fabrication. Planar APDs may provide a solution to this issue as they do not inherently require etching to differentiate devices from one another. Instead, planar APDs leverage hard mask patterning to distinguish devices on the sample. Many planar devices also implement a diffusion process for forming the p-n junction, whereby p-type doped atoms are diffused into an n-type

epitaxially grown material or substrate or through other methods, such as ion implantation. Planar diffused APDs require extensive optimization to encourage an optimal depth of the p-n junction vertically into the structure, while suppressing undesirable lateral diffusion that may take place. If the fabrication processing conditions selected for the diffusion are not ideal for the material, the APD may still suffer from challenges and may prove to be more difficult to fabricate than mesa architecture devices. As briefly mentioned, some planar devices implement an ion implantation process instead of diffusion. Ion implantation is a process by which selected dopants are in a plasma state and accelerated at the epitaxial material[36]. This process of bombarding the material with the dopants enables them to implant some depth into the structure and is dependent upon the dopant ion, the material, and the accelerated energy. While ion implantation has the benefit of being highly reproducible in successfully achieving localized doping at uniform depths, there is potential for the implantation process to be damaging to the material surface that may not be fully removed via annealing. In both diffusion and ion implantation planar structures, additional measures are typically taken to ensure proper performance such as via a double diffusion process or implementing guard rings. Both the double diffusion process as well as attached or floating guard rings mitigate high electric fields that occur at the p-n junction when biased at high voltages[37,38,39,40,41,42]. Additional considerations must be undertaken for the double diffusion and guard rings, which will be discussed later in more detail.

1.5 Prior Work

Previously, much work has been reported for III-V Sb-based APDs and how to develop high performing devices for a variety of applications within the SWIR regime, with a heavy emphasis at 1.55 – 2 μm. Initially, this work has focused on first demonstrating the feasibility of Sb-based III-Vs as multiplier materials via determining the necessary compositions, growth conditions, and substrates for AlGaAsSb and AlInAsSb p-i-n devices[43,44,45,46]. In parallel with these investigations, efforts have been made to determine the key features of APD performance, such as excess noise characteristics and the impact ionization coefficients[47,48,49,50,51,52,53,54,55]. Furthermore, investigations have been completed to determine the background doping polarity of the AlGaAsSb and AlInAsSb material systems[56,57]. Understanding all these components of the Sb-based multiplier materials enables the design and development of more optimized SACM APDs that have lower dark current, low excess noise and higher gains at the operating biases. Recently, work has been focused on demonstrating the SACMs and pushing the operating to achieve triple digit gains, which may enable future performance of linear APDs to achieve high single-photon sensitivity like that of Geiger mode APDs[58,59.60.61.62].

1.6 Problem Statement

Much of the prior work investigating Sb-based III-V APDs has gone into the selection and optimization of materials and the overall SACM. This has been accomplished in efforts to keep dark current low via the design of the structure to enable device operation

at high enough voltages where gain can be maximized. In these investigations, dark current has been the key component to mitigate, namely the bulk dark current, that arises from the structure's design and growth. While bulk dark current is critical to investigate, there is another dark current component, the surface leakage dark current, that hasn't been explored to the same degree and is worth assessing. Surface dark current occurs from fixed charges within the passivation layer and is introduced to the device during the etching process that delineated individual mesa devices. While surface leakage current is present in devices of all sizes that are etched, it becomes especially problematic for small devices. As work moves towards smaller and smaller devices (< 100 μm^2 in area), surface leakage current dominates the dark current. This is because as device dimensions decrease, ratio between the device's surface area to its volume increases and the overall surface leakage dark current compared to the total dark current increases[63]. This is challenging, especially if small device sizes are required for an application or implemented to reduce the likelihood of containing defects that are introduced during the growth. With a larger component of the dark current arising from the surface leakage current, this can make it difficult for devices to operate a higher temperature, whereby SWaP-C is the lowest for the detector system.

1.7 Proposed Solutions

Surface leakage dark current is problematic for devices and can contribute to high dark current overall and premature breakdown of the device that limits how much gain can be produced prior to breakdown. Since surface leakage current is introduced during the

standard fabrication processing of the material, alternative fabrication processes can be implemented to circumvent this. There are two potential pathways that can be gone down to reduce the surface leakage dark current. These are passivation techniques and materials and field engineering as shown in Fig. 5. While different passivants can be selected and will be briefly discussed in subsequent chapters, field engineering may be a more impactful approach to reducing surface leakage dark current. Within the field engineering toolbox, alternative device architectures to the standard single mesa device architecture can be examined. Three device architectures that can be researched as double mesa, triple mesa, and planar devices in relation to surface leakage current. Within this body of work, both double mesa and planar devices have been delved into.

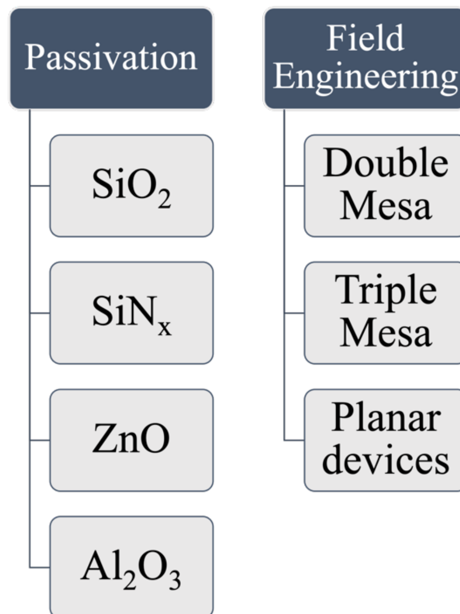

Figure 5. Potential Solutions to Reducing Surface Leakage Dark Current in APDs.

1.8 Research Methodology and Dissertation Organization

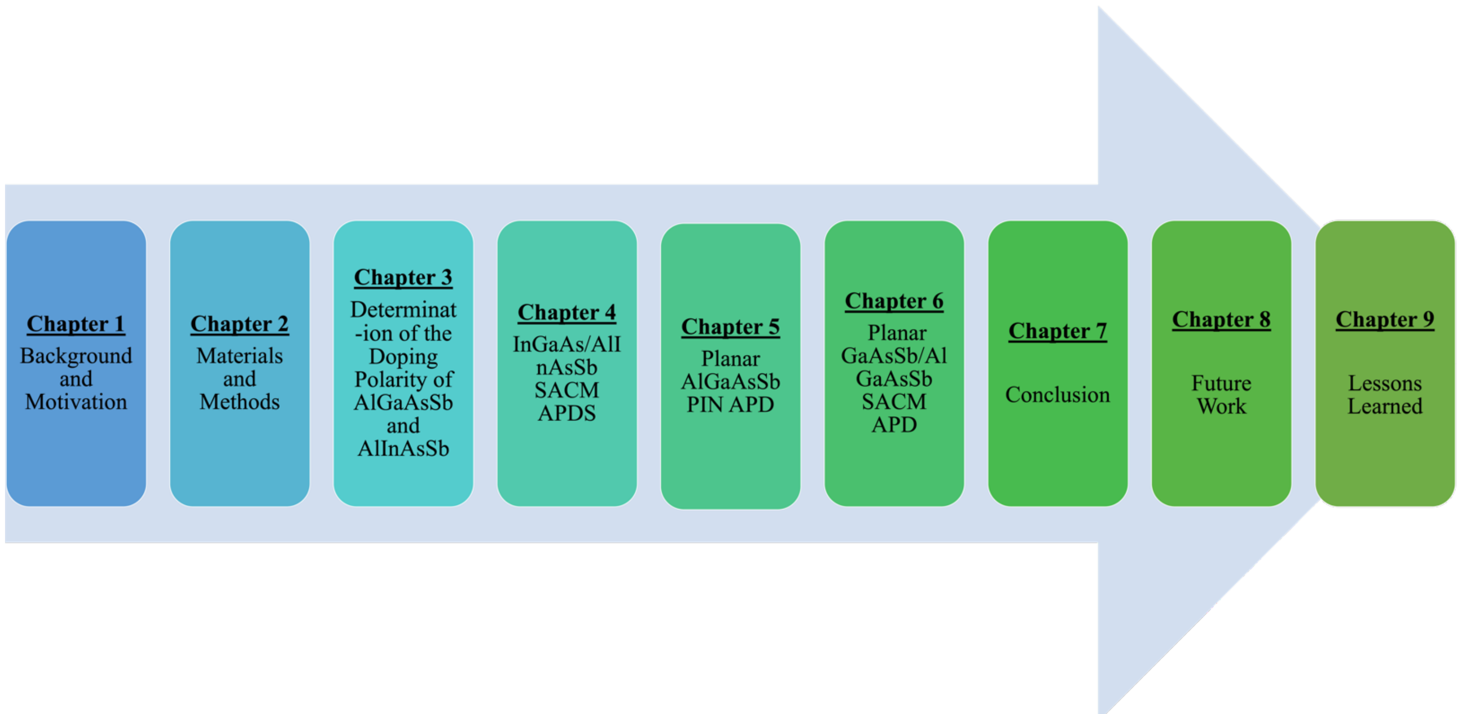

Figure 6. Thesis Organization comprised of nine chapters

As shown in Fig. 6, this body of work has been divided into nine chapters. Chapter 1 discusses the background and motivation behind the research and development of novel APDs for infrared detection applications. Chapter 2 discusses the materials of interest, research life cycle, and the characterization setups for determining APD performance. Chapter 3 investigates double mesa AlGaAsSb and AlInAsSb p-i-n structures on InP substrates to determine the background doping polarity for improved SACM designs employing these multiplier materials. Chapter 4 will discuss the first reported

InGaAs/AlInAsSb SACM APDs on InP substrates. The following two chapters, Chapter 5, and Chapter 6, will cover investigations of planar AlGaAsSb on InP substrates and GaAsSb/AlGaAsSb SACM APD on InP Substrates, respectively. Chapter 7 will then provide assessments of the work undertaken in Chapter 3 through 6 and their potential impact to the scientific community. Chapter 8 will lay the groundwork for future follow-on work that can be investigated. Finally, Chapter 9 will note the lessons learned throughout my Ph.D. journey, both from a technical and nontechnical perspective.

1.9 Contribution of this work

The work outlined and discussed in this dissertation helps move the needle forward to achieving high performing Sb-based III-V APDs by investigating methods to reduce the surface dark current that inhibits high voltage operation to leverage maximum gains, thereby achieving high sensitivity. This is accomplished via determinations of the background doping polarity of two Sb-based multipliers of interest, AlInAsSb and AlGaAsSb which can be utilized to further improving electric field design across complex SACM APDs, thereby staving off high dark current to achieve high gains. This investigation was then implemented to demonstrate the first InGaAs/AlInAsSb SACM APD on InP substrates ever reported that depicted high temperature stability across a variety of temperatures of interest. With this work, InGaAs/AlInAsSb SACM APDs can be employed many different applications at high operating temperatures. Another Sb-based SACM structure which has shown promising results and was investigated is a GaAsSb/AlGaAsSb SACM APD. This work has investigated planar processing of the high

performing structure to mitigate surface edge breakdown and achieve high gain performance through investigations of Zn-diffused planar AlGaAsSb p-i-ns as well as Zn-diffused planar GaAsSb/AlGaAsSb SACM. This is the first reported investigations of Zn-diffusion into these materials in efforts to realize fully planar devices and remove undesirable surface leakage current arising from the nanofabrication process. Furthermore, the first demonstration of floating guard rings was showcased in investigations of the planar GaAsSb/AlGaAsSb SACM APD, which will be critical to employ as work moves towards planar architectures.

Chapter 2. Materials and Methods

Chapter 2 of this work will focus on the materials and methods of this research. First, it will be discussed why the materials selected are of interest for infrared detection applications, the research process that is required to design, develop, and demonstrate high performing APDs, and then the characterization measurements and techniques implemented to inform device behavior. Through this, subsequent structures can be designed, epitaxially grown, fabricated, and tested to meet or exceed the specifications set by the project and achieve improved performance consistently.

2.1 III-V Materials for SWIR Avalanche Photodiodes

III-V materials have been implemented for a variety of applications, including APDs for infrared detection. This is because they have similar lattice constants to those of commercial substrates that enable seamless lattice matching during the growth process in addition to having favorable bandgap energies that detect a variety of wavelengths across the infrared spectrum.

The first consideration made for developing an APD is the required performance metrics, user or customer specifications or the application's requirements. Once these and a targeted wavelength are established, materials are considered for the APD. To determine the required band gap energy of a III-V material for targeting a specific wavelength, an

approximate value can be obtained by using a derivation of the Planck-Einstein relation whereby

$$\lambda_c\ (\mu m) = \frac{1.2398}{E_g\ (eV)} \qquad (8)$$

In Eq. 8 , λ_c is the cutoff wavelength in µm, and E_g is the material's bandgap energy in eV[64]. Once the bandgap energy of the material is selected for the infrared wavelength, materials can be considered and narrowed down. Materials of interest should also be selected to have similar lattice constants to the substrate to maintain crystalline quality, easing the growth of the structure and reducing the likelihood of defects to impact performance. Figure 7 shows lattice constants and bandgap energies for III-V semiconductors across the infrared spectral range at room temperature. Key substrates that are typically selected are in bold in the figure. It can be noted that while GaAs, InP, GaSb, and InAs substrates are all available, the prices differ significantly for each of these substrates. This work has selected InP as the substrate choice, since it has been significantly cheaper than GaSb and InAs historically for large 6" wafers. This is attractive since it provides an easier and more cost-effective path towards potential commercialization of the technologies.

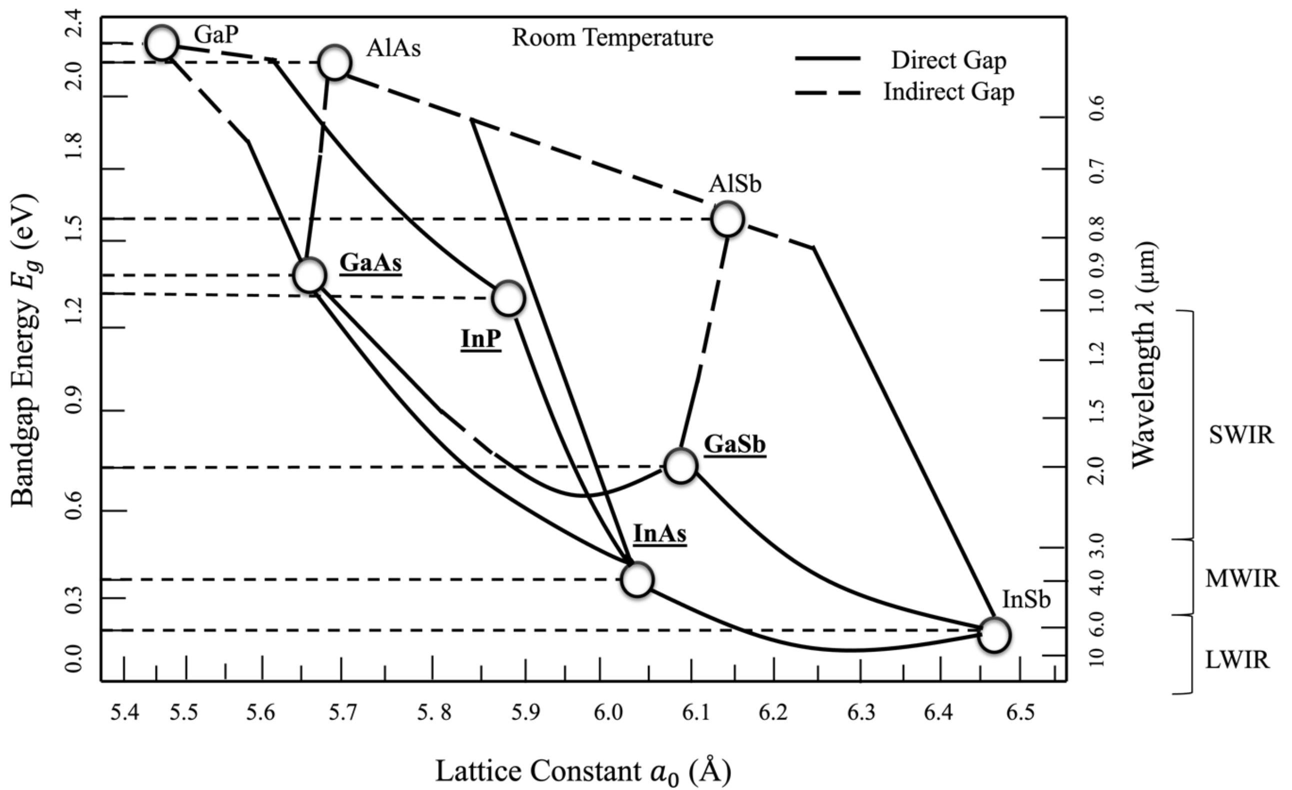

Figure 7. Lattice constants, and bandgap energies for III-V semiconductor materials across the infrared spectral range[65,66]. The figure depicts the short-wave infrared (SWIR), mid-wave infrared (MWIR), and long-wave infrared regimes at room temperatures. Available substrates that can be implemented for III-V materials are underlined and in bold.

This work has been investigating APDs for the short-wave infrared (SWIR) spectral range, which spans the 1-3 μm and is of interest for many different applications some of which include the detection of greenhouse gases in the atmosphere, notably methane and carbon dioxide, mapping of urban infrastructure, autonomous vehicle applications, defense, and other remote sensing applications[67,68,69]. With the SWIR range, 1.55 – 2 μm

has been of additional interest for many of these applications and lasers within this wavelength range may be considered "eye-safe", assuming reasonable power conditions for operation[70,71]. When considering semiconductor materials for infrared detection at 1.55 – 2 μm, popular APDs such as those that are Si-based cannot be implemented due to Si's cut-off wavelength being approximately 1.1 μm. HgCdTe-based APDs are one potential choice for the SWIR detection at this wavelength range due their ability to achieve high gains and excess noise close to unity[72,73]. Despite promising high performance, HgCdTe is not a suitable choice for many applications. This is because HgCdTe APDs may suffer with instability as a result of material nonuniformity and have low fabrication yields and high costs associated with them[74]. Furthermore, the low noise that can be demonstrated with HgCdTe APDs is limited to compositions close to $Hg_{0.5}Cd_{0.5}Te$, where the bandgap is narrow. At the narrow bandgap energy of $Hg_{0.5}Cd_{0.5}Te$, the dark current is high when operating at high temperatures. This limits the operation of HgCdTe APDs typically to 77 K and come at the cost of significant cryogenic cooling, thereby increasing the overall SWaP-C of the system[75]. Due to these challenges, III-V materials have been considered for infrared detection and implemented for APDs. As mentioned above, considerations are undertaken depending on the wavelength of interest, the lattice matching to the substrate of interest and project specifications among others when selecting the III-Vs.

Since the focus is on detection at 1.55 – 2 μm, materials must be selected that have the appropriate narrow bandgap energy. Two typical III-V materials selected for this are InGaAs and GaAsSb and can serve as the absorber region in more complex SACM APDs.

$In_xGa_{1-x}As$ has been a popular choice for commercially available APDs at 1.55 µm due to the favorable bandgap energy that can be tuned to span the near infrared (NIR) to the MWIR, demonstrated low noise and high responsivity, fast rise and fall times, and operability at room temperatures, enabling them to be an attractive option in low-cost applications[76,77,78]. $In_{0.53}Ga_{0.47}As$, which translates to a bandgap energy of 0.73 eV, is an attractive composition for 1.55 µm detection and can be lattice matched to InP substrates[79]. InGaAs/InP have been widely developed commercially from companies such as Laser Components, Excelitas Technologies, and Hamamatsu for 1.55 µm but InGaAs has a high k-value of ~ 0.4 - 0.5 and an absorption coefficient of ~ 10^4 cm^{-1}, which translate to higher excess noise for the APDs and limited speeds for operation[80,81,82,140,141,142,143]. Due to this, alternative materials have also been explored for SWIR detection. One of these is GaAsSb, as it can be lattice matched to InP substrates and can absorb wavelengths up to 1.6 µm[83,61,58]. $GaAs_{0.5}Sb_{0.5}$ may also provide benefits over $In_{0.53}Ga_{0.47}As$ for 1.55 µm in more complex SACM structures as an absorber material, as it has less bandgap discontinuity with a multiplier material of interest, AlGaAsSb. From a performance perspective, this provides easier transport of carriers, minimizes opportunities for trapping and thereby achieving high speeds. From a growth perspective, it provides ease in band grading between the GaAsSb absorber and the AlGaAsSb multiplier, all while remaining lattice matched. This attractive over $In_{0.53}Ga_{0.47}As$, which has a large conduction band offset that requires careful considerations in designing complex SACM APDs.

It is very challenging to develop a single material APD that meets or exceeds all key figures of merit to achieve high performance at the intended wavelength. This motivates SACM heterostructure designs to be implemented instead, which provides optimization of each layer independently of one another to improve the structure overall. The two materials introduced above, InGaAs and GaAsSb, are implemented into the SACM as the absorbers, due to their lower bandgap energies, capable of 1.55 µm detection. To initiate sufficient impact ionization of carriers and maximize the achievable gains, wider bandgap Sb-based quaternary materials are selected as the multipliers. Two Sb-based materials selected as multipliers are AlGaAsSb and AlInAsSb. AlGaAsSb has recently been investigated as a p-i-n APD structure with a thick multiplication layer > 900 nm to leverage the impact ionization process to increase gains and can be grown as either a digital alloy (DA) or random alloy (RA)[43,44]. This is advantageous from a design and growth standpoint because RA growths are easier than DA growths. By demonstrating high performance potential for either growth type, AlGaAsSb can be implemented for a wide variety of SACM designs. In addition to growth flexibility, AlGaAsSb has shown that it can achieve low excess noise characteristics on InP substrates[47,48,84]. When AlGaAsSb is implemented into an SACM design, it can be used with either InGaAs or GaAsSb as the absorber material, although GaAsSb lends itself to easier designing due to conduction band and valence band grading flexibility and has achieved very high gains ~ 278, temperature stability, and low excess noise[58,60,61]. Despite this, SACM APDs with an InGaAs absorber layer and AlGaAsSb multiplier have been implemented for high-speed optical and

telecommunication applications, due to demonstrated high gain-bandwidth products up to 424 GHz and low dark current compared to commercially available InGaAs APDs[85,86,87].

The other Sb-based quaternary material of interest for 1.55 µm is AlInAsSb. AlInAsSb is unique as it is highly tunable to target not only the SWIR regime, but can be adjusted to target NIR, MWIR, and even the LWIR as well[45]. To target wavelengths within each of these regimes, the Al composition can be adjusted and cut off wavelengths of 1, 2, and 3 µm can be achieved with Al compositions of $x = 0.7$, 0.3, and 0.15, respectively as higher Al is correlated with a larger bandgap energy[88]. An Al composition of $x = 0.79$ is implemented in SACM APDs for 1.55 µm detection. AlInAsSb is attractive for SWIR as APDs employing the material have demonstrated low avalanche breakdown temperature dependence, indicating that the material is conducive to a variety of applications and exhibits high temperature stability[51]. Up until recently, AlInAsSb had been mostly restricted to GaSb substrates and had limited applications due to a wide miscibility gap, but this challenge has been resolved via growths within the miscibility gap if AlInAsSb is grown as a digital alloy of the constituent binaries AlAs, AlSb, InAs, and InSb[89,90,91]. Due to the tunability of the quaternary material, AlInAsSb can serve as both an absorber and a multiplier in SACM APDs by tuning the Al composition[59]. Very recently, $Al_{0.7}InAsSb$ has been employed in the first-ever SACM structure with an InGaAs absorber on InP substrates and illustrated low noise characteristics and strong temperature stability, showing potential for future telecommunication applications[92]. This work has reiterated the flexible nature in the design and applications of SACM APDs that use AlInAsSb material systems.

Table 1 shows the comparison of several reported Sb-based III-V SACM APDs employing AlInAsSb and AlGaAsSb alongside commercially available InGaAs APDs for their maximum gains, excess noise values and gain normalized dark current densities. From the table, is evident that Sb-based SACM APDs provide an advantage over commercially available APDs with respect to gain and excess noise, but at the tradeoff of higher gain normalized dark current densities which must be mitigated.

Table 1. Comparison of maximum gains, excess noise and gain normalized dark current density at the highest reported gains for various SWIR APDs for 1.55 μm detection at room temperature operation.

Avalanche Photodiode	**Maximum Gain (Excess Noise)**	**F(M=10)**	**Gain Normalized dark current density, J_d/M (A/cm^2)**
GaAsSb/AlGaAsSb SACM on InP Substrate[58,60]	132-278 (2.48 - 3)	1.52 - 2	5.72×10^{-4} – 1.52×10^{-2}
InGaAs/AlGaAsSb SACM on InP Substrates[84]	~110 (~2.94)	1.93	2.89×10^{-3}

InGaAs/AlInAsSb SACM on GaSb substrate[92]	17 (~2.1)	~2.2	3.33×10^{-3}
AlInAsSb/AlInAsSb SACM on GaSb substrate[59]	50 (~2.1)	~2	1.53×10^{-4}
Laser Components InGaAs APD IAG-200x[141]	20 (5.5)	3.2	1.59×10^{-5}
Excelitas InGaAs/InP APD (C30662)[144]	30 (3.4)	3.4	4.77×10^{-5}
Hamamatsu InGaAs APD (G8931-20)[143]	30 (~13)	~7	1.59×10^{-5}
Hamamatsu InGaAs APD(G14858-0020AA)[142]	30 (~13)	~7	2.12×10^{-6}

As highlighted in this section, there are two key absorber materials and two key Sb-based multiplier materials considered for 1.55 µm using III-Vs. The absorbers are InGaAs and GaAsSb and the Sb-based multipliers are AlGaAsSb and AlInAsSb. The grading and charge layers are determined once the absorber and multiplier is selected and adjustments are made in the compositions to ease bandgap transitions across the structure, promoting ease of electrons under sufficiently high reverse biases to achieve high performance.

2.2 Research Methodology

To develop high performing APDs, a systematic iterative approach is required. Figure 8 displays the design-to-demonstration life cycle of developing APDs. This life cycles first requires an initial heterostructure design which is based upon the project specifications and the APD performance requirements. As previously discussed, many APD heterostructure designs leverage the SACM structure to achieve infrared detection while maximizing gains and suppressing the tunneling dark current. In the design phase of an SACM APD, an initial design is selected using theoretical modeling to determine whether the structure is suitable. The design is iterated using theoretical modeling software tools, such as Silvaco, to determine sufficient material compositions, thicknesses, and doping concentrations of each layer for the intended application.

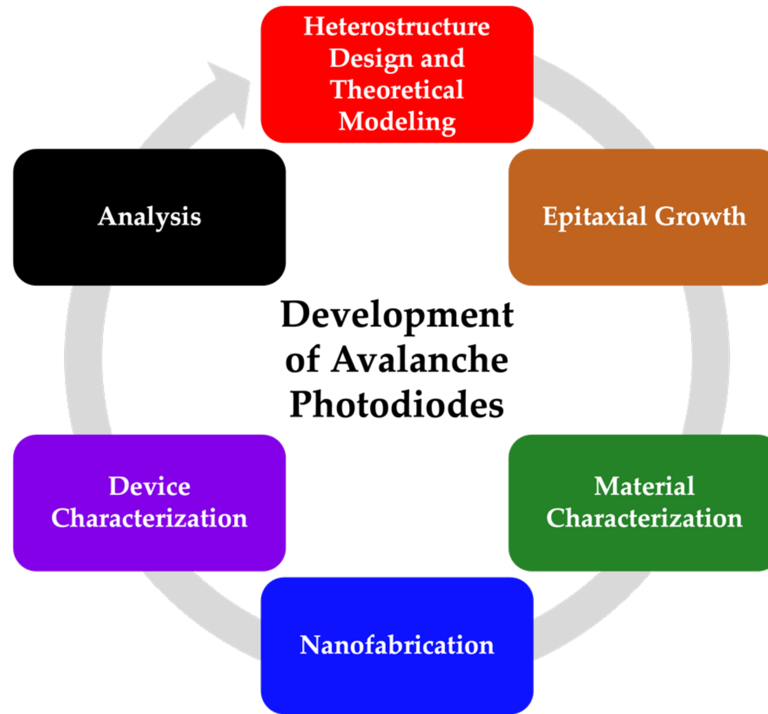

Figure 8. Design to Demonstration cycle for the development of high performing APDs. This process goes through stages of heterostructure design and theoretical modeling, epitaxial growth of the structure and subsequent material characterization, nanofabrication to delineate individual devices, device characterization and analysis.

Once the APD heterostructure has been finalized, the structure can then be grown either through Molecular Beam Epitaxy (MBE) or via Metal Organic Chemical Vapor Deposition (MOCVD). Both growth methods have their advantages and disadvantages, depending on the application and the best one should be selected[93,94,95,96,97]. Before growing the APD heterostructure, several calibration growths are completed first. Calibration growths provide a chance to ensure that the growth rate, growth temperature, targeted material

composition, dopant selection and concentration and other critical parameters are as accurate and as optimized as possible. This ensures that the grown heterostructure will be as close as possible to the finalized design selected and simulated. Once the growth is completed, the material is characterized to determine the quality of the growth and if it is adequate to go through subsequent steps in the life cycle. Material characterization measurements such as X-ray diffraction (XRD) and Nomarski microscopy are undertaken to determine whether extensive defects are present in the grown material and the quality of the growth at the material interfaces. Additional characterization measurements, such as photoluminescence spectroscopy or absorption coefficient and carrier lifetimes may also be measured at this stage as well. If the material characterization determines that the growth went well and defects are limited, the wafer is cleaved into smaller samples to undergo the nanofabrication process.

The nanofabrication process is the procedure by which individual pixels or devices are delineated from the epitaxially grown material. These devices are critical for subsequent characterization steps that will determine the performance of the detector. The nanofabrication process has three overarching steps: device definition, surface passivation, and metallization, which are broken down in Figure 9. In the device definition step for mesa architecture devices, the unprocessed epitaxially grown sample is first coated with a photoresist and then is exposed to light to pattern the material with a selected mask design via a maskless aligner (MLA). This process is known as photolithography. Once the exposure it completed, the sample is then etched, either through a wet or physical etching

process, to the bottom contact layer of the heterostructure. This etching step develops the mesa architecture of the device. After the mesa has been formed, the sample is cleaned, and the photoresist is removed to enter the surface passivation step of the nanofabrication process. The material then undergoes a passivation coat to treat the surface of the mesas and protect against oxidation, degradation and other unwanted interactions that may occur with the environment. From these, the sample is coated with a secondary photoresist, and patterned once more to fully realize the device features. Once the second photolithography is complete, the material is cleaned and prepared for the final component in the nanofabrication: metallization. During the metallization component, the sample is coated with resist that will enable lift off from unwanted areas of the sample, exposed again, and cleaned. Finally, a metallized stack is deposited onto the sample and then the sample goes through liftoff. In lift off, the areas that were coated with the lift off resist will remove unwanted metal to shown clean devices that are ready for testing.

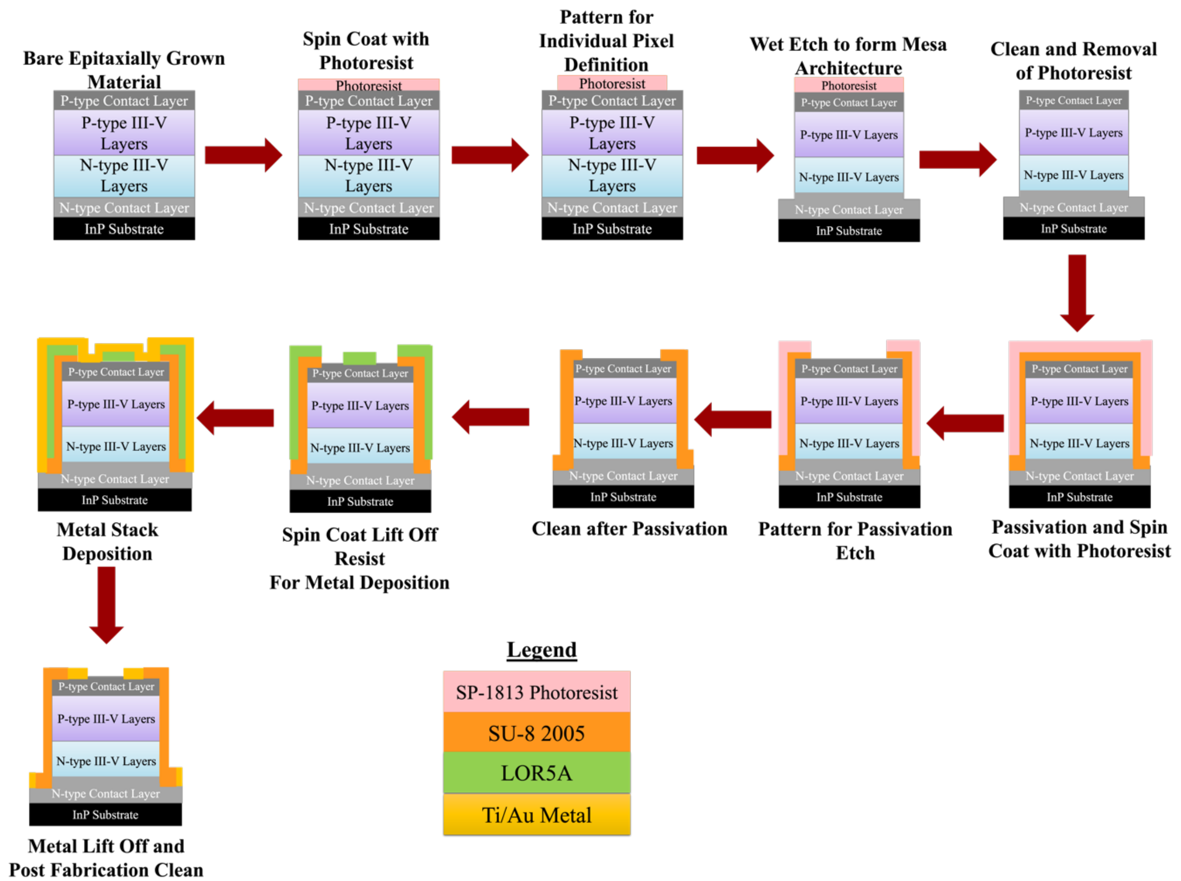

Figure 9. Nanofabrication procedure to develop mesa devices.

While the nanofabrication of planar diffused devices has some overlaps with that of the mesa devices, there are several steps that differ between the two. For planar diffused devices, the epitaxial material is first coated with a hard mask via chemical vapor deposition, then coated with photoresist and exposed to pattern the sample. The sample is then cleaned, and the hard mask is removed through a plasma etching process. Once the hard mask is removed, the photoresist is cleaned off and the sample is ready for the planar diffusion processes. First, ZnO is deposited onto the sample via an atomic layer deposition

(ALD) tool. The Zn atoms are then diffused into the epitaxial material in a diffusion furnace tube. Once this is complete, the sample is coated with a lift off resist and a photoresist, exposed once more and cleaned to finish delineating the area of each planar device. Finally, the sample is prepared for metallization where a metal stack is deposited onto both the front of the sample as well as the back. After both sides are coated with a metal stack, the sample is treated, and the metal is removed from areas that had the lift off resist. Fig. 10 shows the process of fabrication planar diffused devices.

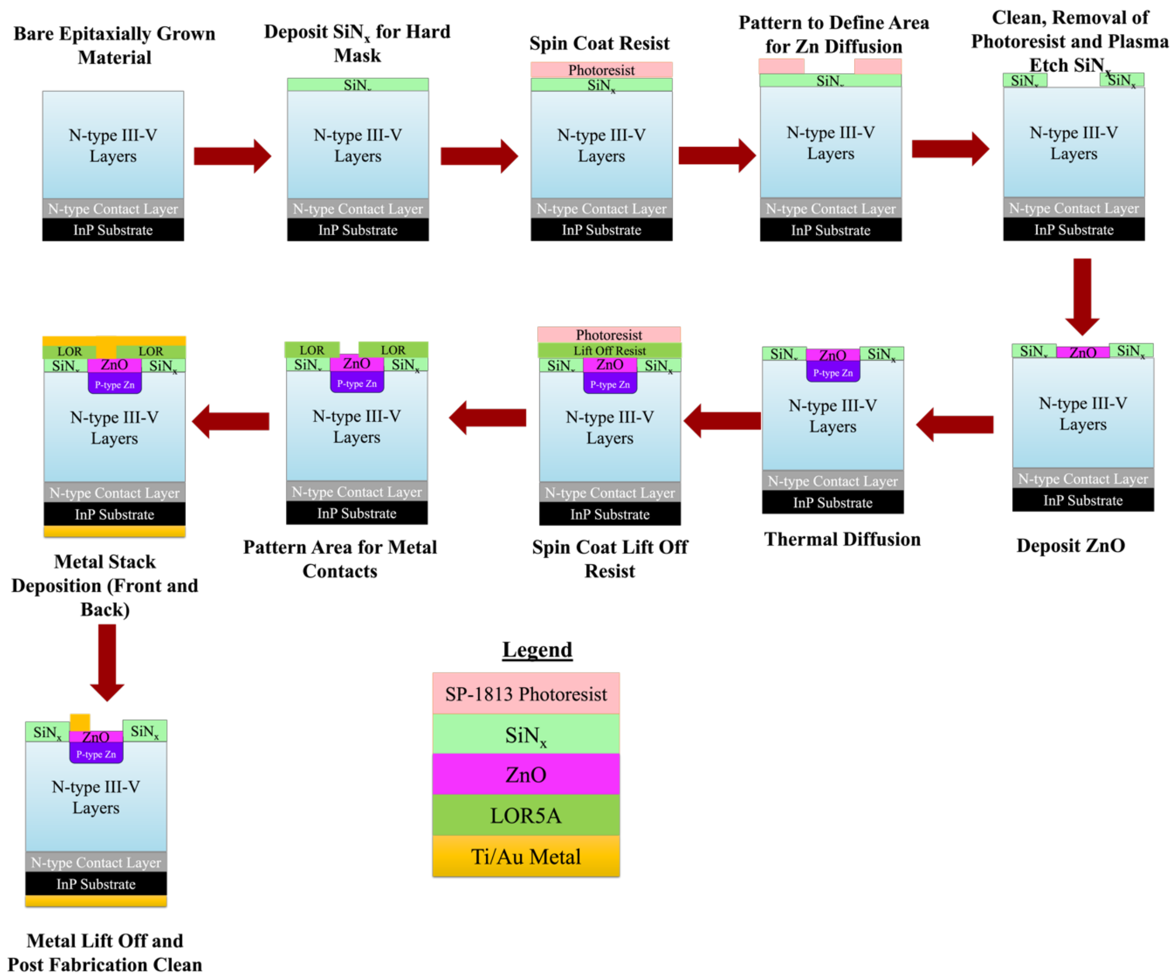

Figure 10. Nanofabrication procedure to develop planar diffused devices

After both types of nanofabrication, defined areas are formed to realize the individual devices. The exact shape and size of the devices is determined from the mask design and the masks designed implement circular devices that are less susceptible to high electric fields at corners that result in abrupt permanent device breakdown. Devices of various areas are developed to determine how the device area impacts performance. This is achieved

through a process called variable area diode analysis (VADA). Fig. 11 provides an image of devices fabricated of sizes varying between 60 µm and 500 µm in diameter.

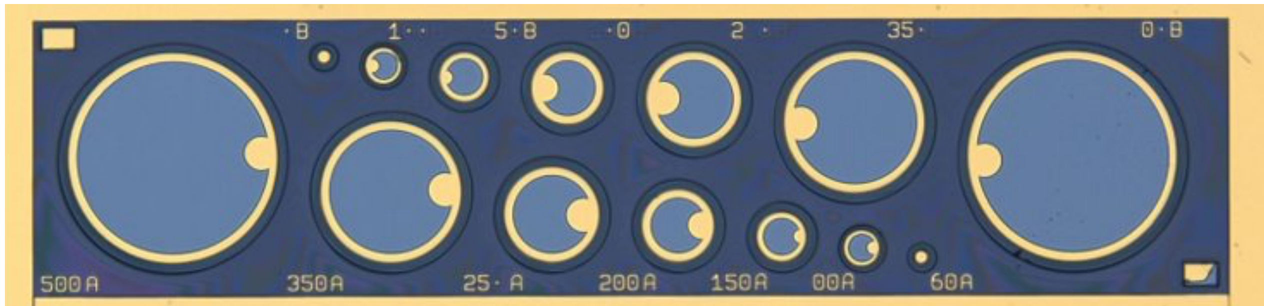

Figure 11. Variable area mesa diodes spanning from 60 µm to 500 µm in diameter.

The sample then enters the device characterization phase of the life cycle. In this stage, the devices are subjected to a variety of characterization measurements and techniques to quantify critical device performance metrics such as capacitance, dark current, maximum multiplication gain, excess noise, and series and contact resistance. These components are analyzed and determine the device performance. In this step, it is determined whether the performance meets or exceeds the requirements. If the device performance is not ideal, root cause analyses are performed to identify the component for poor device behavior. Through this, adjustments can be made in subsequent growths and nanofabrication processing to improve performance. Also in the analysis stage, additional simulations may be considered to further investigate issues with the structure.

2.3 Dark Current

During the characterization stage of developing high performing APDs, the first measurements implemented are dark current measurements. Dark current is a critical component of the overall noise of the detector, thereby lowering achievable SNRs and as a result, hindering detector sensitivity. If the dark current is high, then the power consumption of the LiDAR detector will increase, requiring heavy and costly cryogenic cooling equipment and may result in read-out challenges[63,98]. This, in turn, causes an increase in SWaP-C of the overall system. Due to this, heavy emphasis in the development of novel APDs revolves around the reduction of dark current as high dark current can result in premature breakdown, ergo limiting gains at the device level. Dark current can be defined as the inherent current a device will experience independent of the presence of photons to illicit a photoactive response in the detector.

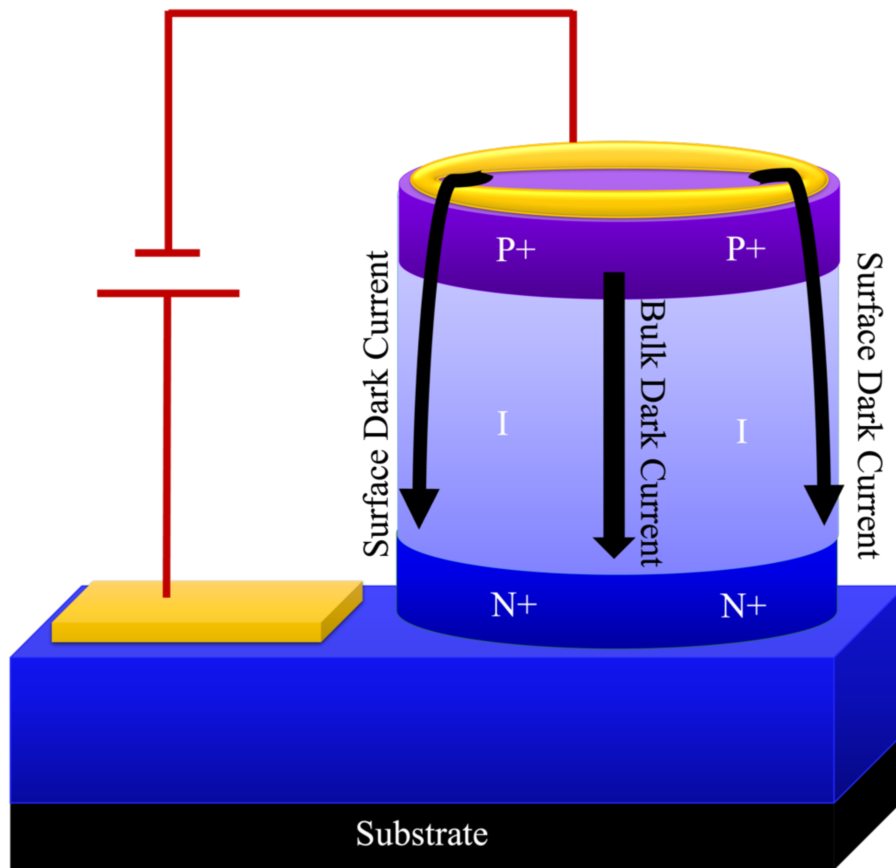

Figure 12. Representative p-i-n mesa device depicting bulk and surface dark current pathways under an applied bias.

Dark current arises from two different aspects of the detector; the epitaxial growth of the material and the following nanofabrication to delineate individual devices. Fig. 12 shows the two pathways the dark current can take in the form of bulk dark current and surface dark current through a p-i-n representative mesa device. The dark current that arises during the growth process is known as bulk dark current and the dark current produced

during the nanofabrication processing is known as surface dark current. The total dark current can be represented in the equation below as

$$I_{total\ dark} = I_{bulk} + I_{surface} \qquad (9)$$

In Eq. 9, $I_{total\ dark}$ is the total dark current the device experiences, I_{bulk} is the bulk dark current and $I_{surface}$ is the surface dark current. As mentioned, bulk dark current arises during the epitaxial growth of the material, the materials selected, how well they are lattice matched, and through the presence of any defects that may be introduced during the growth process. Surface dark current arises during the etching process of the nanofabrication to realize individual devices through a mesa architecture. Surface dark current can be seen as having three different origins in the APD from fabrication. During the etching process, either through physical etching or wet etching, the material is stripped away at the mesa sidewalls. At the crystal level, notches can be exposed at the sidewalls during etching. Additionally, etching produces unsatisfied dangling bonds at the interface of the epitaxial material and the surrounding environment. The unsatisfied bonds become satisfied with nitrogen and oxygen in the environment, coating the structure in a native oxide layer. This native oxide layer is problematic as it develops impure conductive bonds. At the device level of the APD, device experiences Fermi level pinning due to the conductive native oxide layer. The Fermi level pinning occurs close to the conduction band of the APD and causes band bending to occur. Electrons will accumulate in this region but become confined, through a two-dimensional electron gas (2DEG). Finally, at the circuit level, the

surface of the device serves as a low resistive path that current can be driven through, in parallel with the bulk of the device itself. This low resistive path causes the current to increase for the APD. Fig. 13 depicts each of the perspectives for surface dark current origins in an APD.

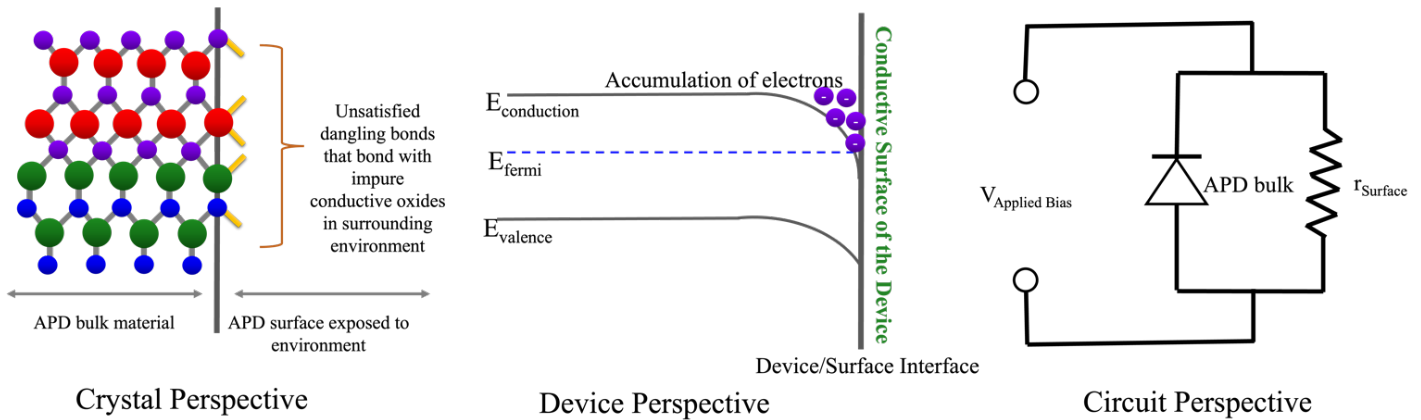

Figure 13. Surface dark current origins in an APD at the crystal, device, and circuit level[99,100]

It is necessary to determine whether the bulk dark current or the surface dark current dominates the device to mitigate it and achieve high performance at larger biases. Quantifying the bulk and surface dark current is achieved via a variable area diode analysis (VADA), by which circular mesa devices can be measured for their current-voltage characteristics across varying of device diameters. Because the surface dark current has a relationship with the perimeter of the device and the bulk dark current has a relationship with the area of the device, VADA provides a way to separate the two dark current

components. To perform a VADA, the following equation is implemented for each device at a given voltage of interest.

$$I_{dark\ current} = \pi r^2 J_{bulk} + 2\pi r J_{surface} \qquad (10)$$

In Eq. 10, $I_{dark\ current}$ is the dark current value for a device at a given voltage, r is the radius of the device, J_{bulk} represents the bulk dark current density and $J_{surface}$ is the surface dark current density[101].

The dark current is comprised of many mechanisms that can be broken down. The total dark current density can be expressed as

$$J_{total} = J_{diff} + J_{BTB} + J_{TAT} + J_{GR} + J_{SH} \quad (11)$$

whereby J_{total} is the total dark current density, J_{diff} is the diffusion dark current density, J_{BTB} is the band-to-band tunneling dark current density, J_{TAT} is the trap assisted tunneling dark current density, J_{GR} is the generation-recombination dark current density, and J_{SH} is the surface dark current density. The bulk dark current mechanisms are diffusion current, band-to-band tunneling current, trap-assisted tunneling current, and generation-recombination current. Diffusion current, band-to-band tunneling current, trap assisted tunneling, and generation-recombination current are all bulk dark current mechanisms. The

diffusion dark current is produced when minority carriers diffuse towards the depletion region of the APD, transitioning from area of high carrier concentration towards lower carrier concentration. The diffusion dark current is produced through either Shockley-Read Hall (SRH), radiative or Auger generation. Band-to-band tunneling dark current arises when carriers tunnel quickly from the valence band to the conduction band of an APD. The trap-assisted tunneling dark current is like band-to-band tunneling but with addition of mid gap traps that serve as steppingstones for carriers to jump from the valence band to the conduction band. Generation-recombination dark current arises when electron-hole pairs are generated either optically or thermally. The surface dark current mechanisms impede APD performance. Unlike many of the bulk dark current mechanisms that have a relationship with temperature and can be reduced through cooled operation, surface dark current is not improved with cooling a device. The primary drivers of the surface dark current in devices arises from either surface related trap-assisted tunneling current or surface related diffusion current through SRH. Defect related surface dark current originates from the etching process of nanofabrication to delineate individual devices. The surface dark current density can be expressed as

$$J_{SH} = \frac{V_j}{R_{SH}} \qquad (12)$$

Where V_j is the effective applied bias, and R_{SH} is the shunt resistance.

To measure dark current and quantify the dark current as being dominated by either bulk mechanisms or surface mechanisms, current-voltage (I-V) measurements are undertaken. In general, I-V measurements are performed in a Lake Shore Cryotronics CRX-6.5K cryogenic probe station with a Keysight Technologies B1500A Semiconductor Device Parameter Analyzer. I-V measurements can also be completed as a function of temperature to further understand the dark current mechanisms as well as demonstrate the devices at the specific temperatures of interest. Current-Voltage-Temperature (I-V-T) measurements are performed in the same setup as ambient I-V measurements, with the addition of an HC-4E CCR Helium Compressor and a Lake Shore Cryotronics Model 336 Temperature Controller. This enables I-V-T to be performed between 8 and 300 K. I-V-T is implemented to determine the activation energy of device across a wide span of temperatures. This is accomplished through Arrhenius plots using

$$\ln(J_{dark}) = \ln(J_o) + \frac{E_a}{kT} \qquad (13)$$

In Eq. 13, J_{dark} is the dark current density, E_a is the activation energy, k is Boltmann's constant, T is the temperature. For an Arrehenius analysis, the dark current is plotted as a function of $1/T$ at voltages of interest and the slopes of the curve are extracted to determine the activation energies. If the extracted activation is approximately equal to the bandgap energy, then the APD is limited by diffusion dark current. If the extract activation energy is approximately half of the bandgap energy, then the APD is limited by

generation-recombination dark current. Finally, Arrhenius plots can also provide the recombination energy of the surface at small reverse biases and at low temperatures.

I-V measurements can also be implemented to determine the ideality factor of an APD. The ideality factor determines how close the diode aligns with an ideal diode and provides insight into what type of recombination the APD is experiencing. It is determined by first performing forward bias I-V measurements of an APD between 0 and 1 V and then using the equation below.

$$n = \frac{q}{2.3kT\frac{d(log_{10}I)}{dV}} \qquad (14)$$

In Eq. 14, n is the ideality factor, q is the electron charge, $\frac{d(log_{10}I)}{dV}$ is the change in current as function of the change in voltage across the forward biased region. Table 2 below shows the recombination types that are associated for different ideality factor values.

Table 2. Ideality Factor values and their respective recombination types for APDs.

Recombination Type	Ideality Factor	Description
SRH, band-to-band (low level injection)	1	Recombination limited by the minority carrier
SRH, band-to-band (high level injection)	2	Recombination limited by both the minority and the majority carriers
Auger	2/3	Two majority and one minority carriers required for recombination
Depletion region (junction)	2	Two carriers limit recombination

2.4 Multiplication Gain

From I-V measurements, the multiplication gain can be realized for an APD, which originates from carriers impact ionizing under high electric fields. When a high electric field is applied to an APD, the carriers accelerate through the structure when they gain enough energy. As they accelerate, they will collide with other carriers producing electron-hole pairs. The average distance an electron must travel before impact ionizing is represented as $\frac{1}{\alpha}$ and the average distance that a hole must travel before impact ionizing is represented as $\frac{1}{\beta}$. The ratio of electrons and holes and their respective impact ionization coefficients can be represented as a ratio given as Eq. 3. It has already been mentioned that

k, the impact ionization ratio between electrons and holes is a component to the excess noise factor and it is desirable to have k be as small and as close to 0 as possible. Having k be close to 1 indicates that neither carrier type is dominating the impact ionization and results in poor APD performance due to the high excess noise factor. If k is closer to 0, then one of the carriers is suppressed while the other dominates, thereby providing a reduction in circuit noise. When carriers impact ionize under an applied reverse bias, the overall current the APD devices experience will increase.

The gain that APDs can leverage is produced from the impact ionization of carriers occurring from incoming photon flux from an illumination source. I-V measurements that are done under illuminated conditions are considered photocurrent measurements. At low reverse biases, the photocurrent will increase as the electric field increases across the depletion region of the APD. Once the APD has been fully depleted, the photocurrent becomes relatively independent of the bias. Under high applied reverse biases, the photocurrent moves into the avalanche breakdown region, where the carriers gain sufficient energy to begin the impact ionization process.

The gain can be quantified through I-V measurements. First, I-V measurements are completed under no illumination to provide dark current characteristics across the voltage range of interest. Then the photocurrent measurements are undertaken, whereby I-V measurements are performed under illumination. Targeted illumination can be accomplished via a tapered fiber optical cable inside the Lake Shore Cryotronics CRX-

6.5K cryogenic probe station that be manually maneuvered to the device of interest and is connected to a Thor Labs benchtop multi-channel laser source. While it is known as a photocurrent measurement, the resulting measurement provides the summation of the dark current and the photocurrent and is viewed as the total current via Eq. 15 where I_{total} is the total current, I_{dark} is the dark current and $I_{photocurrent}$ is the photocurrent. From this equation, it can be determined that the photocurrent is the difference between the total current and the dark current.

$$I_{total} = I_{dark} + I_{photocurrent} \qquad (15)$$

Typically, the dark current and total current will track one another at low biases of an SACM APD until sufficient electric fields are reached, achieving the threshold electric field values, whereby punch-through will occur. From a device physics perspective, punch-through occurs when carriers can transport across the charge layer and is at a voltage where the depletion region extends from the charge layer to the absorber layer[102]. Prior to reaching the punch-through voltage and overcoming the threshold energy required to cause punch-through to occur, the charge layer will serve as a blocking barrier mechanism in the conduction band that holds electrons off from transporting. Once a sufficient voltage is reached, providing enough band bending, then the electrons can overcome the barrier.

Once punch through has been observed in the I-V measurements of a device, the unity gain point can be determined and is implemented to quantify the gain of the APD.

The unity gain point is the voltage at which the device is fully depleted before carriers start to impact ionize and gain is realized for the APD. As the unity gain point, the gain can be considered equal to one. The unity gain voltage can be determined in one of two ways. The first method to determine unity gain of an APD is to assess the I-V characteristics under illumination across the voltage range and note where the slope of the curve remains flat. This should ideally occur shortly after the punch-through behavior is completed. While this method provides quick assessment for unity gain, it may be less accurate then the second approach. The second approach implements capacitance-voltage (C-V) measurements and unity gain is measured as the voltage by which the device becomes fully depleted, and the capacitance values remain stable. C-V will be discussed in greater detail in Section 2.6, but it can be noted that C-V provides a more accurate approach to determine the unity gain via the depletion behavior of the device and may result in less errors as opposed to the I-V method. Determining the unity gain point correctly is vital to provide accurate gain values. If the gains are underestimated or determined incorrectly, then additional performance metrics are impacted such as the gain bandwidth product, excess noise factor and quantum efficiency[102].

After the unity gain point has been accurately determined, the gain of the APD can be measured using the equation below.

$$Gain, M = \frac{I_{photocurrent} - I_{dark}}{I_{photocurrent,unity} - I_{dark,unity}} \qquad (16)$$

In Eq. 16, $I_{photocurrent}$ is the current value of the photocurrent at the voltage of interest, I_{dark} is the dark current at the same voltage, $I_{photocurrent,unity}$ is the photocurrent value at the unity gain voltage, and $I_{dark,unity}$ is the dark current value at the unity gain voltage. The equation is then used to determine the gain values over the operating voltage range after punch through and can be plotted alongside the dark current and photocurrent I-V curves. Ideally, the gain curve should be exhibiting exponential like behavior. From this curvature, it is evident that the highest achievable gains occur at very high biases. At this voltage range, the benefits of an APD are leveraged significantly over p-i-n diodes for low photon detection and signal amplification.

It can be noted that although the above equation simplifies the gain calculation, there is gain associated both from the photocurrent and the dark current. The photocurrent gain can further be categorized as electron injection originating gain or hole injection originating gain. Under sufficiently high electric fields, both the electrons and holes are impact ionizing. Is the material is considered an electron APD, such that $\alpha > \beta$, then the gain is assumed to be dominated by the electron injection, due to the electrons having traveled the furthest "net distance" comparatively to achieve the highest gain[100].

Since gain is a calculation, no additional setups are required to determine the gain of a device if the photocurrent and dark current have been previously measured using the probe station, parameter analyzer, and laser. Figure 14 displays a representative I-V plot for a p-i-n device under dark and illuminated conditions for which gain could be calculated.

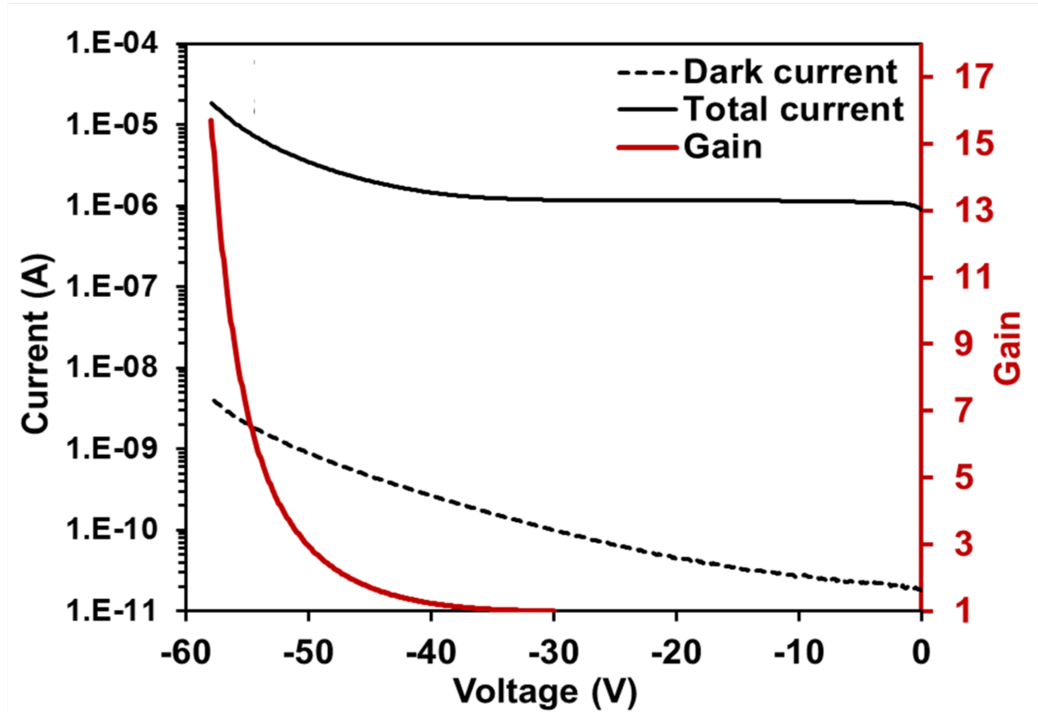

Figure 14. Example I-V behavior under dark and illuminated conditions for a p-i-n device for which multiplication gain is determined.

2.5 Breakdown Voltage and Temperature Variation

Section 2.4 discussed determination of the gain of an APD and how it is desirable to operate devices at as high of a voltage as possible to maximize gain. While this is

beneficial for maximizing sensitivity, voltage breakdown will eventually occur. The breakdown voltage, V_{Br}, is defined as the reverse bias voltage at which the gain goes to infinity or the $1/M$ goes to zero. The multiplication gain goes to infinity at a high voltage where a carrier will initiate the avalanche breakdown process via high enough energy that creates additional carriers via impact ionization. Once the device reaches this point, the APD is no longer operating in linear mode and is now considered to be in Geiger mode for operation where a single photon can rapidly increase the current via quenching. While the reverse breakdown is not inherently destructive to an APD, if the external circuitry does not limit the I*V_{Br} to less than the maximum power rating of the diode, then the device will die and will no longer be operable for additional measurements.

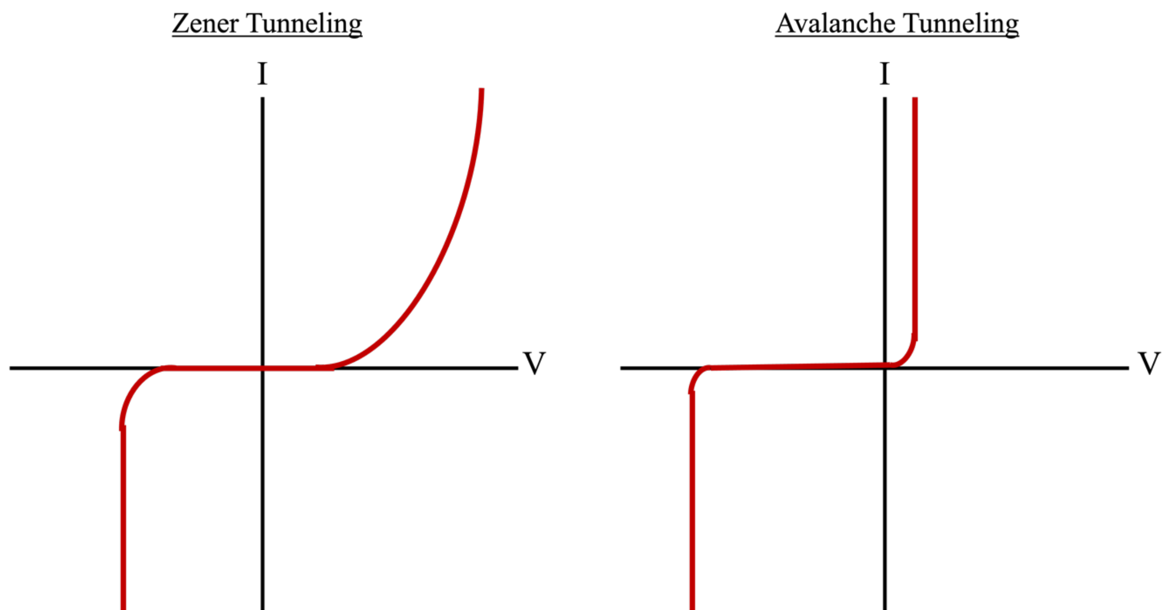

Figure 15. Linear I-V Characteristics of Zener and Avalanche tunneling mechanisms.

It is worthwhile to understand the type of tunneling that the APD is experiencing. There are two types of tunneling: Zener tunneling and Avalanche tunneling. The difference between the two mechanisms is in how the tunneling occurs. In the case of Zener tunneling, both sides of the p-n junction are heavily doped, and the depletion region is thin. When the device is biased over large voltages and is subject to high electric fields, the distance between the valence band and the conduction band at the band bending becomes very narrow, enabling electrons to tunnel across quickly. Zener tunneling also has a relationship with temperature that can be evaluated to understand device performance across the operating temperature range. As the temperature increases for an APD experiencing Zener tunneling, the breakdown voltage will decrease. This is represented as $\frac{\Delta V_{br}}{\Delta T} = -\nu_e$. In the case of Avalanche tunneling, the carriers crossing the depletion region of the p-n junction will be accelerated by the high electric fields between scattering events and will generate additional electron-hole pairs. The new electrons and holes generated will be accelerated by the high electric field until they are no longer in the depletion region. This is the same process as impact ionization. Avalanche tunneling is more likely to occur for larger bandgap materials where higher carrier acceleration is required to generate electron-hole pairs and results in a higher breakdown voltage. If the material is doped heavily, then the peak electric field will be larger, and the breakdown voltage will be reduced. Avalanche breakdown also has a relationship with temperature. As the temperature increases, the breakdown voltage of a device will also increase under Avalanche tunneling and can be described as $\frac{\Delta V_{br}}{\Delta T} > +\nu_e$. Fig. 15 shows the linear I-V behavior of devices both under Zener

tunneling and Avalanche tunneling circumstances. The figure displays that Zener tunneling will have a rounder onset while Avalanche tunneling will have a sharper onset.

Table 3. Zener and Avalanche tunneling mechanisms for voltage breakdown in APDs.

Characteristic	Zener Tunneling	Avalanche Tunneling
Band Diagram	Narrow bandgap materials	Wider bandgap materials
Temperature dependence	Increase in temperature lowers breakdown voltage	Increase in temperature increases breakdown voltage
I-V Profile	Rounded onset	Sharper onset
V_{Br} Location	Lower voltages	Higher voltages

To determine which mechanism is responsible for the APD experiencing sudden sharp increases in current, it is useful to assess breakdown voltage as a function of temperature. The temperature dependence for Avalanche tunneling in an APD can be represented as the temperature coefficient of avalanche breakdown voltage in the equation

$$C_{breakdown} = \frac{\Delta V_{br}}{\Delta T} \quad (17)$$

where $C_{breakdown}$ is the temperature coefficient of avalanche breakdown, ΔV_{br} is the change in the breakdown voltage, and ΔT is the change in temperature. It is desirable to have $C_{breakdown}$ be as small as possible, which indicates that the APDs have high temperature stability. This is attractive for device performance as it provides flexibility to operating temperature for the APD and demonstrates higher stability. If the APD has a strong temperature dependence, this complicates the optical receiver design, and subsequently increases the costs of the lidar system overall.

The breakdown voltage behavior of an APD is realized by taking I-V measurements, both dark current and photocurrent, at various temperatures that are consistently spaced. With the dark and photocurrent measurements, the gain can be calculated. From there, the inverse gain, $1/M$, can be fitted with the reverse biases and the breakdown voltages are determined as the intercepts. Following analyses are performed via linear fitting regression to determine $C_{breakdown}$ via $\frac{\Delta V_{br}}{\Delta T}$.

2.6 Capacitance-Voltage

Capacitance-voltage (C-V) measurements are another measurement implemented to provide useful information related to the semiconductor physics and the growth such as providing the depletion region width, unintentionally doped (UID) region carrier type and concentration as well as the built-in voltage. From device performance perspective, C-V

measurements determine the voltage at which the device has reached unity gain and multiplication gain can be accurately calculated which occurs once the device has achieved full depletion. Put simply, capacitance is defined as the stored charge over the voltage and can be expressed as

$$C = \frac{dQ}{dV} \qquad (18)$$

In Eq. 18, C is the capacitance, and $\frac{dQ}{dV}$ is the change in the stored charge as a function of the change in voltage. As the voltage is increased, the amount of stored charge also increases, resulting in a higher capacitance. This model for capacitance assumes a parallel plate capacitor. Naturally, a high capacitance indicates that the device is storing significant charge. This is problematic when integrated into a circuit, as a higher capacitance results in more charge required to change the voltage, resulting in increases in power consumption. Furthermore, larger capacitances can also distort the signal in high-speed operations and impact data acquisition.

As mentioned, C-V measurements are useful to determine the depletion width of the background carrier concentration of the UID region of a device. This is pertinent since the increases in the stored charge arises from the increase in the depletion width. The depletion width can be calculated from Eq. 19 below. In Eq. 19, N_A and N_D represent the concentration of acceptors and donors, V_{bi} is the built-in voltage, and $V_{applied}$ is the applied

voltage provided. When considering the case of a p-i-n device, whereby the intrinsic region has a much smaller doping concentration, the depletion region can be considered as one-sided to produce Eq. 20, where N_{UID} represents the carrier concentration of the unintentionally doped intrinsic region and A is the device area. From this equation, the built-in voltage can be extracted via plotting $\frac{1}{C^2}$ as a function of voltage and extrapolating the x-intercept[145]. To determine the N_{UID} concentration, the derivative of Eq. 20 can be taken with respect to voltage and results in Eq. 21[145]. In Eq. 21, ϵ_0 is the vacuum permittivity, ϵ_s is the dielectric constant of the semiconductor material. It can be noted that for Eq. 21 to hold, $V_{bi} > V_{applied}$ and under the circumstance that one-side of the p-n junction is doped significantly higher which is true for p-i-n devices[145].

$$W = \sqrt{\frac{2\epsilon(N_A + N_D)}{qN_AN_D}\left(V_{bi} - V_{applied}\right)} \quad (19)$$

$$\frac{1}{C^2} = \frac{2}{q\epsilon A^2 N_{UID}} \ (V_{bi} - V_{applied}) \ (20)$$

$$N_{UID} = \frac{2}{q\epsilon_0\epsilon_s A^2}\left(\frac{d(\frac{1}{C^2})}{dV}\right)^{-1} \quad (21)$$

$$W = \frac{\epsilon_0\epsilon_s A}{C} = \frac{\epsilon_0\epsilon_s \pi(D^2)}{4C} \quad (22)$$

Although Eq. 21 is useful for determining the UID doping concentration with respect to the voltage, it does not construe how the doping concentration relates to depth within the device, which may be more useful to provide feedback on the growth. The depletion width is related to the depletion width, as depicted in Eq. 22, whereby D represents the diameter of the device, in the case of circular devices.

In addition to the depletion width and the background doping concentration, it is helpful to also determine the polarity of the UID region which impacts the SACM design and its performance. A p-type UID region and an n-type UID region will require different doping concentrations of the charge layer in an SACM. If the background doping polarity remains unknown, it is likely that the SACM design will suffer and may not be optimized for peak APD performance. One possibility that may occur if the background doping polarity is unaccounted for is that the absorber layer's electric field may be higher than anticipated while the multiplier's may be lower than anticipated. This scenario would encourage the likelihood of tunneling to occur, drive up current quickly, reduce APD device operation, thereby impacting the achievable maximum and hindering SNR. Another possibility that could occur is the background doping polarity is not assessed is that the absorber layer's electric field is designed to be too low, and the multiplier's electric field is too high. In this instance, punch-through of carriers may not be suppressed sufficiently and could cause a low quantum efficiency.

The background doping polarity of an APD is influenced by the epitaxial growth process, specifically the material selected, crystalline structure of the material, and the presence of impurities that are introduced to the structure during the growth process. The polarity is also impacted by the method utilized to grow the alloy. The background doping polarity can be different for the same material between a random alloy growth and a digital alloy growth. One method of determining the background doping polarity of an APD is through performing C-V measurements on a double mesa structure. As the name suggests, a double mesa device structure has two mesas rather than one that is typically selected in a conventional nanofabrication process. The double mesa structure is produced via over etching and creates two junctions that can vary in area independently of one another. Of the two produced junctions, only one will be the p-n junction. The background doping polarity within the UID region will determine where this p-n junction resides, either at the junction of the top mesa or the junction of the bottom mesa. If the UID background polarity is n-type in nature, then the p-n junction will occur with top mesa junction and if it is p-type in nature, then it will occur with bottom mesa junction of a p-i-n APD. The capacitance scales with the p-n junction area and can be leveraged as a function of mesa diameter to locate the junction[103,56]. Fig. 16 illustrates a representative double mesa architecture of a p-i-n device. It is noted in this structure that the over etched region is typically a shallow etch into the UID region, anywhere from 50 to 100 nm in depth.

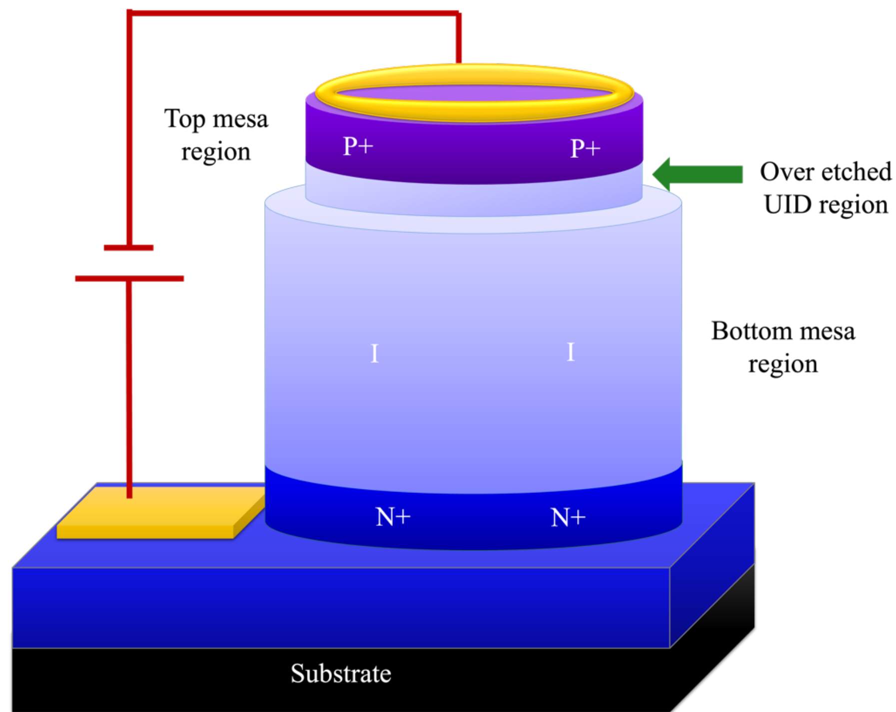

Figure 16. Double mesa architecture for p-i-n APD.

Fig. 17 shows the electric field profiles within a double mesa p-i-n diode and the locations of the peak electric fields if the UID region is n-type or p-type. If the UID region is n-type in nature, the peak electric field will occur at the p-n junction, which occurs near the top mesa and is shown as the deepest red gradients. As the distance away from the junction increases, the electric field profile will be lessened. Similarly, if the UID region is p-type in nature, then the p-n junction will occur near the bottom mesa. It can be noted that while the peak electric field will be at the p-n junction, the second junction may also have some nonnegligible impact. To illustrate the circuitry of the semiconductor junctions, the model below in Fig. 18 can be implemented. In this figure, the junction is represented as

a resistor in series alongside a resistor and capacitor in parallel. If there are two junctions in series, the total impedance for the entire device is shown as two of these models in series, of which one is the high field junction, and the other is the low field junction.

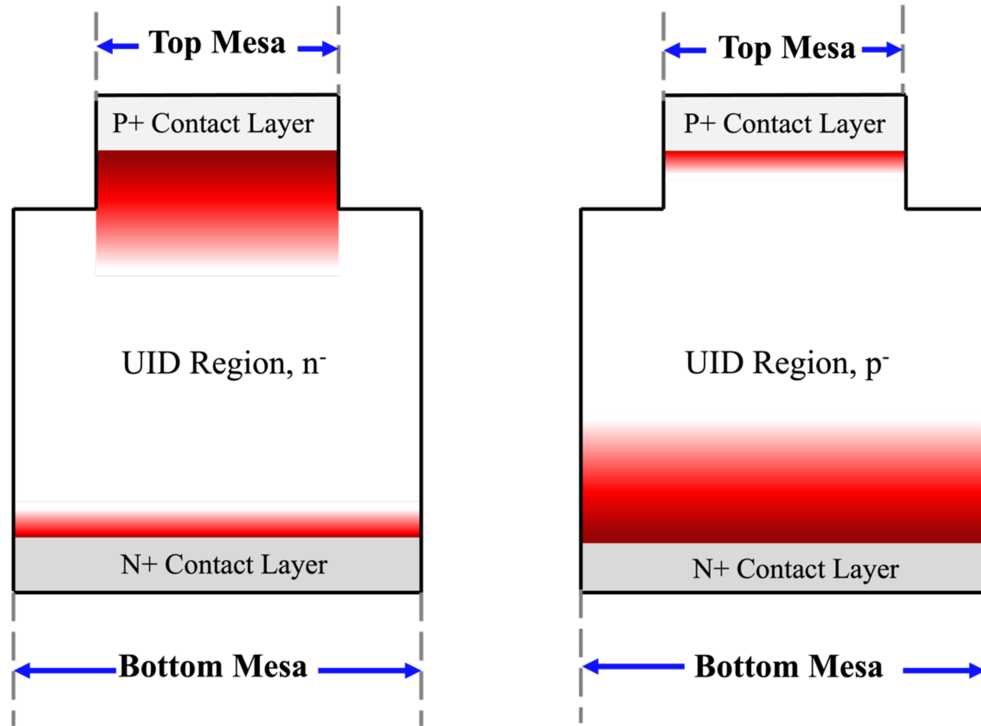

Figure 17. Electric field profile within a double mesa p-i-n diode with either an n-type UID region or a p-type UID region[56,57].

The subscripts below show the high and low field components as well as the components in parallel and series. This model results in non-unique solutions that do not differentiate between the high field and low field components. To circumvent this, capacitance can be considered for its relationship to the junction area, as given in Eq. 22.

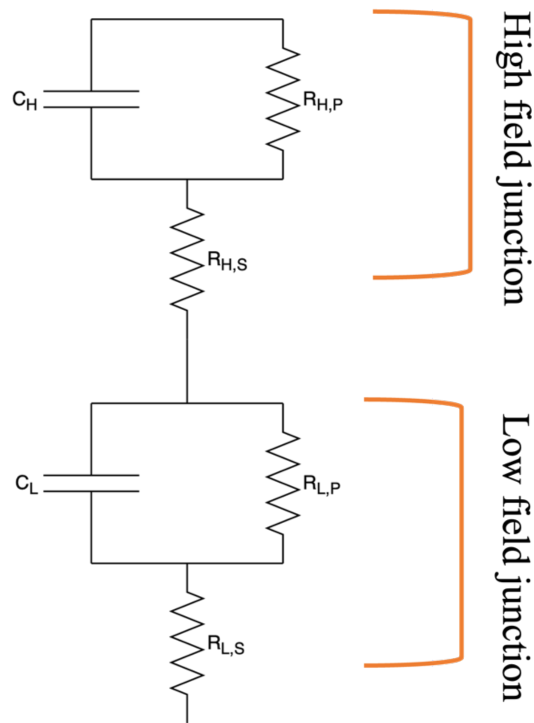

Figure 18. Impedance model for a double mesa p-i-n device[145].

All C-V measurements are performed in the cryogenic probe station and use the parameter analyzer with a built in CMU. Prior to device measurement, calibrations are undertaken to reduce any presence of parasitic capacitance and ensure accuracy. During the measurement, the frequency can be selected for using a C-*f* measurement to determine optimal value.

2.7 Quantum Efficiency

Another useful measurement that can be implemented to fully realize the APD performance and therefore the SNR is the quantum efficiency (QE). QE provides insight into how the device will perform at the specific infrared wavelength of interest and is determined from measuring the responsivity. The QE, also referred to as the external quantum efficiency (EQE) is defined as the effectiveness of the APD to convert incident photons into generated electron-hole pairs. The quantum efficiency can be expressed as

$$\eta = \zeta(1 - Reflectivity)(1 - e^{-\gamma x}) \qquad (23)$$

In Eq. 23, η is the QE, ζ is the ratio of the carriers that are collected versus the carriers that are absorbed, $Reflectivity$ is the reflectivity of the semiconductor, γ is the absorption coefficient of the semiconductor and is reliant on the provided wavelength, and x represents the thickness of the semiconductor material[104]. This equation can be further simplified, with the assumption that the semiconductor's reflectivity is essentially negligible, and that the ratio of carriers collects to the carriers that are absorbed is 100 %.

With these assumptions in mind the thickness of the semiconductor can be used to approximate the achievable quantum efficiency percentages. For instance, if the thickness of the semiconductor is 1/ γ, 2/ γ, 3/ γ or 4/γ, then the expected quantum efficiencies will be 65, 86.4, 95 and 98 %, respectively[100] . In ideal circumstances, quantum efficiency should be as high as possible, which is possible for the 3/γ or 4/γ thickness cases. While in theory, a thicker layer of material should improve quantum efficiency, additional considerations must be made for not only the absorber layer in the SACM but the entire structure overall.

The EQE of a p-i-n device can be written as Eq. 24 below were R_λ is the spectral responsivity, h is Planck's constant, c is the speed of light in a vacuum, λ is the wavelength, and q is the elementary charge constant. Since APDs can leverage gain, a follow-on equation is implemented, where the QE is multiplied with the calculated multiplication gain, as shown in Eq. 25 and is known as the gain quantum efficiency product.

$$EQE = \frac{R_\lambda hc}{\lambda q} \qquad (24)$$

$$Gain\ Quantum\ Efficiency\ Product\ for\ APD = QE * M \quad (25)$$

To measure the quantum efficiency of an APD, the responsivity of the APD is first measured. Responsivity is defined as the measurement of the electrical output to the inputted optical power as can be in units of A/W or V/W. To determine the responsivity,

several factors need to be known. These include the photon flux of the illumination source, wavelength of the illumination source, and whether the photon count is impacted by any external variables within the neighboring environment that could impede the photon count at the device under test (DUT). Responsivity can be determined using Eq. 26

$$Responsivity = \eta \frac{q}{hv} = \frac{I_{photocurrent}}{P} \qquad (26)$$

whereby v is the frequency of the radiation and is related to the velocity and the wavelength of the radiation, and P is the radiant power. The radiant power is calculated from $\emptyset$, the photon flux in Eq. 27.

$$P = \emptyset hv \qquad (27)$$

Typically, the photon flux is unknown and must be accounted for to obtain meaningful responsivity results. Two different setups can be implemented to determine the photon flux; a blackbody radiation source or via using Fourier Transform Infrared Spectroscopy (FTIR) and a monochromator. The second method has been implemented and requires calibrated detectors. The calibrated detectors have a known responsivity and calibrated photocurrent that is used in comparison to obtain the responsivity of the device under test.

$$Responsivity_{DUT} = Responsivity_{calibrated\ detector} * \frac{I_{photocurrent\ DUT}}{I_{photocurrent\ calibrated\ detector}} \quad (28)$$

Eq. 28 depicts the calculation to determining the responsivity of the device under test using the responsivity and the photocurrent of the calibrated detector at the wavelength of interest and the photocurrent of the device under test. The calibrated detectors are either HgCdTe (MCT) or Deuterated triglycine sulfate (DTGS) and can span into the mid infrared regime. Fig. 19 shows a block diagram schematic of the quantum efficiency setup. The DUT is placed in the cryostat and connected to the pins via a leaded chip carrier that wire bonds out devices to measure.

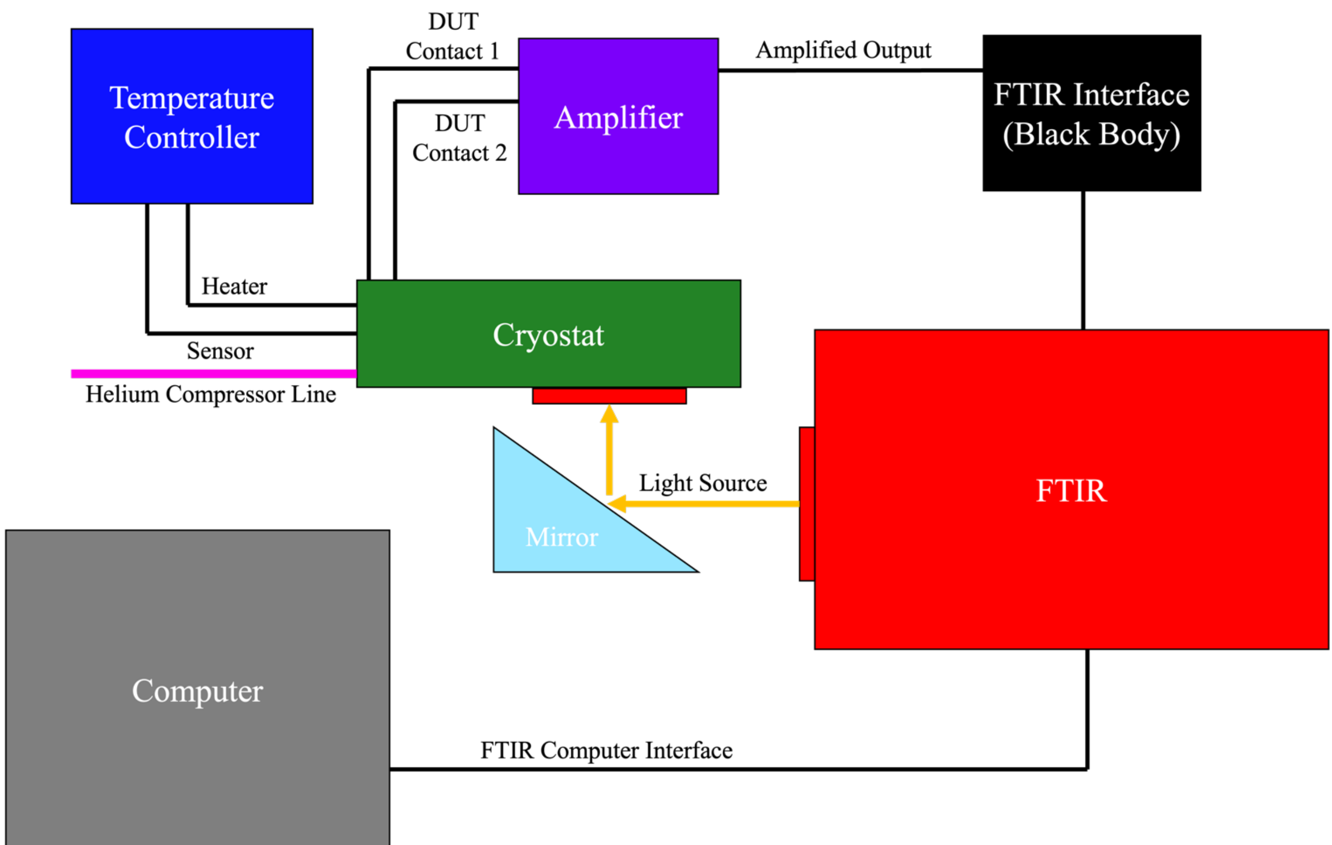

Figure 19. Block diagram of one of the commonly implemented setups for QE using an FTIR.

2.8 Excess Noise

The final measurement to discuss that is pertinent to quantifying APD performance is the excess noise. As defined in Eq. 5, Eq. 6 and Eq. 7, the excess noise factor is a contributor to the shot noise which originates from the random variation of the current forming carrier[105]. It is essentially a random process when photogenerated carriers are generated and the optical or thermal excitation in the p-i-n causes the current to fluctuate[106]. With the shot noise being a component of the noise, having high excess noise reduces the SNR overall and is undesirable.

While APDs can leverage the impact ionization process for gain, impact ionization is not a streamlined phenomenon. It is stochastic in nature, meaning that there is a general randomness to the process at which carrier impact ionize. The instability in the process does produce internal gain, but also introduces multiplication noise with it, known as the excess noise factor, $F(M)$, given as Eq. 2 . The excess noise factor can also be represented as the ratio of the standard deviation to the mean square value of the gain, M[107,108].

$$F(M) = \frac{\langle M^2 \rangle}{\langle M \rangle^2} \qquad (29)$$

If the assumption is made that the electric field is uniform, then McIntyre local field model can be harnessed and was expressed in Eq. 2 as $F(M) = k \cdot M + (1 - k) \cdot \left(2 - \frac{1}{M}\right)$ and the impact ionization coefficient ratio is given in Eq. 3 as $k = \frac{\beta}{\alpha}$. As mentioned in

Section 1.1., $\frac{1}{\alpha}$ is the average distance an electron will travel before impact ionizing and $\frac{1}{\beta}$ is the average distance a hole will travel before impact ionization begins under a sufficiently high applied electric field. The electron or hole must first reach the threshold energy required to impact ionize and the distance the carrier travels prior to achieving the threshold energy to begin impact ionization is called the dead space effect. Once impact ionization of carriers begins, the carriers will continue to accelerate until they collide with other carriers, thereby losing energy and creating a secondary electron hole pair. α and β can be quantified to determine the ratio of the impact ionization, k, and whether the APD is a hole APD or an electron APD. As the names suggest, a hole APD is an APD in which the hole carriers dominate the impact ionization process and an electron APD is an APD in which the electrons dominate the impact ionization process. It is ideal to have one carrier type dominate the impact ionization process as equivalent impact ionization of both electrons and holes produces a k of approximately 1 and is associated with poor APD performance due to a high excess noise factor. If k is closer to 0, this indicates that sufficient suppression of one carrier type impact ionizing is present and can assist in reducing the circuit noise. When designing an APD, it is worthwhile to first determine whether an APD is an electron APD or a hole APD. Electron APDs are more common than holes APDs since holes typically have a higher effective mass than holes thereby making it more difficult for them to accelerate enough to reach the threshold energy and start impact ionizing. To determine whether an APD is an electron or hole APD, α and β can be determined via Eq. 30 and Eq. 31.

$$\alpha = A_n \, e^{\left[-\left(\frac{B_n}{E}\right)\right]^{Cn}} \qquad (30)$$

$$\beta = A_p \, e^{\left[-\left(\frac{B_p}{E}\right)\right]^{Cp}} \qquad (31)$$

In the above equations, A_n, A_p, B_p, B_n, C_p and C_n are fitting parameters and E is the applied electric field[32,53,109]. From these equations, it is evident that the impact ionization coefficients have a relationship with the applied electric field. As a result, the impact ionization coefficients will differ with the intrinsic region thicknesses of epitaxially grown structures and under lower applied electric fields as opposed to higher electric fields[52]. In addition to this, impact ionization coefficients also have a dependence on temperature, with both α and β decreasing at approximately the same rate at which the temperature increases[110,111,112,113,114]. The impact ionization coefficients can be determined by first characterization the dark and photocurrent behavior of p-i-n and n-i-p structures. The gain can be extracted for both pure electron and pure hole injection across devices and then M^{-1} can be plotted as a function of the applied reverse bias. From there, the impact ionization threshold energies of both electrons and holes can be obtained and the coefficients can be quantified as a function of $1/E$ to determine the k value. The k value is dependent upon the material selected. As shown in Fig. 20 below, the k value has been determined for several materials as a function of increasing gains[104].

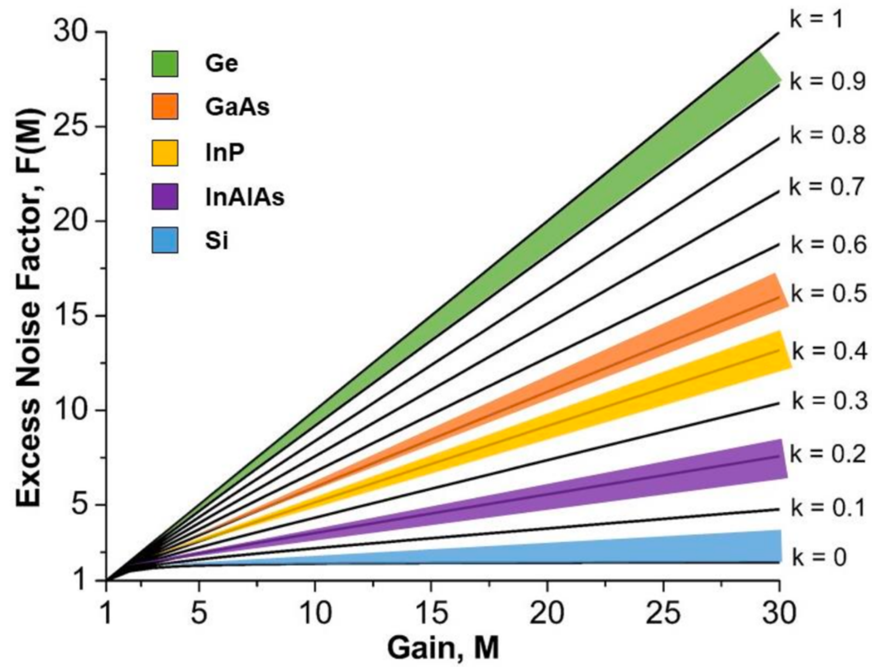

Figure 20. Impact Ionization coefficient ratio, k, for material systems of interest for APDs[104]

The excess noise factor, $F(M)$, can be measured for an APD using a noise figure meter, a source meter unit, and a HeNe gas laser to determine the photocurrent. A Hewlett Packard HP 8970B Noise Figure Meter is implemented to measure the noise power at a given frequency. Prior to measuring the noise power, calibrations are undertaken to account for unintended noise. The calibrations are completed using a HP 346A calibrated noise source and reference information for the calibrated noise source. Once calibrations are complete, the measured noise power from the noise figure meter can be implemented to determine the noise power density given as Eq. 32 and Eq. 33.

$$Noise\ Power\ Density = -174\frac{dBm}{Hz} * 10^{Measured\ Noise\ Power/_{10}} \quad (32)$$

$$Noise\ Power\ Density = 4.0474 * 10^{-21}\frac{W}{Hz} * 10^{Measured\ Noise\ Power/_{10}} \quad (33)$$

For the laser, a Meredith-Instruments 2 mW power 543 nm HeNe free space laser is implemented, and the light is focused onto the device under test (DUT) using a microscope objective. The sample is placed on the sample stage and DUT is selected for electrical probing using a GS or GSG probe. Once the setup is prepared for measurements, the dark current characterization is completed to determine the voltage range and resolution for the excess noise measurements at which gain is evident. The noise power versus bias voltage is also determined under dark conditions for the DUT. Once determined, the photocurrent is measured using the laser at the unity gain point and the noise power versus bias voltage is measured again until all key biases of interest have been measured. From here, the Avalanche free noise power density can be determined from the difference between the total current (or photocurrent) measurements and the dark current measurements. Avalanche Free Noise Power Density is given below as Eq. 34. The Gain vs. Voltage behavior can also be extracted using Eq. 35.

$$Avalanche\ Free\ Noise\ Power\ Density = 2qR * I_{Avalanche\ Free\ Photocurrent} \quad (34)$$

$$Gain = \frac{I_{Measured\ Photocurrent}}{I_{Avalanche\ Free\ Photocurrent}} \quad (35)$$

After the gain, the photocurrent noise power density and the Avalanche free noise power density are identified, the excess noise as a function of the applied bias can be determined using Eq. 36. Once the excess noise behavior is identified for the material as a function of bias, excess noise factor as a function of increasing gain can be determined.

$$Excess\ Noise = \frac{Photocurrent\ Noise\ Power\ Density}{Gain^2 * Avalanche\ Free\ Noise\ Power\ Density} \qquad (36)$$

Chapter 3. Determination of Unintentionally Doped AlGaAsSb and AlInAsSb

In Section 2.6, C-V measurements were introduced as a method to determine the depletion width, unity gain, background carrier concentration, and the background carrier polarity for APDs. In this chapter, C-V measurements were investigated for two high performing multipliers, AlGaAsSb and AlInAsSb, that are implemented into III-V SACM APDs. When designing multipliers for SACM APDs, it is critical to understand the background doping polarity of the materials to achieve optimal performance. To further improve the SACM designs, the background doping polarity of $Al_xGa_{1-x}As_ySb_{1-y}$ and $Al_xIn_{1-x}As_ySb_{1-y}$ p-i-n were investigated using the double mesa approach.

The advantage of this method to determine the background doping polarity of materials is threefold as opposed to other methods that can be implemented, which typically include Hall measurements, electrochemical capacitance-voltage (ECV) and secondary ion mass spectrometry (SIMS)[115,116,117,118]. Firstly, this method of measurement enables C-V measurements to be completed independent of the substrate. Secondly, this method of measuring the sample to determine the background doping polarity is nondestructive to the sample and the devices, providing repeated measuring capabilities to obtain additional data. And lastly, the double mesa C-V method of determining the background doping polarity is relatively simple to perform, which may improve accuracy and higher quality of the acquired data.

3.1 Design

As previously discussed, the background doping polarity of a material is pertinent to realize to improve performance when applied into an SACM APD design. In this investigation, two p-i-n structures were grown to fabricate double mesa devices for C-V measurements with the top and bottom mesa varying independently of one another. This enables the determination of the p-n junction location, ergo determining whether the unintentionally doped region is p-type or n-type in nature for both random alloy AlGaAsSb and AlInAsSb.

Two p-i-n structures were first designed using Silvaco TCAD software to determine the required material compositions, layer thicknesses, and doping concentrations within each layer, prior to growing the material. Using the software, the band diagram and electric field were simulated both at 0 V and at -20 V. Fig. 21 and Fig. 22 show the band diagram and electric field profile for the AlGaAsSb p-i-n at 0 V, respectively. Fig. 23 and Fig. 24 show the band diagram and electric field profile for the same structure when a reverse bias of -20 V is applied. From the iterated Silvaco simulations shown below, a finalized AlGaAsSb structure was selected that had two InGaAs contact layers that sandwiched the AlGaAsSb p-i-n structure with 300 nm of the p-doped region, 100 nm of the n-doped region and a 910 unintentionally doped (UID) region in the middle.

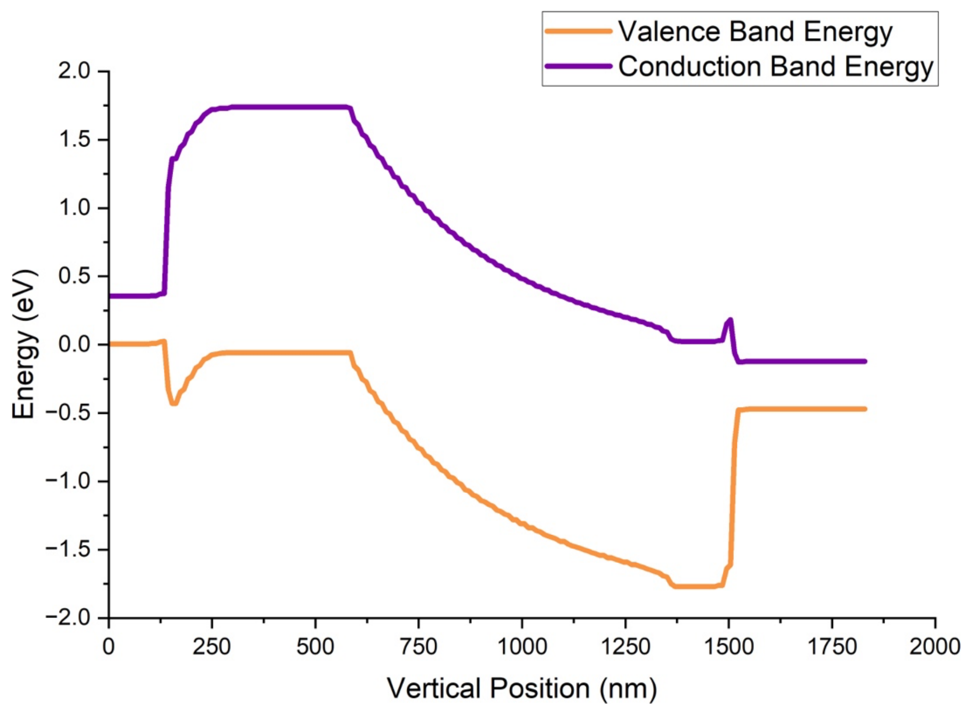

Figure 21. Simulated band diagram for AlGaAsSb p-i-n at 0 V.

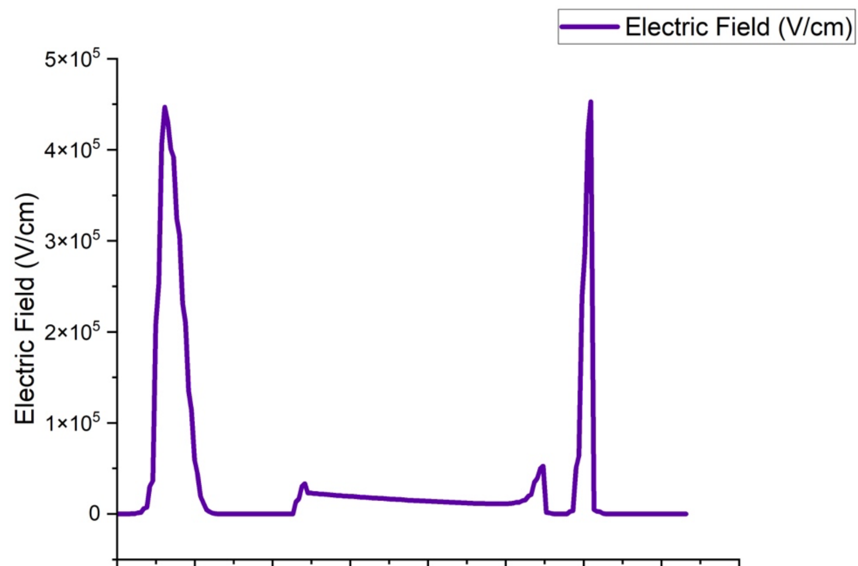

Figure 22. Simulated electric field profile for AlGaAsSb p-i-n at

0 V

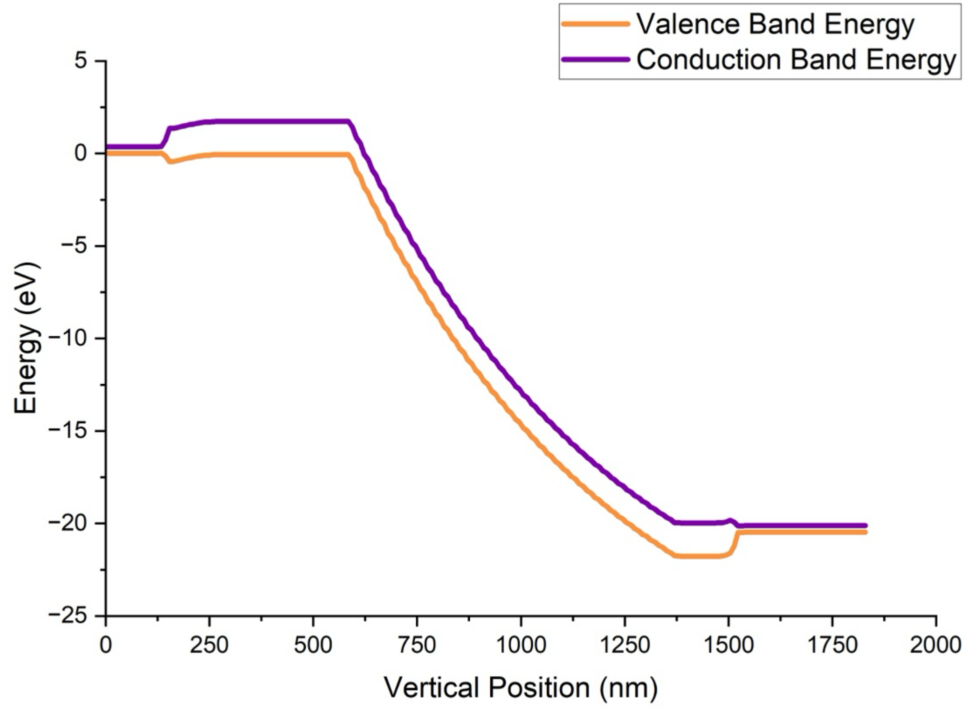

Figure 23. Simulated band diagram for AlGaAsSb p-i-n when a reverse bias of -20 V is applied

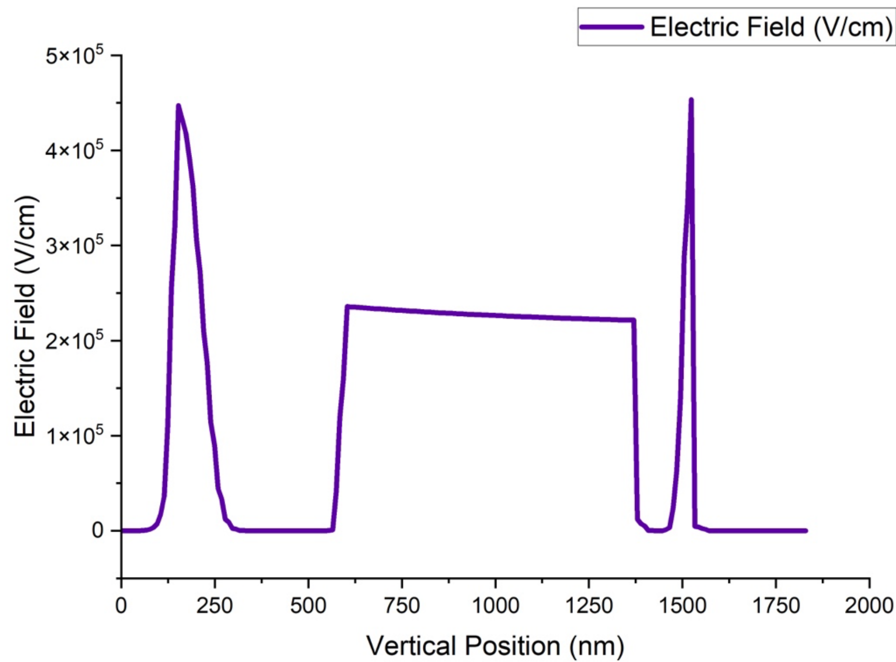

Figure 24. Figure 24. Simulated electric field profile for AlGaAsSb p-i-n when a voltage of -20 is applied.

Next the AlInAsSb p-i-n structure was simulated in Silvaco and the band diagram and the electric field were plotted to inform the structure design. The band diagram and electric field profiles were assessed at both 0 and – 20 V and can be shown in Fig. 25, Fig. 26, Fig. 27, and Fig. 28. Several structures were simulated until a finalized structure was selected. The structure selected has InGaAs contact layers, 300 nm p-type AlInAsSb layer, 100 nm UID AlInAsSb layer, and 100 nm n-type AlInAsSb layer.

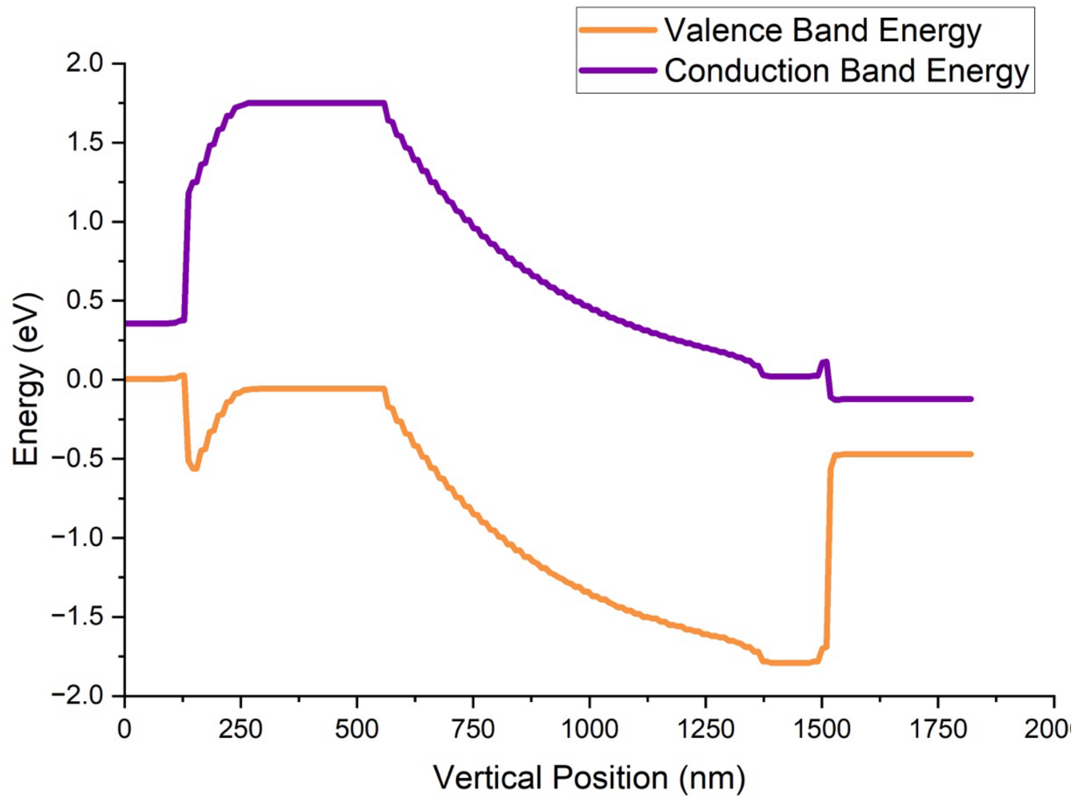

Figure 25. Figure 25. Simulated band diagram of AlInAsSb p-i-n structure at 0 V.

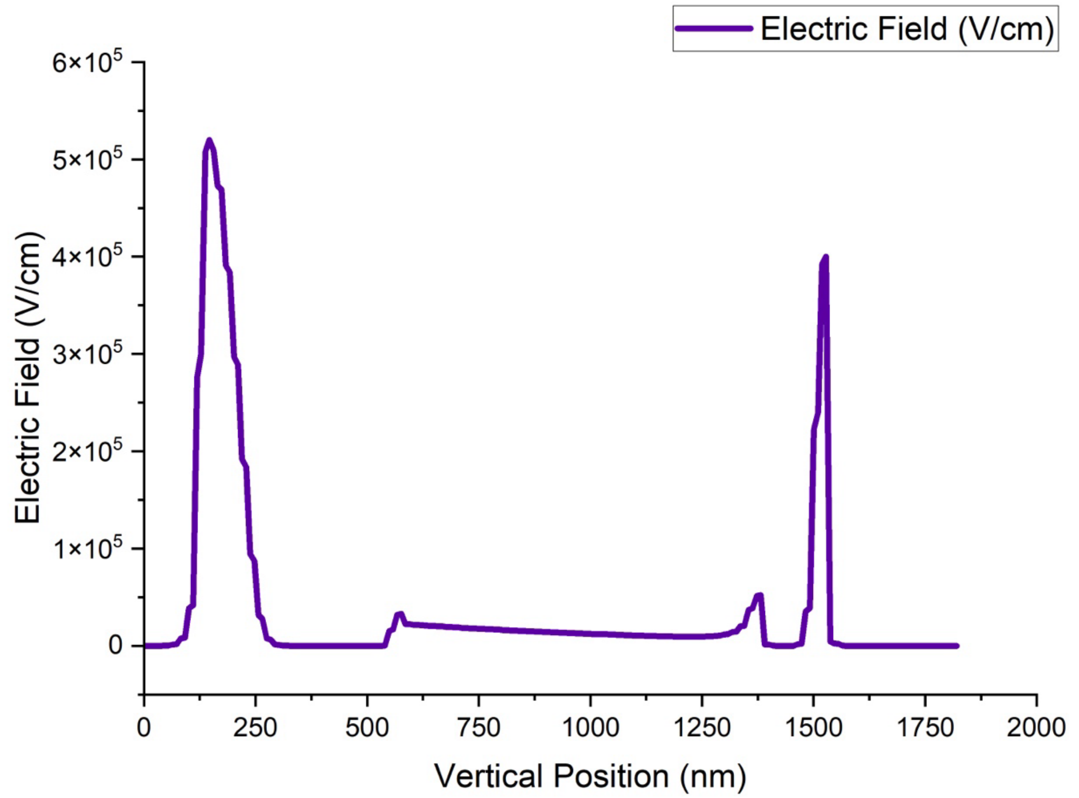

Figure 26. Simulated electric field profile for AlInAsSb p-i-n at 0 V.

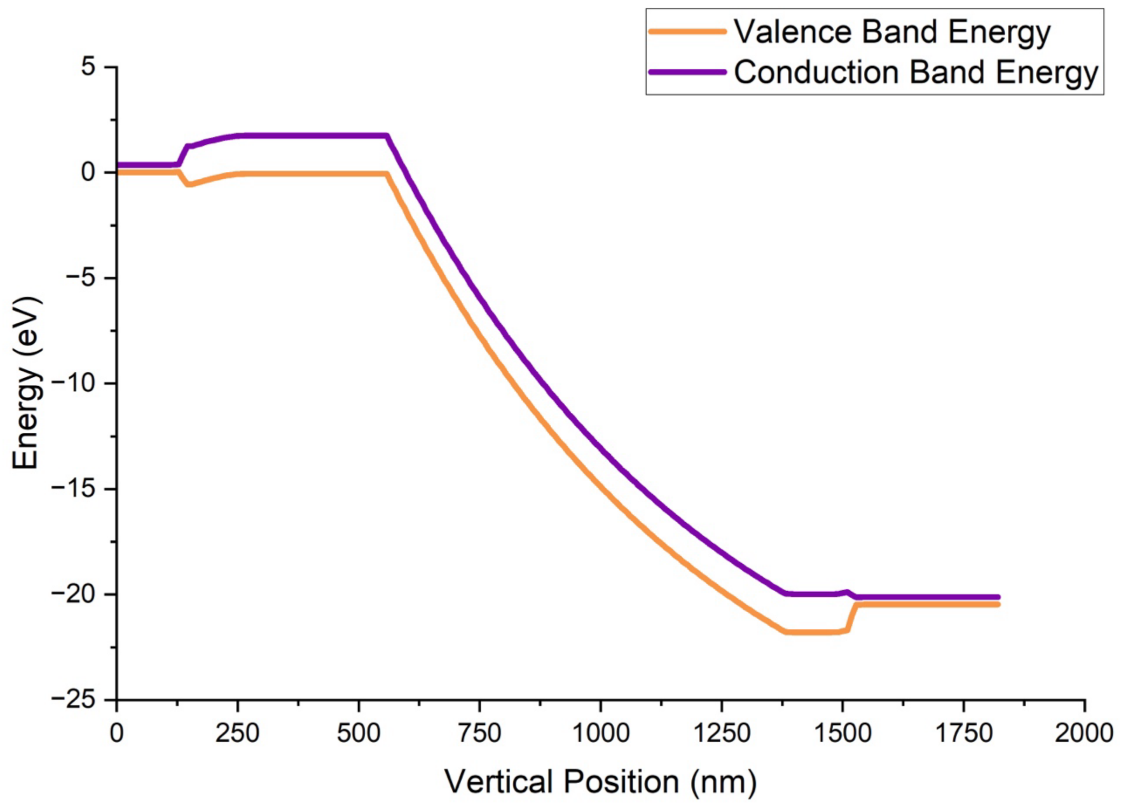

Figure 27. Simulated band diagram for AlInAsSb p-i-n when a reverse bias of -20 V is applied.

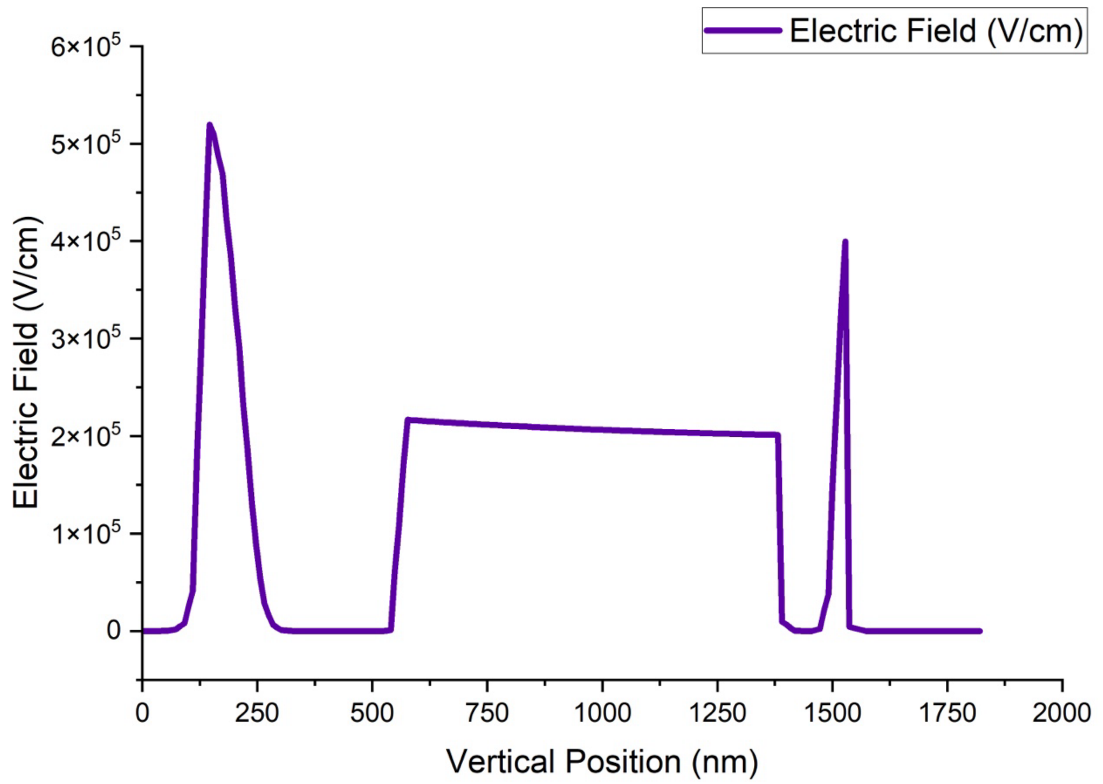

Figure 28. Simulated Electric field profile for AlInAsSb p-i-n when a reverse bias of -20 V is applied.

3.2 Growth

For this investigation, two p-i-n structures were grown and then fabricated to delineate double mesa architecture devices to measure capacitance over a variety of mesa diameters. For the AlGaAsSb p-i-n structure, $Al_{0.85}Ga_{0.15}As_{0.56}Sb_{0.44}$ was grown as a random alloy on a semi-insulating InP substrate via molecular beam epitaxy (MBE). The structure grown had a 910 nm thick UID AlGaAsSb region grown as the multiplication layer that would be over etched to achieve the double mesas. Figure 29 below shows the structure of the AlGaAsSb p-i-n along with respective doping and thickness for each layer.

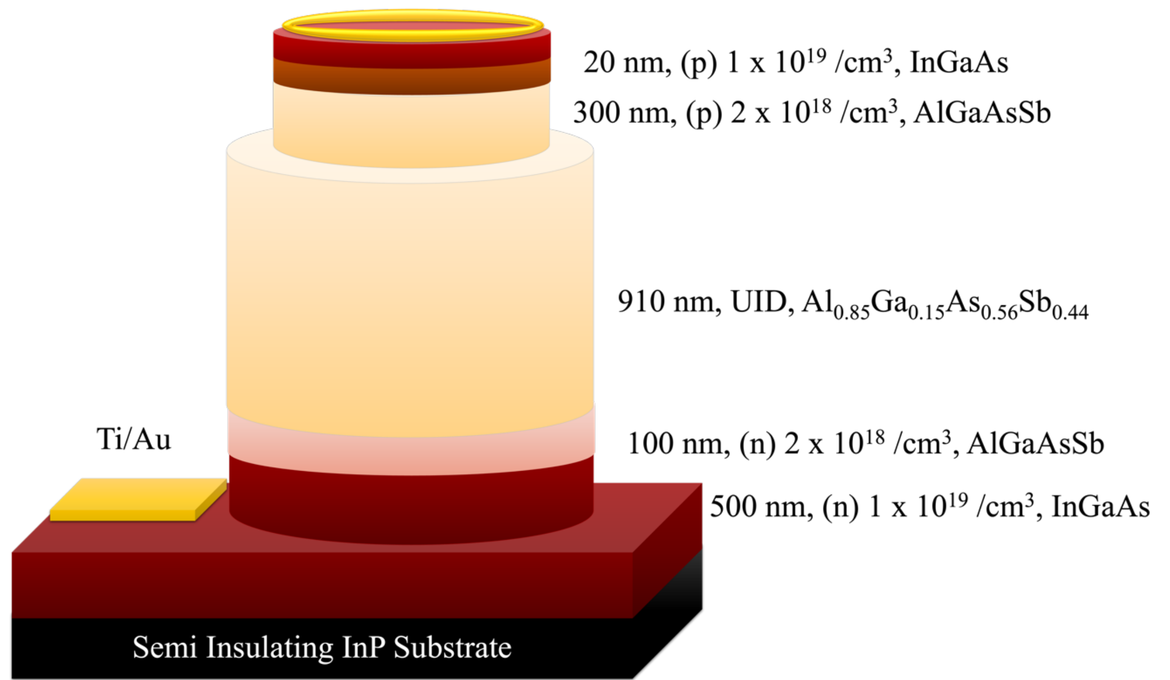

Figure 29. Double Mesa Architecture for Random Alloy AlGaAsSb p-i-n.

For the AlInAsSb p-i-n structure, $Al_{0.79}In_{0.21}As_{0.74}Sb_{0.26}$ was grown as a random alloy via MBE on semi-insulating InP substrates. The UID region was grown to be 1000 nm in thickness. Figure 30 depicts the AlInAsSb structure as a double mesa architecture.

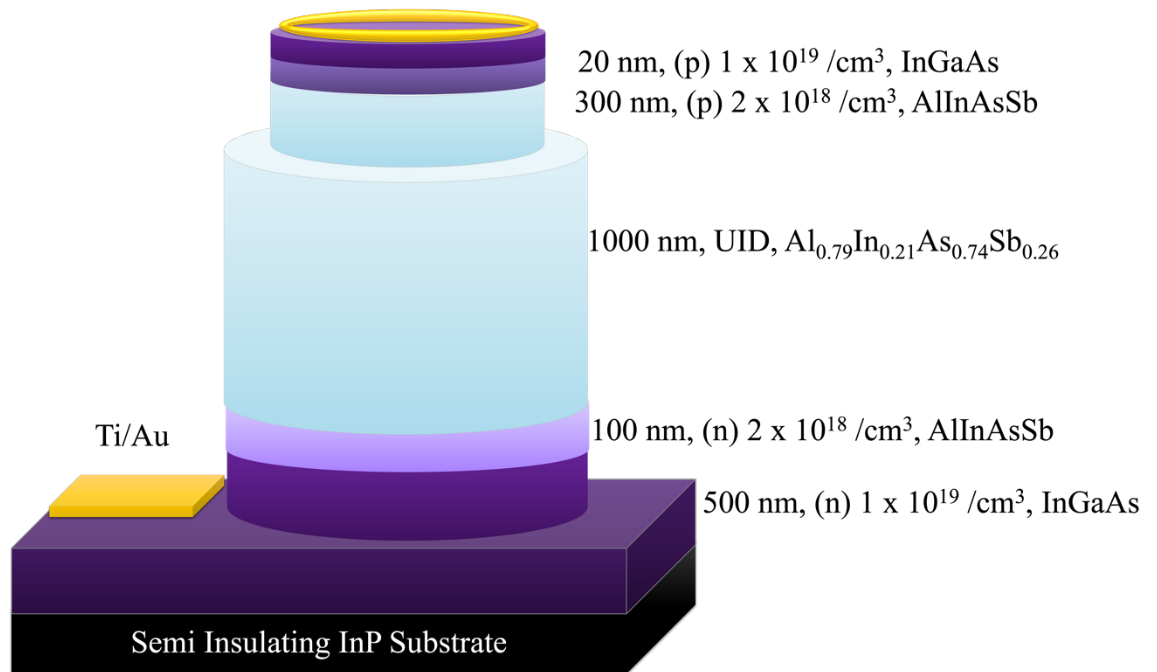

Figure 30. Double Mesa Architecture for Random Alloy AlInAsSb p-i-n.

3.3 Fabrication

For the fabrication of both the double mesa AlGaAsSb and the AlInAsSb p-i-n structures, a similar processing recipe was implemented which includes four overarching steps. During the first step of processing, the sample was first treated with an $HCl:H_20$ (1:10) dip for 30 seconds to remove the native oxide layer on the surface of the material. Once the native oxide layer was removed, a metal stack of 12 nm Ti/150 nm Au was deposited on the material via an electron beam evaporator. During the second step of processing, circular top mesas were formed on the material via a wet etch solution of citric acid (40 g)/H_3PO_4 (10 mL)/ H_2O_2 (240 mL). The etch depth targeted was approximately 50 – 100 nm into the UID region. For step 3, the same process as step 1 was repeated to

deposit the bottom contact. Finally, step 4 of the processing consisted of passivating the sidewalls with SU-8 2000.5 to cure any surface defects present. Prior to the deposition of SU-8, the side walls were treated with the $HCl:H_20$ (1:10) dip for 30 seconds to remove the native oxide layer. The only difference between the processing of the AlGaAsSb and the AlInAsSb p-i-ns to delineate double mesa devices was that the AlInAsSb had slightly more Ti deposited at 20 nm for the metal stack.

For both samples, the same mask design was employed that included double mesa devices that had varying top and bottom mesa diameters. For the top varying mesa region of the mask, the bottom mesa diameter was held consistent at 450 μm and the top mesa diameter was varied between 100, 150, 200, 250, 300, 350 and 400 μm in diameter. For the bottom varying mesa devices, the top mesa remained at 100 μm and the bottom mesa was varied between 100, 150, 200, 250, 300, 350 and 400 μm in diameter. Figure 31 shows the mask design used to assess the varying double mesa designs.

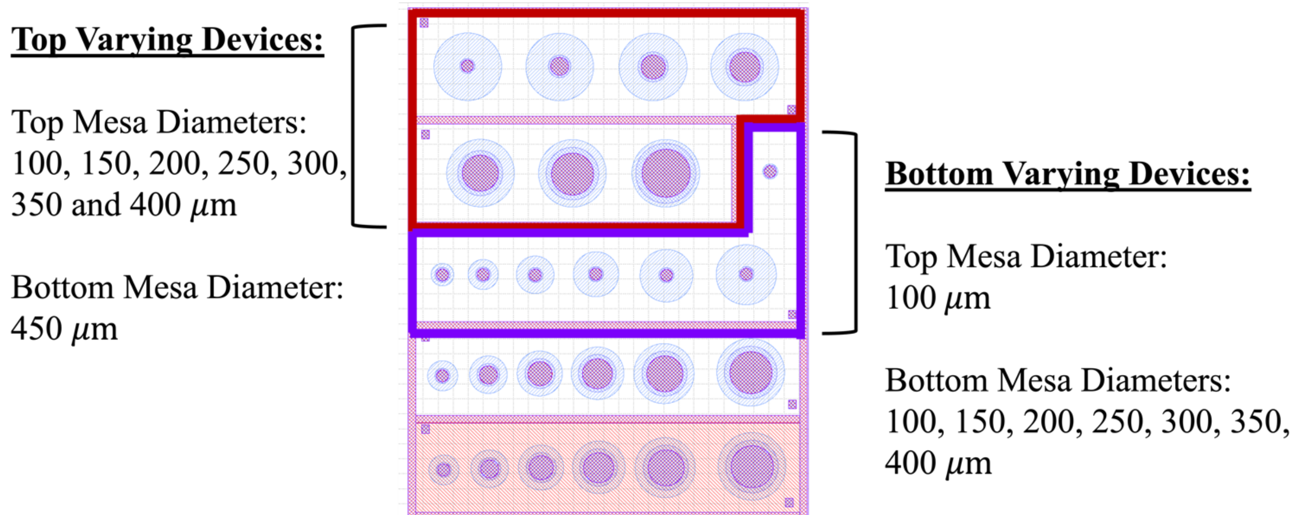

Figure 31. Double mesa mask design with varying top and bottom mesa diameters.

3.4 Characterization

Characterization of the double mesa AlGaAsSb and AlInAsSb p-i-ns was completed in the Lake Shore CRK-6.5K cryogenic probe station and measurements were taken using a Keysight Technologies B1500A parameter analyzer with a source measurement unit (SMU) and a capacitance measurement unit (CMU). Prior to performing the C-V measurements on the samples, circuit calibrations were performed to reduce any presence of parasitic capacitance. C-V measurements were then completed using a magnitude of 50 mV selected for the AC applied signal and a measurement frequency of 1 MHz. For the C-V measurements, three temperatures were selected to assess behavior. These temperatures were 295, 150 and 77 K for both the AlGaAsSb and the AlInAsSb devices. The reasoning for completing cooled C-V measurements in addition to room-temperature measurement is two-fold. Firstly, this provides an understanding of how the

devices will operate under several temperatures of interest and whether their capacitance behavior differs significantly. And secondly, cooled C-V are useful to understand whether carrier switching will occur with a decrease in the operating temperature.

As described in Eq. 19 and Eq. 20, the measured capacitance is dependent upon the voltage supplied. In turn, the differences in capacitance over smaller and larger reverse biases will be present and the depletion width is also impacted. To investigate this, determine where the devices reach full depletion and accurately identify what the background doping polarity several voltages were selected to analyze with the varying mesa diameters. For the AlGaAsSb p-i-n sample, 0 and -10 V were selected as the devices displayed depletion behavior near forward biases. For the AlInAsSb p-i-n sample -10 and -20 V were selected.

3.5 Analyses

Figure 32 below displays the C-V measurements of double mesa random alloy AlGaAsSb varying top and bottom mesas at 295 K. From this figure, it is evident that the measured capacitance across the varying mesa devices does have a relationship with the device diameter, notably the top mesa diameter, as the capacitance increases when the top mesa diameter increases from 150 μm to 450 μm. Consequently, there is no relationship with the bottom mesa diameter varying but the top mesa remaining consistent, as shown in the red group of devices labeled as "100-X". To further evaluate and confirm this observation, capacitance measurements were performed at 150 and 77 K, in addition to the

295 K measurements and obtained capacitances were plotted with the differences in top and bottom mesa diameters at 0 and -10 V. The experimental results of the capacitance measurements were compared against theoretical capacitances to determine how well the devices behaved as expected. Due to variation that may be present within the measurement equipment or between devices due to the fabrication, standard $\pm$ 5% error bars were included for the measurements. To determine the theoretical capacitances, Eq. 22 was implemented with the assumption that the dielectric constant of AlGaAsSb was 11.4 from previous investigations[43,60]. The depletion width was determined to be 1017 nm at 295 K and 1107 nm at 77 K from calculations. Fig. 33 shows that capacitances as a function of increasing the top mesa diameter and Fig. 34 shows the capacitances as a function of increasing the bottom mesa diameter.

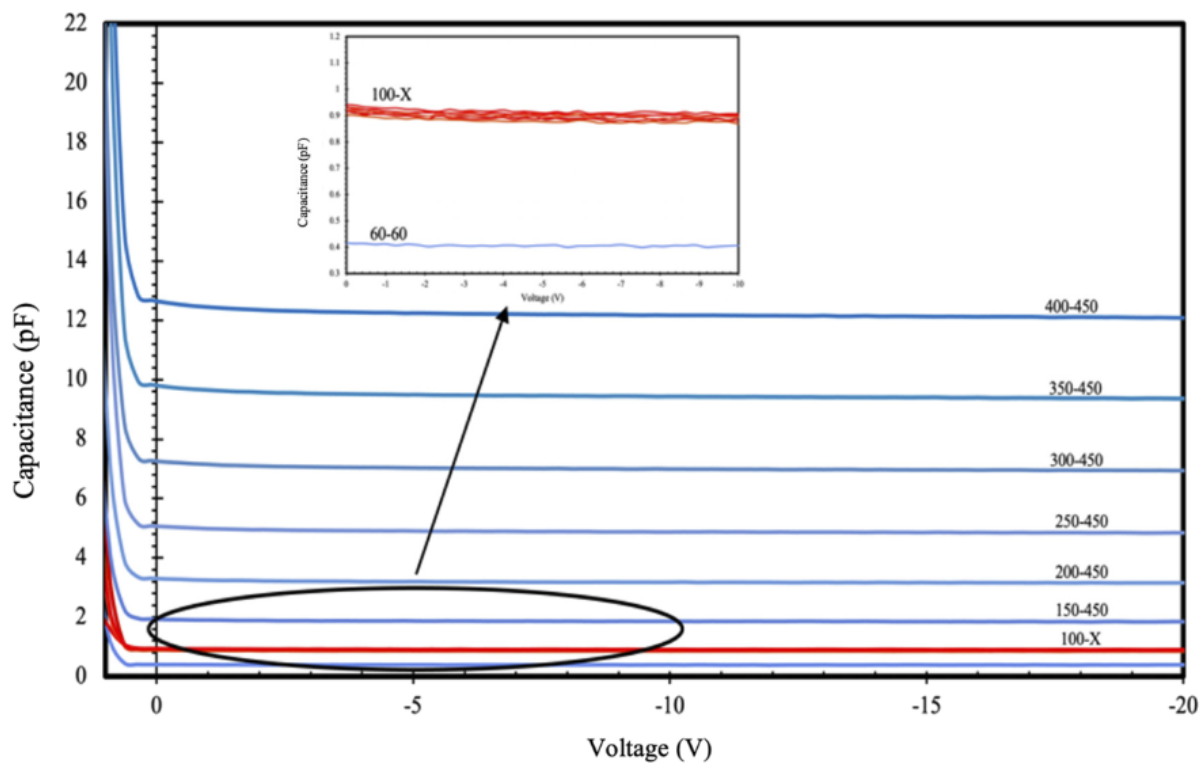

Figure 32. Capacitance-Voltage measurements for measurements for random alloy AlGaAsSb at 295 K. The double mesa devices tested had varying top or bottom mesa diameters.

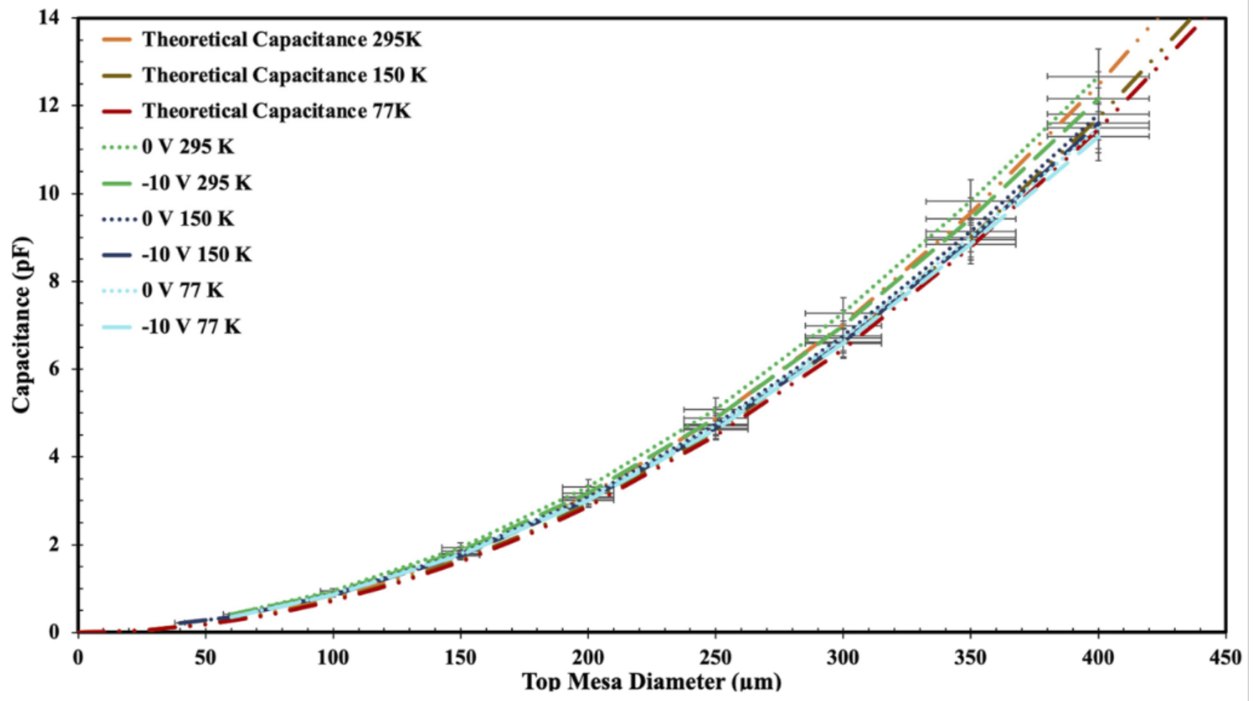

Figure 33. Measured and theoretical capacitances as a function of varying the top mesa diameter of random alloy AlGaAsSb devices at 295, 150 and 77 K and across 0 and -10 V.

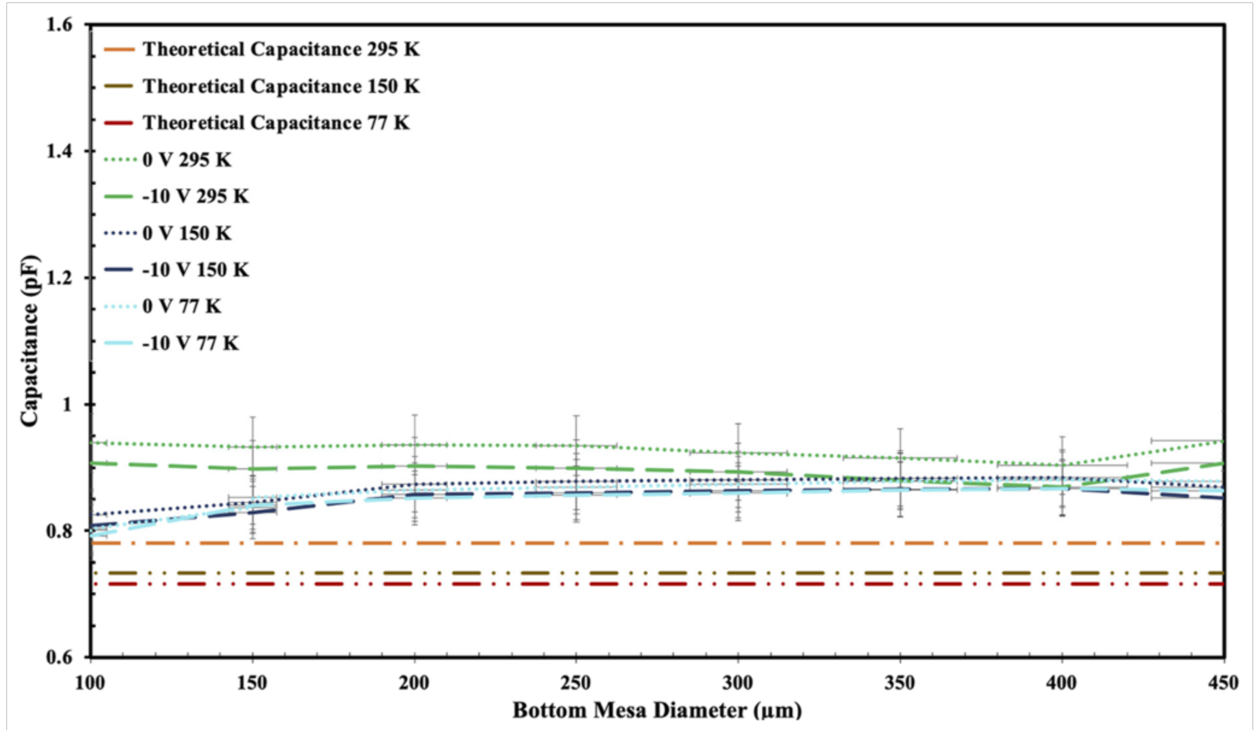

Figure 34. Measured and theoretical capacitances as a function of varying the bottom mesa diameter of random alloy AlGaAsSb devices at 295, 150, and 77 K and across 0 and -10 V.

From Figures 33 and 34, it can be noted that for the random alloy AlGaAsSb p-i-n structure, the top varying mesa devices and their subsequent measured capacitances behaved similar to that of the theoretical capacitances rather than the bottom varying mesa devices. This remained true across the three temperatures investigated, although the closest fitting to the theoretical curve was observed at 295 K. This is likely due to the dielectric constant and depletion widths selected for the theoretical capacitances. Based upon the C-V measurements at 295, 150, and 77 K across both selected voltages for the random alloy double mesa AlGaAsSb sample, it was concluded that the UID polarity is n-type in nature

and is independent of the temperature and bias voltage. This was determined due the capacitance varying with the top mesa diameter, indicating that this is the mesa where the p-n junction occurs close to. Since this remained consistent with decreases in temperature, it can be noted that the random alloy AlGaAsSb does not experience carrier switching at this composition.

The same approach was implemented for the random alloy AlInAsSb double mesa structure and C-V measurements were first assessed at 295 K. Fig. 35 depicts these measurements across the varying top and bottom mesa devices. Measurements indicated that the devices were not depleted fully until larger reverse biases as opposed to the random alloy AlGaAsSb sample. Measurements were then completed at 150 and 77 K to extract analyses. For this material system, a dielectric constant of 13.7 was implemented to determine the depletion width[46]. Using this value, depletion widths of 1078 nm and 1250 nm were determined for 295 K and 77 K, respectively. Figure 36 and Figure 37 show the measured capacitances for the random alloy AlInAsSb double mesa devices with the varying top and bottom mesa diameters at 295, 150, and 77 K and at -10 and -20 V, respectively. The data obtained was compared against the theoretical capacitances.

Similar to the AlGaAsSb double mesa devices, the measured capacitances increased with the increases in the top mesa diameter and did not increase with the changing the bottom mesa diameter. It can be noted that the measured data did not fit closely as the data obtained for the AlGaAsSb sample to the theoretical curves and

remained consistent across the lower temperatures. This is likely due to the assumed depletion width and dielectric constant values implemented. The values are likely different and may improve the fitting. Despite the fitting not being as close as anticipated, it is still indisputable that at each temperature and the biases selected, varying the top mesa diameter of the devices increases the capacitance, thereby indicating that the p-n junction is occurring at the interface of the p-region at the top of the structure and the UID region, where the top mesa resides. Therefore, the UID region of the random alloy AlInAsSb is n-type and the material does not indicate any carrier switching is present.

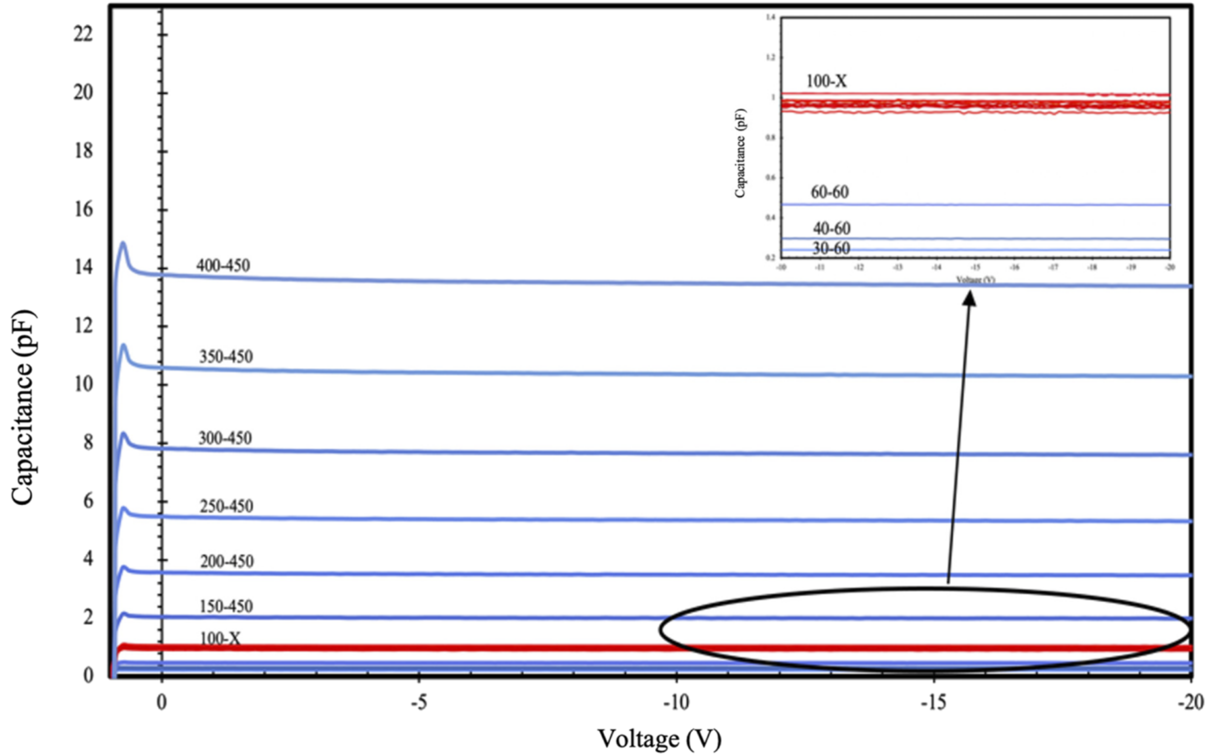

Figure 35. Capacitance-Voltage measurements of varying top and bottom mesa devices for random alloy AlInAsSb p-i-n at 295 K.

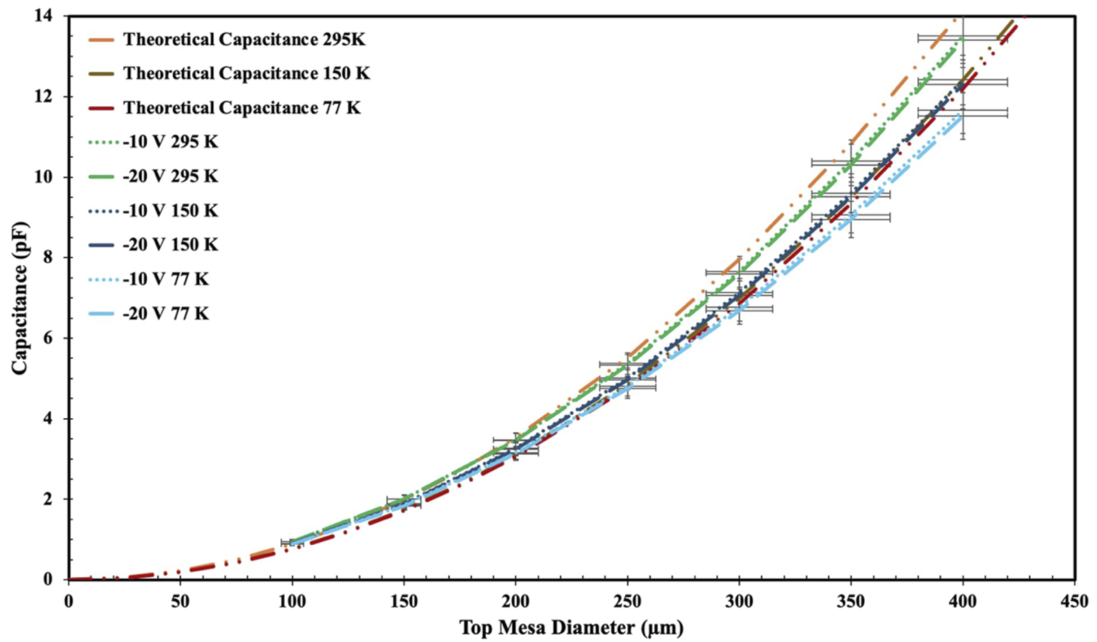

Figure 37. Measured and theoretical capacitances as a function of varying the top mesa diameter of random alloy AlInAsSb devices at 295, 150 and 77 K and across -10 and -20 V.

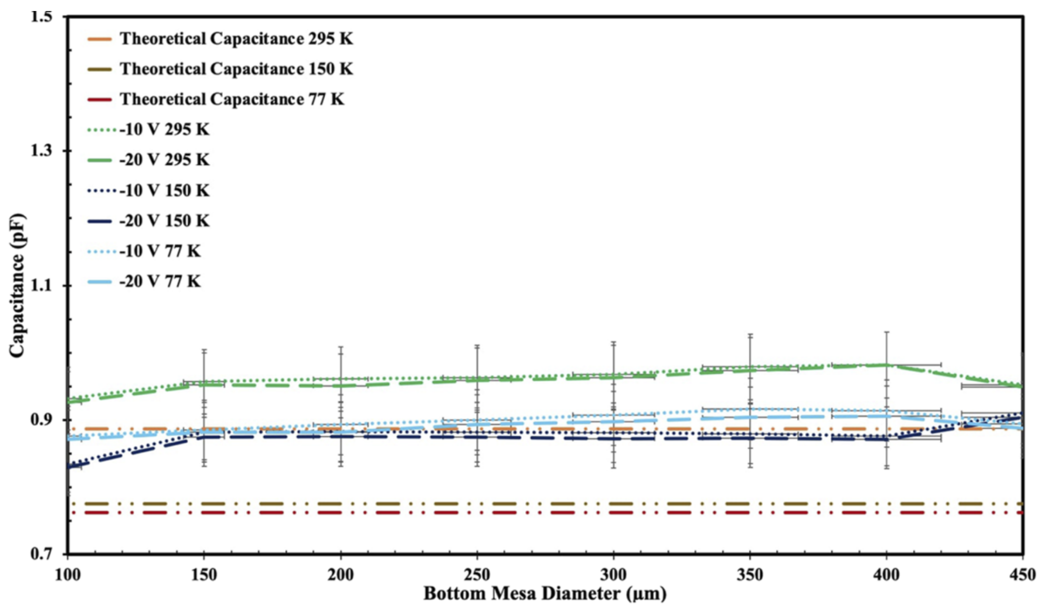

Figure 36. Measured and theoretical capacitances as a function of varying the bottom mesa diameter of random alloy AlInAsSb devices at 295, 150, and 77 K and across -10 and -20 V.

3.6 Technical Challenges

In this investigation, both random alloy AlGaAsSb and AlInAsSb have been determined to be n-type in nature when unintentionally doped during the epitaxial growth using a dual junction analysis and implementation of a double mesa strucutre. While this investigation of the unintentionally doping polarity of random alloy AlInAsSb and AlGaAsSb double mesa structures via capacitance-voltage measurements provided clear results, some work going forward may improve the analysis and fitting. The dielectric constant was assumed to remain consistent across the temperature range. In reality, the dielectric constant of a material is inversely proportional to the temperature, meaning that if the temperature is lower, then the dielectric constant should increase. One way to accurately determine this for a material could be through using a cooled ellipsometer, however this tool is not currently available at Ohio State.

Chapter 4. InGaAs/AlInAsSb Avalanche Photodiodes on InP Substrates

In this chapter, $Al_xIn_{1-x}As_ySb_{1-y}$ (hereafter AlInAsSb) is implemented into the first $In_{0.53}Ga_{0.47}As/Al_{0.7}In_{0.3}As_{0.79}Sb_{0.21}$ SACM APD structure on InP substrates and had demonstrated high temperature stability, comparable excess noise to other APDs, paving the way for this structure to be further investigated and future implementation for high speed, and lower SWaP-C applications.

AlInAsSb has been previously investigated as a material grown lattice matched to GaSb and has previously demonstrated excess noise comparable to Si and tunability in the Al composition that lends to the material being implemented in many applications, spanning from the NIR to the MWIR[45,50,90,119]. AlInAsSb on GaSb substrates has limited bandwidth capabilities due to the highly doped substrate which results in a low RC limited bandwidth[120]. Recently, AlInAsSb has been demonstrated on InP substrates and exhibit low excess noise and low dark current[46]. From these previous reports showcasing the potential of AlInAsSb based APDs, the material system has been implemented into more complex SACM designs to further performance even more. InGaAs has been selected as the absorber material due to its favorable bandgap energy for SWIR detection at 1550 nm.

While the key figures of merit outlined so far for high performing APDs have revolved around mitigating the dark current and excess noise and maximizing the multiplication gain and quantum efficiency, the temperature dependence of the breakdown voltage may be of

strong interest depending on the application of the technology. Typically, APDs are strongly influenced by temperature and lower temperature operation reduces the bulk dark current, thereby improving the sensitivity of the detector overall. This motivates the implementation of cryogenic cooling to achieve optimal APD performance but comes at the cost of higher SWaP-C.

4.1 Design and Growth

The InGaAs/AlInAsSb SACM APD was grown via MBE and implemented a digital alloy 1 µm AlInAsSb multiplier, with bandgap energy of approximately 1.29 eV, and a 1 µm InGaAs absorber. AlInAsSb was grown as a digital allow of the constituent binaries AlAs, AlSb, and InAs in a 10-monolayer period. The choice was made to grow the material as a digital alloy, as AlInAsSb has historically been a challenging material to grow as random alloy because of the wide miscibility gap[89]. Prior to the growth of the InGaAs/AlInAsSb SACM structure, careful consideration was taken via simulations to ensure that the electric field remained low in the absorber region and was properly graded to achieve high electric fields in the AlInAsSb to leverage the impact ionization in the production of gain. Fig. 38 shows the structure design and grown via MBE and Fig. 39 shows the band diagram of the structure under no applied bias. One of the key challenges for the design and growth of the structure was the large conduction offset between the InGaAs absorber and the AlInAsSb, which required careful grading. To achieve this, the grading was completed in two layers. The first layer of the grading focused on grading the Ga composition out from $In_{0.53}Ga_{0.47}As$ to InAlAs over 50 nm and the second layer of the

grading increased the Al composition of x = 0 to the desired composition of x = 0.7 over 50 nm. This two-pronged method of grading the structure prevents the presence of the conduction band offset inhibiting carrier injection from the absorber to the multiplier. To verify that the material quality was grown sufficiently, high resolution X-ray diffraction (HR-XRD) was performed prior to fabrication[92].

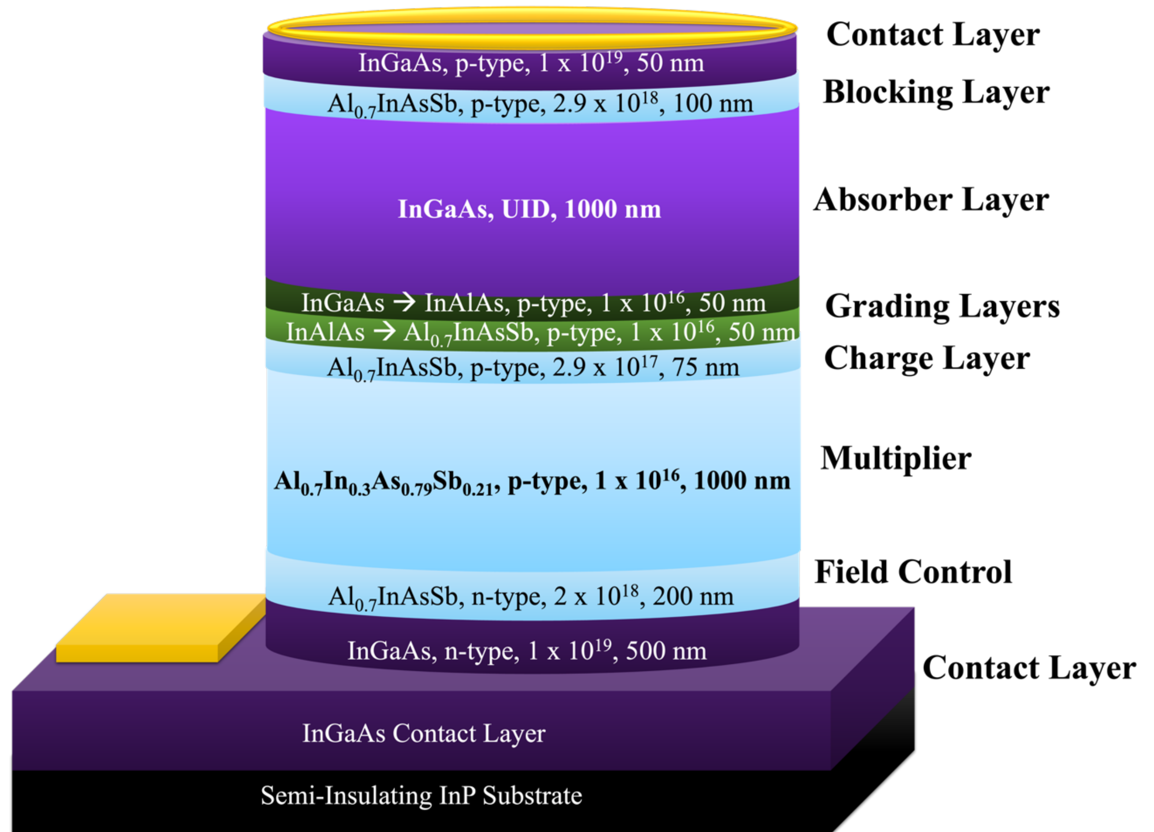

Figure 38. Epitaxially grown structure of the In0.53Ga0.47As/Al0.7In0.3As0.79Sb0.21 SACM APD on Semi-Insulating InP Substrate.

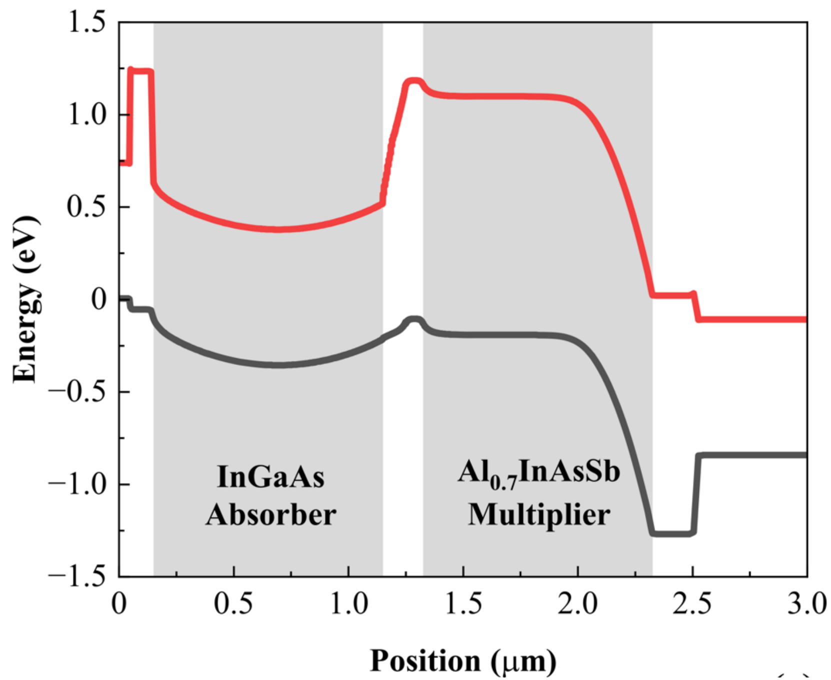

Figure 39. InGaAs/AlInAsSb heterostructure band diagram under no applied bias.

4.2 Fabrication

Devices were fabricated from the epitaxial material using standard fabrication procedures outlined in Chapter 2. The epitaxial material was etched to produce the mesa architecture via an etching chemistry of H_3PO_4/H_2O_2/H_2O/Citric Acid and the side walls were passivated with SU-8. Metal contacts of Ti/Au were deposited via an electron beam evaporator.

4.3 Characterization

Individual devices were first characterized at 295 K to determine their current-voltage behavior both under dark and under 1550 nm illuminated conditions to subsequently extract the gain. Fig. 40a shows the I-V behavior and calculated gains for a 150 µm diameter circular device. The devices tested displayed initial punch-through behavior to get to the multiplier at ~ -48 V, although a secondary punch-through-like step from -55 to -57.5 V which is not ideal. The secondary punch-through step has been attributed to the presence of traps that may have been produced during the epitaxial growth of the grading layers. Despite the presence of the step, higher temperature operation made it less pronounced. While not ideal, the secondary punch-through step was determined to be the unity gain, at which gain can be calculated from and a maximum gain of 17 was obtained. This gain is lower than desired, and it is possible that higher gains can be demonstrated with the structure in the absence of the secondary punch-through and if a new structure is grown with higher doping of the charge layer with the intention to prevent premature tunneling of carriers in the absorber.

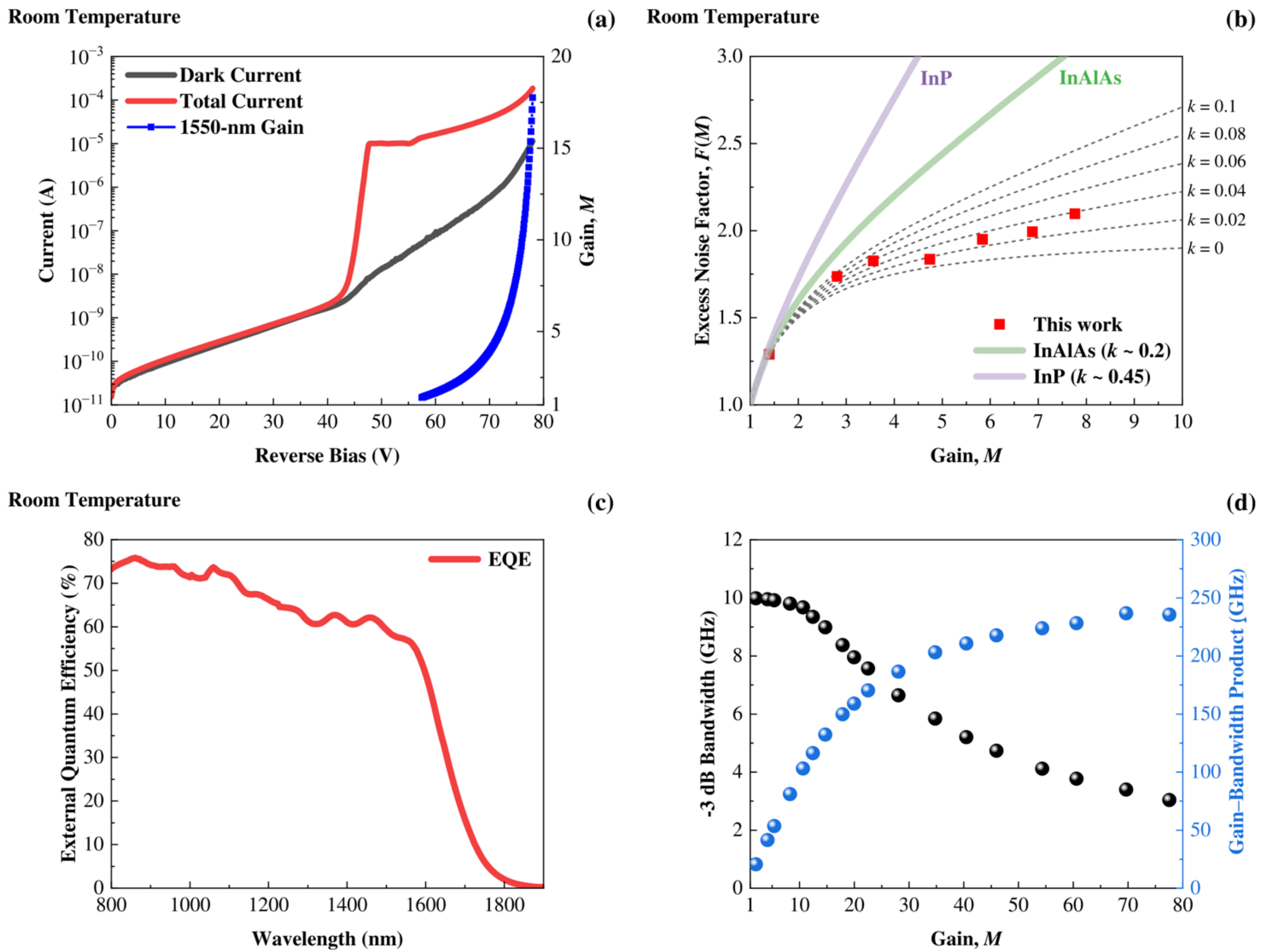

Figure 40. Characterization of the InGaAs/AlInAsSb SACM APD at 295 K. (a) Demonstrated dark, photocurrent at 1550 nm, and calculated gains for a 150 µm diameter device at 295 K. (b) Excess noise factor as a function of increasing gain for a 150 µm diameter device. (c) External quantum efficiency as a function of increasing wavelength. (d) Simulated -3 dB bandwidth and gain-bandwidth product for a 40 µm diameter device.

Fig. 40b displays the excess noise behavior of the structure as a function of increasing the gain up to gains of 10. For fitting and to serve as a reference, F(M) curves were included for *k*-values from 0 to 0.1 using Eq. 2. From the measurements collected on the InGaAs/AlInAsSb APD, the measured *k*-values fall into the range of 0.02 – 0.04. This range of *k*-values for the SACM is in line with our group's previous reports of $Al_{0.79}In_{0.21}As_{0.74}Sb_{0.26}$ p-i-n APDs as well as Ge/Si SACM APDs[46,102,121]. Furthermore, this k-value range obtained for the InGaAs/AlInAsSb SACM APD is significantly lower than demonstrated for both InGaAs/InP and InGaAs/InAlAs SACM APDs by an order of magnitude[122,123,124,125]. Fig. 40c shows the external quantum efficiency for the structure from 800 nm to 1900 nm when measured at the unity gain of the APD. From the plot, it is evident that high external quantum efficiencies are achieved, notably at 1064, 1301, and 1550 nm with values of 73 %, 61 %, and 57 %, respectively. While these values of external quantum efficiency are promising, higher quantum efficiency may be realized with the implementation of anti-reflection coating. Finally, -3 dB bandwidth and gain-bandwidth product as a function of gain was simulated for the structure at the University of Virginia using a 40 μm diameter device as is depicted in Fig. 40d and was calculated using a random path length model[126].

In Section 2.5, we discuss the importance of the determining the breakdown voltage and its relationship with increasing or decreasing the temperature and identifying what the dominate mechanism is responsible. Eq. 17 showed an equation that is implemented to quantify the temperature coefficient of avalanche breakdown, C_{bd} via the change in the

breakdown voltage as a result in the change in operating temperature. To determine the C_{bd} of the InGaAs/AlInAsSb SACM structure, current-voltage measurements were completed from 200 to 340 K in 20 K incremental steps under both dark and 1550 nm illumination

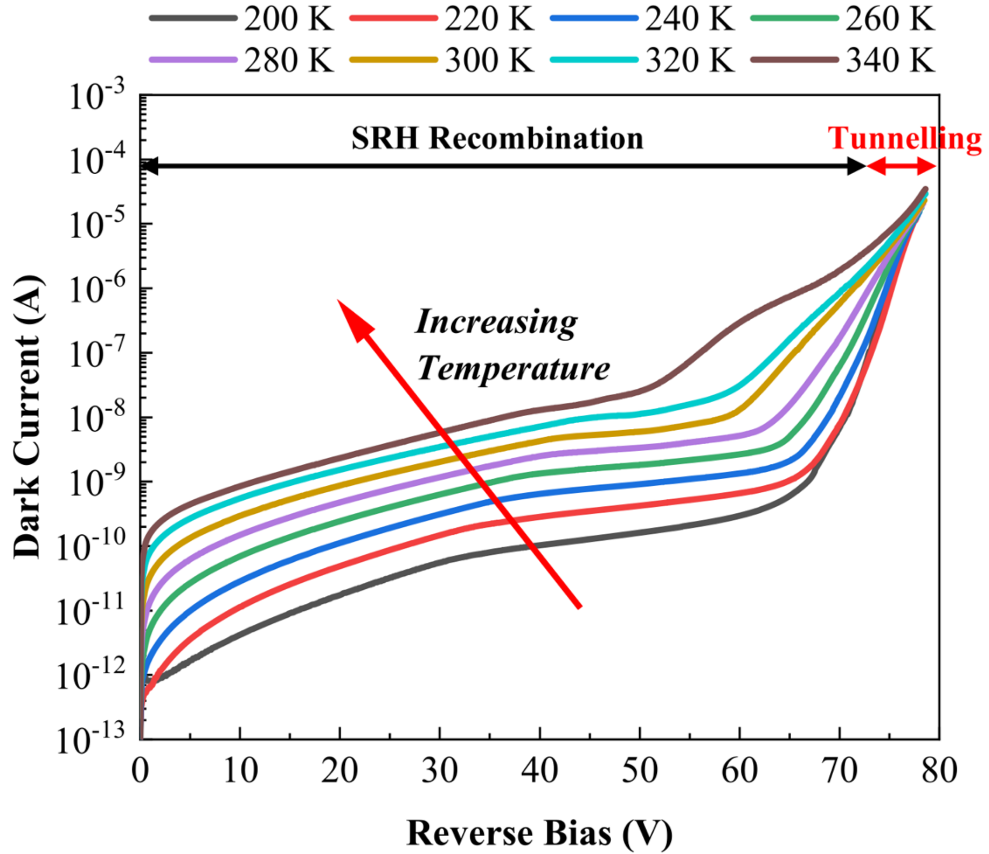

Figure 41. Dark current-voltage behavior of 150 µm diameter device from 200 K to 340 K.

for a 150 µm diameter device. Fig. 40 shows the dark current IVT plot for the device as the temperature increases. From this figure, it can be noted that Shockley Read Hall (SRH) recombination was observed at reverse biases up to ~ -70V, and then from approximately -70 V to -78 V, the tunneling behavior was observed.

Fig. 42 shows the gain calculated from the dark current and 1550 nm illuminated photocurrent measurements across 200 K to 340 K, with gain values found between 9 and

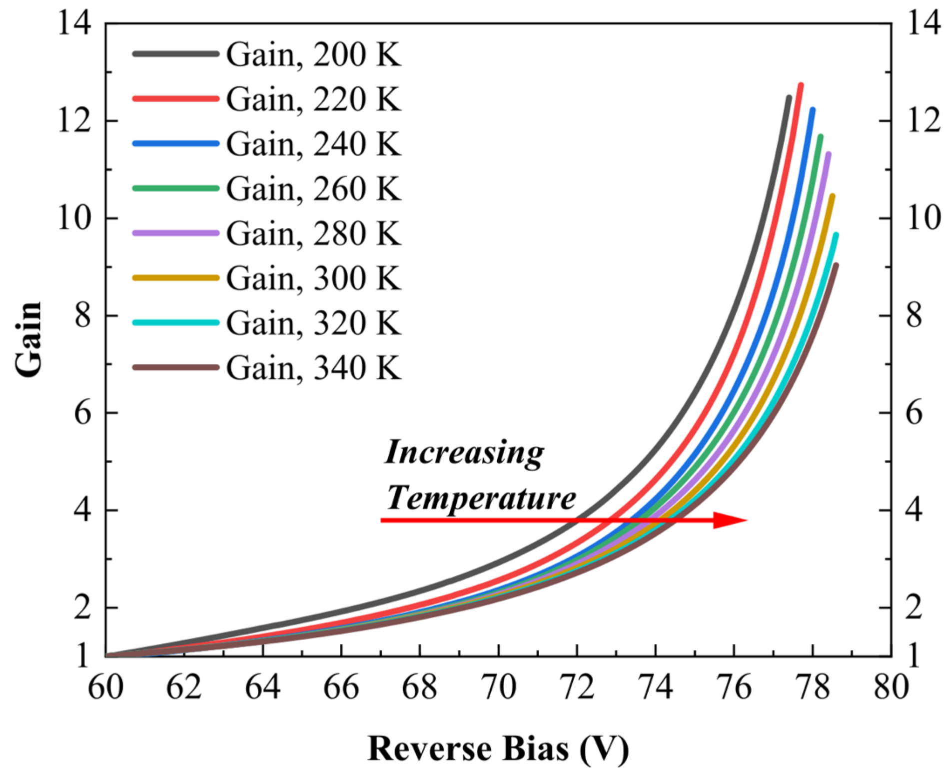

Figure 42. Calculated gains as a function of reverse bias across the temperature range from 200 K to 340 K for a 150 μm diameter device.

approximately 13. From this figure, the breakdown voltage across each temperature were determined via fitting the intercepts at which the inverse of M = 0 and is shown in Fig. 43.

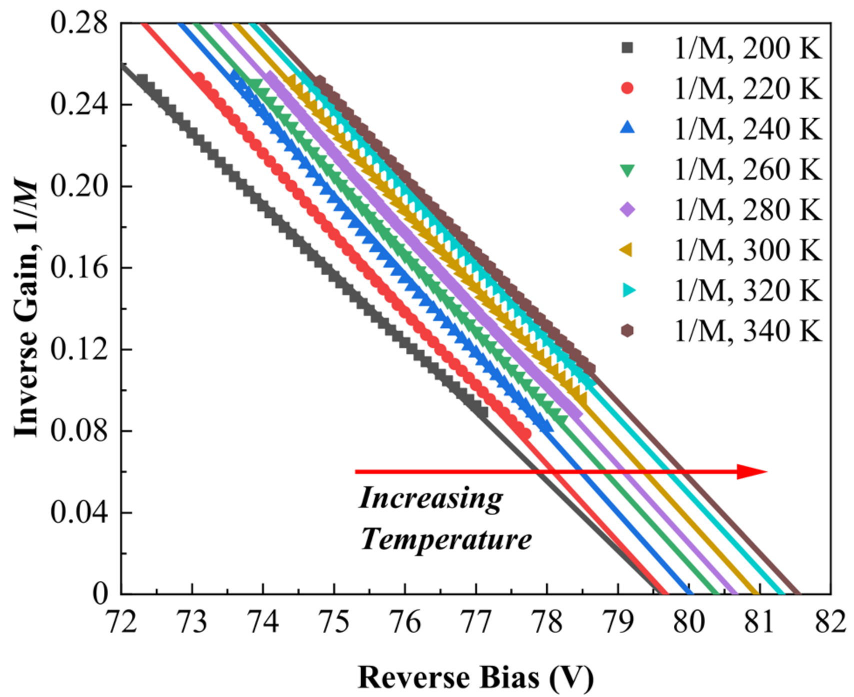

Figure 43. Inverse gain for the 150 μm diameter device as a function of increasing reverse bias across the temperature range of 200 K to 340 K.

4.4 Analyses

From the fitting based off of Fig. 43, the C_{bd} was determined to be 14.58 ± 0.63 mV/K through a linear fitting regression model. In order to compare against other APD

structures, the gradient of C_{bd}, represented as *P*, was found to be 6.7 mV/K/μm for the InGaAs/AlInAsSb SACM APD. *P* provides a way to compare the structure and its impact of temperature variation using different materials and their respective differences in depletion regions[110]. *P* values were compared against other structures of interest, such as $AlAs_{0.56}Sb_{0.44}$, InAlAs, InP and Si APDs and can be seen in Table 4 below[110,111,127]. Of these structures, the InGaAs/AlInAsSb SACM APD demonstrated the lowest gradient of C_{bd}, *P*, (notably a 1/6 lower value than InP) thereby affirming the strong temperature stability of the heterostructure which may translate to potential reductions in circuit complexity, and overall cost that is attractive for a wide variety of applications.

Table 4. Comparison of the gradients of C_{bd} for several APD structures of interest.

APD Structure	**Gradient of C_{bd} (mV/K/ μm)**
$In_{0.53}Ga_{0.47}As/Al_{0.7}In_{0.3}As_{0.79}Sb_{0.21}$	6.7
AlAs0.56Sb0.44	8.5
InAlAs	16.5
Si	25
InP	43

4.5 Technical Challenges

As highlighted, the InGaAs/AlInAsSb SACM APD is the first on InP substrates and has exhibited promising behavior of temperature stability which is attractive for a variety of applications where cost is required to be lowered. While this encouraging, additional iterations of the structure are required to improve the critical parameter of dark current and subsequently improve gain values. At present, the maximum gains realized with the structure was ~ 17, which may limit the sensitivity. To combat this issue and improve the overall performance, it is beneficial to evaluate the structure and increase the charge layer doping in the next structure. This will inhibit carriers tunneling from the InGaAs absorber to the AlInAsSb multiplier prematurely and resulting in a rapid increase in the dark current. Additional growths also improve the secondary punch-through behavior observed with the structure, that likely occurred due to traps being present in the heterostructure.

Chapter 5. Zn-Diffused AlGaAsSb p-i-n on InP Substrates

In Chapter 2, another Sb-based material, AlGaAsSb, was discussed as a promising APD material to serve a multiplier material in an SACM APD and in Chapter 3, we investigated the doping polarity of the material grown as a random alloy. That work was motivated from previous reports that demonstrated the low noise capabilities of $Al_{0.85}Ga_{0.15}As_{0.56}Sb_{0.44}$, encouraging gain values, and low dark current densities for p-i-n structures grown on InP substrates[43,44]. Since then, much work has focused on the continuing efforts into reducing the overall dark current and to push the gain even further for higher sensitivity of the detector, notably at higher operating temperatures. While significant work has been undertaken for reducing the bulk dark current, less effort have been made to mitigate the surface dark current components, which will be investigated in this chapter, as well as Chapter 6.

Recently, there has been interest into exploring alternative architectures of APDs, notably planar structures as a way to reduce, or potentially remove all surface leakage current associated with the etching process to delineate a mesa device. This is especially advantageous as efforts move to ultra-sensitive detectors on the cusp of single photon detection like Geiger mode. To achieve this, it is necessary to suppress the edge breakdown effect that reduces the breakdown voltage of devices and planar devices are one method to combat this challenge. To form optimal planar devices and still define an active of each device, a p-n junction is still required. One method to do this is through a diffusion process

of p-type dopants into n-type material. Different dopants can be selected as the p-type dopant for the diffusion process, but a very common one selected for III-V materials, notably for InGaAs/InP APDs is Zinc[128,129,130,131,132]. Many reports have demonstrated Zn diffusion into III-V via metal-organic chemical vapor deposition (MOCVD) or MOVPE, however we have recently demonstrated the feasibility of an alternative method to promote Zn-diffusion using Atomic Layer Deposition (ALD) to deposit ZnO and a diffusion furnace tube in InGaAs/GaAsSb superlattice structure[133]. The motivation of this approach over the other approaches mentioned above or ion implantation for Zn-diffusion is multi-faceted. First, using ALD is a highly manufacturable and scalable process that is capable of uniform thin film depositions and high accuracy, thereby paving the way for future development of the processing[134]. Secondly, ALD is relatively inexpensive as opposed to the other methods mentioned, and has a quick turnaround, unlike ion implantation and does not sacrifice the material quality. And finally, ALD is readily available at OSU. In addition to ALD, the diffusion furnace tubes are attractive for the diffusion process, as they can be adjusted for their temperature and atmospheric conditions to initiate and maximize the Zn dopants to diffuse into the structure.

5.1 Design

While reports have been investigated into Zn-diffusion and planar for other III-Vs, no such work has investigated Zn-diffusion into AlGaAsSb APDs, with the eventual integration into planar architecture devices. This is important to study as one way to improve device performance, target higher voltage operation at high operating

temperatures, and leverage the gain potential of the Sb-based APD. For these reasons, this study has investigated a novel investigation of Zn-diffused AlGaAsSb p-i-n APDs, with the eventual path leading to fully planar Zn-diffused AlGaAsSb p-i-n APDs. This work determined the feasibility of the process for future APDs.

5.2 Growth

Fig. 44 below shows the $Al_{0.85}Ga_{0.15}As_{0.56}Sb_{0.44}$ p-i-n structure grown via MBE on Semi-insulating InP substrates to investigate the Zn-diffusion process. InGaAs and InAlAs were used as the contact layers of the structure and AlGaAsSb was grown a random alloy very thick 2000 nm UID region. UID was selected as random alloy AlGaAsSb is a known to be n-type in nature, as concluded in Chapter 3. No intentional p-type region was grown, to ensure that the p-type Zn diffusion was assessed properly in the structure.

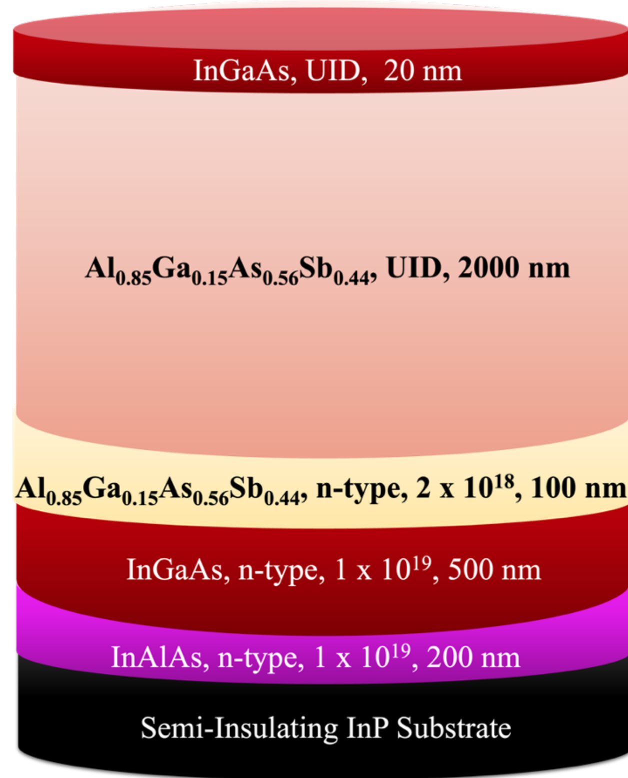

Figure 44. AlGaAsSb structure grown on SI InP substrates for Zn-diffusion.

5.3 Fabrication

For the fabrication process, a standard mesa recipe was implemented to delineated circular devices with the addition of an ALD and diffusion furnace step to deposit ZnO and diffuse the p-type dopants into the structure. For the ALD, $(C_2H_5)_2Zn$ (Diethyl Zn) was selected as the precursor to deposit ZnO on the epitaxial material. In order to deposit ZnO, Diethyl Zn is first introduced into the ALD chamber where it adheres onto the sample's

surface to form a monolayer. De-ionized H_2O gas is then introduced into the ALD chamber, where it reacts with the Diethyl Zn monolayer to form a ZnO monolayer. This process is shown in Fig. 45 below and represents one cycle of completion which deposits approximately 0.1 nm of ZnO onto the sample. During previous investigations of the Zn-diffusion into the InGaAs/GaAsSb, the ZnO thickness deposited was investigated to determine its influence over Zn diffused into the structure[133]. For this process, ~ 30 nm of ZnO was deposited at a substrate temperature of 150 °C. To verify the deposited thickness, a Si reference chip was also placed in the ALD during the deposition and then subsequently measured using an ellipsometer to determine the ZnO thickness. Following the ZnO deposition, the sample was placed into a quartz boat and inserted into a diffusion furnace tube. To promote the breaking of the ZnO to diffuse the p-type Zn into the structure, the diffusion was completed under 20 sccm of forming gas. Forming gas, which is a mixture of N_2 and H_2, encourages the bonding of the oxygen atoms to the H_2 to produce H_2O, freeing the Zn to diffuse more than an inert atmosphere would promote. Fig. 46 represents the diffusion under forming gas conditions. Another consideration that was made for the diffusion process was the time the sample was in the furnace tube. Early in the investigation, a diffusion time of 90 minutes was selected but was observed to result in early breakdown of devices, and subsequent fabrications were completed using 20 and 10 minute diffusion times which will be discussed further in the next section. Once fabrication was complete for the Zn-diffused samples, the device structure was as shown in Fig. 47.

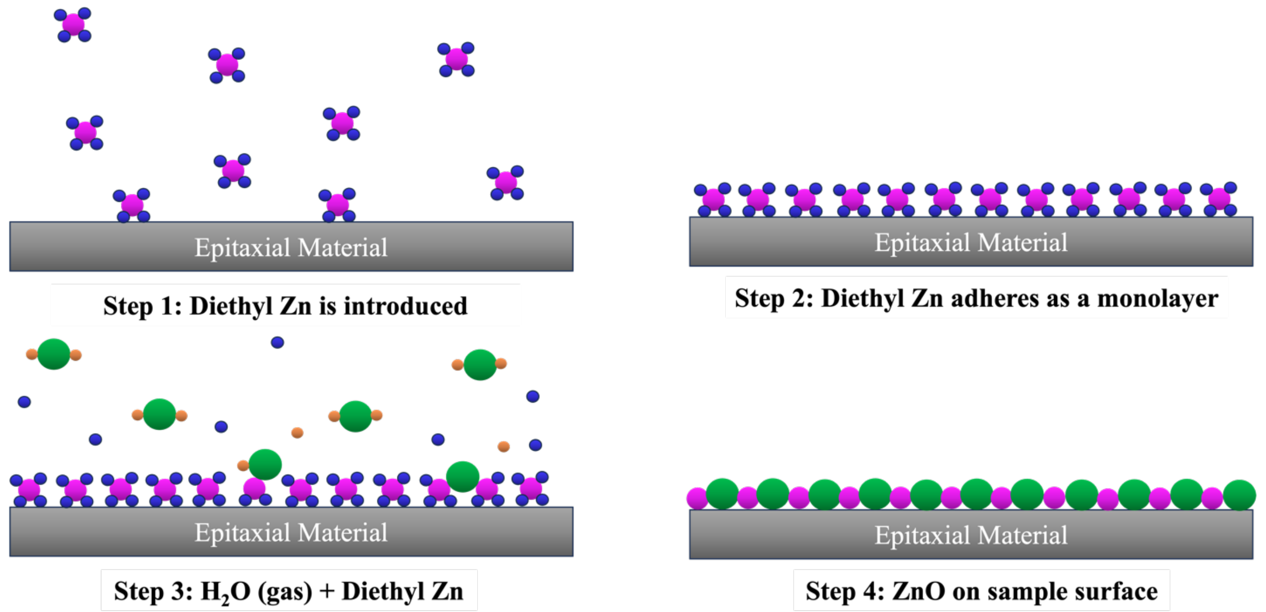

Figure 45. ALD Process for thin film deposition.

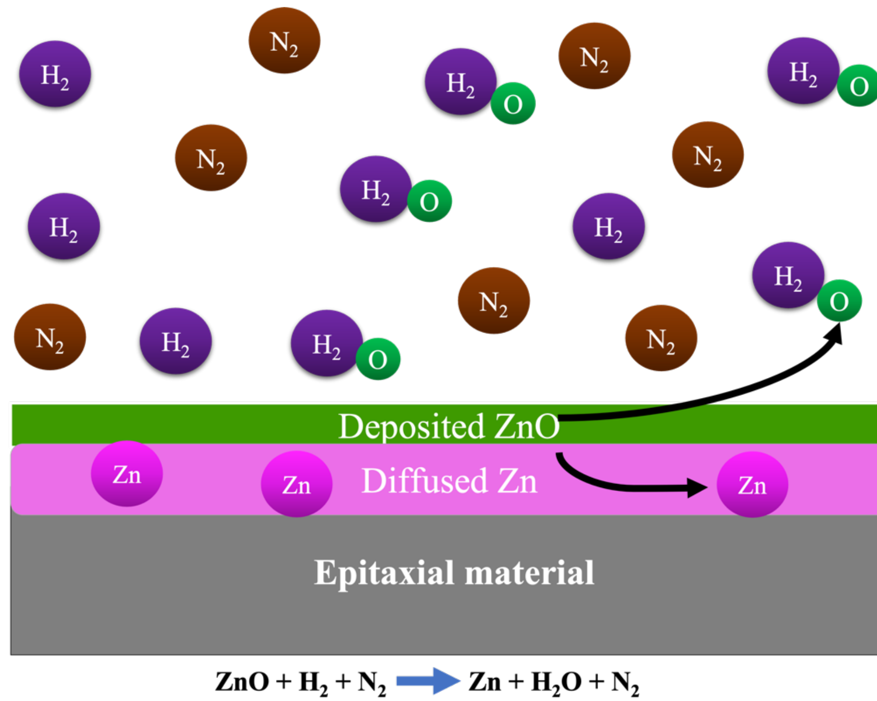

Figure 46. Diffusion under forming gas.

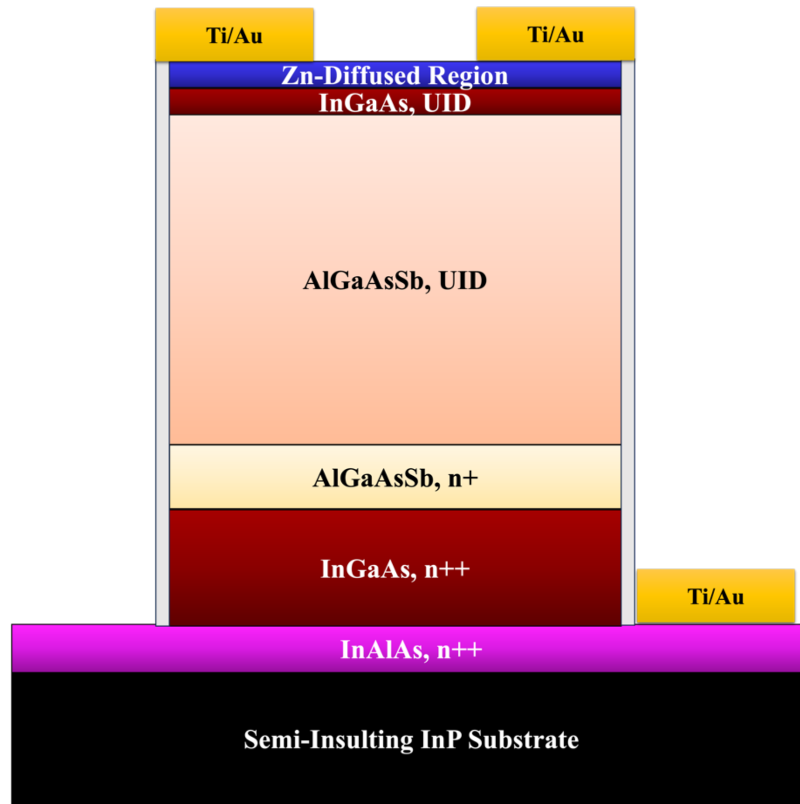

Figure 47. Processed AlGaAsSb p-i-n material into a Zn-diffused mesa.

5.4 Characterization

As mentioned in the fabrication section, Zn-diffused AlGaAsSb devices were fabricated first under three different time conditions within the furnace tube. The times selected were 90, 20, and 10 minutes. This was completed to first determine optimal conditions for the diffusion process prior to undergoing more intensive analyses. From these initial samples, dark current I-V characterization was completed across varying circular devices with different diameters and can be seen in Fig. 48 for the 90 minute

sample and is further zoomed in to see the irreversible breakdown of devices on the 90 minute sample as Fig. 49. Fig. 50 and Fig. 51 showcase the varying device behavior under 20- and 10-minute diffusion times, respectively. From these graphs, it is evident that the diffusion furnace time is a critical variable within the process and a reduction in diffusion time pushes the breakdown voltage to larger reverse biases and lowers the dark current across the devices. This has been assumed that is likely related to the increase in diffusion enabling Zn dopants to diffuse further laterally over the longer diffusion time.

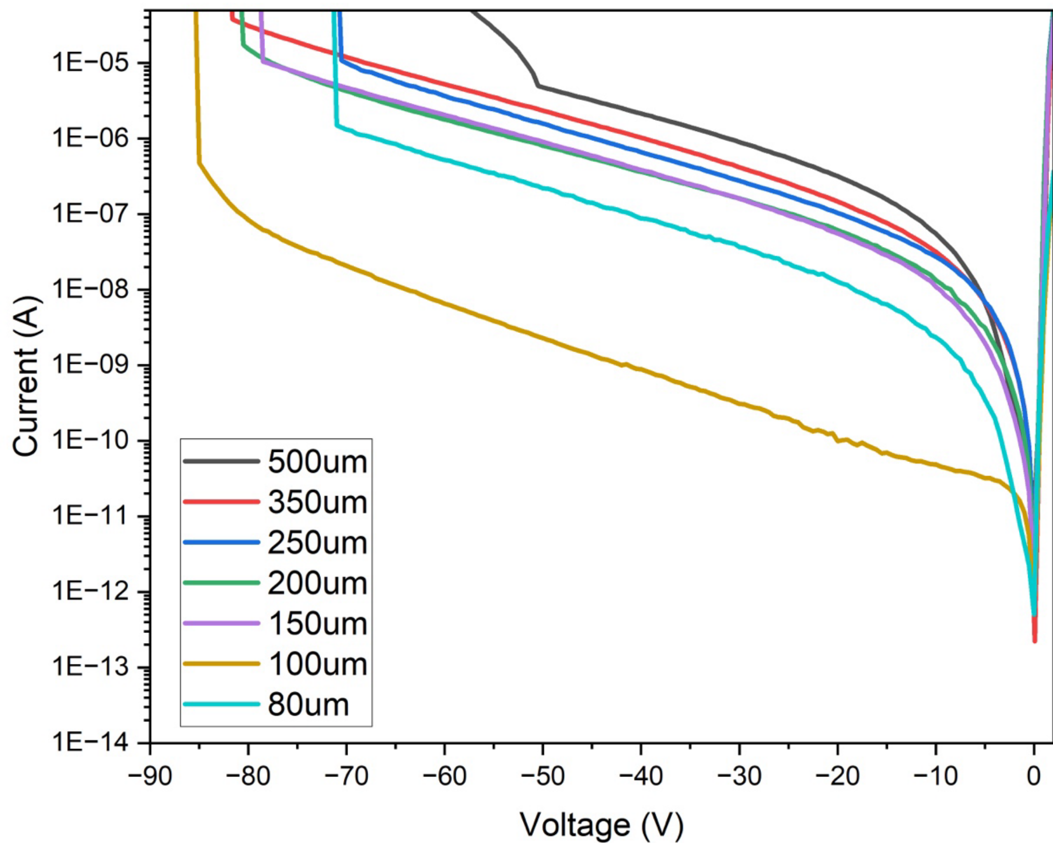

Figure 48. Zn-diffused AlGaAsSb mesa devices and their current-voltage behavior at 295 K with 90 minute diffusion time.

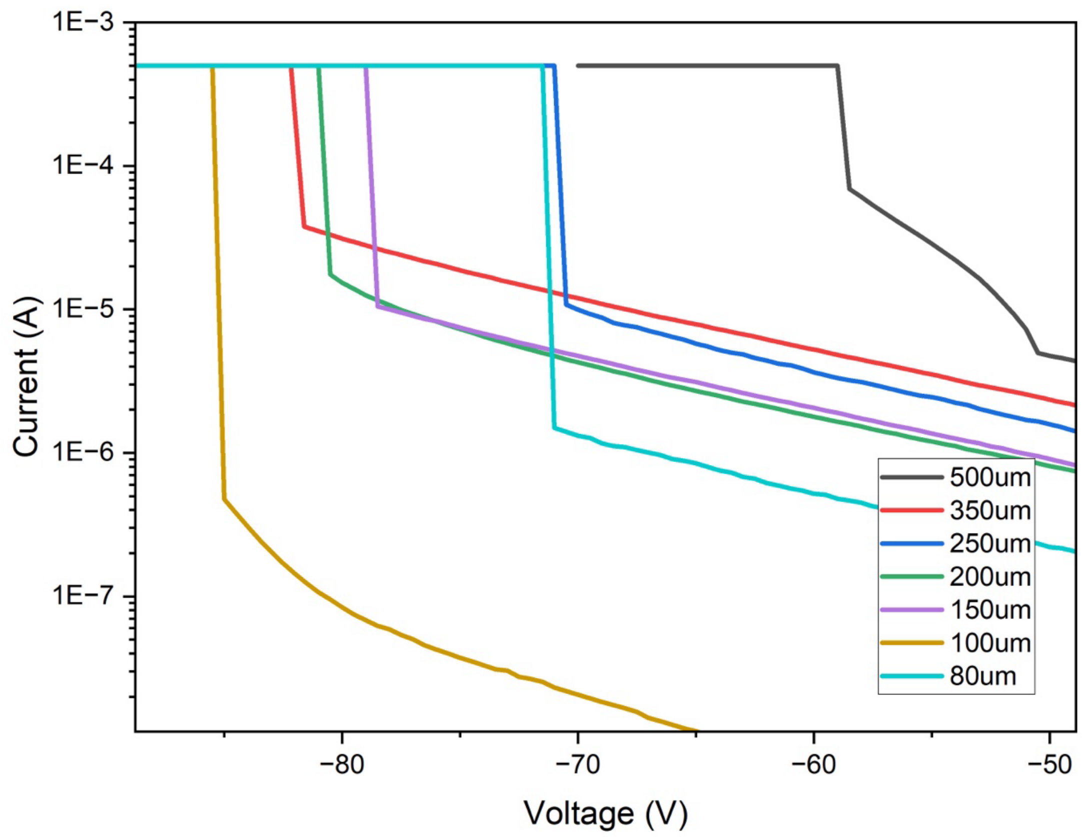

Figure 49. Zoomed-in device behavior of varying device diameters on the 90 minute diffusion time sample.

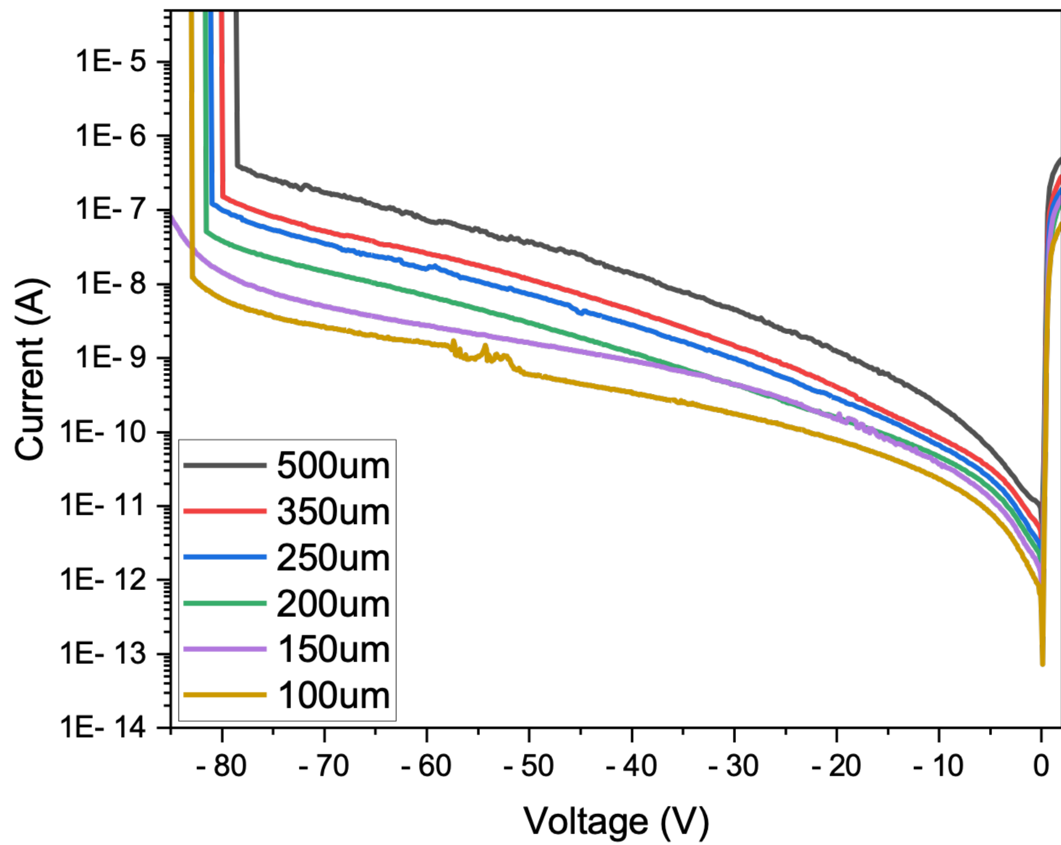

Figure 50. Zn-diffused AlGaAsSb mesa devices and their current-voltage behavior at 295 K with 20-minute diffusion time.

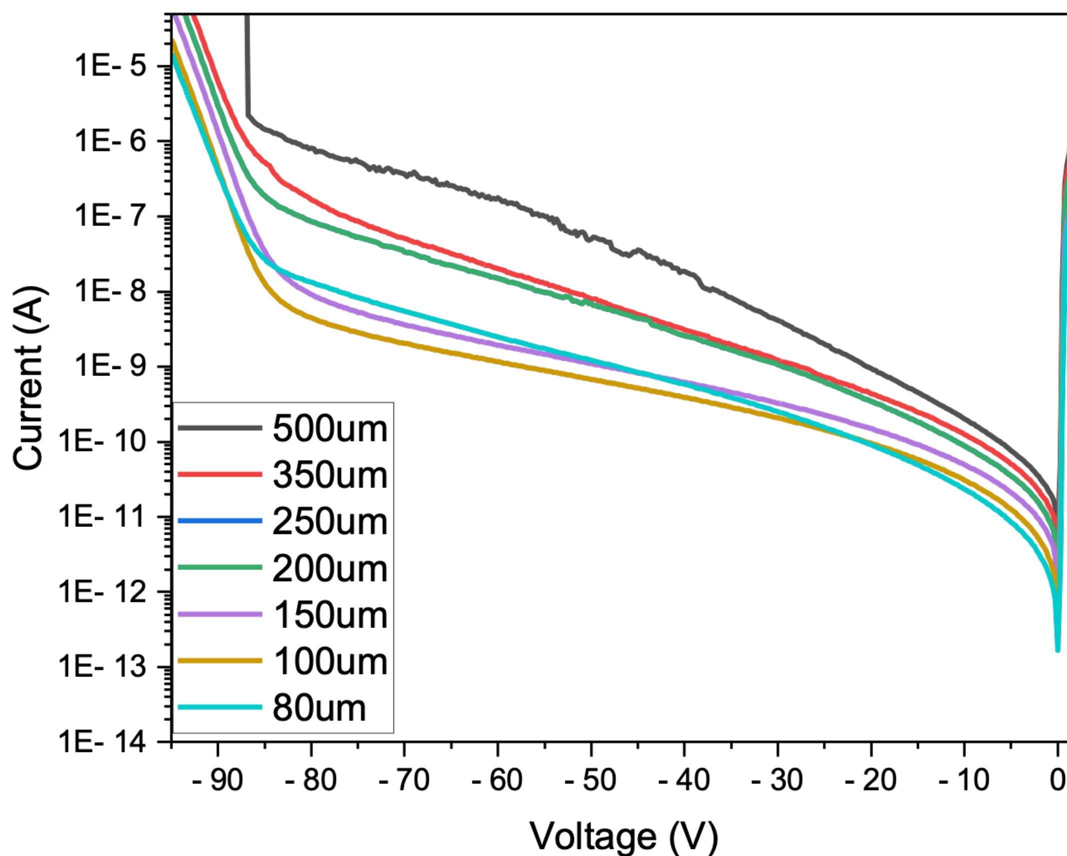

Figure 51. Zn-diffused AlGaAsSb mesa devices and their current-voltage behavior at 295 K with 10 minute diffusion time.

Based upon the results above, the 10-minute diffusion sample was the focus of further characterization. For the further characterization, I-V, C-V, and IVT were performed to glean an assessment of the device performance. Fig. 52 shows I-V performed on a 100 µm diameter device under both dark and overhead lamp illuminated conditions. The results obtained show promising potential, with the difference between the dark current

and the illuminated photocurrent being over an order of magnitude up until tunneling is introduced after – 85 V.

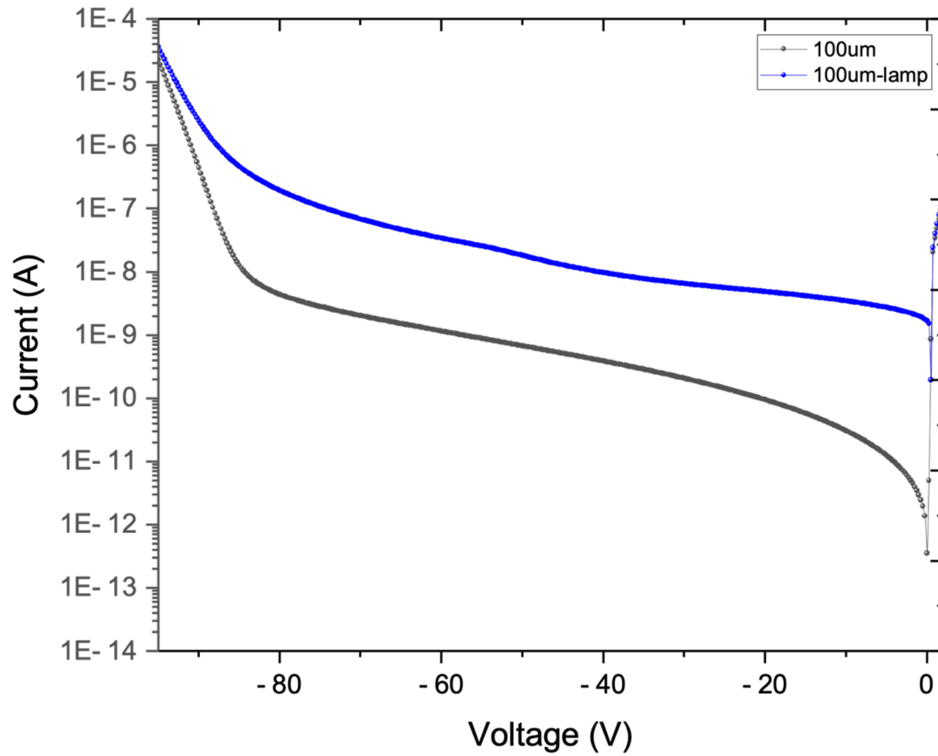

Figure 52. Dark current-voltage and lamp illuminated current voltage measurements on the 10-minute diffusion time sample for a 100 μm diameter device at 295 K.

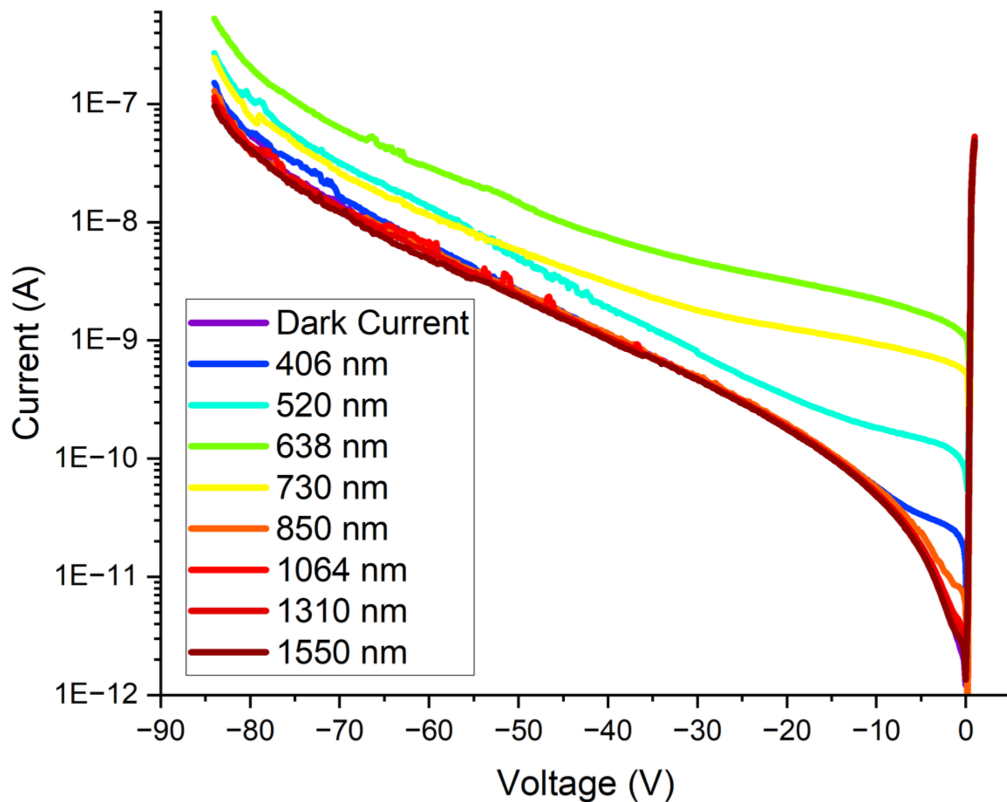

Figure 53. Current-voltage behavior of a 200 µm diameter device at 295 K under dark and illuminated conditions using different wavelengths to determine the bandgap energy.

To investigate the photocurrent behavior more extensively and accurately determine the bandgap energy of the Zn-diffused AlGaAsSb p-i-n, a study of device behavior under varying wavelengths of illumination was executed. Using Eq. 8, and previous work investigating the wider bandgap AlGaAsSb multiplier material, wavelengths between 406 nm and 1550 nm under maximum power were selected to measure a 200 µm diameter device at 295 K. First the device was measured under dark conditions, to determine its baseline I-V behavior, and then the device was illuminated at

each wavelength using a multi-channel laser and a tapered optical fiber to target the photoactive region of the device. With the knowledge of cutoff wavelengths, the device will only have a photoactive response to wavelengths that fall below the cutoff wavelength, given the bandgap energy of the material. Fig. 53 shows the behavior of this device and based upon this figure, it is evident that the Zn-diffused structure has a photo-response to lower wavelengths of illumination, notably between 520 nm and 730 nm. At 850 nm, the device no longer has a photo-response, thereby indicating that this wavelength is at or has surpassed the structure's cutoff. Using the lower limit of 730 nm and the upper limit of 850 nm in Eq. 8, the range where the bandgap energy was determined. Using these values, it was determined that the upper limit of the bandgap energy for the Zn-diffused AlGaAsSb p-i-n was approximately 1.699 eV and the lower limit was 1.45 eV, which is consistent with previous reports of the multiplier material with no Zn diffusion.

To provide a quantitative understanding of the device behavior and subsequently the gain achieved with the Zn-diffused mesa sample, current-voltage characterization was completed using 520 nm illuminated laser source at its maximum power for a 200 μm show below in Fig. 54. In this plot, gains were calculated assuming unity gain at approximately -45 V since the device was fully depleted at this voltage based upon capacitance-voltage measurements. With this unity gain selected a maximum gain of approximately 110 was achieved at a bias of -84 V. This shows promising performance since the device can be further pushed to achieve even higher gains.

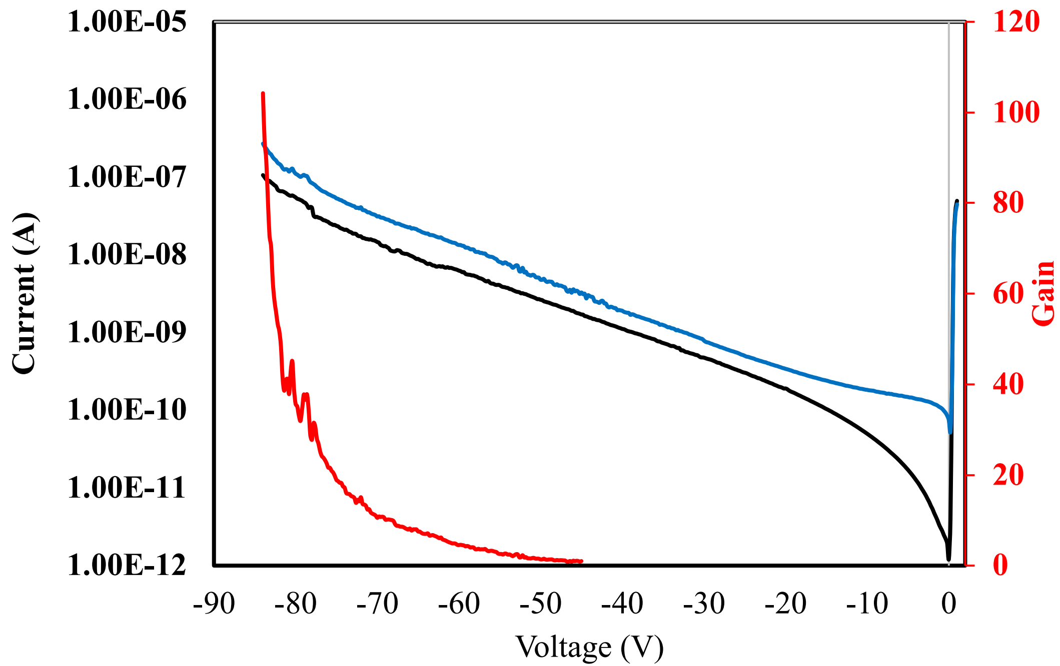

Figure 54. Dark current-voltage and 520 nm illuminated measurements and calculated gains on the 10-minute diffusion sample for a 200 µm device at 295 K.

Following this characterization, further I-V characterization was completed at 295 K across the varying sized devices to assess the voltages regimes where bulk and surface dark current dominate. Dark-current voltage measurements were completed at 295K in the VADA regions of the sample, with device sizes varying from 60 µm in diameter to 500 µm in diameter and can be seen in Fig. 55.

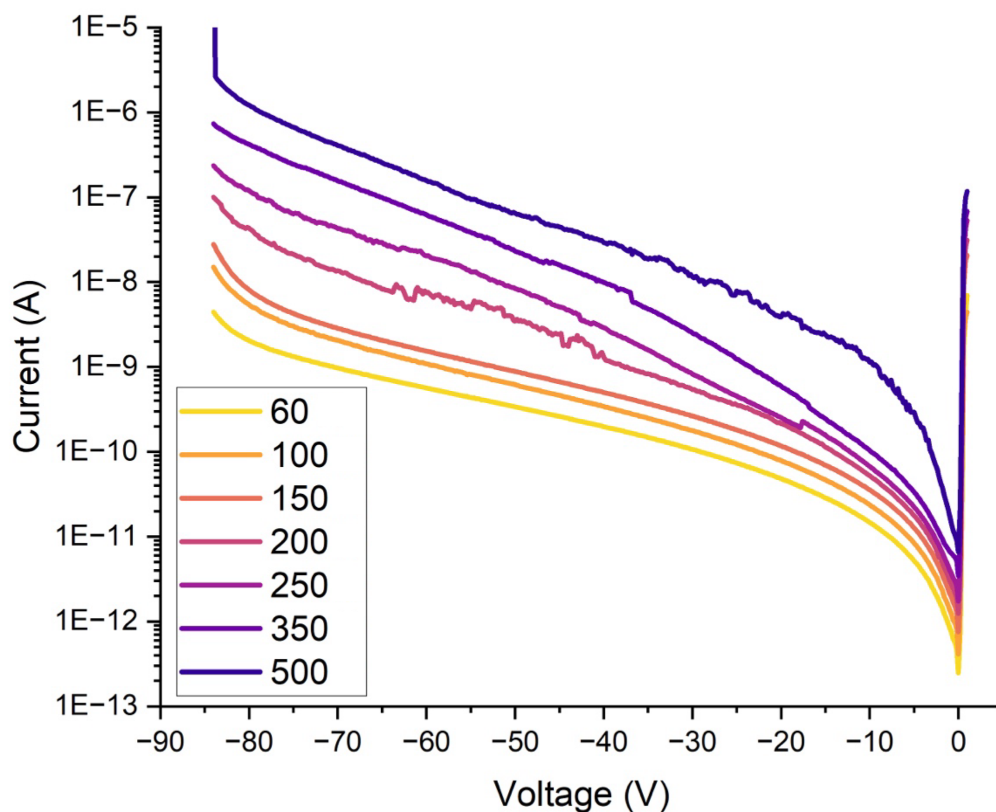

Figure 55. Dark current-voltage behavior at 295 K from varying sized diameter devices from 60 to 500 μm.

Using Eq. 10, the total dark current across the varying sized devices can be divided into either stemming from the bulk dark current or the surface dark current when accounting for differences in device area and perimeter. Fig. 56 shows the dark current when assessed with the perimeter (A/cm) across the devices to assess for the surface leakage dominating. Regions where the different devices are closely aligned with one another indicate that the dark current is dominated by that area of the structure. From Figure

56, it can be deduced that for small diameter devices until -70, the Zn-diffused AlGaAsSb is surface limited. This is consistent with the ratio of surface perimeter to device area being larger as device sizes are decreased. The devices that were 200 μm in diameter or larger did not align when adjusting for differences in perimeter. The larger devices do not fit this trend as closely and may be due to device-to-device variation or nonuniformity of the Zn-diffusion across the sample. Since this Zn-diffused AlGaAsSb investigation was completed as a mesa device architecture, it is understood that the etching to realize mesa devices may also be attributing to the surface leakage current dominating.

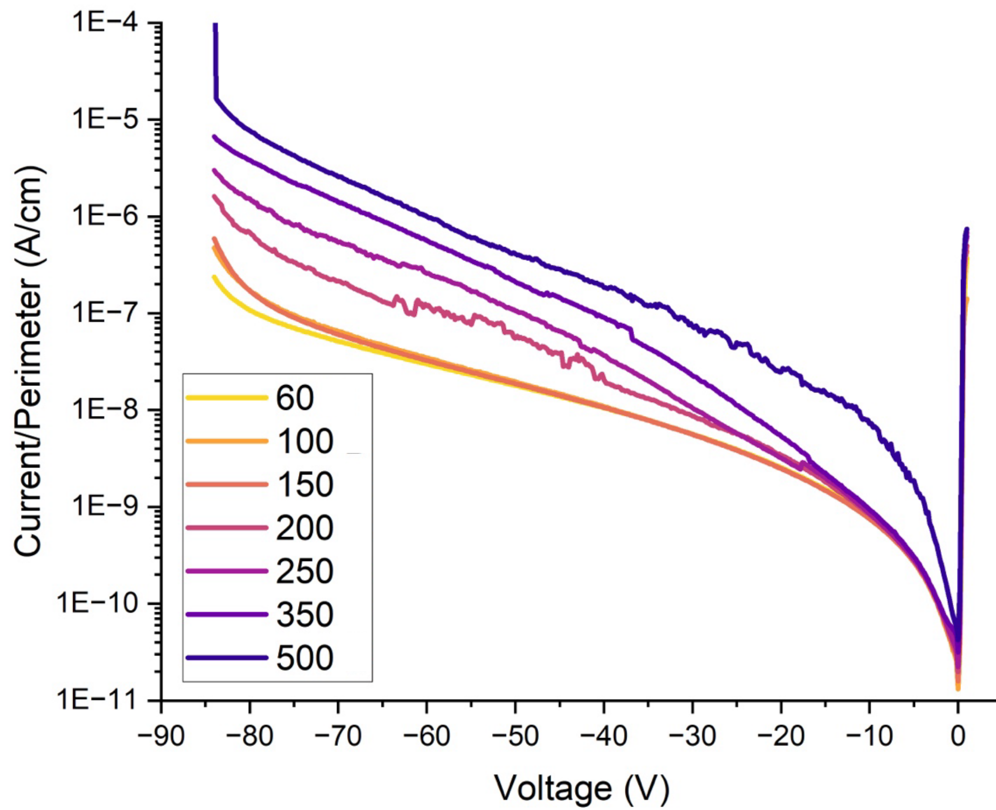

Figure 56. Current-voltage with differences in device perimeter at 295 K to determine if surface leakage current dominates the Zn-diffused mesa AlGaAsSb p-i-n.

To also investigate the bulk dark current component of the Zn-diffused AlGaAsSb, the dark current was assessed across the varying sized devices and their respective differences in area. Fig. 57 shows the behavior of current/area of the devices at 295 K. Unlike Fig. 56, device current-voltage behavior is not as aligned until high biases but 200, 250, and 350 µm do follow one another until -25 V, indicating that they are bulk limited at small biases. 500 µm remains both an outlier for both the perimeter and area assessments

of the VADA, likely due to being a poor performing device, which was confirmed by the high dark current and its premature permanent breakdown.

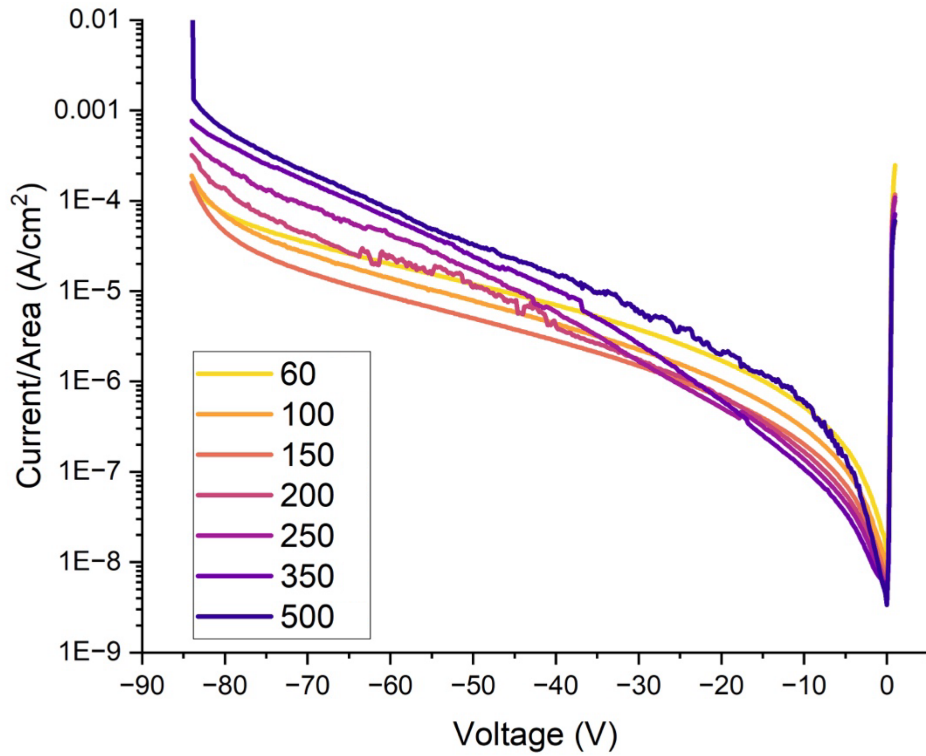

Figure 57. Current-voltage with differences in device area at 295 K to determine if bulk dark current dominates the Zn-diffused mesa AlGaAsSb p-i-n.

Capacitance-voltage measurements were then undertaken across the varying diameter devices at 1 MHz. Fig. 58 shows the capacitance-voltage behavior of the devices. It can be noted that 500 µm device was only measured to -55 V, due to abrupt irreversible breakdown. The capacitance values did not fully scale with area, further suggesting variation in the Zn-diffusion. An interesting observation was made across all devices except the 500 µm, whereby after the devices exhibit full depletion behavior and the capacitance stabilizes at approximately -50 V, it subsequently increases across all devices slightly. This behavior has not been observed before with typical non-diffused p-i-n and

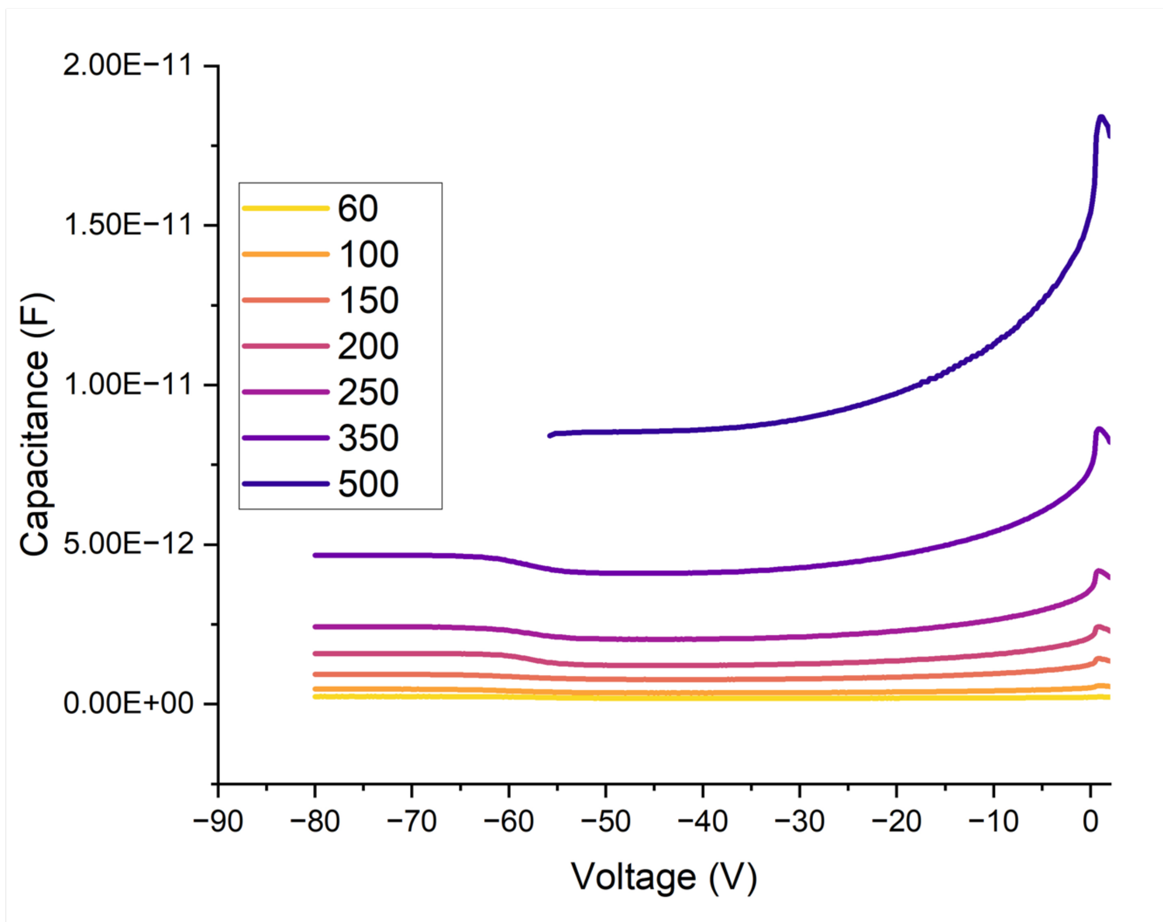

Figure 58. Capacitance-Voltage behavior of varying diameter devices at 295 K.

SACM APDs, and is being investigated further but may be resulting from higher doping in the n-type region following depletion of the intrinsic layer.

To quantify both the depletion width and the background carrier doping concentration, and thereby estimate the doping concentration of the Zn dopants into the structure, analyses were performed on 250 µm device that had a depletion width of 2440 nm at - 46 V and was calculated assuming a high frequency dielectric constant of 11.4. Figure 59 shows the capacitance and the depletion width with voltage for the 250 µm device. The background doping calculated for AlGaAsSb region was calculated to be approximately 1 x 10^{16} cm^{-3} at the maximum which indicates that if Zn dopants were able to diffuse sufficiently into the AlGaAsSb UID layer, their doping concentrations were very low, if the assumed background doping concentration of the AlGaAsSb UID region is approximately 5 x 10^{15} cm^{-3}.

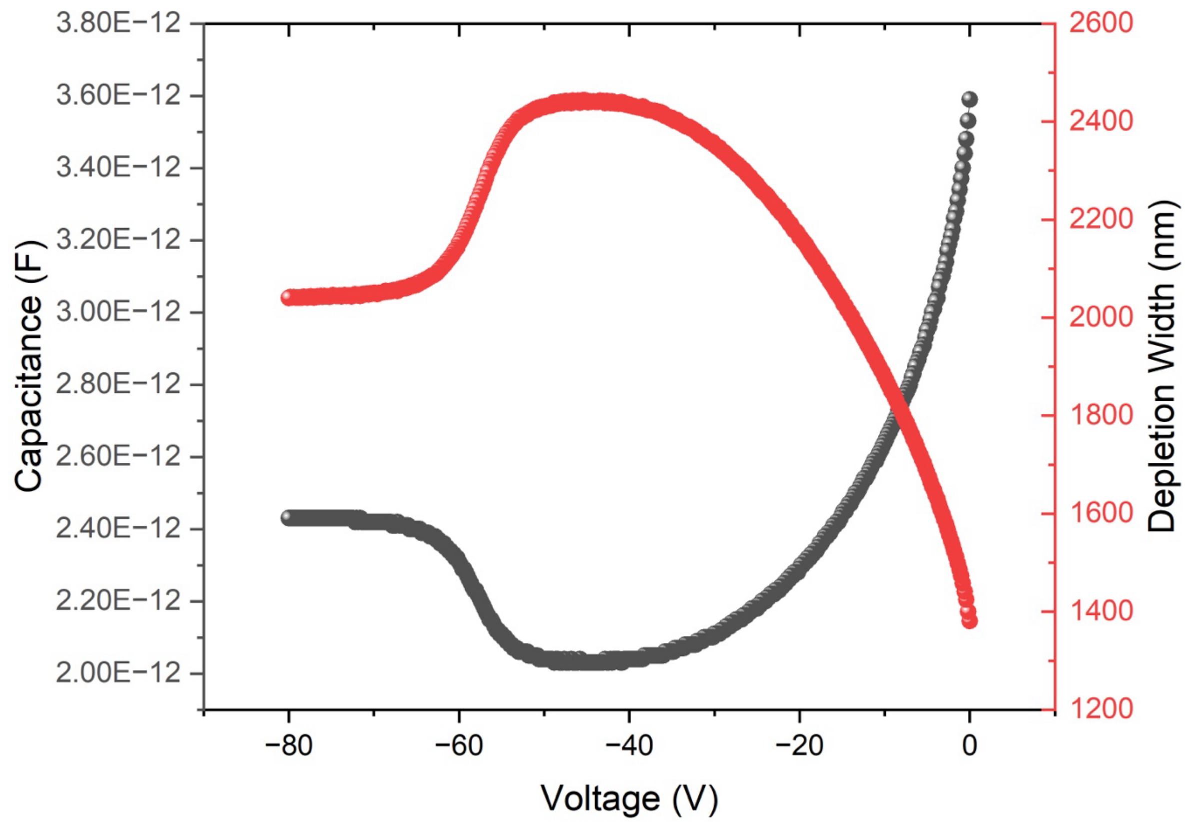

Figure 59. C-V and Depletion width with respect to reverse bias for a 250 μm device at 295 K.

While optimal operation for these devices is at higher operating temperatures to reduce SWaP-C, significant understanding is acquired by observing their behavior under cryogenic cooling, namely the dominate dark current mechanism within each temperature range. To accomplish this, dark IVT was taken for a 200 µm device from 20 K to 300 K, in 20 K step sizes to perform an Arrhenius analysis. Due to current floor limitations of the parameter analyzer, current measurements of the device at temperatures below 160 K could not be accurately assessed and were excluded from the subsequent analyses, ergo limiting the amount of data obtained on the Arrhenius. Fig. 60 shows the IVT behavior of the 200 µm device from 160 K to 300 K. Between 220 K and 300 K, there was an over 2 order of magnitude reduction in the dark current exhibited at high operating voltage of

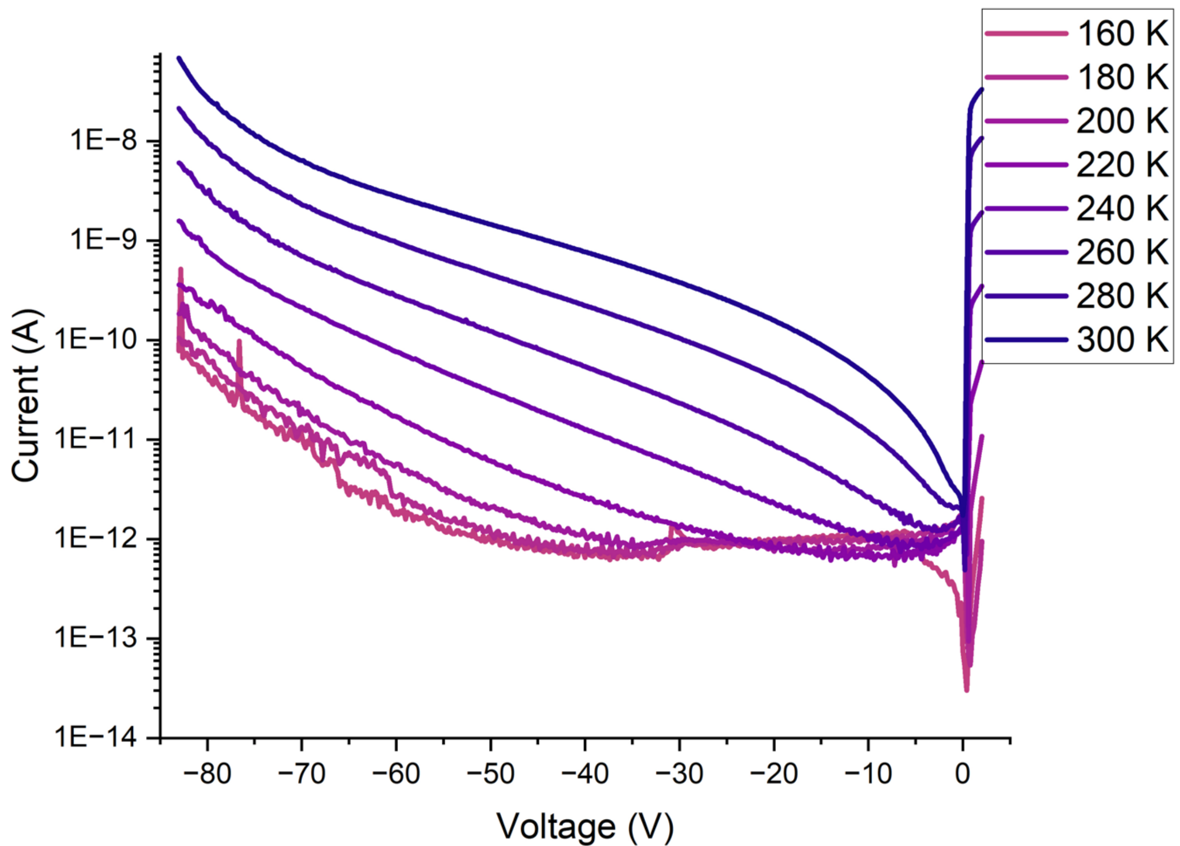

Figure 60. IVT behavior of 200 µm device from 160 K to 300 K.

approximately -83V, which is attractive for some applications that permit slight cooling for improved sensitivity.

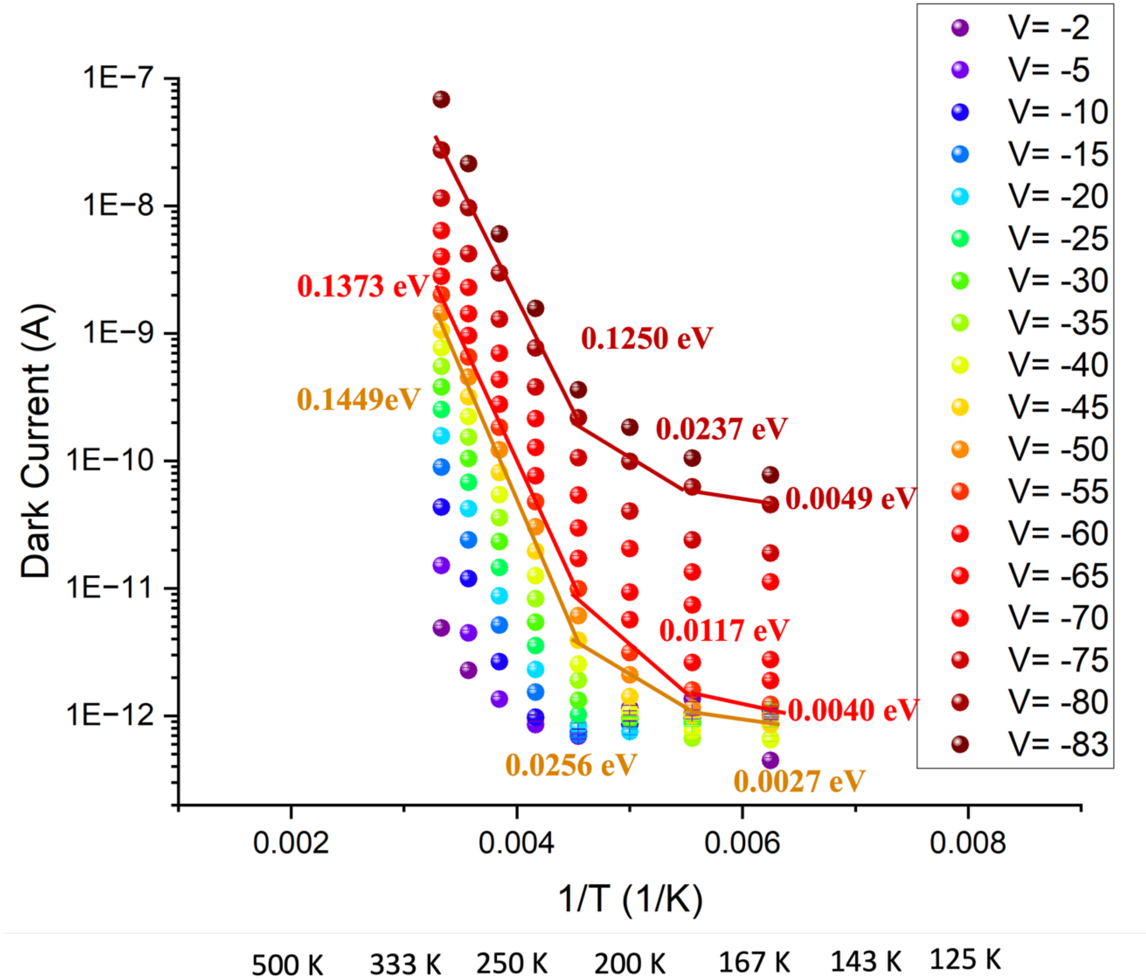

Figure 61. Arrhenius plot for the 200 µm device across voltages of interest.

From the IVT show above, an Arrhenius plot could be extracted for the 200 µm device, which plots the dark current as a function of 1/Temperature. Fig. 61 shows the Arrhenius extracted from the IVT and assesses the device's performance and dominate

dark current mechanism across a wide span of voltages where operation may occur for the device. To account for any variation in the measurement, 5 % error bars were in included in the plot. While many voltages plotted ranges from -2 V to -83 V, three were selected for determining the activation energy. First, -45 V was selected to represent the device behavior just prior to the unity gain, which has been observed to occur -46 V. For -45 V, from 220 K to 300 K, the activation energy was determined to be 0.1449 eV, and from 180 K to 220 K the activation energy was 0.0256 eV. At the lowest temperatures assess, the activation energy was 0.0027 eV for V = - 45 V. The next voltage assessed was V = -55 V, due to falling just past unity gain. Similar to V = - 45 V, at high operating temperatures, the activation energy was 0.1373 eV, 0.0117 eV between 180 K and 220 K and 0.0040 eV at the 160 K. To understand high voltage behavior of the devices, as they approach tunneling, V = -80 V was investigated. At high operating temperatures, the activation energy was 0.1250 eV, from 180 K to 220 K it was 0.0237 eV and finally, the activation energy was 0.0049 eV at 160 K. Although the values for each voltage for the high temperature regions is not half the bandgap energy, the structures behaves as if the dark current is G-R limited by drift in the depletion region as well as trap-assisted-tunneling[98].

Finally, the resistance was quantified for the Zn-diffused mesa sample using a Transfer Length Measurement (TLM) method of implementing uniform rectangular structures on the sample and varying the spacing distance in micrometer between them. Using this method, the contact resistance, sheet resistance, semiconductor resistance, total

resistance, contact resistivity and transfer length can be approximated. For the Zn-diffused AlGaAsSb mesa sample for 30 minute diffusion, Table 5 shows these values.

Table 5. TLM extracted data for the Zn-diffused AlGaAsSb sample.

Parameter	**Value**
Contact Resistance, R_c	$1.07946*10^{-9}$ Ω
Sheet Resistance, R_s	$3.18048*10^{-11}$ Ω
Semiconductor Resistance, R_{semi}	$3.9756*10^{-12}$ Ω
Total Resistance, R_T	$2.1629*10^{-9}$ Ω
Transfer Length, L_T	6788.03 μm
Contact Resistivity, ρ_c	$1.46548*10^{-3}$ $\Omega * \mu m^2$

5.5 Analyses

Based upon the results discussed, this is the first report of a Zn-diffused AlGaAsSb p-i-n on semi-insulating substrate and has been deemed successful, given that the current-voltage behavior exhibited rectification and low dark current. In this work, it has been concluded that a shorter diffusion time greatly reduces the dark current in the structure, and likely results from more controlled diffusion of the Zn dopants.

Through the VADA assessment, it was deemed that the devices exhibit surface leakage dominating the performance at low biases prior to tunneling occurring in the device. The high surface leakage current is likely a combination of the diffusion processing as well as the etching to delineate the mesa devices. Exploring a Zn-diffused AlGaAsSb that has a planar architecture would provide insight into this further.

To form a comparison of the Zn-diffused AlGaAsSb mesa structure to previously reported AlGaAsSb p-i-n devices and their respective performance characteristics, Table 5 is shown below. In this table, the Zn-diffused AlGaAsSb is compared against both a digital alloy grown AlGaAsSb p-i-n structure employing a 1000 nm intrinsic region, and a random alloy grown AlGaAsSb p-i-n structure employing a 910 nm intrinsic region. Although the structures differ in intrinsic region thickness. Although the differences in i-region thickness do not provide a one-for-one comparison, it does provide an estimate of performance of devices both grown and fabricated at Ohio State, now utilizing Zn-diffusion. From Table 6, it is evident that the Zn-diffused mesa has a significantly higher breakdown voltage, over -100 V, compared to the other two devices that reached their breakdown voltages at -53 and -58 V for the DA and RA structures, respectively. The significant push in breakdown voltage is likely due to the much thicker i-region of the Zn-diffused mesa at 2000 nm. With the larger available voltage range of the Zn-diffused mesa, significantly higher gains could be obtained. The gains achieved for the Zn-diffused mesa are over 2 times larger than that of the DA structure and over 5 times larger over the RA p-i-n[43,44]. The gain normalized dark current density was also determined for the structures,

normalizing their differences in device diameter, and achieved gains. The Zn-diffused structure had a gain normalized dark current density of approximately 1.157×10^{-3} A/cm^2, while the DA and RA structures had gain normalized dark current densities of 9.45×10^{-6} and 4.455×10^{-6} A/cm^2, respectively. The discrepancies in gain normalized dark current density arise from differences in achieved current values at the highest voltages reported. The DA and RA structures experiences abrupt irreversible breakdown at lower voltages whereby they had lower dark current, which was not the case for the Zn-diffused mesa. Finally, the excess noise at a gain of 10 was compared for structures. Both the DA and RA p-i-ns had excess noise factors of approximately 2 at gains of 10, demonstrating their low-noise behavior. Although the Zn-diffused mesa structure was tested for the excess noise behavior, measurements were unsuccessful due to device instability under high voltages to realize gain for an extended period of time. This could likely be mitigated going forward with processing optimization. Despite the excess noise challenges of the Zn-diffused mesa, it is likely that the realized excess noise behavior at gains of 10 will be similar or decreased to the to other structures, since the *k*-value to determine the excess noise factor is a material parameter. Lastly, the ideality factor was obtained for the Zn-diffused AlGaAsSb structure by assessing the forward bias characteristics across several devices at 295 K. From Eq. 14, the ideality factor was calculated to be within the range of 1.701 and 2.019 and has been determined that the recombination type is likely Shockley-Read-Hall and band-to-band under high injection and is likely limited by both the majority and the minority carriers.

Table 6. Comparison of Zn-diffused AlGaAsSb p-i-n to previously reported AlGaAsSb p-i-n structures.

Structure	**This Work**	**1000 nm UID Digital Alloy $Al_{0.85}Ga_{0.15}As_{0.54}Sb_{0.46}$[43]**	**910 nm UID Random Alloy $Al_{0.85}Ga_{0.15}As_{0.54}Sb_{0.46}$[44]**
Breakdown Voltage	> -100 V	-53 V	-58 V
Gain Normalized Dark current density at V_{Br} (A/cm^2)	1.157×10^{-3} (at -100 V)	9.45×10^{-6}	4.455×10^{-6}
Maximum Gain	110	42	20
Excess Noise at *M*=10	N/A	>2	~ 2

5.6 Technical Challenges

This worked demonstrated the feasibility of Zn-diffusion into the AlGaAsSb multiplier material with the eventual integration into a planar APD device. While the Zn-diffusion was very encouraging, additional work and growths are required to determine its feasibility in a planar structure. This could not be fully investigated in this study, due to the InP substrate being semi-insulating and not enabling proper conduction for a back metal contact, which is required in a planar structure. Follow on work requires a regrowth of the structure to circumvent this issue and demonstrate Zn-diffused planar AlGaAsSb devices. One challenge that was not heavily investigated but should be further considered with future work is the furnace atmosphere. While forming gas has been investigated to promote diffusion more productively than the inert atmosphere, alternative gases such as N_2 may improve the diffusion. Additionally, more accurate low temperature measurements would greatly improve understanding the full device dark current behavior and should be further assessed with alternative equipment that has a lower current floor. The structure was also assessed for measuring excess noise and NEP; however the device performance was not stable and operating at high voltages over a long period of time due to the high electric fields at the corners of the mesa. Follow fabrications may resolve this issue and provide meaningful data on the overall signal and noise components of the Zn-diffused AlGaAsSb structure.

One of the most pressing technical challenges in regard to this work is accurately quantifying the depth and concentration of Zn dopants. One method to do is through SIMS, which is unavailable at OSU and therefore requires significant time and resources to perform elsewhere but is worth future work investigating.

Chapter 6. Planar GaAsSb/AlGaAsSb SACM Avalanche Photodiodes on InP Substrates

In Chapter 5, Zn-diffusion into a AlGaAsSb p-i-n structure was investigated and displayed promising rectifying behavior and low dark current values which confirm that the diffusion process was successful. Since the motivation is to develop high performing APDs as an SACM structure, work has been completed investigating Zn diffusion into an SACM. Previous work has demonstrated ultra-high gain at room temperature (M = 278), low excess noise and temperature stability of a $GaAs_{0.5}Sb_{0.5}/Al_{0.85}Ga_{0.15}As_{0.56}Sb_{0.44}$ SACM APD for 1550 nm detection using mesa architecture devices[58]. While this performance is encouraging, there is motivation to target gains up to 500, whereby Geiger-like mode single photon detection may be achieved and is particularly attractive for photon starved applications. To assist in obtaining higher gains, planar devices are being considered to eliminated the surface leakage and push the breakdown voltage to higher biases. In conjunction with the planar device, Zn-diffusion is also be investigated for SACM structure, which is novel and has never been reported previously in literature on III-V APDs.

6.1 Design

To investigate a planar Zn-diffused GaAsSb/AlGaAsSb SACM structure, a study was developed to assess the differences in diffusion time to encourage sufficient Zn-diffusion into the GaAsSb absorber. Two samples of the GaAs/AlGaAsSb SACM structure

were processed to determine their performance characteristics with adjusted in the diffusion time. The second processed material also had devices with guard rings considered in the mask design which are often reported with planar devise to prevent premature edge breakdown[135,136,137,138,139]. Similar to the Zn diffusion process, several variables can be investigated in regard to guard rings to achieve the lowest dark current, namely the thickness of the guard ring, and the spacing of the guard ring from the device under test.

6.2 Growth

The SACM APD was grown via MBE by IntelliEPI and Table 7 shows the structure. The material was previously designed for mesa device architecture and as a result, included p-doped contact layers. The GaAsSb absorber was selected to be especially thick at 2000 nm to reduce the likelihood of carriers tunneling, thereby driving dark current up quickly, and to increase the quantum efficiency obtained for the structure. To transport electrons from the narrower bandgap GaAsSb absorber to the wider bandgap AlGaAsSb multiplier, the structure was graded over 150 nm where the Al composition was increased from $x = 0$ to $x = 0.85$. A thin p-type doped AlGaAsSb was then implemented to serve as the charge layer and quickly increase the electric field to the multiplier. The multiplier was then grown as 1000 nm thick layer.

Table 7. MBE Grown GaAsSb/AlGaAsSb SACM APD on InP Substrates.

Layer	Material	Doping Concentration and Polarity (cm^{-3})	Thickness	Purpose
1	InGaAs	1E19, P++	20	P-contact layer
2	InAlAs	2E18, P+	100	Blocking layer
3	GaAsSb	UID	2000	Absorber Layer
4	GaAsSb → AlGaAsSb	UID	150	Grading Layer
5	AlGaAsSb	2.7E17, P	110	Charge Layer
6	AlGaAsSb	UID	1000	Multiplier Layer
7	AlGaAsSb	2E18, N+	100	Field Control Layer
8	InGaAs	1E19, N++	500	N-contact Layer
9	InP	N	-	Substrate

Fig. 62 below shows the SACM structure's band diagram which was simulated under no applied bias. The regions of the band diagram that align with the various layers of the structure are marked in the figure.

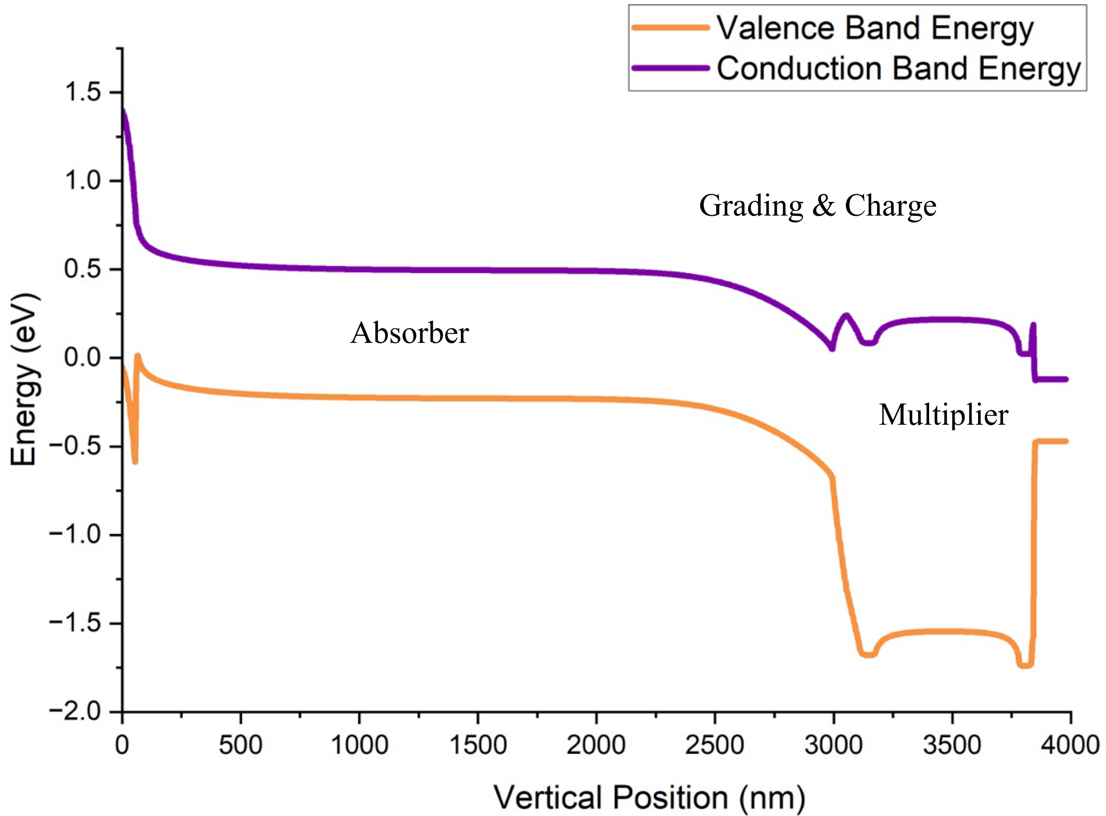

Figure 62. Simulated Band diagram of GaAsSb/AlGaAsSb SACM APD under no applied bias.

6.3 Fabrication

Since the material was already grown for processing mesa structure devices, it had to first be prepared for a p-type Zn diffusion into the GaAsSb absorber via removing the top p-type contact and p-type blocking layer through a wet etch chemistry of citric/H_2O/H_3PO_4/H_20_2. Once removed, the sample was coated with SiN_x by using a Plasma

Enhanced Chemical Vapor Deposition (PECVD) tool to deposit 150 nm of SiN_x. The SiN_x served as a hard mask to indicate areas of Zn-diffusion for the planar devices. After SiN_x deposition, the sample underwent a photolithography process using S-1813 as the photoresist and a maskless aligner to expose circular features on the sample. Once the features were present, the SiN_x thickness was then verified and sufficiently removed from the sample using a plasma etcher. After the SiN_x removal, the sample was ashed to remove any remaining photoresist residue prior to the ZnO deposition.

The sample was then placed in the ALD for the ZnO deposition. 150 cycles was selected to deposit 30 nm of ZnO onto the sample and the substrate temperature for deposition was set at 150 C. Following the ZnO deposition, the thickness was verified using a Si reference chip and an ellipsometer. The Zn was then diffused into the structure under 20 sccm of forming gas at 400 C. The first sample was in the furnace tube for 90 minutes while the second sample was in for 30 minutes. Following the Zn diffusion, the sample underwent a second photolithography step where it was coated with LOR5A lift off resist and S-1813 and exposed once more in the maskless aligner to fully realize individual regions of devices on the sample and define metal contact regions. Finally, Ti/Au (12/150 nm) was deposited for the metal contacts on the front of the sample and blanketed coated on the back of the n-type InP substrate for the back contact. Fig. 63 shows the overarching steps of the Zn-diffusion and planar processing of the GaAsSb/AlGaAsSb SACM structure.

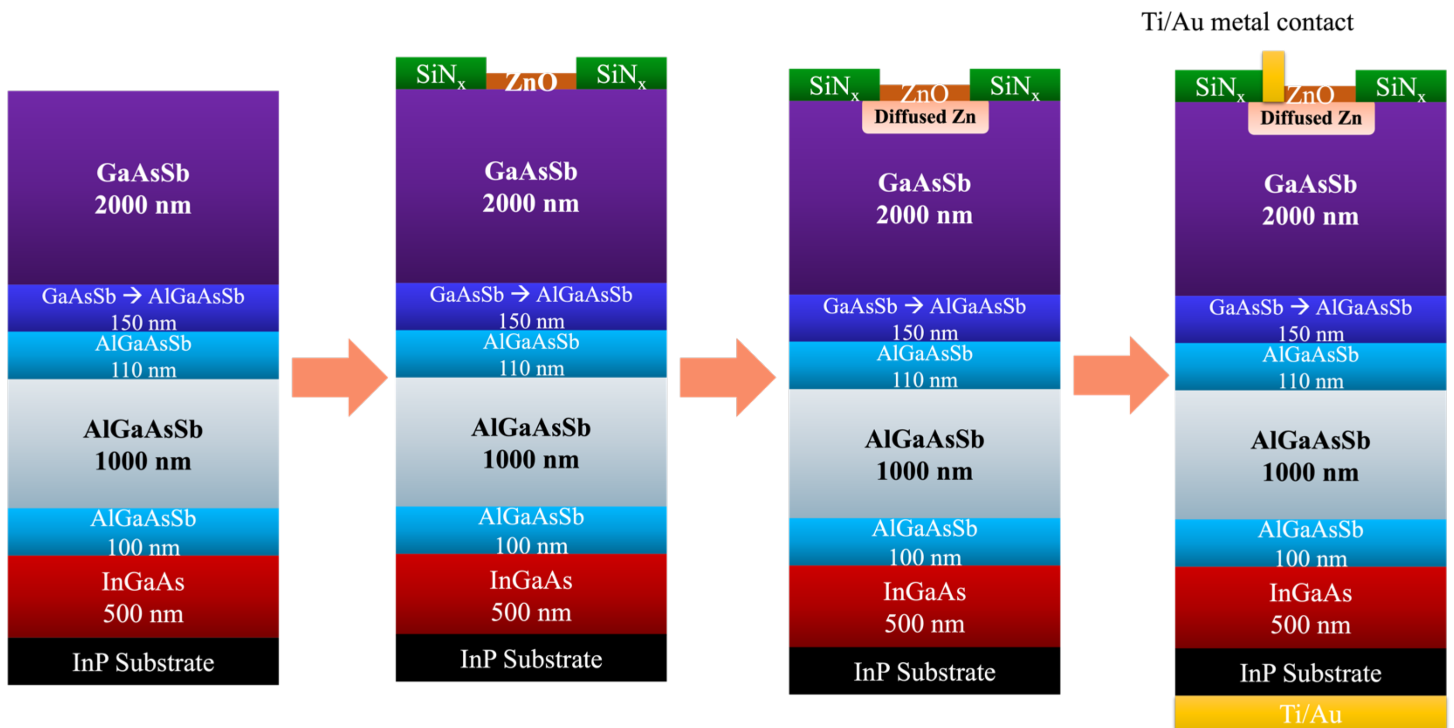

Figure 63. Overarching diffusion and planar fabrication processing of the GaAsSb/AlGaAsSb SACM APD on InP Substrate.

6.4 Characterization

First, characterization was completed at room temperature for the 90 minute and 30 minutes samples to determine their dark current behavior. Fig. 64 shows the dark current behavior at 300 K for the 90-minute diffusion sample and Figure 65 shows the behavior for the 90-minute sample under slightly cooling at 260 K to determine if any reduction in dark current could be achieved.

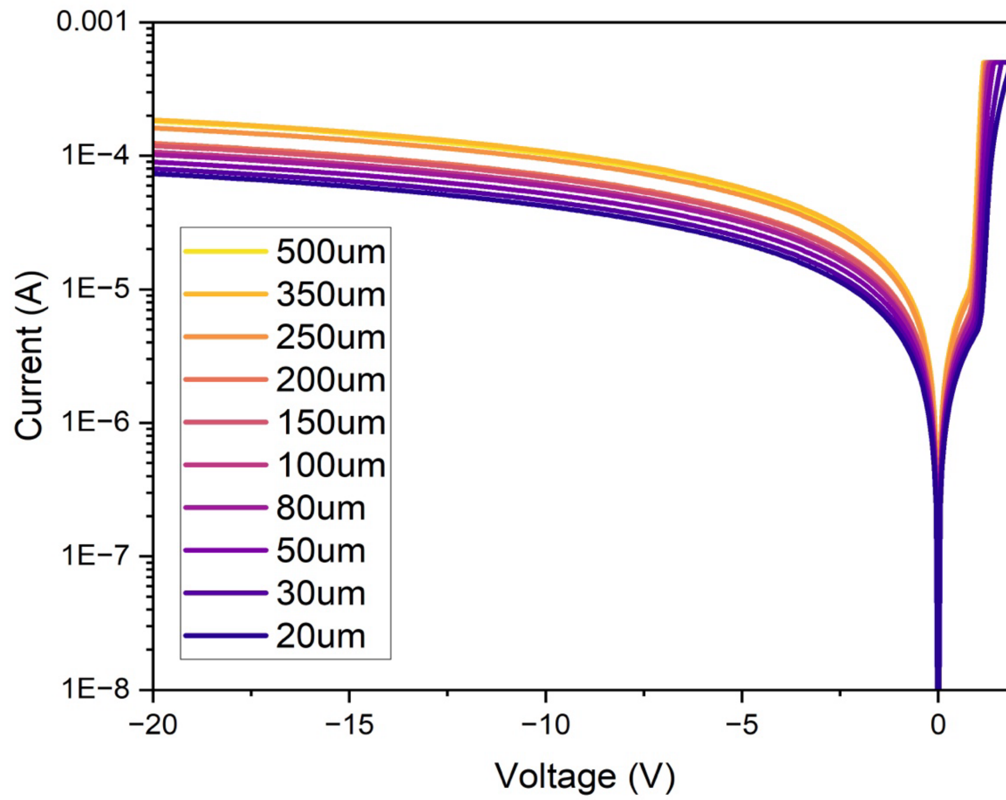

Figure 64. Zn-Diffused GaAsSb/AlGaAsSb SACM APD Dark current behavior at 300 K with 90-minute diffusion time.

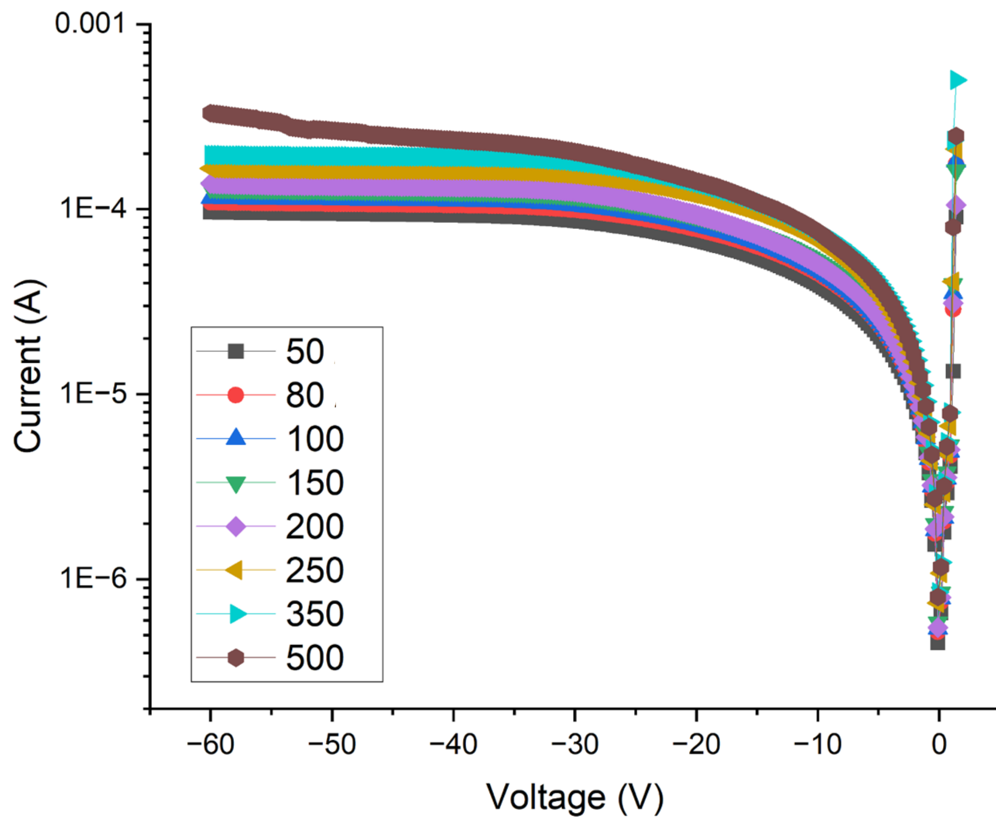

Figure 65. Zn-diffused GaAsSb/AlGaAsSb SACM APD Dark current behavior at 260 K with 90 minute diffusion time.

To realize the cooled behavior of the 90-minute diffused sample and current-voltage performance across varying devices, cooled measurements were completed at 20 K and are shown in Fig. 66 below. From this figure, several observations regarding the Zn-diffusion and planar processing of the GaAsSb/AlGaAsSb SACM APD could be identified. First, although a reduction in dark current was seen in all devices compared to Fig. 64,

devices with diameters of 200 μm and smaller exhibited over a two order magnitude reduction in dark current, while the larger sized devices experiences a smaller reduction in dark current. This may be attributed to a higher likelihood of Zn-diffusion nonuniformity in the larger sized devices, or higher likelihood of defects being present in larger sized devices. When performing a VADA to determine whether the dark current at 20 K was dominated by surface or bulk dark current chiefly, neither type of dark current was more significant than the other. This concludes that the 90-minute diffused planar devices exhibit both high dark current stemming from the bulk as well as the surface leakage.

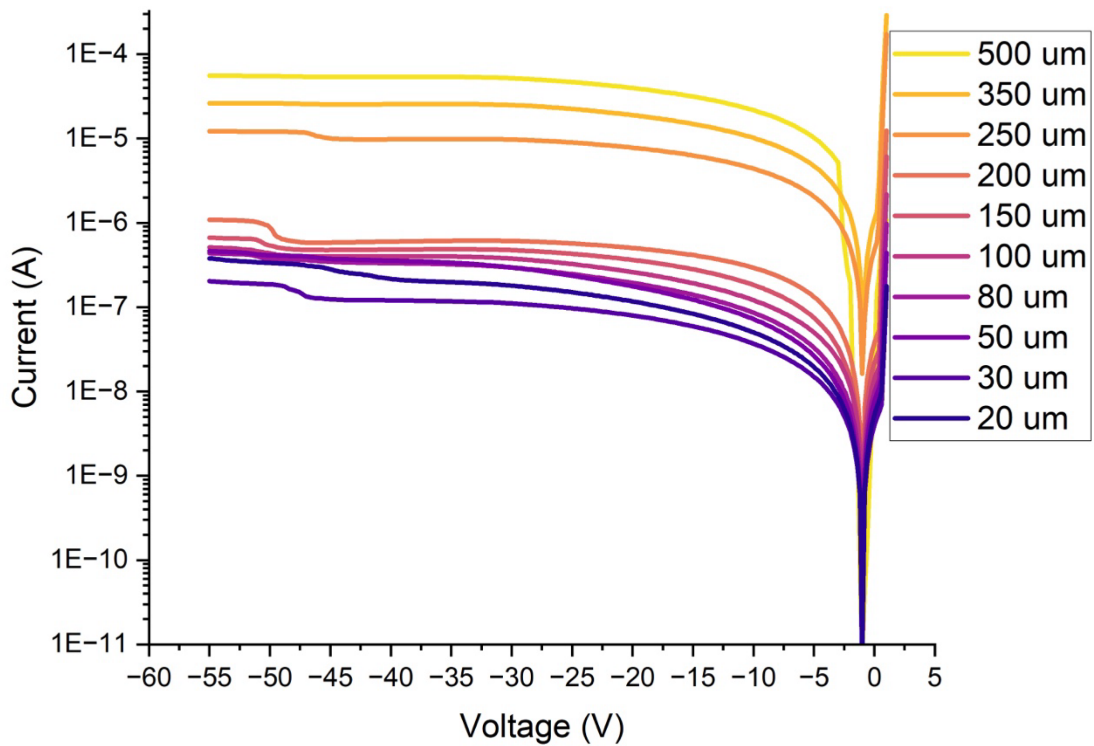

Figure 66. Current-Voltage behavior for varying diameter devices at 20 K with a 90 minute diffusion time.

Based upon the results shown above in the figures, it was determined that the 90-minute diffused sample significant dark current behavior across all device sizes, likely resulting from excessive lateral diffusion of the Zn atoms. To improve this, the 30-minute diffusion time was investigated, with the hypothesis that a reduction in diffusion time may reduce the dark current, as evident in Chapter 5's findings. To account for the difficulties with planar devices and to improve device performance, a guard ring section of the sample was included in the 30-minute fabrication. A guard ring, which can seen in Fig. 67, is a metallized ring that surrounds that device under test and can be diffused similar to the device. The guard ring serves as an alternative conductive pathway for electrons to go to, driving current away from the device itself and enabling higher voltage operating and lower dark current. The guard rings reduce the curvature of the depletion region within the device under its perimeter and thereby reduce the magnitude of the electrical field as well. As a result, a reduction in surface electric field is achieved and the voltages can be pushed further for operation due to the breakdown voltage increasing. Fig. 68 shows the electric field under the planar device and at its p-n junction with the presence of a single guard ring.

To achieve the highest performance of the planar device, much work has focused on the variables of the guard ring, notably metal thickness, and distance away from the device.

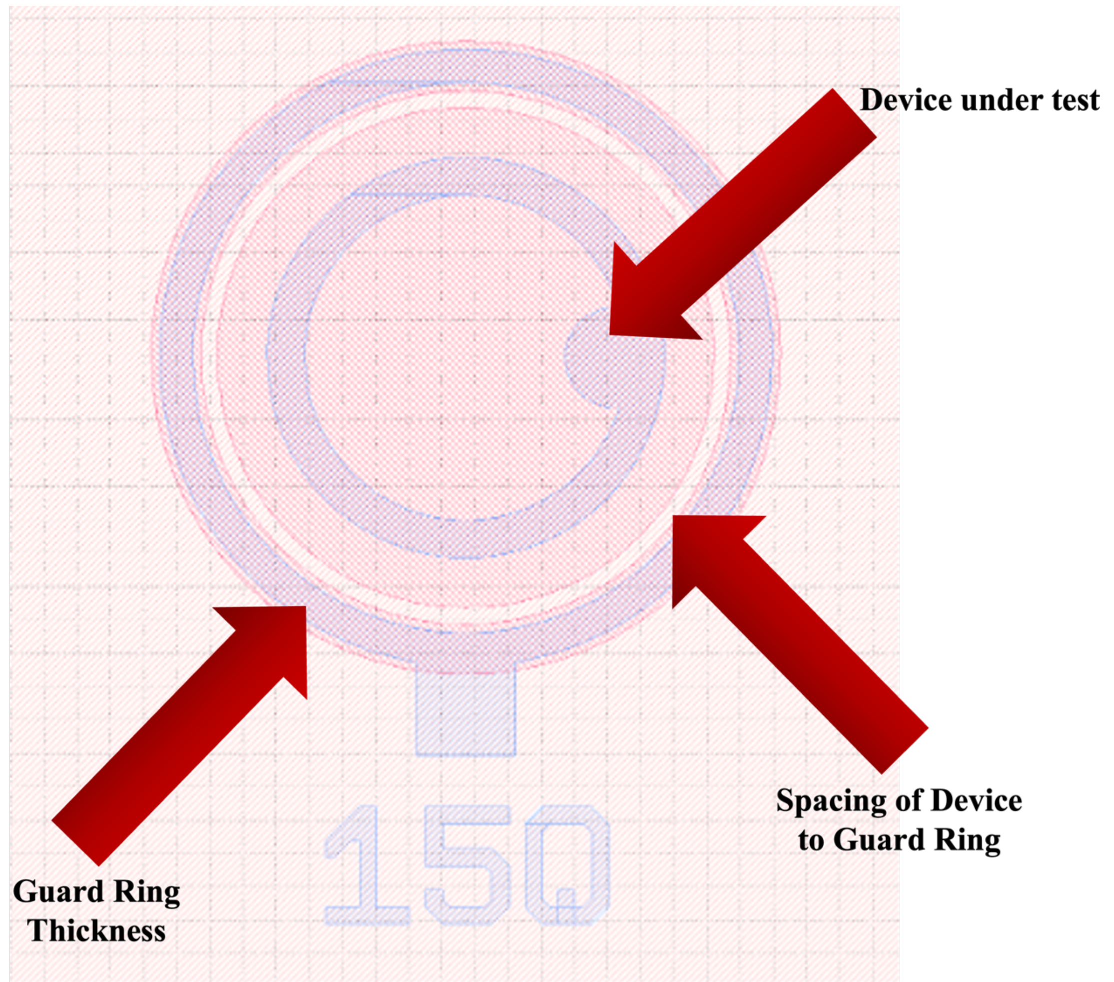

Figure 67. Circular planar device fabricated with guard ring.

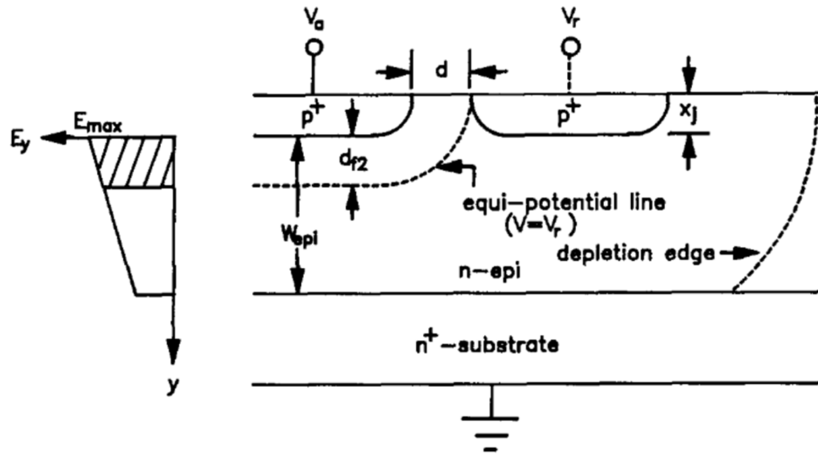

Figure 68. Guard ring surrounding planar device[139].

To investigate the performance of planar devices on the 30 minutes diffusion time sample both with and without the presence of floating guard rings, an alternative mask design as implemented. In this mask, areas were allocated to various floating guard ring conditions for 50 µm diameter devices. Floating guard ring thicknesses of 5, 10, 15, and 20 µm were selected. For the spacing distance between the device under test and the guard ring, distances of 5, 7.5, 10, 12.5, 15, and 17.5 µm were selected. With the combinations of available guard ring thicknesses, and spacing distances, 24 different variations were measured for their respective influence to the device's dark current performance. Table 8 shows the combinations available for illustration.

Table 8. Metal Guard Ring Thickness and Guard Ring Spacing from 50 μm devices

Metal Guard Ring Thickness (μm)	*Guard Ring Spacing Away from Device (μm)*				
5	5	7.5	10	12.5	17.5
10	5	7.5	10	12.5	17.5
15	5	7.5	10	12.5	17.5
20	5	7.5	10	12.5	17.5

On the 30-minute sample, devices both with and without guard rings were present and could be characterized for their performance. Fig. 69 and Fig. 70 show varying diameter circular devices on the 30-minute sample both with and without guard rings present and their respective dark current-voltage behavior at 300 K. Although the reduction in diffusion time from 90 minutes to 30 minutes did not significantly reduce the dark current at room temperatures, the presence of guard rings on the 30-minute diffusion sample did cluster the dark current plots across the different device sizes, indicating that they were successful in reducing the electric field within the device. This was consistent across the varying devices and their differences in diameters.

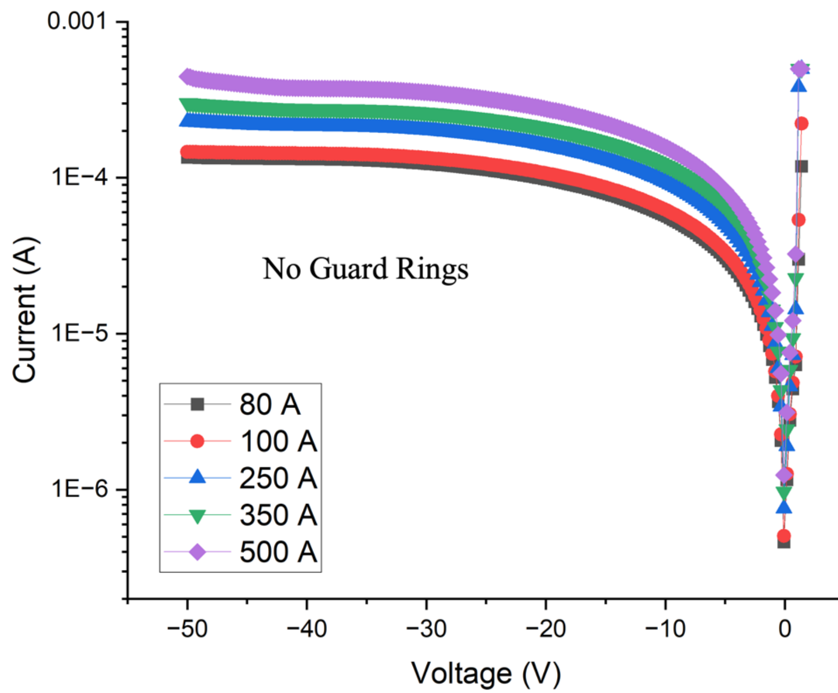

Figure 70. Planar Devices on the 30 minute sample without guard rings present at 295 K.

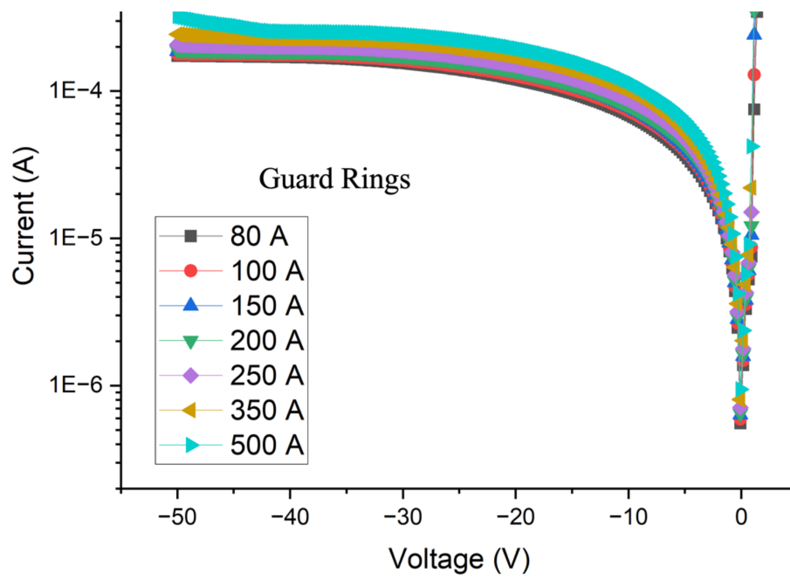

Figure 69. Planar Devices on the 30-minute sample with guard rings present at 295 K.

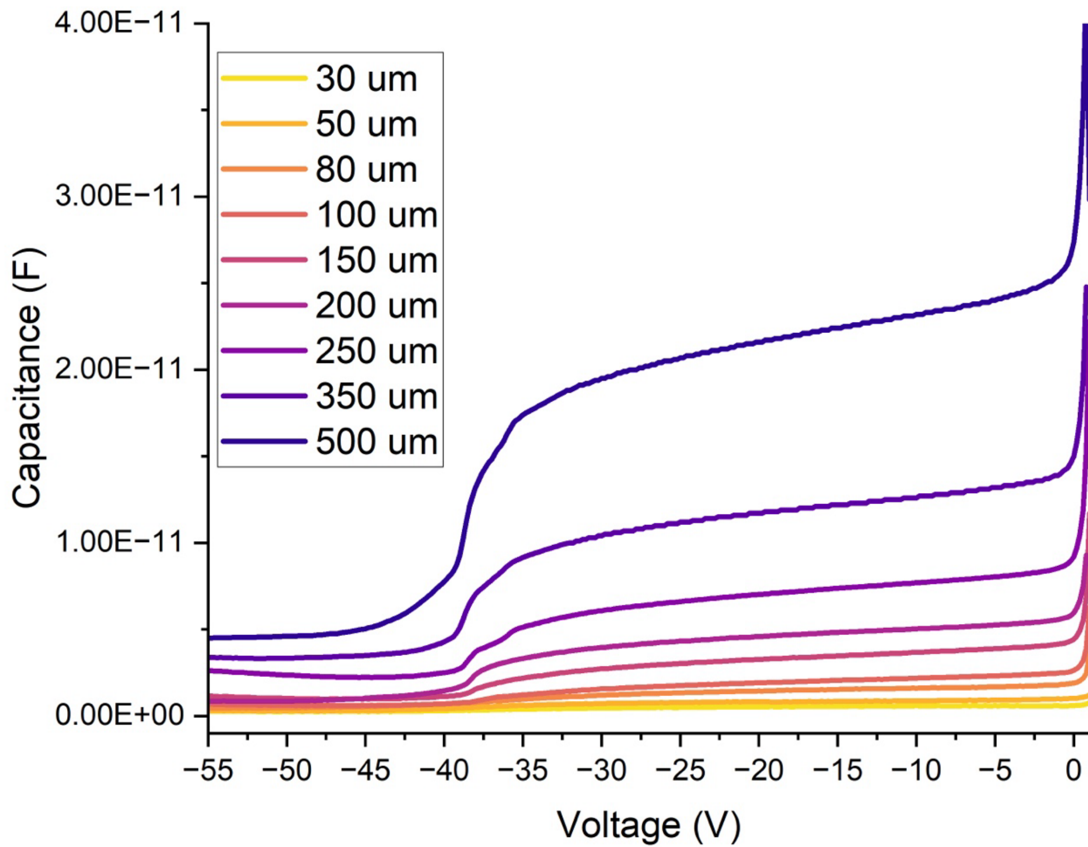

Figure 71. C-V measurements of devices on 30-minute sample at 295 K.

C-V measurements were undertaken on the devices on the 30-minute sample to determine the unity gain, depletion width, and quantify the carrier concentration within the GaAsSb absorber where the Zn-diffusion occurred and are shown in Fig. 71. When normalizing for the differences in device area, the capacitances did not scale with area, indicating that the lateral diffusion to the device's planar area is significantly, particularly for the smaller devices. This is shown in Fig. 72.

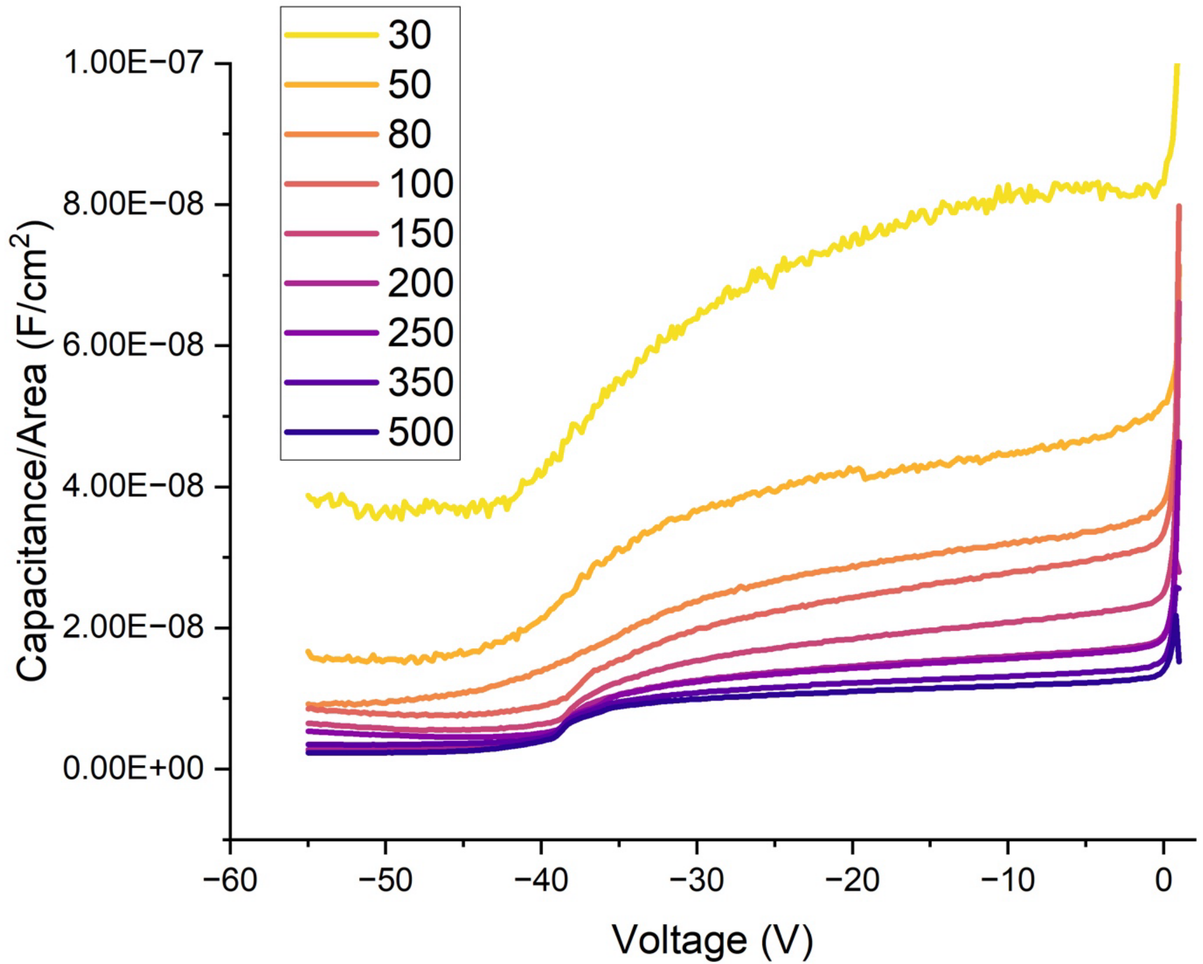

Figure 72. Area normalized C-V measurements of devices on 30-minute sample at 295 K.

From the C-V measurements, it was determined that fully depletion was achieved at approximately – 51 V. For the 200 µm device, the depletion width was calculated to be approximately 3600 nm at this voltage. To estimate the carrier concentration, both UID GaAsSb region and the Zn dopants in the region, a calculation was made using Eq. 21. The maximum doping concentration determined for the structure was approximately 1.0×10^{17}

cm^{-3} but within 250 nm, the doping carrier concentration decreased to 5.9 x 10^{15} cm^{-3} within 500 nm vertically in the device. The difference can be assumed to be the Zn dopants which is estimated at 9.41 x 10^{16} cm^{-3} and is likely occurring mostly in the lateral directions.

To realize the dark current behavior under low temperatures and determine the dominate dark current mechanisms, a low-temperature IVT was performed on a 200 µm device with no guard rings. The temperature sweep ranged from 20 K to 300 K with 20 K step sizes is shown in Fig. 73. It is observed that the dark current remains high with little change from 300 K to 240 K and subsequently lowers only slightly. Within this range, the dark current is too high, such that punch-through is not evident. Only at 100 K, is a slight punch-through observed due to the reduction in dark current. This is realized even further as temperatures continue to reduce until 20 K, there over 2 order magnitude reduction in dark current is noticeable at -64 V operation. From Fig. 73, an Arrhenius plot was produced and is shown in Fig. 74 with several voltages of interest.

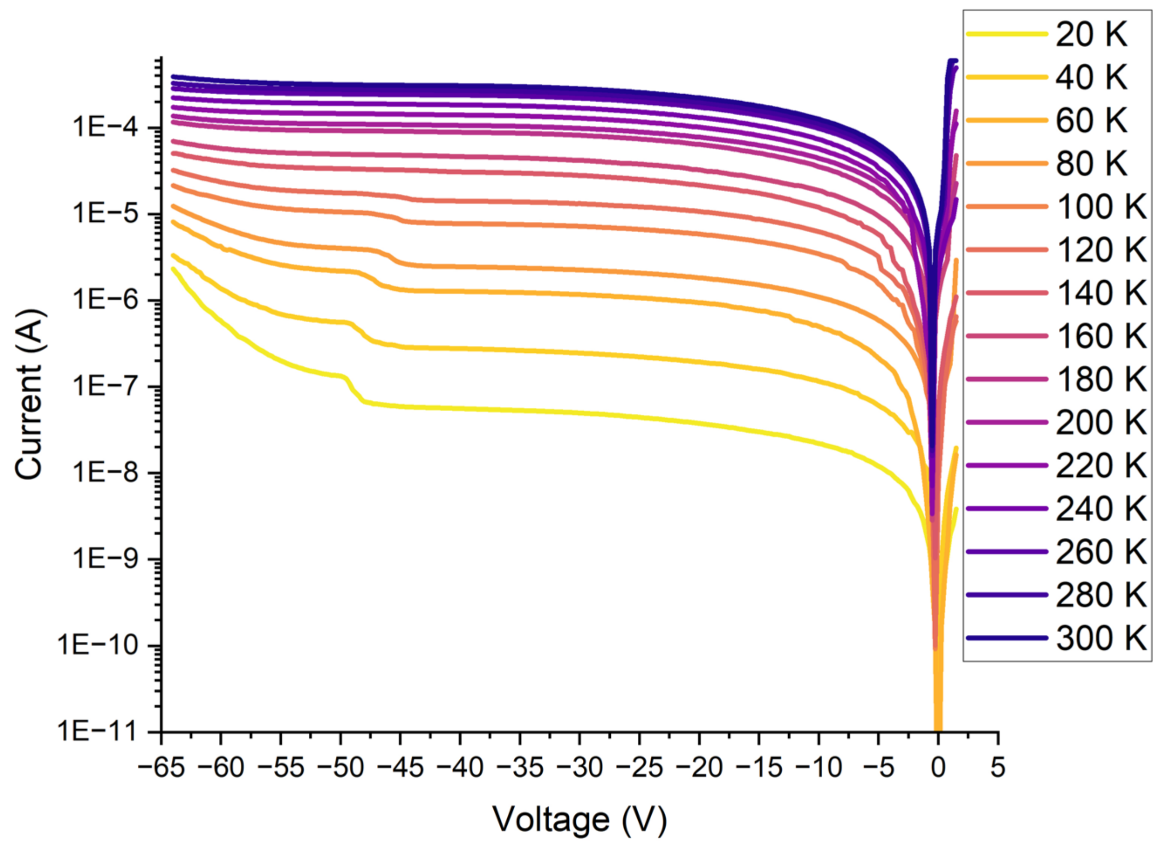

Figure 73. Low temperature IV behavior of 200 μm device.

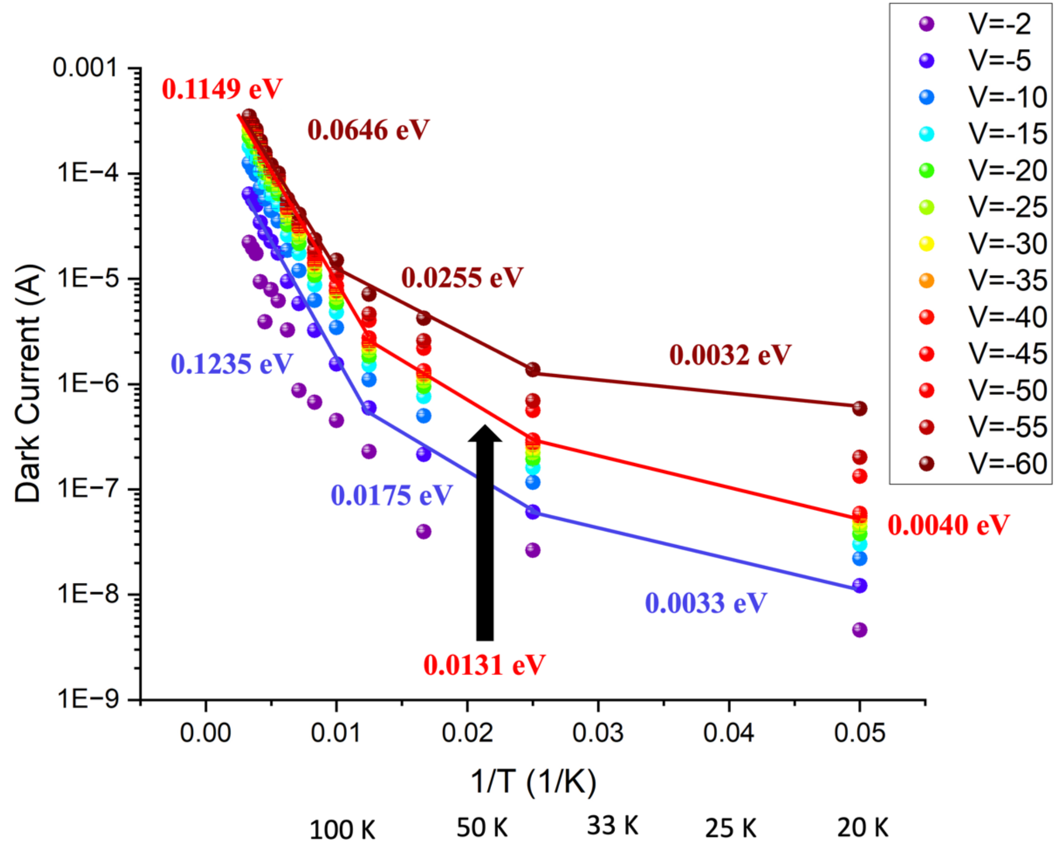

Figure 74. Arrhenius plot for 30-minute diffused sample.

Fig. 74 shows the data points for the dark current at the voltages across the temperature sweep and data points include 5% error bars to account for measurement variations. The activation energy was estimated for -5 V, -40 V and -60 V. These voltages were selected to reflect the device behavior at small reverse biases, prior to punch-through and after punch-through when carriers are impact ionizing. For all three voltages at high temperatures, the activation energies ranged from 0.06046 eV to 0.1235 eV, which is

significantly smaller than the bandgap energy which would indicate that the dark current is diffusion limited and therefore is closer to being half of the bandgap energy, thereby indicating that the dark current is more likely to be generation-recombination and trap-assisted tunneling limited.

6.5 Analyses

In this investigation, the various floating guard ring combinations were also analyzed for their differences in the behavior of the device under test. I-V can be seen in Fig. 75 and a more zoom-in view can be seen in Fig. 76. Since cooled dark current

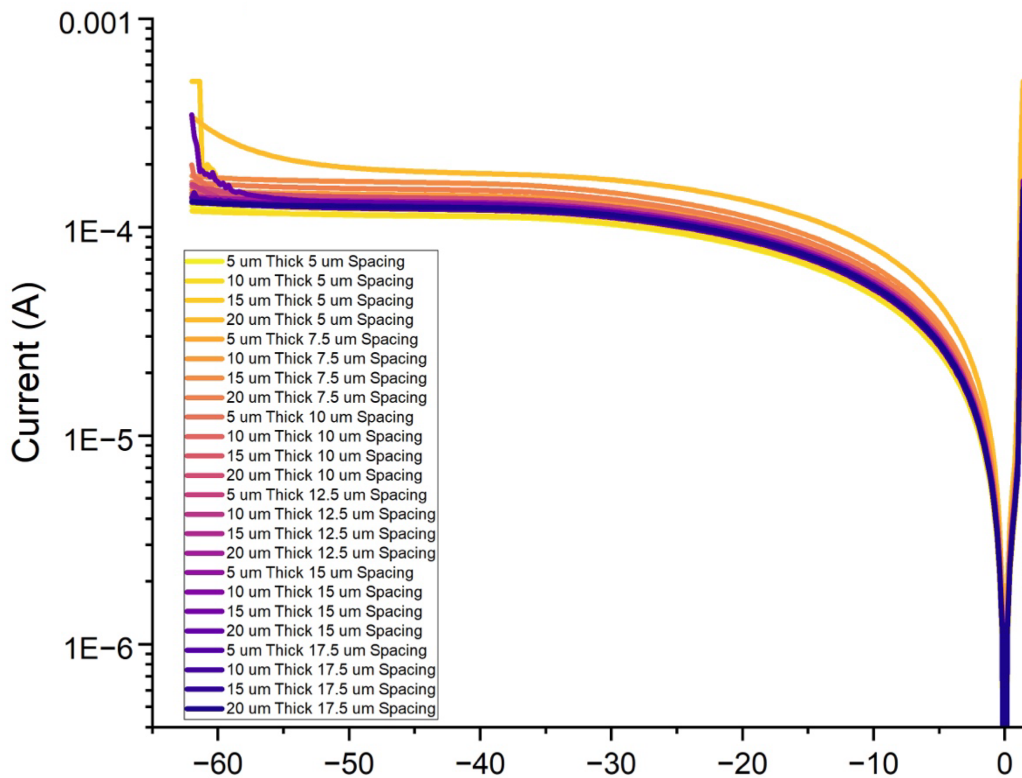

Figure 75. I-V characteristics of 50 μm device behavior with various floating guard ring configurations present at 295 K.

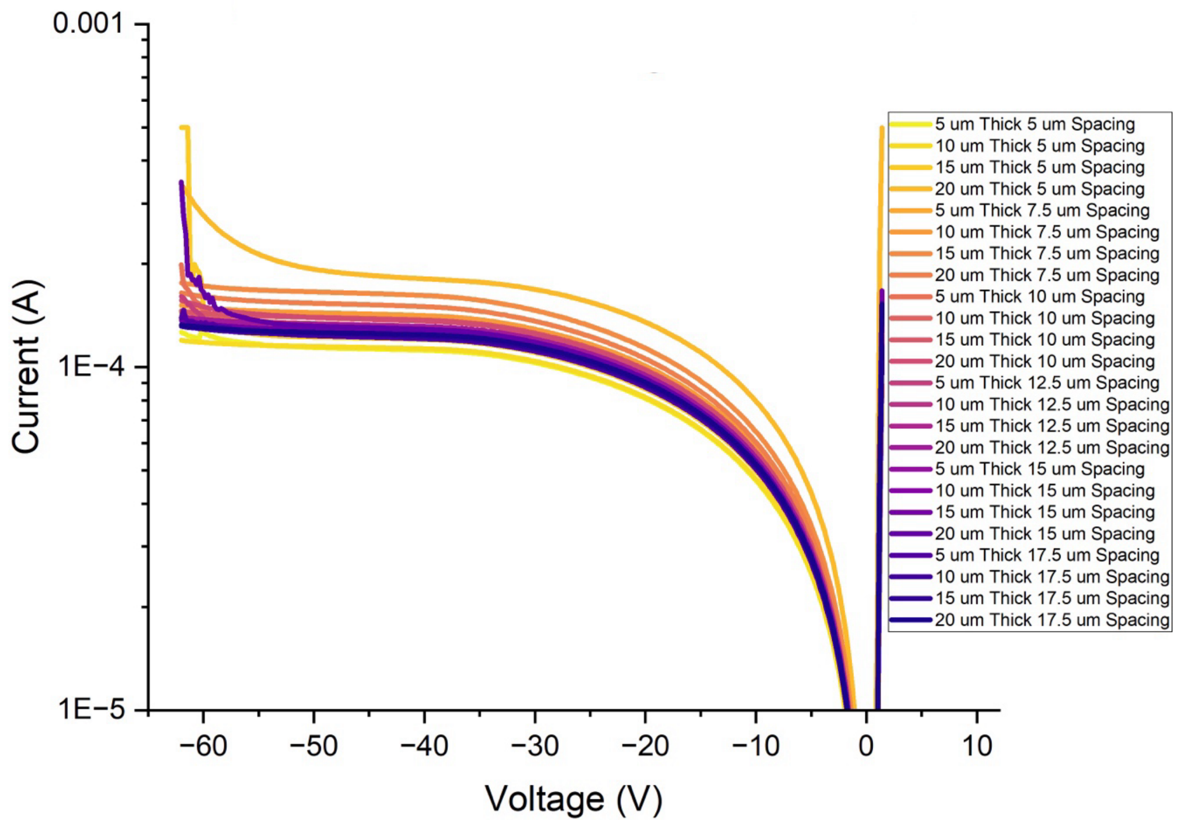

Figure 76. Zoomed in 50 μm device behavior with various floating guard ring configurations present at 295 K.

has proven to be more insightful due to the challenges in planar processing exhibiting nonideal dark current and high operating temperatures, the 50 μm devices employing floating guard rings were assessed at 20 K and are illustrated in Fig. 77. From Fig. 77, it can be noted that a three order magnitude reduction in dark current was realized for the majority of the devices compared to their behavior at 295 K.

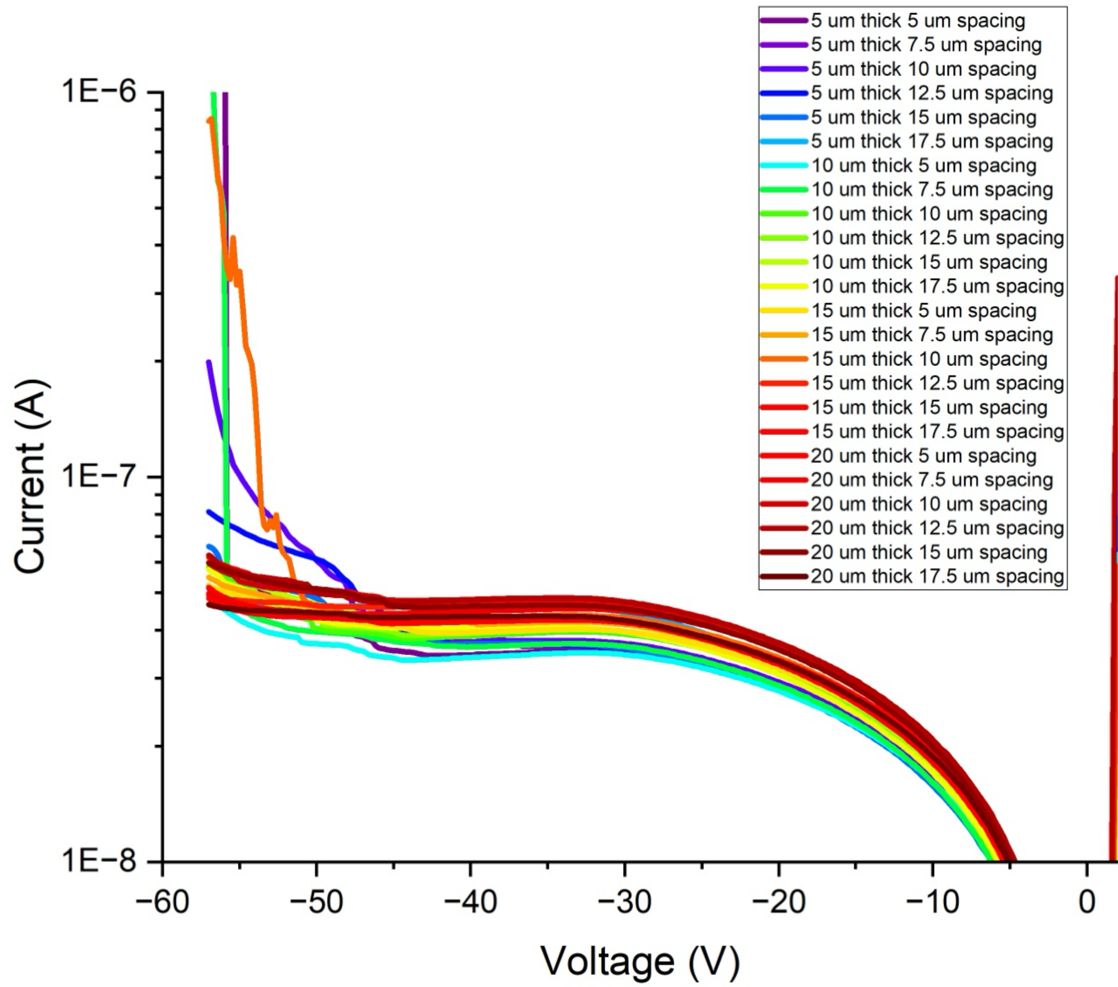

Figure 77. Zoomed in 50 μm device behavior with various floating guard ring configurations present at 20 K.

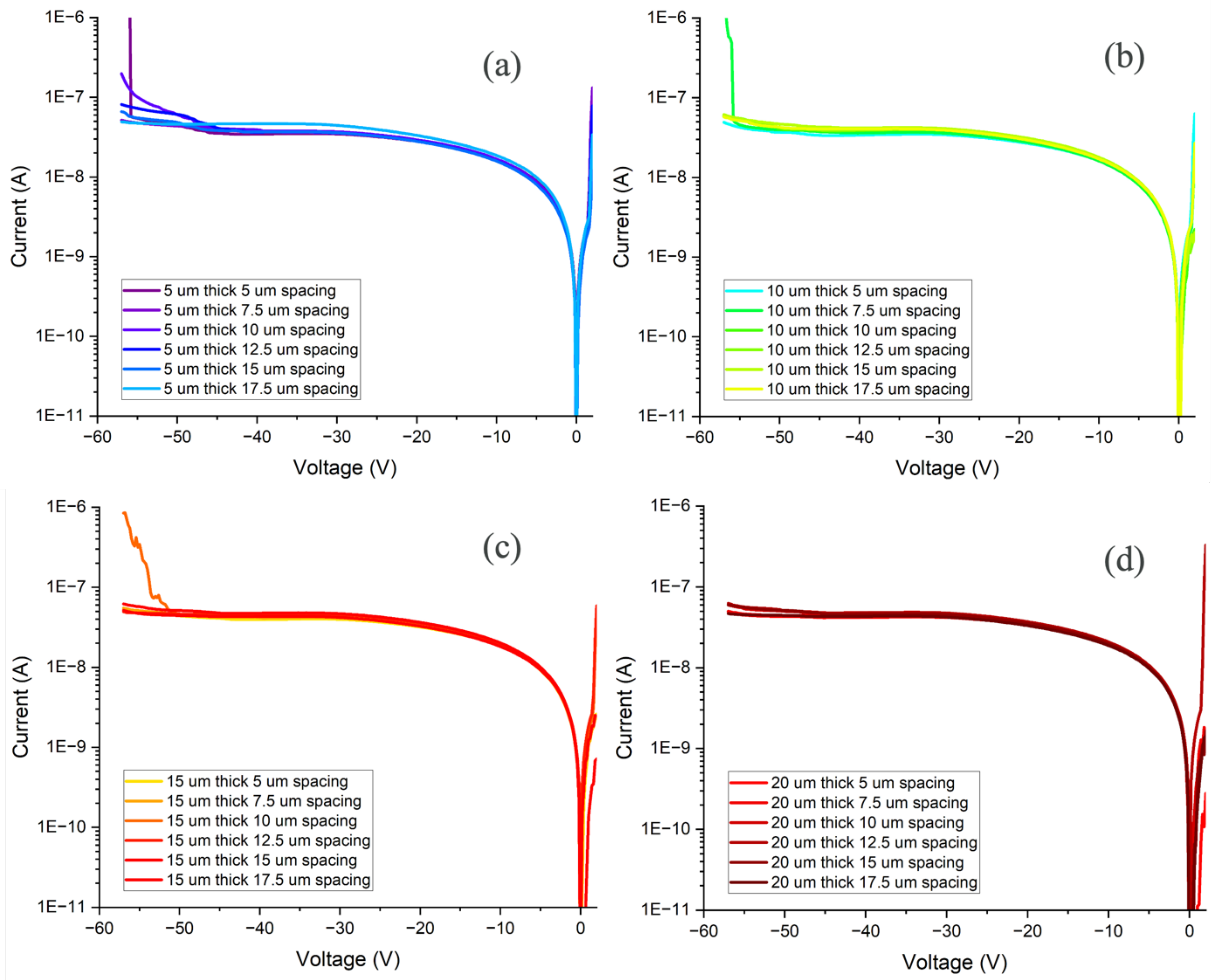

Figure 78. 50 µm with floating guard rings varying metal guard ring thicknesses from device under test at 20 K.

Since both the metal guard ring thickness and spacing away from the device under test were investigated, current-voltage measurements were completed at low temperatures to determine how the variables influenced device behavior. Fig. 78 shows the 50 µm devices when separating their I-V behavior with respect to the metal guard ring thickness at 20 K. Fig. 78a shows the 5 µm, Fig. 78b shows the 10 µm, Fig. 78c shows the 15 µm,

and Fig. 78d shows the 20 μm thick metal guard rings. It can be observed that an increase in guard ring thickness and the respective diffusion under it did not improve the dark current achieved significantly.

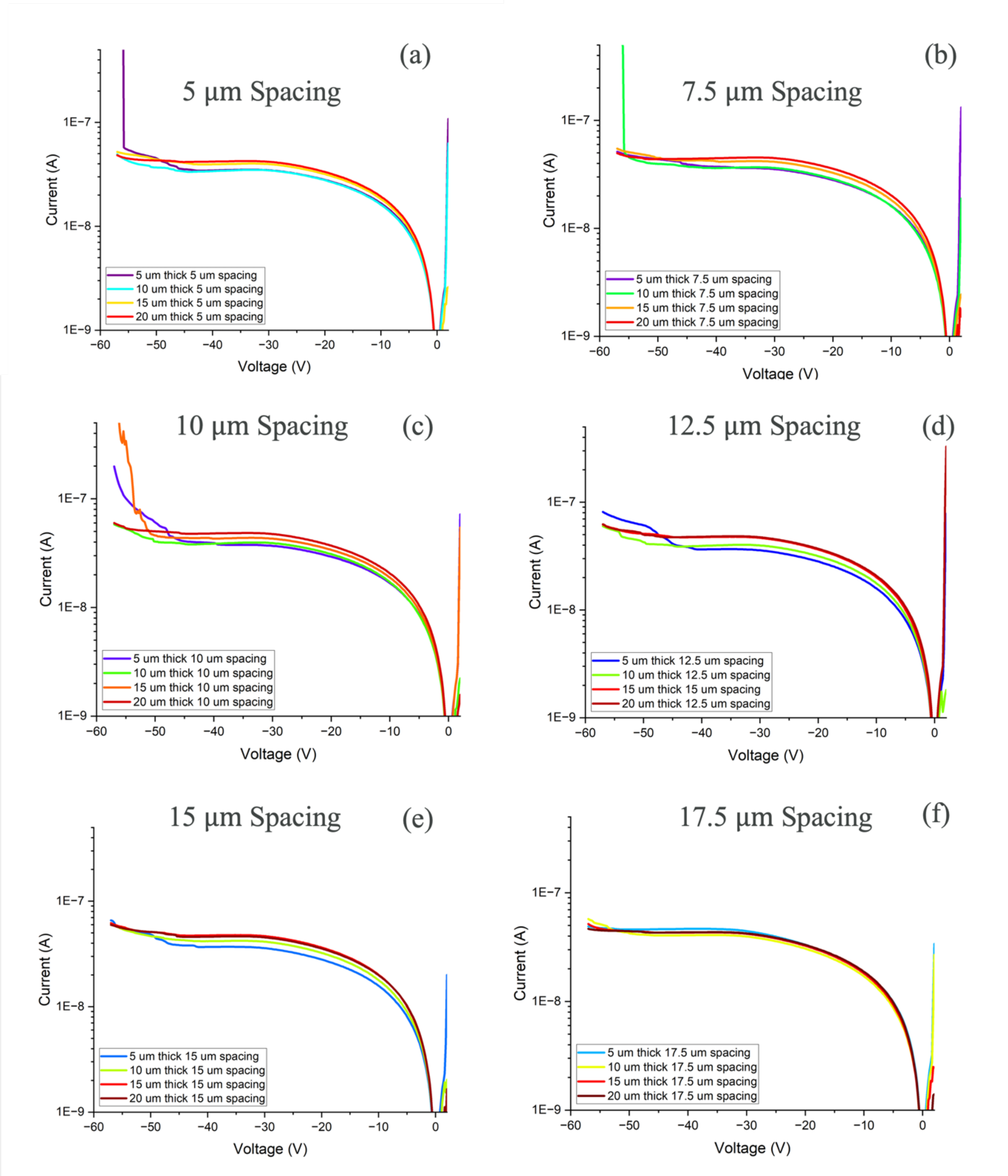

Figure 79. Device I-V behavior with relation to the guard ring spacing from the device under test at 20 K.

To account for the same spacing across the various 50 µm devices, Fig. 79 is depicted, where Fig. 79a shows the 5 µm spacing, Fig. 79b shows the 7.5 µm spacing, Fig. 79c shows the 10 µm spacing, Fig. 79d shows the 12.5 µm spacing, Fig. 79e shows the 15 µm spacing and Fig. 78f shows the 17.5 µm spacing. The greatest difference in device I-V behavior was noted with closer spacing, notably 5 and 7. As the spacing away from the device increases, the variation across the devices reduced, which indicates that the guard ring was less effective. The lowest dark currents observed were with the 5 µm spacing, as being closer to the junction enables improved electric field reductions. It can be noted that although the presence of the floating guard rings did influence the behavior of the device under test, the impact is observed to be minimal. This may result from the diffusion conditions selected, namely the diffusion time, temperature and diffusing atmosphere[146]. An increase in diffusion temperature to 500 C has been reported to promote further improve the Zn depth and diffusion processing in GaAsSb[146]. Furthermore, the atmosphere for which diffusion takes place is likely to encourage further Zn diffusion via breaking the ZnO bonds. Although forming gas was employed for this investigation, H_2 or SiH_4 may be a more attractive gas choice for further investigations, as the hydrogen component is what is critical to break the bonds.

Although the diffusion processing conditions may benefit with further optimization thereby potentially improving the guard ring behavior, it can be noted that the reduction in diffusion time from 90 minutes to 30 minutes was successful in reducing the

dark current devices exhibited, likely due to mitigating the lateral spreading. Fig. 80 below depicts the changes in dark current behavior of 200 μm devices at 20 K across both samples. From this figure, it is noted that a reduction in diffusion time from 90 minutes to 30 minutes did reduce the dark current by approximately an order of magnitude at -55 V and further voltage measurements could be obtained with the 30-minute sample. This is consistent with the diffusion time behavior showcased in Chapter 5 as well and may indicate that a further reduction in diffusion time of the GaAsSb/AlGaAsSb SACM APD may realize lower dark current going forward.

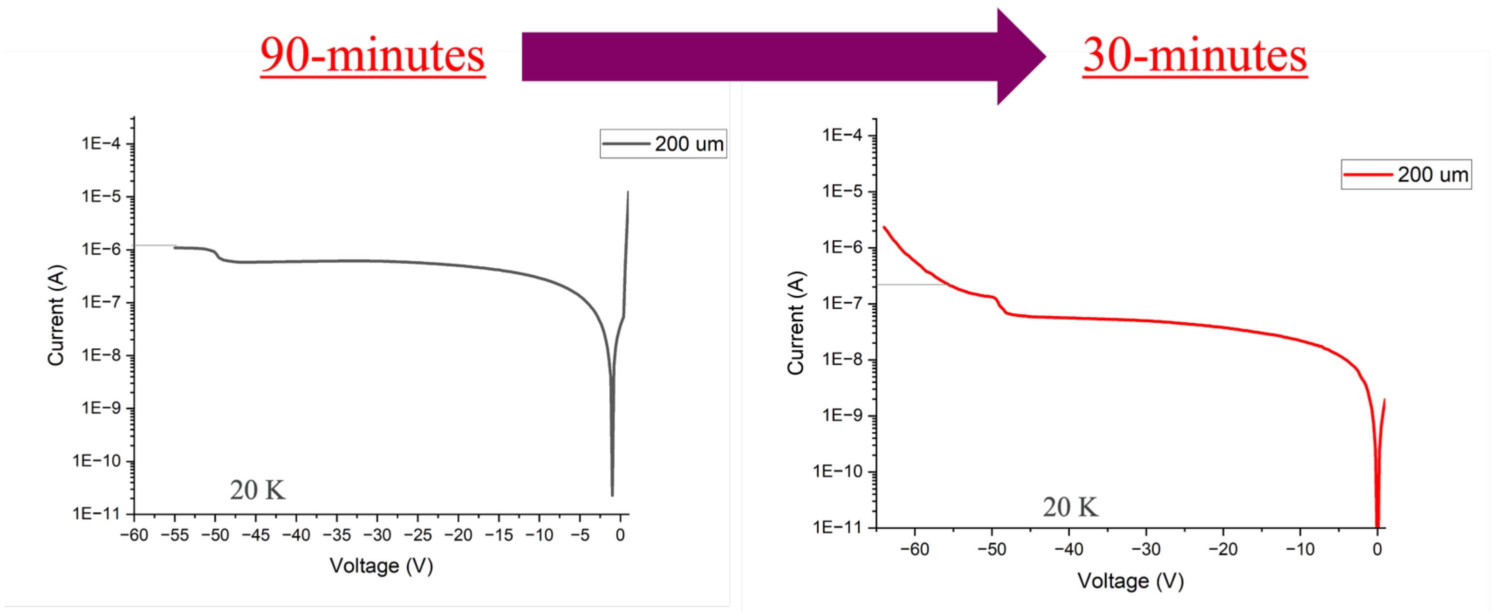

Figure 80. Current-voltage comparison at 20 K for 200 μm devices on 90 minute sample versus the 30 minute sample.

Lastly, it is necessary to understand the resistance components of the structure using TLM structures present on the 30-minute sample. The parameters extracted from TLM measurements can be found in Table 9 below. From the table, it is noted that the contact resistance is higher than ideal and was confirmed with both the 90-minute and 30-minute samples, as evident by the "notch" behavior in the forward bias of both samples. This has been concluded to originate from the Ti/Au metal contacts adhered to the GaAsSb layer. An alternative metal stack may eliminate the "notch" behavior and improve the contact resistance such as Pd/Pt/Au[140].

Table 9. TLM extracted data for the planar GaAsSb/AlGaAsSb sample.

Parameter	**Value**
Contact Resistance, R_c	$1.66990*10^{-4}\ \Omega$
Sheet Resistance, R_s	$2.48342*10^{-6}\ \Omega$
Semiconductor Resistance, R_{semi}	$3.10428*10^{-7}\ \Omega$
Total Resistance, R_T	$3.34290*10^{-4}\ \Omega$
Transfer Length, L_T	$13448.39\ \mu m$
Contact Resistivity, ρ_c	$4.49149*10^{2}\ \Omega * \mu m^2$

6.6 Technical Challenges

Although the investigation of the Zn-diffused planar GaAsSb/AlGaAsSb SACM APD was successful in demonstrating Zn-diffusion and employing guard rings, the study presented several challenges. First, the device behavior was significantly higher in dark current than anticipated and when compared to the AlGaAsSb Zn-diffused mesa. This is likely a combination of several components. First, the GaAsSb/AlGaAsSb SACM APD required initial wet etching to remove the p-type contact layers and examine the device performance under Zn-diffused planar circumstances. Through the wet etching process, it is likely that defects were produced which would inhibit device performance. Secondly, the high dark current the devices showed are likely also present due to the diffusion conditions selected. Although a similar approach to the AlGaAsSb Zn-diffusion was used, it is likely that GaAsSb diffusion is more complex and enables further lateral diffusion. This could be investigated further with additional adjustments in the diffusion time and the atmosphere for which diffusion occurs. Thirdly, both planar GaAsSb/AlGaAsSb samples demonstrated high contact resistance behavior, as indicated by the sloping of the forward bias current-voltage. This was deduced to be the result of the Ti/Au metal stack implemented. After the conclusion of this study, further reading arose reports that other metal stacks such a Pd/Pt/Au should be adopted for contacts made directly to GaAsSb[140]. This was unknown previously, as previous SACM and p-i-n structures investigated employ InGaAs contact layers.

When comparing the planar GaAsSb/AlGaAsSb device performance to APD structures outline in Table 1, it is evident that the planar GaAsSb/AlGaAsSb do not meet or exceed the performance parameters both of commercially available InGaAs APDs as well as more complete reported SACM APDs that implement mesa architectures. This is likely due to the challenges arising from the novel planar processing that require further optimization. Despite the ease of planar processing when using ALD and the diffusion furnace tube, Zn-diffused planar GaAsSb/AlGaAsSb SACM APDs may also be realized by other methods such as MOCVD or ion implantation, which may translate to uniform sufficient Zn depths achieved in the structure especially in the case of ion implantation by which the dose and implantation energy can be controlled to reduce lateral spread[147,148].

Chapter 7. Conclusion

7.1 Assessment of Background Doping Polarity of AlGaAsSb and AlInAsSb

In Chapter 3, the background doping polarity of random alloy AlGaAsSb and random alloy AlInAsSb were successfully determined using a double mesa device architecture and C-V measurements. This is useful for further designing of more complex SACM APDs that utilize these Sb-based material systems for multiplier materials to achieve high performance for SWIR applications.

7.2 Assessment of InGaAs/AlInAsSb SACM APD on InP Substrate

In Chapter 4, the first InGaAs/AlInAsSb SACM APD on InP substrates was demonstrated and indicated high temperature stability, over other materials of interest. This investigation was successful and will be further built upon to achieve higher gains for the SACM structure.

7.3 Assessment of Zn-Diffused AlGaAsSb on InP Substrate

In Chapter 5, the first reported Zn-diffused AlGaAsSb p-i-n mesa device was demonstrated using ALD and diffusion furnace tubes to promote the Zn diffusion. This

was determined to be a successful investigation, as the devices exhibited low dark current, notably with reducing the diffusion furnace time.

7.4 Assessment of Zn-Diffused Planar GaAsSb/AlGaAsSb SACM APD on InP Substrate

In Chapter 6, the first reported Zn-diffused GaAsSb/AlGaAsSb SACM APD has been investigated and demonstrated. This is the first of its kind to be done with Zn-diffusion directly into the absorber and utilizing floating guard rings to determine improved device performance, which lowest dark current at 295 K occurring with guard ring spacing of 5 µm.

Chapter 8. Future Work

This work has laid the ground for further work to build upon, especially in the realm of AlGaAsSb and GaAsSb/AlGaAsSb SACM planar devices. First, the AlGaAsSb has been explored with Zn-diffused mesas and was deemed successful in the demonstration of rectifying characteristics, low dark current and a selected diffusion furnace time. Future work regarding the Zn-diffused AlGaAsSb should explore the atmosphere conditions of the diffusion furnace tube to determine the optimal conditions to promote sufficient Zn depths, as the concentrations are estimated to be low within this investigation. In addition to the diffusion atmosphere study, it is beneficial to investigate a fully planar AlGaAsSb structure, which would require a n-type InP substrate for the growth. Additionally, a planar study of the AlGaAsSb could also incorporate an investigation of guard rings which was not explored in this work.

For the GaAsSb/AlGaAsSb planar SACM structure, device characteristics were investigated under two diffusion times. Similar to the AlGaAsSb future work, further work should investigate the diffusion atmosphere, as well as a lower diffusion time to reduce the lateral diffusion present. Other studies have also implemented a double diffusion process, whereby a secondary Zn-diffusion is added to the fabrication and may result in lowered electric fields which would encourage higher performance of the SACM devices. Regardless of the investigation, future work should adopt the Pd/Pt/Au metal stack to also remove undesirable contact resistance.

Chapter 9. Lessons Learned

No PhD experience is complete without the occasional (or frequent!) challenge. Throughout my PhD, I faced several challenges that I would like to highlight for the next graduate student who may face similar difficulties.

9.1 Technical Lessons

APD Heterostructure Design and Modeling

Preliminary APD design and modeling is arguably the most critical component of a project because if a design is not well thought out and developed intentionally to meet or exceed the required performance specifications, it will not succeed. With this in mind, it is pertinent that sufficient time is spent developing accurate and meaningful modeling tools to obtain as accurate results as possible, especially when designing more complex structures like the SACM.

From a material perspective, it is necessary to understand the materials you are implementing into the model, through sufficient literature and the knowledge of semiconductor physics. Many parameters for materials can be found in literature, such as the impact ionization coefficients of materials, and by utilizing these values in your model, you will get more meaningful results. In relation to this, fully understanding the models in your simulation is crucial.

Iterating the design model is key. To optimize an SACM design, it is necessary to make minute adjustments in the material compositions, thicknesses of each layer, and doping concentration to ensure proper performance. From these, electric fields and band diagrams can be obtained. Even further, I-V and C-V behavior can be simulated. In these simulations, the behavior will likely differ from actual device behavior unless consideration is taken into the different mechanisms that kick in at high biases, such as avalanche tunneling.

Design and modeling can be incredibly complex and time consuming, but it is worthwhile to spend the time to do it.

Device Fabrication

Deposition

- It is useful to include reference samples when performing deposition processes in the fabrication. In particular, Si reference chips were implemented during both the SiN_x deposition via Chemical Vapor Deposition (CVD) and the ZnO deposition via Atomic Layer Deposition (ALD) alongside the actual sample being processed. Before and after both depositions, the Si reference chip is measured via an ellipsometer to verify the deposited material thickness, which is assumed to be the same for the actual sample being processed.
- Contact resistance can be problematic for device performance and is introduced to a structure during the metal deposition process to produce

contacts for subsequent device characterization. While a metal stack of Ti (12) /Au (150nm) has worked well for InGaAs contact layers on the APDs, it is not a suitable choice for GaAsSb contacts, as evident during the planar diffusion investigation. This was further affirmed via literature whereby Ti-containing metal stacks on GaAsSb demonstrate higher specific contact resistivity[140]. A metal stack such as Pd/Pt/Au is more suitable choice for GaAsSb based contact layers will lower the contact resistance of the devices.

Device Characterization

Device characterization is imperative to quantify key performance metrics and inform subsequent growths and fabrications of new material. With this in mind, it is vital that care is taken when performing device characterization and that it remains consistent. A standard approach has been developed to test devices and provide meaningful results quickly. First, devices are measured at 295 K to provide quick feedback on the dark current behavior and breakdown voltage across a span of devices. If the dark current values are at or below the acceptable threshold, devices will be measured for their photocurrent at the intended wavelength of operation to calculate the expected gain. If current-voltage measurements demonstrate that the devices are performing well, capacitance-voltage measurements are taken to do several things such as determine the unity gain at

which the junction is depleted, determine the depletion width, and the background carrier concentration at 295 K.

Once preliminary data is collected, it is decided if the material is performing well enough to require additional testing. If the device exhibit poor behavior, the only additional measurements that may be useful may include a VADA, whereby the bulk and surface dark current is quantified to inform the next growth or fabrication. This enables the growth or fabrication to be adjusted to improve device performance. Also, within this stage, transfer length measurements (TLM) can be performed to provide values for series and contact resistance.

If room temperature behavior is good for the devices, cryogenically cooled measurements are next considered. When completing cryogenic measurements, additional steps are required. First, it is necessary to cool completely to the lowest temperature of interest first. This is useful as it allow the setup to remain stable first before taking measurements and provides an easier method of simply heating the system up incrementally to cover the temperature range of interest.

When performing IVT, caution should be taken when handling the probes that will contact devices repeatedly at each temperature within the range. Using too much pressure to land the probes on the devices repeatedly introduces additional damage to the device and will likely cause the device to breakdown permanently before all temperatures are measured. While it is possible to keep the probes in contact with the device over the entire temperature sweep, only one device can be measured then and is not typically enough to collect meaningful data. Bearing this in mind that

some variation is present device to device, and it is useful to collect a lot of data to see trends overall.

While performing cooled measurements, additional vibrations are introduced to the setup that may lead to noisier measurements. The vibrations cause the probes to move incrementally across the device while in contact which may damage both the probe and the device and result in early permanent breakdown. There are several ways in which this can be mitigated both for the safety of the probe and the device, in addition to improving the data acquired.

- A helium compressor is implemented with the setup to assist in reaching the desired temperature and maintaining. While it is necessary to cool the system, it introduces the vibrations into the setup. To mitigate this, the helium compressor may be turned off while taking measurements but should be subsequently turned back on afterwards to maintain the temperature.
- It is highly encouraged to keep the probes off the devices if not actively measuring or during the cooling process to protect the probe and the device from damage.
- If possible, considerations should be made for the type of probe used for low temperature measurements. Lakeshore Cryotronics produces specific continuously variable temperature (CVT) probe tips that are designed to absorb probe arm movement that result from thermal expansion and contraction. These may be useful to remove excess vibrations in the setup

while cooled and could be implemented in future automated characterization setups to streamline data acquisition and improve measurement quality. The downsides attributed with the CVT flexible probe tips is that they have anecdotally had shorter lifetimes of use due to being more fragile. Furthermore, they are more expensive than the standard probes used. One solution to this may be to replace the CVT tips after personal use and put the standard probe tips back on for other users who use the cryogenic probe station. Some caution should be taken when replacing the probe tips, as they can get damaging during the installation process.

The type of probe tip and its material may matter for your measurements. I have found that while Tungsten probe tips are standard for general use and are durable, they are not suitable for all samples and may have higher inherent contact resistance than other available probe tips. BeCu probe tips had lower contact resistance and improved conductivity over the Tungsten probe tips but are softer and more prone to bending easily. It is worthwhile to consider the probe tips installed when trying to troubleshoot and identify poor measurements and the cause, although the material and fabrication should first be ruled out as the culprit first.

A significant challenge that was faced with performing device characterization at low temperatures was the time and attention required to collect data. The current setup is manual, meaning all probing of devices is done by hand, at each temperature across the range. It requires a student or user to be present for 8-12 hours, begin the cooling process, measure devices manually, heat the system up

incrementally for the next temperature and wait for the system to stabilize, and then continuing measuring more devices. The process is extremely time consuming and takes away from completing other tasks. One way to improve the IVT data acquisition and increase efficiency is to automate the cryogenic probe station setup. An automated setup of the tool could include developing a LabView program that communicated with the temperature controller, takes measurements at each temperature of interest using Source Meter Units (SMUs) and then increase the temperature to repeat the process. This setup would also implement the CVT probes discussed previously and would allow for one device to be measured across the entire temperature range for its dark current behavior. If desired, the multi-channel laser could also be programs to modulate as well and power on to get photocurrent measurements at each temperature as well for the extraction of multiplication gain. Considerations are being undertaken to propose this as an undergraduate student capstone project.

9.2 Non-technical Lessons

Documentation

Documenting during every aspect of the research life cycle is vital and can't be stressed enough. Developing a consistent documentation practice is both useful at the present moment of fabrication processing or device characterization and in the future when referring back on the work accomplished and performing analyses. Developing a fabrication processes/traveler is helpful to note any observations

during the processing or deviations from the standard recipe implemented. A similar approach can be taken with the device characterization. Both enable easier paths towards identifying the reasons behind why an APD exhibits poor performance and what step in the research process is responsible and must be adjusted.

Along the same token of documentation, it is helpful to develop a standard approach for troubleshooting if poor results are obtained. This helps easily identify if an issue arises from the device or if the equipment is failing or malfunctioning.

The Value in Mentorship

I have been blessed with the opportunity to have several people serve as a mentor during both my undergraduate and graduate careers and the role these individuals have played into my success can't be emphasized enough. There is immense value in having a mentor to support and provide guidance for you. I am grateful that the KIND group and Dr. Krishna instill the importance of having senior graduate students who mentor the junior graduate students. This has been incredibly useful for me early on my PhD, as my mentors helped me learn the ropes of the research but also as my PhD has drawn to a close and I have served as a mentor to others. I value the role mentors serve for others and hope to be a mentor throughout my career.

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Appendix 1: ZnO Diffusion Planar APD Processing Recipe

Pictures: Take pictures before and after fab (Use Optical Profilometer for pictures post fab)

1. **Sample Preparation (Cleaning)**
    a. Clean samples in IPA, Acetone and DI water for 1 minute each
    b. Air dry sample with air gun
        i. If samples are not sufficiently dry, heat the samples on hot plate at 150 C for 1 min.
    c. Heat the samples at 150 for 1 min.
2. **Etching off P layers (If applicable)**
    a. Determine p layer from structure and what depth is necessary to reach UID layer.
    b. Use wet-etch chemistry below.
        i. In this order). Use a magnet to stir solution at 80-100 rpm on hotplate Have Leave the solution for about 30min. Place the sample in the solution, while magnet is being stirred at 100rpm. Check the etched depth and do the etching in steps (Use the dummy samples before real sample etch to verify etch rate)
        ii. **Wet Etch Chemistry:**
            1. Citric (1:1) 40mL (in hallway)
            2. H_2O 200mL
            3. H_3PO_4 10 mL (in hallway)
            4. H_2O_2 10mL
            5. Mix for 30 min, rpm: 100 rpm

a. Always test the etch rate; **It should be about 100nm/min**

c. Rinse the sample in DI Water two times in a row. Check etch depth using Dektak

3. **Depositing SiNx via PECVD**

    a. Deposit 150 nm (1500 Å) of SiNx via CVD

4. **Photolithography**

    a. Clean samples in IPA, Acetone and DI water for 1 minute each

    b. Air dry sample with air gun

        i. If samples are not sufficiently dry, heat the samples on hot plate at 150 C for 1 min.

    c. Set up spin coater COT04 for S-1813

        i. Spin coat S1813 (1.5 um): 4000 RPM, 60”, at 500 RPM/sec.

        ii. Bake at 115 C for 1 min

        iii. Let the sample to cool for 2 min

    d. **Maskless Aligner (MLA)**

        i. Prepare MLA with gds file. **Select first layer only for exposure**

            1. Settings for Planar:

                b. Exposure quality: high

                c. Invert: off

                d. Dose: 145 mJ

                e. Defoc: 0

                f. GDS structure: TOP**

        ii. Expose using MLA (for S1813: MLA at 145 mJ /cm^2, 405 nm)

iv. Develop in MF-319 for 1.5min and in DI water for 1min.

1. Dry samples with air gun

v. Check feature quality

1. Can be done under microscope

5. **SiN_x Thickness Verification and Plasma Etching**

a. Verify SiN_x thickness using the Ellipsometer (Do this on reference Si sample)

b. Do a plasma etch on the sample to remove SiN_x

ii. Use large Si carrier or quartz carrier for this process.

1. Samples are adhered to the quartz carrier via a dab of diffusion oil.

2. Adjust loops/iterations first to check the etch depth of the SiN_x etching first

a. Do an etch with 1 loop, remove sample, and verify new SiN_x thickness using Ellipsometer again.

iv. After completing SiN_x etch, run an argon clean flow after in ETC04

v. After SiN_x plasma etch

1. Remove diffusion oil from quartz carrier via IPA

c. Removal of photoresist

i. Place all samples in IPA first and then acetone.

ii. Dry samples afterwards with air gun

iii. Verify that the photoresist has been removed by viewing sample under the microscope. If not all the photoresist has been removed, place sample back in IPA and repeat the process.

iv. Optional: you can remove any photoresist residues with O_2 Ashing for 5 min

6. **ZnO Deposition (ALD)**

   a. ALD Specifications

      i. Depositing 150 cycles (~30 nm) of ZnO via ALD (Using DeZn)

         1. Set substrate temperature to 150 C
         2. Change number of desired cycles to 150

      iii. TE2 = substrate temperature = 150 C

      iv. TE1 = max allowed value for heater = 250 C

      v. While ALD gets ready, prepare the HCl:DI dip

         1. Dip the sample in HCl:DI (1:10) for 20 sec. Have additional DI water only glassware ready, in a beaker for a dip after.
         2. Air dry samples afterwards with air gun

      vi. Place both bare Si chip and sample into ALD for deposition to verify ZnO thickness

         1. Verify ZnO deposition thickness with ELP03 on Si chip after

7. **Diffusion Furnace Tube # 2**

   a. Turn on 20 sccm of forming gas

b. Verify desired temperature with thermocouple.

c. Set temperature: 400 C

i. Due to variation in temperature in the furnace tube, the actual diffusion temperature is closer to 423-425 C

d. Set time: 10-30 minutes

8. **Photolithography**

a. Clean samples in IPA, Acetone for 1 minute each

b. Air dry sample with air gun

i. If samples are not sufficiently dry, heat the samples on hot plate at 150 C for 1 min.

c. Spin coat LOR5A – 4000 RPM, 10,000 RPM/Sec, 60sec.

d. Let the sample sit for 1' before the bake

e. Bake sample at 180C for 5min

f. Let the sample to cool down for 2 min

g. Spin coat SP1813– 300 rpm/ 100rpm/sec/8sec at 3000rpm/5000rpm/sec/30sec

h. Bake it – 115C for 1 min

i. Let the sample dry for 2 min

j. Expose using MLA; 405nm, (Defoc may differ)

1. Settings for Planar:
2. Make sure that for the second exposure
3. Do manual alignment to alignment markers

a. Invert: off

b. Dose: 145

c. Defoc: -2

ii. Expose using MLA (for SP1813: MLA at145 mJ /cm^2, 405 nm)

k. Develop – MF319 for 1min 15 sec and in DI water for 1 min

i. Develop in MF-319 for 1.5min and in DI water for 1min.

ii. Check feature quality

1. Can be done under microscope

l. Clean IPA and Acetone glassware while MLA exposes

Metal Depositions

1st Metal Deposition

m. Optional: O_2 plasma ash for 5-10 min to remove excess resist

n. Dip the sample in HCl:H20 (1:10) for 20 sec.

p. Deposit Ti/Au (12/150nm) (120 Å/1500 Å) **(Note: can also deposit Ti/Pt/Au 30/30/500nm if wire bonding)**

i. Ti deposition speed: 0.5-1 Å /sec

ii. Au deposition speed: 0.5-1 Å /sec

q. **NMP Liftoff:**

i) Preheat the NMP on hotplate at 105C for 30 min

ii) Place the sample in NMP for 30min (Hot plate at 105C)

iii) Check if the liftoff happened smoothly. If not, place the sample in NMP at room temperature between 2 hours to overnight.

r. Use IPA to clean sample. No DI (Prefer no ultrasonic) Wash in IPA only and air dry with air gun

s. Take microscope images of fab

2nd Metal Deposition

t. Set up spin coater COT04 for S1813 to front of sample

i. Spin coat S1813 (1.5 um): 4000 RPM, 60”, at 500 RPM/sec.

ii. Bake at 115 C for 1 min

iii. Let the sample to cool for 2 min

u. Deposit Ti/Au (12/150nm) (120 Å/1500 Å)

i. Ti deposition speed: 0.5-1 Å /sec

ii. Au deposition speed: 0.5-1 Å /sec

v. Clean S1813 off sample front after metal deposition using acetone. Dry sample afterwards