Radiation Tolerant Gallium Nitride Electronics

Thesis

Presented in Partial Fulfillment of the Requirements for the Degree Master of Science in the Graduate School of The Ohio State University

By

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Abstract

Gallium Nitride (GaN) devices are gaining widespread adoption in high performance power and RF applications. Recently, GaN has gained a lot of attention for its high tolerance to extreme environments. Due to its high displacement energy and bond strength, GaN has high intrinsic radiation tolerance. This work presents a radiation tolerant GaN monolithic technology to integrate digital circuits using AlGaN/GaN depletion mode and Gate Injection Transistor (GIT) based enhancement mode HEMTs. Using depletion load logic, logic inverters and universal gates were implemented and fabricated.

The type of radiation damage on GaN is dependent on the type of radiation and dose. This digital logic technology proved feasible in low dose gamma radiation environments with no significant degradation in electrical performance. AlGaN/GaN HEMTs have shown high degradation after suffering displacement damage. This work proposes highly scaled FinFET structures to architect these devices to be less susceptible to radiation induced buffer damage. TCAD simulations of fin structures showed little shift in 2DEG concentration compared to similar planar structures. An E-Beam lithography process was also developed to fabricate AlGaN/GaN FinFETs.

Dedication

Dedicated to my family

Acknowledgments

My time in graduate school was very fulfilling and enlightening which was all made possible by Prof. Siddharth Rajan. I am deeply grateful to him for being my advisor. I would also like to extend my gratitude to Prof. Wu Lu for serving in my thesis committee.

I also consider myself to be very fortunate to have worked in a group with excellent members with whom I have had many insightful discussions. I am very thankful to Wahidur Rahman, who mentored me in cleanroom device fabrication and device characterization. I have enjoyed working with Chandan, Ashok, Tae Young, Nidhin, Sushovan, Ifat, Agnes, Hyunsoo, Andreas, Towhid, Shahadat, Yinxuan and other group members. I would also like to thank all the Nanotech West staff members for their support.

I finally would like to thank my family for all their support and motivation in every step of my life.

Vita

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Chapter 1

Introduction

1.1 Radiation Damage in Semiconductor Materials

Semiconductor devices, when subject to nuclear radiation undergo damage affecting its electrical performance. These radiation exposure events, often classified into three categories, have significant impact on complex systems in nuclear power plants, avionics, and satellites. A shift in the threshold voltage of a transistor caused by a radiation event of a in a digital system could result in incorrect logic levels leading the system to catastrophically fail. It is imperative to develop technologies that are radiation hard that enable electronics that work in these environments. Radiation exposure on semiconductors is classified into Single Event Effects (SEEs), Displacement Damage and Total Ionization Dose damage.

SEEs are caused by a single energetic particle passing through the semiconductor can be either destructive or nondestructive. They are mainly caused by cosmic rays and high energy protons [1], [2]. These effects create an ion track inside the semiconductor material extending depletion regions, causing bitflips or be potentially destructive and result in hot carrier effects.

Displacement Damage, a result of nuclear interactions such as scattering causes lattice defects, is a type of permanent damage [2], [3]. Missing atoms, complexes and interstitials manifest themselves as trap states and could act as recombination centers affecting minority carrier lifetimes. These trap states also affect the electric fields in the device impacting its electrical performance. Displacement damage is caused by energetic particles such as protons and neutrons.

Total Ionizing Dose damage is due to cumulative accumulation of ionizing radiation. This is typically caused by accumulation of high energy X-rays, γ-rays or charged particles. TID damage often results in annealing effects, release and transport of protons, shifting trap levels and occupancies impacting device characteristics.

1.2 Gallium Nitride for Radiation Tolerant Applications

Wide Bandgap Semiconductor (WBG) are an emerging class of semiconductor materials with wide applications in power and RF electronics. With high critical breakdown fields, WBG class of materials enable high voltage and high efficiency power electronics with significant reduction in die area. Recently, WBG materials have gained a lot of attention for its operational capabilities in extreme temperature and radiation environments [4], [5].

Gallium Nitride (GaN), in its Wurtzite form (E_g=3.4 eV) is often used in making high performance High Electron Mobility Transistors (HEMTs) with wide applications in RF

and Power. With bulk GaN being very expensive, it is often epitaxially grown on SiC, Sapphire or Si substrate often graded down from a buffer layer.

Wurtzite AlGaN/GaN systems exhibit spontaneous and piezoelectric polarization phenomena along the c-plane (0001) [6], [7]. This polarization enables device designs with 2-D Electron Gas (2DEG) channel charges as high as $3x10^{13}$ cm^{-2} without the introduction of any dopants. The absence of dopants results in no impurity related scattering enabling channels with high electron mobility.

GaN has attracted a lot of attention for high performance radiation tolerant applications [3] in space and front-end electronics for nuclear power generation. The high bonding in binary and ternary nitrides gives this class of materials resistance to radiation intrinsically. This is attributed to strong bonding of GaN with high displacement energies (E_d). The high displacement energy attributes to high radiation tolerance as it is a measure of how strongly bonded the atoms are and how difficult it is to create crystal defects with an observed inverse variation relationship with lattice constant [8]. There have also been reports indicating how displacement damage induced defects have acted as scattering centers that reinject scattered carriers back into the 2DEG channel owing to minimal changes in device performance in certain AlGaN/GaN systems [9].

1.3 Thesis Objectives and organization

This objective of this thesis is to develop a radiation tolerant monolithic technology to integrate digital circuits. The thesis investigates the performance under the accumulated gamma exposure and propose radiation hard device design structures resistant to defects induced due to displacement damage.

Chapter 2 introduces the normally on and normally off transistor structures used. It also details the cleanroom fabrication process of these structures. Finally, the chapter discusses the electrical characteristics of these devices.

Empirical models are developed for these fabricated devices in Chapter 3 which aid in designing digital logic circuits in GaN. The chapter also briefs about the process integration and discusses the electrical characteristics of fabricated logic inverters. Fabricated samples were gamma irradiated and the results of this experiment are discussed. Finally, the chapter presents AlGaN/GaN FinFET design approaches [10] to make the channel less susceptible to radiation induced damage.

The final chapter of the thesis discusses the fabrication process of AlGaN/GaN FinFETs using E-Beam defined fins. It also discusses the electrical characteristics of the fabricated FinFETs. A summary of the work is presented along with future possibilities in this chapter.

Chapter 2

GaN Digital Logic Transistors

2.1 Background

When a thin film of AlGaN is grown heteroepitaxially on GaN, the interface is strained and results in piezoelectric polarization induced two-dimensional electron channel, referred to as 2-D Electron Gas (2DEG) [6]. This chapter introduces depletion mode and enhancement mode HEMT structures, both of which form the building blocks of the presented digital logic technology. Both devices are integrated on the same epiwafer to enable fabrication of digital logic circuits.

2.2 Depletion Mode (D-Mode) AlGaN/GaN HEMT structure

The depletion load logic family uses pull up normally on devices. These devices use the standard AlGaN/GaN HEMT structure (Figure 2.1). The energy band diagram of this structure is shown in Figure 2.2.

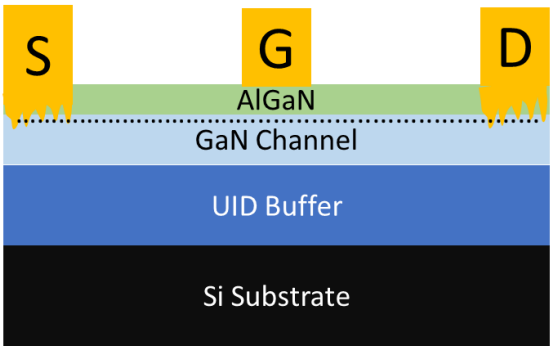


Figure 2. 1 AlGaN/GaN Depletion Mode HEMT structure

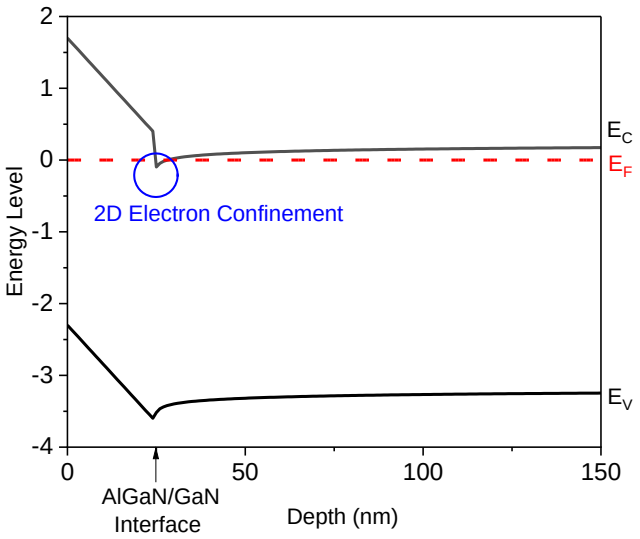


Figure 2. 2 Energy band diagram of an $Al_{0.25}Ga_{0.75}N$/GaN system

The 2D triangular confinement of electrons in at the AlGaN/GaN interface is shown in the energy band diagram. The charge control model can be used to estimate the carrier concentration. For an AlGaN/GaN HEMT structure, 2DEG concentration n_s is given by [11]:

$$n_s\,(V_G) = \frac{Q_\pi\, d_{AlGaN} - \epsilon\left[V_G - \left(\phi_b - \frac{\Delta E_C}{q}\right)\right]}{qD} \qquad \text{Eq 2.1}$$

Q_π is the net polarization charge concentration due to piezoelectric and spontaneous polarization. The distance D includes the shift of the centroid charge distribution from the heterointerface by δd. The 2DEG concentration is dependent on the thickness of the barrier layer and the Al composition of the barrier. The energy band diagram of an AlGaN/GaN system computed using BandEng [12] shows the 2D confinement of electrons forming the 2DEG channel along the source drain axis of the HEMT.

2.3 Enhancement Mode (E-Mode) HEMTs

Normally-off GaN HEMTs can be realized by using many types of structures including recessing the AlGaN under the gate or structures with completely etched AlGaN (under the gate) MOS structures [13]. With each structure having their own advantages and trade-offs, this work uses the Gate Injection Transistor (GIT) structure as it provides best threshold voltage invariability and process repeatability [14]. The radiation endurance of GITs is also expected to be better compared to the MOS structures. The GIT structure uses a highly acceptor doped gate which pinches-off the channel underneath the gate by hole injection [15], [16].

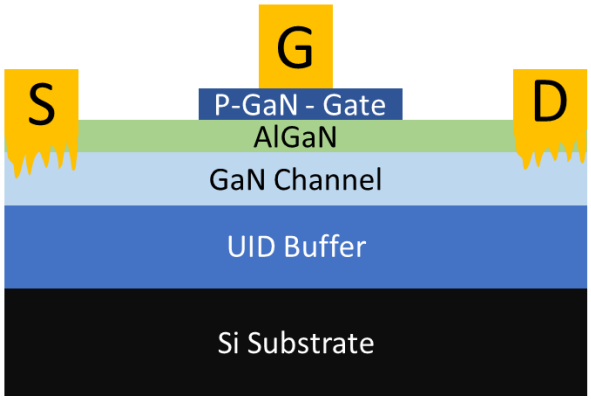


Figure 2. 3 E-Mode Device (GIT) Structure

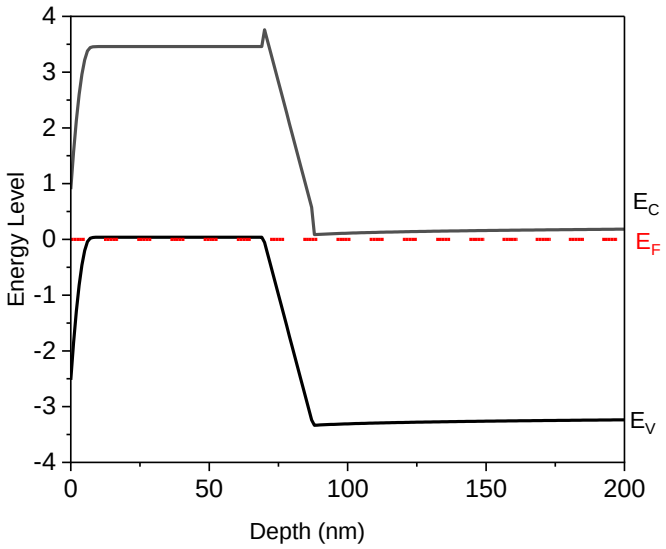


Figure 2. 4 Energy band diagram of a p-GaN/AlGaN/GaN system

2.4 Transistor Fabrication Process

The integration of E-Mode and D-Mode devices is enabled by MOCVD grown p-GaN capped AlGaN/GaN wafers. The D-Mode devices are obtained by etching the p-GaN cap layer. The gate of the E-Mode devices is defined by the Mg doped ($1x10^{19}$ cm^{-2}) 70 nm

P-GaN layer. The epitaxial structure used, and its energy band diagram are shown in Figure 2.5 and Figure 2.4.

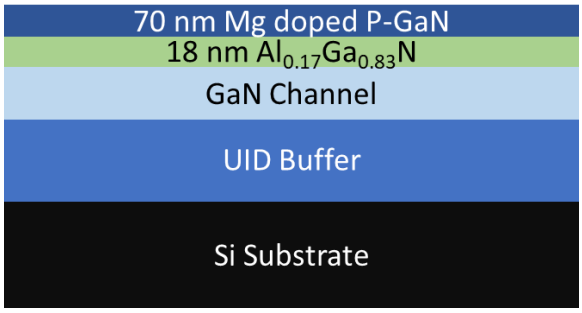
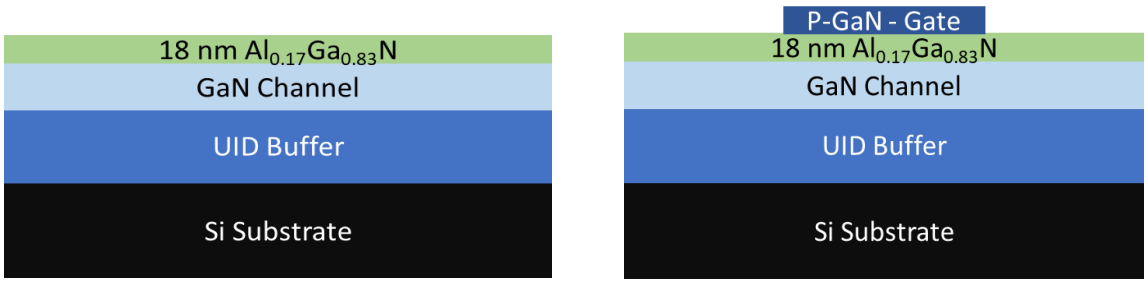


Figure 2. 5 E/D Mode Epitaxial Structure

STEP 1: Definition of P-GaN Gate

The E-Mode device gates are defined by slow dry etching of the P-GaN layer. Initially the gates are pattered using SPR955 photoresist exposed using Heidelberg Maskless Aligner MLA 150. The etch recipe uses Cl_2 and BCl_3 flows with an RF voltage of 40 V and 40 W ICP power. The plasma is cycled in loops of 2 minutes with 1 minute stabilization intervals resulting in an average etch rate of 10.5 nm/min (excluding stabilization). The etch depth is controlled by timing the recipe and estimating the etch rate of each iteration with a calibration chart. The depths are validated by measuring gate step heights using AFM.



D-Mode after P-GaN etch E-Mode After P-GaN etch

Figure 2. 6 Devices after P-GaN Gate definition

STEP 2: Mesa Isolation of Devices

In this step, individual devices are isolated. Mesas are created in the active area by etching away the channel outside the devices. The RIE etch is continuous with Cl_2 and BCl_3 flows with an RF power of 30 W succeded by the slow etch recipe described in the previous step. Typical mesa etch depths were around 170 nm.

STEP 3: Deposition of Ohmic contacts

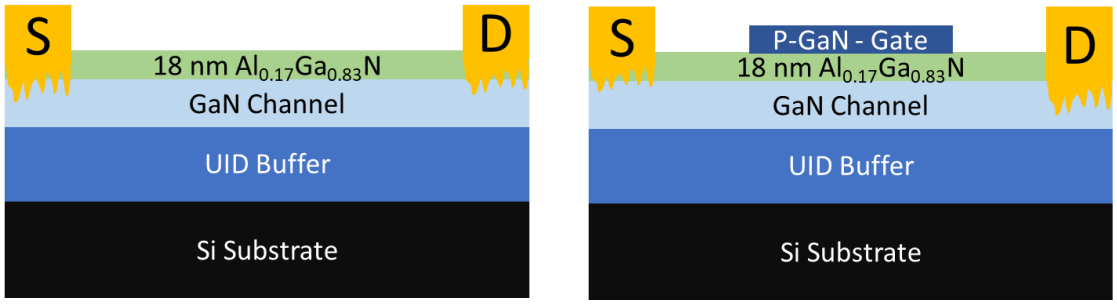
Ohmic contacts are e-beam evaporated to make source and drain contacts. A bilayer process using LOR5A and SPR955 resists is used to achieve good lift-off and metal features. The ohmic metal stack is deposited in the order shown in Table 2.1.

Metal	Thickness (Å)
Ti	200
Al	1200
Ni	300
Au	500

Table 2. 1 Ohmic Metal Stack

STEP 4: Rapid Thermal Annealing of Ohmic contacts

The deposited metal stack in step 3 is annealed to form alloyed Ohmic contacts. When annealed at 860^{o} C in N_2 ambient for 30 seconds, the metal alloy forms spikes that contacts the 2DEG channel. This process is well optimized to achieve low contact resistances. Figure 2.7 shows the devices after metal stack deposition and thermal annealing.



D-Mode E-Mode

Figure 2. 7 Devices after source/drain ohmic metal deposition and annealing

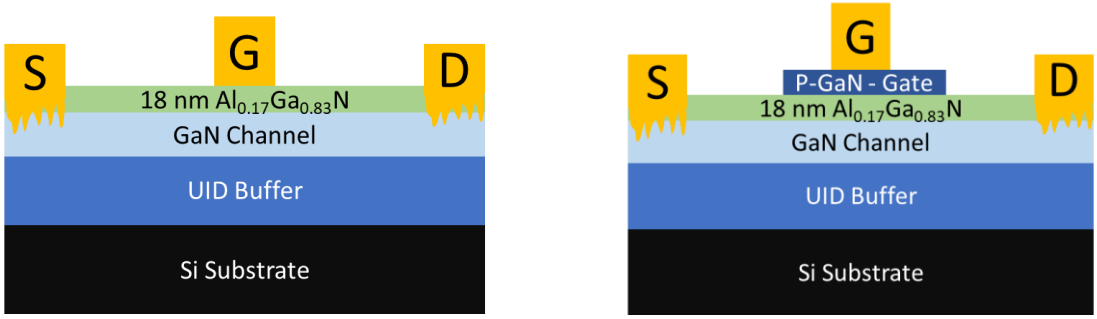
STEP 5: Interconnects, Pads and Gate Contact

Ni forms Schottky gate contact with AlGaN and a low-barrier height contact with P-GaN. The gate metal stack, pads and interconnects are patterened with the same bilayer process used in Ohmic stack deposition. The stack is e-beam evaporated in the following order:

Metal	**Thickness (Å)**
Ni	300
Au	1000
Ni	500

Table 2. 2 Gate Metal Stack

The finished device structures are shown in Figure 2.8. Completed devices are generally passivated with SiN_x and passivation windows are opened with an extra dry etch step.



D-Mode E-Mode

Figure 2. 8 Final device after fabrication

2.5 Device Characteristics

Figure 2.9 and Figure 2.10 shows the measured DC characteristics of fabricated D-Mode devices. On-wafer DC characterizations were performed with a B1500A. The characterized device has a width of 12 µm, 2 µm gate length, 1 µm source and drain region access region lengths. Using hall effect measurements, the measured sheet resistivity was 1140 Ω/sqr, sheet carrier density was 3.72×10^{12} cm^{-2} and hall mobility was 1490 $cm^2V^{-1}s^{-1}$. The D-Mode devices had a threshold voltage of -1.8 V.

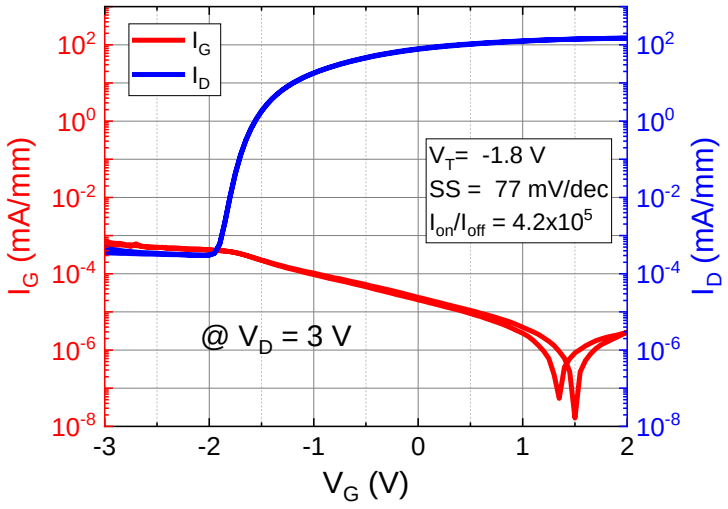


Figure 2. 9 D-Mode HEMT Transfer Characteristics

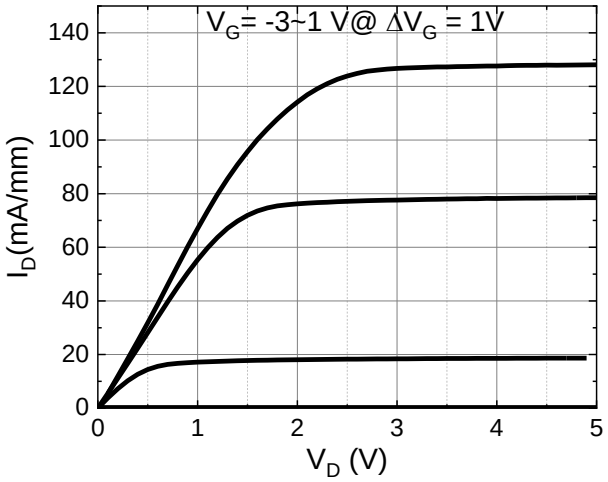


Figure 2. 10 D-Mode Device DC Characteristics

Figure 2.11 and Figure 2.12 show the DC characteristics of the E-Mode device with the same dimensions as the D-Mode device characterized. The E-Mode device has a thereshold voltage of 1 V.

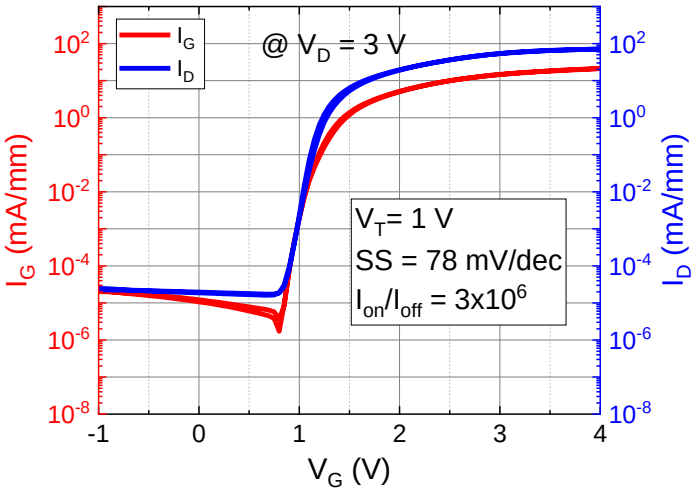


Figure 2. 11 E-Mode Device Transfer Characteristics

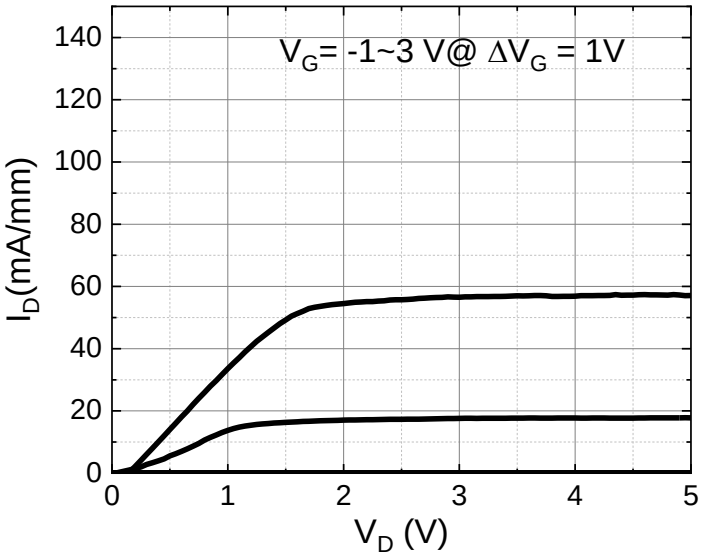


Figure 2. 12 E-Mode Device Output Characteristics

Chapter 3

Integration of Radiation Tolerant GaN Devices and Circuits

3.1 Background

This chapter presents how the D-Mode and E-Mode devices are monolithically integrated to make GaN digital logic circuits. Digital logic inverters and gates based on Depletion Load Logic (DLL) [5], [17]–[20] were designed and fabricated. The chapter also discusses how empirical device models were developed for E-Mode and D-Mode devices for enabling circuit simulations.

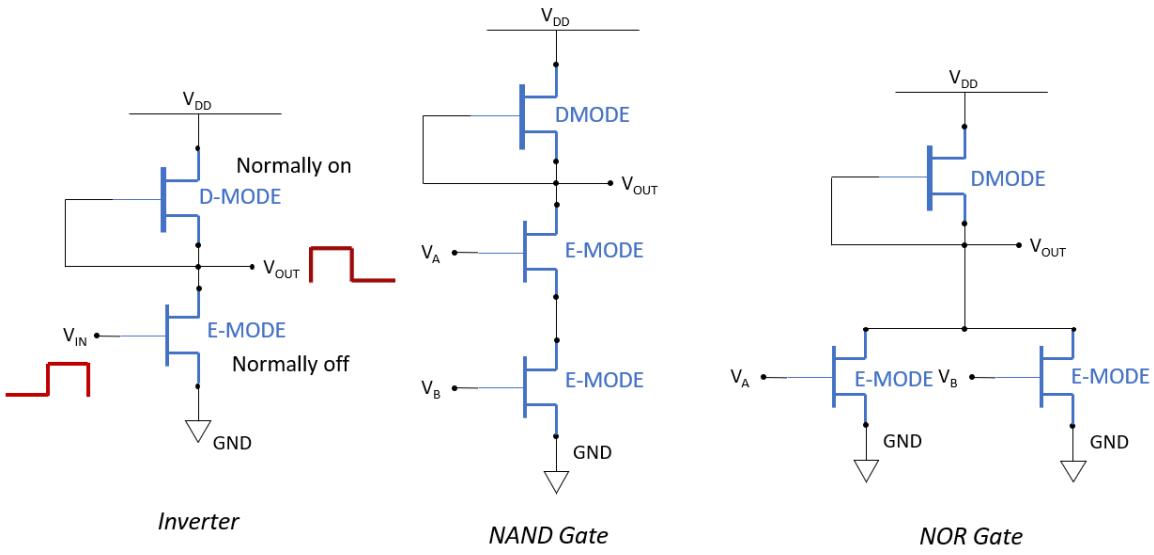


Figure 3. 1 Depletion Load Logic Gates

Depletion Load Logic uses ratioed D-Mode devices for pull up with the core logic implemented using pull down E-Mode devices. The dimensions of the devices must be carefully designed to get good noise margins. Figure 3.1 shows the schematics of some gates implemented using DLL.

3.2 E/D-Mode Empirical Device Models

To enable the design of complex digital logic circuits with this technology, accurate device models are needed. This section describes the development of empirical models for drain current and process of parameter extraction from measured device data.

The drain current model requires the transfer, output, and the gate current characteristics for parameter extraction. A tool to automatically fit and extract various parameters was developed on MATLAB (Appendix A). These parameters are fit into the output drain current equation given by:

$$I_D = K_1 \tanh(K_2 V_{DS}) (1 + K_3 V_{DS}) \qquad \text{Eq. 3.1}$$

Parameters K_1, K_2, and K_3 are gate bias dependent and are calculated using polynomial fitting functions. The physical significance of these parameters and the polynomial functions are shown in Table 3.1.

Fitting Parameter	Physical Dependence	Polynomial Fitting Function
K_1	Transconductance (g_m) and Saturation Velocity (v_{sat})	$= M_1V_{GS}^4 + M_2V_{GS}^3 + M_3V_{GS}^2 + M_4V_{GS} + M_5$
K_2	On-Resistance (R_{on})	$= P_1V_{GS}^5 + P_2V_{GS}^4 + P_3V_{GS}^3 + P_4V_{GS}^2 + P_5V_{GS} + P_6$
K_3	Output conductance in saturation ($g_{o\text{-}sat}$)/ effect of I_G on I_D	$= A_1V_{GS}^4 + A_2V_{GS}^3 + A_3V_{GS}^2 + A_4V_{GS} + A_5$ (D-Mode) $= A_1V_{GS}^5 + A_2V_{GS}^4 + A_3V_{GS}^3 + A_4V_{GS}^2 + A_5V_{GS} + A_6$ (E-Mode)

Table 3. 1 Drain Current Fitting Parameters

The model extraction process flow is shown in Figure 3.2. The process works by recursively fitting I_D-V_D curves into Eq 3.1. Nonlinear fitting solutions are obtained using the Levenberg-Marquardt algorithm [21]. The fit is performed for each I_D-V_D range dependent on V_{GS} and K_1, K_2 and K_3 are obtained for each fit. These obtained parameters are fit into n^{th}-order polynomials with V_{GS} as the independent variable. The process results in coefficients M_i, P_i and A_i for these polynomials. A similar process is followed to fit the gate turn-on characteristics of the device to a linear-exponential function. These coefficients with the fitting functions are written into a Verilog-A file which can be imported into any supported circuit simulator like Cadence Virtuoso for digital logic design.

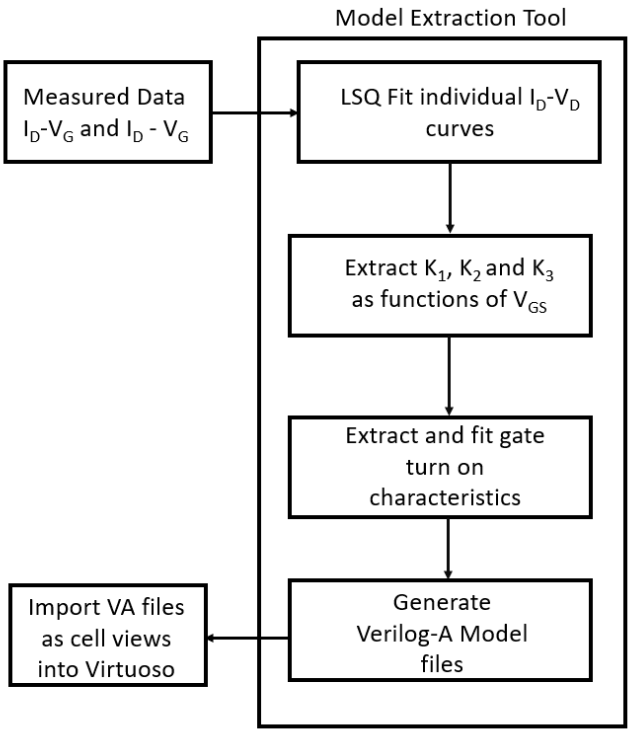


Figure 3. 2 Model Extraction Process Flow

Transfer and output characteristics of fabricated devices were measured using a B1500A. Output characteristics were measured with gate voltage steps of 50 mV to obtain a good model fit. D-Mode device matched characteristics shown in Figure 3.3 and Figure 3.4 had a width of 100 um with access region lengths of 2 um and gate length of 4 um. E-Mode devices, characteristics shown in Figure 3.5 and Figure 3.6, were 100 um wide with source to gate access length of 2 um, gate to drain access length of 3 um and gate length 3 um.

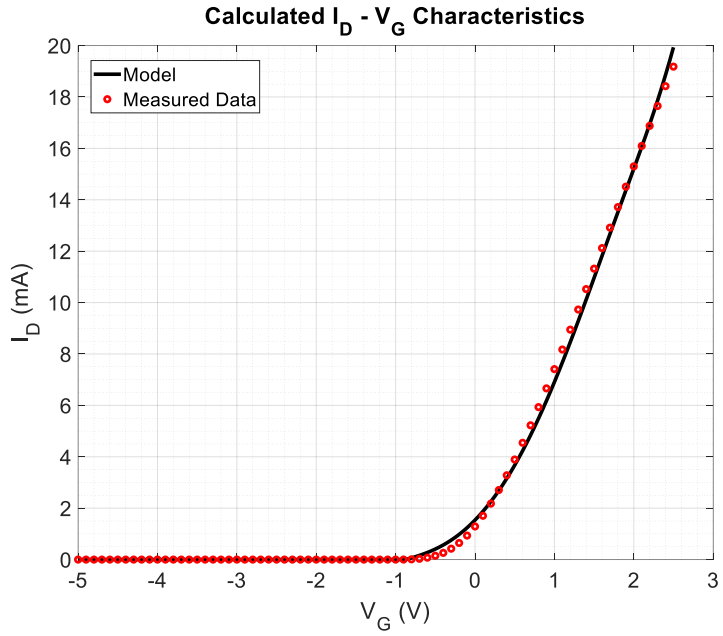


Figure 3. 3 Matched D-Mode Transfer Characteristics (V_D = 5 V)

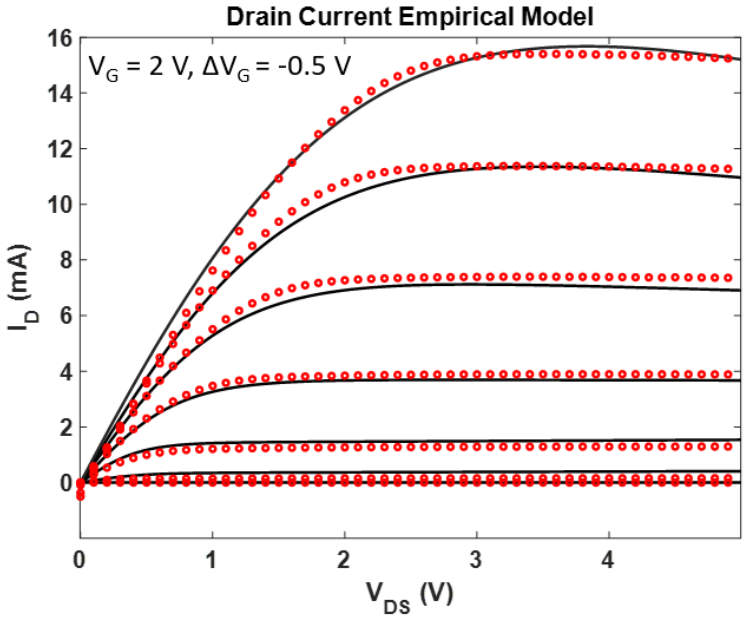


Figure 3. 4 Matched D-Mode Output Characteristics

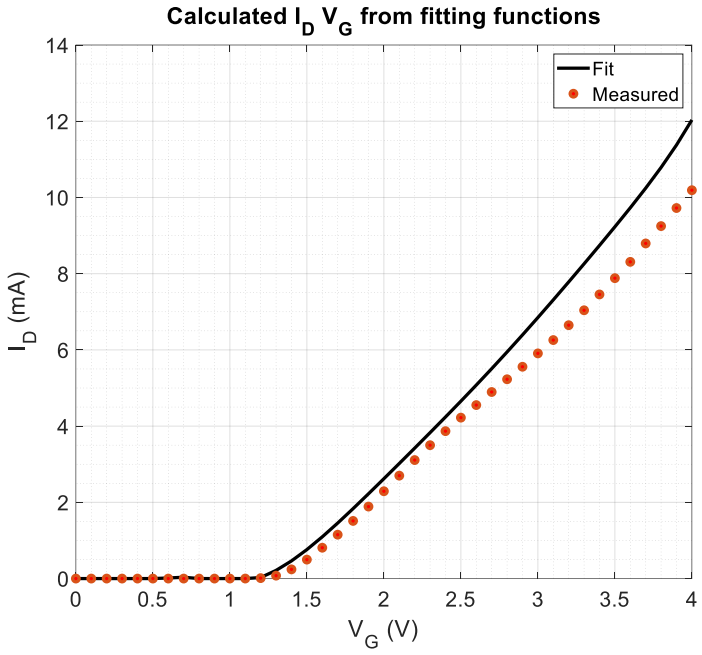


Figure 3. 5 Matched E-Mode Transfer Characteristics (V_D = 5 V)

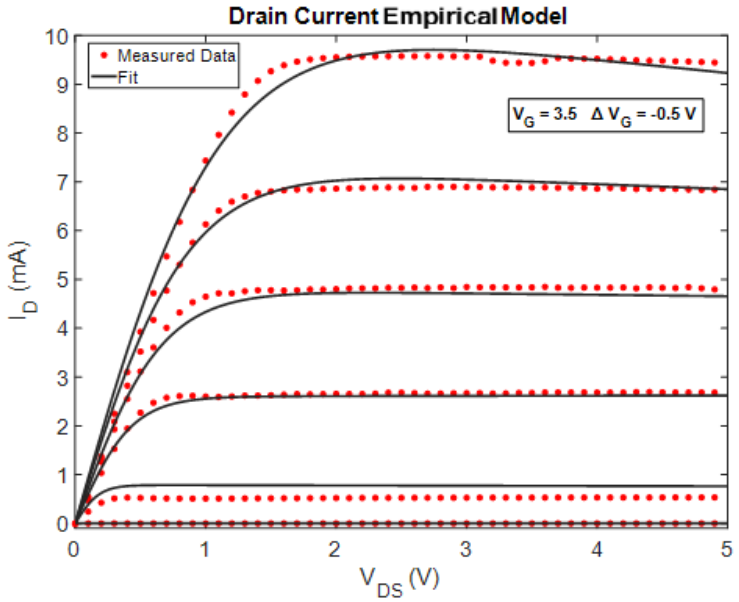


Figure 3. 6 Matched E-Mode Output Characteristics

3.3 Process Integration of Digital Logic on GaN

The developed models were used to design logic inverters, NOR and NAND gates. Layout for all the cells were done on K-Layout, a free open-source layout design tool [22].

To enable rapid development of layouts, Parametric Cells (P-Cells) were developed in Python. The P-cells are completely scalable with auto generation of all process layers. This process includes one layer of metal (M1) for pads and interconnects. Table 3.2 shows the different process layers. The layouts for an E-Mode device and a logic inverter are shown in Figure 3.7.

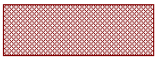
	Active/Mesa
	P-GaN Gate
	Ohmic Contact
	M1/Pads/Gate Contact

Table 3. 2 Process Layer Definitions

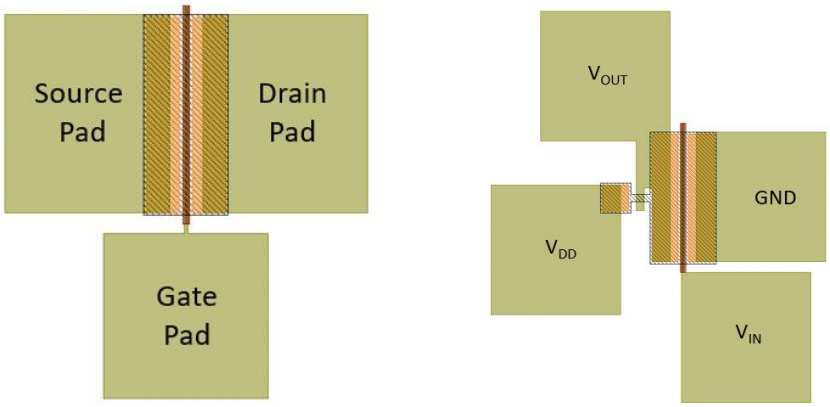


Figure 3. 7 Layout of an E-Mode Device (left) and Logic Inverter (right)

The process flow used to fabricate the E/D-Mode logic cells was discussed in section 2.4. Layer M1 makes Schottky gate contact with the D-Mode devices and is used for interconnects and pads. Features were directly written using MLA150 with 0.6 um critical dimensions. It was critical to consider lithography tolerances to account for layer misalignment. Micrographs of fabricated cells are shown in Figures 3.8 and 3.9.

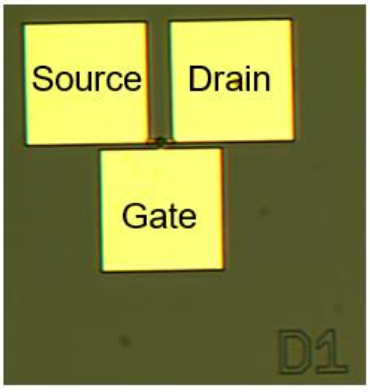
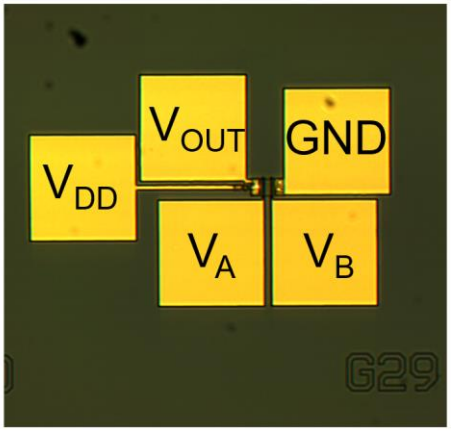
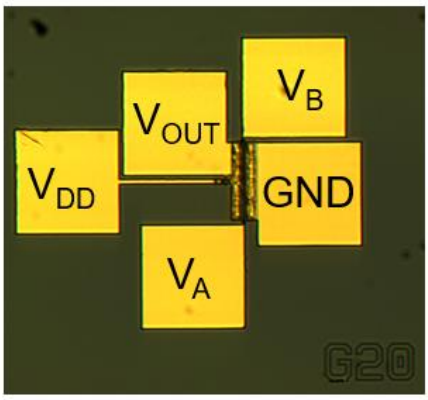


Figure 3. 8 Fabricated E/D-Mode Device

INVERTER



NAND GATE



NOR GATE

Figure 3. 9 Micrograph of Fabricated Digital Logic Cells

3.4 Characterization of Digital Logic

The fabricated inverters were powered with a V_{DD} of 3V. They were characterized and the Voltage Transfer Characteristics (VTC) of the inverters are shown in Figure. 3.10. Both the D-Mode and E-Mode devices of the inverters have gate lengths of 1 um. The D-Mode device widths of INV 1, INV 2 and INV 3 are 2 um, 2 um and 4 um. The widths of the E-

Mode devices were chosen conservatively to achieve good pull-down strength and reasonable V_{OL} with GIT widths of INV1, INV2 and INV3 of 16 um, 24 um and 40 um. Noise Margins of these inverters are shown in Table 3.3.

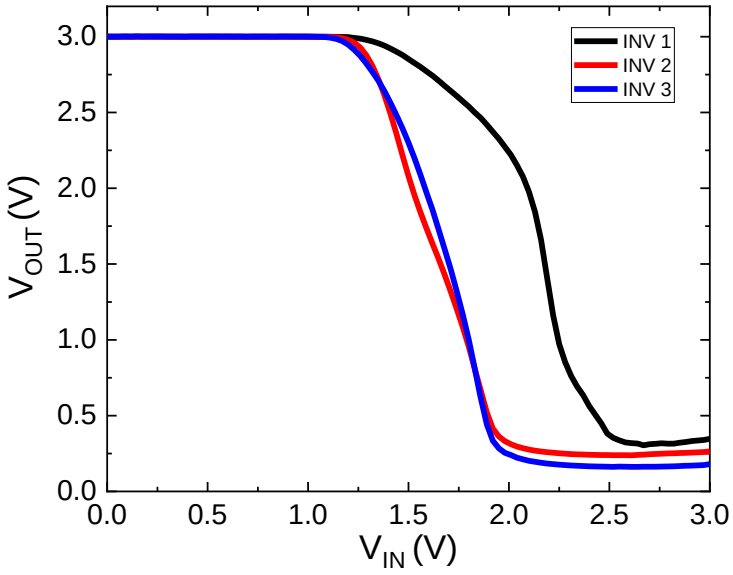


Figure 3. 10 VTC of fabricated logic inverters

	INV 1	**INV 2**	**INV 3**
V_{OH} (V)	3	3	3
V_{OL} (V)	0.35	0.26	0.18
V_{IH} (V)	2.49	1.95	1.95
V_{IL} (V)	1.62	1.23	1.12
NM_H (V)	0.51	1.05	1.05
NM_L (V)	1.27	0.97	0.87

Table 3. 3 Characteristics of fabricated logic inverters

INV1 was probed with the probes were connected to a DC power supply, an oscilloscope, and a waveform generator. The input of the inverter was excited with a 1 kHz pulse and the waveforms are shown in Figure 3.11. The V_{OL} (output low) was measured to be 0.35 V with a V_{OH} (output high) of 3 V.

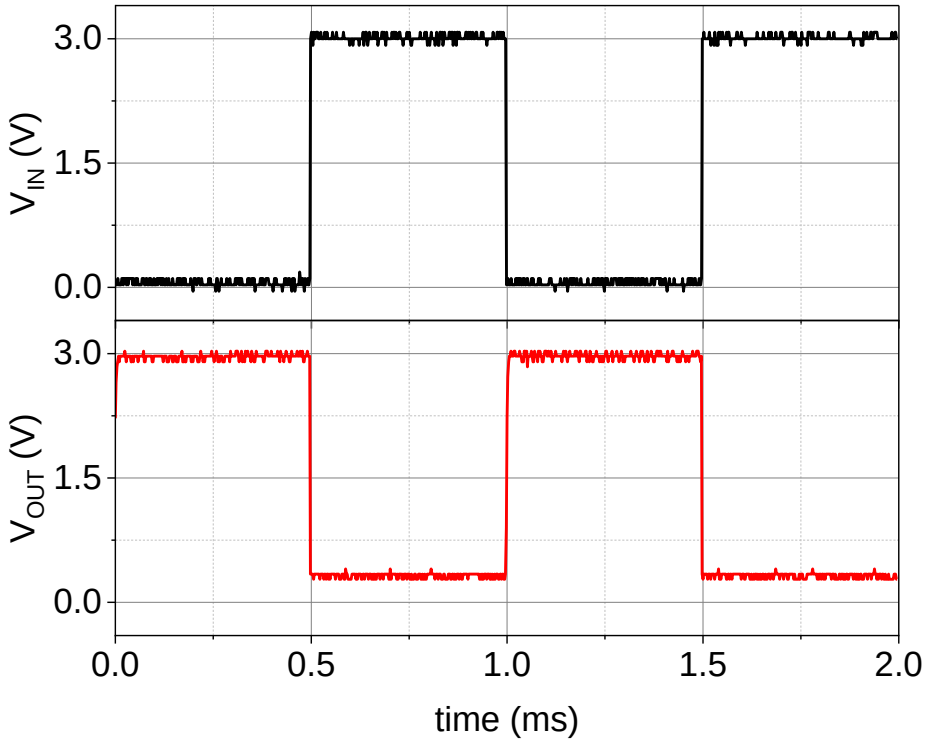


Figure 3. 11 INV 1 transient waveforms

3.5 Tolerance to Ionizing Radiation

The use of radiation hard electronics ranges from front end reactor electronics to space applications. Various studies have shown Gallium Nitride's high resistance to gamma radiation [3],[23].

To study the effect of gamma radiation on the presented digital logic technology, the fabricated devices and gates were exposed to gamma radiation produced from decay of ^{60}Co. The GaN on Si samples (Figure 2.8) were inside plastic wafer shipper when loaded into the reactor chamber. The samples accumulated a net dose of 5.04 MRad. Electrical characterizations were performed pre and post radiation.

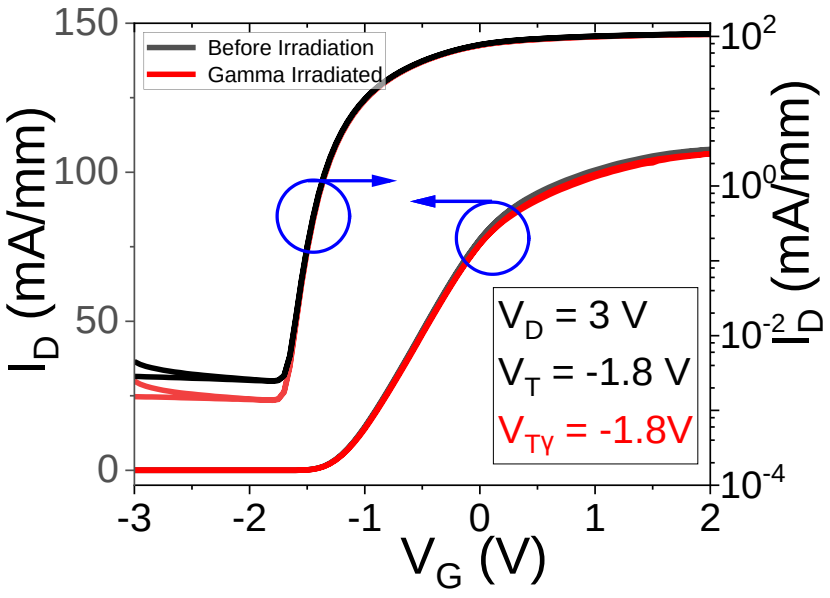


Figure 3. 12 D-Mode transfer characteristics before and after gamma irradiation

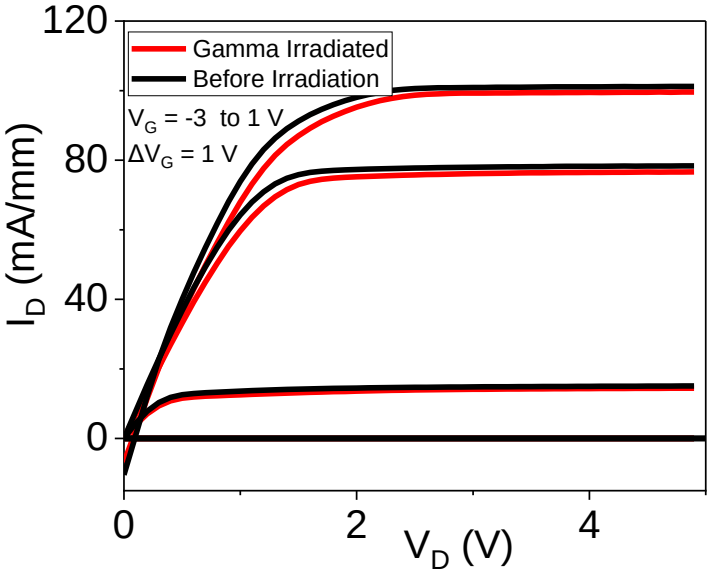


Figure 3. 13 D-Mode transfer characteristics before and after gamma irradiation

Capacitance-Voltage and hall measurements were also performed along with DC characterization. For the accumulated gamma dose, no significant changes in electrical performance were observed. The hall sheet resistivity, carrier density and mobility remained unchanged for both the irradiated samples. The C-V characteristics of both E-Mode and D-Mode devices are shown in Figure 3.14 showing no threshold voltage shift compared to a control sample.

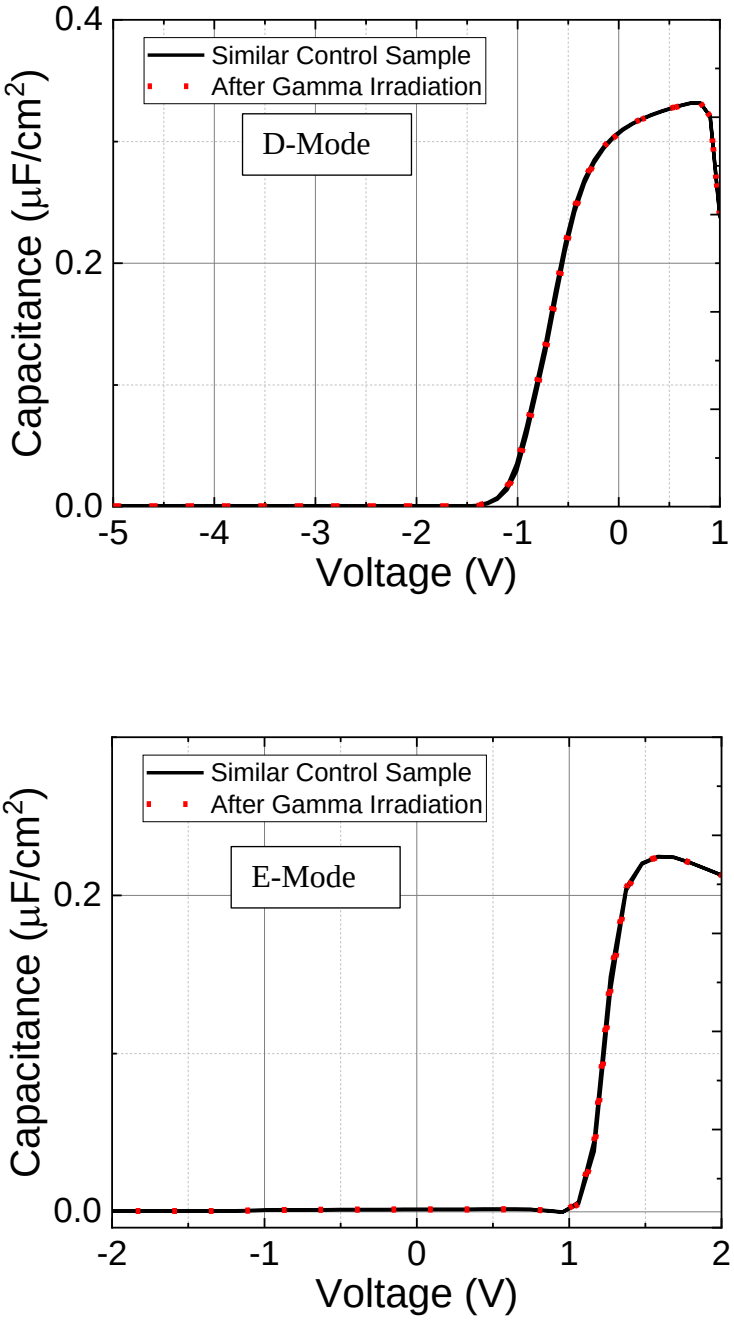


Figure 3. 14 Capacitance-Voltage characteristics of irradiated and unirradiated devices

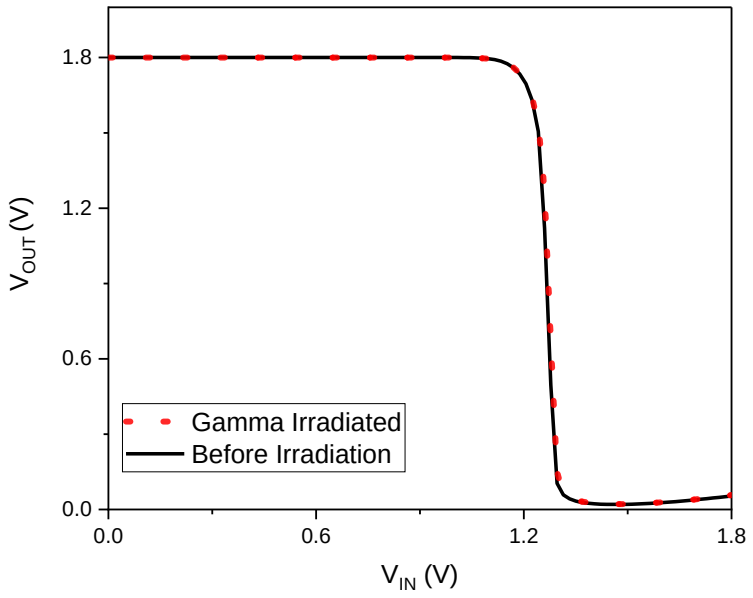


Figure 3. 15 VTC of logic inverter before and after gamma irradiation

The unchanged electrical characteristics resulted in no changes in the VTC of logic inverters (Figure 3.15) on both the samples. Si MOSFETs have shown significant degradation after accumulating a few hundred kRad of gamma dose [24]–[26] proving monolithic GaN as a great candidate for gamma radiation tolerant electronics.

3.6 Displacement Damage Tolerant Devices

When semiconductor materials are exposed to particle fluences, scattering with atoms in lattice creating and/or activating trap states affecting the threshold voltage significantly [27]. The energetic knockout by neutrons and protons causes lattice site vacancies V_{Ga} (Gallium Vacancy) and complexes in GaN which acts as electron traps [28]–[30]. These

acceptor-like V_{Ga} sites are ionized near the 2DEG in the AlGaN/GaN HEMT images positive charges in the channel resulting in a positive threshold voltage shift and degradation in transconductance.

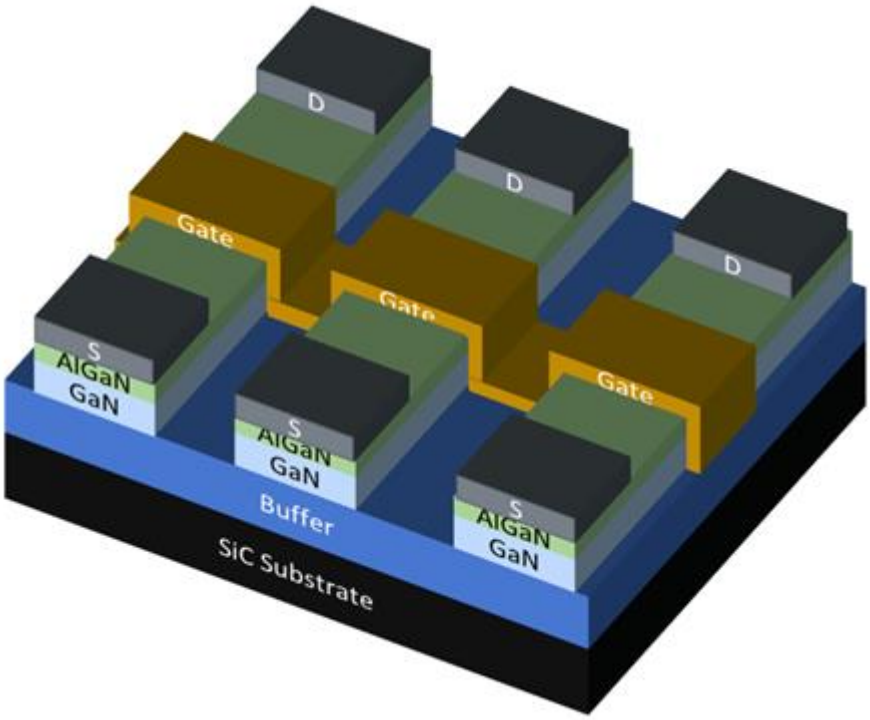


Figure 3. 16 AlGaN/GaN FinFET

To mitigate the effect of displacement damage and effectively screen the channel from effect of buffer damage, FinFET structures are explored in this section. Mamouni et. Al showed the dose dependence of fin-width, threshold voltage and subthreshold swing on ionizing radiation induced damage caused at the gate oxide interface in Si MOSFET

structures [31]. This study showed the electrostatic advantage provided by the 3D structure reducing the effect of radiation damage on threshold voltage. The effect of buffer damage in AlGaN/GaN FinFET structures are simulated by introduction of acceptor like states caused by knockout damage throughout the devices caused by particle irradiation using TCAD tools. The electrostatics of FinFETs reduces the effects of buffer damage.

Silvaco TCAD HEMT models for planar and 3D fin geometries were developed to simulate the effects of these radiation induced traps. Effects of high displacement damage was simulated by addition of deep acceptors to the channel and buffer layers of the device. The structure used to simulate had a 25 nm $Al_{0.25}Ga_{0.75}N$ cap layer with a 300 nm UID GaN channel. The background doping was assumed to be $5x10^{15}$ cm^{-3} donors.

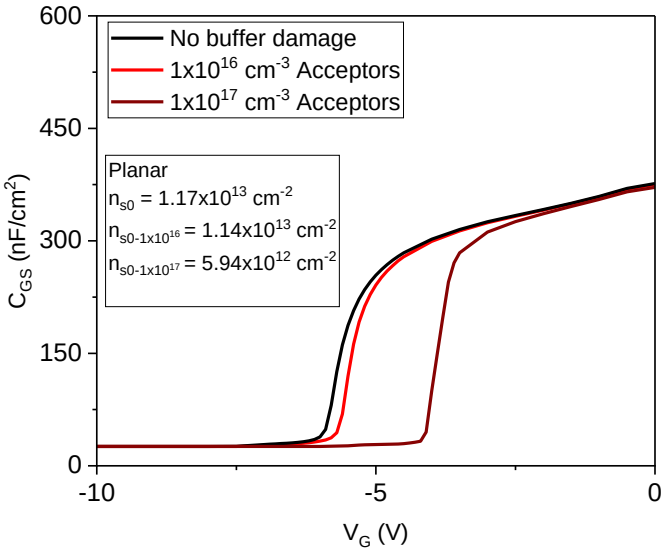


Figure 3. 17 Displacement Damage C-V characteristics of a planar structure

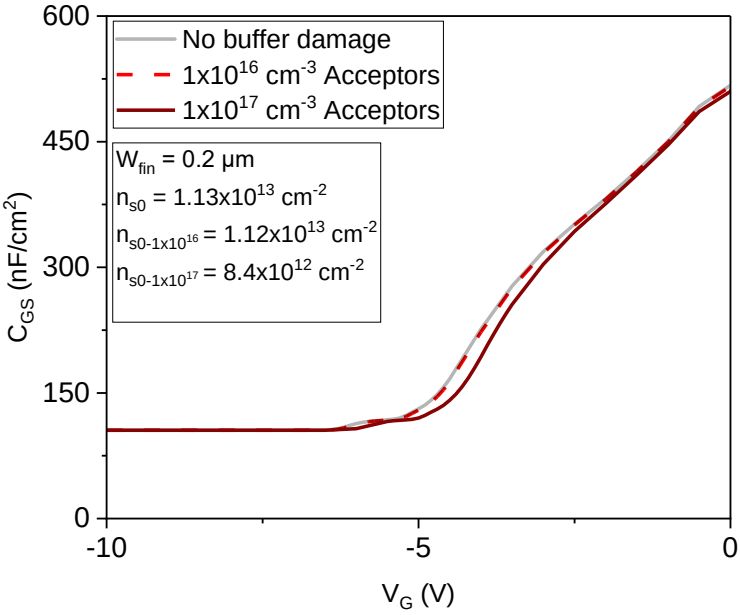


Figure 3. 18 Displacement Damage C-V characteristics of 3-D Fin geometry

The C-V characteristics of AlGaN/GaN structures with planar and fin geometries were simulated at 1 MHz. The structure with the narrowest fin channel was least affect by radiation induced traps with the planar structure most affected. The improved resistance to radiation can be explained by the gate metal imaging the acceptors generated by radiation induced damage in the buffer, rather than directly affecting the 2DEG channel like in the planar devices.

Chapter 4

Future Work

4.1 Looking Ahead

Last chapter explained the development of radiation tolerant technology and how fin geometries could make these devices more robust. This chapter presents the fabrication process and device characteristics of highly scaled AlGaN/GaN FinFETs [10] using electron-beam lithography. Various FinFETs with different fin densities were fabricated aided by layout automation using Parametric Cells (P-Cells). At the time of writing this thesis, particle radiation and high ionizing dose (>100 MRad) experiments are being planned to study the effects of and validate the radiation robustness of these structures.

4.2 Processing of AlGaN/GaN FinFETs

The process flow for fabrication of AlGaN/GaN FinFETs is very similar to the process flow presented in chapter 2. The patterning of fins was performed using Vistec EBPG5000 E-Beam Lithography system with CSAR 6200 resist with all the other lithography performed with the MLA150. The gate contact was Ni/Au/Ni and the source and drain were alloyed Ti/Al/Ni/Au. The devices were processed on AlGaN/GaN on SiC epitaxial

wafers obtained commercially. The AlGaN cap layer had an Al mole fraction of 25% and was 22 nm thick with a 300 nm GaN channel layer.

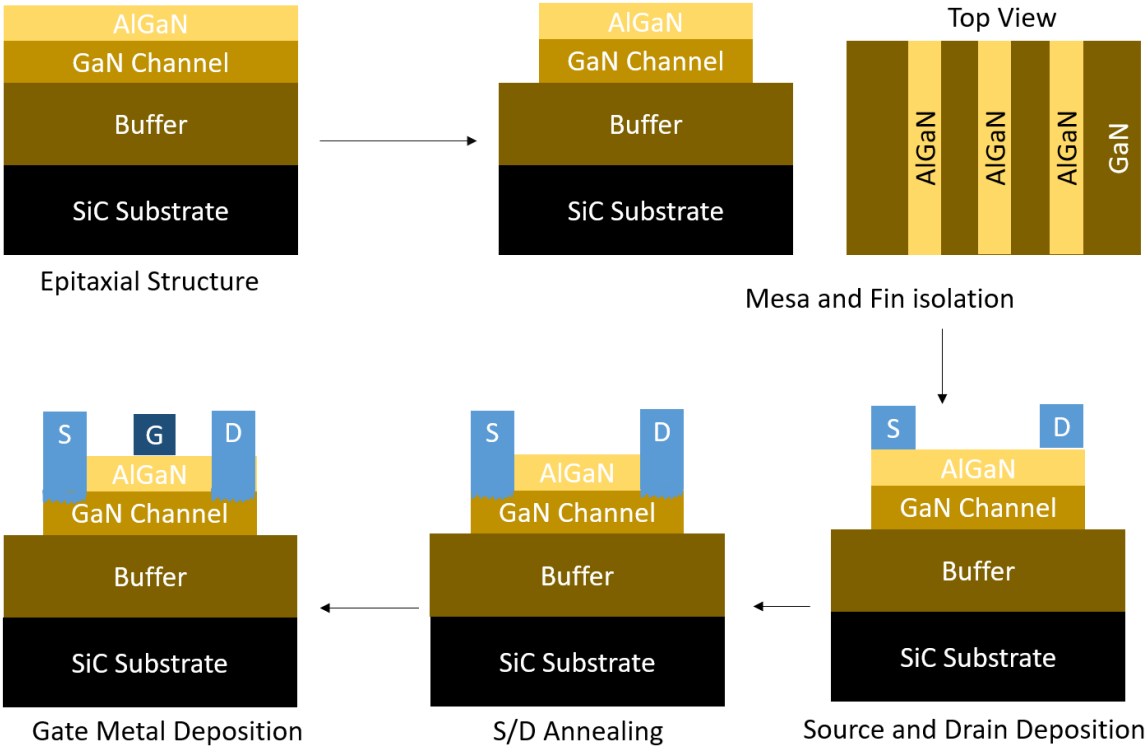


Figure 4. 1 AlGaN/GaN FinFET process flow

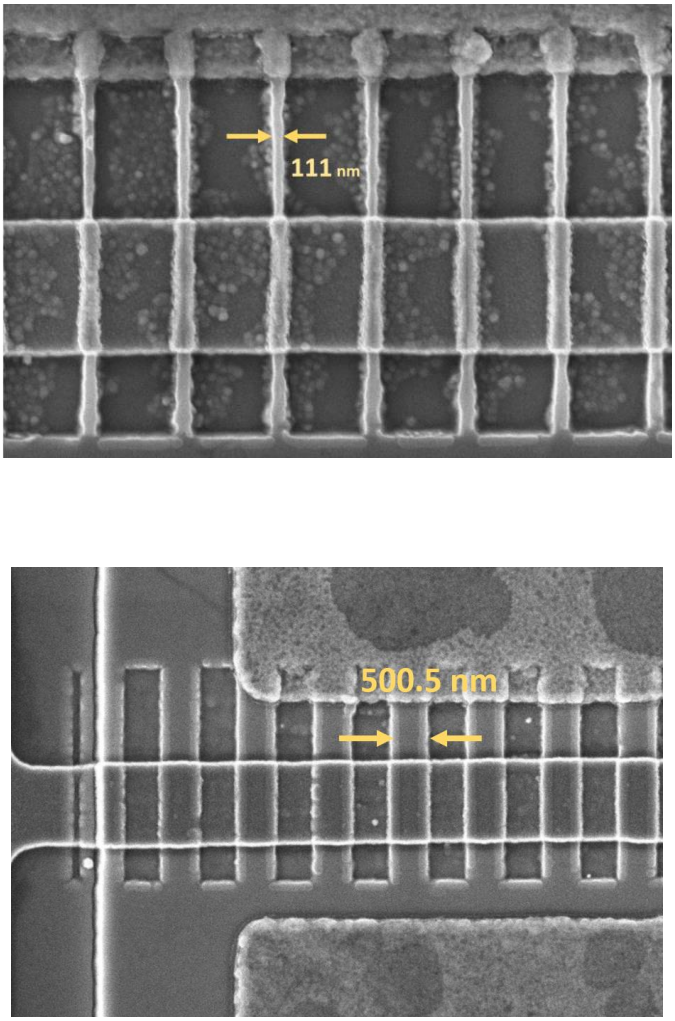


Figure 4. 2 SEM images of the fabricated FinFETs

The Output and Transfer characteristics of a FinFET with 54 fins is shown in Figure 4.3. The device was 54 um wide with 100 nm wide fins. The spacing between the fins was 900 nm with L_G = 1 um. The currents were normalized to the effective channel width (product of number of fins and device width).

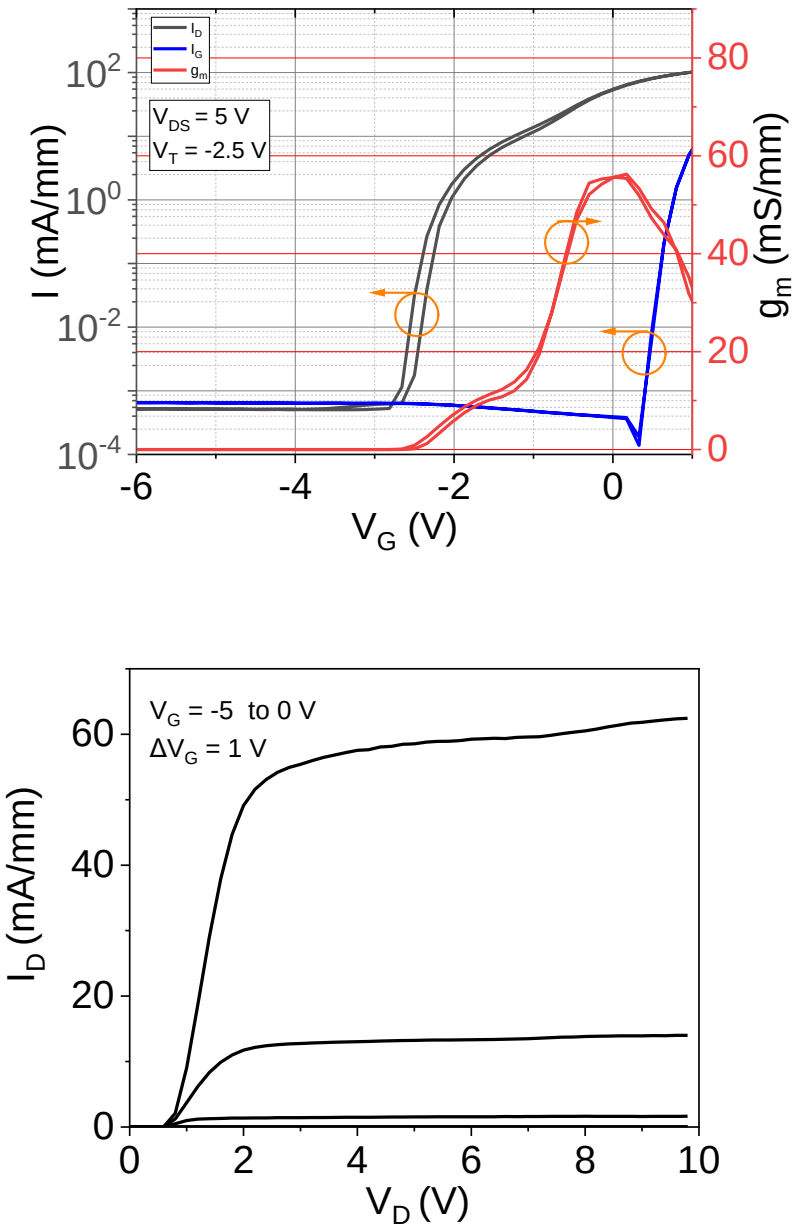


Figure 4. 3 DC I-V characteristics of the fabricated 100 nm FinFET

Hall effect measurements were performed on the sample and the sheet resistivity was 258 Ω/sq with a sheet carrier density of 1.05×10^{13} cm^{-2}. A misalignment in the source side of the device caused the annealed source contact to wrap around the channel. This caused the channel to be pinched off near the source which is what resulted in non-ohmic behavior in the linear region of operation. The damage tolerance of fin structures is to be evaluated by subjecting them to displacement damage once the device process and performance are optimized.

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Appendix A. Device Model Extraction

A.1 Fitting Process

I_D-V_G, I_G-V_G and I_D-V_D characteristics are measured and exported into csv format. These files are imported into MATLAB and the following example script is run to fit I_D – V_D characteristics for a measured gate bias:

```
function [k] = fitIDVD(idvd_meas,vg_select,genplot);


idvd_filter=[];
for i=1:size(idvd_meas,1)
    if(idvd_meas(i,5)==vg_select)
        idvd_filter = [idvd_filter; idvd_meas(i,:)];
    end
    if(idvd_meas(i,5)>vg_select)
        break;
    end
end


Vd = idvd_filter(:,1);
ID_meas = idvd_filter(:,2);

IDF = @(k,vds) k(1).*tanh(k(2).*vds).*(1+k(3).*vds);

k0 = [0.00788  1.1 -0.017];

k=[];
[k,resnorm,~,exitflag,output] =
lsqcurvefit(IDF,k0,Vd,ID_meas);

if(genplot);
plot(Vd,IDF(k,Vd));
hold on
```

```
scatter(Vd,ID_meas);
end

end
```

The coefficients K_1, K_2 and K_3 (Table 3.1) are returned by the function for the fit gate bias using method of least squares and Levenberg-Marquardt method. This function is run in a loop to establish a polynomial relationship between gate bias and the fitting coefficients.

```
idvd_meas = readmatrix("idvddat.csv");
kvg =[];
for vi=-1:1:4
   disp(vi)
   kvg = [kvg; vi fitIDVD(idvd_meas,vi,true)];
   hold on
end
```

Once the relationship is established, these coefficients are fit with V_G (similar to the initial fit process with corresponding expressions from Table 3.1) to obtain polynomial expressions to make these coefficients bias dependent. These bias dependent coefficients are written into a Verilog-A file.

A.2 Verilog-A Models

The following code shows an example Verilog-A drain current model extracted from a 100 um **D-Mode** device with L_G = 4 um, L_{SG} = 2 um, L_{GD} = 2 um:

```
// VerilogA for EmpModel, dmode, veriloga

`include "constants.vams"
`include "disciplines.vams"
```

```
module dmode(s,g,d);
     inout s,g,d;
     electrical s,g,d,b;
     //K1 Fitting Params
     real k1, M1,M2,M3,M4,M5;
     //K2 Fitting Params
     real k2,P1,P2,P3,P4,P5,P6;
     //K3 Fitting Params
     real k3,A1,A2,A3,A4,A5;
     //IG Fitting Params
     real G1,G2;
     // Variables
     real vg,vds,id_fit,ig_fit;
     real vth1;

     analog begin
     //Voltages
     vth1=0.5;
     vg=V(g,s);
     vds=V(d,s);
     //vsat dependent fitting parameter

     M1=-0.000101270485190979;
     M2=0.000629634251574028;
     M3=0.00244848863709883;
     M4=0.00322127412127163;
     M5=0.00142303929594126;
     k1 = M1*pow(vg,4)+M2*pow(vg,3)+M3*pow(vg,2)+M4*vg+M5;
     //R_on dependent fitting parameter
     P1=-0.00541342262049338;
     P2=  0.0895025727957739;
     P3=-0.451485290562668;
     P4=1.26363739834778;
     P5=-2.25685985765049;
     P6=2.24009181627455;
     if(vg>0)
          k2 =
P1*pow(vg,5)+P2*pow(vg,4)+P3*pow(vg,3)+P4*pow(vg,2)+P5*vg+P
6;
     else
          k2=2.3;

     //Output conductance in saturation
     A1=0.00162321143321224;
     A2=-0.00782934222292554;
```

```
     A3=0.0128745296507768;
     A4=-0.0411514069338882;
     A5=0.0157951740885520;
     k3 = A1*pow(vg,4)+A2*pow(vg,3)+A3*pow(vg,2)+A4*vg+A5;

     G1 = 0.000150151901711791;
     G2 = -0.000247754169073040;

     ig_fit = G1*vg+G2;
     id_fit = k1*tanh(k2*vds)*(1+k3*vds);


     if(id_fit>=0)
          I(d,s)<+id_fit;
     else
          I(d,s)<+0;
     end


endmodule
```

The following code shows an example Verilog-A drain current model extracted from a 100 um **E-Mode** device with L_G = 3 um, L_{SG} = 2 um, L_{GD} = 3 um:

```
// VerilogA for EmpModel, emode, veriloga

`include "constants.vams"
`include "disciplines.vams"

module emode(s,g,d);
     inout s,g,d;
     electrical s,g,d;
     //K1 Fitting Params
     real k1, M1,M2,M3,M4,M5;
     //K2 Fitting Params
     real k2,P1,P2,P3,P4,P5,P6;
     //K3 Fitting Params
     real k3,A1,A2,A3,A4,A5,A6;
     //IG Fitting Params
     real G1,G2;
     // Variables
```

```
      real vg,vds,id_fit,ig_fit;
      real vth1;

      analog begin
      //Voltages
      vth1=0.7;
      vg=V(g,s);
      vds=V(d,s);
      //vsat dependent fitting parameter
      M1=0.000236156359138656;
      M2=-0.00216463890662841;
      M3=0.00804822303812048;
      M4=-0.00969021658179320;
      M5=0.00332473587844094;
      k1 = M1*pow(vg,4)+M2*pow(vg,3)+M3*pow(vg,2)+M4*vg+M5;
      //R_on dependent fitting parameter
      P1=-0.266817665703647;
      P2=4.24848603878910;
      P3=-26.8999347219502;
      P4=84.8146627972914;
      P5=-134.002782573141;
      P6=86.8418793435242;
      k2                                                          =
P1*pow(vg,5)+P2*pow(vg,4)+P3*pow(vg,3)+P4*pow(vg,2)+P5*vg+P
6;
      //Output conductance in saturation
      A1=0.00665842251357183;
      A2=-0.0967786280167862;
      A3=0.551578594120391;
      A4=-1.54492467509120;
      A5=2.11447856706935;
      A6=-1.12484277035713;
      k3                                                          =
A1*pow(vg,5)+A2*pow(vg,4)+A3*pow(vg,3)+A4*pow(vg,2)+A5*vg+A
6;

      G1 = 0.000150151901711791;
      G2 = -0.000247754169073040;

      ig_fit = G1*vg+G2;
      id_fit = k1*tanh(k2*vds)*(1+k3*vds);
```

```
        if(id_fit>0 && vg>vth1)
             I(d,s)<+id_fit;
        else
             I(d,s)<+0;
        end


endmodule
```