Experimental and Simulated Analysis of Voltage Stress Within a Bar-Wound Synchronous Machine Excited by a Silicon Carbide Inverter

Thesis

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By

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Abstract

Advancements in semiconductor technology present new challenges in electric machine construction, operation, and control. Silicon carbide (SiC)-based power electronics are becoming the new standard for high-power consumer and commercial devices, and are implemented in technologies such as power inverters, converters and rectifiers. This paper focuses on the effects of inverter drives for traction motors in electric vehicles with high dV/dt rates on bar-wound machine windings, including the expected impacts on insulation materials under prolonged periods of high voltage stress. Partial discharge inception voltage testing was performed to evaluate the voltage bus level at which breakdown will start to occur. A simulation model was constructed using finite element analysis, the results of which were validated with experimental results using a commercially available SiC inverter and traction motor. Correlation has been established between the preliminary simulation results and experimental data. It is proven that as DC bus voltages increase with the capabilities of SiC devices, the voltage stresses inside the stator windings approach levels which could cause partial discharge and premature insulation degradation in existing stator designs.

Acknowledgments

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Chapter 1. Introduction

Until recently, limited mobile energy storage capacity in forms other than combustible fossil fuels has hampered the widespread use of electric traction machines in the automotive industry. Rapid advancements in battery technology within the last two decades have allowed several manufacturers to offer electrified vehicles which are competitive in many respects to traditional internal combustion engine-powered vehicles. However, the prices of energy and power dense batteries remain high, and even the most energy dense batteries pale in comparison to the energy density of gasoline or diesel fuel. For both reasons, manufacturers desire to minimize the battery capacity of their vehicles while still maintaining decent drivable range and dynamic performance.

One way to reduce necessary energy storage is by increasing efficiency and thereby reducing losses. There are several ways to reduce electrical losses in an electrified vehicle, the most prevalent of which are increasing the voltage of the high voltage bus and designing less lossy electric machines and power electronics. The limiting factor in bus voltage selection for an electrified vehicle is often the operating voltage of the power electronics, which is determined by the semiconductors within. Traditional inverters and converters are silicon-based. Silicon (Si) in its pure form is the most widely used semiconductor in the industry due to its scale of manufacturing and associated low cost.

Silicon carbide (SiC) is quickly becoming the new standard semiconductor for next-gen power electronics over elemental Si because of its performance in many aspects. Its wider electrical bandgap allows for switching at much higher temperatures, voltage, and frequencies, which results in better longevity, efficiency and dynamic performance, respectively.

However, concerns exist with the application of SiC devices in electric machine drives [3]. The higher rated voltage of the power electronics means that the machine can also be driven at higher voltages, increasing performance and efficiency, but at the cost of increased insulation to avoid breakdown and partial discharge. Insulation degradation has already been observed with silicon-based inverters on AC machine windings [5]; quicker switching transients can produce even higher voltage overshoots at the input terminals of the machine, which further stress machine windings and insulation. Machines currently driven by silicon-based power electronics observe voltage transients of around 5 kV/μs, but SiC can increase the rise and fall times to upwards of 20 kV/μs [17]. These voltage stresses are the focus of this investigation.

General Motors (GM) is among several large automotive manufacturers which will be using SiC-based power electronics to increase system performance in their products along with the transition to an 800 V architecture from more typical bus voltages of 400 to 600 V DC. This study is part of an effort by GM to understand the overall system impacts of using SiC in inverters. The traction machine used in the Chevrolet Bolt

electric vehicle, a three-phase interior permanent magnet synchronous motor (IPMSM), is the basis of this analysis; understanding the voltage stresses in a machine under typical DC bus levels is necessary before making improvements in future designs to compensate for the risks of insulation breakdown. Complete stator and rotor assemblies were provided by GM, along with an off-the-shelf reference design package from CREE/Wolfspeed. The construction of the stator is advanced, utilizing bar windings. Bar-wound machines are also referred to as hairpin-wound or form-wound, but for consistency will be referred to as bar-wound throughout this paper. Bar windings have advantages over traditional stranded windings including high slot-fill and surface contact with the stator, increasing thermal dissipation from the windings [9]. Also important is the significant decrease in difficulty of automating stator manufacturing with rigid bar windings. For these reasons, bar-wound machines are often cheaper to manufacture, are more efficient and have better performance compared to similarly sized stranded machines [17]. The use of SiC power electronics in driving bar-wound traction motors is likely to become commonplace across the automotive industry [9], as both have significant benefits over current generation technologies.

Figure 1. Chevy Bolt traction motor assembly with section view of hairpin windings [15]

Previous works have explored voltage stresses within machine windings [1-6]. The procedure for this paper largely follows the progress made by [1,2] examining the voltage stresses inside a strand-wound IPMSM, with significant adaptations because of the difference in winding configuration. These examples serve as partial validation of the approach presented in this paper.

Other publications explore the degradation of winding insulations by [6, 9, 11, 12]; it has been determined that the functional lifetime and performance of electric vehicle (EV) powertrains can be significantly reduced by this phenomenon. If the voltage overshoot and ringing produced by switching devices with a high dV/dt rate are significant enough, current traction machines will need to be redesigned with more robust insulation to compensate for the potential difference between windings [6].

This study analyzes the voltage stress in the Chevy Bolt stator windings through various approaches. First, an experimental testing system was developed using a

CREE/Wolfspeed SiC inverter and a Bolt stator assembly. Custom software was developed to drive the inverter at the desired operating conditions. Voltage measurements were taken at various points in the stator windings, which were used to calculate the voltage stresses between neighboring conductors in the stator slots. To understand the level of voltage stresses present relative to the level at which partial discharge (PD) and subsequent insulation degradation would occur, testing was also performed using a Bolt stator to observe partial discharge inception voltage (PDIV) under varying temperature and pressure ranges. Alongside the experimental testing, a 2D electromagnetic simulation was constructed using ANSYS Maxwell, which utilizes finite element analysis (FEA) and Maxwell's equations for electromagnetism to compute the voltage stresses within the stator windings. The measurements from testing were compared against the simulation results, and correlations were observed. This paper contributes 1) characterization of switching behavior in the CREE/Wolfspeed SiC inverter package connected to bar-wound stator, 2) a method of determining voltage stress within neighboring layers in a slot without measuring each layer, 3) an analysis of voltage stresses within bar-wound stator windings, 4) determination of PDIV for a bar-wound stator assembly under varying temperature and pressure, and 5) construction and implementation of a 2D FEA model to simulate voltage stresses.

Chapter 2 describes the design of the test setup, as well as the measurements and results from testing. The winding construction and methodology for selecting measurement points is also discussed in Chapter 2. Chapter 3 describes the partial discharge inception

voltage (PDIV) testing performed to relate the observed voltage stress levels to voltages at which insulation degradation due to PD could occur. Chapter 3 explains the simulation approach, construction, and performance, including a comparison between simulated and observed voltage stresses. Finally, Chapter 4 derives conclusions about the Bolt stator winding construction and insulation based on these results.

Chapter 2. Machine Construction and Testing

This chapter first explains the Chevy Bolt stator construction and details the selection of test points within the stator windings. The overall test setup including the power supply and inverter is described and depicted. The test procedures, measurements and experimental results are also discussed.

2.1 Stator Construction and Winding Configuration

The traction machine implemented in all production years of the Chevy Bolt as of 2021 is a three-phase wye-connected interior permanent magnet synchronous machine (IPMSM). The stator bar windings pass through 72 total slots and are stacked in six layers within each slot. The winding pattern is of the wave type, with both coil and pole pitch of nine (fully pitched coils). There is one winding turn per coil. Within each phase, current flows through three parallel paths of 24 turns. The two sides of the stator in the axial direction are referred to as the crown and weld sides. On the crown side, the phase leads are connected to the windings, along with the neutral bus. There are jumper bars on the crown side which change the winding sequence between slots periodically because of the winding pattern. The crown side of the stator is shown in Figure 2. All the jumping connections between slots, as well as phase lead and neutral bus connections to the

windings are hidden under the black plastic guard located along the upper right half of the stator crown as seen in Figure 2.

Figure 2. Stator as viewed from the crown side

On the weld side of the stator, the hairpin coils are welded together after insertion into slots during manufacturing. These are the only connections on this side. Because of the difference in voltage phase and amplitude from the phase leads and neutral bus as the windings pass through the stator core from the weld side to the crown side, all measurements described in this study were recorded from test points added to the crown side. For further explanation, if the turn voltage of every turn within one parallel path of one winding phase is measured using connections on the crown side, the sum will be the total line-neutral excitation voltage at that instant. If the same was done on the weld side, the sum would not amount to the same voltage since there is some voltage drop that

exists as the winding passes through the core. This also means that measuring the voltages on the crown side of the stator allows for computation of the voltage relative to the neutral bus at each winding point, which can be used as a common reference between winding phases. A view of the weld side of the stator is shown in Figure 3.

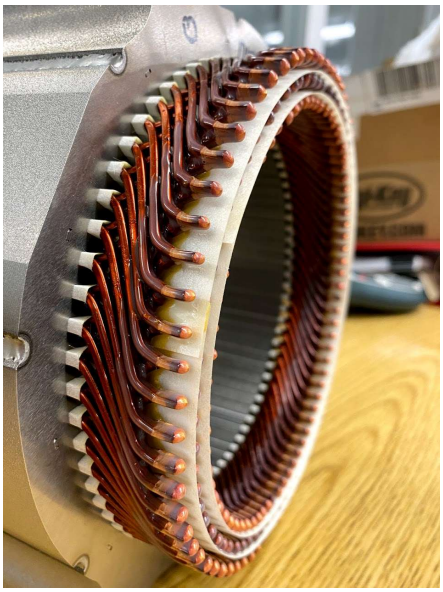

Figure 3. Stator as viewed from the weld side

Also visible in Figure 3 are various insulation types used to electrically isolate conductors. The windings are almost entirely coated in a thin layer of varnish. When the coils are welded together during manufacturing, the weld locations must be stripped of any varnish which might have been applied prior to insertion into the stator assembly. This results in an exposed portion of the coil, and so extra insulation is visible on this side around these locations. The weld points were dipped in a thicker coating of varnish as

seen in the milky coating in Figure 3 near the welds, and insulation paper separates the neighboring winding layers. Also visible are the slot liners which add extra protection between the windings and the grounded stator wall. The slot liners' position within a slot, as well as the ordering of the conductors within the slot is depicted in Figure 4.

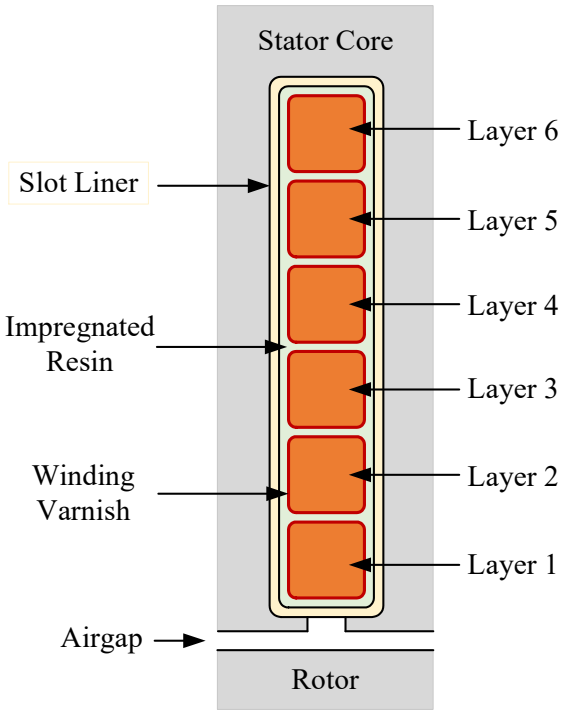

Figure 4. Detail cross-sectional view of winding layers, slot liners and impregnated resin

To determine the location of the measurement points within the windings that serve as the basis for calculating voltage stress, a naming convention was developed using the machine winding diagram provided by GM. Each turn within the winding paths was indexed starting from the turn connected to the neutral bus which was in the closest layer

to the rotor (in Layer 1). The turn naming convention is shown for a single phase, Phase U, in Figure 5. The turn numbers for Phase V and W are provided in the appendix (Figure 56 – 58). In each turn, the coil alternates from one layer to the adjacent layer in the current pair. The first and third parallel paths alternate between two pairs of layers; the first 12 serial turns in the path are in one pair and jump to another pair for the remaining 12 serial turns. This winding configuration balances the electromotive force (EMF) generated between each parallel path in each phase through inductive balancing.

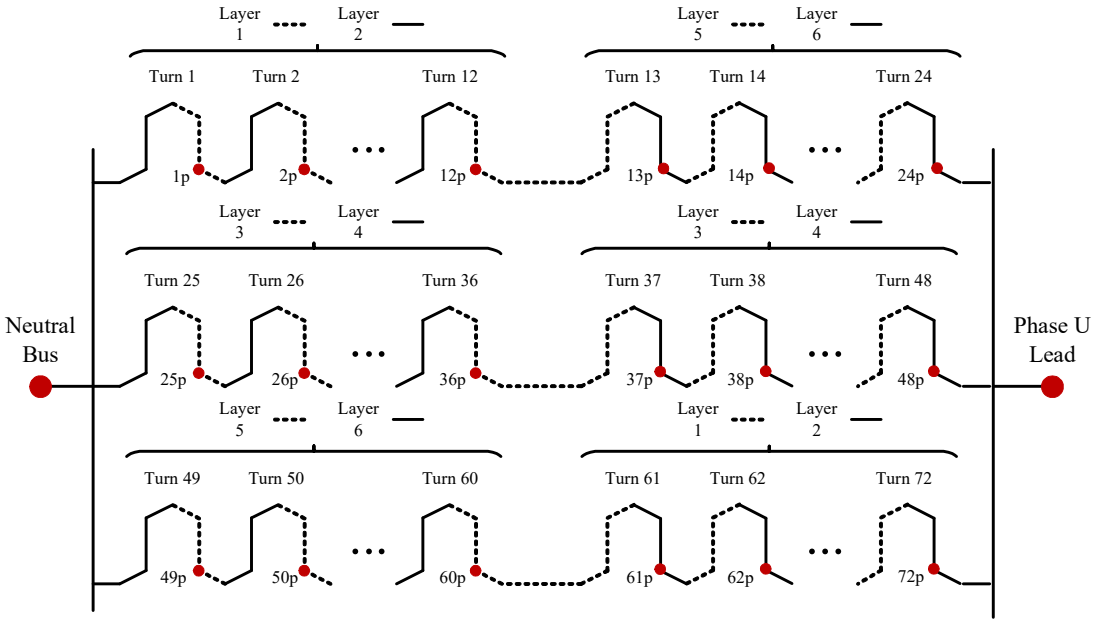

Figure 5. Phase U turn naming convention

The measurement points added to the stator windings are depicted by red dots neighbored by its name in Figure 5. The letter *p* following the name of each test point denotes the measurement as being taken from the positive end of the coil. Only one side of each coil was measured because there is only a small difference in voltage between the end of one coil and the end of the next sequential coil, as they are only centimeters apart from each other at the end windings where the measurements were taken. Also, it is important to measure from the same location at each coil to ensure consistency across all measurement points.

Measurement points were physically incorporated into the stator windings by soldering short lead wires to the windings after carefully removing the insulating varnish from the conductor. The location of the connections was kept as close to the stator core as was possible to remove the effect on the measurements from the end windings on the voltage of the conductor in the slot. Figure 6 demonstrates how the measurement leads were attached. Near the bottom of the image, bare copper is exposed after filing the varnish. Solder was added to the exposed conductor in the middle of the image, then the lead wires were attached at the top. The points' proximity to the exit point of the conductors from the stator core is apparent.

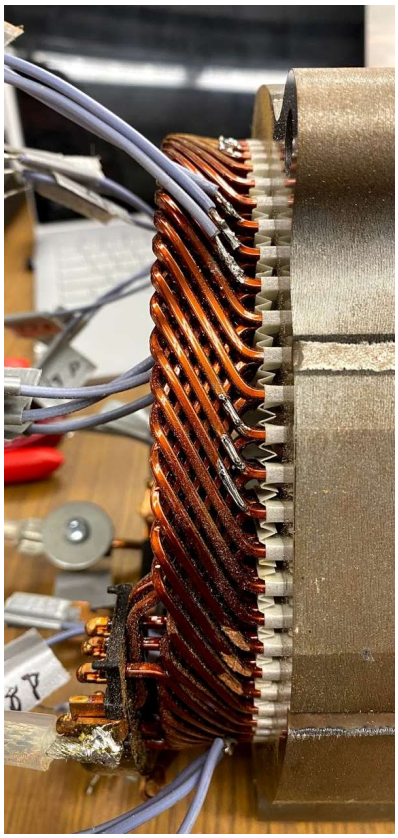

Figure 6. Forming measurement points on the stator windings

After soldering the leads to the stator windings, the exposed conductors at the joints were insulated using several layers of MG Chemicals Super Corona Dope, a highly insulating varnish, and then a thick layer of liquid electrical tape from a local hardware store.

Only one parallel path of turns from each phase was measured due to the inaccessibility of the inner winding layers. Only layer 1 and 6 are easily accessible close to the exit point of the winding from the core. However, the first and last parallel paths of each phase pass through layers 1 and 6 as seen in Figure 5; the first path was selected for testing arbitrarily. Test leads were added along the outer diameter of the windings to capture

points in layer 6 as well as the inner diameter for layer 1. Data from a single parallel path in each phase is sufficient to calculate the voltage stress across all conductors in the windings because of the balanced winding construction; the voltage distribution across serial turns should be identical for a corresponding turn index in each of the parallel paths. In other words, the voltage across the fifth turn in the first parallel path of Phase U should be very similar to the voltage across the fifth turn in the second and third parallel paths of Phase U. This approximation is validated later in the chapter.

An additional test lead was soldered to the neutral bus so that the voltage of each measurement point had a common reference. The connection to the neutral bus is visible in Figure 7.

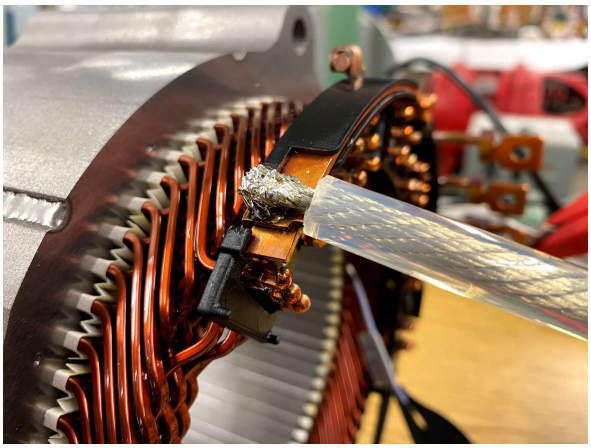

Figure 7. Neutral bus measurement lead with connection

2.2 Inverter

The inverter provided for use in this study is a 300 kW CRD300DA12E-XM3 reference design by the Wolfspeed power products subsidiary of CREE. This is an off-the-shelf package that incorporates CAB450M12M3 half-bridge power modules with SiC MOSFETs and CGD12HBXMP gate drivers [25]. The inverter is liquid-cooled, rated for 900 V at the DC bus and 300 A DC. A schematic provided by CREE for the contents within the reference package is shown in Figure 8. The power density is 32.25 kW/L, which is over twice the density of comparable silicon-based inverters [25].

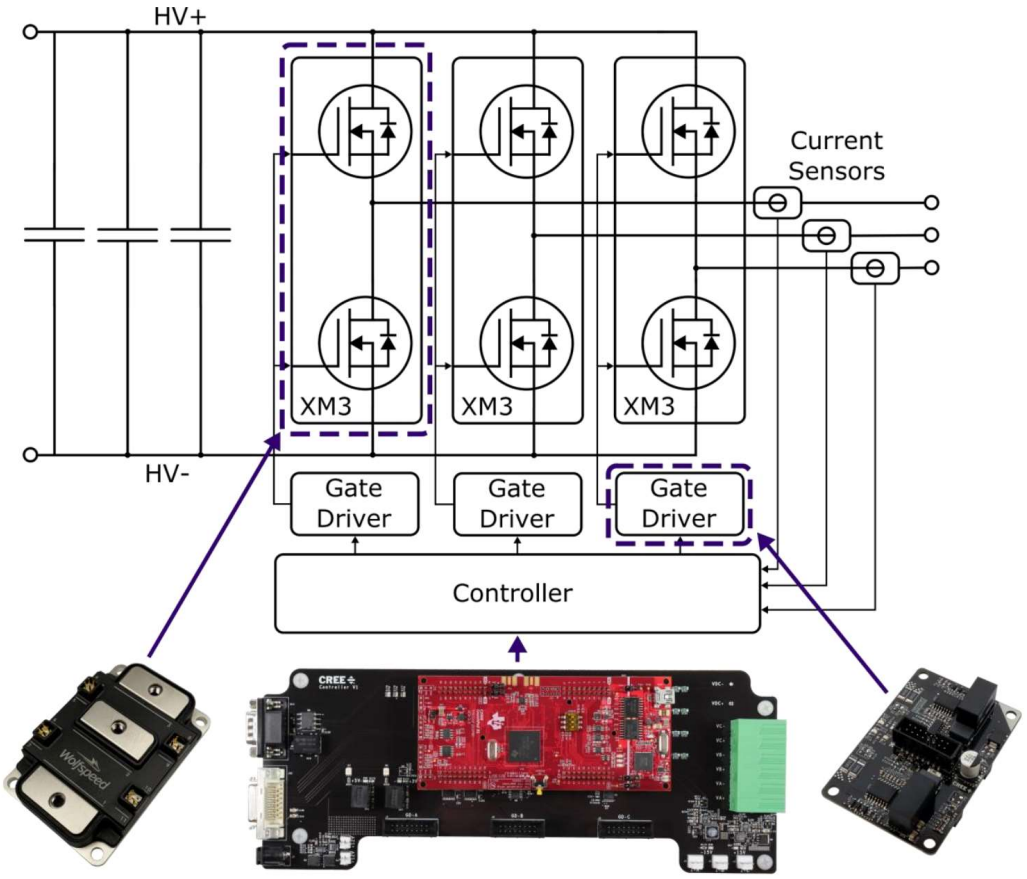

Figure 8. CREE inverter schematic [25]

Inverter functionality was controlled by programming the Texas Instruments TMS430F28379 controller board integrated into the reference design. Included with the board are several peripherals which optimize its performance for real-time controls and signal processing [25]. Existing source code was provided by CREE which generates open-loop 3-phase sine-PWM. The source code was adapted to produce space-vector PWM (SVPWM) using third-harmonic injection, a much more popular control scheme, through the same GUI as provided with the demo software. The user interface with controllable parameters and toggle switches is visible in Figure 9. The software is installed on a personal computer and communicates with the TI controller over a CAN bus. An additional adapter to convert USB communication into CAN was utilized to connect the devices. The software provided with the inverter only generated asymmetrical 3-phase sine-PWM. Custom software was developed and uploaded to the onboard microcontroller which controls the inverter operation to convert the generated waveform to SVPWM.

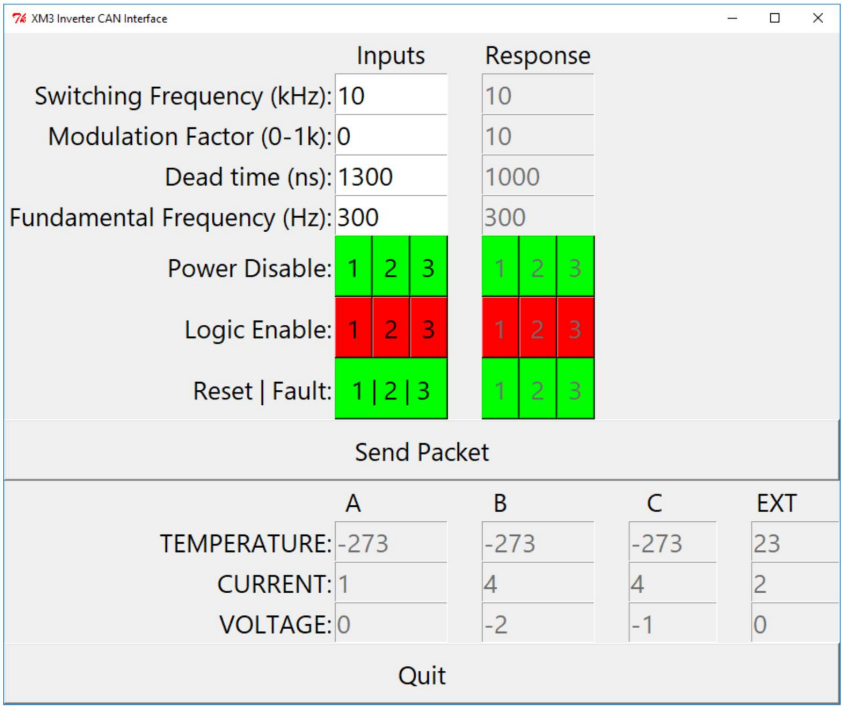

Figure 9. XM3 inverter CAN interface [5]

2.3 Test setup and measurements

The overall system configuration for applying SVPWM voltage waveforms to the stator windings is straightforward. The DC bus terminals are connected to the output terminals from a high-voltage DC power supply from Magna. The inverter AC outputs are connected to the phase leads of the stator windings through the same 8-gauge high voltage cable used to connect the inverter to the power supply. The connection cables were kept as short as possible to minimize inductance, though stray inductances caused by these measurement leads will produce some error. A schematic of the test setup is shown in Figure 10. Figure 11 shows the cables connecting the inverter to the stator windings, as well as some of the test probes used for measuring voltage and current. Figure 12 shows the complete instrumented test setup. A protective shield was placed over the stator assembly as a safety precaution during testing. A box fan was used to provide cooling to the stator. The inverter was water-cooled through tubes connected to the cooling passages of the inverter as visible in the bottom right of Figure 11.

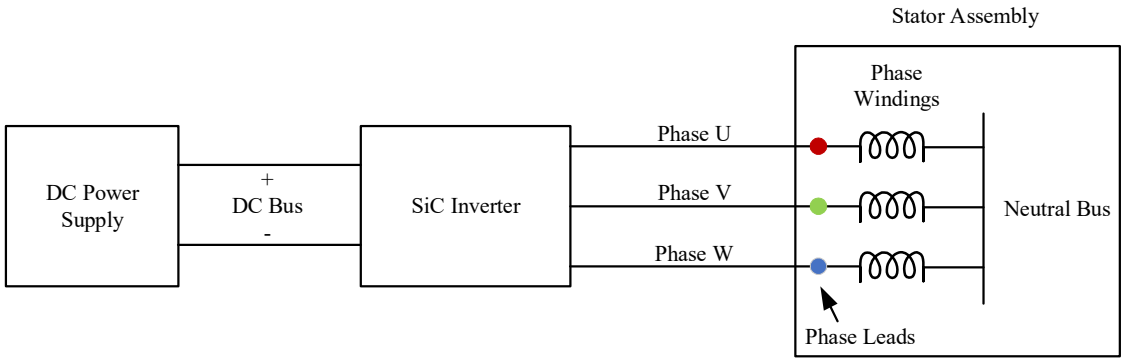

Figure 10. Test setup schematic

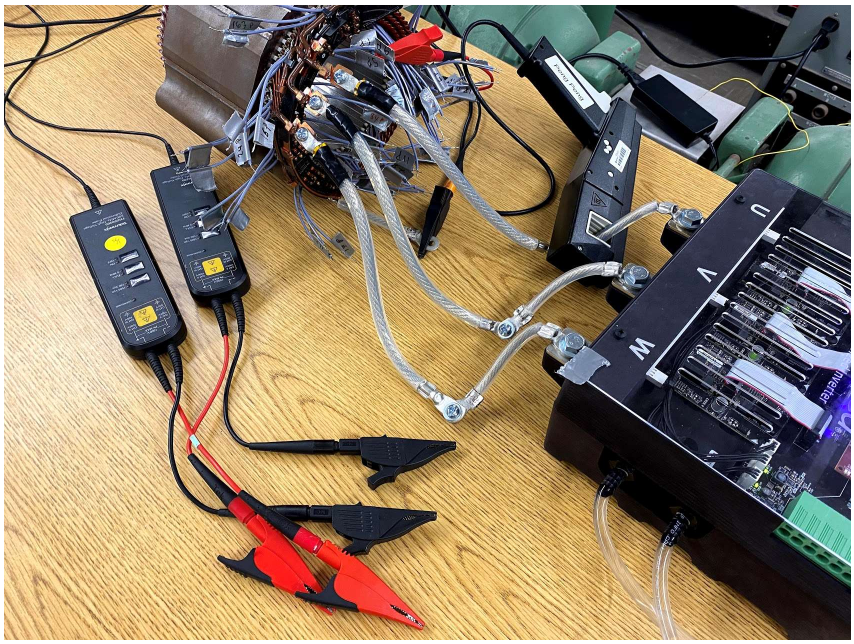

Figure 11. Connection between stator and inverter, and inverter cooling lines

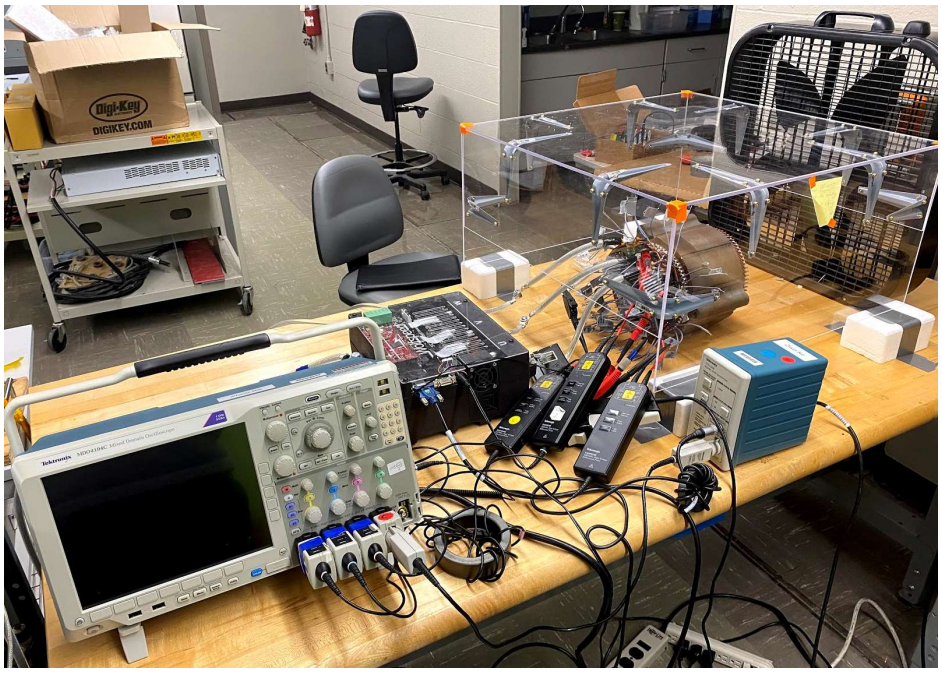

Figure 12. Fully instrumented three-phase test setup

2.4 Measurement and Data Logging

Voltage measurements were taken using THDP0200 high voltage differential probes from Tektronix. The probes have a bandwidth of 200 MHz and a maximum voltage of ±1.5 kV. Current measurements were recorded with a TCP404XL current probe with a 750 A DC current limit passing through a TCPA400 amplifier. All probes were connected to an MDO4104C oscilloscope with a bandwidth of 1 GHz and a maximum sampling rate of 5 GS/s. Voltage and current probes along with the oscilloscope are depicted in Figures 11 and 12.

For each winding test point along the selected parallel paths, four waveforms were simultaneously recorded using the scope (the maximum number of channels available). Each channel is described in Table 1.

Table 1. Four channel descriptions for each measurement point during testing

Channel	Description
1	Voltage between Phase U lead of the stator and the negative DC bus terminal at the inverter.
2	Voltage between a secondary phase lead of the stator and the negative DC bus terminal at the inverter. The choice of secondary channel is selected to capture the phase in which the winding measurement point is located. For points in Phase U, the secondary channel was arbitrarily selected as Phase V since Phase U is already captured in Channel 1. For Phase V, the secondary channel was Phase V. For Phase W, the secondary channel was Phase W.
3	Voltage between the measurement point lead wire and the neutral bus lead cable.
4	Line current of the phase in which the winding measurement point is located.

The horizontal window size was set to capture one fundamental switching period and was triggered off the current waveform in Channel 4. The data was exported from the oscilloscope and plotted using MATLAB. An example of one recorded set of waveforms from one testing point is shown in Figure 13; the excitation provided by the inverter was using a DC bus voltage of 800 V, switching frequency of 10 kHz, fundamental frequency of 1 kHz, and modulation index of 0.4. The point measured during this test was 24p, which is the end of the 24^{th} and closest turn to the phase lead in one parallel path of Phase U. Since the end of this turn is separated from the Phase U lead only by a couple centimeters, the waveform in this case is virtually identical to a measurement between the phase lead and neutral bus.

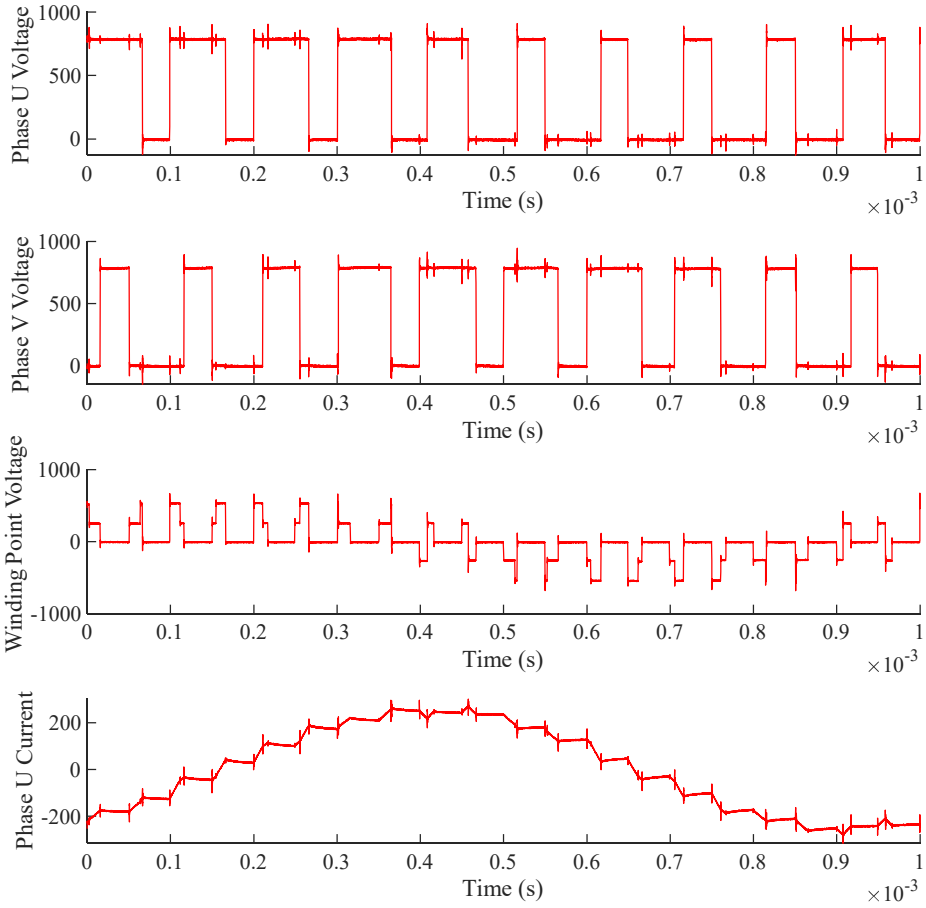

Figure 13. An example set of recorded waveforms for one test point, 24p

2.5 Effect of Control Parameters on Measurements

One of the desired outputs from this study is to understand the voltage stresses at high bus voltages and rapid switching times enabled by SiC MOSFETs. As such, the focus of the analysis to follow will be largely based on measurements recorded at 800 V DC bus, 10 kHz switching frequency, 1 kHz fundamental frequency, and 0.4 modulation index. The relatively low switching frequency was selected compared to a higher and more typical frequency of 20+ kHz to separate each switching event far enough away from each other that the amount of interfering transient times is reduced. A sample set of measurements from the same testing points as in Figure 13 at 20 kHz switching frequency are shown in Figure 14.

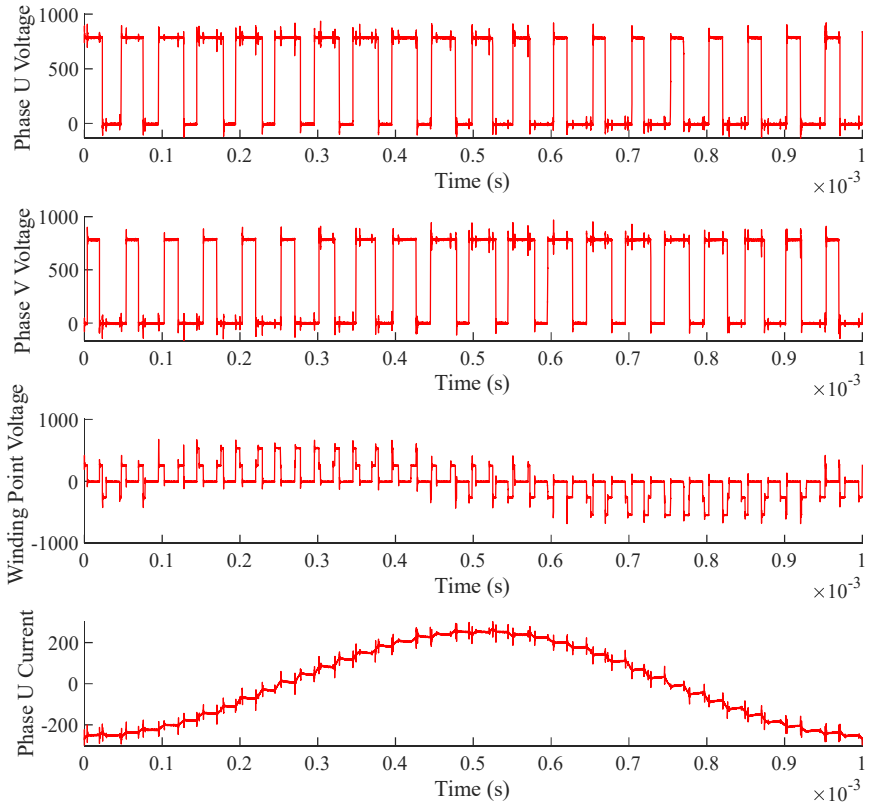

Figure 14. Measured waveforms for point 24p at 20 kHz switching frequency

A transient period follows each switching event under typical inverter operation. Following switch activation, the line voltage will overshoot the positive bus voltage (in an H-bridge) after a rising edge or undershoot the negative bus voltage following a falling edge. The additional harmonics observed after the rising/falling edge is referred to as "ringing." The magnitude and duration of the transient ringing that occurs after each switching event is dependent on many parameters, including stray capacitances in the stator windings, and resistance and inductance of the windings. An example of ringing being observed after a switching event is shown in Figure 15. While holding these

machine parameters constant, the amplitude and duration of this ringing is also determined by adjusting the inverter parameters such as bus voltage, switching frequency and modulation index.

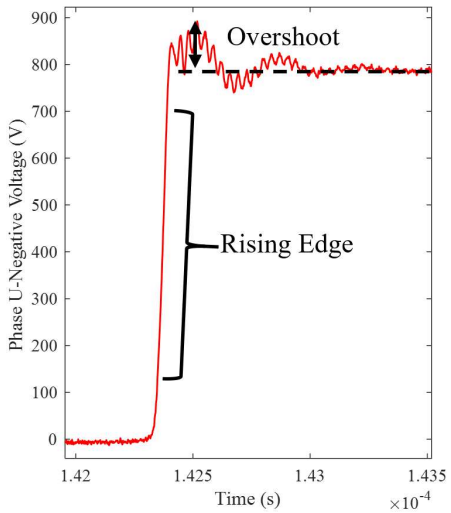

Figure 15. Voltage overshoot and ringing following a rising edge at the stator Phase U lead

To evaluate the impact of varying the bus voltage, switching frequency and modulation index on the switching characteristics of the inverter, a series of tests were performed to measure switching speed and overshoot/undershoot above/below the steady-state bus voltage. For one series of tests, the bus voltage was varied between 200, 400, 600 and 800 V DC while holding switching frequency, fundamental frequency, and modulation frequency constant. At 400 and 800 V DC bus, additional waveforms were recorded at 20 kHz switching frequency, and at 400 and 600 V DC bus, more were recorded at higher modulation indexes to maintain the AC current level at the same current level as the 800

V tests at 0.4 modulation index. At 600 V, this meant a modulation index of 0.53, and at 400 V 0.8. The results of these tests are tabulated in Table 2. Each given measurement is the average of five random rising/falling edges within the recorded waveform. The normalized percentage in the rising and falling edge columns equates to the error in the maximum value for the rising edge case over the positive DC bus voltage and the error in the minimum value for the falling edge case below the negative DC bus voltage, respectively. The fastest switching speed observed during testing was 13.52 kV/μs at a bus voltage of 800 V DC, with a switching frequency of 20 kHz. Switching speeds were observed during testing to be higher than the values provided in Table 2 without the stator windings connected. The inductance of the windings decreases the observed rising and falling times when connected to the inverter. The maximum normalized voltage overshoot for the rising edges was 17.33% observed at 400 V DC bus and 20 kHz switching frequency; the maximum undershoot for the falling edges was 17.20% observed at 200 V DC bus, 10 kHz switching frequency.

Table 2. Switching speed and voltage overshoot/undershoot

			Rising Edge			Falling Edge		
Bus Voltage (V)	**Switching Frequency (kHz)**	**Modulation Index**	**Max value (V)**	**Normalized %**	**dV/dt (kV/μs)**	**Min value (V)**	**Normalized %**	**dV/dt (kV/μs)**
800	10	0.4	878.00	9.8%	13.16	-86.28	10.79%	-13.19
	20	0.4	886.13	10.77%	13.52	-100.81	12.60%	-13.37
600	10	0.4	681.86	13.64%	11.39	-78.81	13.13%	-11.80
	10	0.53	674.53	12.42%	11.56	-83.34	13.89%	-11.62
400	10	0.4	461.64	15.41%	6.27	-63.77	15.94%	-6.28
	10	0.8	459.41	14.85%	8.52	-65.07	16.27%	-8.66
	20	0.4	469.31	17.33%	6.60	-68.11	17.03%	-7.36
200	10	0.4	232.70	16.35%	3.52	-34.39	17.20%	-3.36

The trend observed in voltage peak overshoot/undershoot against bus voltage is plotted in Figure 16 for measurements with 10 kHz switching frequency and 0.4 modulation index. As the bus voltage was increased, the normalized magnitude of both overshoot and undershoot decreased exponentially with a coefficient of determination (R^2) of 0.9967, indicating high correlation to the plotted black regression line. The equation for the regression line is also provided in Figure 16.

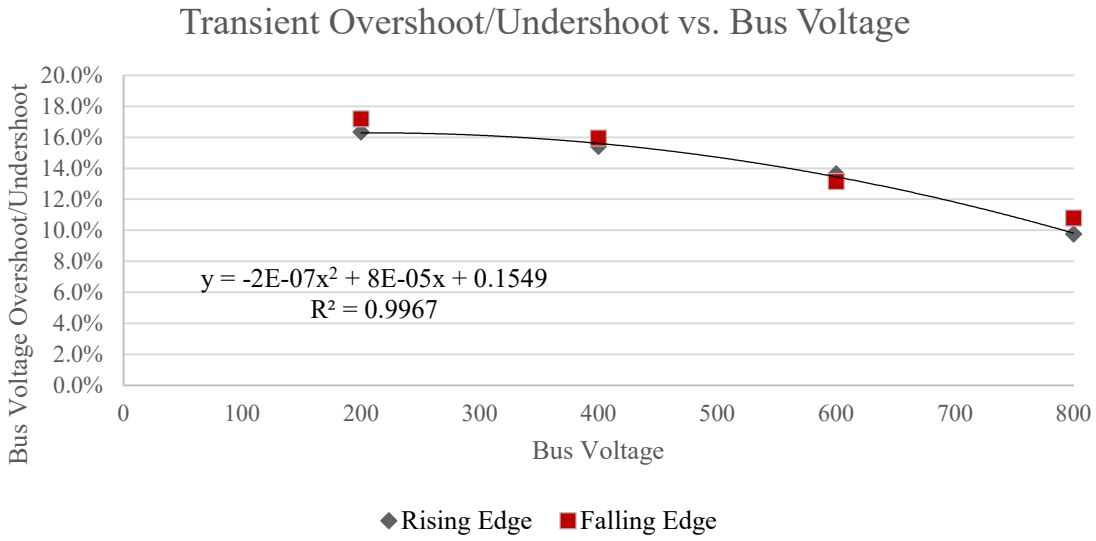

Figure 16. Transient overshoot/undershoot for various bus voltage levels, measured at both rising and falling edges of the Phase U voltage waveform with respect to the negative inverter DC bus terminal

While operating at 800 V DC bus provides the lowest amount of relative normalized overshoot, this does not conclude that it should stress the winding insulation the least. The peak voltage seen at the phase lead occurs at 800 V DC bus, with an average value of 78 V over positive bus voltage, and -86.28 V under negative bus voltage at 10 kHz switching frequency during rising edge transients.

The trend in switching speed against bus voltage is plotted in Figure 17 for measurements with 10 kHz switching frequency and 0.4 modulation index. As the bus voltage was increased, switching speed increased linearly with a coefficient of determination (R^2) of

0.9841, indicating high correlation to the plotted black regression line. The equation for the regression line is also provided in Figure 17.

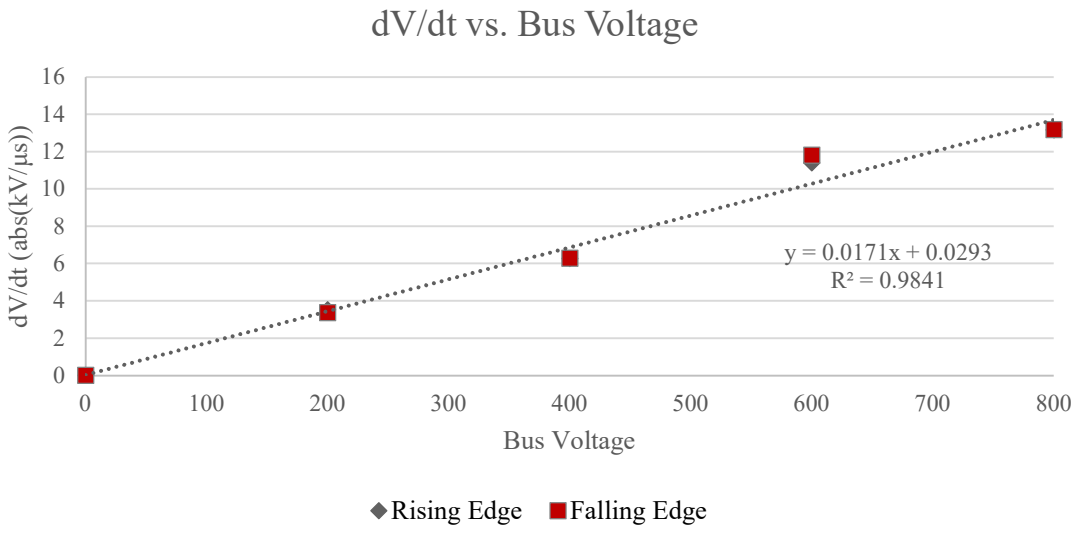

Figure 17. Switching speed as a function of bus voltage, measured at both rising and falling edges of the Phase U voltage waveform with respect to the negative inverter DC bus terminal

The result of plotting the overshoot/undershoot seen at the inverter phase lead against the switching speed is shown in Figure 18. The trend is that as the switching speed increases, the peak deviation from the intended voltage decreases with an exponential relationship. The R^2 value for the regression line is 0.9755, again indicating high correlation.

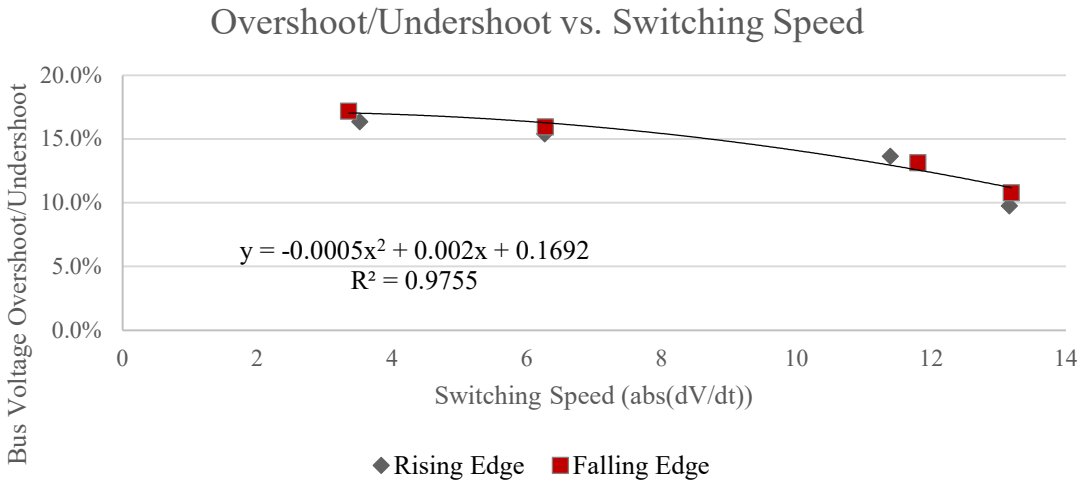

Figure 18. Plotting Overshoot/Undershoot as a function of switching speed, measured at both rising and falling edge of the Phase U voltage waveform with respect to the negative inverter DC bus terminal

Measurements taken at the same bus voltage with varying modulation indexes differed on average less than 1%, inferring that modulation index is insignificant on the voltage transient applied at the phase leads. Switching frequency does appear to slightly affect the voltage overshoots and switching speeds, but only slightly. Because of the small difference, the testing presented in the following sections will still use an excitation at 800 V DC bus, 0.4 modulation index and 10 kHz switching frequency to reduce overlap between transient periods which are close together as previously mentioned. This reasoning will be further demonstrated in the subsequent data processing section.

2.6 Data Aggregation and Processing

To calculate the voltage between two points within the stator windings at an instant in time, the recorded waveforms must be synchronized. The four waveforms recorded for each measurement point (corresponding to the four channels of the oscilloscope) are synchronized in time, but each set of four waveforms vary in time from measurement to measurement since the trigger point of the scope on the current waveform does not always trigger at precisely the same location. In other words, the current phase at which the recording of the single fundamental cycle starts in each data file varies from measurement set to measurement set. To remedy this, each set of four recorded waveforms for each measurement point was shifted through time in several different ways to ensure proper alignment, to simulate as if all measurements were recorded simultaneously at the desired instant in time.

First, the waveforms in each dataset were phase shifted so that the minimum current value observed throughout the fundamental period was then the starting point for the time scale. At this point, all waveforms within each phase were overlaid and checked for rough alignment. The minimum or maximum current value within a fundamental period does not always happen during the same switching state, and upon inspection of the collected data usually happens within a range of three switching pulses at a 10 kHz switching frequency with a fundamental frequency of 1 kHz. This means that each individual set of waveforms must be manually checked and potentially shifted in time by one switching pulse in either direction to realign the current waveforms, so they properly

lie on top of one another. This manual alignment process is prone to error, as the current waveforms can vary significantly in shape from period to period because of the slight timing errors present within the DSP control board and gate drivers.

As a check to ensure the correct amount of shifting, the Phase U lead waveform in Channel 1 of each measurement set was used as a secondary alignment. When the waveforms are properly aligned within one phase, the pulse trains from the first two channels should roughly align. If they do not align properly, the clear pattern of increasing and decreasing pulse widths throughout the fundamental period is not visible. When all three phases are aligned together, only Channel 1 can be used as a constant reference between measurement sets since it is the only waveform measurement location that is held constant. Shifting by visual reference when 72 waveforms are plotted on the same chart is difficult, so each phase was first individually corrected, and then a phase shift of $\pm 2\pi/3$ was added to shift the three phases apart with some minor adjustment to ensure all Phase U waveforms align again. The 24 sets of recorded measurements for Phase U are shown in Figure 19. The variation in the shape of the current waveform is visible in the thickness of the waveform band when all measurements are overlaid, even though the similarity in the switching waveforms for Phase U and V are apparent. Figure 20 shows all 72 measurement points, one from each of 24 turns of one parallel path of each phase, roughly aligned using this method. All Phase U waveforms are aligned well, while the second subplot representing the other phase lead measurement shows misalignment because the measured phase changes depending on the phase, as previously

mentioned. The red waveforms are measurement sets from Phase U, green are from Phase V sets, and blue are from Phase W. This coloring scheme is continuous throughout this paper.

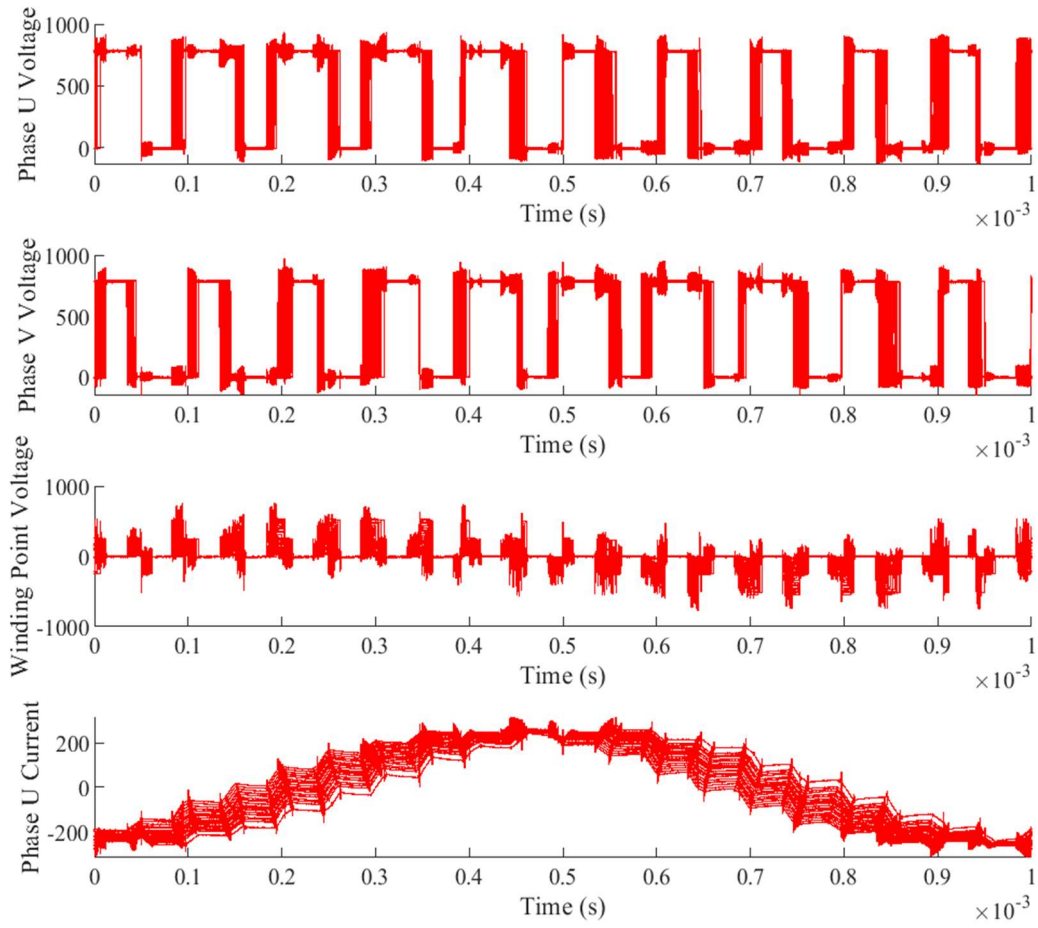

Figure 19. 24 sets of four channels of recorded data aligned to the minimum line current time index, with slight alignment correction

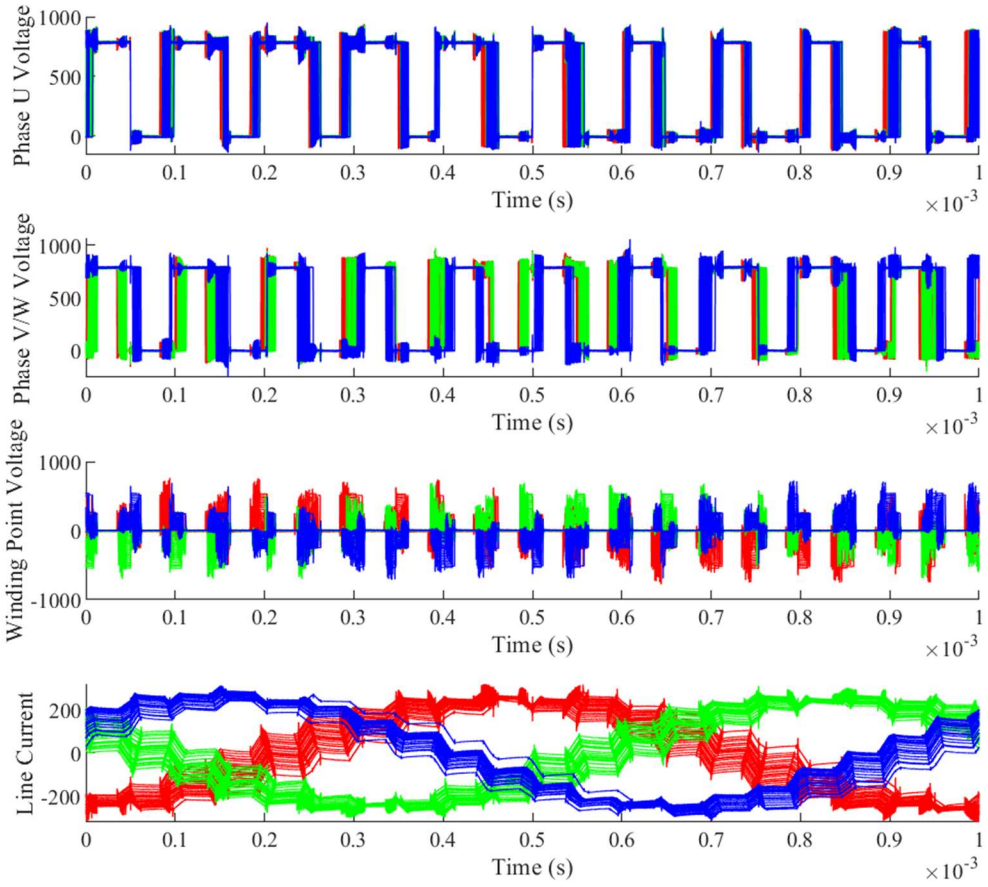

Figure 20. All 72 measurement sets of 4 channels for voltage stress analysis at 800 V DC bus, 10 kHz switching frequency, 1 kHz fundamental frequency, 0.4 modulation index

Though it appears all waveforms are aligned, additional fine tuning is necessary to ensure accuracy around the desired time for voltage stress calculation. Figure 21 shows a zoomed-in view of Channel 1 from Figure 20 around t=0.5ms. The misalignment between the pulse trains is apparent. To reiterate, to calculate voltage stresses at an instant in time, the waveforms need to be as aligned as possible to act as if all the measurements had been recorded at the same instant. The method to achieve this in this

study is, after achieving a rough alignment using the aforementioned methods, to precisely align all waveforms to a specific rising edge from one switching state in Phase U. In doing so, a region of high confidence in synchronization is created around the rising edges where the voltage stresses are expected to be the highest. Because of the variability in pulse widths between repeated fundamental periods caused by inherent error in switching timing, this confidence region cannot be extended to even the neighboring switching events in relation to the aligned edge.

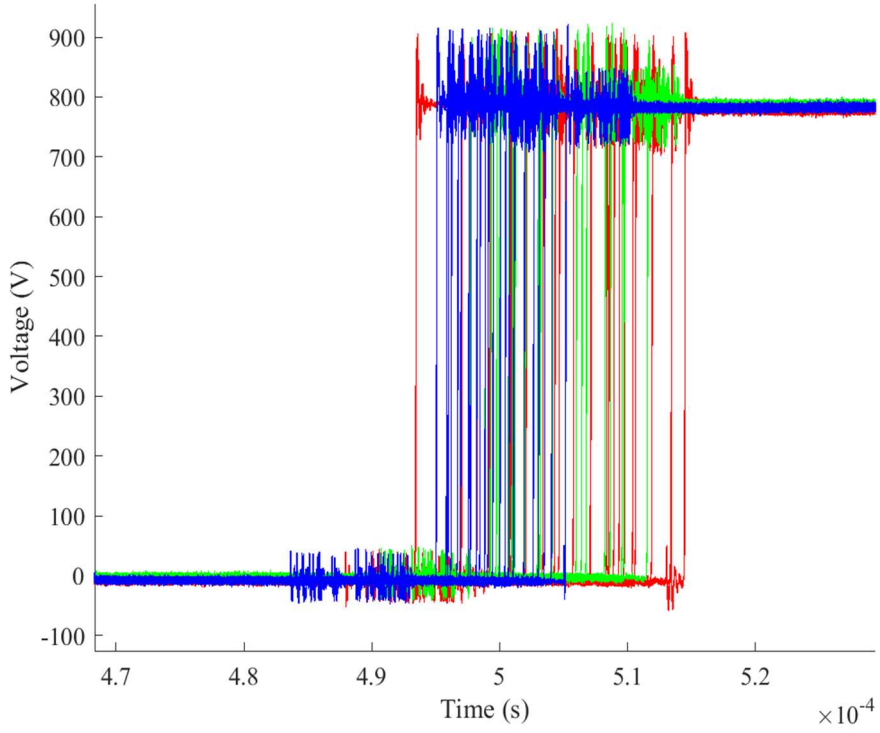

Figure 21. Small misalignment between Phase U measurements at the test lead after making rough alignments using the current waveform

To demonstrate how only one rising edge can be aligned across all measurement sets at one time because of timing error, Figure 22 shows all the Channel 1 measurements shown in Figure 20 which have been realigned to have the rising edge closest to t=0.5 ms be shifted to t=0.5 ms. Figure 23 shows a zoomed-in version of Figure 22; observing the proceeding and succeeding falling edges clearly demonstrates how misaligned the waveforms get even from one switching state to the next.

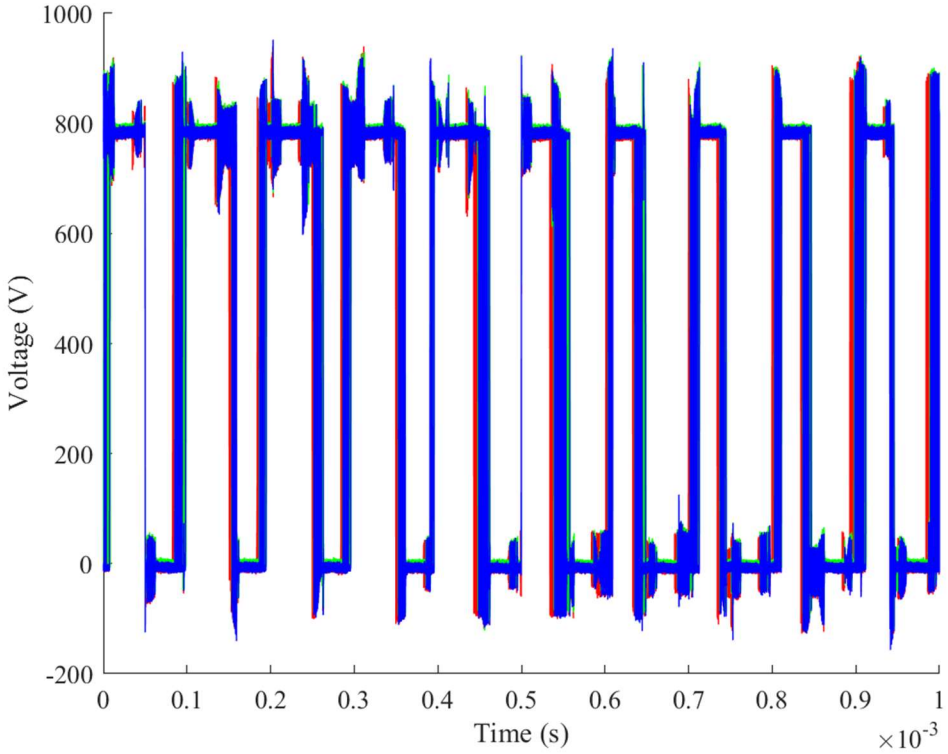

Figure 22. One fundamental period of Phase U measurements at the test lead as shown in Subplot 1 of Figure 20, realigned to t=0.5 ms

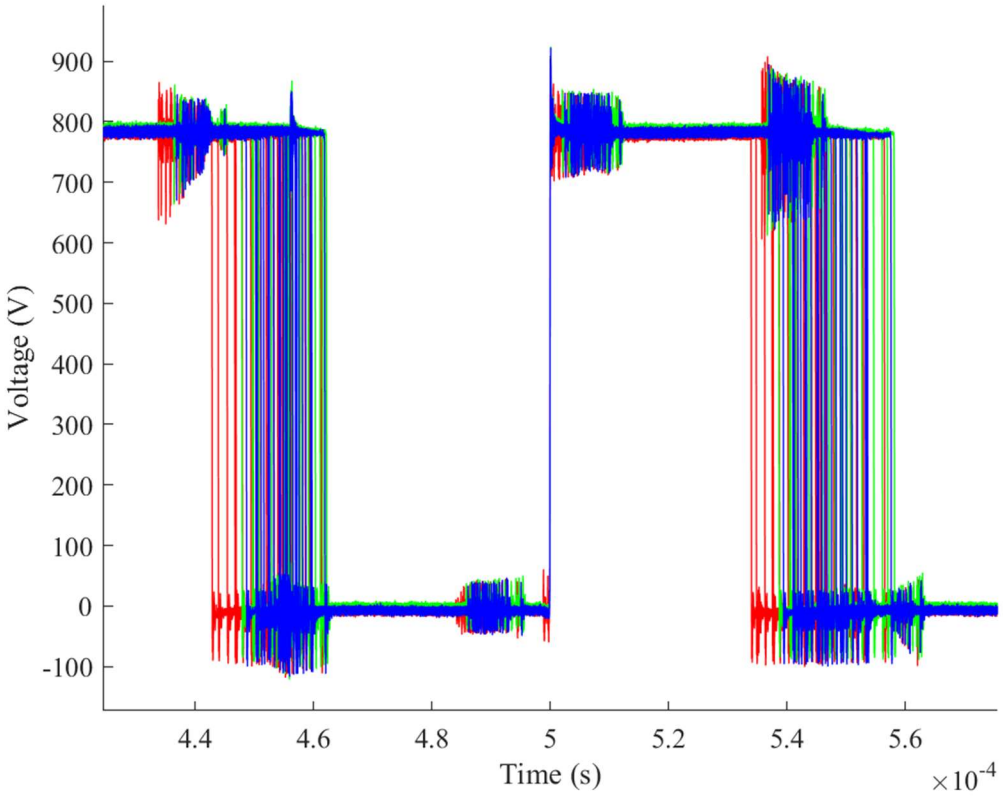

Figure 23. Zoomed-in view of waveforms aligned so that the rising edges closest to t=0.5 ms were shifted to t=0.5 ms, and the misalignment of neighboring falling edges

The impact of this alignment on the waveforms necessary to calculate voltage stresses, those recorded from the measurement points and presented in Channel 3 (third subplot) of Figure 20, is shown in Figures 24, 25 and 26. Both Figure 24 and 25 show the same zoomed-in view of the switching pulses around t=0.5ms. Figure 24 shows all measurement points before alignment, Figure 25 shows the same measurement points after realignment at t=0.5ms. Figure 26 shows an even closer view of the realigned transient ringing caused by the rising edge.

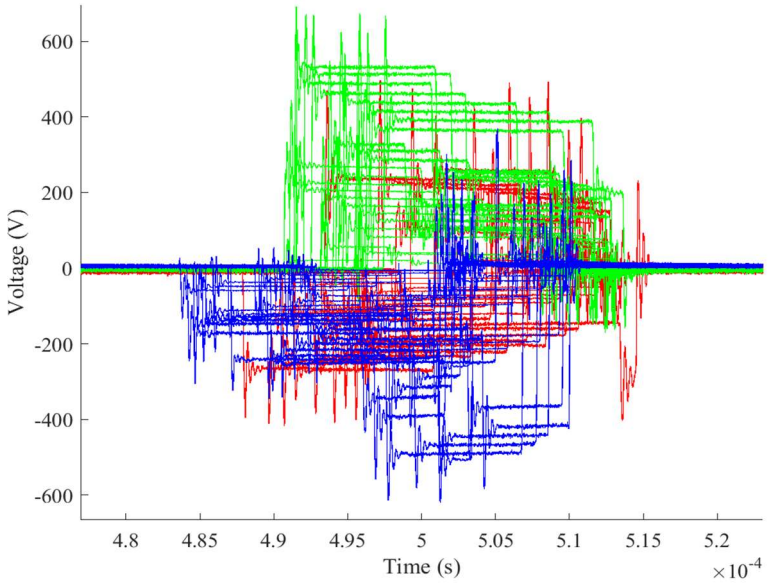

Figure 24. Three-phase measurement points before fine realignment

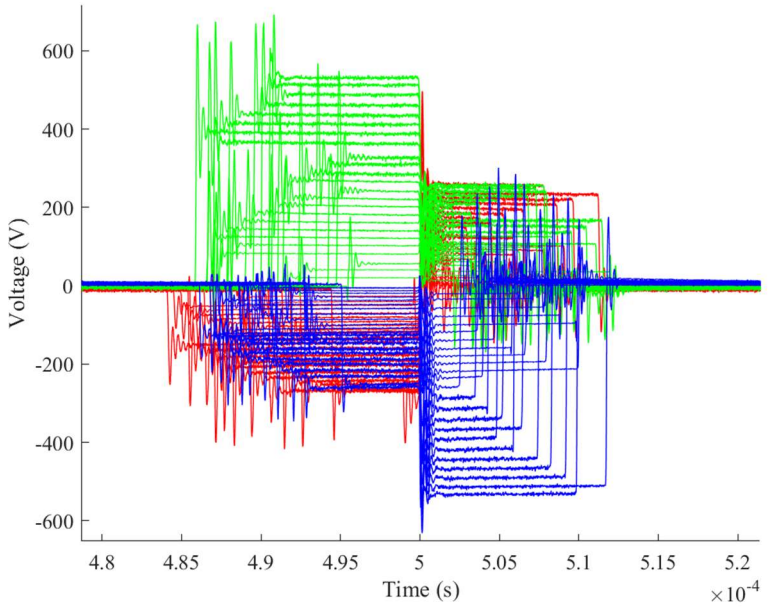

Figure 25. Three-phase measurement points after fine realignment to t=0.5ms

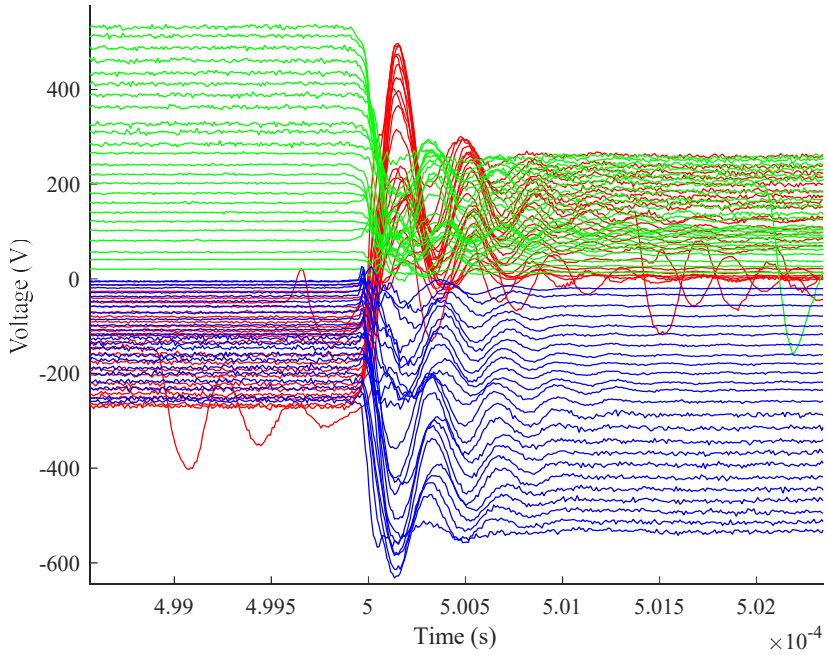

Figure 26. Close-up view of transient ringing caused by Phase U switching from inactive to active state after completely aligning waveforms in time

There are several waveforms in Figure 26 which see transient periods before and after the aligned transient region that are a result of the random switch timing error. In some instances, two switching events happen close enough in time that they start to overlap occasionally as instanced in Figure 26. As the time index is moved further away from the alignment time instant, these overlaps and random timing inconsistencies become more present, so a region of confidence was established and held constant throughout the rest of the analysis. The region of confidence amounts to 50 samples on either side of the alignment time; at a sampling rate of 100 MS/s, this equates to a window of 1 μs, centered at 0.5 ms in this instance. These interfering switching events are the primary

reason why the rest of this analysis was performed at a lower switching frequency of 10 kHz; higher switching frequencies push the pulses closer to each other which introduces more error into the voltage measurements even after alignment.

2.7 Calculating Voltage Stresses

The voltage at every test point can be extracted from any sample within the region of confidence around the selected rising or falling edge. Using these voltage values along with the winding diagram of the stator windings, the voltage stress between two adjacent conductors at a given time instance was determined. To understand how voltage stresses can be calculated between all six conductors in each slot while only measuring two, the machine winding layout will be revisited. Six layers of bar windings are stacked in each slot. The conductors in one slot lie only within one phase. All three parallel winding pathways of that one phase are represented twice within each slot if that slot is located within one of that phase's poles. For an example, the turn indexes passing through slot 30 are shown in Figure 27. On the left is the actual winding configuration per layer in that slot. The first turn of the first parallel path enters through Layer 1 closest to the rotor, makes it way around the stator and returns through Layer 6 at the 16^{th} turn. The first turn of the second parallel path enters at Layer 3 in slot 30, makes its way around the stator and passes again through Layer 4 at the 16^{th} turn. Likewise, the first turn of the third parallel path enters at Layer 5 and returns through Layer 2 at the 16^{th} turn. Thus, in this slot, the first and 16^{th} turns of each parallel path in Phase U are represented. Because of the balanced winding layout, the voltage distribution from turn to turn down each parallel

path should be roughly equivalent within a given phase. Slot 30 can then be equivalently represented by alternating the end of the 16th turn in parallel path 1 and the first turn of parallel path 1 to get the pattern shown on the right side of Figure 27. Now that every conductor within the slot is measured, the voltage stress between any two neighboring conductors can be calculated by taking the difference between their potentials.

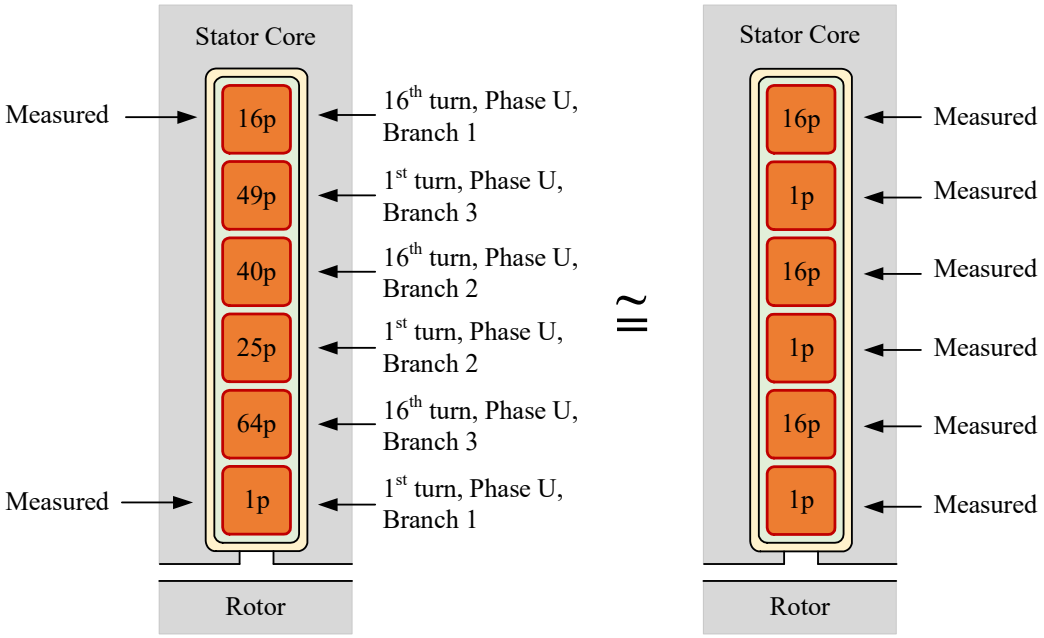

Figure 27. Left: slot 30 of the stator with the turn indexes of the winding passing through each layer. Right: slot 30 of the stator with the equivalent representation using the parallel path voltage distribution approximation

This pattern can be extended to any of the stator slots of this machine and allows for the calculation of the average voltage stress between two neighboring conductors at any instant in time along a given region of confidence. For example, for the waveforms

aligned in the previous section to t=0.5ms past the minimum current phase of Phase U, the average voltage stress at 13 samples (.13 μs) past the aligned rising edge is shown in Figure 28. Only the slot indexes in which the positive poles are located are plotted, since all the winding points selected were on the positive end of each winding coil. Slots with windings from Phase U are shown in red, Phase V are in green, and Phase W are in blue. The switching state change corresponding to this switching event is (010 → 110), where the first digit corresponds to the state of the Phase U top MOSFET and inversely the bottom MOSFET, the second digit corresponds to the state of the Phase V top MOSFET and inversely the bottom MOSFET, and likewise for Phase W.

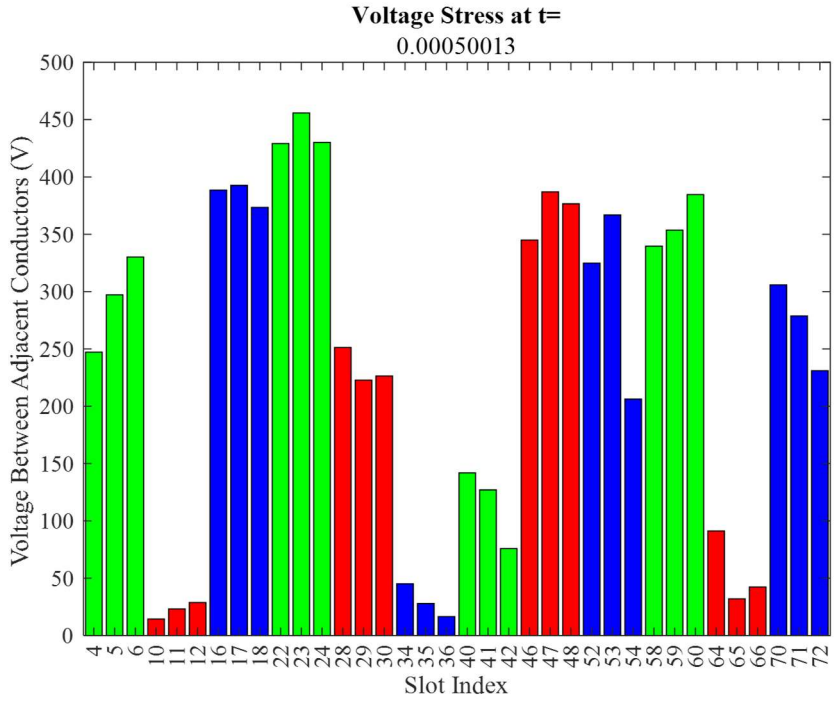

Figure 28. Maximum voltage stress by positive pole slot index near the peak overshoot from switching state (010 → 110)

To find the maximum voltage stress within the region of confidence near each switching event in Phase U, the voltage stresses were calculated iteratively through software from 50 samples (50 μs) before each rising/falling edge to 50 samples after each rising edge. The program identified 1) the time instant when the maximum voltage stress within one slot was observed and 2) the time instant when the maximum sum of all voltage stresses within all slots was observed. Often, these two times were either identical or very close to one another and occurred near the peak overshoot or undershoot times. The example stress measurement provided in Figure 28 is representative of this circumstance; the time index at which the stress is plotted here contains both the maximum voltage stress in a single slot and the maximum sum of voltage stresses in all slots.

The comprehensive set of voltage stress measurements along Phase U switching events is presented in Appendix A. For each switching event, a figure shows Channel 3 of Figure 20 zoomed-in on the corresponding measurement point waveforms after alignment. Also provided with each switching event is the calculated voltage stress for all slots at the time indexes of maximum voltage stress within a slot and when the maximum sum of all voltage stresses within the slots was observed. If these two times were the same, only one voltage stress figure is plotted. Next, the voltage across each turn at these instances in time are calculated by finding the difference in voltage between two neighboring measurement points along the stator windings. An example of a plot showing the turn voltages calculated at the same instance in time as Figure 29 is shown in Figure 29. Typical maximum turn voltages are less than 200 V.

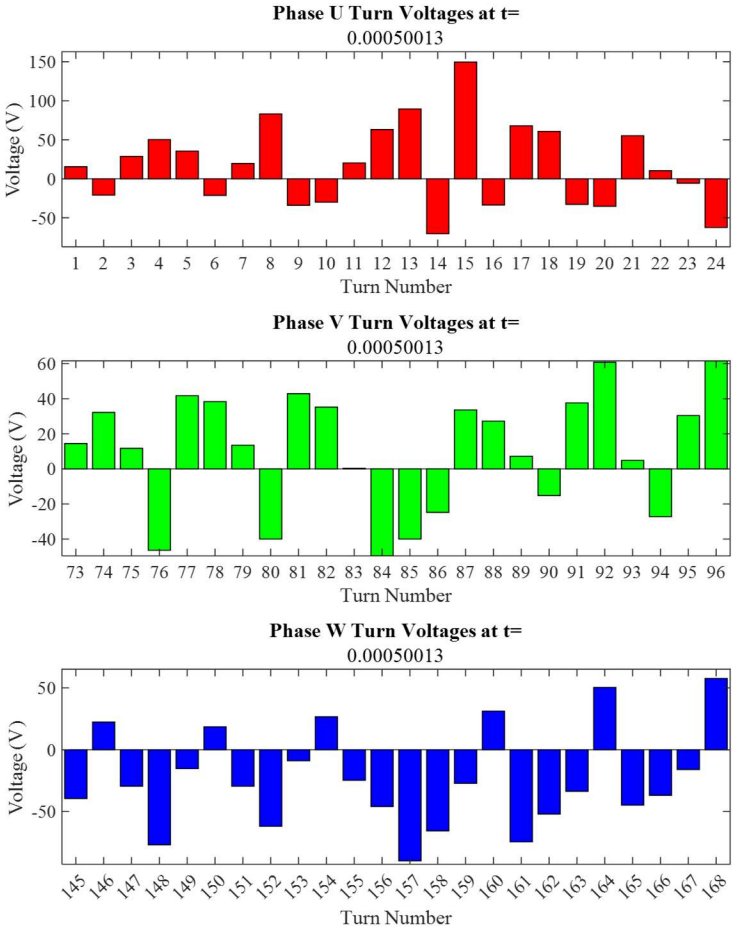

Figure 29. Three-phase turn voltages calculated during peak voltage stress timing around the t=0.5 ms switching event (010 → 110).

2.7 Parallel Pathway Testing and Verification

To validate the approximation in the voltage stress calculation of the turn voltages within the parallel winding paths of each phase being roughly equal at corresponding indexes within their branches, additional test points were added to the end windings on the crown side. One test point was added to two winding points on either side of a coil within each of the three parallel paths of each phase. The location of the test points on the end windings differs from the rest of the test points used in the voltage stress measurements in that they are the farthest away from the stator core, but this is necessary to gain access to the second parallel winding pathways which pass through the inner layers. The location of the points relative to the stator core is insignificant in this case as this test serves only to demonstrate the similarity in voltage waveforms and thereby turn voltages between pathways. Figure 30 shows the difference between the test points used for voltage stress measurement and the leads used for parallel path testing.

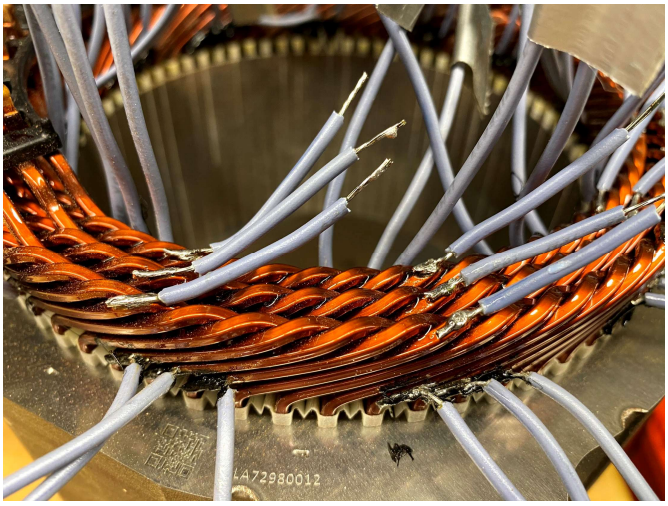

Figure 30. Parallel winding path test connections located on the bend in the coil near the middle of the image compared to the voltage stress testing points located near the bottom of the image closest to the stator core

Figure 31 shows the four monitored channels during the parallel path testing. All measurement points for this example are located within Phase U windings. Three turn voltages at the same index within each parallel path of Phase U were examined after measuring the positive and negative ends of each coil. The red and black traces in Figure 31 and Figure 32 correspond to the positive and negative sides of each parallel winding coil, respectively. The turns selected for measurement due to their accessibility from the top of the stator crown are as follows: Turn 3 (turn 3 of Phase U parallel path 1), Turn 27 (turn 3 of Phase U parallel path 2), and Turn 51 (turn 3 of Phase U parallel path 3).

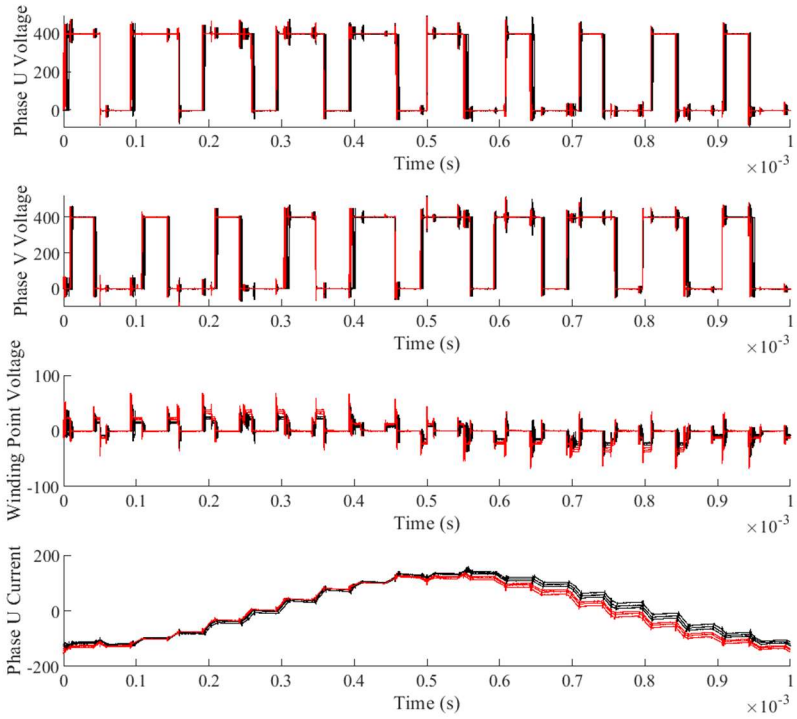

Figure 31. Four measured channels for parallel path testing. Red traces are recorded waveforms at a positive coil end, black traces are recorded waveforms at a negative coil end

Figure 32 shows a close-up view of the winding measurement point waveforms near the t=0.5 ms rising edge to which all waveforms were aligned. The red waveforms corresponding to the positive coil ends group together, and so do the black waveforms corresponding to the negative coil ends.

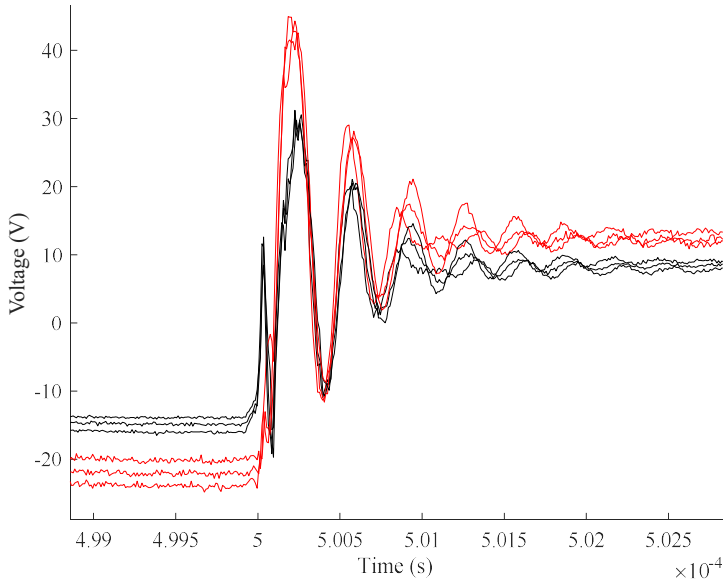

Figure 32. Measured voltages at the selected test points during parallel path testing, aligned to t=0.5 ms rising edge. Red traces are recorded waveforms at a positive coil end, black traces are recorded waveforms at a negative coil end

The turn voltages can be calculated in the same manner as during voltage stress measurements by finding the potential difference between the ends the coil. The turn voltage for each parallel turn is plotted in Figure 33. The similarity between these waveforms is demonstrated upon comparison. The average difference in voltage between each pair of parallel turns across the window shown in Figure 33 is tabulated in Table 3. These values are very small compared to the actual turn voltage and could possibly be due to probe error at such low voltages relative to their range of 150 V during this measurement.

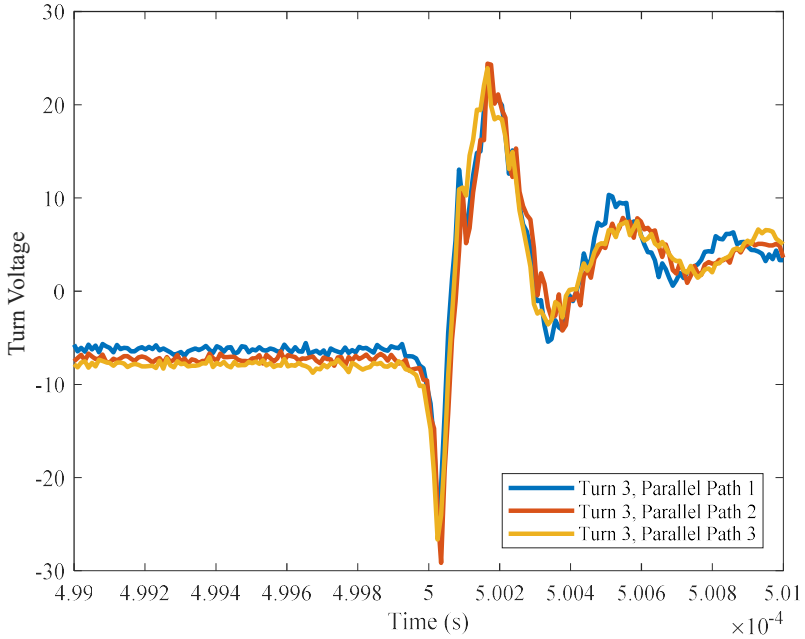

Figure 33. Turn voltages measured across the third turn of each parallel path in Phase U relative to the neutral bus

Table 3. Average difference between parallel turns within each pair of parallel paths

Turn Comparison	Mean Voltage Difference
Turn 3, Path 1 to Path 2	1.5278
Turn 3, Path 2 to Path 3	1.1921
Turn 3, Path 3 to Path 1	1.7503

Chapter 3. PDIV Testing

This section details the approach and results for evaluating PDIV of the Bolt stator. PDIV was observed under standard temperature and pressure (STP), as well as in a high-altitude low-pressure setting and a high temperature environment.

3.1 Partial Discharge Overview

Partial discharge (PD) is a phenomenon when an electrical discharge occurs across a surface or space but is not intense enough to result in a total breakdown event which would produce a self-sustained plasma arc. PD can occur between any two conductors when their potential difference is significant enough to occasionally short across the dielectric material between them. PD can take the form of corona discharge though a gaseous space, cavity discharge through a solid dielectric, or surface discharge along the solid's surface. At high enough voltage levels, these discharge events can be observed both visually and audibly without any instrumentation, however the inception of partial discharge events occurs at lower voltages than can be detected in such a manner and thus require additional measurement devices. PD pulses occur at high frequencies and attenuate quickly since they are not self-sustaining events. This results in EM noise emissions that can be detected using antennas and RF equipment. Despite some PD events not being visually or audible observable, they result in gradual degradation of the

dielectric material and can eventually lead to total insulation failure. In the case of this study, PD events are most likely to occur either between the stator windings themselves or to the stator core which is grounded when situated in a vehicle.

The focus of this portion of the analysis is on the partial discharge inception voltage (PDIV), the voltage at which partial discharge EM noise emanating from the stator is first observed. Increasing the voltage beyond this level results in stronger and longer-lasting partial discharge events, causing increased insulation breakdown.

3.2 Test Setup

The PDIV test setup used in this experiment was developed by other graduate students and faculty at the Center for High Performance Power Electronics (CHPPE) at the Ohio State University. Previously used in several published research papers, the test setup is proven and well-documented [21-24]. A high voltage power supply powers a SiC switching device as controlled by a gate driver which applies a constant duty cycle PWM waveform to the sample under test. The MOSFET module is rated at 10 kV but has a low current limit, so a current limiting resistor is placed in series with the half bridge. Voltage at the output of the switching module is monitored with the same voltage probe model used in the voltage stress testing. The current is monitored with a high frequency current transformer. A Faraday cage encloses the sample under test to reduce external EM interference. An air-tight acrylic test chamber encloses the sample within the Faraday cage so that the ambient pressure can be adjusted. A high frequency antenna is placed

inside the Faraday cage but outside the pressure chamber to measure noise emissions from the sample. The electrical connections to the stator are made through sealed pass-through leads in the wall of the pressure chamber and Faraday cage. A schematic of the PDIV test setup is provided in Figure 34. Table 4 lists the specific instruments implemented in the test setup along with general operating parameters. Figure 35 shows the opened-up pressure chamber and Faraday cage surrounding the stator before a test. Figure 36 shows the power electronics located outside the cage as excited by the HVDC power supply outside of the image.

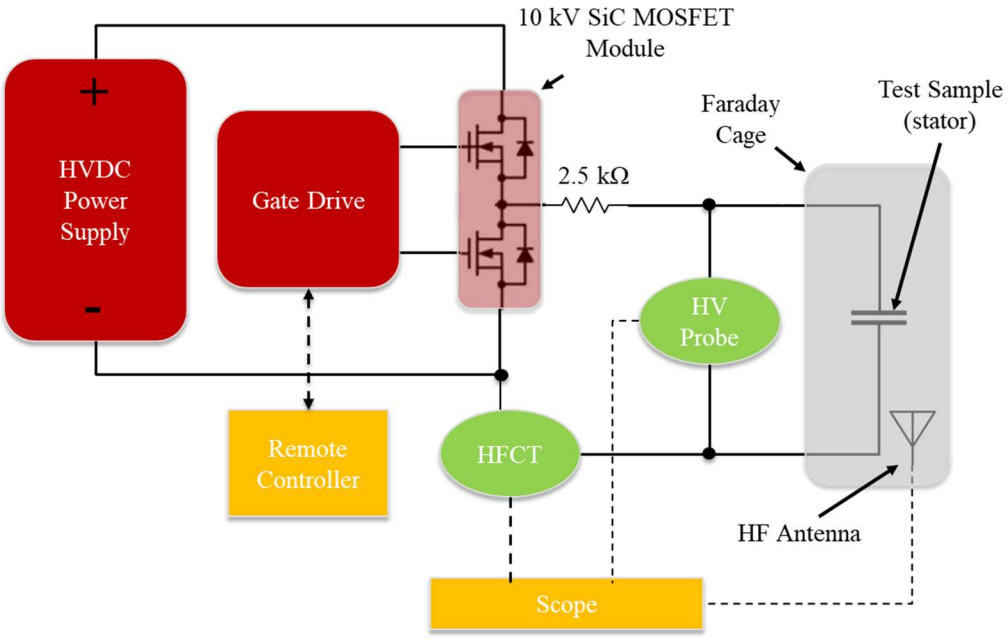

Figure 34. Complete PDIV test setup

Table 4. PDIV Power Electronics and Measurement Device Information

Equipment	Operating Description
Magna XR Series HVDC Power Supply	10 kV, 0.8 A DC, 8 kW
SiC MOSFET Half-Bridge	10 kV, >10 A, max slew rate of 130 kV/µs at 6 kV
Tektronix THDP0100	100 MHz bandwidth, 6 kV range
Pearson 2877 High Frequency Current Transformer	2.5 A_{RMS}, 300 Hz – 200 MHz bandwidth
RF Antenna	136 – 960 MHz connected to 500 MHz high-pass filter

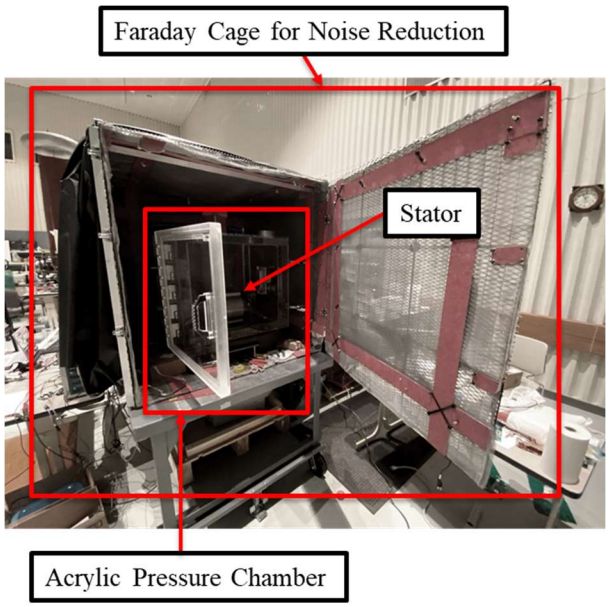

Figure 35. Faraday cage containing pressure chamber containing the sample under test

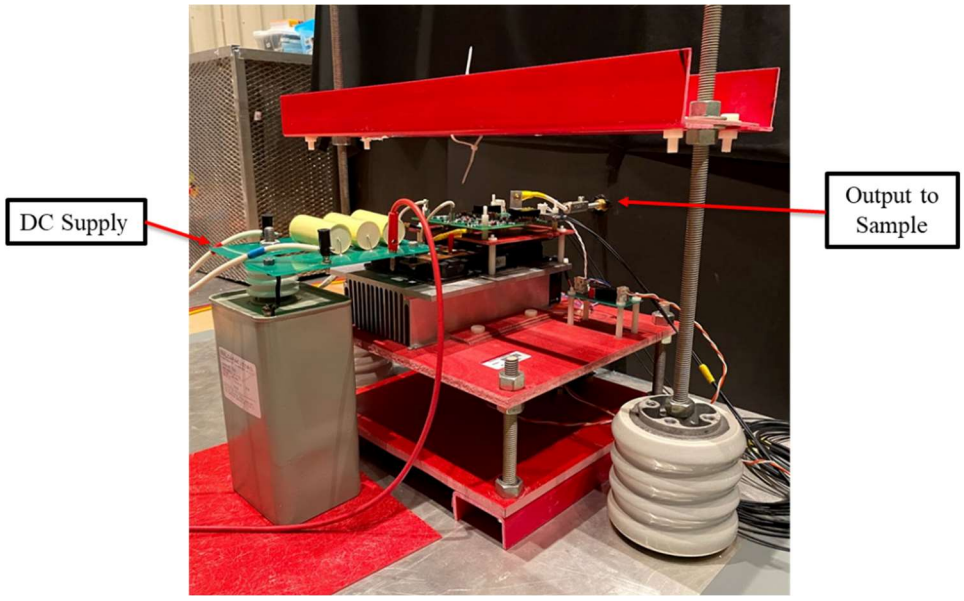

Figure 36. Power electronics including half-bridge SiC module and gate driver as fed from the HVDC power supply

The stator used in PDIV testing was a different stator than the one used for voltage stress testing and had not been damaged to add measurement points, which would otherwise create suitable points for charge buildup. The voltage was applied to the stator windings in this test procedure with the positive voltage lead (connected to the middle leg of the half-bridge) connected to one phase lead, and the negative voltage lead connected to the exterior of the stator core. Applying the voltage from the windings to the stator core was chosen over phase-to-phase excitation for several reasons. First, because of the current limitations of the power electronics driving the voltage. Since the machine is wye-connected, applying a voltage between two phases would result in a high current as observed in the voltage stress testing. Second, it was desirable for this experiment to

produce and observe PD in the most likely scenario, which is between conductors that are the closest together. The conductors that are closest together in this stator design are neighboring winding layers within a slot, as well as the stator core slot wall to the windings within the slot. Phase-phase PD is only potentially likely to happen at the end windings and connection points on the crown side of the stator since two phases never mix within any slot. Insulation degradation is still possible and detrimental at the end windings, but the voltage stresses within the slots themselves are the focus of this study.

The half-bridge driver was selected for use instead of the CREE inverter because the voltage rating of the CREE inverter was not expected to be high enough to observe consistent PD, and the current demand is low due to the lack of a conductive current path between the stator and windings.

The left image in Figure 38 shows the instrumented stator inside the PDIV test chamber. The positive connection at the phase lead is surrounded by insulating tape to reduce any noise potentially emanating from the sharp edges of the bolt securing the wire to the lead. The negative/reference ground connection was made to the exterior of the stator wall using conductive copper tape. A probe was placed inside the test chamber that recorded temperature, pressure and humidity and was used to ensure consistency between test trials.

The right image in Figure 37 shows the sealed pass-through connections of the wires into the chamber, as well as the antenna used to detect RF emissions from PD.

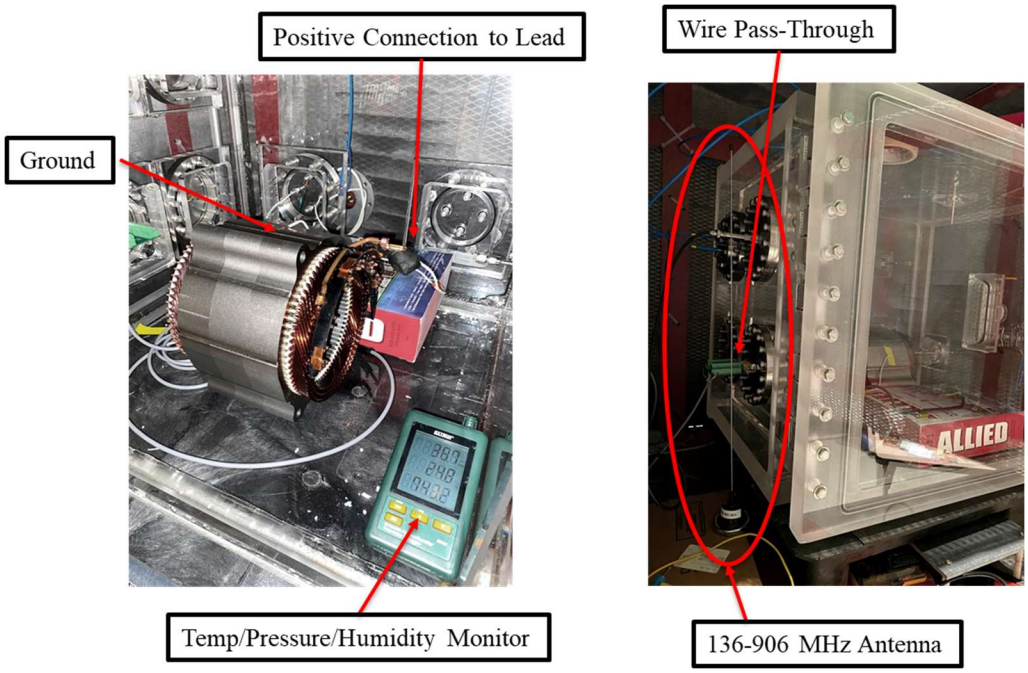

Figure 37. Instrumented stator inside the pressure chamber (left), measurement antenna inside the Faraday cage (right)

3.3 Procedure and Testing Results

Three waveforms were recorded during each test: the excitation voltage from the differential probe, the line current from the HFCT, and the induced voltage of the antenna. The voltage applied was a constant width square wave at 10 kHz switching frequency. The switching speed at this voltage range is slower than the output from the

CREE inverter at this voltage level, at around 2.4 kV/μs at 1.15 kV with the stator attached.

The general test procedure for each of the test series follows the standard set by IEC 60270 [21-24]. The voltage was gradually ramped up until PD noise was observed at the antenna trace on the oscilloscope. Once PD was observed, the voltage was set to zero followed by a waiting period of at least 5 minutes to allow the built-up charges on the conductors to dissipate. The time in between test trials has a significant impact on the observed PDIV [21-24], so the repetitions were done as close to five minutes apart as possible. Each series of tests to follow was composed of five sequential trials.

Figure 38 shows the three measurement channels from the oscilloscope: the black trace is the applied voltage, the blue trace is the current waveform, and green is the antenna voltage. Two PD events are observed in this window; the noisy pulses located at the same time as the maximum current amplitude is observed is indicative of a partial discharge event.

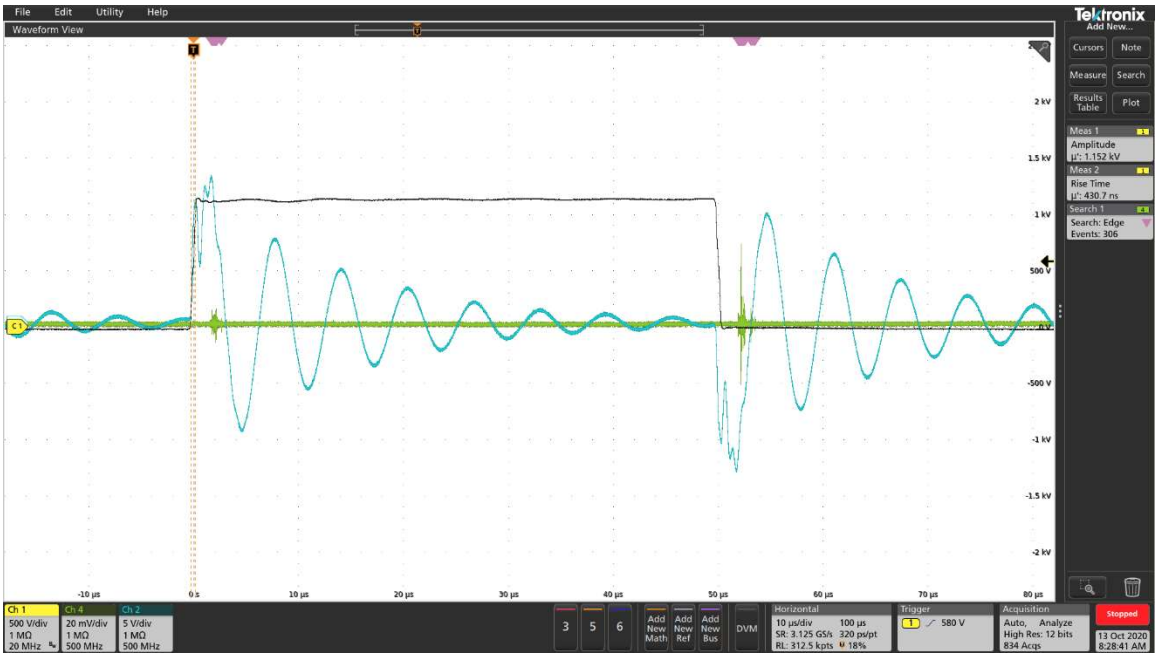

Figure 38. Channels monitored by the oscilloscope during testing with apparent PD in the green antenna trace near switching events

Variability in PDIV under identical test conditions is observed in Figure 39. A total of 15 measurements were recorded in this plot: five trials for each winding phase at room temperature and standard pressure (average of 760 Torr). There is not an apparent trend visible between PDIV and the phase under excitation. The mean and standard deviation of these test are recorded in Table 5.

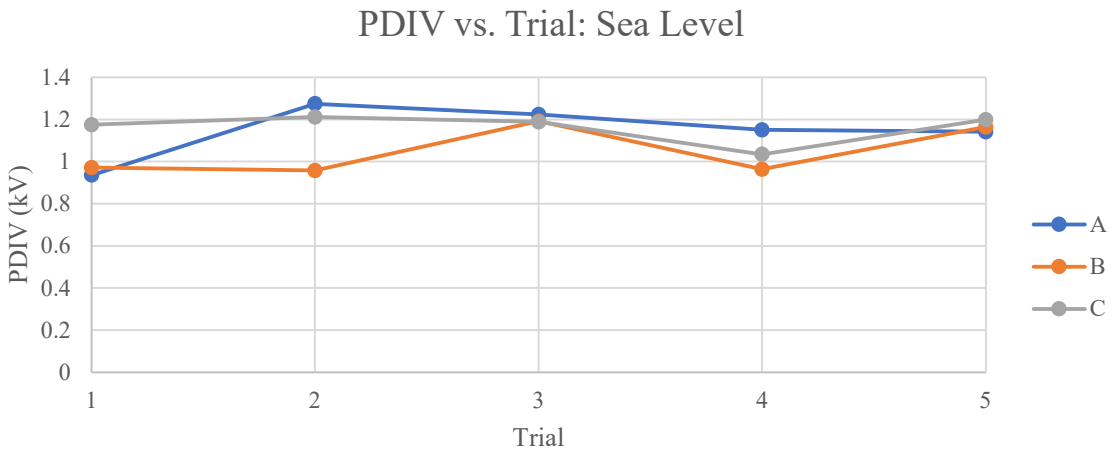

Figure 39. Observed PDIV per phase at each of five trials at STP

Table 5. Mean and standard deviation of PDIV measurements for each phase at standard temperature and pressure

Phase	Mean	Standard Deviation
U	1,145 V	129.29 V
V	1,050 V	117.48 V
W	1,162 V	72.32 V

The variability continues to be demonstrated in Figure 40, which plots observed PDIV per phase for five trials each at a reduction in ambient pressure of 25%. This corresponds to an elevation of 8000 feet, or an average of 570 Torr. Again, there is not an apparent trend visible between PDIV and the phase under excitation. The mean and standard deviation of these test are recorded in Table 6.

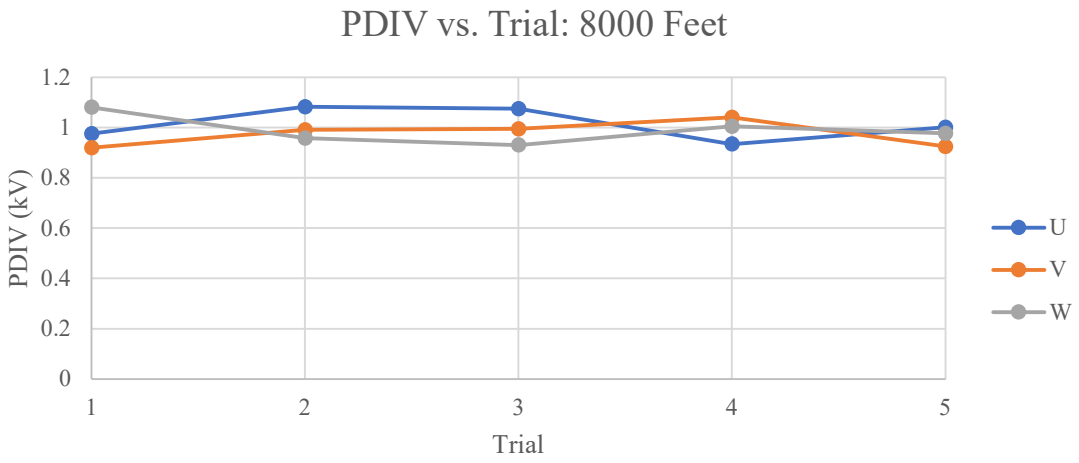

Figure 40. Observed PDIV per phase at each of five trials at 25% reduced pressure

Table 6. Mean and standard deviation of PDIV measurements for each phase at standard temperature and reduced pressure

Phase	Mean	Standard Deviation
U	1,014 V	64.98 V
V	1,975 V	51.27 V
W	1,990 V	57.36 V

To observe the impact of reduced pressure on PDIV, the means are plotted per phase in Figure 41. On average across all phases, PDIV was lower by 11.3% after reducing the ambient pressure by 25%.

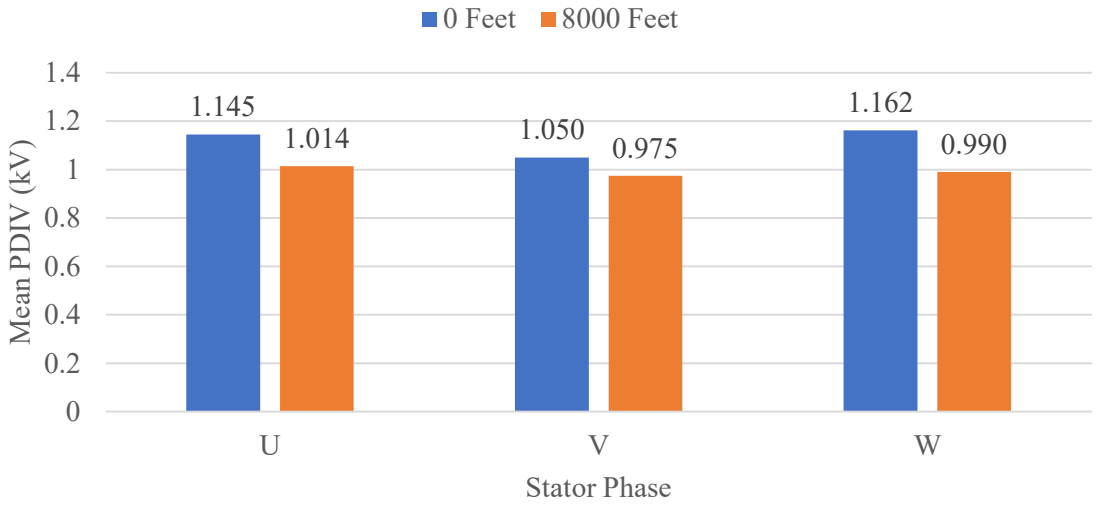

Figure 41. Comparison between average PDIV for each phase and pressure level

The effect of winding temperature on PDIV is demonstrated in Figure 42. To increase the winding temperature, the machine was excited using the CREE inverter until the average winding temperature increased to slightly above the desired temperature value. The leads were then reconnected to the half-bridge drive module and PDIV testing was performed. Since no correlation between stator winding phase and PDIV was observed in the previous experiment, only Phase U was analyzed for the study on winding temperature. The mean and standard deviation of the five trials is presented in Table 7. One interesting observation is that although the PDIV was reduced once winding temperature was increased from ambient temperature, there was not a significant difference between observed PDIV at higher winding temperatures. The operating temperature of the stator is

significantly higher than the temperatures tested in this experiment, but due to safety and handling concerns during test setup, the maximum temperature tested was 100° C.

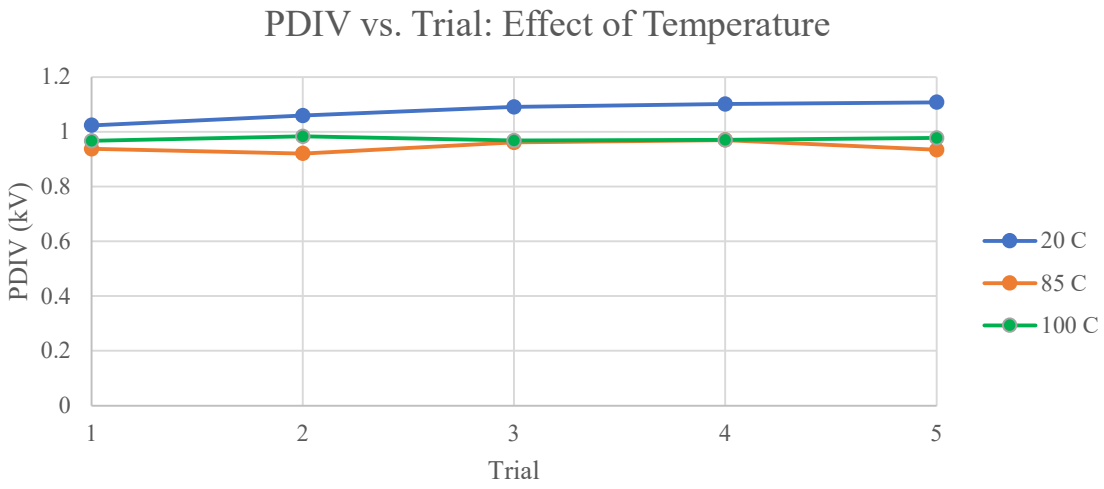

Figure 42. Observed PDIV per trial for varying winding temperatures, Phase U only

Table 7. Mean and standard deviation of PDIV measurements for each phase at standard pressure and varying winding temperature

Temperature	Mean	Standard Deviation
20° C	1,077 V	34.8 V
85° C	945 V	20.1 V
100° C	974 V	6.9 V

Chapter 4. 2D FEA Modeling and Simulation

While experimental testing is the most accurate method to determine the actual voltage stresses inside a stator, it remains desirable to develop a virtual model out of which voltage stress measurements can be extracted. This eliminates the need to measure each individual winding point manually, which is a time-consuming process. Such a simulation model was constructed in this chapter, the output of which is verified against the output of the experimental portion of this study for validation.

4.1 FE Modeling Approach

The electromagnetic simulation was constructed and calculated using ANSYS Maxwell, a powerful and efficient motor design and analysis tool. Maxwell contains a variety of solvers which can simulate different electromagnetic phenomena, including both static and transient electric and magnetic fields. The two solvers used in this study are the electrostatic solver and the magnetic transient solver, which were used to calculate capacitances and inductances of the machine windings, respectively. While Maxwell possesses 3D modeling capabilities, the simulation presented here was constructed in 2D to decrease simulation runtime. Previous analyses using the 2D approach have demonstrated its feasibility as an approximation to the full 3D model [1,2].

The order of operations from dimensioning the model to extracting voltage measurements is shown in Figure 43. Both solvers use the same 2D model, but with different inputs and outputs. The input for the electrostatic case is a DC voltage excitation to each conductor and produces a matrix output in the form of a capacitance matrix. The inputs and outputs for the magnetic case are variable depending on the scenario in question and will be described later.

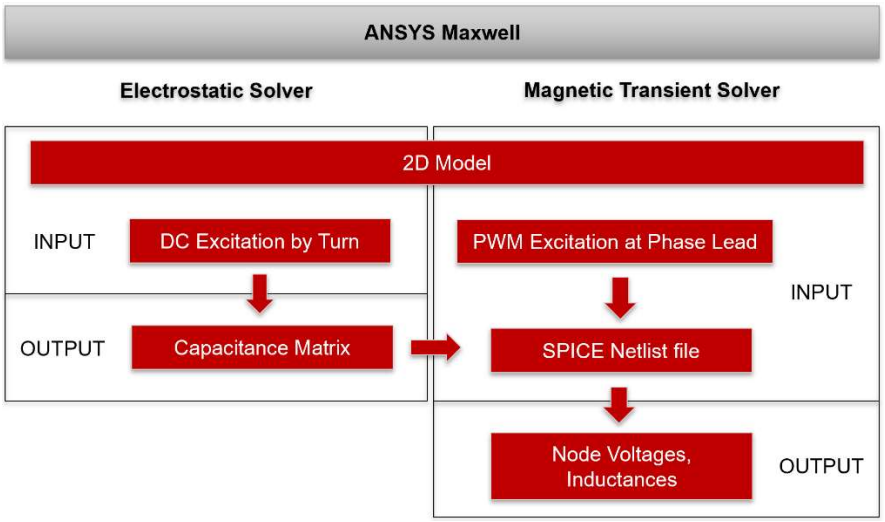

Figure 43. Simulation algorithm utilizing both electrostatic and magnetic transient solvers

The physical dimensions of the stator core and windings were provided by GM, which were used to construct the two-dimensional model shown in Figure 44. This cross-sectional view of the stator is shown as viewed from the crown side of the machine, which includes the phase output terminals and neutral bus, and is opposite the weld side of the machine where the hairpin windings are bonded together. The slot index starting

position was arbitrary (the 2D representation approximates the stator core with a spherical outer diameter, while it has actual bolt mounting ears to index off on the actual stator), with the indices increasing sequentially clockwise.

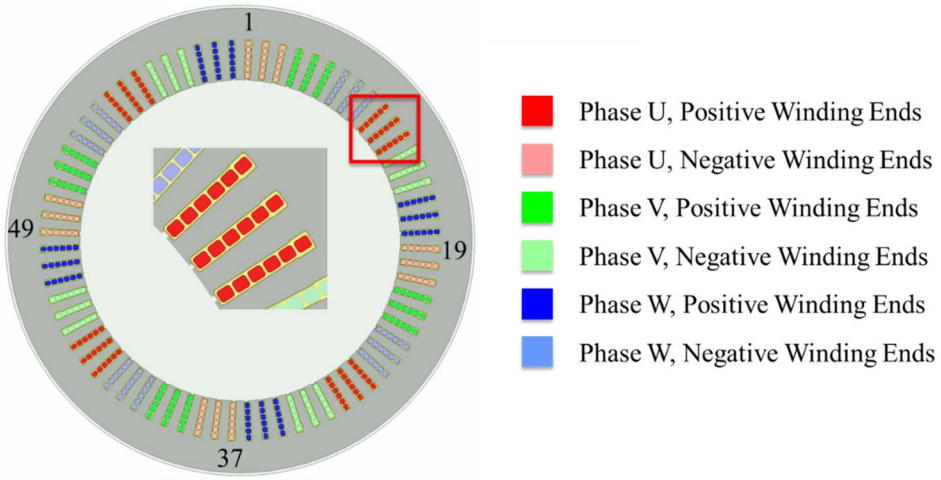

Figure 44. 2D stator cross section in ANSYS Maxwell, with a detail view of one positive pole of Phase U

In addition to the stator core and windings, additional components were incorporated into the model to closer represent the true construction. Slot liners were added surrounding the inside perimeter of each slot. The slot liners are composed of three individual layers: two 50 µm layers of aramid paper sandwiching a 100 µm layer of a polyamide/epoxy composite material. These materials and dimensions are based on the supplier datasheet for the actual material used in the Chevy Bolt stator. The proprietary dielectric properties of these materials were incorporated into the model material properties. Including the slot liners increased the self-capacitances (calculated later in this section) by approximately

20%, which increased the amplitude of the voltage ringing by 5%. Next, the varnish coating on each of the conductors was created, again using proprietary supplier data for the dielectric constants of the material. Finally, the airgap within the slots was filled with a material that represents the equivalent air-to-resin mixture that GM targets for the machine. After the hairpins are seated in the slots and welded together, the stator assembly is vacuum impregnated with this resin to provide additional insulation and thermal performance. GM sets a target ratio of air to resin within the slots which can be verified by weighing the assembly before and after impregnation. This ratio was used along with the dielectric constants for the material and air to represent a mixture of the two which fills the space around the conductors in each slot. The rotor and end windings are not included in this model. This approximation has still proven to produce accurate results for voltage stress measurements [1,2].

4.2 Solving for a Capacitance Matrix Using Electrostatics

ANSYS Maxwell performs analysis using Maxwell's equations. Gauss' law is applied in the electrostatic solver to calculate the capacitance between any two conductors in the model which contain an electric potential. The basic differential form of Gauss' law is given by (1).

$$\nabla \cdot D = \rho \tag{1}$$

$$\nabla \cdot \left(\varepsilon_r \varepsilon_o \nabla \phi(x, y)\right) = -\rho \tag{2}$$

The electric flux density D is calculated using the permittivity of the material and the 2D scalar potential vector ϕ, which are defined in the setup of the simulation model. The

differential equation that the electrostatic solver produces is given by (2) [8]. The boundary condition imposed on the model is a zero-potential balloon boundary surrounding the stator.

The 2D model is broken into a solvable discrete triangular mesh. The electrostatic solver is adaptive and automatically generates a mesh which is iteratively refined until the desired accuracy threshold is obtained. Parameters can be assigned to the electrostatic solver including force, torque, and the Maxwell capacitance matrix. Capacitances between two conductors are determined by relating the voltage across two conductors to the charge present on the conductors. Therefore, it is necessary to apply a voltage excitation to each conductor within the model to calculate the capacitances. Each pair of conductors corresponding to the positive and negative coil ends of each turn were excited with a 10 V, and the stator was excited with a 0 V excitation and designated as ground.

The general form of the capacitance matrix C is given in Figure 45. The subscript of each capacitance value corresponds to the two conductors across which it is calculated. Values in the matrix are given in units of picofarads per meter, so the output was multiplied by the stack length of the stator to obtain the lumped capacitance. Self-capacitances ($C_{1,1}$, $C_{2,2}$, …) were determined by adding the sum of one row or column to its element in the matrix diagonal. In the 2D model, each "conductor" represents one pair of winding ends so that the capacitance value is calculated as a lumped equivalent.

$$\begin{bmatrix} C_{1,1}+C_{1,2}+\cdots+C_{1,n} & -C_{1,2} & \cdots & -C_{1,n} \\ -C_{2,1} & C_{2,1}+C_{2,2}+\cdots+C_{2,n} & \cdots & -C_{2,n} \\ \vdots & \vdots & \ddots & \vdots \\ -C_{n,1} & -C_{n,2} & \cdots & C_{n,1}+C_{n,2}+\cdots+C_{n,n} \end{bmatrix}$$

Figure 45. Maxwell capacitance matrix general form

Since the simulation model approximates the machine construction with equal distances between conductors and identical positioning within each stator slot, the capacitances between conductors within each slot were all determined to be around 7 picofarads, while nearly all self-capacitances (between each conductor and "ground," identified as the stator core) were around 23 picofarads. All other capacitance values between conductors were orders of magnitude smaller and insignificant. The overall pattern of the three-phase capacitance matrix between winding turns in the GM stator is shown in Figure 46. Only the values of the capacitances which have a significant value (over 1 pF) are shaded black. The self-capacitances are largest and always significant and are visible as the diagonal line running from top left to bottom right. There are three clusters of other significant capacitances, which correspond to the mutual capacitances in each of the three winding phases. The subclusters within each phase cluster correspond to neighboring conductors within a given slot. If the windings are more than one or two layers away from another winding in a slot, their capacitances are insignificant based on this calculated matrix.

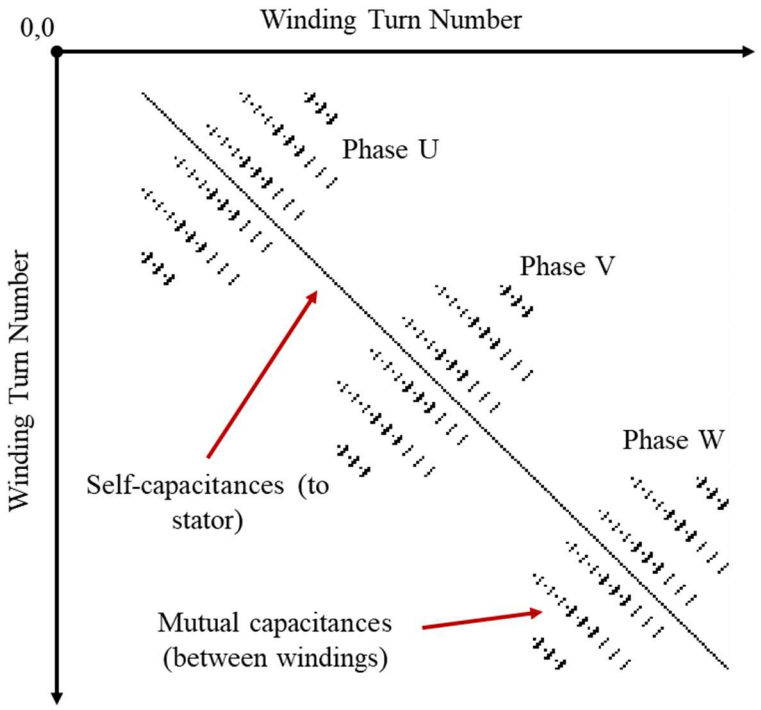

Figure 46. Three-phase capacitance matrix for the stator windings

4.3 Equivalent Circuit Representation of a Bar Wound Machine Winding

To construct an accurate time-varying magnetic simulation, the machine windings were connected in 24s3p series/parallel configuration for each phase according to the winding diagram provided by GM. Each turn in the machine has a resistance, inductance, and capacitance. The turn resistances were assumed to be equal due to the equal length of each hairpin and were determined using a resistance meter connected to the phase leads of the physical stator. The inductances of each turn were calculated after the magnetic transient case was simulated.

The magnetic transient solver can import an “external circuit” in the form of a netlist file, which is the same text-based circuit representation used by other electrical design tools based on the SPICE framework. ANSYS Maxwell has its own circuit editor which can be used to draw and design circuits through a user interface but is cumbersome to use for modeling a circuit with hundreds of elements. To automate the external circuit construction, MATLAB code was developed which imports data from .CSV files and writes its own Netlist file by connecting the appropriate resistors and capacitors to each winding in the simulation.

The winding resistances and capacitances were connected in circuit form according to the π-equivalent transmission line representation, which reduces the number of computational nodes as compared to the nominal T-equivalent and increases simulation speed [20]. Figure 47 shows the π-equivalent of a single turn n, where the capacitance is value is halved and placed on either side of the winding inductance and resistance. Additional capacitors were added to each turn in the same manner if significant mutual capacitances were present.

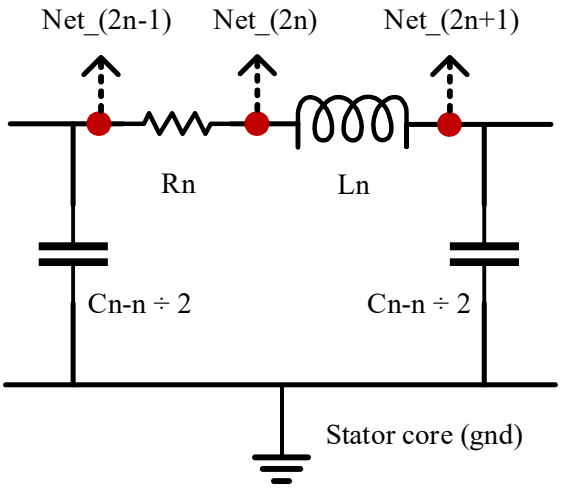

Figure 47. Π-equivalent lumped parameter equivalent of Turn "n" with naming convention for SPICE nodes

To better visualize how self-capacitances and mutual capacitances are connected between SPICE nodes, Figure 48 shows an example of the self and mutual capacitances for the first three turn indexes. The Net indexes are first assigned to connect the resistors and inductors according to the convention shown in Figure 48, and then capacitances are assigned in the π-equivalent form to each turn by connecting to the necessary Net indexes.

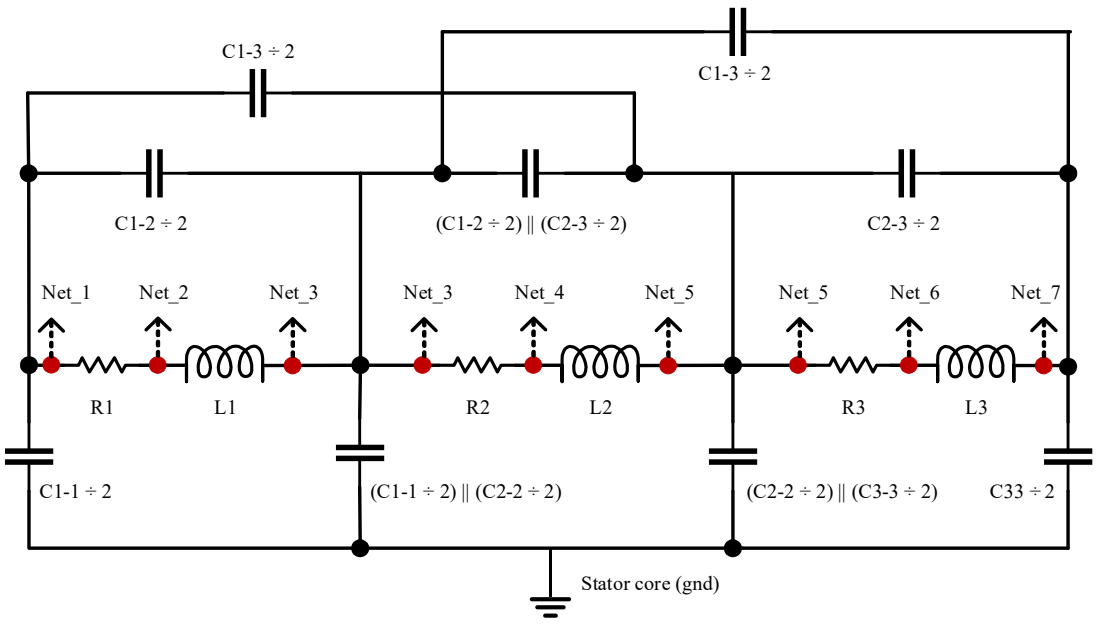

Figure 48. Three-turn example for connecting capacitances between SPICE nodes in the lumped-parameter circuit model for the winding turns

The MATLAB script automates these connections and neglects any capacitances smaller than 1 pF, which is too small for Maxwell to compute. Windings were excited in the magnetic transient case by applying a piecewise line-neutral voltage source in the same netlist file as the previous circuit elements. The source was connected from the phase lead to the neutral bus across all three parallel branches of 24 turns in each phase. The discrete data for this source was a line-neutral waveform recorded during voltage stress testing in Chapter 2.

4.4 Magnetic Transient Analysis

The magnetic transient solver produces a solution using all of Maxwell's equations [8]. The same boundary conditions and material properties were used as defined in the electrostatic case. Winding turns were created in the magnetic model by assigning pairs of conductors as the positive and negative turn ends. The netlist was imported and paired with the 2D model by naming these turns with the same name as used in the netlist. The magnetic solver does not possess adaptive meshing capabilities, so a custom mesh was imposed on each active element in the 2D model using Maxwell's mesh operations tool.

Design settings and parameters were defined before computing the solution to the magnetic transient case. The solution stop-time and time step were defined to match the input waveform included in the netlist. The stack length of the stator was incorporated by specifying its value in the model depth setting, which scaled the output accordingly. Instead of specifying parameters in the solution definition, voltage measurements points were defined in the external circuit netlist. Plots were created using these measurement points in the same manner that they were plotted using the measurement points added to the physical stator.

To evaluate the voltage stresses derived from the output of the transient solver relative to the observed voltage stresses during testing, the same excitation parameters were used as in Chapter 2. The line-neutral recorded waveform for excitation at 800 V DC bus, 10 kHz switching frequency, 1 kHz fundamental frequency and 0.4 modulation index is shown in

Figure 49. A zoomed-in version of this waveform around the t = 0.75 switching event of Phase U is shown in Figure 50. This event was selected as an example input because it had some of the lowest interference from other switching states after the initial rise time. The time index of the switching time shown in Figure 50 is not exactly t = 0.75 because this waveform was not shifted in time for alignment purposes; it is only one recording of a fundamental period.

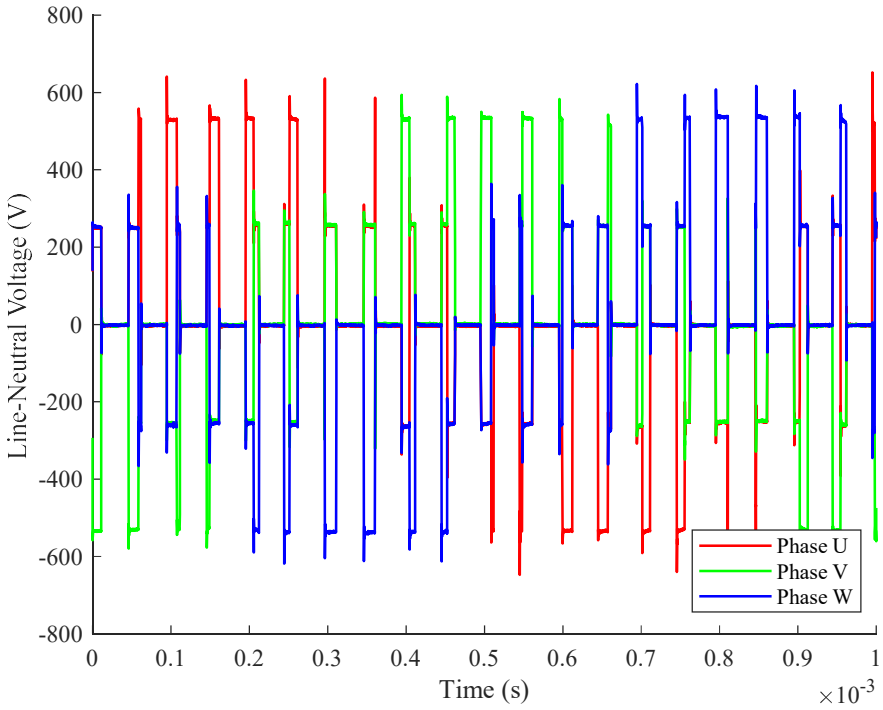

Figure 49. Line-neutral voltage waveform used for simulation input

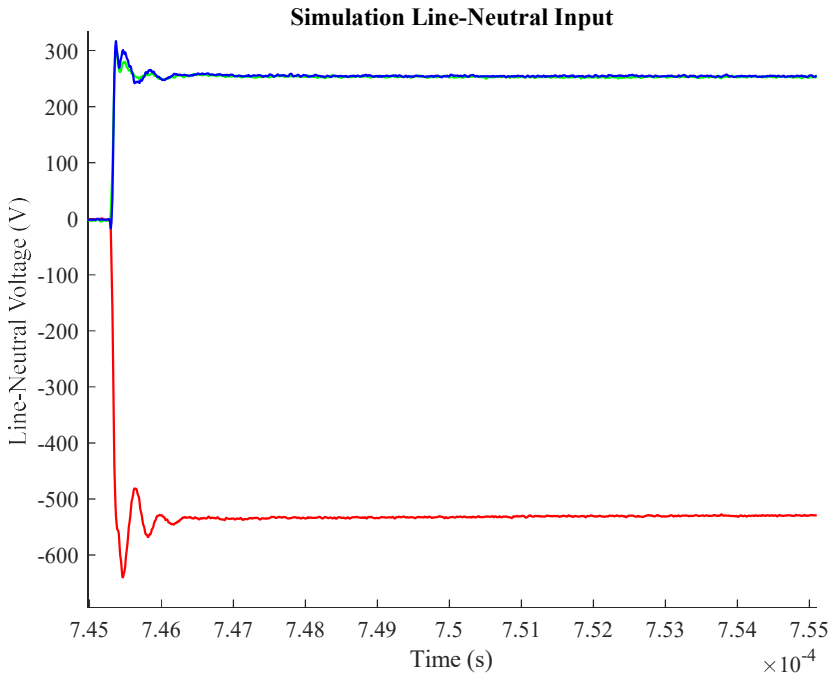

Figure 50. Close-up view of line-neutral three-phase input waveform near the 0.75 switching event

After running the simulation using the piece of the line-neutral input from Figure 50, the voltages across measurement points defined in the imported Netlist file can be extracted by plotting the induced voltages in each turn as calculated by the transient solver. The 24 turn voltages from one parallel path of each phase are plotted in Figure 51. Like the rest of the measurement plots in this paper, the red traces correspond to measurements in Phase U, green in Phase V and blue in Phase W.

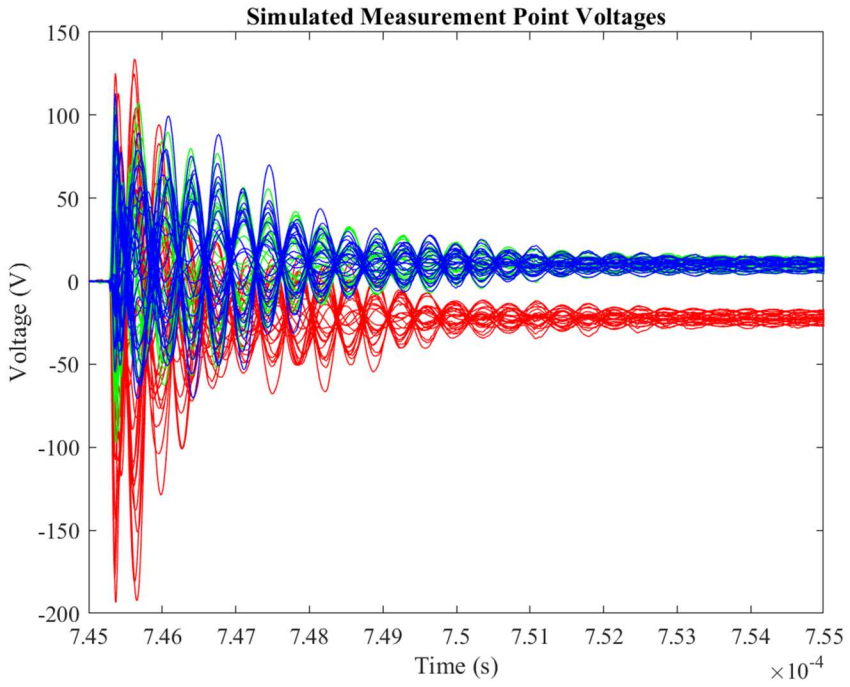

Figure 51. Simulated turn voltages from ANSYS Maxwell after one switching event

To extract the voltage at a given measurement point from this data, the turn voltages were summed together methodically to obtain the voltage at each measurement point. For example, the voltage at measurement point 3p is the sum of Turn 1, Turn 2 and Turn 3. The measurement point voltages for the same 72 measurement points added to the experimental stator are shown for the given excitation in Figure 52. The recorded waveforms during testing aligned to the same switching event are plotted in Figure 53. The time scales are shifted between the two figures because the time scale of the input waveform was different as previously mentioned. The transient ringing observed in the

simulated results persists longer than during testing, but there are distinct similarities between the two images.

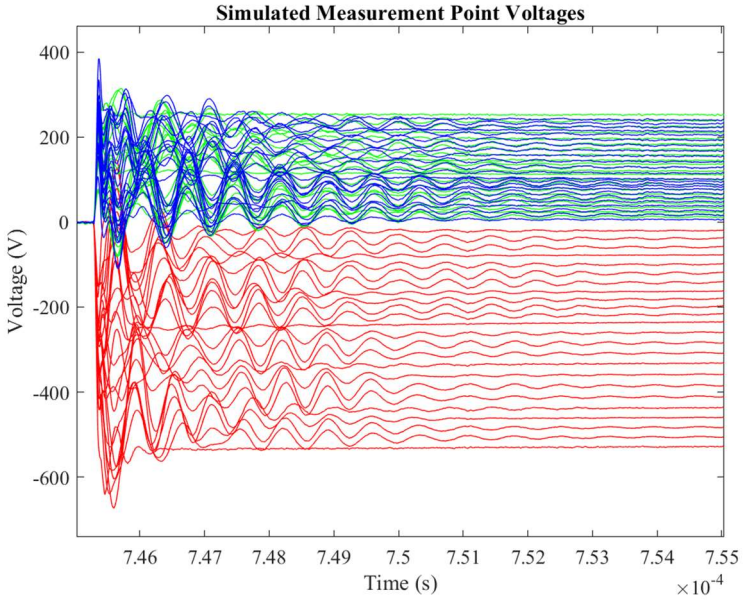

Figure 52. Measurement point voltages extracted from simulation output

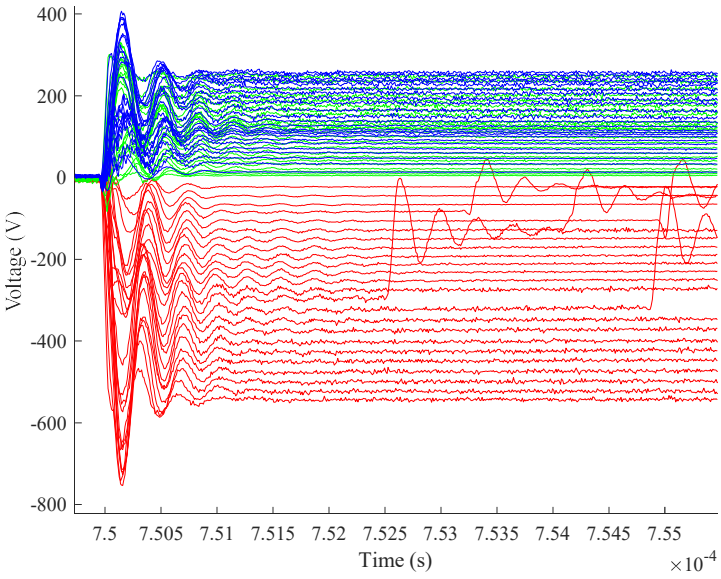

Figure 53. Measurement point voltages extracted from experimental test setup

Like in Chapter 2, the average voltage stresses between neighboring conductors in each slot can be plotted. In the 2D model, measurement points were added to every winding turn including all three parallel paths in each phase, but the same approximation will be used for plotting voltage stresses using only one parallel path to provide visual consistency. Figure 54 shows the calculated peak voltage stresses observed during testing at the t = 0.75 ms switching event. Figure 55 does the same but instead using the data extracted from the simulation output. When the time scale of the simulated waveform is shifted to align the rising edge of the switching event with the rising edge in the experimental waveforms, the time sample at which the maximum voltage stress is observed is exactly the same (16 samples past the switching transient, right at the peak transient overshoot region). There is some variability between the two calculations, for example the low voltage stress in slot 59 of the measured plot compared to the high voltage stress in slot 59 in the simulated plot. These variations are likely due to the interference of switching events present in the experimental testing as previously mentioned in Chapter 2. Overall, there is good correlation between the voltage stresses calculated between the model and testing. The poles of phase V and W contained within slots 52-54 and 58-60 clearly have higher stress levels than the other poles in this transient period.

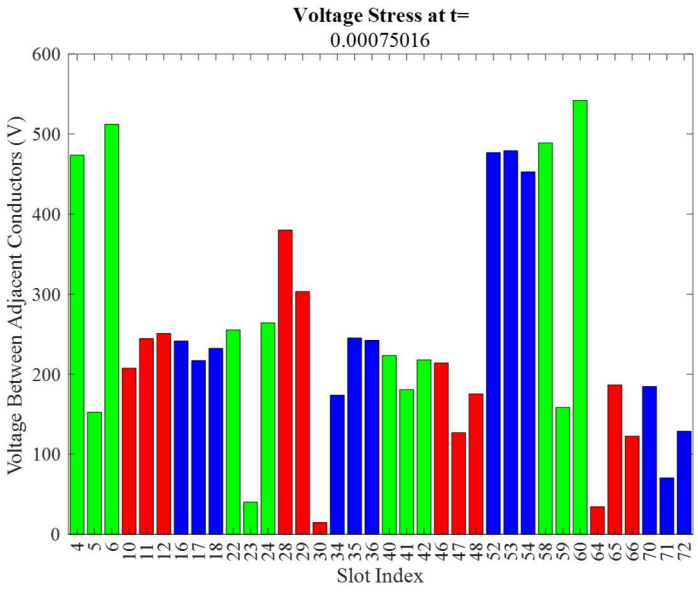

Figure 54. Maximum total voltage stresses observed for the t=0.75 Phase U switching transition during testing

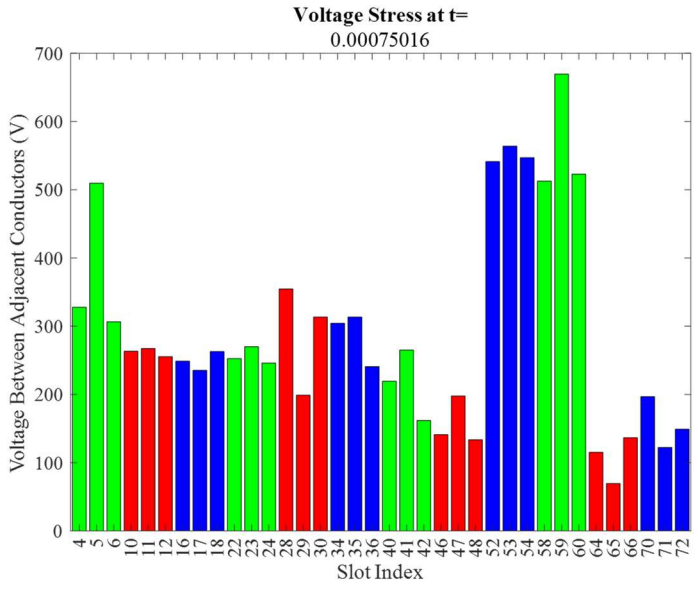

Figure 55. Maximum total voltage stresses observed for the t=0.75 Phase U switching transition produced by simulation

Chapter 5. Conclusions and Recommendations

5.1 Conclusions from Experimental Testing

One interesting observation from experimental testing was that the normalized voltage overshoot after a switching event decreases with increasing switching speeds. This is likely because of the relation of the overshoot to the dI/dt rate of the switching speed. Rapid changes in current after a switching event interacts with the inductance of the stator windings to produce the overshoot voltage. As the bus voltage increases, the rate at which dI/dt increases might not be as significant. If dI/dt does not increase at the same rate or greater than the rate of dV/dt increase, then the normalized overshoot should decrease like it did in this study. Regardless of the normalized overshoots, the absolute overshoot remains the highest at the highest bus voltage level, so the potential for PD events to occur is still highest at 800 V for a SiC inverter like the one used.

The peak voltage stresses seen between neighboring winding layers are typically around 500 V, with occasional peaks around 600 V. The winding coils are well insulated inside the slots; in between two adjacent windings in one slot are two layers of insulating varnish on the windings themselves, as well as insulating resin injected through vacuum impregnation. The winding varnish alone has a typical dielectric strength of 85 kV/mm,

and even at a thickness of around 0.1mm still provides appears to provide good insulating strength at these voltage levels.

Upon comparison of all Phase U switching events across one fundamental electrical period (provided in the Appendix), there is not necessarily a trend observed that relates the current phase to the level of voltage stress. However, it is observed that there tends to be higher voltage stresses on Phases V and W in relation to levels seen in Phase U windings during Phase U switching transients. Also, the voltage stress across all slots is significantly lower when the state transition is into a (000) or (111) state. For example, (011→111) or (100→000). This is intuitive as these switching states have zero line-line voltage at steady state, so any voltage seen in the windings at these times is purely due to transient ringing as it stabilizes to a zero line-line voltage.

Another observation from voltage stress testing is that the voltage distribution through sequential turns in the stator windings is not entirely consistent with the distribution in random-wound machines. Previous studies [1,2] have shown that the highest voltage stress across winding turns occurs in the first turns in the coils closest to the applied voltage phase lead. That trend does not appear in the results of this study, likely due to this machine winding being in a wave pattern rather than a lap pattern, as well as only having one turn per coil rather than multiple.

5.2 Conclusions from PD Testing

PDIV was observed under varying temperature and pressure conditions. At standard temperature and pressure (room temperature of 20° C, 760 Torr), the average PDIV was 1.12 kV. This is significantly higher than the expected future automotive bus voltage of 800 V. However, at reduced pressure this average was reduced by 11.3% to 993 V, which is relatively close to the maximum voltage seen applied by the inverter during switching transients of 886 V (Table 2). Once the windings were heated up to the middle of their operating temperature range, an approximate reduction in PDIV of 10% to 945 V was seen at 85° C, which is also close to the maximum observed voltage during inverter testing relative to the negative bus. Combining both effects could result in a reduction to the same peak voltage that is produced by the inverter at the 800 V DC bus level, which means that observing occasional PD events for very brief instances immediately following inverter switching events is possible. It can be reasonably concluded that the PD observed during testing was between the stator windings and the stator core itself rather than between windings, since very little current was being applied and therefore only small turn voltages were induced. It is recommended to perform additional PD testing using a different measurement setup to observe PD while the machine is under more realistic operating conditions.

5.3 Conclusions from Simulation

Comparisons between the calculated voltage stress between neighboring conductors using the simulation output and the experimental testing results show similar trends in

voltage stress per pole. Individual comparisons between voltage stresses in any given slot can vary between the two measurement methods, however, the average level of voltage stresses is very close. The simulation in its current state therefore can provide a good estimate for the voltage stresses in a bar-wound machine design. Accuracy was likely reduced by the variation in actual manufacturing tolerance from the ideal design as was built in the model, as well as deviation in actual resin impregnation volume compared to the target value of 80% provided by the manufacturer. Fidelity could be improved by fine-tuning the amount of dielectric material in each slot.

5.4 Future Research Opportunities

Accuracy of the experimental test setup for calculating voltage stresses is severely limited by the available number of simultaneously measured channels. If the oscilloscope available had five channels instead of four, the voltage at each phase lead relative to the negative DC bus could be recorded for every measurement, which would allow alignment of the waveforms to switching events in any of the three phases. This would provide a definitive answer for whether higher voltage stresses are always seen in the other two phase windings when a switching event occurs in the switching phase.

The method of simulating voltage stresses within stator windings as first proposed by [1-2] for a random-wound stator has been validated for the bar-wound stator design. 2D modeling using FEA for voltage stress analysis is a powerful tool to optimize insulation design of an electric machine and can likely be extended to other stator designs. The

validity of this form of simulation using other winding patterns for the bar-wound machine has yet to be determined.

5.5 Closing Remarks and Contributions

This paper analyzed voltage stresses within a bar-wound IPMSM excited by an inverter with SiC MOSFETs. Extensive experimental testing was performed to characterize the switching performance of SiC inverters when connected to a bar-wound machine. PDIV testing was also performed to quantify the bus voltage level at which insulation degradation due to partial discharge may occur. A 2D FEA model was also constructed to provide another method of voltage stress calculation for this type of stator. Major contributions of this paper have been 1) characterization of switching behavior in the CREE/Wolfspeed SiC inverter package connected to bar-wound stator, 2) a method of determining voltage stress within neighboring layers in a slot without measuring each layer, 3) an analysis of voltage stresses within bar-wound stator windings, 4) determination of PDIV for a bar-wound stator assembly under varying temperature and pressure, and 5) construction and implementation of a 2D FEA model to simulate voltage stresses in a bar-wound stator.

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Appendix A. Comprehensive list of voltage stresses and turn voltages during all switching events of Phase U over one fundamental period

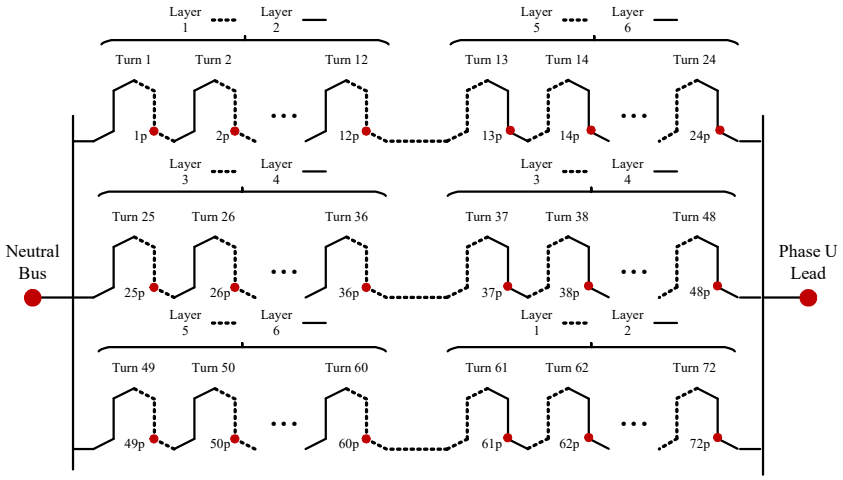

Figure 56. Phase U winding layers per parallel path with measurement points labelled

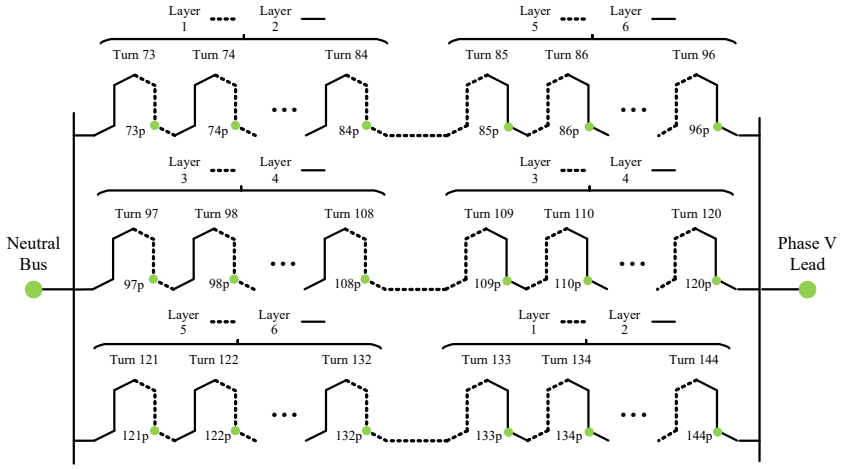

Figure 57. Phase V winding layers per parallel path with measurement points labelled

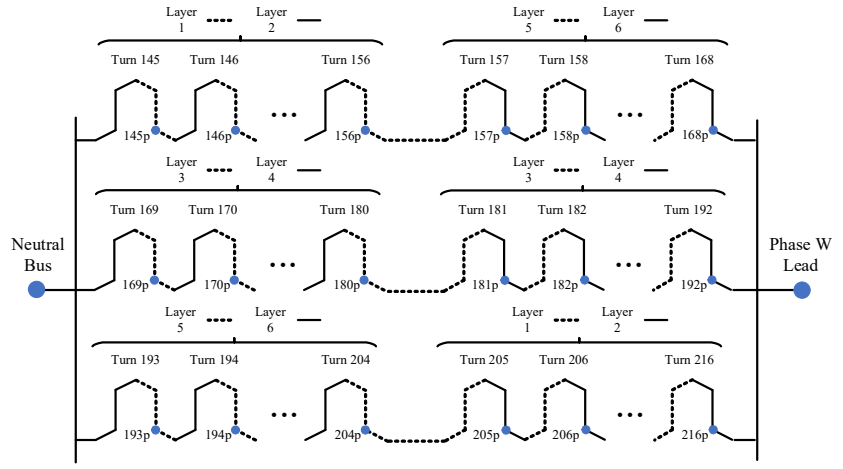

Figure 58. Phase W winding layers per parallel path with measurement points labelled

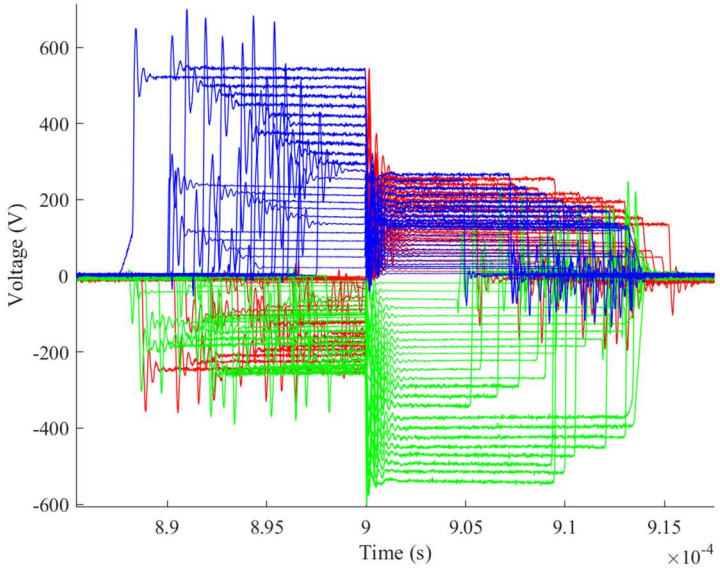

Figure 59. Aligned winding measurement point waveforms to t=0.00 ms (001 → 101). Time axis is shifted within the fundamental period by 0.1 ms in this figure to bring the t=0.00 ms switching pulses within a viewable window, i.e. t=0.9 ms is actually t=0.0 ms

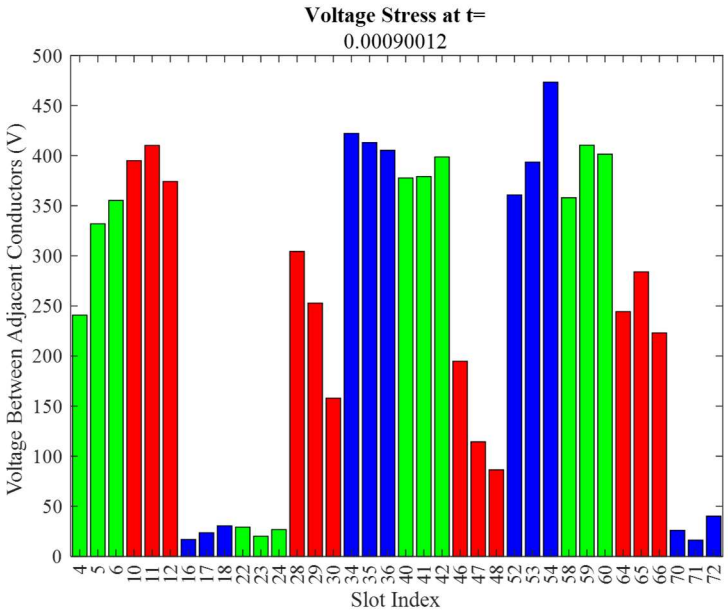

Figure 60. Maximum total and maximum peak stress near t=0.00 ms (001 → 101). Time axis is shifted within the fundamental period by 0.1 ms in this figure to bring the t=0.00 ms switching pulses within a viewable window, i.e. t=0.90012 ms is actually t=0.0012 ms

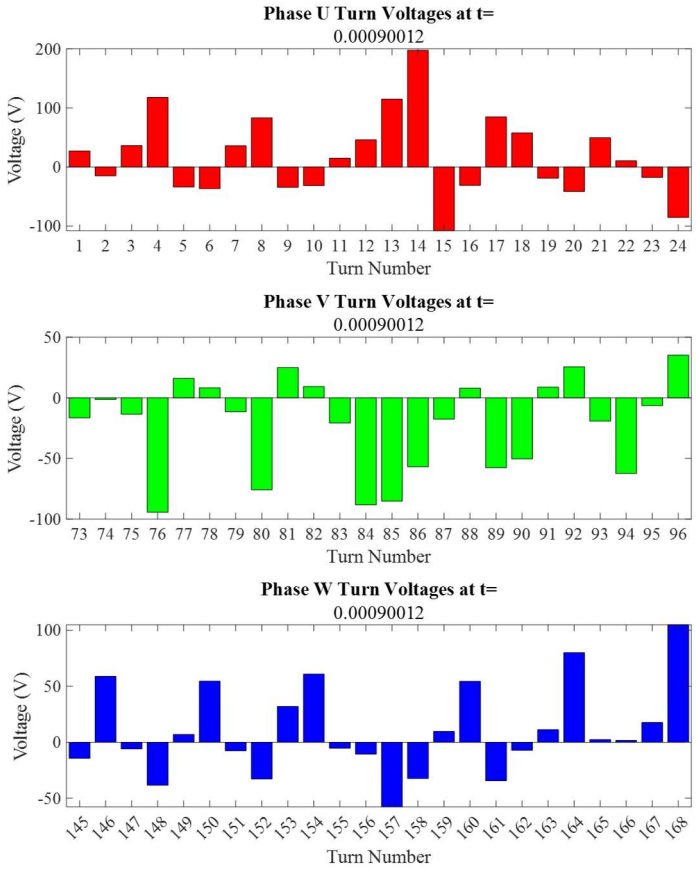

Figure 61. Turn voltages per phase at the time instant of maximum overall observed voltage stresses near t=0.00 ms (001 → 010). Time axis is shifted within the fundamental period by 0.1 ms in this figure to bring the t=0.00 ms switching pulses within view, i.e. t=0.90012 ms is actually t=0.00012 ms

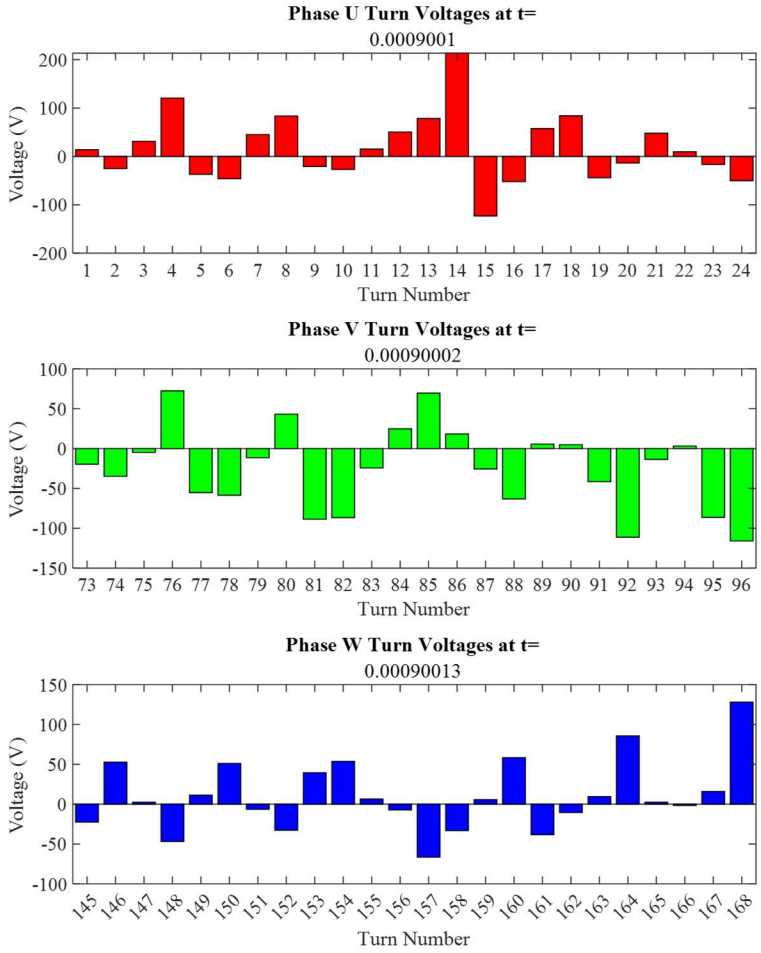

Figure 62. Turn voltages per phase at time instants near t=0.45 where the maximum turn voltage was observed (110 → 010). Time axis is shifted within the fundamental period by 0.1 ms in this figure to bring the t=0.00 ms switching pulses within view, i.e. t=0.90001 ms is actually t=0.00001 ms

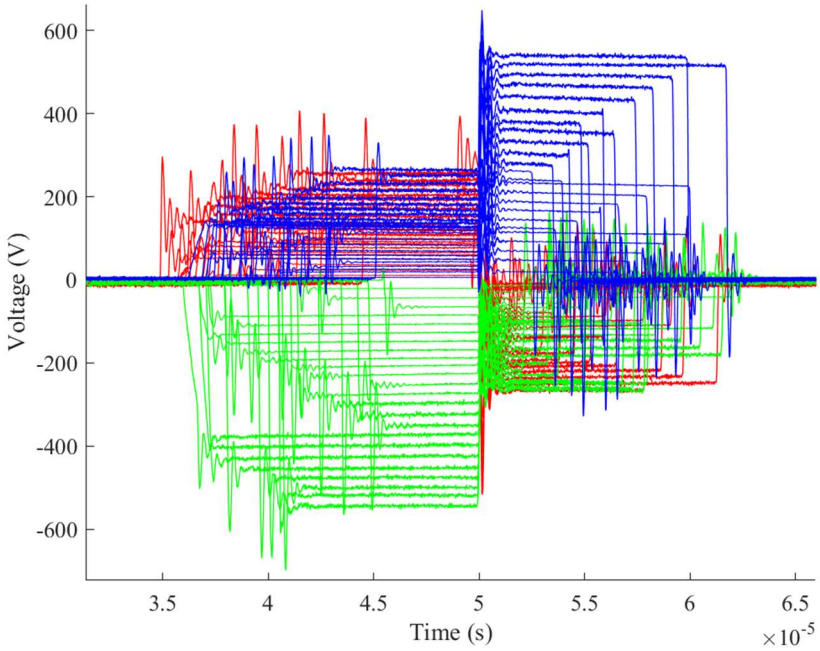

Figure 63. Aligned winding measurement point waveforms to t=0.05 ms (101 → 001)

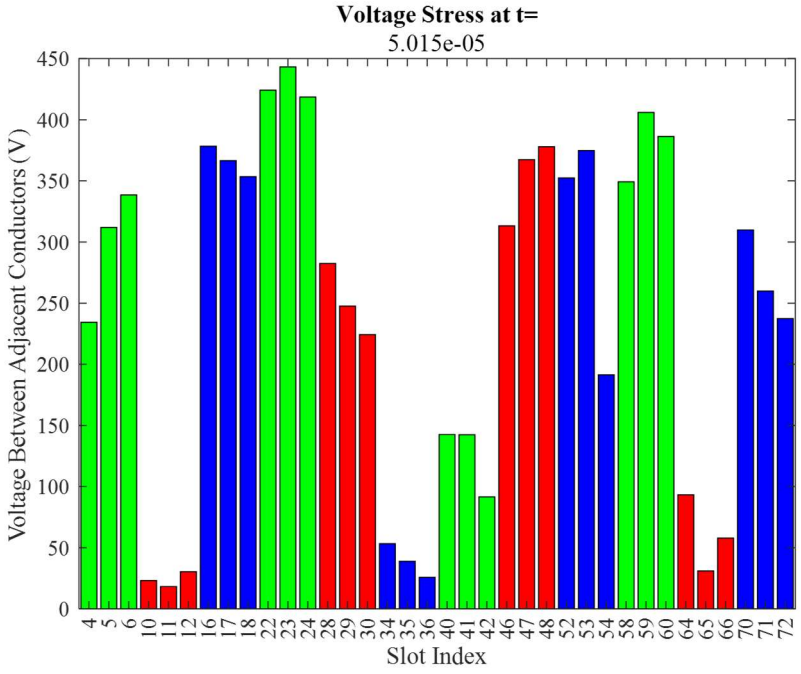

Figure 64. Maximum total and maximum peak stress near t=0.05 ms (101 → 001)

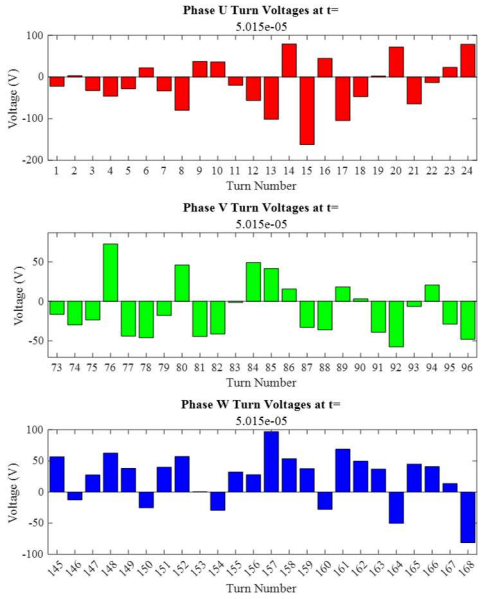

Figure 65. Turn voltages per phase at the time instant of maximum overall observed voltage stresses near t=0.05 ms (101 → 001)

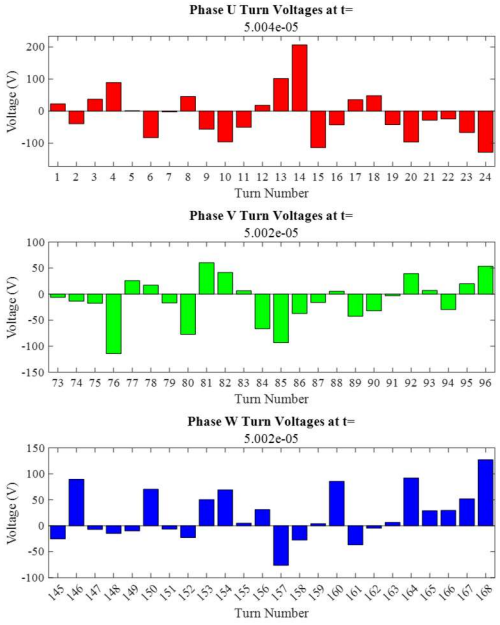

Figure 66. Turn voltages per phase at time instants near t=0.05 where the maximum turn voltage was observed (101 → 001)

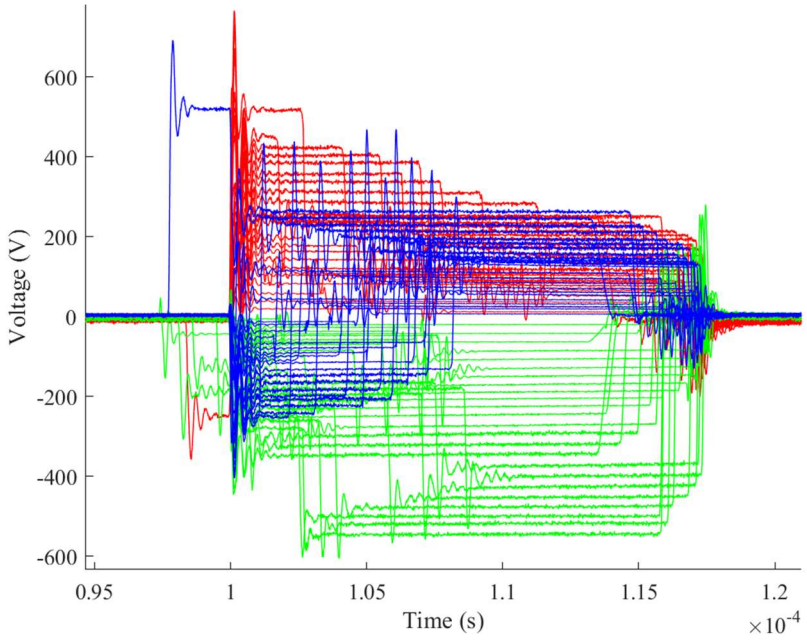

Figure 67. Aligned winding measurement point waveforms to t=0.1 ms (000 → 100)

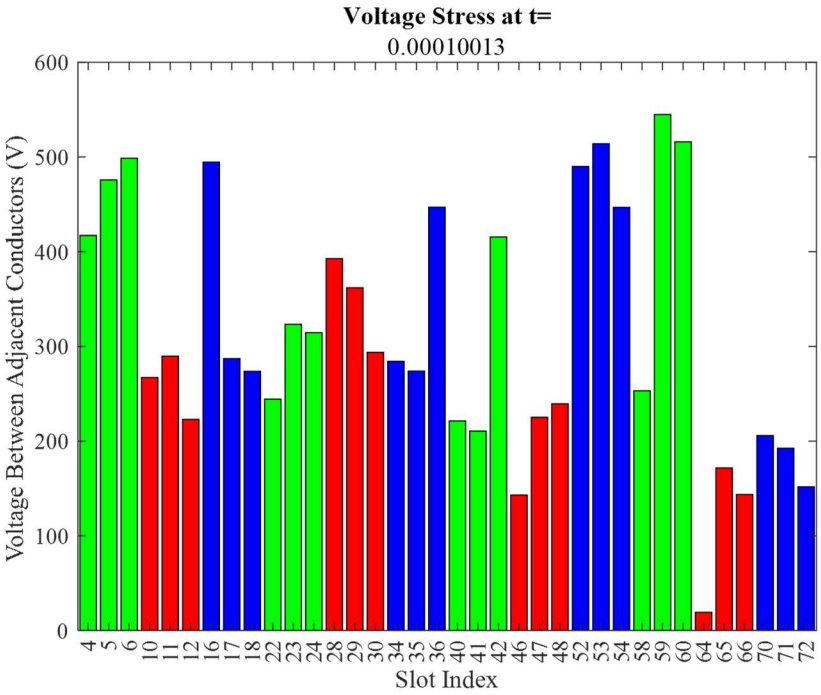

Figure 68. Maximum total and maximum peak stress near t=0.1 ms (000 → 100)

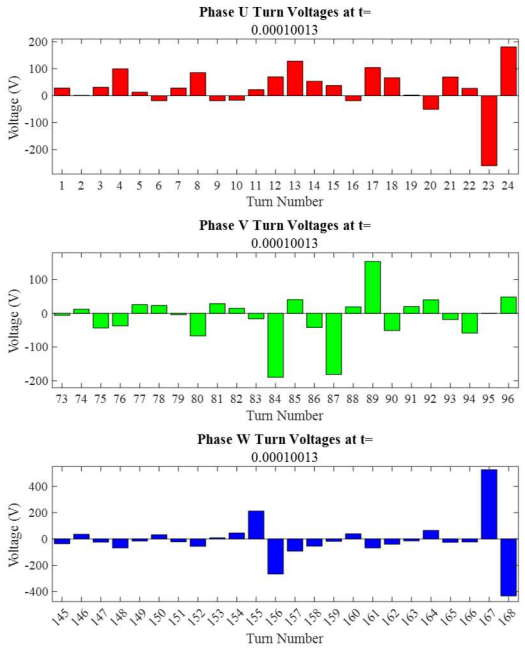

Figure 69. Turn voltages per phase at the time instant of maximum overall observed voltage stresses near t=0.1 ms (000 → 100)

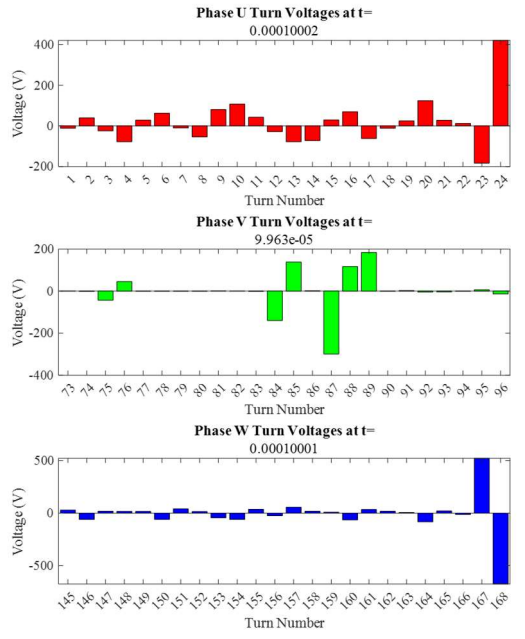

Figure 70. Turn voltages per phase at time instants near t=0.1 where the maximum turn voltage was observed (000 → 100)

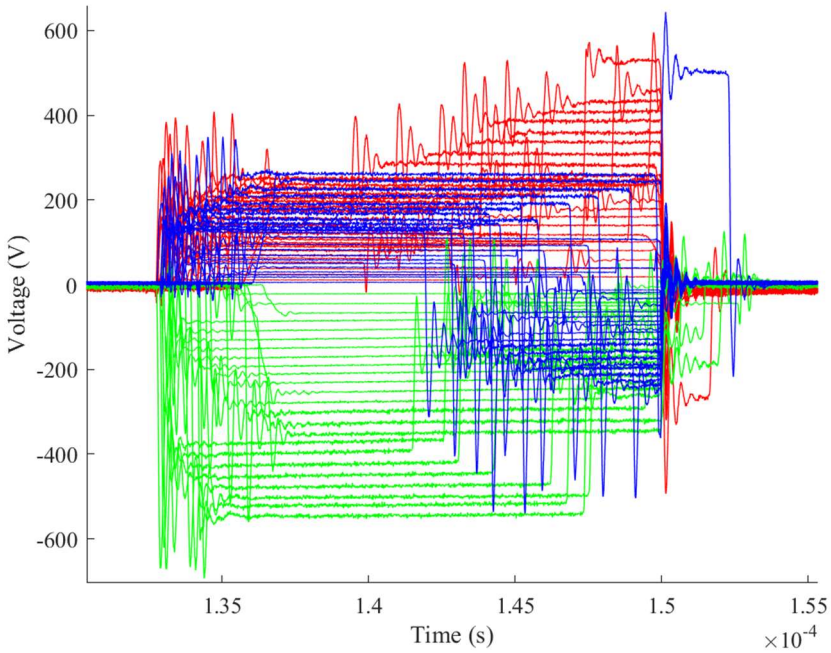

Figure 71. Aligned winding measurement point waveforms to t=0.15 ms (100 → 000)

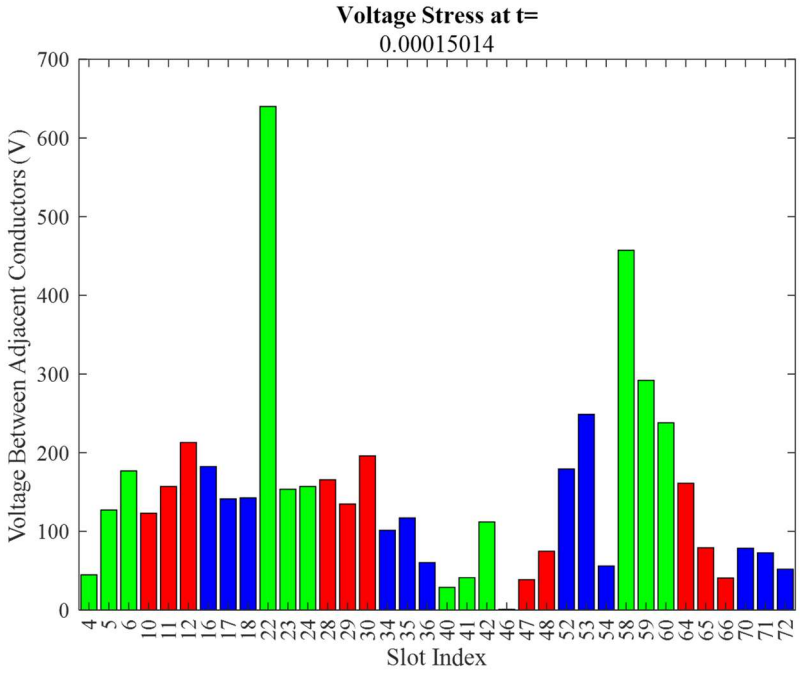

Figure 72. Maximum peak stress near t=0.15 ms (100 → 000)

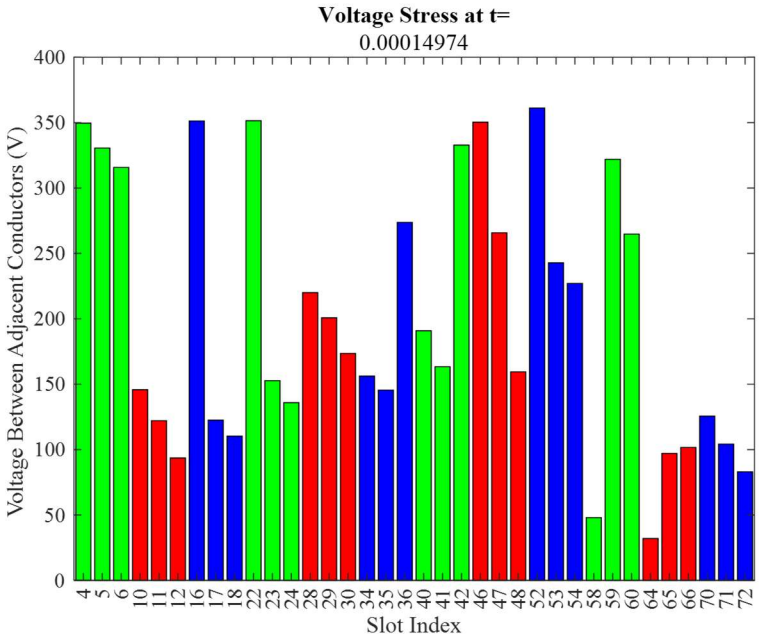

Figure 73. Maximum total stress near t=0.15 ms (100 → 000)

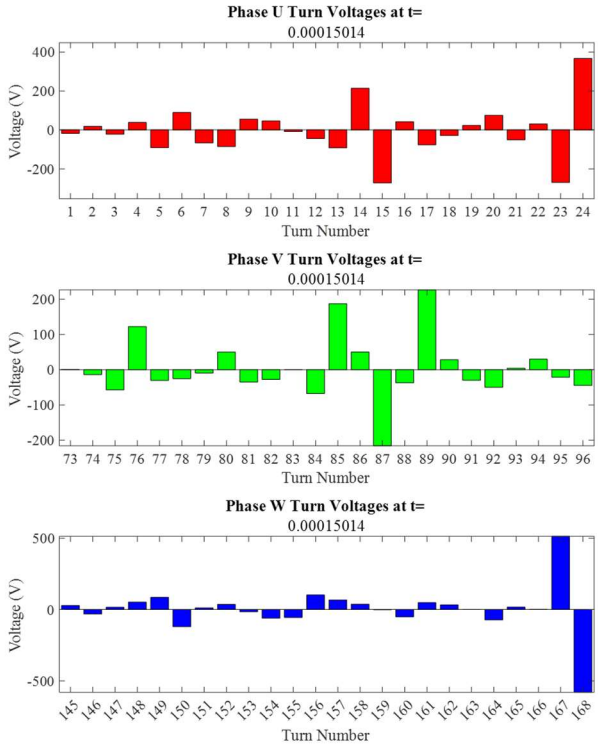

Figure 74. Turn voltages per phase at the time instant of maximum peak observed voltage stresses near t=0.15 ms (100 → 000)

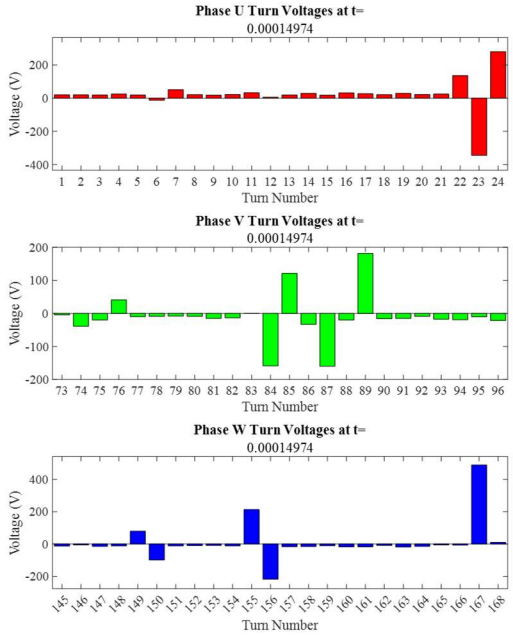

Figure 75. Turn voltages per phase at the time instant of maximum total observed voltage stresses near t=0.15 ms (100 → 000)

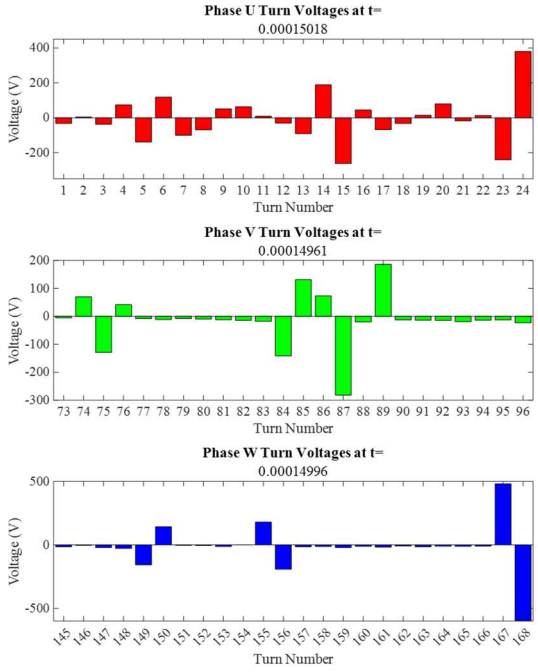

Figure 76. Turn voltages per phase at time instants near t=0.15 where the maximum turn voltage was observed (100 → 000)

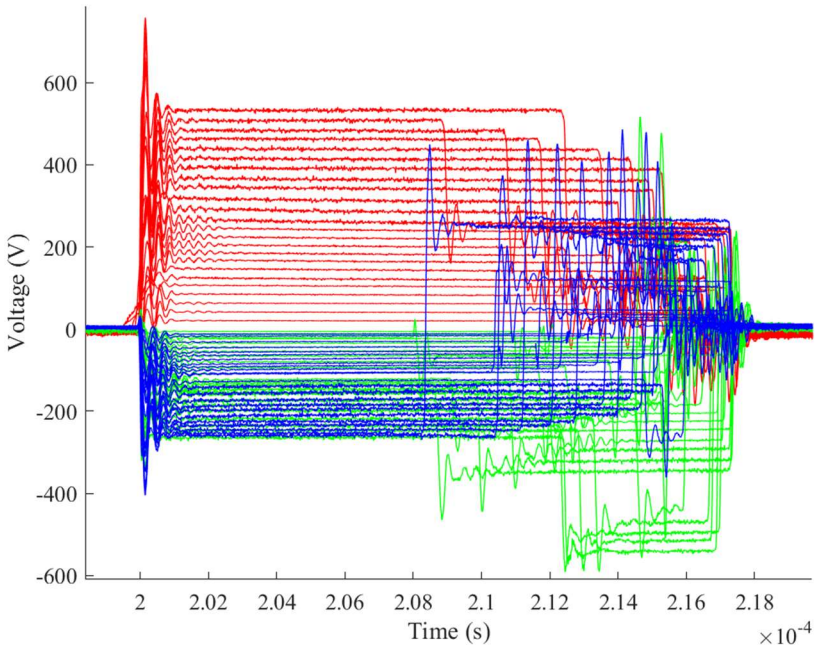

Figure 77. Aligned winding measurement point waveforms to t=0.2 ms (000 → 100)

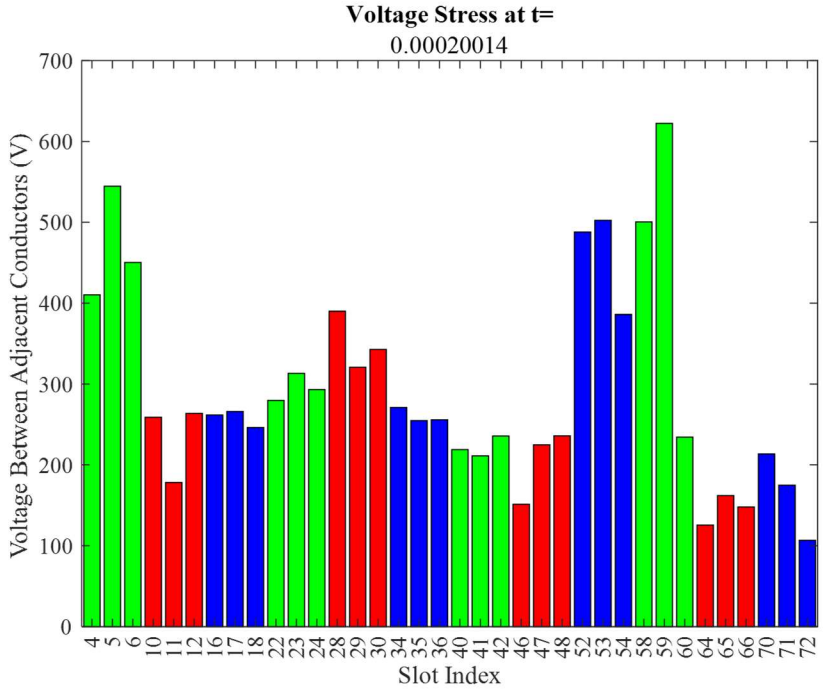

Figure 78. Maximum total and maximum peak stress near t=0.2 ms (000 → 100)

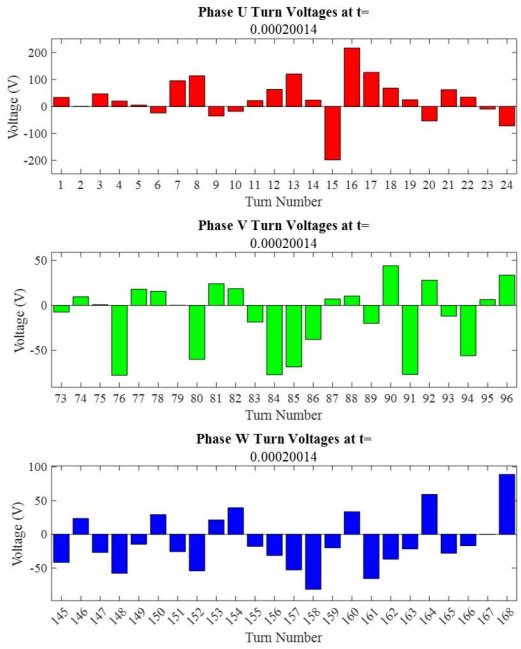

Figure 79. Turn voltages per phase at the time instant of maximum overall observed voltage stresses near t=0.2 ms (000 → 001)

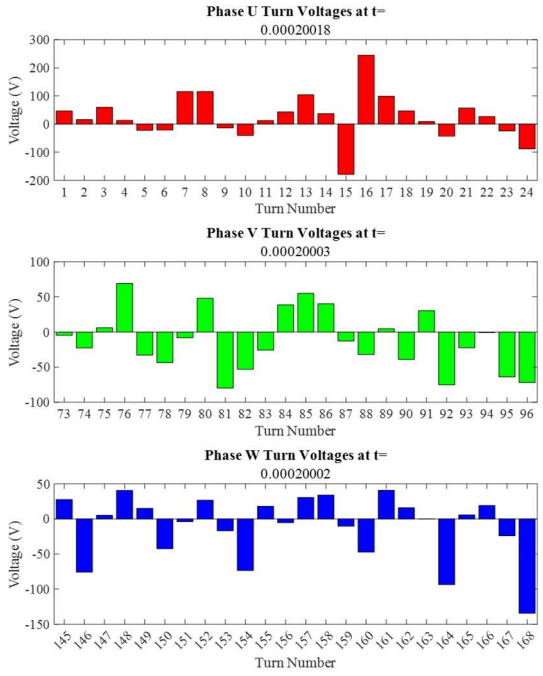

Figure 80. Turn voltages per phase at time instants near t=0.2 ms where the maximum turn voltage was observed (000 → 001)

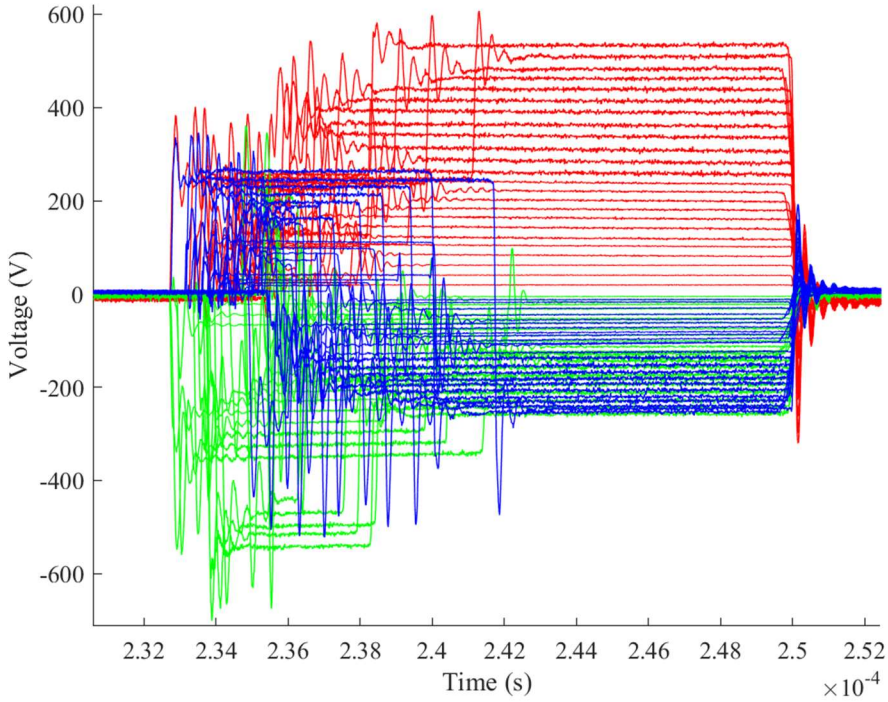

Figure 81. Aligned winding measurement point waveforms to t=0.25 ms (100 → 000)

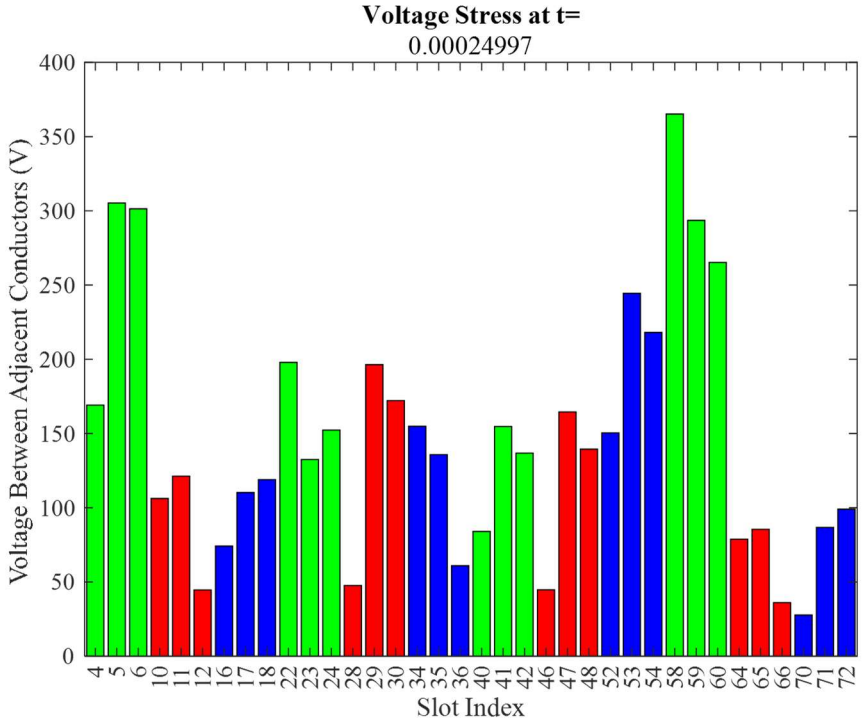

Figure 82. Maximum peak stress near t=0.25 ms (100 → 000)

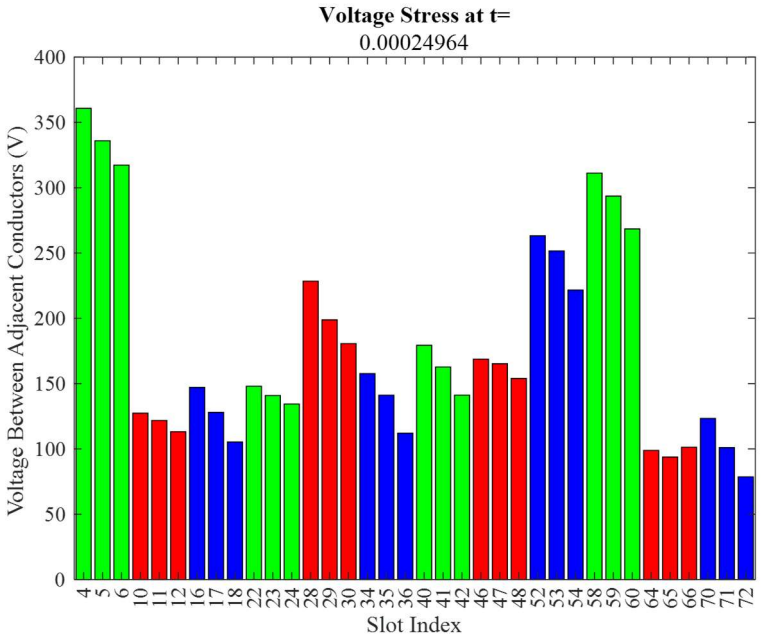

Figure 83. Maximum total stress near t=0.25 ms (100 → 000)

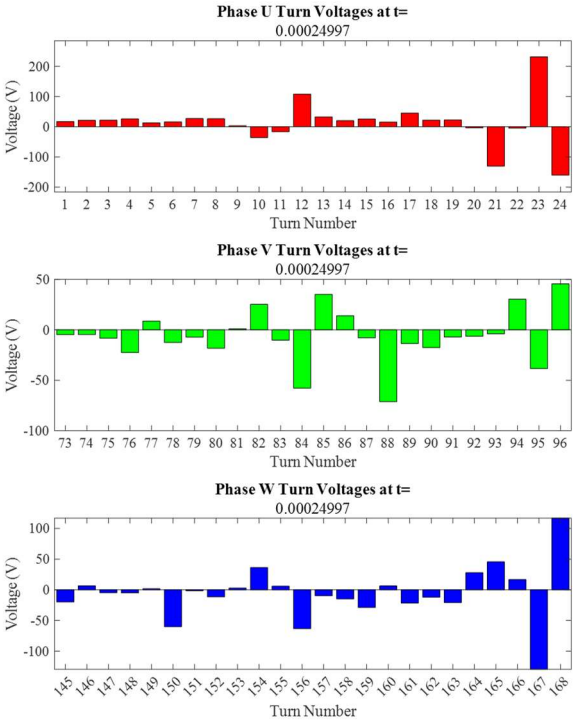

Figure 84. Turn voltages per phase at the time instant of maximum peak observed voltage stresses near t=0.25 ms (100 → 000)

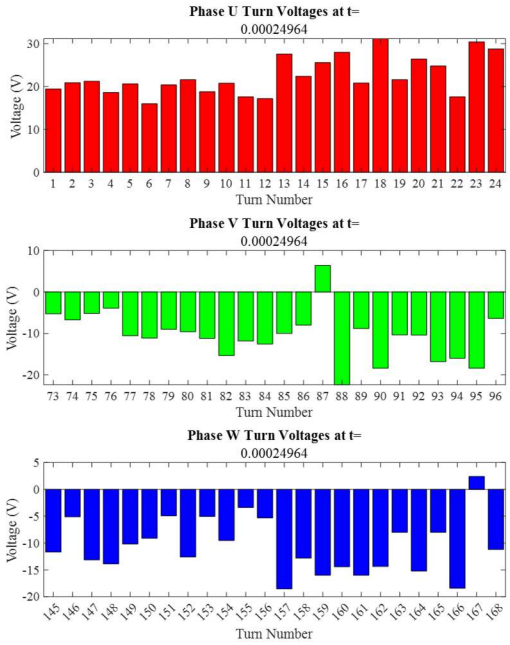

Figure 85. Turn voltages per phase at the time instant of maximum total observed voltage stresses near t=0.25 ms (100 → 000)

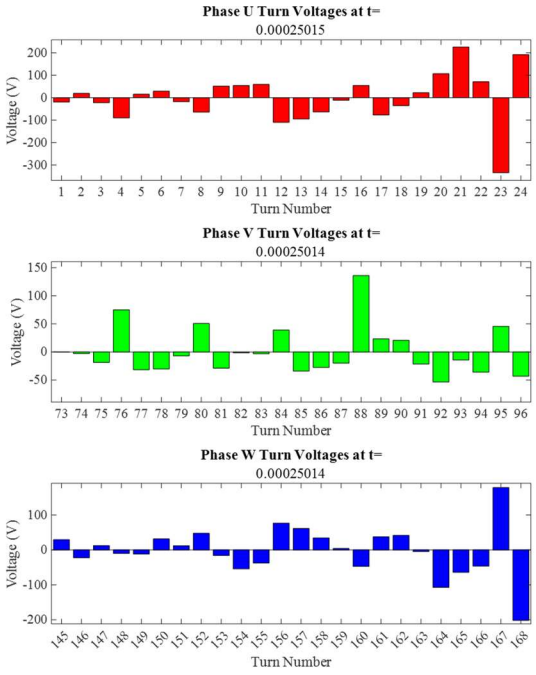

Figure 86. Turn voltages per phase at time instants near t=0.25 where the maximum turn voltage was observed (100 → 000)

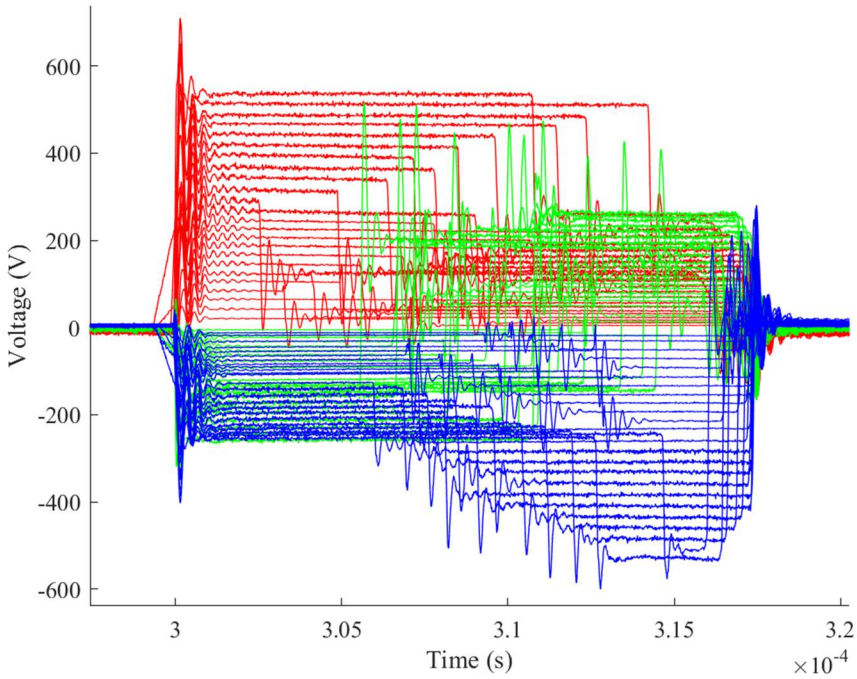

Figure 87. Aligned winding measurement point waveforms to t=0.3 ms (000 → 100)

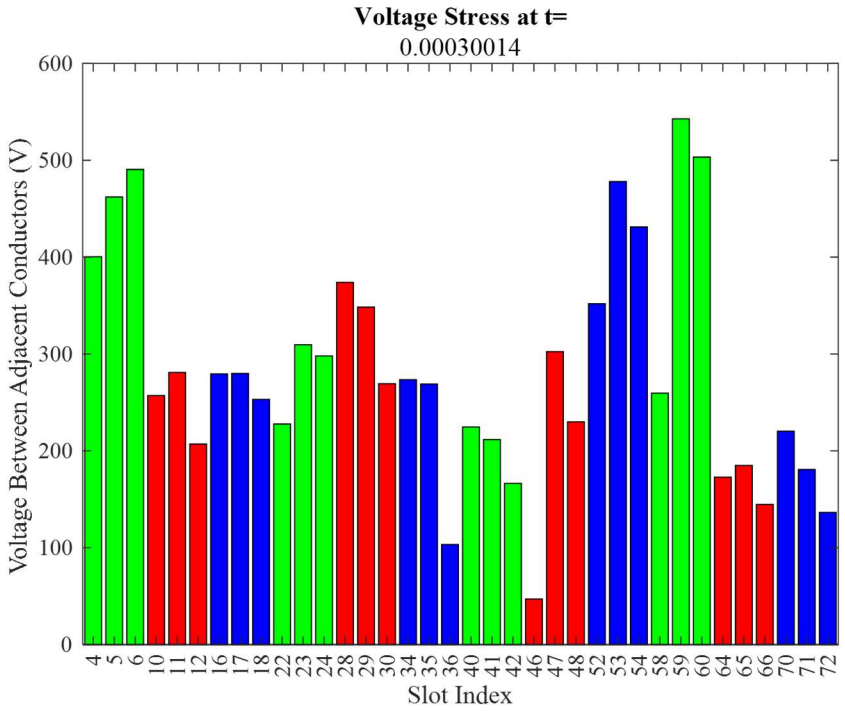

Figure 88. Maximum total and maximum peak stress near t=0.35 ms (000 → 100)

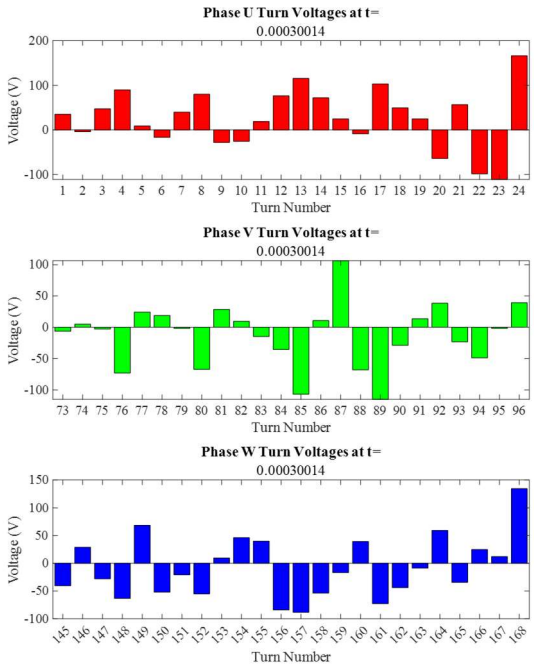

Figure 89. Turn voltages per phase at the time instant of maximum overall observed voltage stresses near t=0.3 ms (000 → 001)

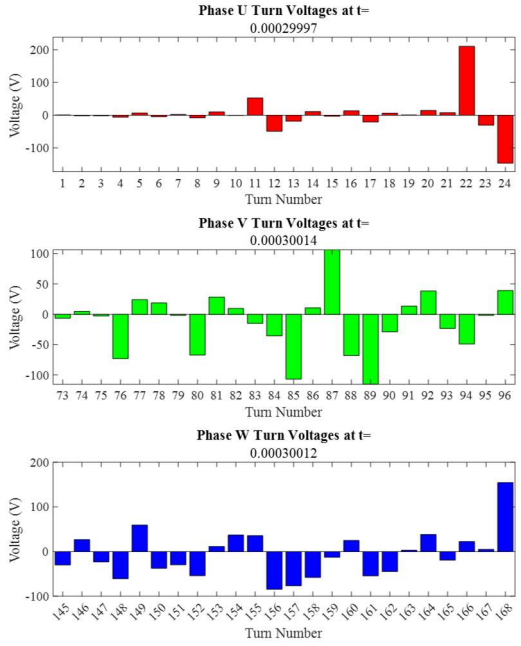

Figure 90. Turn voltages per phase at time instants near t=0.3 ms where the maximum turn voltage was observed (000 → 001)

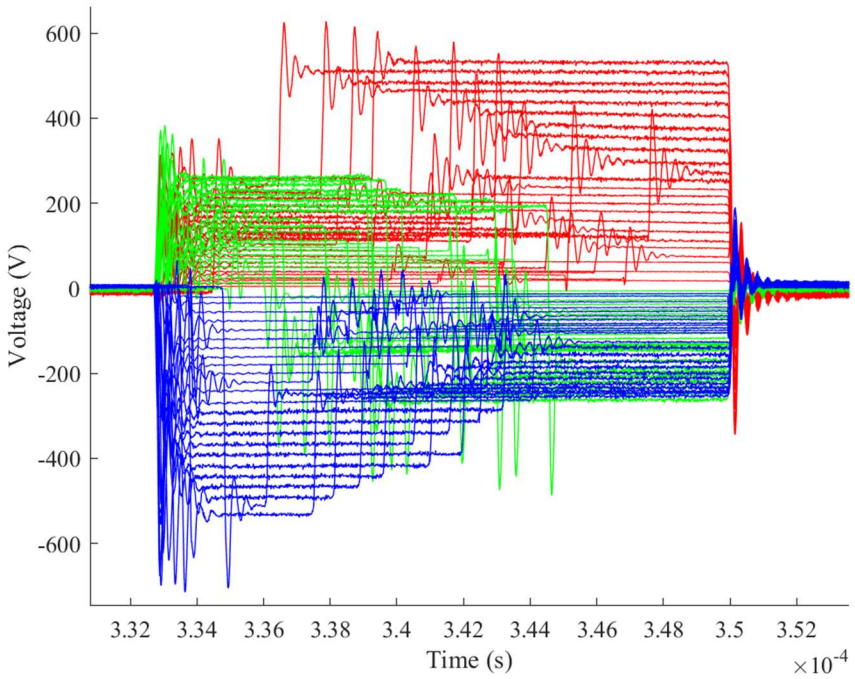

Figure 91. Aligned winding measurement point waveforms to t=0.35 ms (100 → 000)

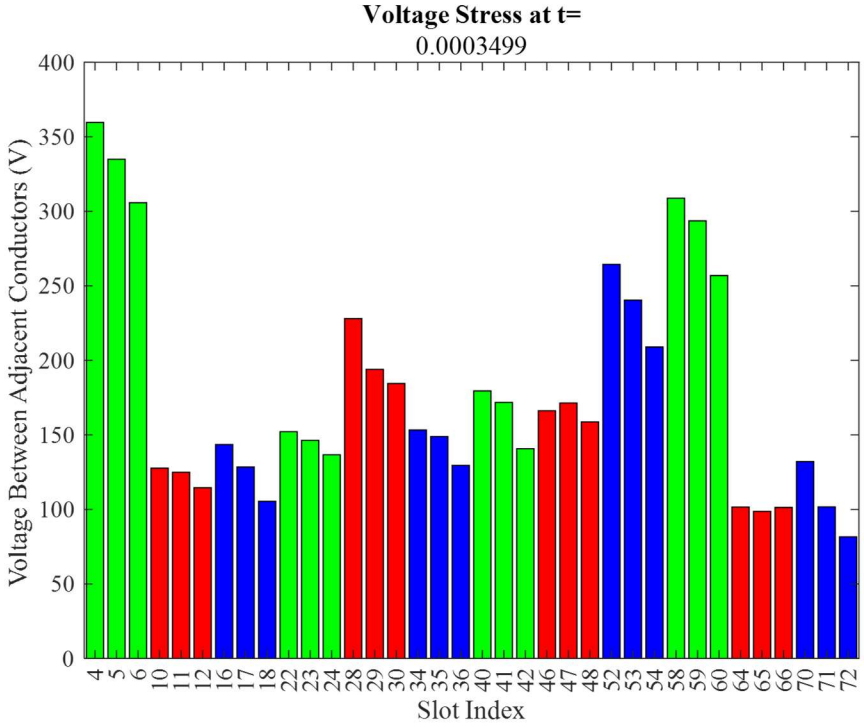

Figure 92. Maximum total and maximum peak stress near t=0.35 ms (100 → 000)

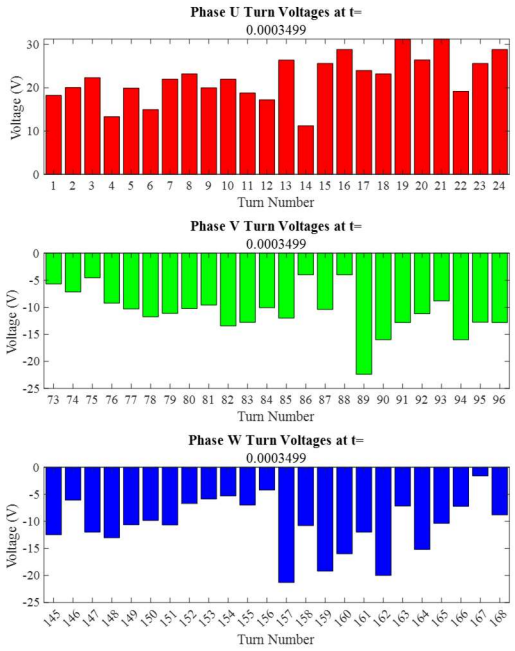

Figure 93. Turn voltages per phase at the time instant of maximum overall observed voltage stresses near t=0.35 ms (100 → 000)

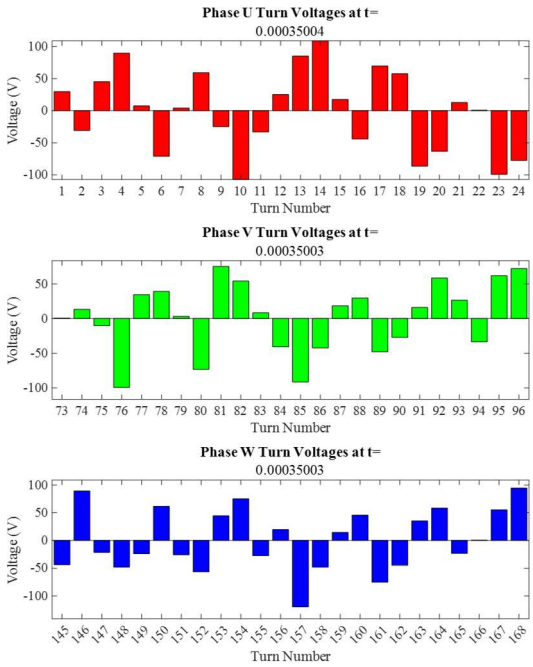

Figure 94. Turn voltages per phase at time instants near t=0.35 ms where the maximum turn voltage was observed (100 → 000)

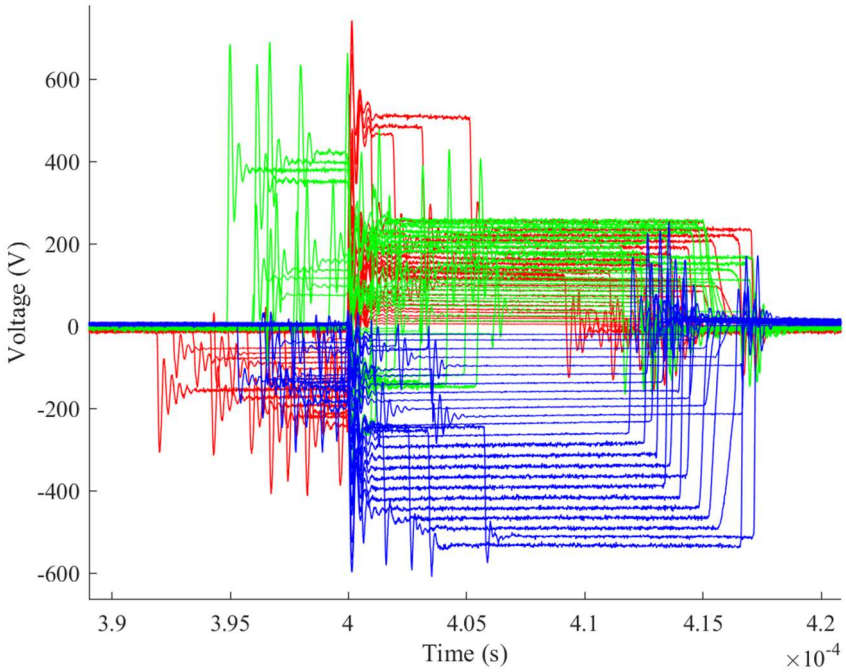

Figure 95. Aligned winding measurement point waveforms to t=0.4 ms (010 → 110)

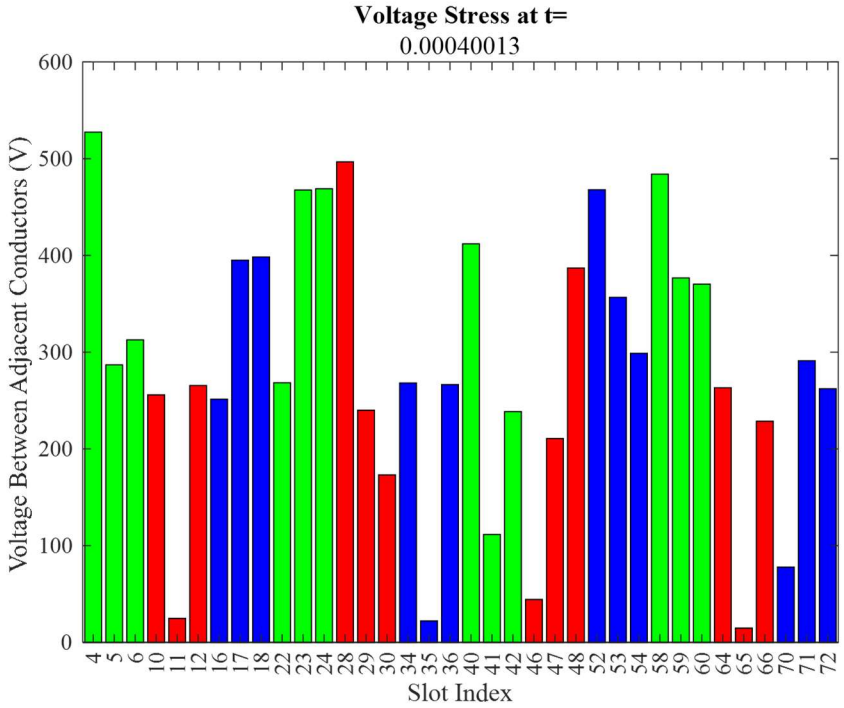

Figure 96. Maximum total and maximum peak stress near t=0.4 ms (010 → 110)

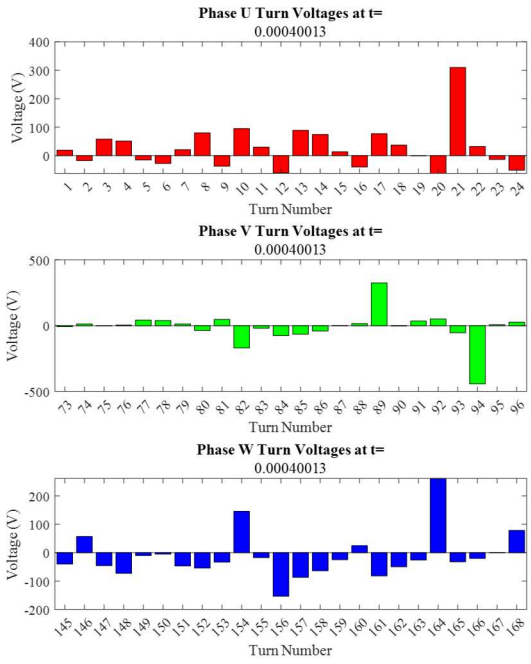

Figure 97. Turn voltages per phase at the time instant of maximum overall observed voltage stresses near t=0.4 ms (010 → 110)

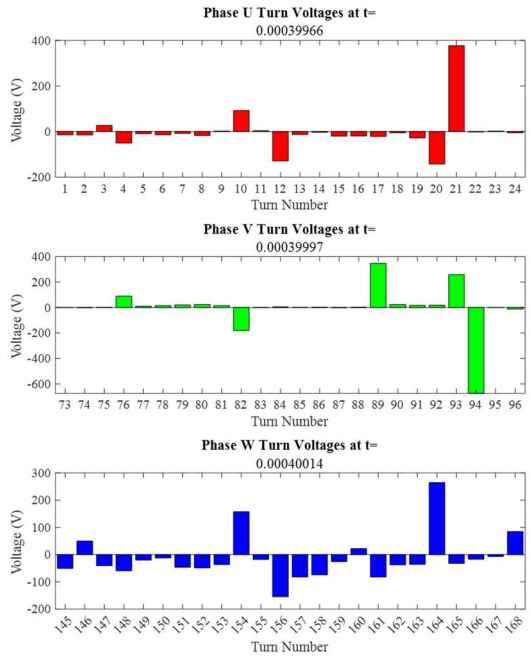

Figure 98. Turn voltages per phase at time instants near t=0.4 ms where the maximum turn voltage was observed (010 → 110)

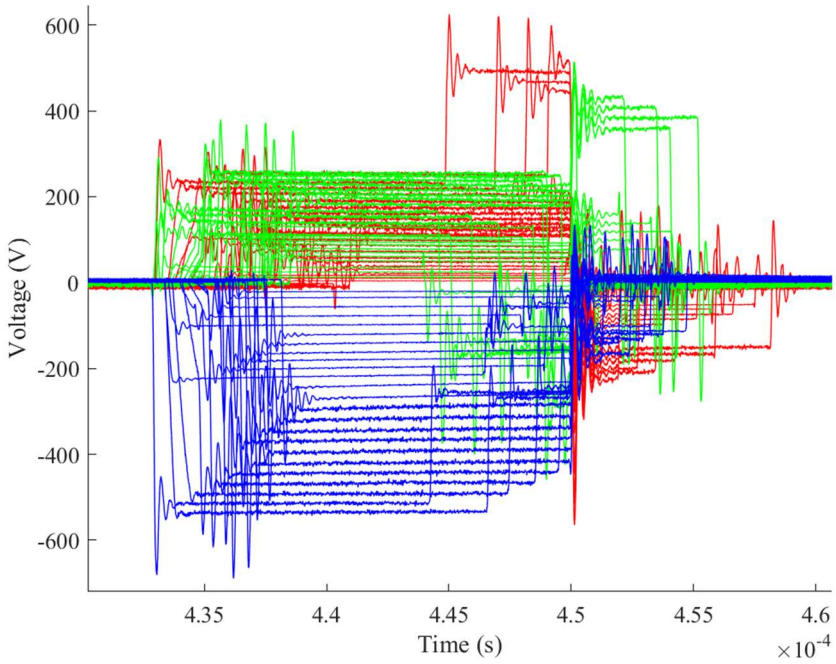

Figure 99. Aligned winding measurement point waveforms to t=0.45 ms (110 → 010)

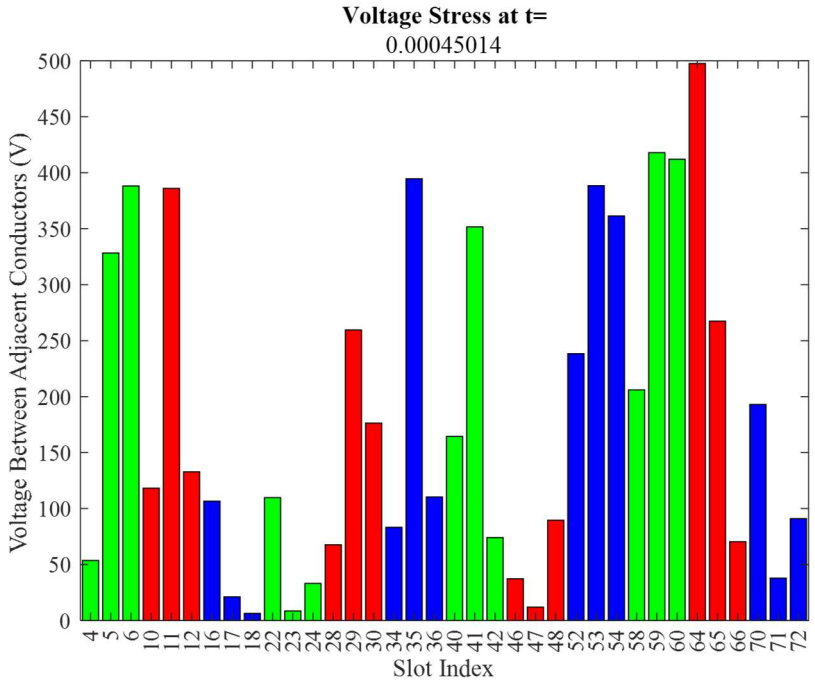

Figure 100. Maximum total and maximum peak stress near t=0.45 ms (110 → 010)

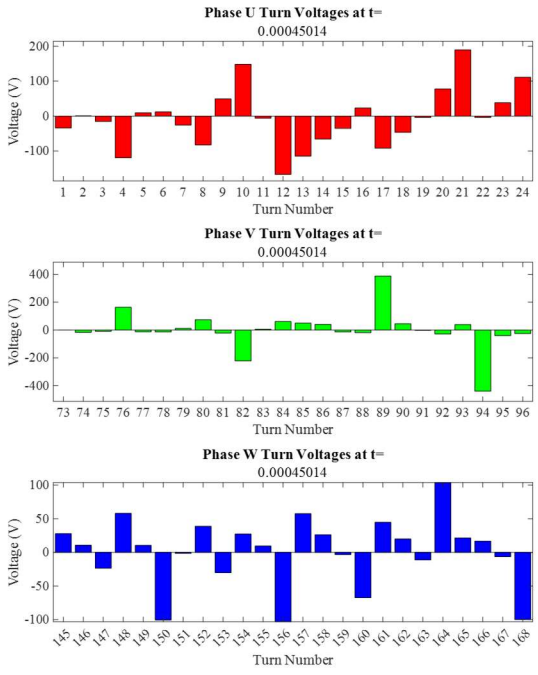

Figure 101. Turn voltages per phase at the time instant of maximum overall observed voltage stresses near t=0.45 ms (110 → 010)

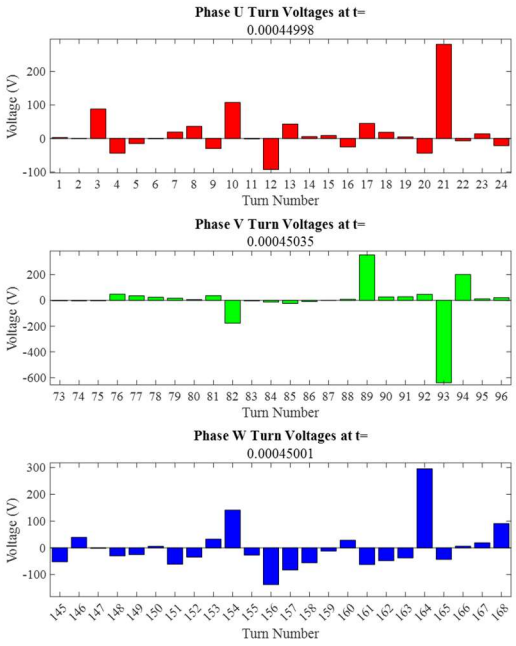

Figure 102. Turn voltages per phase at time instants near t=0.45 ms where the maximum turn voltage was observed (110 → 010)

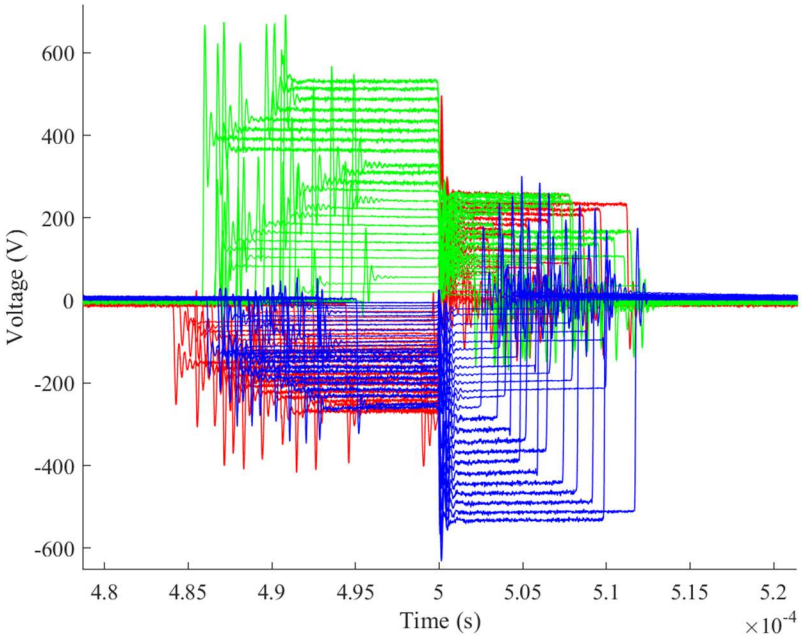

Figure 103. Aligned winding measurement point waveforms to t=0.5 ms (010 → 110)

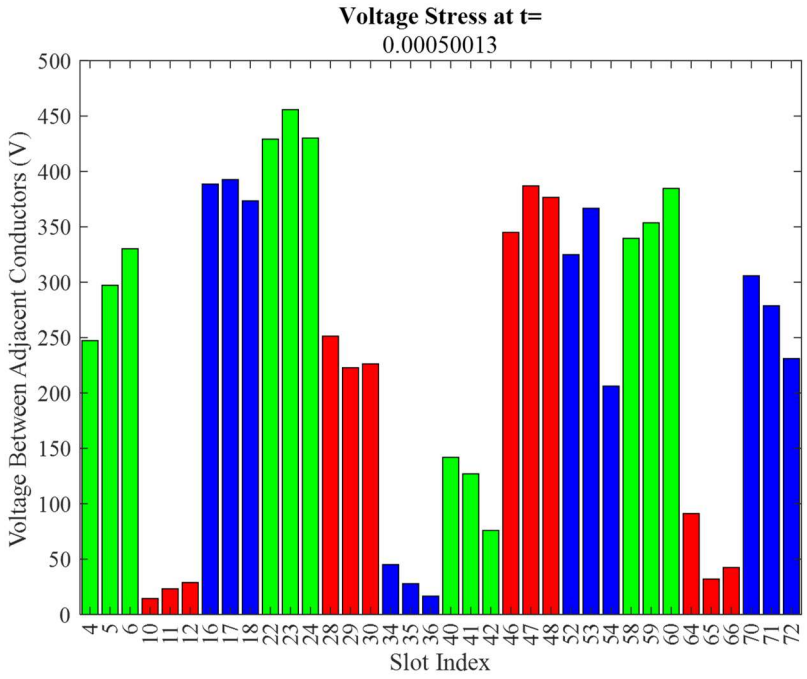

Figure 104. Maximum total and maximum peak stress near t=0.5 ms (010 → 110)

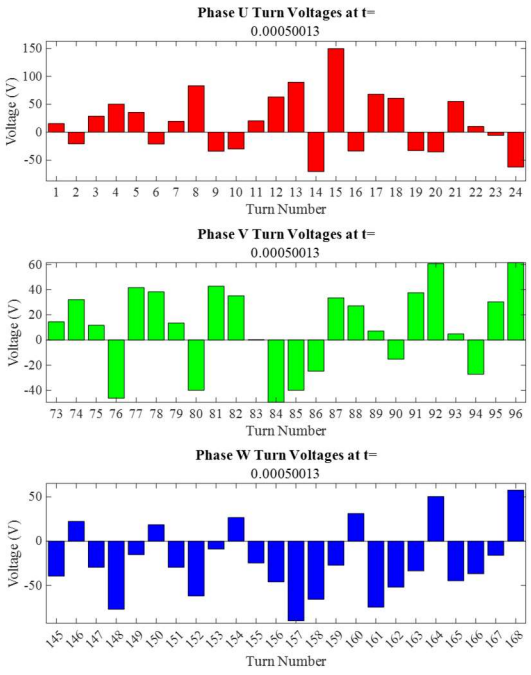

Figure 105. Turn voltages per phase at the time instant of maximum overall observed voltage stresses near t=0.5 ms (010 → 110)

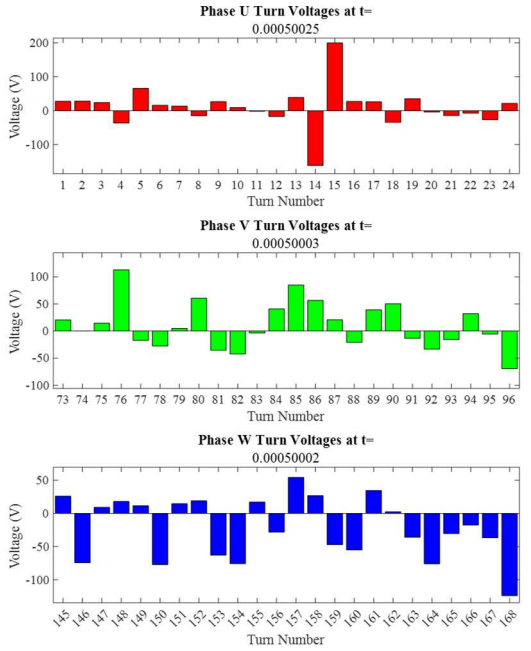

Figure 106. Turn voltages per phase at time instants near t=0.5 ms where the maximum turn voltage was observed (010 → 110)

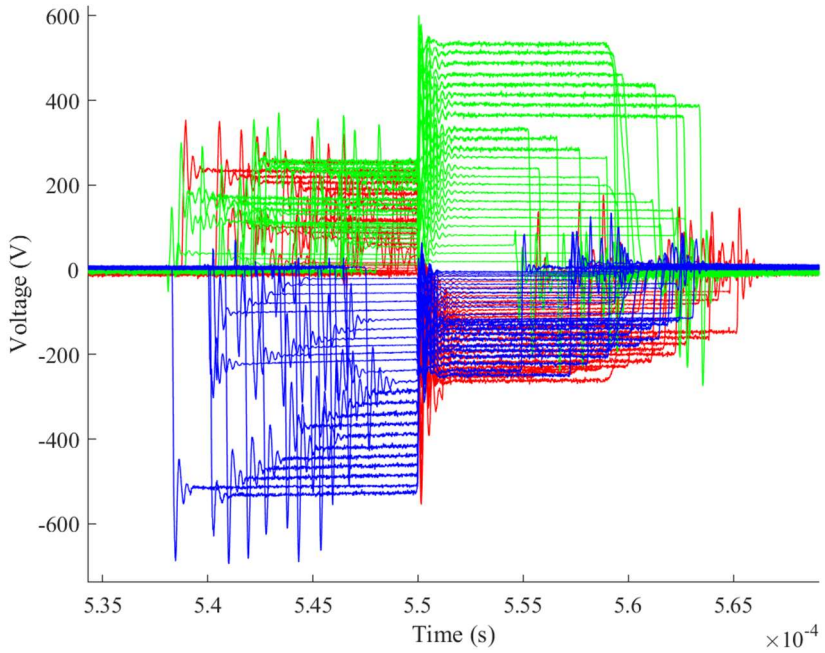

Figure 107. Aligned winding measurement point waveforms to t=0.55 ms (110 → 010)

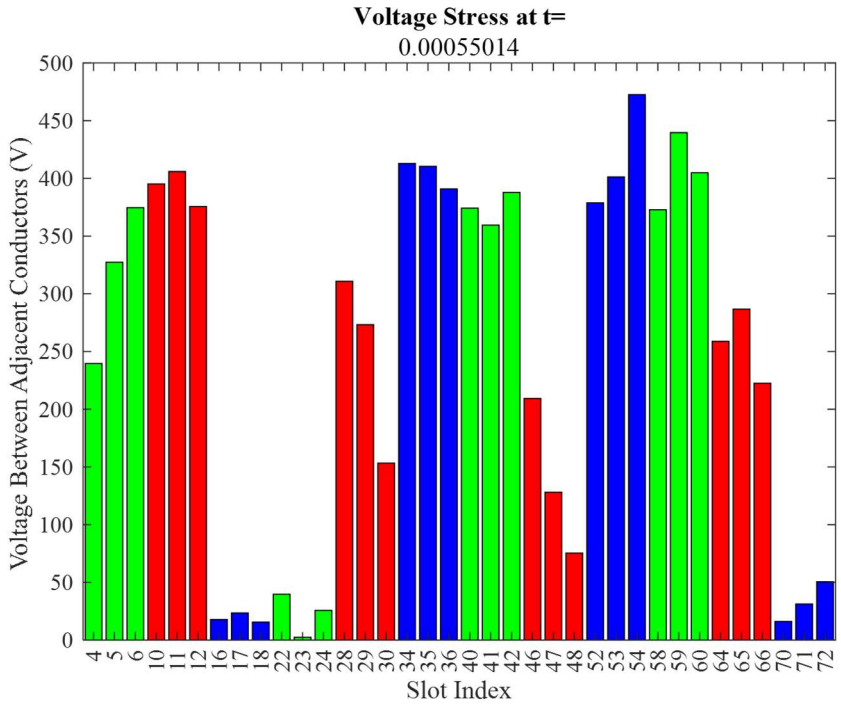

Figure 108. Maximum total and maximum peak stress near t=0.55 ms (110 → 010)

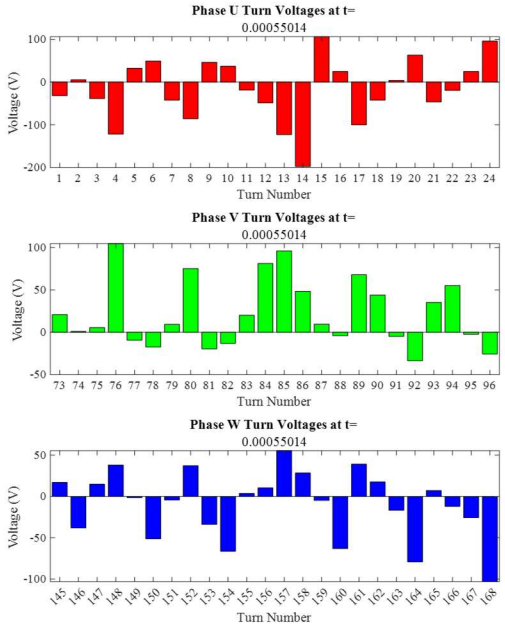

Figure 109. Turn voltages per phase at the time instant of maximum overall observed voltage stresses near t=0.55 ms (110 → 010)

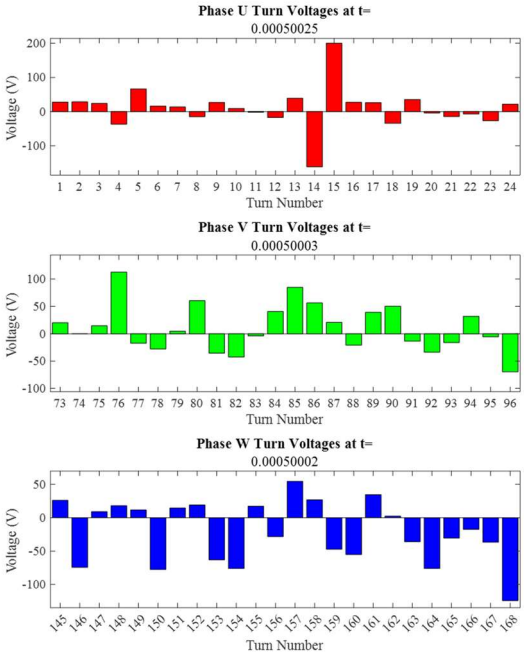

Figure 110. Turn voltages per phase at time instants near t=0.55 ms where the maximum turn voltage was observed (110 → 010)

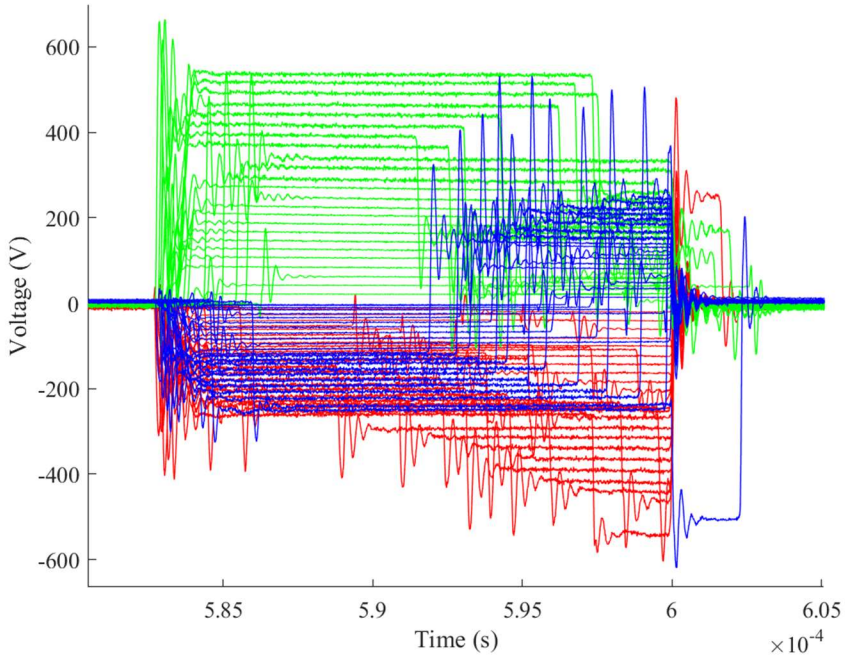

Figure 111. Aligned winding measurement point waveforms to t=0.6 ms (011 → 111)

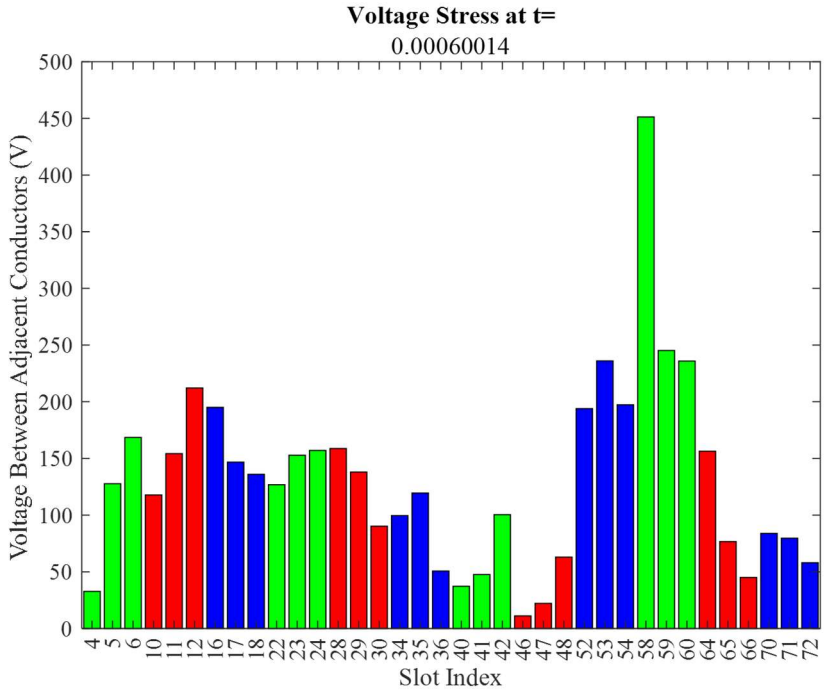

Figure 112. Maximum peak stress near t=0.6 ms (011 → 111)

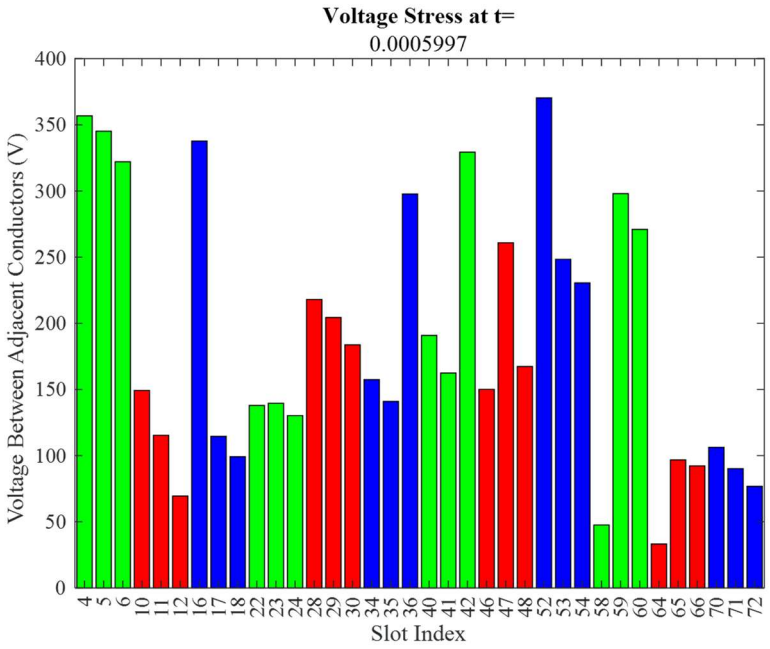

Figure 113. Maximum total stress near t=0.6 ms (011 → 111)

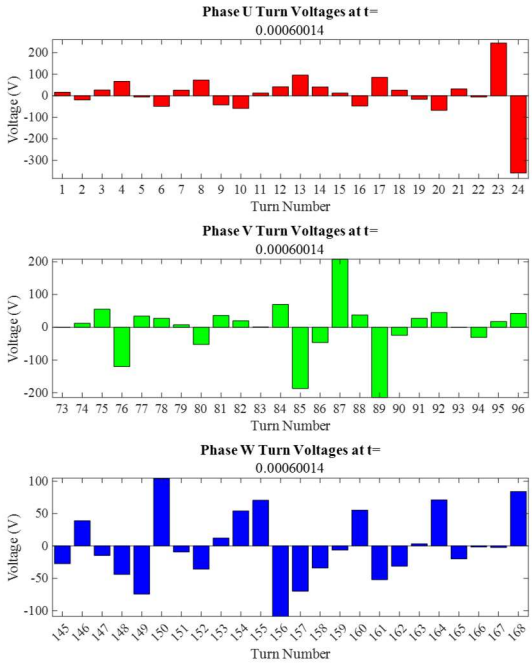

Figure 114. Turn voltages per phase at the time instant of maximum peak observed voltage stresses near t=0.6 ms (011 → 111)

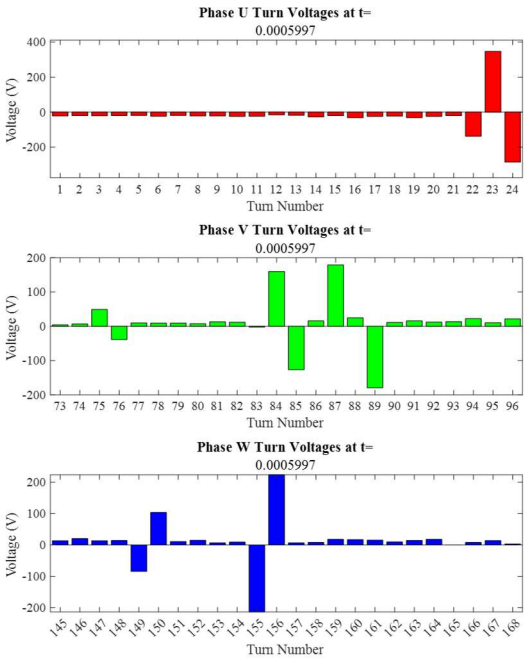

Figure 115. Turn voltages per phase at the time instant of maximum total observed voltage stresses near t=0.6 ms (011 → 111)

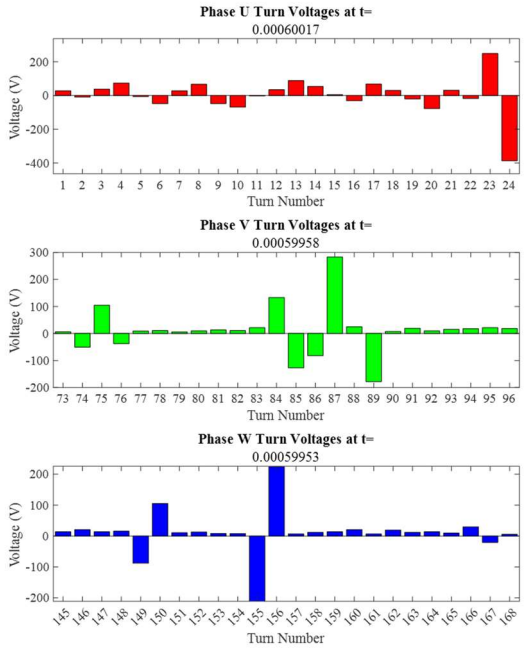

Figure 116. Turn voltages per phase at time instants near t=0.6 ms where the maximum turn voltage was observed (011 → 111)

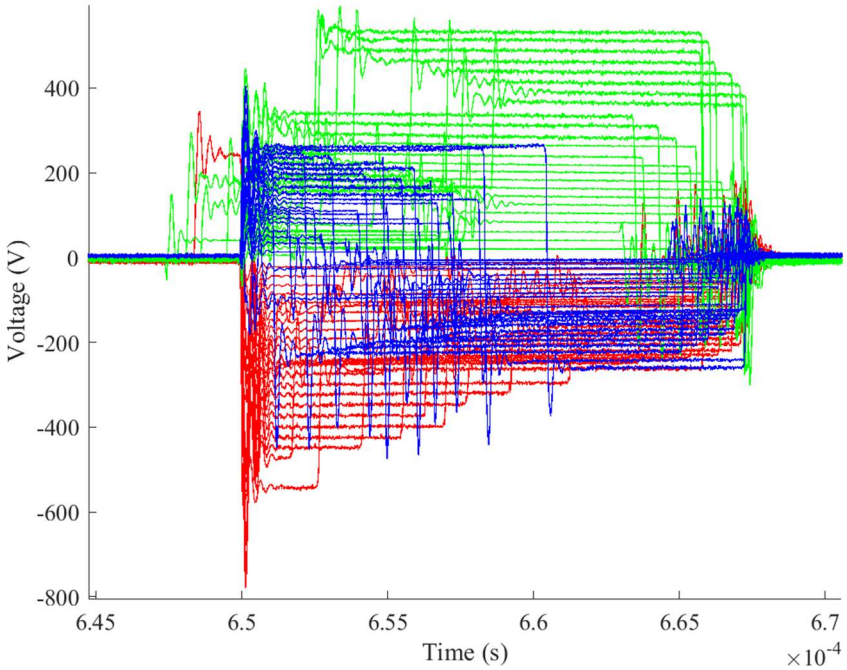

Figure 117. Aligned winding measurement point waveforms to t=0.65 ms (111 → 011)

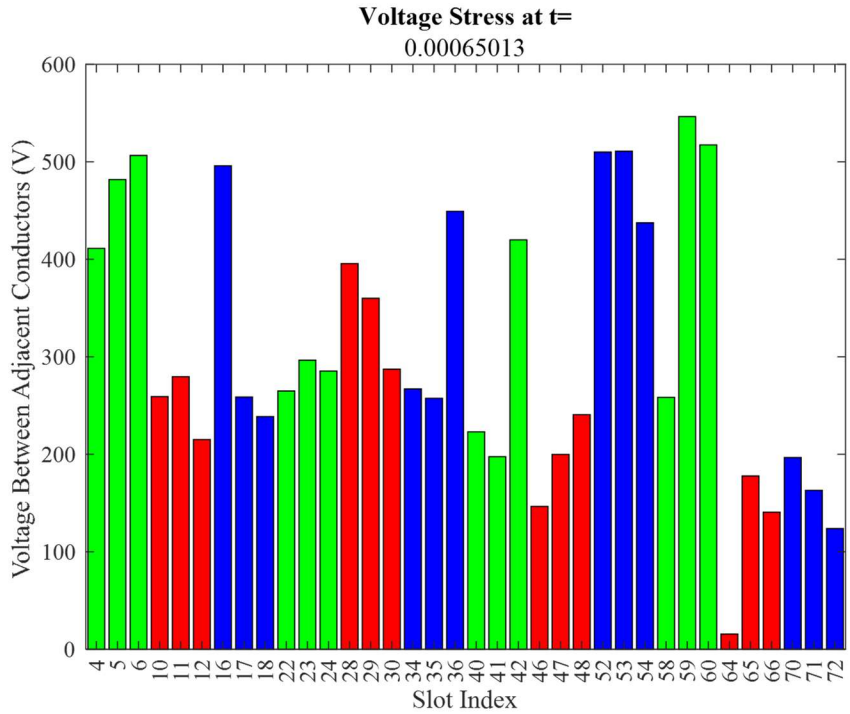

Figure 118. Maximum total and maximum peak stress near t=0.65 ms (111 → 011)

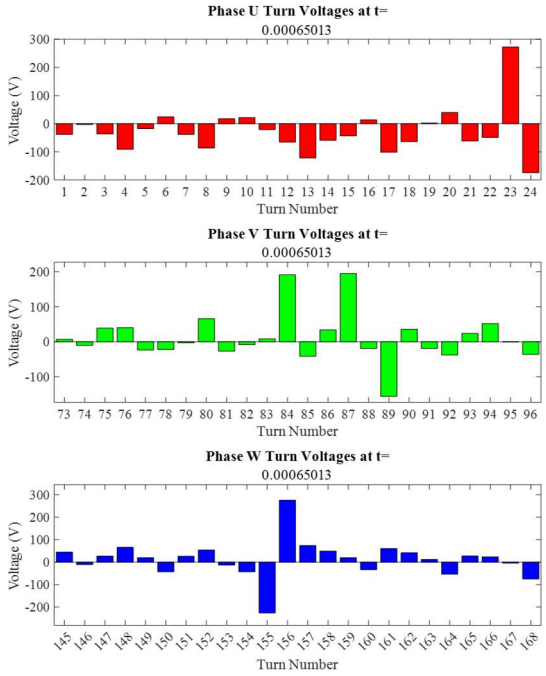

Figure 119. Turn voltages per phase at the time instant of maximum overall observed voltage stresses near t=0.65 ms (111 → 011)

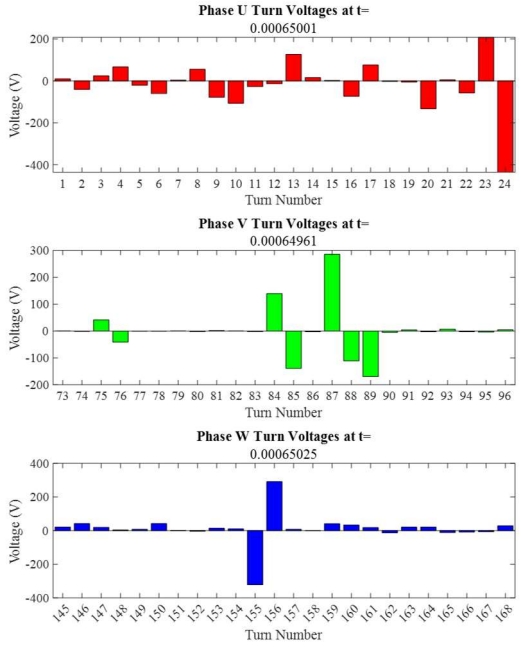

Figure 120. Turn voltages per phase at time instants near t=0.65 ms where the maximum turn voltage was observed (111 → 011)

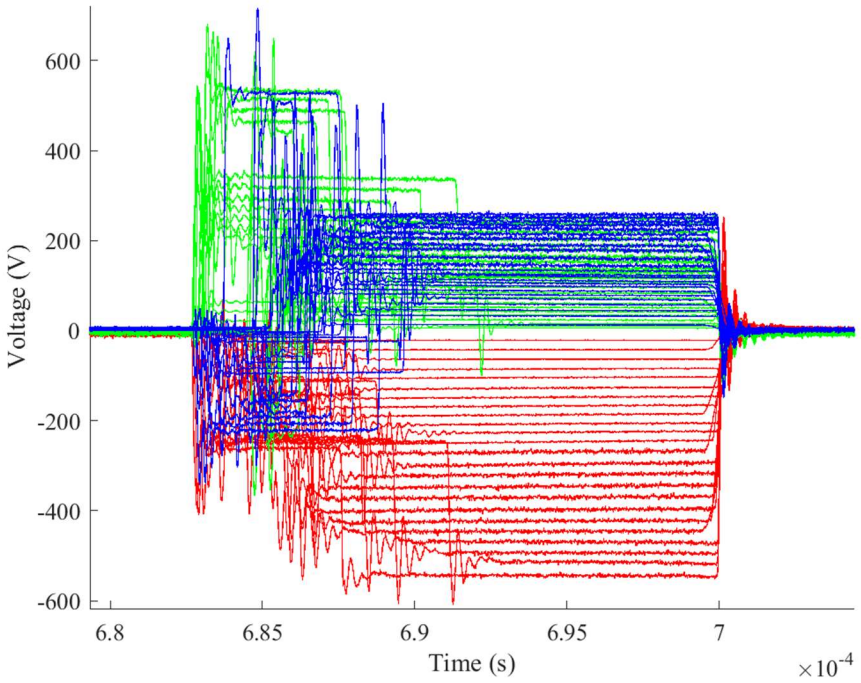

Figure 121. Aligned winding measurement point waveforms to t=0.7 ms (110 → 111)

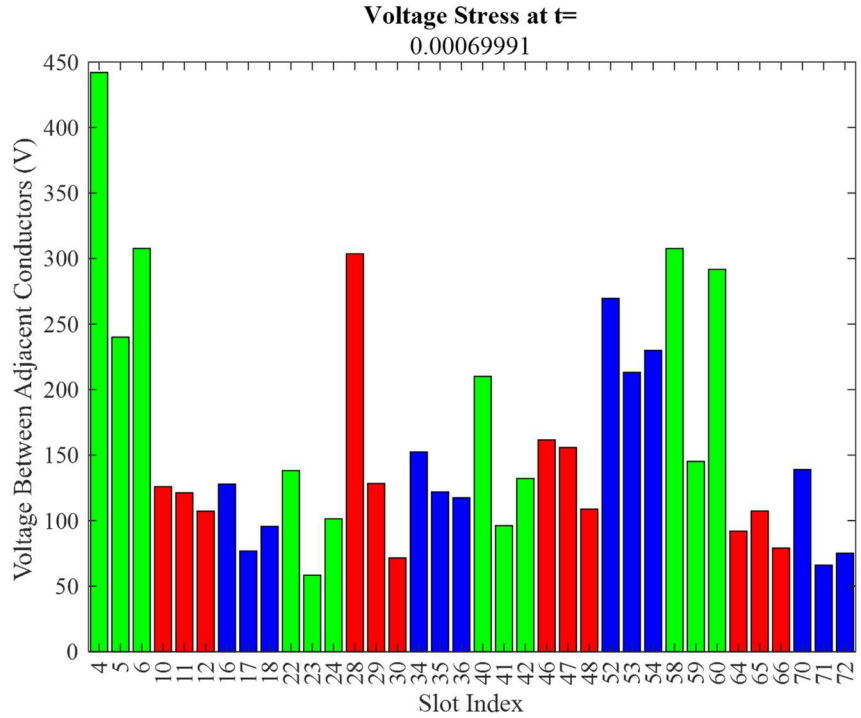

Figure 122. Maximum peak stress near t=0.7 ms (110 → 111)

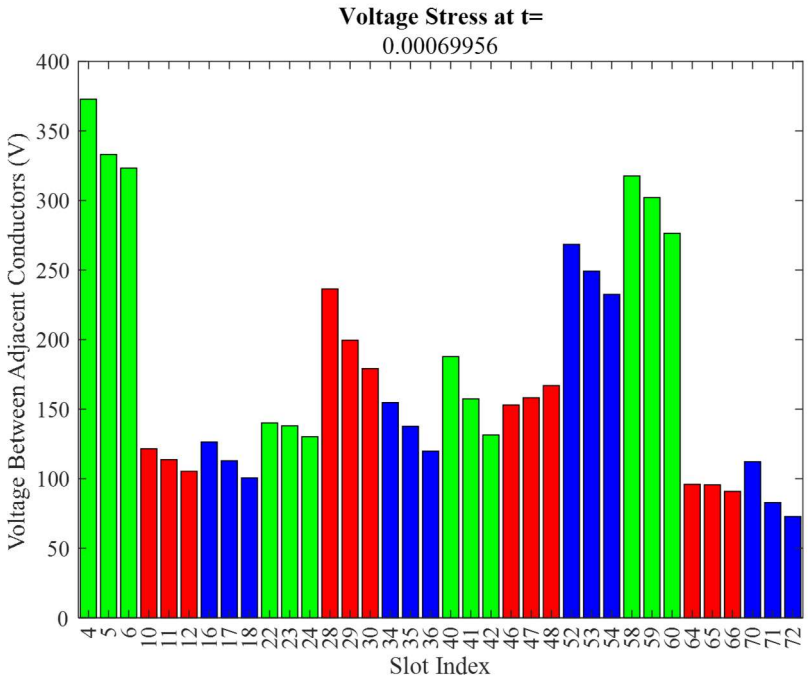

Figure 123. Maximum total stress near t=0.7 ms (110 → 111)

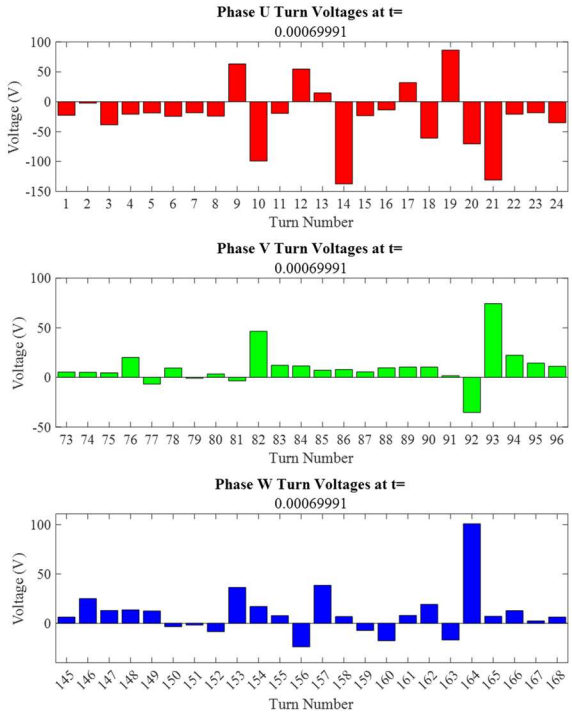

Figure 124. Turn voltages per phase at the time instant of maximum peak observed voltage stresses near t=0.7 ms (110 → 111)

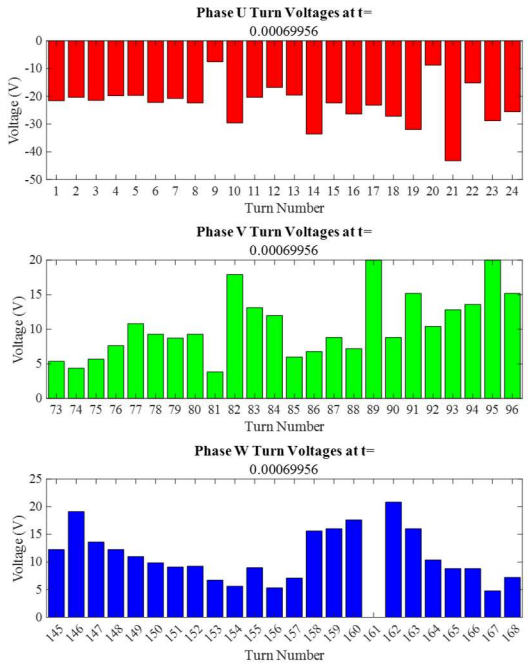

Figure 125. Turn voltages per phase at the time instant of maximum total observed voltage stresses near t=0.7 ms (110 → 111)

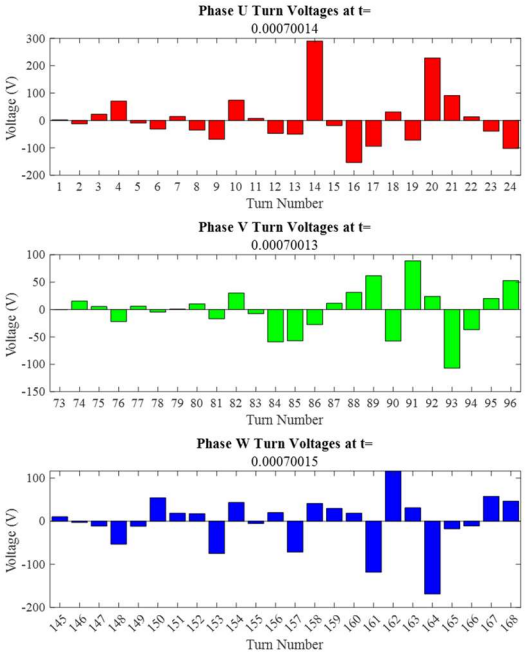

Figure 126. Turn voltages per phase at time instants near t=0.7 ms where the maximum turn voltage was observed (110 → 111)

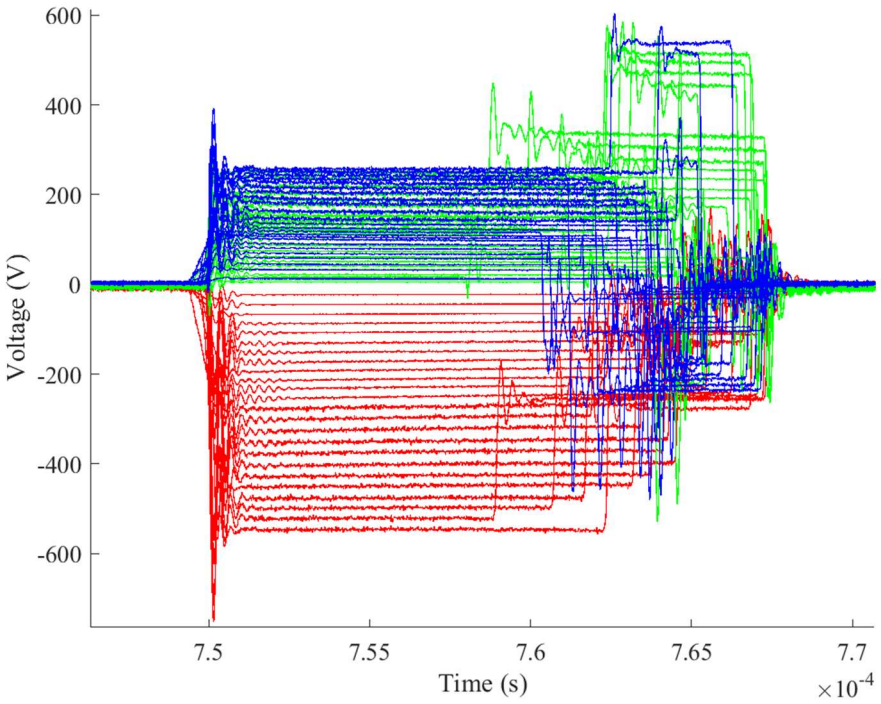

Figure 127. Aligned winding measurement point waveforms to t=0.75 ms (111 → 011)

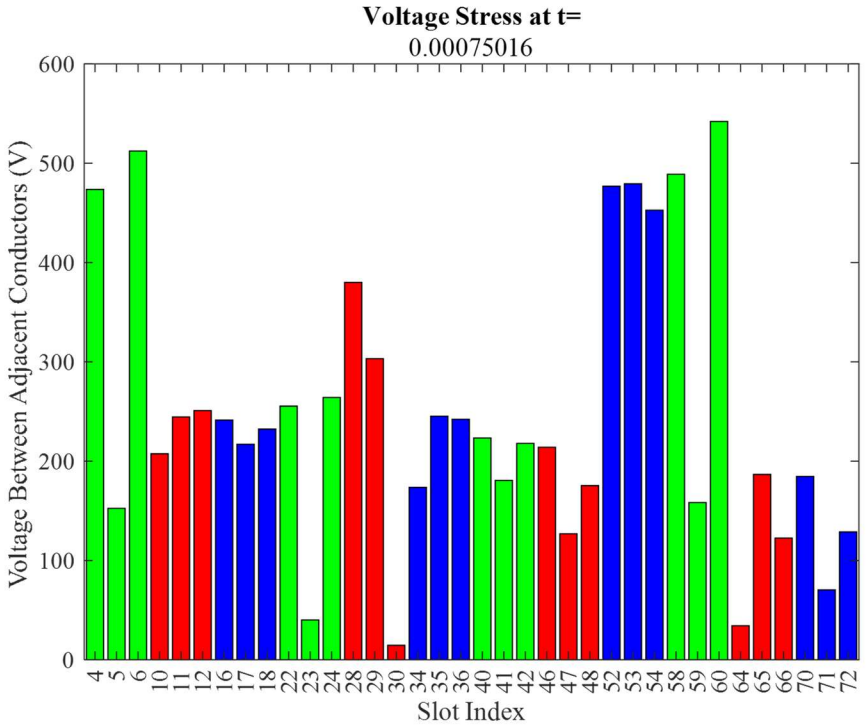

Figure 128. Maximum total and maximum peak stress near t=0.75 ms (111 → 011)

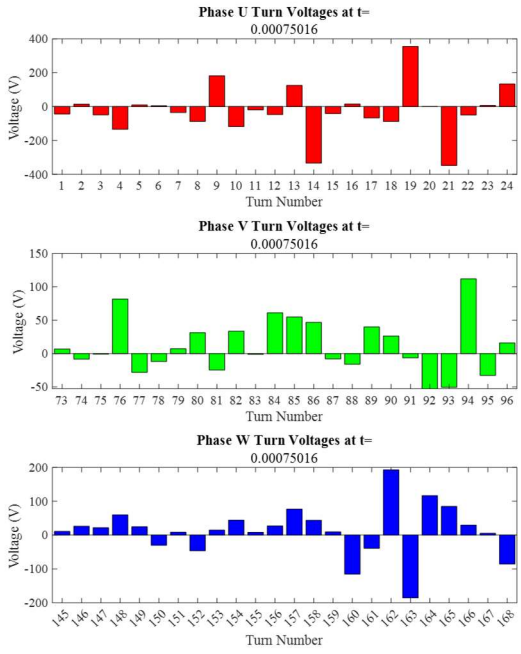

Figure 129. Turn voltages per phase at the time instant of maximum overall observed voltage stresses near t=0.75 ms (111 → 011)

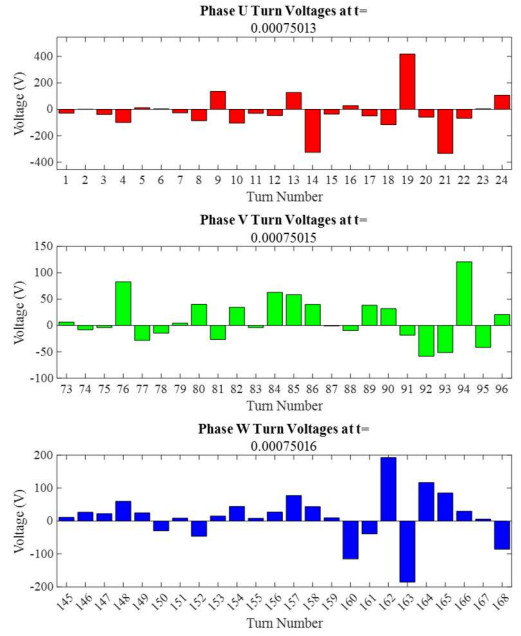

Figure 130. Turn voltages per phase at time instants near t=0.75 ms where the maximum turn voltage was observed (111 → 011)

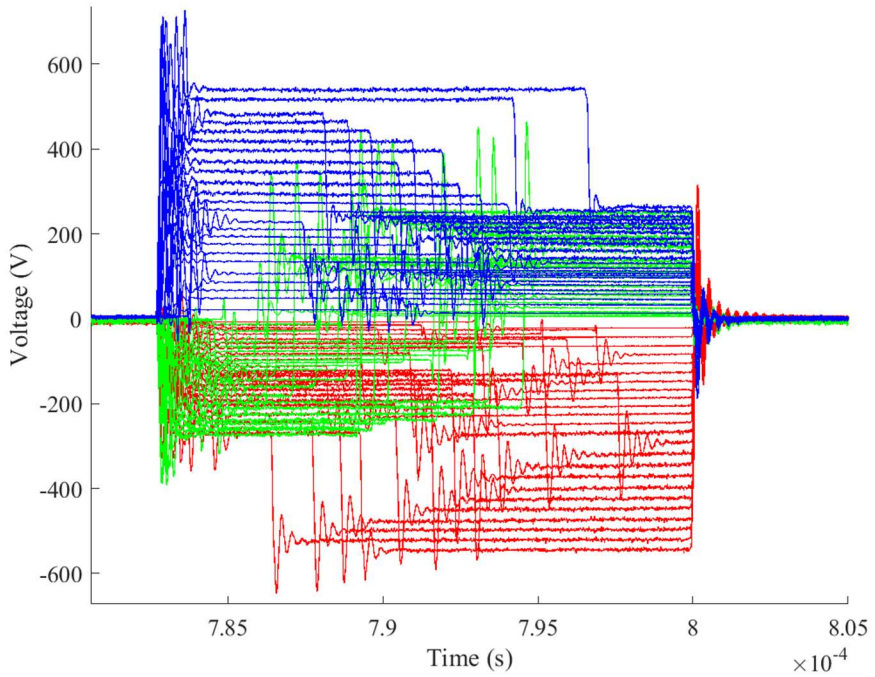

Figure 131. Aligned winding measurement point waveforms to t=0.8 ms (011 → 111)

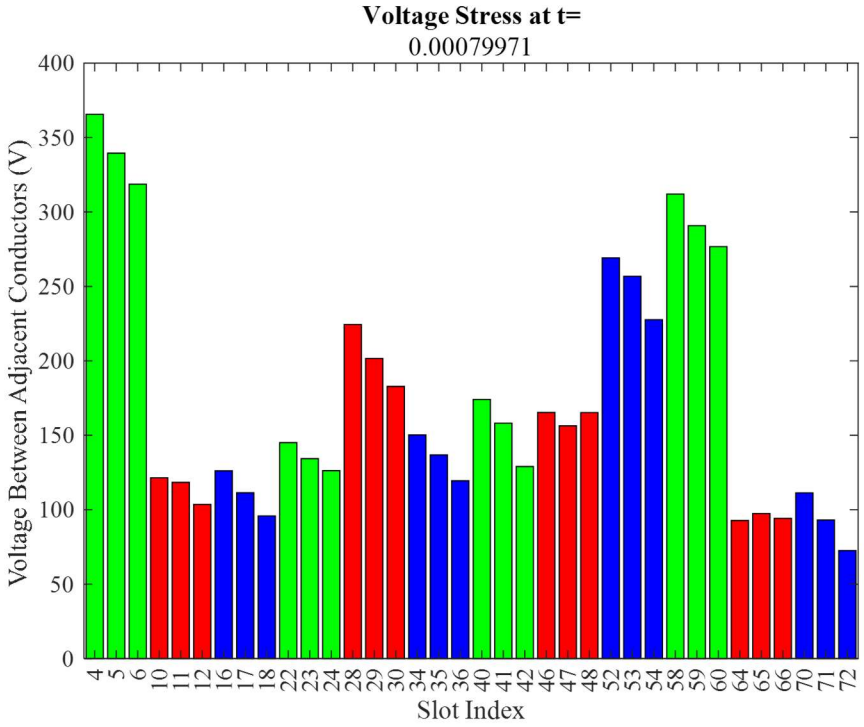

Figure 132. Maximum peak stress near t=0.8 ms (011 → 111)

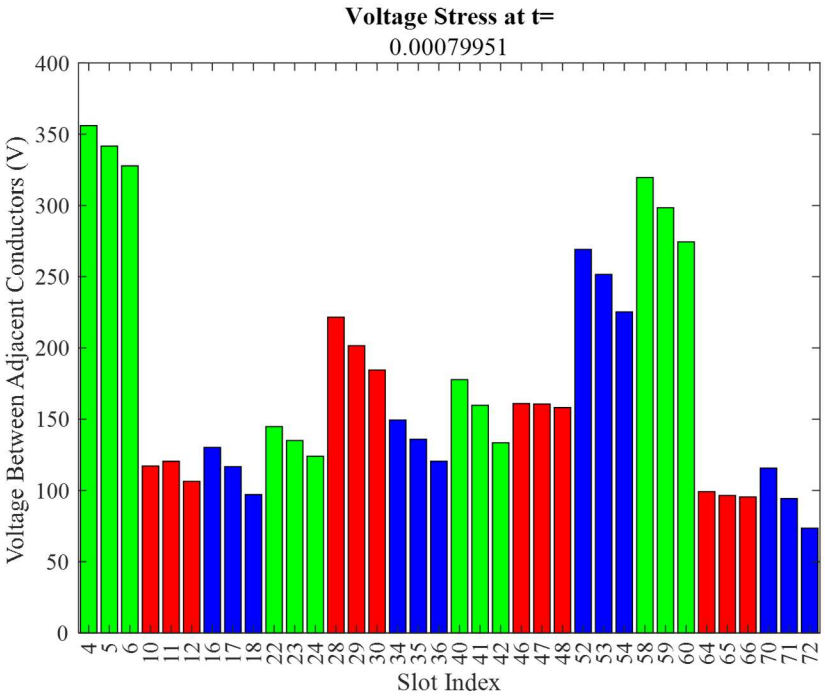

Figure 133. Maximum total stress near t=0.8 ms (011 → 111)

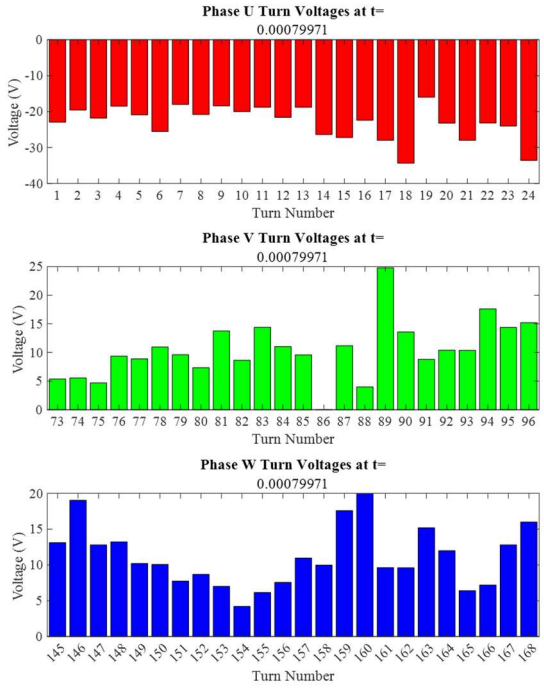

Figure 134. Turn voltages per phase at the time instant of maximum peak observed voltage stresses near t=0.8 ms (011 → 111)

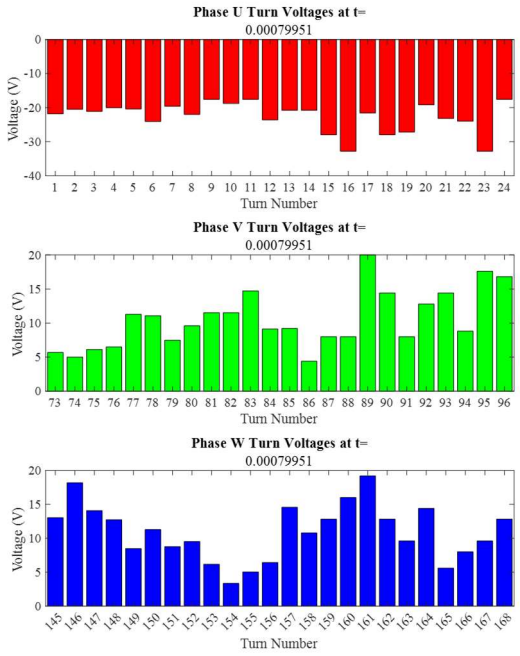

Figure 135. Turn voltages per phase at the time instant of maximum total observed voltage stresses near t=0.8 ms (011 → 111)

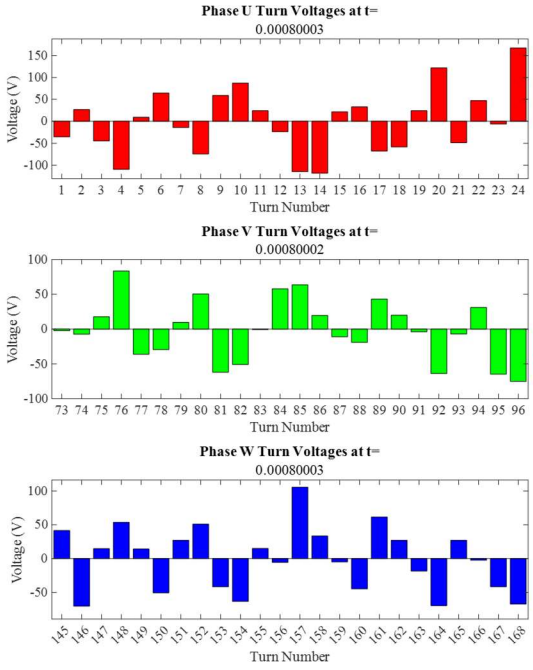

Figure 136. Turn voltages per phase at time instants near t=0.8 ms where the maximum turn voltage was observed (011 → 111)

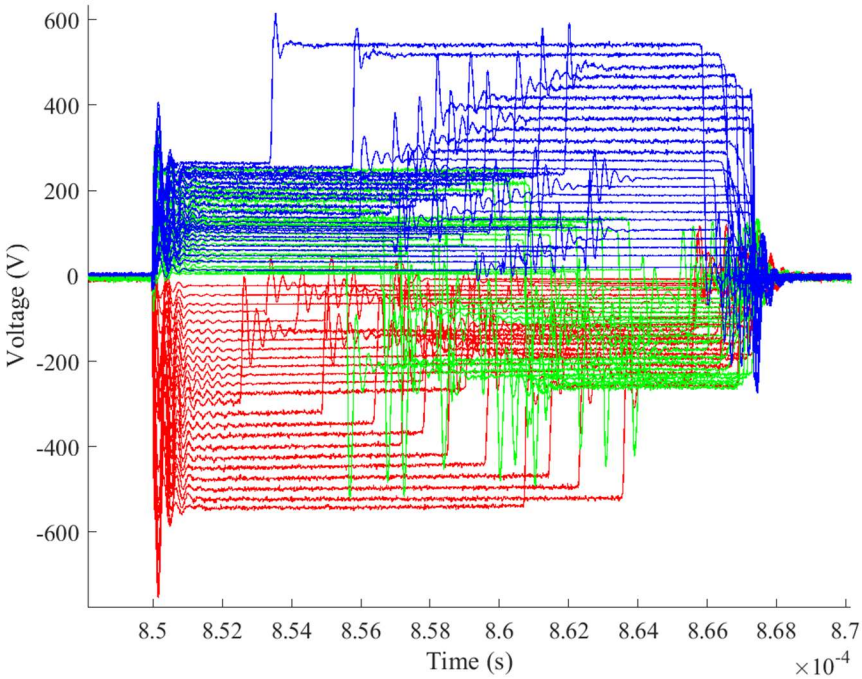

Figure 137. Aligned winding measurement point waveforms to t=0.85 ms (111 → 011)

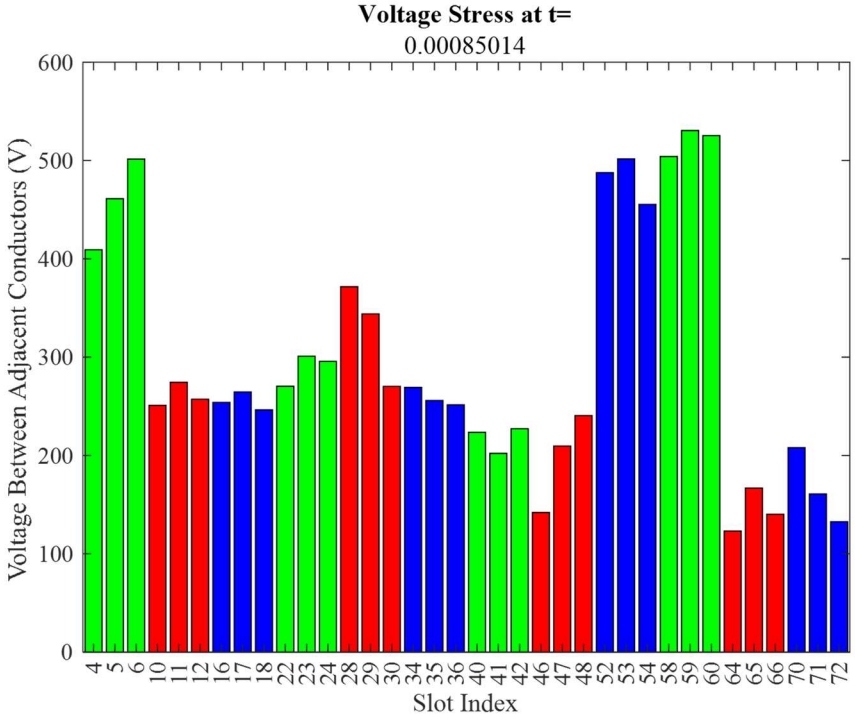

Figure 138. Maximum total and maximum peak stress near t=0.85 ms (111 □ 011)

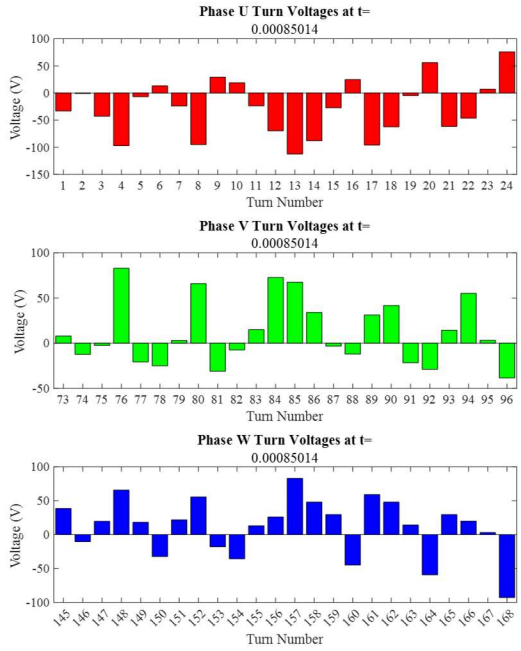

Figure 139. Turn voltages per phase at the time instant of maximum overall observed voltage stresses near t=0.85 ms (111 → 011)

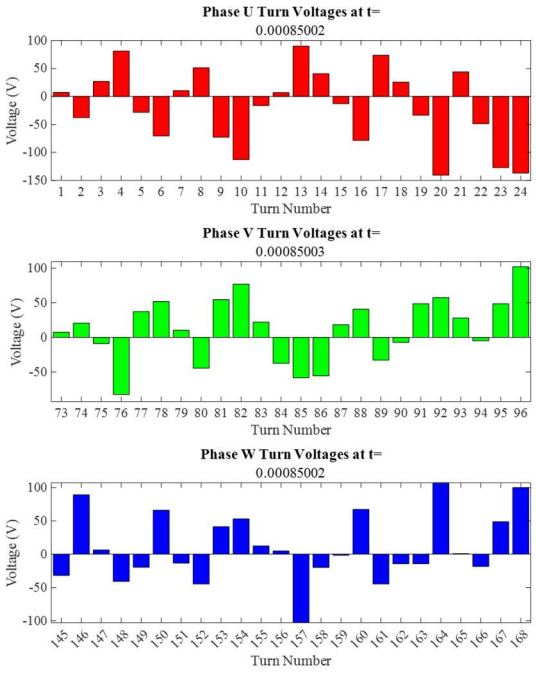

Figure 140. Turn voltages per phase at time instants near t=0.85 ms where the maximum turn voltage was observed (111 → 011)

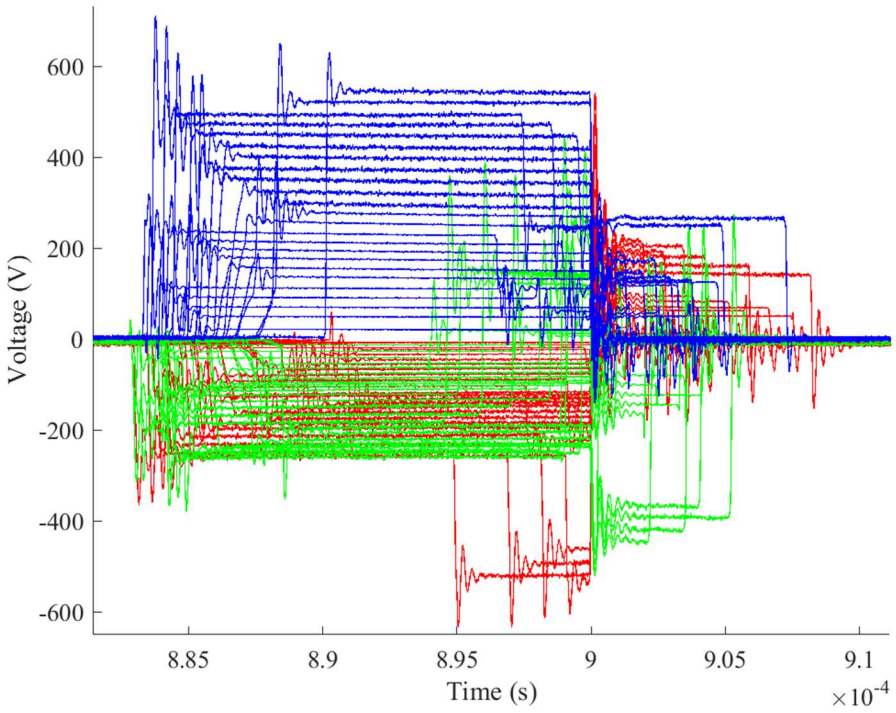

Figure 141. Aligned winding measurement point waveforms to t=0.9 ms (001 → 101)

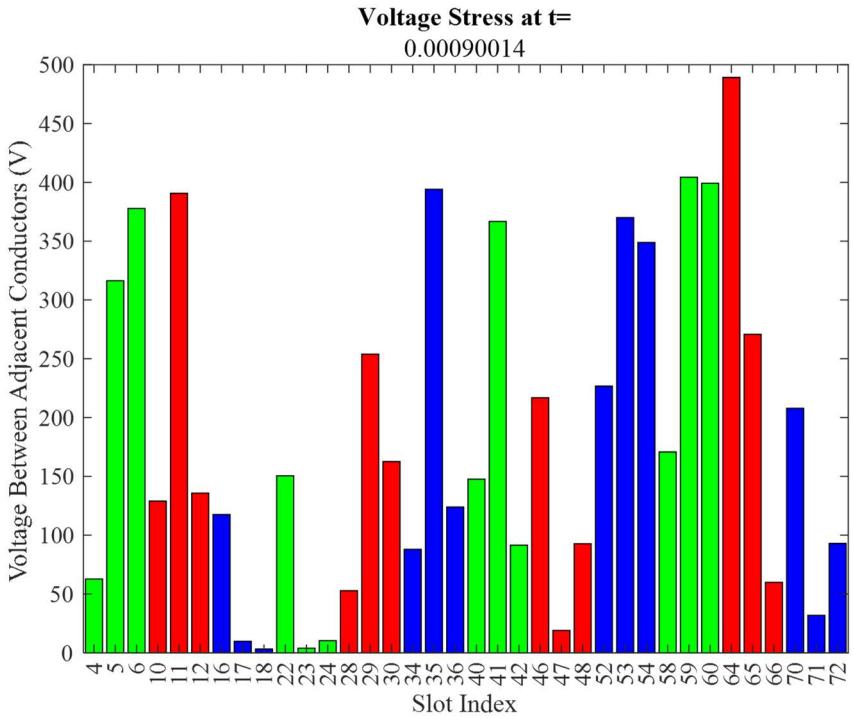

Figure 142. Maximum peak stress near t=0.9 ms (001 → 101)

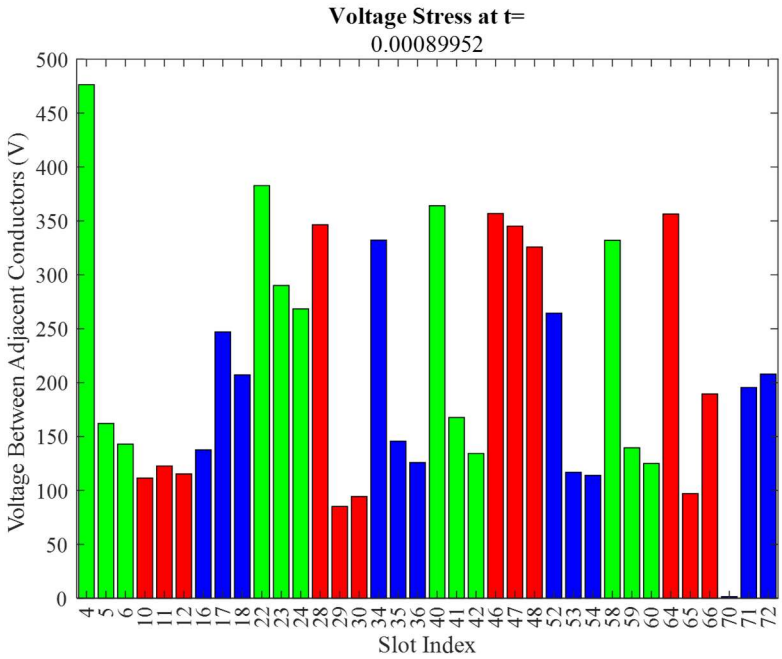

Figure 143. Maximum total stress near t=0.9 ms (001 → 101)

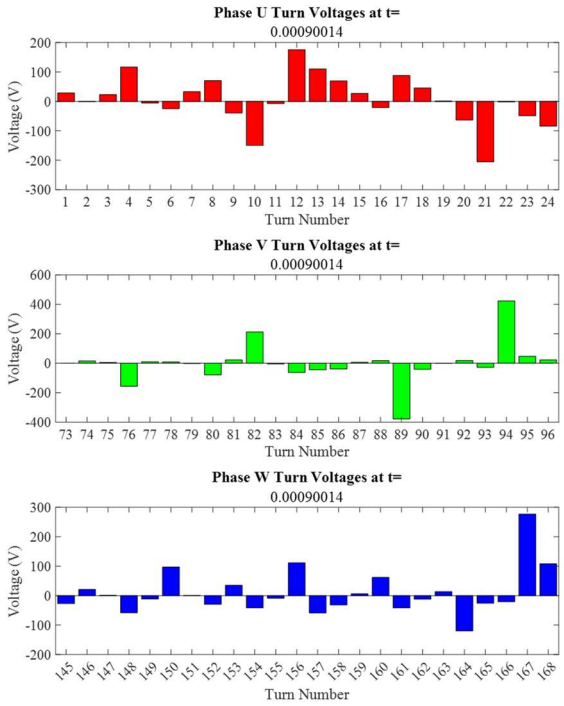

Figure 144. Turn voltages per phase at the time instant of maximum peak observed voltage stresses near t=0.9 ms (001 → 101)

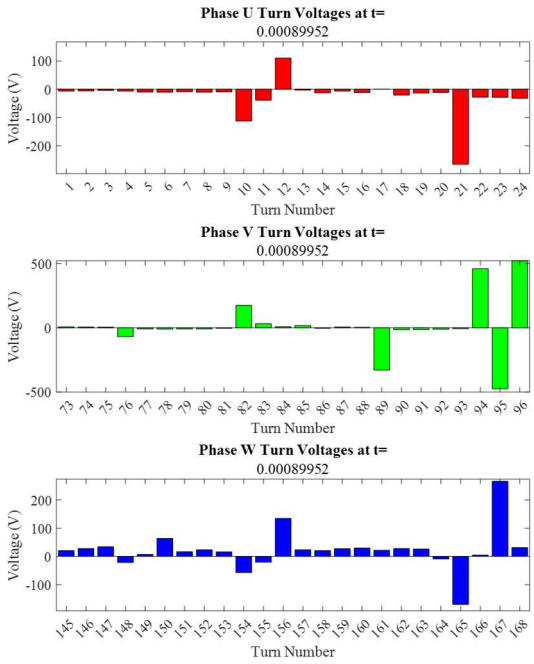

Figure 145. Turn voltages per phase at the time instant of maximum total observed voltage stresses near t=0.9 ms (001 → 101)

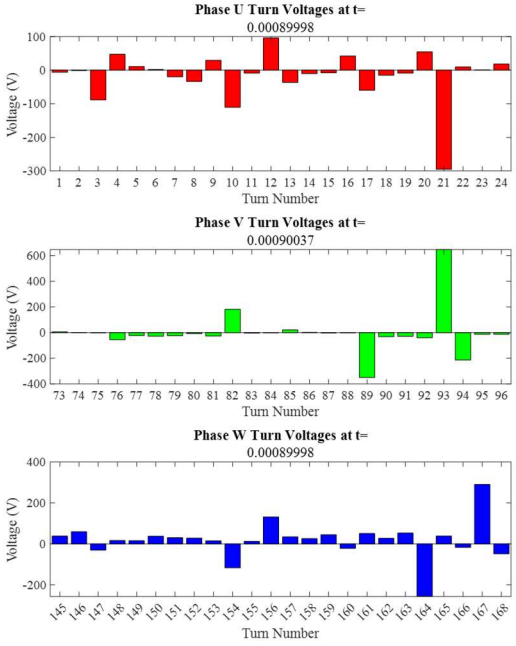

Figure 146. Turn voltages per phase at time instants near t=0.9 ms where the maximum turn voltage was observed (001 → 101)

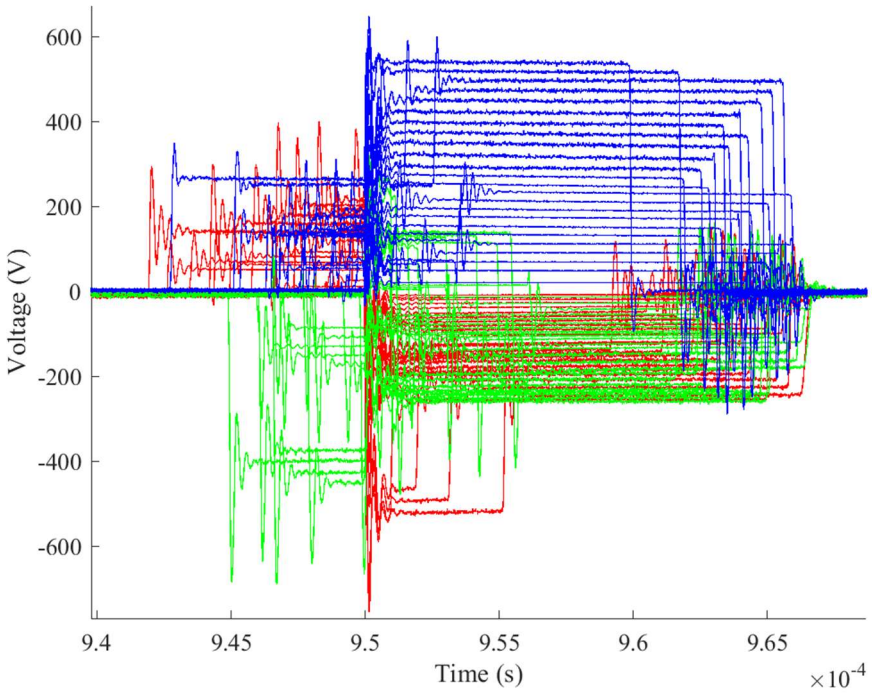

Figure 147. Aligned winding measurement point waveforms to t=0.95 ms (101 → 001)

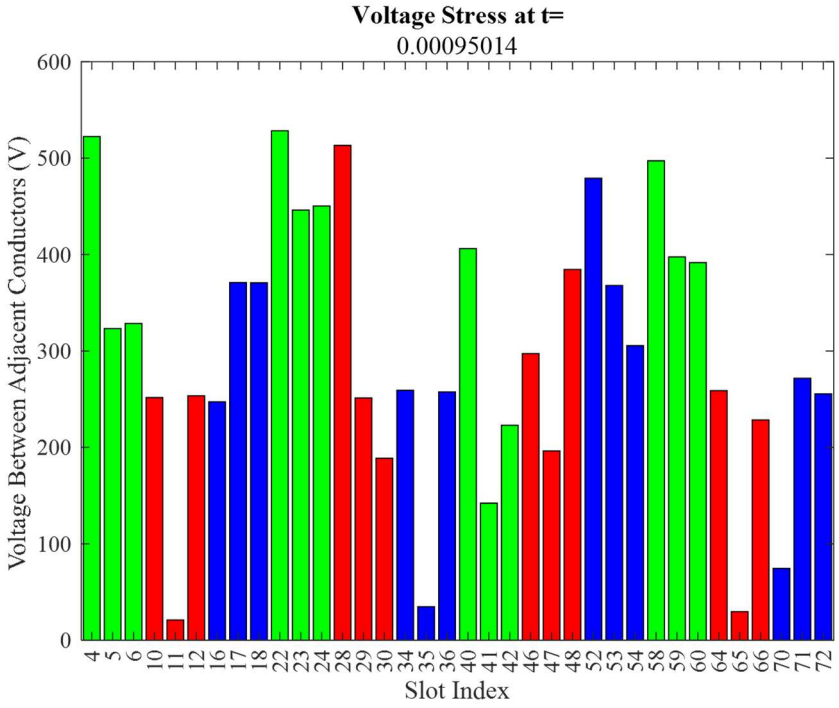

Figure 148. Maximum total and maximum peak stress near t=0.95 ms (101 → 001)

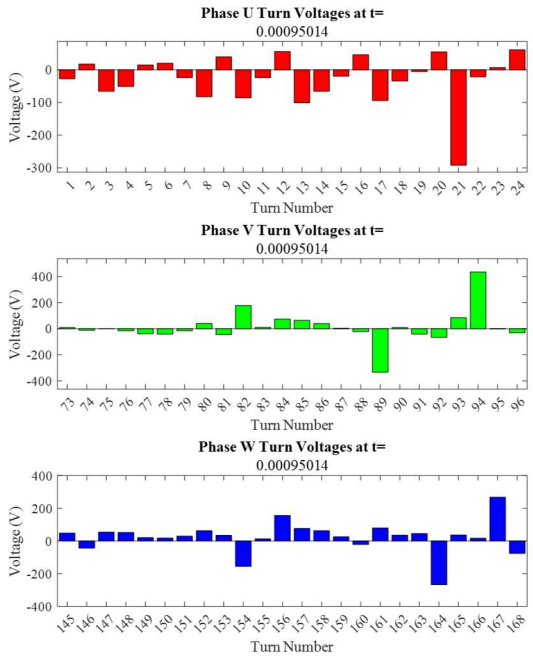

Figure 149. Turn voltages per phase at the time instant of maximum overall observed voltage stresses near t=0.95 ms (101 → 001)

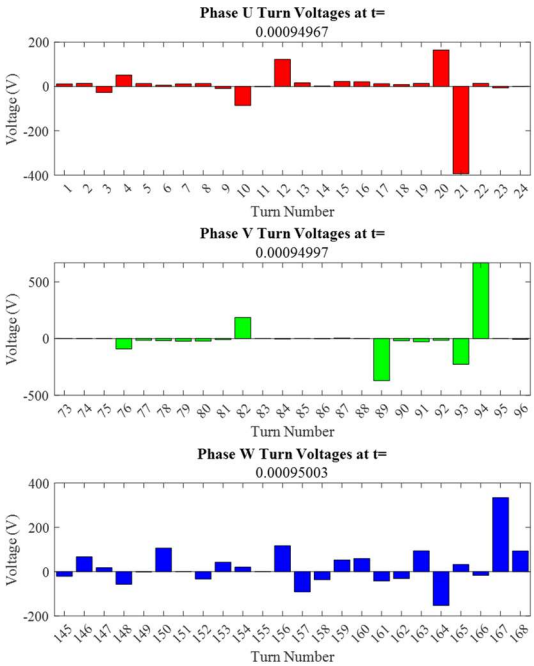

Figure 150. Turn voltages per phase at time instants near t=0.95 ms where the maximum turn voltage was observed (101 → 001)