Power Module Design and Protection for Medium Voltage Silicon Carbide Devices

DISSERTATION

Presented in Partial Fulfillment of the Requirements for the Degree Doctor of Philosophy in the Graduate School of The Ohio State University

By

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The Ohio State University

2020

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Abstract

Silicon Carbide (SiC) power devices become popular in electric/hybrid vehicles, energy storage power converters, high power industrial converters, locomotive traction drives and electric aircrafts. Compared with its silicon counterparts, SiC metal oxide semiconductor field effect transistors (MOSFETs) feature higher blocking voltage, higher operating temperature, higher thermal conductivity, faster switching speed, and lower switching loss. This dissertation studies the medium voltage SiC power switch design, packaging, reliability testing and protection, aiming to achieve high power density low cost design with improved reliability.

This work first investigates medium voltage SiC MOSFET short circuit capability and degradation under short circuit events. Lower short circuit energy is an effective approach to protect the medium voltage SiC MOSFET from catastrophic failure and slow down the device degradation under repeated over-current conditions. To ensure high efficiency operation under normal conditions and effective protection under short circuit condition, a three-step short circuit protection method is proposed. With ultra-fast detection, the protection scheme can quickly respond to the short circuit events and actively lower the device gate voltage to enhance its short circuit capability. Eventually, the conventional desaturation protection circuits confirm the faulty condition and softly turns off the device. Based on the 3300 V SiC MOSFET characteristic and circuit parameters, the protection circuit design guideline is provided.

The exploration on the medium voltage SiC MOSFET packaging follows. To further increase the power density, the medium voltage SiC device packaging becomes a multi-disciplinary subject involving electrical, thermal, and mechanical design. Multi-functional package components are desired to deal with more than one concerns in the application. The relationship between electrical, thermal, and mechanical properties needs to be understood and carefully designed to achieve a fully integrated high-performance power module. The adoption of ceramic baseplate is assessed in the aspects of the insulation design, the thermal design, the power loop layout, the electromagnetic interference considerations, respectively. Mathematical models, simulations, and experimental results are presented to verify the analysis.

The adoption of the medium voltage SiC MOSFETs in the various application is slowed by its unclear long-term reliability and high cost. The reliability issue can be mitigated by the aforementioned three-step protection method. An economic alternative for medium voltage power switch is the super-cascode structure. The super-cascode structure is composed of series connected low voltage MOSFET and normally-on junction gate field-effect transistors (JFETs). The voltage balancing among series connected devices is realized by the added capacitors and diodes. Circuit models during the switching transients are built. Based on the developed models, a method to optimize the voltage balancing circuit parameters is proposed. The analysis and optimization method are verified by the experimental results. Sensitivity analysis is conducted to see the impact of the capacitance tolerance.

Conclusions and recommendations for future work are presented at the end of this dissertation.

Dedication

This document is dedicated to my family.

Acknowledgments

I would like to express my sincere gratitude for my advisor, Prof. Jin Wang, for his guidance, encouragements, trust, and support during this journey. His extensive knowledge, broad vision and creative thinking have been a source of inspiration for me throughout the years. His attitude and dedication to work is so valuable for my pursuing the future career. Without his support and guidance, I would never reach this far.

My thanks also go to the committee members: Prof. Longya Xu, Prof. Anat Agarwal, Prof. Vadim I. Utkin, and Prof. Ahmet Selamet for their support, advice, and directions.

I would also like to thank the NASA ULI team on the electric propulsion, Dr. Meyer Benzakein, Ms Vera Fosnot, Prof. Thomas Jahns, Prof. Bulent Sarlioglu, Prof. Julia Zhang, Prof. Mahesh Illindala, Prof. Patrick McCluskey, Prof. John Kizito, Mr. Christopher Perullo, Mr. Hao Zeng, Mr. Zhaoxi Yao, Mr. Jason Robinson and Mr. Walt Vancleave, for their guidance and support during my Ph.D. study.

I also want to thank Dr. Liming Liu, Dr. Jing Xu and Dr. Sandeep Bala at ABB Corporate Research Center, Dr. Larry Li at United Silicon Carbide.

Thanks to Ms. Xiaodan Wang for being my best support in both life and work throughout these years. Thanks to Dr. Feng Guo, Dr. Xuan Zhang, Dr. Chengcheng Yao, Dr. Cong Li, Dr. Mark Scott, Mr. Lixing Fu, Dr. Xiu Yao, Dr. Luis Herrera, Dr. Boxue Hu, Ms. Gengyao Li, Dr. Karun Potty, Dr. Yousef Abdullah, Mr. Zhuo Wei, Mr. Diang Xing, Mr. Bailey Hall, Mr. Haoyang You, Mr. Rob Bojas, Mr. Jamie Shaffer, for accompanying

me over the years as both close friends and colleagues. I also cherish the help, and friendship from all CHPPE alumni and students, including but not limited to Mr. Jinzhu Li, Mr. Da Jiao, Mr. Fanbo Zhang, Mr. Andong Lang, Dr. Linyu Zhu, Mr. Pengzhi Yang, Ms. Chaoran Han, Mr. Ke Zhu, Mr. Mingzhi Leng, Mr. Eric Bauer, Mr. Zhengda Zhang, Mr. Yue Zhang, Ms. Huanyu Chen, Dr. Zhendong Zhang, Dr. Thomas Tsai, Ms. Pu Xu, Mr. Cong Deng, Dr. Dakai Hu, Dr. Haiwei Cai, Dr. Miao Wang, Dr. Jianyu Pan, Dr. Feng Qi, Mr. Rachid Darbali Zamora, Mr. Ernest Davidson, Dr. Chen Yuan, Dr. Risha Na, Mr. Khalid Alkhalid, Mr. Faisal Alsaif, Mr. Zhuxuan Ma, Mr. Xingyue Tian, Mr. Jiawei Liu, Ms. Niu Jia, Mr. Junchong Fan, Mr. Ke Wang, Ms. Xiao Li, Mr. Yizhou Cong, Mr. Nihanth Adina for sharing this journey at the Ohio State University. Thank you all for those joys and shared memories. I will not forget all the days I was embraced by your friendship, help and support.

I own my deepest gratitude to my parents Mr. Juntang Lyu and Ms. Linfang Li, my brother Mr. Jiyuan Lyu, my aunt Ms. Meizhen Lyu, my uncle Ming Yan, my husband Dr. He Li, and my parents-in-law Zhongqiang Li and Mei He. Without your love and support, I would not have been where I am today.

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Publications

[1] X. Lyu, H. Li, Y. Abdullah, K. Wang, B. Hu, Z. Yang, J. Liu, J. Wang, L. Liu and S. Bala, "A Reliable Ultrafast Short-Circuit Protection Method for E-Mode GaN HEMT," in IEEE Transactions on Power Electronics, vol. 35, no. 9, pp. 8926-8933, Sept. 2020.

[2] X. Lyu, H. Li, Z. Ma, B. Hu and J. Wang, "Dynamic Voltage Balancing for the High-Voltage SiC Super-Cascode Power Switch," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 7, no. 3, pp. 1566-1573, Sept. 2019.

[3] B. Hu, X. Lyu, D. Xing, D. Ma, J. Brothers, R. Na and J. Wang, "A Survey on Recent Advances of Medium Voltage Silicon Carbide Power Devices," 2018 IEEE Energy Conversion Congress and Exposition (ECCE), Portland, OR, 2018, pp. 2420-2427.

[4] X. Lyu, H. Li, B. Hu, Z. Ma and J. Wang, "High voltage SiC super-cascode power switch parameter optimization for loss reduction," 2018 IEEE Applied Power Electronics Conference and Exposition (APEC), San Antonio, TX, 2018, pp. 1701-1705.

[5] X. Lyu, H. Li, Y. Abdullah, K. Wang, B. Hu, Z. Yang, J. Wang, L. Liu and S. Bala, "A Reliable Ultra-Fast Three Step Short Circuit Protection Method for E-mode GaN

HEMTs," 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), Anaheim, CA, USA, 2019, pp. 437-440.

[6] H. Li, X. Li, X. Wang, X. Lyu, H. Cai, Y. Alsmadi, L. Liu, S. Bala and J. Wang, "Robustness of 650-V Enhancement-Mode GaN HEMTs Under Various Short-Circuit Conditions," in IEEE Transactions on Industry Applications, vol. 55, no. 2, pp. 1807-1816, March-April 2019.

[7] X. Lyu, H. Li, Z. Ma, B. Hu and J. Wang, "Optimization Method to Eliminate Turn-on Overvoltage Issue of the High Voltage SiC Super-Cascode Power Switch," 2018 IEEE 4th Southern Power Electronics Conference (SPEC), Singapore, Singapore, 2018, pp. 1-6.

[8] H. You, H. Li, X. Lyu, Z. Wei, B. Hu and J. Wang, "Design of a PWM-type Bipolar Pulse Generator with High Dv/dt Output," 2018 1st Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia), Xi'an, China, 2018, pp. 220-225.

[9] H. Li, X. Lyu, K. Wang, Y. Abdullah, B. Hu, Z. Yang, J. Wang, L. Liu and S. Bala, "An Ultra-Fast Short Circuit Protection Solution for E-mode GaN HEMTs," 2018 1st Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia), Xi'an, China, 2018, pp. 187-192.

[10] X. Lyu, X. Tian, H. Li, H. You and J. Wang, "Design of a Lightweight Low Inductance Power Module with Ceramic Baseplates," 2020 IEEE Applied Power Electronics Conference and Exposition (APEC), New Orleans, LA, USA, 2020, pp. 2782-2787.

[11] L. Fu, X. Zhang, H. Li, X. Lu and J. Wang, "The development of a high-voltage power device evaluation platform," 2014 IEEE Workshop on Wide Bandgap Power Devices and Applications, Knoxville, TN, 2014, pp. 13-17.

[12] L. Fu, H. Li, X. Lu and J. Wang, "Overview and evaluation methodologies of high voltage power devices," 2014 IEEE International Power Modulator and High Voltage Conference (IPMHVC), Santa Fe, NM, 2014, pp. 546-549.

[13] F. Guo, L. Herrera, M. Alsolami, H. Li, P. Xu, X. Lu, A. Lang, J. Wang and Z. Long, "Design and development of a reconfigurable hybrid Microgrid testbed," 2013 IEEE Energy Conversion Congress and Exposition, Denver, CO, 2013, pp. 1350-1356.

[14] F. Guo, H. Li, C. Yao, M. Alsolami, A. Lang, X. Lu and J. Wang, "Residential usage profile optimization and experimental implementation of the retired HEV battery with a hybrid microgrid testbed," 2014 IEEE Energy Conversion Congress and Exposition (ECCE), Pittsburgh, PA, 2014, pp. 428-435.

[15] M. J. Scott, E. Davidson, C. Li, R. Duarte, X. Lu, T. Chen, F. Guo, J. Wang and R. Darbali-Zamora, "Bidirectional, three-port, three-phase multilevel inverter based on switched-capacitor cells," 2013 IEEE Energy Conversion Congress and Exposition, Denver, CO, 2013, pp. 3057-3061.

[16] C. Li, D. Jiao, M. Scott, C. Yao, L. Fu, X. Lu, T. Chen, J. Li and J. Wang, "A 2 kW Gallium Nitride based switched capacitor three-port inverter," The 1st IEEE Workshop on Wide Bandgap Power Devices and Applications, Columbus, OH, 2013, pp. 119-124.

[17] X. Zhang, C. Yao, X. Lu, E. Davidson, M. Sievers, M. Scott, P. Xu and J. Wang, "A GaN transistor based 90W AC/DC adapter with a buck-PFC stage and an isolated Quasi-switched-capacitor DC/DC stage," 2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014, Fort Worth, TX, 2014, pp. 109-116.

Fields of Study

Major Field: Electrical and Computer Engineering

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Chapter 1. Introduction

1.1. State of Medium Voltage Silicon Carbide Device Technology

Compared with silicon (Si), silicon carbide (SiC) material has about three times energy gap, six times breakdown electric field strength and three times thermal conductivity. Silicon carbide power electronic semiconductor have emerged and commercialized with the advantages for high voltage, high frequency, and high temperature applications. Early demonstration of kilo watt-level megahertz frequency operated bipolar junction power transistors is reported in [1]. By continuously solving and improving the manufacturing issues and defects, the SiC power semiconductors are in various research and early mass production. The commercialized SiC power devices include, but not limited to, PiN diodes, Schottky barrier diodes, metal-oxide-semiconductor field effect transistors (MOSFETs), junction gate field effect transistors (JFETS), and super junction transistors (SJT). At the same time, the research community starts to look at the next generation semiconductor structure and materials, including but not limited to 6.5 kV super cascode SiC JEFT, 10 kV SiC junction barrier Schottky diodes [2], 10 kV and above SiC MOSFET [3]-[6], 10 kV and above SiC IGBT [6]-[7], and 15 kV SiC emitter turn-off transistor (ETO) [8]-[9], 15 kV SiC gate turn-off transistor (GTO) [10], and the next generation ultra-wide bandgap (UWBG) materials based devices. The UWBG materials have bandgaps significantly wider than that of 3.26 eV SiC and 3.44 GaN eV. For example, quasi-vertical AlN/AlGaN based heterostructure have been demonstrated in recent years with superior performance in certain aspects [11].

Compared to Si power devices, SiC power devices exhibit superior advantages at the following four major aspects. First, intrinsic carrier concentration for Si material is about 1.4×10^{10} /cm^3 at room temperature. The intrinsic carrier concentration of SiC material is 2.5×10^{-10} /cm^3, which is 10^{20} times lower than the Si material. Low intrinsic carrier concentration, as well as the high energy bandgap, allow for high temperature operation since the leakage current is much lower at elevated temperature. Secondly, the critical electric field of SiC material is about 6.6 times of that of Si material over a wide range of doping concentration. Higher critical electric field leads to higher blocking voltage of the packaged device, and higher blocking voltages can simplify converter circuit design with a smaller number of series connected devices, less gate drive circuits, less isolated power supply circuits. The design, testing, manufacturing, installment, and maintenance benefit from simpler converter design. Thirdly, higher electron saturation velocity leads to higher switching speed. This characteristic not only reduces the device switching loss, but also make high frequency converter operation possible. With higher operation frequency, the passive components, capacitors and inductors, could have smaller volume and weight. The converter power density can be further improved. The fourth advantage is the high thermal conductivity. Higher thermal conductivity enhances the heat spreading and benefit thermal management of the packaged device.

SiC devices are now competing with Si IGBTs and MOSFETs in high voltage high power applications with device voltage ratings higher or equal to 1,200 V. In general, SiC devices are changing the landscape of power electronic industry with accelerated speed.

Their merits create new application as well as renovate the existing solutions. In the coming decade, SiC based power transistors will take a huge portion of the market.

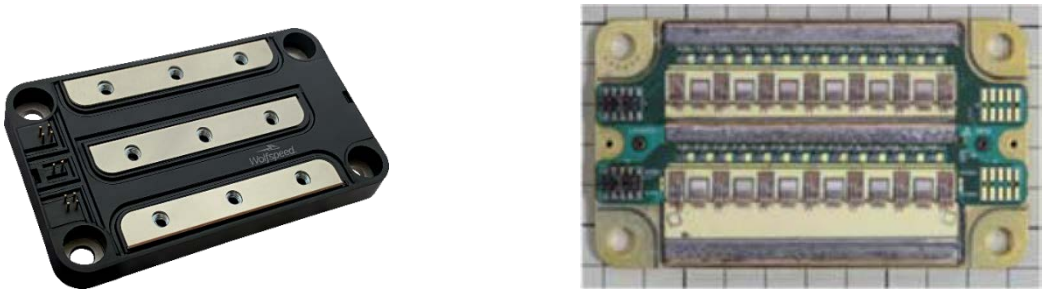
1.2. State of Medium Voltage Device Package

The medium voltage SiC devices has demonstrated superior performance of the high voltage blocking capability, high switching speed, and high temperature operation. Researchers and designers are exploring new packaging materials and package designs to fully utilize the superior property of the SiC devices.

The device packages of the 1200 V SiC MOSFET power modules have been improved to accommodate to the characteristic of the SiC MOSFETs. Wolfspeed has demonstrated two generations of the low inductance light weight power module package, specially designed for SiC MOSFETs. In Figure 1.1, the external look and internal layout of the high performance 62 mm package are shown. To realize high switching speed, wide copper plates which are directly attached to the substrate are used as power terminals to reduce the introduced parasitic inductance. Also, this package enables 175 ℃ continuous operation with the silicon nitride (Si_3N_4) power substrate and aluminum silicon carbide (AlSiC) baseplate. The Si_3N_4 substrate and AlSiC baseplate have close coefficient of thermal expansion to SiC and good mechanical robustness under extreme operation conditions.

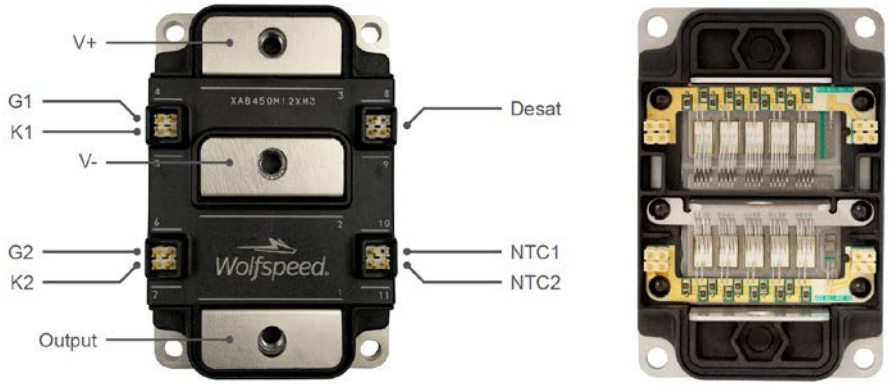
The next generation high performance package XM3 series also adopts Si_3N_4 substrates for robust high temperature operation. In this package, the power loop area is further reduced with positive and negative DC terminals arranged on the same side. The power loop parasitic inductance is reduced with smaller power loop area, optimized dc busbar design and proper dc link capacitor selection. Another improvement in this package

design is the barrier design around the gate-Kelvin source connection and NTC connection. The barrier increases the creepage distance between the dc positive terminal and gate-Kelvin source terminals. This design will help prevent partial discharge and enhance the high voltage insulation capability in various operation conditions.



(a) External package (b) Internal layout [12]

Figure 1.1 Wolfspeed high performance 62 mm low inductance light weight package



(a) External package and pinout (b) Internal layout

Figure 1.2 Wolfspeed XM3 series low inductance package

For 3.3 kV and 6.5 kV SiC power module packaging, conventional packages for 3.3 kV and 6.5 kV IBGT power modules are utilized. Wolfspeed [13], Mitsubishi [14], GeneSiC [15] and Fuji Electric [16] have reported their effort on the SiC power module development. The conventional packages contain a single switch with multiple paralleled

semiconductor chips. Neither chopper nor half-bridge structure has been reported. In Figure 1.3, a typical single device power module package is shown. On the surface of the 6.5 kV and 10 kV housing, special patterns to increase the creepage distance between the device drain/collector terminal and the source/emitter terminal, between the device drain/collector terminal and the gate terminal, between the device drain/collector terminal and the baseplate are designed. Copper is the common baseplate material. No information on the internal structure has been found. The conventional packages could meet the isolation requirements, but they are not optimized for high switching speed operation.

(a) GeneSiC 3.3 kV (b) Mitsubishi 6.5 kV (c) Mitsubishi 10 kV

Figure 1.3 Typical commercial single switch power module package.

In engineering samples, the half-bridge structure for 10 kV and 15 kV SiC devices are reported in [13], as shown in Figure 1.4. Similarly, the top surface of the housing is specially designed to increase the creepage distance between terminals with high voltage difference. The gate terminals are designed close to the device source/emitter terminals, which are of similar voltage potentials. On the side of the housing, special structures are not designed to increase the creepage distance between the high voltage terminals to the baseplate. For the 10 kV and 15 kV power module, aluminum nitride (AlN) substrate is used for the high voltage isolation. Single layer substrate is used for the insulation, which leads to around 2 A leakage current during normal operation. These packages might be

able to provide enough isolation for the 10 kV and above SiC devices, but they are neither optimized for high switching speed operation and high power operation.

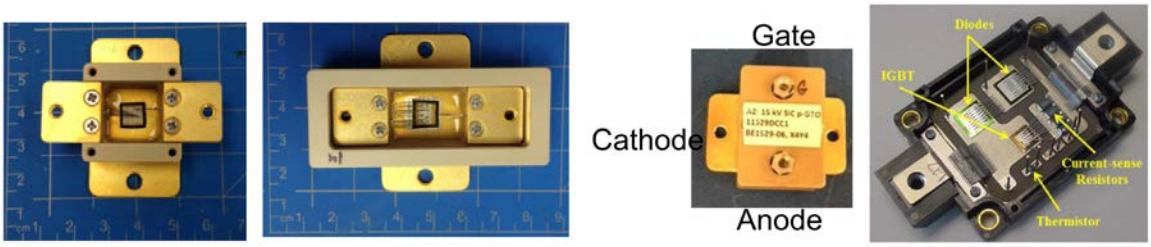
(a) (b)

Figure 1.4 Engineering sample package for half-bridge power module (a) 10 kV SiC MOSFET (b) 15 kV 80 A SiC IGBT

The quick prototype package for semiconductor die lab characterization are shown in Figure 1.5. In the first three packages, the package bottom is connected to the high voltage potential. Additional insulation needs to be inserted to install these packages to the cooling system. Meanwhile, compared to the semiconductor chip size and the area per die in commercial power module, this package is bulky. The parasitic capacitance and inductance from these packages are relatively large, which would limit the operation switching speed of the devices. The creepage distance is not carefully designed for this package either.

To improve power module power density, the thermal dissipation capability is critical. The SiC device can operate under higher current with excellent cooling. Generally liquid cooling has smaller junction to coolant thermal resistance. Multiple efforts have been taken to increase cooling area, increase heat transfer coefficient, and reduce the distance between heat source and coolant. In the commercial products, Infineon [17]-[18], Wolfspeed [19] and Mitsubishi [20] have designed power module with wave fin and pin fin baseplate for high power direct liquid cooling application. These modules can be assemblied directly to

the cooling sink, getting rid of the thermal interface material layer, and increasing the effective cooling area. The design is shown in Figure 1.6.



(a) (b) (c) (d)

Figure 1.5 Package for quick prototype package for medium voltage SiC power devices (a) 10 kV SiC MOSFET [4] (b) 15 kV MOSFET [4] (c) 15 kV ETO [6] (d) 15 kV IGBT [5]

(a) (b) (c) (d)

Figure 1.6 Baseplate with wave fin and pin fin design (a) Infineon wave fin baseplate design with ribbon bonding (b) Infineon pin fin baseplate design (c) Wolfspeed pin fin baseplate design (d) Mitsubishi pin fin baseplate design

In academic area, multiple advance cooling approaches have been reported. Power module design with double side cooling capability have been proposed. Figure 1.7(a) shows a pin-fin integrated, double-side cooled, SiC module design from ORNL [21],which achieves a 40% reduction in thermal resistance. Figure 1.7(b) shows another SiC power module design with double side cooling capability.

(a) (b)

Figure 1.7 Bond-wireless SiC power module design with double side cooling capability (a) ORNL pin fin integrated double side cooling power module (b) A*STAR Singapore double side cooling power module

The Army research laboratory also propose to ultilize the power module parts for multi-functions [22]. A pin fin structure is designed to work as the electrical connection to gate/drain/source terminals of the SiC MOSFETs, as well as a pin fin for heat dissipation purpose. Insulated coolant is used to flow through the pin fins, taking away the power loss in high power operation.

When applying the aforementioned cooling method to the medium voltage SiC MOSFET packaging, electric insulation become a concern. The jet impingement cooling is adopted in the 10 kV SiC MOSFET packaging [23]. Internal coolant channels are carefully designed so that the coolant can be impinged directly to the DBC bottom layer right underneath the semiconductor chips. The prototype for the integrated jet-impingement cooled power module is shown in Figure 1.8. This method has high requirements on the insulation capability of the coolant. After long time running, conductive impurities in the coolant might cause short circuit in the energized circuits.

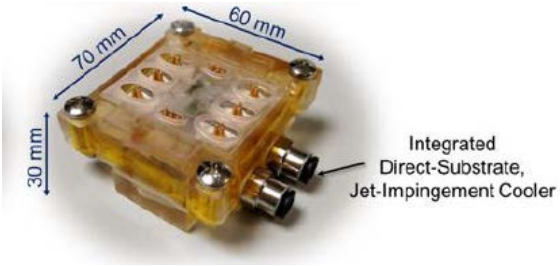


Figure 1.8 Integrated jet-impingement cooling in the SiC device packaging

From the review above, the package for the SiC device with 3.3 kV and above voltage rating is not optimized for the SiC device high speed high voltage high power operation. There are still potential issues and opportunities in the medium voltage SiC device packaging design.

1.3. Motivations of This Work

The development of the SiC power transistors enable the next generation power conversion systems design. The huge market of motor drive inverter, locomotive traction drive, and grid-tie inverter[24]-[26] has an increasing interest in SiC based solutions.

Simply replacing the Si MOSFETs/IGBTs with SiC devices cannot extract the full benefits from medium voltage SiC devices. Each part of the system needs to be carefully inspected and designed. On the packaging level, the following aspects need to be investigated. 1) The power loop layout. In the high switching speed operation, the device drain to source overshoot voltage induced by the power loop parasitic inductance needs to be reduced. A high overshoot voltage will limit the voltage level the SiC devices can work with. The overshoot voltage also causes extra the switching loss and reduce the system efficiency. The power loop layout could be improved to reduce the power loop parasitic inductance. As a result, the overshoot voltage can be reduced accordingly. 2) The insulation

designs. In the insulation design is divided into two categories. The electric field strength control under dc or low frequency ac voltage stress, and the electromagnetic interference (EMI) shielding. The electric field control is to prevent severe insulation breakdown, surface flashover or partial discharge (PD). Inside the power module, there are electric field concentration at certain locations, and the high electric field strength lead to PD before actual insulation breakdown. When PD happens, the insulation part will be eroded gradually and breaks down much earlier. The approach to limit the maximum electric field strength needs to be investigated. On the other hand, the high switching speed of the SiC devices leads to higher leakage current and EMI shielding challenge. The principle to reduce the interference is to reduce the noise source, add bypass path for the noise, and increase the impedance along the noise traveling path. The design to enable medium voltage device high speed switching needs to be explored. 3) The cooling designs. Cooling is an unavoidable topic for in the medium voltage power module design. With powerful cooling, the device can deal with more power conversion, simplifying the overall system, and reducing the cost and maintenance of the system. Light weight high power density power module designs are desirable in the electric vehicle and aircraft applications. Light weight high power density design will help extend the mile range. Increasing power density while maintaining good insulation brings more challenges in the power module design. The medium voltage SiC device package design becomes a multi-disciplinary topic with the various concerns from electrical, thermal, and mechanical side. The utilization of the multi-function parts becomes a trend in the package design. More possibilities in the package are expected to be explored.

On the circuit level, the current gate drive circuit cannot satisfy the requirements of the SiC devices in terms of short circuit protection. The high switching speed and high blocking voltage of the medium voltage SiC MOSFET raise higher requirements on the driving current, CMTI, and protection. Also, the cost of the medium voltage SiC power modules can be reduced with simple circuit design and lower voltage rating devices. Simple gate drive circuits and power circuits are discussed to improve the medium voltage device reliability.

To answer these questions, this work starts with the commercial medium voltage SiC device characterizations, expands with the device packaging discussion, and end up with circuit level realization and optimization to demonstrate a feasible design approach for next generation medium voltage high power density SiC power module design.

1.4. Chapter Review

This dissertation is to illustrate the methodology for medium voltage power switch design with SiC MOSFETs. Chapter 2 focuses on the SiC MOSFET reliability evaluation and solutions to enhance the medium voltage SiC MOSFET short circuit capability with improved gate drive circuit design. A commercial discrete 3300 V SiC MOSFET is evaluated for its short circuit withstand time under various gate voltages. Correspondingly, a design guideline is provided for the proposed medium voltage SiC MOSFET gate drive design with improved short circuit protection capability. In Chapter 3 and 4, the application of ceramic materials as the baseplate or heatsink in the medium voltage power module package is assessed in various perspectives. The excellent electrical insulation capability, relatively low material density, and good thermal conductivity of the ceramic material

bring multiple potential benefits in the medium voltage SiC MOSFET power module design. Both simulation model and experimental testing are used to verify and quantify the improvements. An economic approach to realize medium voltage power switches, super-cascode structure, is discussed in Chapter 5. This chapter is to investigate the impact of the major components in the super-cascode structure and improve the power switch dynamic performance by optimizing circuit parameters. An analysis model of the super-cascode structure during the switching transients is built and used for the parameter optimization. Experimental results are provided to verify the analysis. Chapter 6 summarizes the contribution of the work and recommends future works for further improvements. This dissertation reports work collaborated with Mr. Diang Xing in Chapter 1.

Chapter 2. Medium Voltage SiC MOSFET Short Circuit Evaluation and Protection

Medium voltage semiconductor switches have been widely used in traction drives and high-power industrial converters. Medium voltage SiC MOSFETs benefit from absence of tail current and reverse recovery and demonstrate higher switching speed and lower switching loss than the Si IGBT counterparts. Researchers from academia and industry have been improving the design and manufacturing process of the medium voltage SiC MOSFETs. Compared to Si devices, the medium voltage SiC MOSFET short circuit withstand time is shorter and degrade fast under short circuit conditions. For large scale application, the device reliability needs to be further improved. The drive circuits and protection circuits also need to be reconsidered to adapt to the device characteristics and effectively protect the medium voltage SiC devices.

2.1. Review of Medium Voltage SiC MOSFET Short Circuit Capability

At low doping concentration, electron mobility of SiC is smaller than that of Si. To compensate for the lower electron mobility, SiC MOSFET uses shorter channel length. Also, the breakdown electric field strength of SiC is about 8 times of Si, so for the same voltage rating, SiC semiconductor mass is smaller than that of the Si devices. Under short circuit event, Joule heating cannot be dissipated through the baseplate and the cooling structure. The generated heat is absorbed by the semiconductor mass. Smaller mass and shorter channel length make it more challenging for SiC device to survive through short circuit events.

Limited short circuit capability of the SiC MOSFETs with rating voltage 3300 V and above have been reported in the literature [27]-[30]. In Figure 2.1, the reported short circuit withstand time of the 3300 V SiC discrete devices are summarized. In the figure, the device designs A - B [30] and J [28] are tested under 1800 V dc bus voltage, while device designs C - H [27] and I [28] are under 1500 V dc bus voltage. In literature [27], the device design parameters are tuned to balance the on-resistance and short circuit capability on the same die area. Larger on-resistance will help reduce the short circuit energy and enhance the device short circuit capability. But during normal operation, lower on-resistance will improve converter system efficiency. Tradeoff has to be made to balance the performance under normal operation and short circuit condition. Usually, to reduce the on-resistance under normal operation, the manufacture recommended gate to source turn-on voltage is usually at 20 V or 18 V. all the reported case cannot survive 10 μs short circuit events. Device design D, E, and F successfully turns off under short circuit condition, but fails several microseconds after turn-off. Under lower gate voltage (15 V), the short circuit withstand time increases, but still cannot survive the 10 μs short circuit events.

The short circuit failure causes have been investigated and reported [27], [30]-[35]. During short circuit events, the device enters saturation region, withstanding high current and high voltage simultaneously. Several Joules of short circuit energy is generated in nanosecond-level. The heat increases the die junction temperature, and the die could be damaged by the high temperature. Increased gate leakage current has been observed after repeated short circuit events [30]. Gate oxide degradation due to high junction temperature under short circuit condition is believed to be critical to the device short circuit capability

[30]-[36]. Also, the aluminum bonding wire melting is also observed via SEM investigation. During short circuit test, the die source surface temperature exceeds the aluminum bonded wire melting point. The molten aluminum penetrates the p-base/n-drift junction, leading to device drain to source short circuit [36].

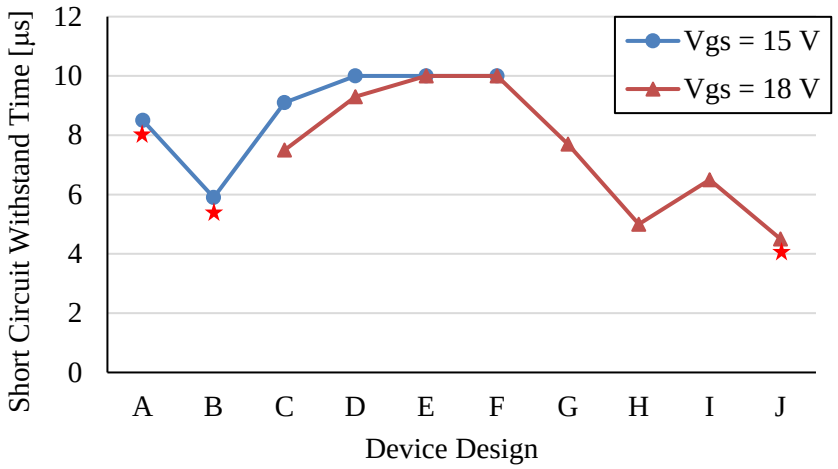


Figure 2.1 3300 V SiC MOSFET short circuit withstand time.

The medium voltage SiC MOSFETs degrade fast under short circuit conditions. In literature [37], the 10 kV SiC MOSFET degradation under short circuit events is reported. As the short circuit pulse width increases, the device sees obvious degradation, showing increasing threshold voltage, larger channel resistance and visible boding wire melting. Short circuit condition is an extreme situation, indicating the performance of the SiC MOSFET under long-term thermal stress or repeated over-current conditions.

The gate drive circuits can also be improved to accommodate the characteristics of the medium voltage SiC MOSFETs. In this chapter, a three-step short circuit protection solution is described, featuring ultra-fast short circuit detection, quick gate drive voltage

response, and double confirmation. The proposed solution can effectively reduce the short circuit energy and protect the device under test from catastrophic damage. At the same time, the converter efficiency during normal operation is not compromised.

2.2. Three-Step Short Circuit Protection for Medium Voltage SiC MOSFET

The proposed short circuit protection method for the medium voltage SiC MOSFET consists of three stages: a high-pass filter based ultra-fast detection unit, an active gate voltage clamping circuit, and a desaturation based soft turn-off circuit. The diagram of the protection circuit is shown in Figure 2.2, which is described in detail below. The flow chart for the protection scheme is shown in Figure 2.3.

Step 1): Ultra-fast detection. For a typical bridge based circuit, this short circuit detection is based on the phase-leg voltage, which is the voltage across the upper device drain and the lower device source. The detection position is illustrated in Figure 2.4, the phase-leg voltage (V_{plv}) is monitored. The V_{plv} waveforms under normal operation and short circuit condition are compared in Figure 2.5. In normal operation, V_{plv} is the dc bus voltage, plus small switching noises. Under the short circuit condition, V_{plv} will show a sudden dip due to the parasitic inductance in the power loop and a high *di/dt*. When the sudden voltage dip is detected, the fault trigger flag will be set. The response time of the detection circuit can be within tens of nanoseconds. The detailed detection circuit design will be discussed in Section 2.3.

Step 2): Active gate voltage clamping. Once the voltage dip is detected, V_{gs} will be reduced to enhance the device short circuit capability. In Figure 2.2, a low voltage clamping switch in series with a resistor, R_{clamp}, is connected to the device gate terminal.

R_{clamp} and the device gate resistor form a voltage divider which will reduce the device drive voltage to a lower voltage, e.g. 14 V, for a predetermined period. The gate voltage clamping time can be adjusted by changing the pulse generator control parameters.

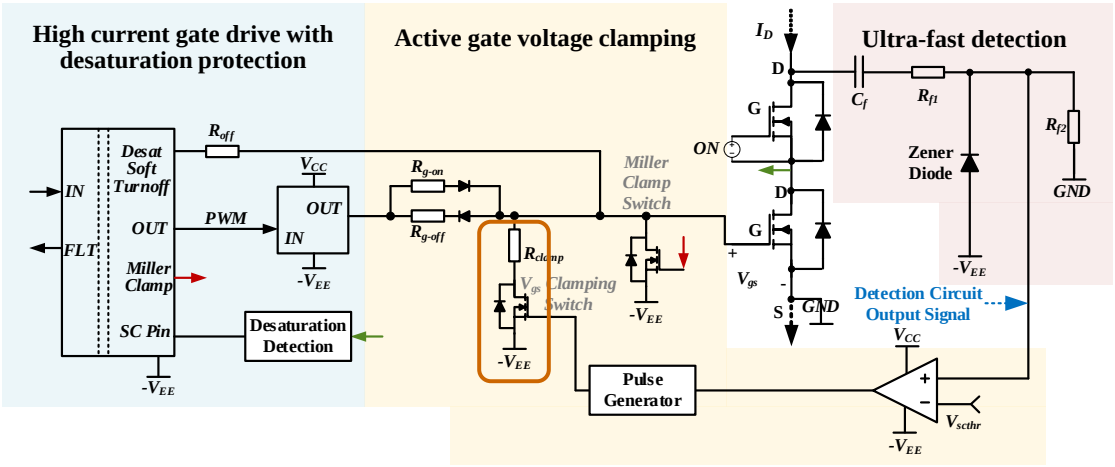


Figure 2.2 Diagram of the proposed three-step short circuit protection circuit.

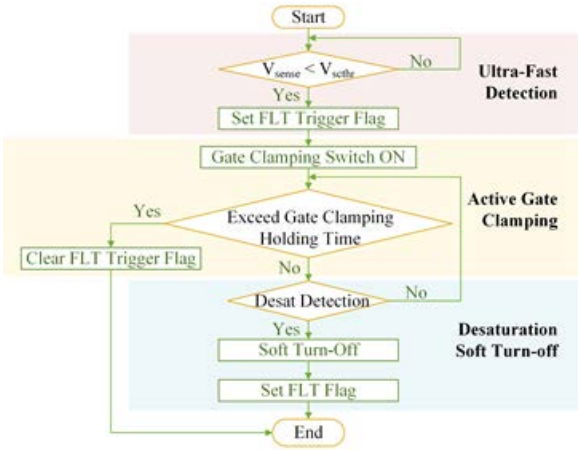


Figure 2.3 Flow chart of the proposed three-step short circuit protection method.

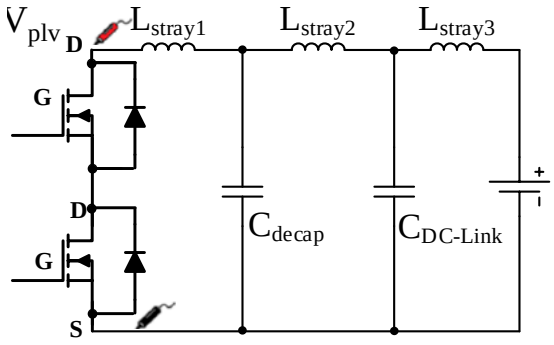
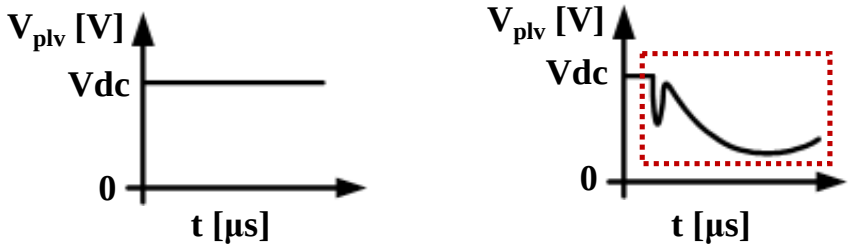


Figure 2.4 Three-step short circuit protection detection position.



(a) (b)

Figure 2.5 Three-step short circuit protection detection signal (a) under normal operation (b) under short circuit condition.

Step 3): Desaturation based soft turn-off. A conventional desaturation detection circuit is deployed to confirm the short circuit fault and slowly turns off the device. If the fault condition is sustained, the desaturation circuit will detect excessive on-state drain to source voltage and turn off the device slowly. If the detected short circuit event is a false signal, the device gate voltage will return to its normal value in the next switching period, and the converter's operation will not be interrupted.

2.3. Design of the Ultra-Fast Short Circuit Detection Circuit

2.3.1. Impact of the Power Loop Parasitic Parameters

A highly sensitive and responsive detection circuit is the key to successful protection. As shown in Figure 2.2, the input signal to the detection circuit is the phase-leg voltage V_{plv}. This voltage under short circuit condition differs from that under normal and heavy load conditions.

Because of the ultra-fast response time of the detection circuit, the parasitic parameters of the circuit have high impact on the proposed method. A SPICE based simulation is performed to investigate the influence of parasitic parameters on the amplitude of the phase-leg voltage change

The circuit diagram is shown in Figure 2.4.

L_{stray1} represents the stray inductance of the loop formed by the decoupling capacitors and the SiC MOSFET phase leg. The current conduction loop is represented by the solid line shown in Figure 2.4. L_{stray1} incorporates the stray inductance from device package, PCB traces, and the equivalent series inductance of the decoupling capacitors.

L_{stray2} represents the stray inductance of the loop formed by the dc-link capacitor and decoupling capacitor. The loop is represented by the dashed line in Figure 2.4.

C_{decap} represents the decoupling capacitors.

$C_{DC\text{-}Link}$ represents the dc-link capacitor bank.

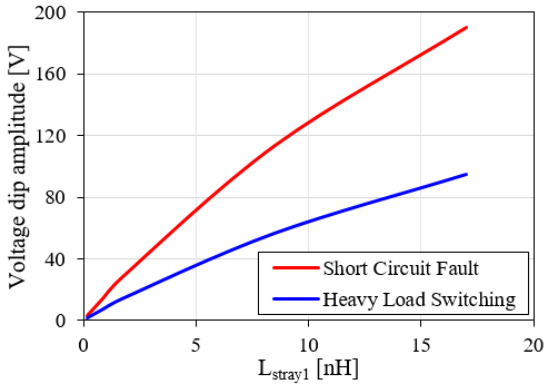


Figure 2.6 Relationship between L_{stray1} and the target voltage dip amplitude.

During a short circuit fault, the phase-leg voltage first experiences a quick voltage dip and then oscillates. As a result, it can be used as an ultra-fast indicator for the short circuit detection.

The relationship between L_{stray1} and the amplitude of the target voltage dip is simulated and plotted in Figure 2.6. The higher the value of L_{stray1}, the larger the amplitude of the voltage dip. When L_{stray1} is as low as 1.7 nH, which is quite optimized for the switching overshoot voltage reduction, it still can cause more than 30 V voltage dip during a short circuit event.

2.3.2. Detection Circuit Design Process

The guidance for the detection circuit design is explained below. Besides simulations, initial short circuit test and heavy load test are also carried out to determine the input signal of the detection circuit. Test results show that under normal switching with a 45 A inductive load current, the monitored phase-leg voltage V_{plv} has lower than 3% ripple voltage. The

voltage dip at short circuit is a high dv/dt signal which occurs right after the device turns on.

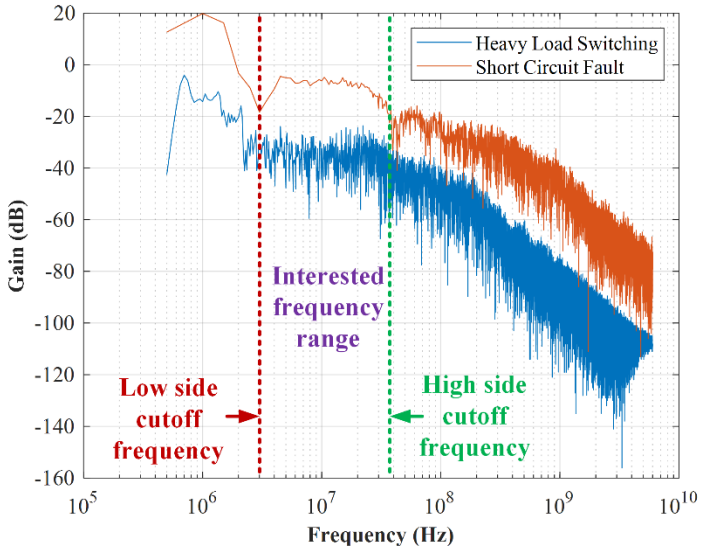


Figure 2.7 Detection circuit design: FFT analysis of V_{plv} for detection circuit filter design.

An FFT analysis of V_{plv} under heavy load switching and short circuit fault is shown in Figure 2.7. Generally, the amplitude of the phase-leg voltage under fault condition is higher than that under heavy load switching. Specifically, there is noticeable amplitude difference between these two voltages at the frequency band between 3 MHz and 50 MHz. Thus, a high pass filter is designed to detect the high frequency voltage dip during the short circuit event. The schematic of the proposed high pass filter is shown in Figure 2.2. It is composed of C_f, R_{f1}, and R_{f2}. To protect the comparator after the filter, a Zener diode is also included. The junction capacitance of the Zener diode, C_j, forms an intrinsic low pass filter with R_{f1}. To maximize usage of the 3 MHz to 50 MHz band, Cj should be kept low.

Combining all these components, the transfer function of the detection circuit is derived as Eq. (1).

$$H(s)=\frac{s\cdot R_{f2}C_f}{s^2\cdot R_{f1}R_{f2}C_fC_j+s\cdot\left(R_{f1}C_f+R_{f2}C_f+R_{f2}C_j\right)+1} \quad (1)$$

The parameters of the high pass filter were decided as follows.

$C_f=300\,pF,\ R_{f1}=100\ \Omega,\ R_{f2}=1\,k\Omega$

A 5 V Zener diode with 225 pF junction capacitance is selected.

More discussions on the influence of the filter component parameters can be found in [38].

2.4. Experimental Verification of the Three-Step Protection

A test platform was built to verify the proposed three-step short circuit protection method. The test board is shown in Figure 2.8. The detection and protection circuit of the Device Under Test (DUT) is on the right side. Under normal operation, the gate voltage is 18 V (ON) and –4 V (OFF). Under short circuit condition, the gate voltage is clamped at 14 V before soft turn-off. The gate drive board is designed with the three-step protection function. In the short circuit test, the protection function can be disabled.

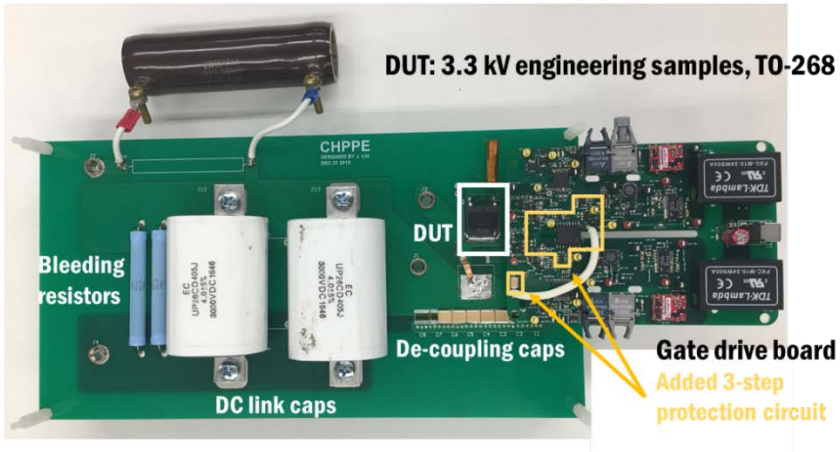


Figure 2.8 3300 V SiC MOSFET short circuit protection evaluation board

2.4.1. Experimental Results of the 3300 V SiC MOSFET Short Circuit Performance

The DUT is GeneSiC 3300 V 450 mΩ discreet SiC MOSFET in TO-268 package. The device short circuit performance is evaluated under 2000 V dc bus voltage and 18 V gate voltage. The pulse width is increased by 1 μs step until the DUT fails. After each pulse, the dc voltage is reduced gradually to 0 V, and there is 10-minute interval time between pulses for device cooling down. The test results are shown in Figure 2.9. The DUT drain current peak value reaches around 95 A. When the pulse width increases to 5 μs, the DUT cannot fully turns off. Several Amperes of current remains. After 0.5 μs, the drain current increases dramatically. A burnt spot on the package is observed after the DUT fails.

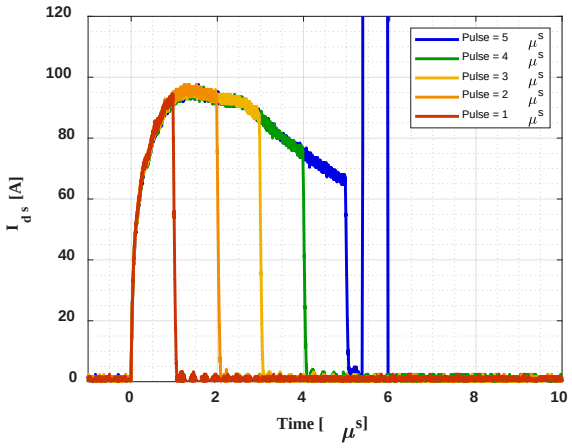


Figure 2.9 3300 V SiC MOSFET short circuit withstand time

From previous analysis, lower gate voltages can reduce the peak short circuit current, reduce short circuit energy, and extend DUT short circuit withstand time. The short circuit capability under various gate voltages are also tested. The dc bus voltage is 2,000 V. As shown in Figure 2.10, compared with the maximum drain current with 18 V gate voltage (V_{gs}), the current with 14 V V_{gs} is reduced by 36.8%, and the current with 10 V V_{gs} is

reduced by 76.8%. For this specific type of 3,300 V SiC MOSFET, gate voltage reduction under short circuit condition can effectively reduce the short circuit energy.

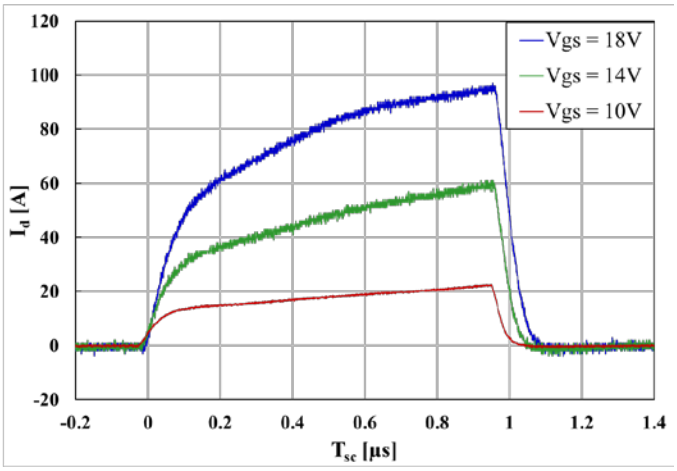


Figure 2.10 Short circuit current under different gate voltages.

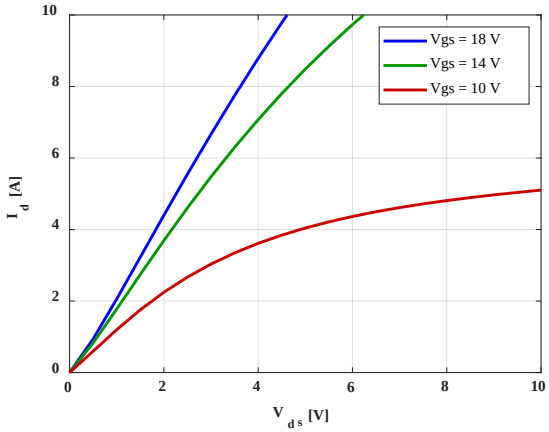


Figure 2.11 3300 V SiC MOSFET I-V curve

The proposed protection method will clamp the gate voltage once the ultra-fast detection circuit is triggered. The clamping gate voltage shall not push the DUT to the saturation region. The device I-V curve is extracted, as shown in Figure 2.11. The DUT is rated at 5 A. With 10 V V_{gs}, the device enters saturation region with 5 A load current, and

the DUT drain to source voltage will trigger the desaturation detection under normal operation. Thus, the clamping gate voltage is selected as 14 V.

2.4.2. Experimental Results of the Three-Step Short Circuit Protection

The experiment to verify the proposed three-step short circuit protection method is conducted under 2,000 V dc bus voltage. The test waveforms are shown in Figure 2.12. Each step in the proposed protection method is clearly annotated in the figure. Channel (CH) 1 is the short circuit fault flag signal. CH2 is the DUT gate to source voltage. CH3 is the dc bus voltage, which is measured at the upper device drain. CH4 represents the DUT drain to source current. The short circuit fault is detected around 80 ns, and the short circuit fault signal is set simultaneously, as in Figure 2.12. Then the DUT gate to source voltage is clamped to 14 V and the circuit waits for the confirmation from the desaturation detection circuit. In this stage, the increase of the device saturation current slows down and gradually saturates at around 85 A. After 2.2 μs, the desaturation circuit confirms the fault, and then softly turns off the device. During step 1 period, the di/dt of the short circuit current induces the voltage drop across the stray inductance in the power loop. As the device drain current quickly increases, the voltage dip can be easily seen in the figure and detected by the protection circuit. As soon as the short circuit fault signal is set, the DUT gate to source voltage is clamped to 14 V.

With 14 V clamping voltage, the short circuit current can be reduced effectively. The short circuit energy under 1 μs pulse width is reduced by 32% with the ultra-fast detection and gate voltage clamping.

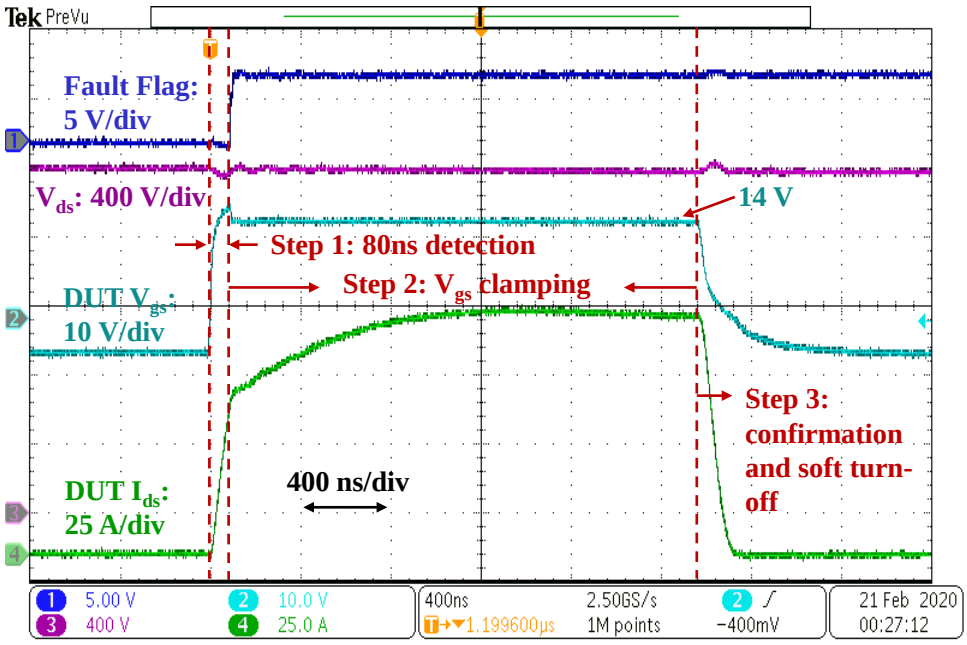


Figure 2.12 3300 V SiC MOSFET three-step protection waveform

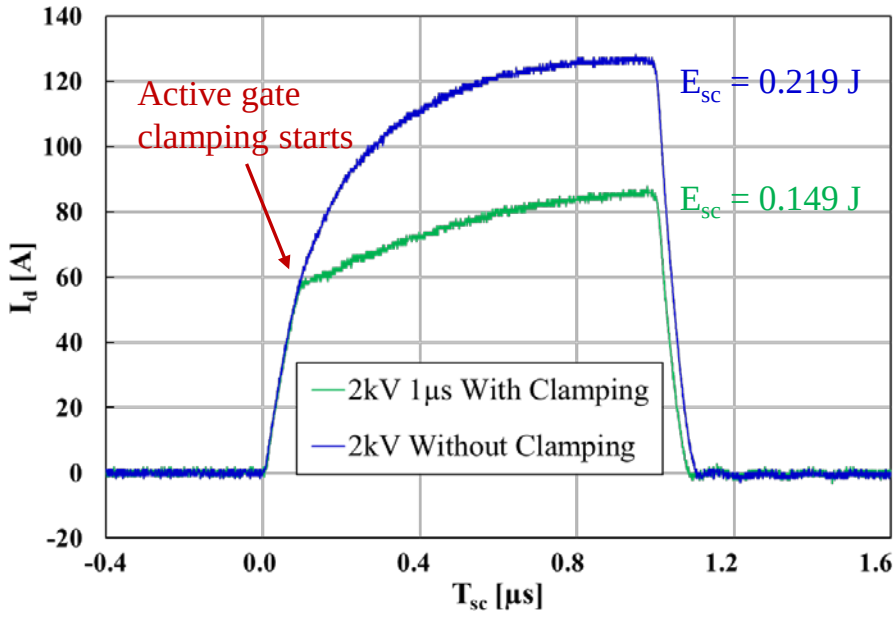


Figure 2.13 Short circuit current comparison with and without gate clamping

The proposed protection method is implemented in a phase-leg design. To realize the gate voltage clamping of the high side device, an isolated gate driver is needed to pass the signal from the detection circuit to the high side gate drive circuit, and control the clamping switch. For both high side and low side switches, the manufacture recommended drive voltage is adopted under the normal operation. For the gate loop PCB layout, small gate loop is preferred to reduce gate voltage noise and prevent false turn-on during the switching transients. Also, there should be no trace overlap between the primary side and secondary side. For the high side switch gate drive, the CMTI of the power supply, isolator and isolated gate driver needs to be at least 100 V/ns. The barrier capacitance is preferred to be in few pico-farads.

2.4.3. Noise Immunity Capability of the Three-Step Protection Method

Since the added detection circuit is highly sensitive, the noise immunity capability of the detection circuit is critical. Thus, an inductive load test is implemented to verify the noise immunity of the proposed protection method. The DUT is rated at 3,300 V 5 A. During the test, the DUT switches at 2,000 V dc bus, with load current up to 8 A. The experimental results are shown in Figure 2.14. CH1 is the fault flag signal, which shows whether the protection circuit is triggered or not during the operation. CH2 is the device gate to source voltage, CH3 is the switching node of the phase-leg, and CH4 is the load current. As the DUT switches under higher load current, the noise on the short circuit fault flag signal does not have obvious increase. Even at 8 A of load current for a 5 A rated device, the protection circuit is never mis-triggered. This verifies the noise immunity capability of the proposed three-step short circuit protection method.

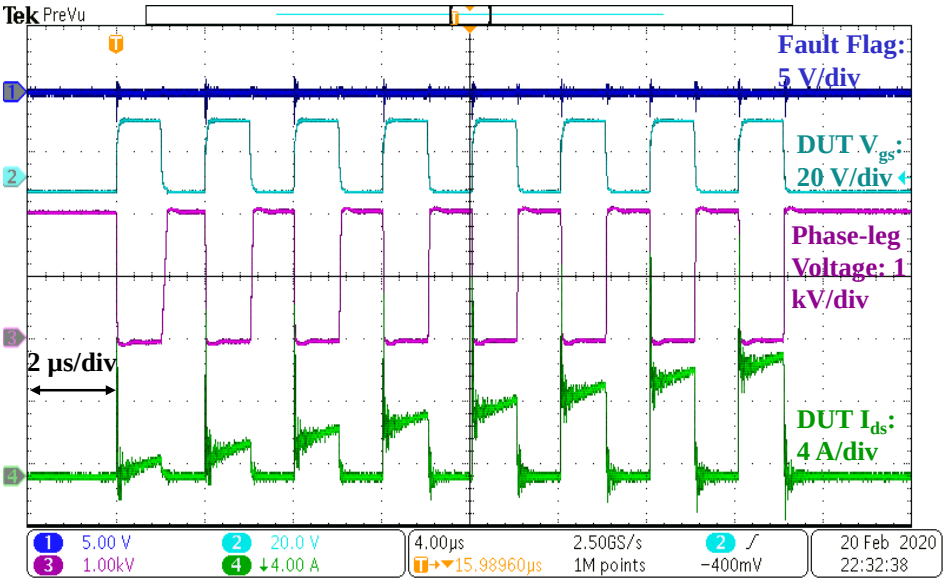


Figure 2.14 Noise immunity test under different load current.

2.5. Summary

In this chapter, a three-step short circuit protection method with ultra-fast detection and protection circuit is analyzed and verified. The voltage dip on the phase-leg voltage is a clear and quick fault indicator during short circuit events. The detection circuit and the gate voltage clamping circuit together are used to limit the 3300 V SiC MOSFET short circuit energy and protect the devices through short circuit events. Experimental results verify that the short circuit condition can be detected within 100 ns. As soon as the short circuit fault is detected, the device gate voltage is successfully clamped to 14 V. After 2.2 µs the desaturation circuit confirms the fault condition and then soft turns off the device. The detection and protection circuit have good noise immunity, and are not mis-triggered under heavy load operations. The proposed protection method successfully extends the short circuit capability of 3,300 V SiC MOSFET without sacrificing the efficiency of the

circuit during normal operation. The test results show that it is an effective and reliable way to protect the medium voltage SiC MOSFETs.

Chapter 3. Low Inductance Medium Voltage SiC MOSFET Power Module Design

To further increase the power density, the medium voltage SiC device packaging becomes a multi-disciplinary subject involving electrical, thermal, and mechanical design. Multi-functional package components are desired to deal with more than one concerns in the application. The relationship between electrical, thermal, and mechanical properties needs to be understood and carefully designed to achieve a fully integrated high-performance power module. New materials and new technologies are explored to further improve the device performance under harsh operating conditions.

The switching speed of the SiC MOSFET can be ten times higher than the Si devices. Under high speed switching, the requirement for the power loop stray inductance becomes strict, since the power loop stray inductance introduces voltage overshoot during switching transients. In this chapter, the proposed vertical power loop design or half-bridge structure is analyzed. A case study for 3300 V / 160 A power module is conducted in this chapter and Chapter 4. The power loop layout, current distribution, electrical insulation, EMI performance, and thermal performance are discussed in detail.

3.1. Half-Bridge Power Loop Design with Low Parasitic Inductance

3.1.1. Review of the State-of-the-Art Half-Bridge Power Module Design

The power loop inductance reduction is critical for SiC MOSFET power module to lower device voltage stress under peak power operation. Using laminated bus bar is a simple but effective way to reduce the loop inductance outside the power modules [39][40]. Adding decoupling capacitors on PCB or inside the power module is another widely known

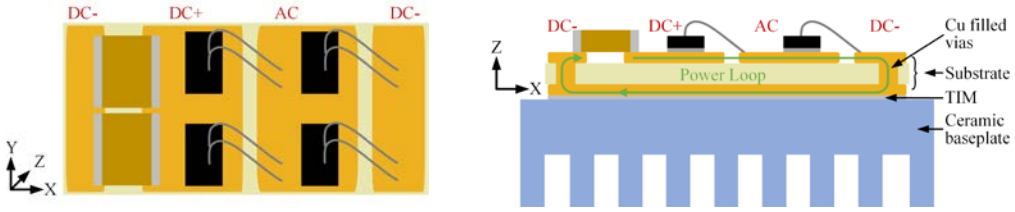
method. In paper [41] and [42], decoupling capacitors are integrated into the power module for 800 V dc application. In paper [43], integrated symmetrical ceramic capacitor placement realizes a more balanced power loop inductance for paralleled SiC MOSFET dies. In papers [44] and [45], sandwiched power modules with islanded substrates and integrated ceramic capacitors are fabricated and tested. These previous works prove the effectiveness of the reduction of the overshoot voltage by reducing the power loop inductance. However, the design becomes difficult when more MOSFET dies need to be paralleled. In this section, a power module with low loop inductance DBC layout and the AlN baseplate is introduced and analyzed. The design can be easily scaled to higher current rating power module design.

3.1.2. Proposed Half-Bridge Power Module Design

The proposed vertical power loop design is shown in Figure 3.1. It is a half-bridge structure with integrated decoupling capacitors. The bottom Cu layer of the substrate is utilized to form a complete current commutation loop. Cu filled vias work as the interconnection between the top and bottom Cu layers. Compared to the lateral layout of the power loop [41]-[43], this vertical loop design further reduces the power loop area, requires smaller substrate size, and ensures symmetrical loop inductance in the multi-chip layout.

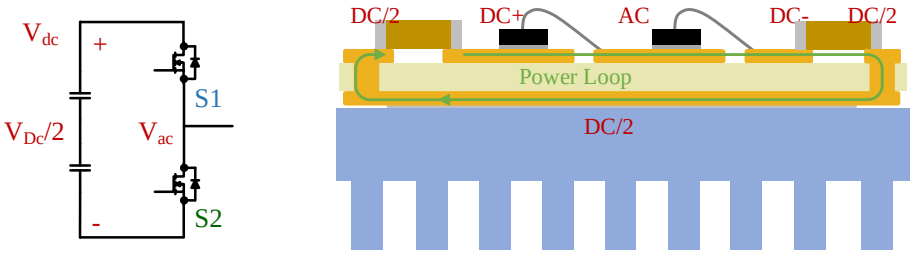
For SiC MOSFET with 3,300 V and higher voltage rating, the design in Figure 3.2 is recommended. The dc bus is split by two series connected dc link capacitors. The direct bond copper (DBC) bottom Cu layer works as the middle dc voltage rail. The integrated decoupling capacitor is recommended to be 100 times larger than the MOSFET output

capacitance. When splitting the dc bus voltage, capacitors with lower voltage rating can be selected. With lower voltage rating, the capacitance can be much higher. Another benefit to split the dc bus voltage is the electric field control under differential mode voltage. This part will be discussed in Section 4.3.



(a) (b)

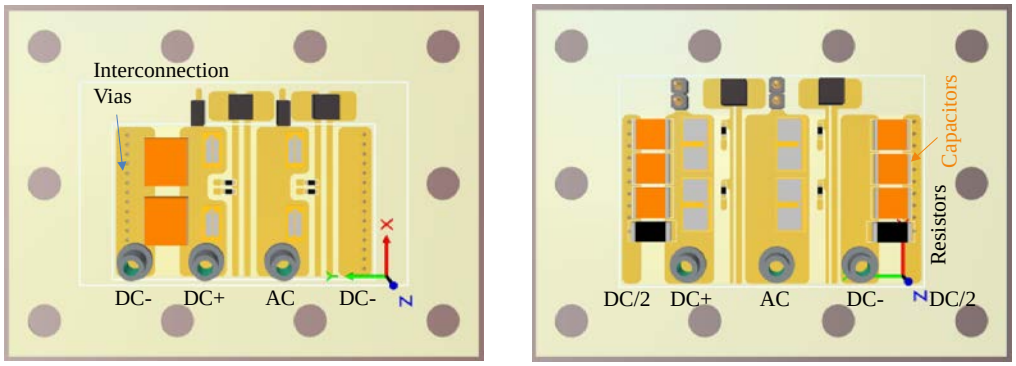
Figure 3.1 Half-bridge power module design with the vertical power loop layout (a) the top view of DBC layout (b) the side view of the power module structure.



(a) (b)

Figure 3.2 Half-bridge power module design with the vertical power loop layout (a) equivalent circuit (b) the side view of the power module structure.

The DBC thickness is selected to be around 1 mm according to the analysis in Chapter 3. The AlN layer is 0.025 inch and the top and bottom Cu layer thickness is 0.008 inch. Considering the die size, the DBC layout for 1,200 V SiC MOSFET and 3,300 V SiC MOSFET are shown as in Figure 3.3. Cu filled vias are used as the top-bottom interconnection. In the 3,300 V DBC layout, resistors are connected in parallel with the capacitors, to balance the voltage distribution between the series connected resistors.



(a) (b)

Figure 3.3 DBC vertical power loop layout (a) 1200 V SiC MOSFET (b) 3300 V SiC MOSFET.

In the following sections, details in the DBC design are discussed, in terms of electric field strength control, power loop parasitic inductance reduction, and current density control.

3.2. DBC electrical insulation design

To ensure good electrical insulation of the DBC top layer energized circuit, enough clearance or creepage distance need to be reserved. Otherwise, partial discharge or even breakdown will happen at lower applied voltage. In literature [46]-[47], the partial discharge behaviors under high dv/dt switching are investigated. DBC samples with varying trench distances and chamfer radius are prepared, and the partial discharge inception voltage (PDIV) under repetitive square-wave voltages are measured. The DBC sample design is shown in Figure 3.4. The DBC insulation layer is AlN, with 0.15 inch thickness. On the top layer, there are two Cu pads, working as the two electrodes connecting to ground and high dv/dt square-wave voltage. The trench distance between the two Cu pads is designed at 0.3 mm, 0.5 mm, and 0.7 mm. The chamfer radius of the pads

are 0.3 mm, 0.5 mm, 0.7 mm and 0 mm (right angle). The DBC samples are covered with encapsulation gel. The breakdown dielectric strength is 16 kV/mm. In the PDIV test, photomultiplier tube (PMT) and a 200 MHz bandwidth high frequency current transformer based PD measurement equipment are used to indicate the happening of PD. The test results are illustrated in Figure 3.5.

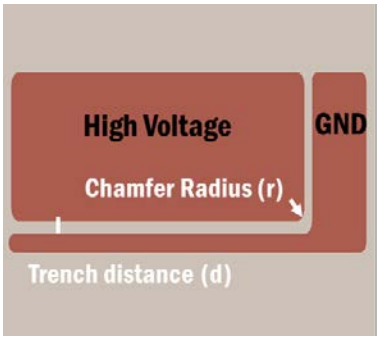


Figure 3.4 DBC sample design illustration

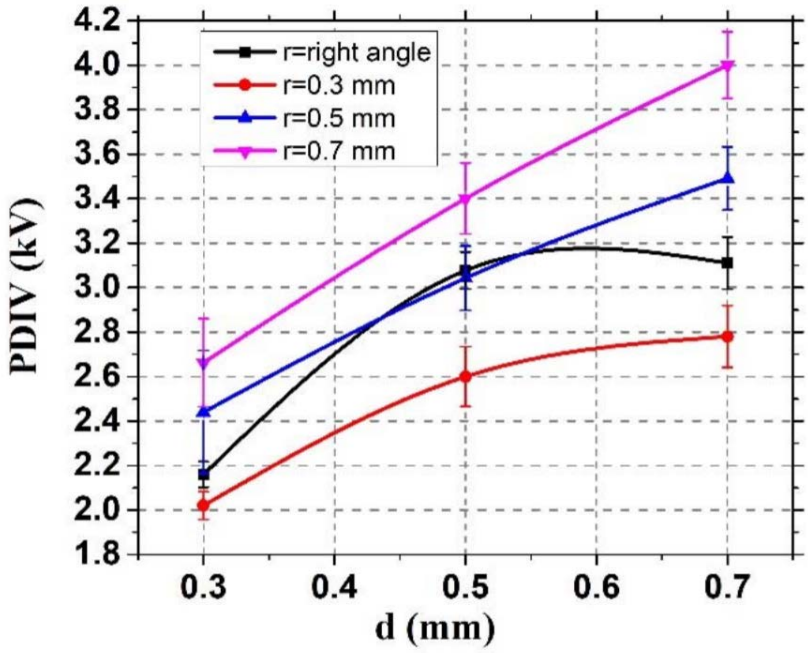


Figure 3.5 The relationship between PDIV, trench distance d and chamfer radius r

Larger trench distance and larger chamfer radius, higher PDIV. In the 3,300 V power module design, the trench distance is designed larger than 0.7 mm, and the chamfer radius is between 0.5 mm and 0.7 mm. So two test points are used for the electric field strength simulation, trench distance 0.7 mm chamfer radius 0.7 mm case and trench distance 0.7 mm chamfer radius 0.5 mm case. For each case, the minimum PDIV is selected. 3.8 kV and 3.35 kV respectively.

3D models are built in Ansys Electronic Desktop, and the static electric field distribution is simulated. The worse case is shown in Figure 3.6, with 0.7 mm trench distance and 0.7 mm chamfer radius. The electric field concentrates at the triple joint of Cu pad, AlN insulation and encapsulation gel. The maximum electric field strength along the high voltage Cu pad is around 38 kV/mm. In the proposed 3,300 V power module DBC design, 38 kV/mm is the upper limit of the electric field stress for PD free design.

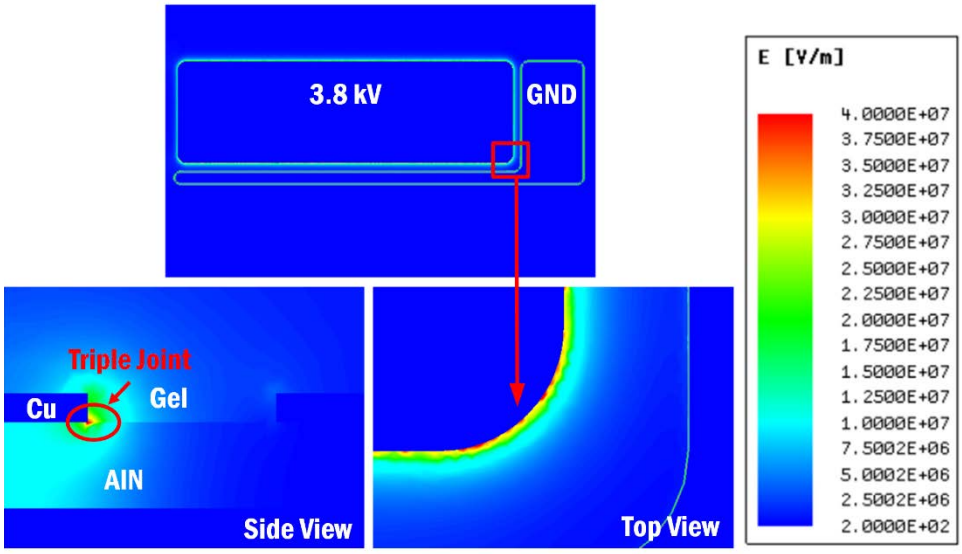


Figure 3.6 Electric field distribution of the DBC sample with 3.8 kV voltage excitation

Based on the simulated electric field strength, the clearance in the 3,300 V power module DBC is designed as shown in Figure 3.7. The clearance between device drain pad and gate trace is critical, since these two Cu pads see the largest voltage difference inside the power module. In this design, 1.2 mm is reserved for the clearance. 1 mm chamfer radius is designed for the larger Cu pads, and 0.5 mm chamfer radius is used for thinner Cu traces.

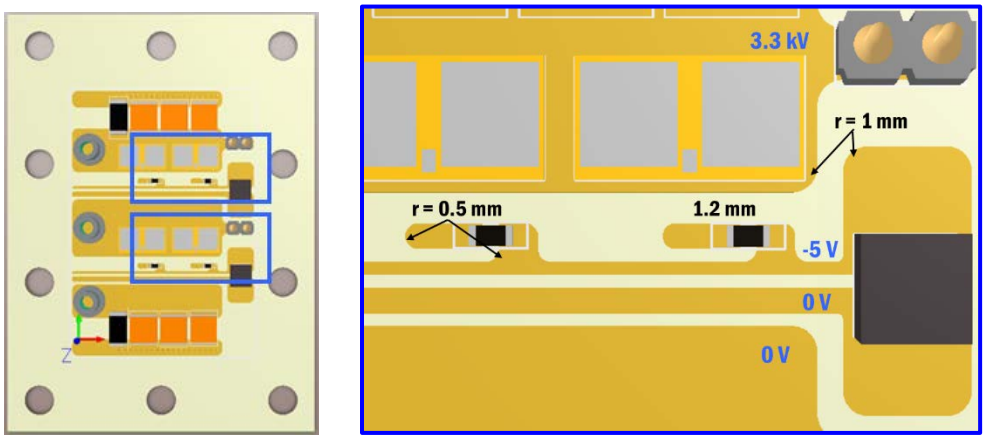


Figure 3.7 3,300 V power module DBC clearance design

3D models are built in the Ansys Electronic Desktop. The positive DC voltage excitation is set at 3,300 V. The gate trace voltage potential is -5 V. The bottom Cu layer is assigned with half dc bus voltage, 1,650 V. The source trace is grounded. 832FX encapsulation gel is also included with its dielectric constant 3.06. The electric field stress distribution is shown in Figure 3.8. The electric field also concentrates at the triple joint around the drain pad and the gate trace. The electric field stress distribution along four lines are plotted in Figure 3.9. The position and direction of the four lines are shown in Figure 3.8. The electric field stress is relatively lower in the middle of the clearance distance, and higher at the location closer to the Cu pad edges. The maximum electric field stress happens

at the tip of the gate pad, where R_edge line starts, 14.8 kV/mm. Compared to the electric field strength under PDIV stress (38 kV/mm), 58% margin is reserved for the electric insulation design.

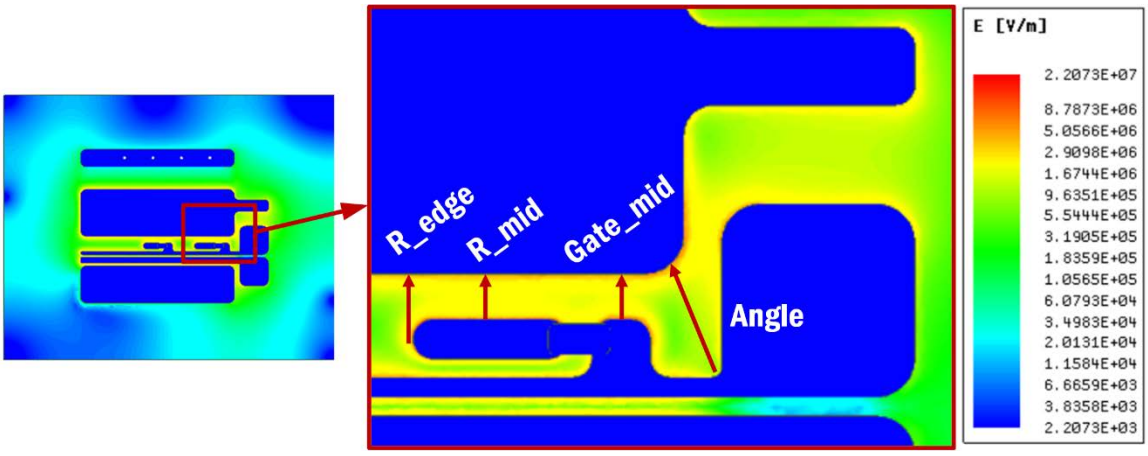


Figure 3.8 3,300 V power module DBC electric field stress distribution

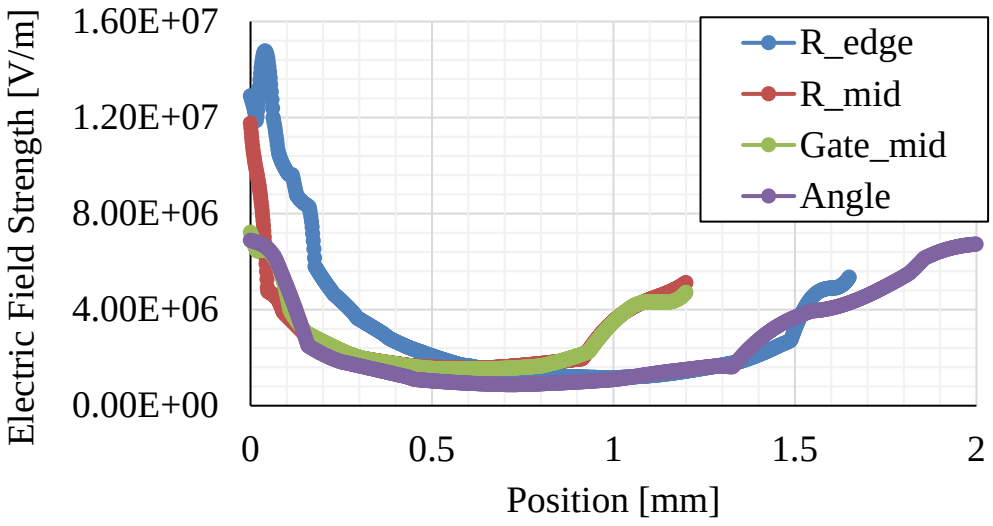


Figure 3.9 The relationship between PDIV, trench distance d and chamfer radius r

3.3. Power Loop Parasitic Inductance Extraction

Ansys Q3D is used to extract the parasitic power loop inductance of the proposed designs. In the 1,200 V model, bonding wires are also modeled to complete the power loop, as shown in Figure 3.10. In this design, 15 mil wide ribbon bonding is used. The extra power loop area introduced by the bonding needs to be included in the parasitic inductance extraction. The height of the bonding is 2.5 mm. In the 3,300 V model, similar ribbon bonding is used to complete the power loop. Also, one capacitor position is shorted to simplify the simulation model and result matrix. The SiC MOSFET switching time is around 70 ns, which is equivalent to 5 MHz signal. The 1,200 V power loop inductance is 3.9817 nH at 5 MHz, and the 3,300 V power loop inductance is 4.4571 nH at 5 MHz.

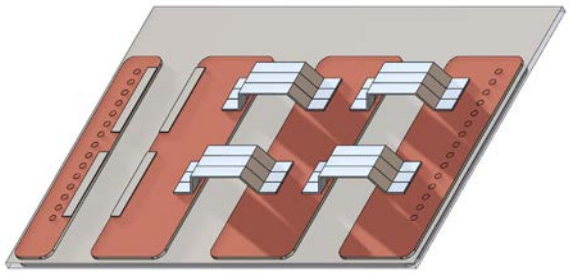


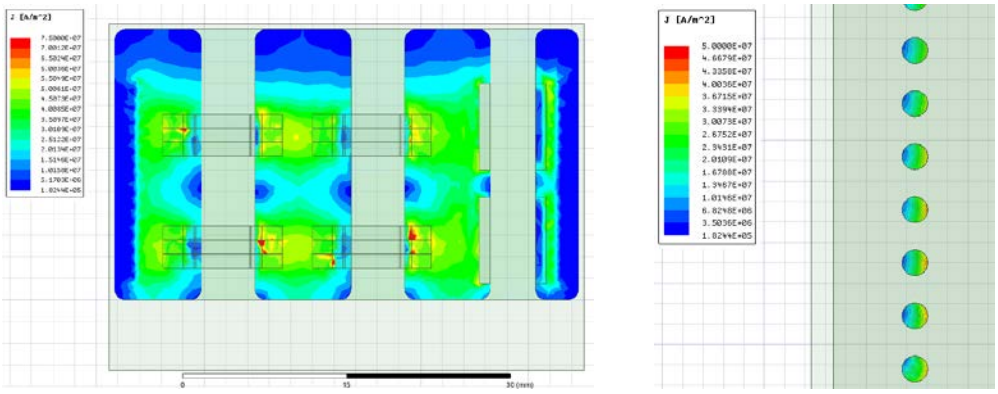
Figure 3.10 Power Loop Parasitic Inductance Extraction Model

3.4. Current Distribution of the DBC Layout

The current distribution based on the DBC layout is simulated with Ansys. In the 3D model, the Cu thickness is 0.2 mm. The interconnection via diameter is 0.635 mm, which is the maximum via diameter of 0.635 mm thick AlN insulation layer. 75 A dc current is assigned to the capacitor terminal, total 150 A dc current is assigned to the whole power module. Across the top Cu pads, the current is concentrated near the bonding area, the

average current density is 35 A/mm^2. In the interconnection vias, the current concentrates on the active circuit side, the average current density is about 25 A/mm^2.

Larger via radius and fewer via number are preferred if the manufacturability allows. The via cross-section area is proportional to the square of the via radius. The current density can be easier to reduce with larger via radius. A single layer via design is recommended. If two layers of interconnection vias are used, the vias on the external layer are shielded by the internal layer and will not help sharing the current.



(a) (b)

Figure 3.11 Current Distribution (a) across the Cu Trace (b) through Interconnection Vias

3.5. Experimental Results

The proposed liquid cooled power module structure is fabricated and shown in Figure 3.12. The SiC MOSFET dies are CPM2-1200-0040B from Wolfspeed. Two dies are paralleled per switch position, creating a 1,200 V / 126 A rated SiC power module. The decoupling capacitors are 1,000 V rated 0.15 µF ceramic capacitors.

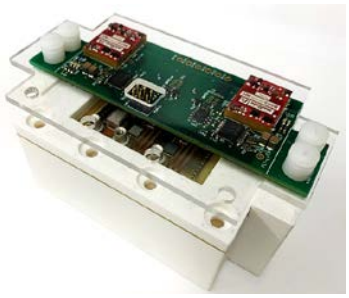


Figure 3.12 Proposed vertical loop based power module assembly with ceramic baseplate and liquid cool housing.

The power loop inductance is measured as 1.1 nH by impedance analyzer. The switching performance is examined with inductive load test. The bottom switch gate voltage and drain to source voltage are observed. Load current is measured as an indicator of the switching current. In Figure 3.13, the turn-on and turn-off transients at 700 V / 25 A inductive load switching are presented. During the turn-off transient, 30V drain to source overshoot voltage is observed at 22.33 V/ns switching. The overshoot voltage is only 4.3% of the dc operation voltage.

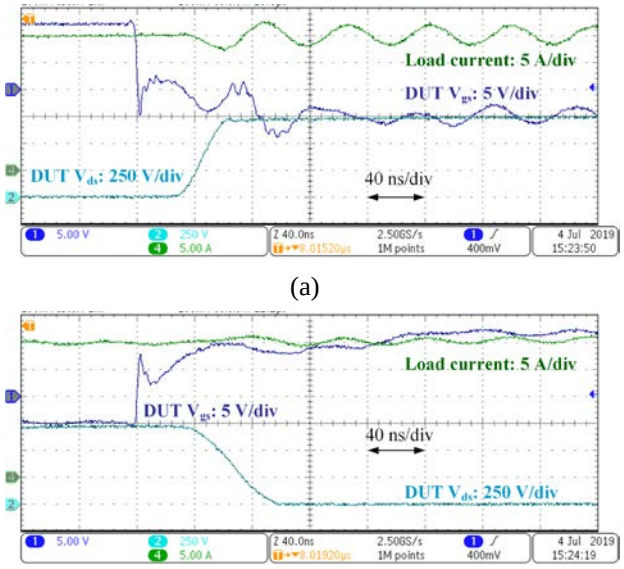


Figure 3.13 Switching performance of the vertical loop based power module at 700 V dc and 25 A load current, room temperature (a) turn-off transient, (b) turn-on transient.

3.6. Summary

The vertical loop structure is proposed for the medium voltage SiC MOSFET featuring low power loop inductance. Two vertical loop designs for 1,200 V 224 A power module and 3,300 V 160 A power module respectively are illustrated. Detailed DBC designs are discussed in the aspects of the electric insulation design, the power loop inductance reduction, the current design reduction. In the 1,200 V power module prototype, the manufactured DBC realizes 1.1 nH power loop inductance. Experimental results show 4.3% voltage overshoot during the 700 V 25 A turn-off transient.

Chapter 4. Lightweight Power Module Design with Ceramic Baseplates

The proposed vertical loop layout of the half-bridge structure shows low power loop inductance. Since the DBC bottom copper layer is utilized as part of the energized power loop, an electric insulation layer needs to be inserted between the energized circuits and the cooling system. In this chapter, the adoption of the ceramic baseplate is assessed in the aspects of the power density, the insulation design, and the thermal design. Section 4.1 discusses the challenges of increasing medium voltage SiC MOSFET power density, and reviews potential solutions to be used in the ultra high power density medium voltage SiC MOSFET packaging. In Section 4.2, a case study is shown to discuss the thermal design of ceramic baseplates. Section 4.3 and 4.4 discuss additional benefits on the electromagnetic interference (EMI) and electric field control. Section 4.5 provides the design guideline and summarizes the chapter.

4.1. Investigation of Light-Weight Material Utilization in Semiconductor Packaging

4.1.1. Exploration of Baseplate Material for Medium Voltage SiC MOSFET Packaging

The conventional power device package is shown in Figure 4.1. Generally, a power module includes the semiconductor dies, the die attachment, the substrate or the direct bond copper (DBC), the DBC attachment and the baseplate. The power module is mounted to the heatsink or cooling structure with screws. Thermal interface material (TIM) is applied to fill the air void and to enhance the thermal dissipation capability of the assembly. In some ultra high power rated device, there is specially designed fins on the baseplate, eliminating the additional TIM and heatsink. The thermal dissipation capability can be further enhanced by direct liquid cooling.

In the conventional package, the electrical insulation between the active power circuit and the cooling structure is provided by the ceramic layer in the direct bond copper (DBC) [48]. The baseplate layer is for heat-spreading and mechanical support, and its material is metal or metal alloy. Copper alloy (Cu) is used as the baseplate when enhanced cooling is required and the system is less sensitive to weight. Aluminum alloy (Al-6061) is widely used in automotive industry as the baseplate material, thanks to its good thermal conductivity and light weight. Aluminum silicon carbide (AlSiC), a metal matrix composite material, becomes popular for high power insulated gate bipolar transistors (IGBTs) due to its compatibility with the thermal expansion value of the substrate inside the package. The AlSiC thermal conductivity and material density is a little higher than Al-6061. All these materials are electrically conductive.

The medium voltage SiC MOSFET has lower switching loss than the IGBTs, so its thermal dissipation is not demanding. At the same time, SiC MOSFET switching speed is higher, the parasitic parameters of the DBC have larger impact on the device dynamic performance and electromagnetic interference (EMI) performance.

Another important consideration is the insulation requirement of the medium voltage package. According to the IEC standard, the common mode voltage blocking capability is around twice the device operating voltage. With the conventional package structure, the DBC ceramic layer solely withstands the required common mode voltage. For the device with 3,300 V and higher blocking capability, the insulation layer design becomes tricky.

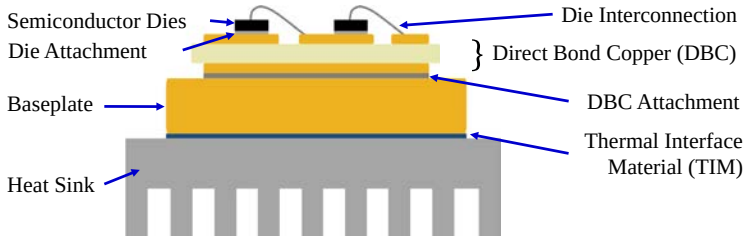


Figure 4.1 The Conventional Power Module Structure

A light-weight baseplate with good thermal conductivity and insulation capability is necessary for a high power-density medium voltage power module design. The thermal dissipation capability and material density of multiple baseplate materials are summarized in Table 4.1. The material thermal conductivity is from the datasheet of certain heatsink product, which value is lower than the pure material. In this chapter, Cu and Al are used to refer to the copper alloy and aluminum alloy heatsink material. Here, the term specific thermal conductivity is used, indicating the thermal dissipation capability per unit mass of the material. Cu, Al and AlSiC are electrically conductive materials, and AlSiC shows the highest specific thermal conductivity. The rest in Table 4.1 are insulated ceramic materials. BeO has higher thermal conductivity than Al and AlSiC, and the specific thermal conductivity is 1.35 times of AlSiC. The thermal conductivity of AlN is similar to Al, and the specific thermal conductivity of AlN is between Cu and Al. AlN could provide acceptable thermal dissipation capability of the baseplate. The comparison in Table 4.1 shows that AlN and BeO ceramic materials have similar or higher specific thermal conductivity than Cu, Al and AlSiC. Furthermore, the ceramic material can also provide electrical insulation between the power module internal electrical circuitry and the cooling

system. Since BeO powder may cause health issues to human body, AlN material is selected for this work.

Table 4.1 Comparison of Baseplate Material Property

Material	**Thermal Conductivity [W/mK]**	**Density [g/cm^3]**	**Specific Thermal Conductivity [(W/mK)/(g/cm^3)]**
Cu [10]	398	8.96	44.42
Al-6061 [14]	167	2.70	61.85
AlSiC-9 [13]	200	3.01	66.45
Al_2O_3 (96%) [15]	24	3.95	6.07
Si_3N_4 [15]	90	3.17	28.39
AlN [15]	170	3.26	52.14
BeO [10]	270	3.00	90

4.1.2. Power Density Comparison of Different Power Module Structures

In this section, the thermal performance and the power density of different power module structures with Al-6061 and AlN baseplates are evaluated and compared. In the comparison, the DBC and baseplate dimensions of different structures are identical. The baseplate is designed for direct liquid cool, and there is a pin fin structure on the bottom side of the baseplate. The dimension of the baseplate is 50 mm (L) by 34 mm (W) by 12 mm (H). The pin fin diameter is 2 mm and height 9 mm, as shown in the Figure 4.2.

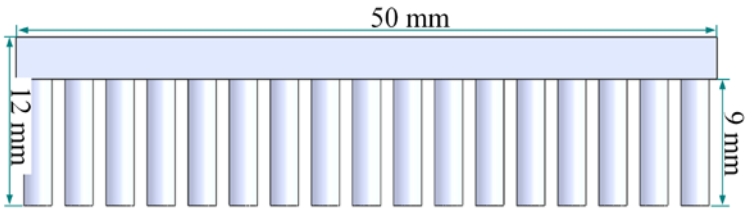


Figure 4.2 Dimensions of the pin fin baseplate

AlN baseplates provide additional insulation between the DBC and the cooling system. The electric circuit layout on the DBC layer becomes flexible, and the DBC bottom copper can be utilized for electric conduction. To keep the same flexibility in the DBC layout, an insulation layer between DBC and the Al baseplate is inserted.

Figure 4.3 shows four power module structures. In all the four structures, the DBC ceramic layer is 0.0125-inch AlN. The top and bottom Cu layer is 0.008 inch. The SiC MOSFET die is 6.44 mm long, 4.04 mm wide, and 0.18 mm thick. The die attachment layer is Sn63/Pb37 solder, 0.08 mm thick. Figure 4.3 (a) is the structure with an Al baseplate, the dark blue layer is an electrically insulated thermal interface material. The TIM thickness is 0.3 mm with 2 W/mK thermal conductivity. Figure 4.3 (b) is the structure with an Al baseplate. Additional DBC layer is inserted to provide electrical insulation. The attachment between DBCs and between DBC and baseplate is Sn63/Pb37 solder, 0.2 mm thick. Figure 4.3 (c) is the structure using an AlN baseplate with 0.01 mm copper metallization layer on the top flat surface. DBC is soldered to the metalized AlN baseplate, with the solder thickness 0.2 mm. Figure 4.3 (d) is the structure with an AlN baseplate. The TIM between DBC and the baseplate is graphic sheet, with in-plane thermal conductivity 1300 W/mK and through-plane thermal conductivity 20 W/mK. The total weight of the four structures is summarized in Table 4.2.

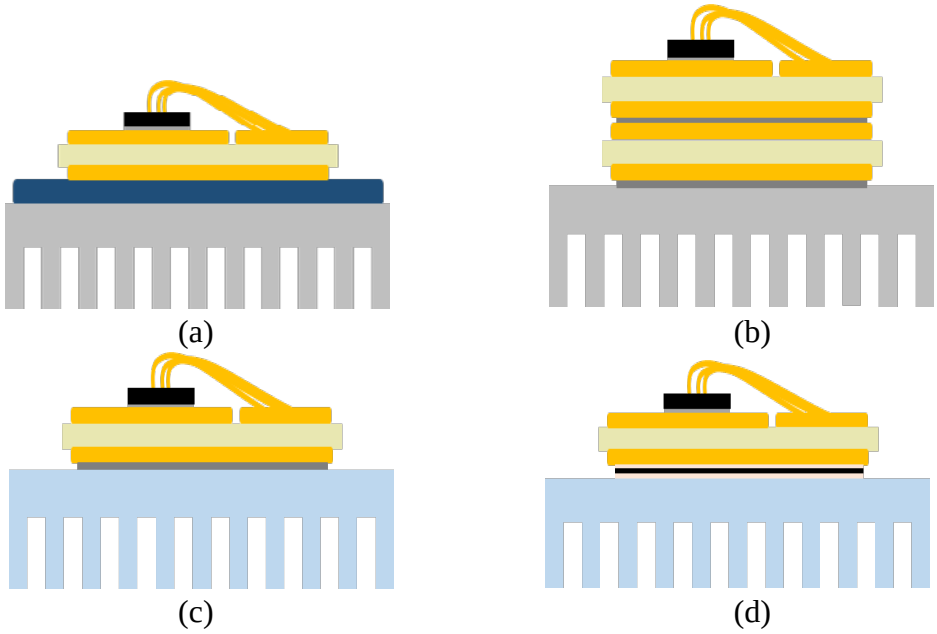


Figure 4.3 Four Power Module Structures with Al and AlN pin fin baseplates

The thermal performance of the four structures is evaluated with finite element analysis simulation, Ansys Icepak. Simulation models are built based on the four power module structures. In each simulation model, four semiconductor dies work as the heat source. 70 W loss is assigned to each die. The coolant is water with 10 L/min flow rate. The coolant temperature is set at 55 °C. With the same simulation conditions, the maximum junction temperatures of the four structures are extracted and summarized in Table 4.2.

Table 4.2 Thermal Performance Comparison of Different Power Module Structures

Power Module Structure	**Maximum Junction Temperature**	**Power Module Weight**
(a) DBC + TIM (Insulated) + Al baseplate	140.47 °C	25.73 g
(b) DBC + DBC + Al baseplate	114.16 °C	31.69 g
(c) DBC + Solder + AlN baseplate	112.85 °C	31.37 g
(d) DBC + Graphite + AlN baseplate	109.65 °C	30.52 g

The insulated TIM layer is the bottleneck in the thermal dissipation of structure (a), it sees the highest junction temperature among the four structures. Structure (a) could be used in the less thermal demanding weight sensitive applications. Among the other three designs, the structure with AlN baseplate provide better thermal dissipation capability as well as higher power density in terms of weight.

From the analysis above, the AlN baseplate could provide equivalent or better thermal dissipation capability and weight-wise power density than conventional metal based baseplate. Besides, the excellent insulation capability of the ceramic material makes the DBC design to be flexible.

4.2. Thermal Performance Improvement with Ceramic Design

The impacts of the DBC thickness and baseplate fin type on the thermal performance are discussed in this section.

4.2.1. Impact of the insulation layer thickness on the cooling capability

The cooling performance and the DBC thickness under the same simulation condition is not linearly related. A thinner DBC selection does not mean better cooling. A simulation model is built in Icepak to investigate the relationship. The model is shown in Figure 4.4. Four dies are simulated, with 70 W power loss per die. The DBC copper layer is 0.2 mm. The baseplate dimension is the same as that in Section 3.3.

The die attachment and DBC attachment can be either soldering or sintering. For different attachment combinations, the junction to baseplate thermal resistance are different. In the simulation, the attachment layers are not modeled, but are indirectly represented by different equivalent thermal resistance of the DBC insulation layer. In the

simulation, the DBC insulation layer thickness and equivalent thermal conductivity are the variables. The DBC insulation layer is selected as AlN, whose thermal conductivity is 170 W/mK. The solder thermal conductivity is around 65 W/mK, and silver sintering around 200 W/mK. So the equivalent thermal conductivity is selected as 150 W/mK and 200 W/mK. The thickness of the AlN layer are the common thickness of commercial DBCs, 0.01 inch, 0.025 inch, 0.04 inch, and 0.08 inch.

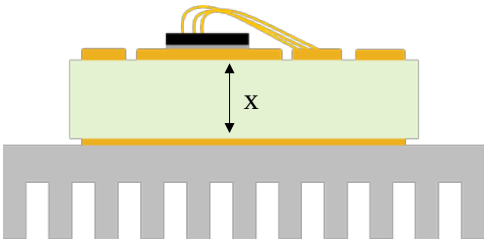
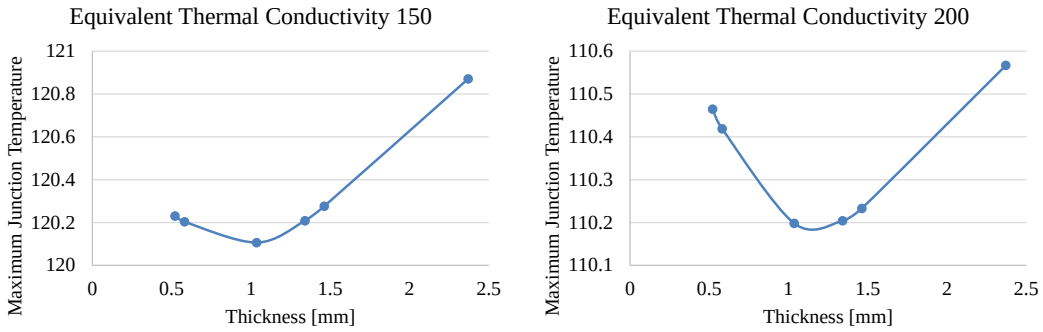


Figure 4.4 Thermal Simulation Model for DBC Thickness Impact

In the simulation, the coolant is water with 10 L/min flow rate, and the temperature is set at 55 ℃. The maximum junction temperature is selected to present the cooling performance under each variable. The results shown in Figure 4.5. In the figure, the x-axis is the total thickness of the AlN layer and top/bottom copper layer. That is, when the AlN layer is 0.025 inch, the thickness in the figure is 1.035 mm. To better show the trend, two more points are added, 0.5 mm and 1.5 mm thick. As shown in Figure 4.5, thinner DBC layer leads to higher maximum junction temperature. When the DBC total thickness is around 1 mm, the structure has the best cooling performance. Higher equivalent thermal conductivity leads to lower overall temperature. Use silver sintering as the die attachment and DBC attachment could help enhance the power module cooling capability. Also, for this specific case, 1 mm DBC total thickness gives best cooling performance.



(a) (b)

Figure 4.5 Relationship Between Maximum Junction Temperature and DBC thickness

4.2.2. Impact of the ceramic baseplate fin type on the cooling capability

The cooling capability can be further enhanced with advance fin design. From literature [56], the cone-shaped pins show the best cooling performance. In this part, the impact of the baseplate fin type on the overall cooling performance are investigated. With advanced ceramic 3D printing technology, complex fin types can be realized. AlN 3D printing is still quite challenging. On the other hand, less complex ceramic baseplate can be shaped with molds and fired. When this work is on-going, the ceramic manufacturing approaches are limited. The vendors could only be able to mill the AlN block to straight fin type or waveshape fin type. In this section, the following three types of baseplate fins are assessed. As shown in Figure 4.6 (a) and (d), the fins are cone shaped. The radius of the round side is 1 mm. The tail length is 2 mm. The distance between adjacent fins are 3.96 mm. In Figure 4.6 (b) and (e), the radius of the round pin fin is 1 mm, and the distance between adjacent fins are 3.96 mm. In Figure 4.6 (c) and (f), waveshape fins are used, the fin thickness and the channel width are 3 mm. In all the three designs, the base thickness is 3 mm, and the fin height is 9 mm. The maximum junction temperatures are summarized

in Table 4.3. As expected, the machinable waveshape fin baseplate gives the highest junction temperature. The maximum junction temperature is below 150 ℃ under the assigned power loss. The design can meet the system cooling requirement.

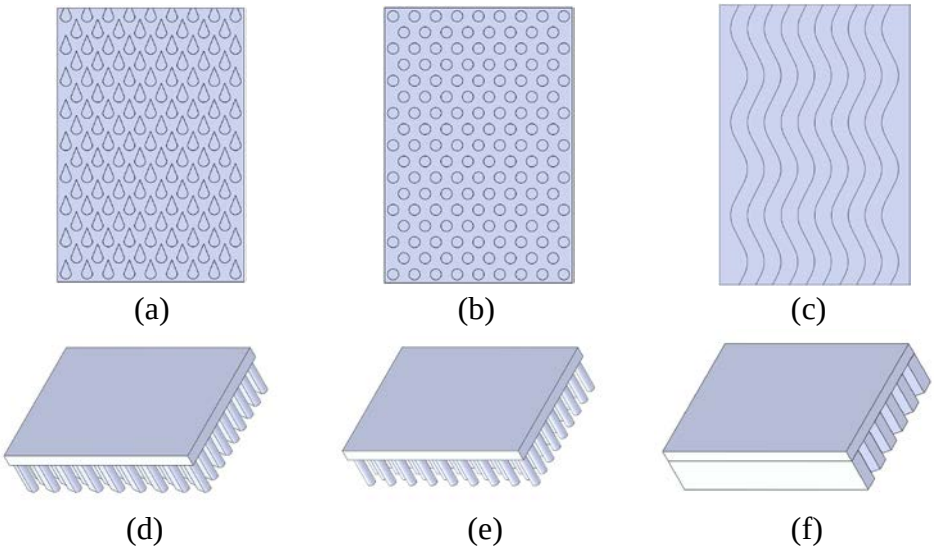


Figure 4.6 Ceramic baseplate designs for comparison

Table 4.3 Comparison of Baseplate Fin Design

Baseplate Fin Type	**Maximum Junction Temperature**
(a) Cone shaped pin fin	105.05 ℃
(b) Round pin fin	112.04 ℃
(c) Waveshape fin	140.56 ℃

4.3. Advantages in Electric Field Control

With insulated baseplates, the electric field for common mode voltage and differential mode voltage can be decoupled. This will reduce the difficulty in the medium voltage power module insulation design.

High electric field strength causes partial discharge or even insulation breakdown inside the power module. The electric field distribution comparison under both differential

mode (DM) voltage excitation and common mode (CM) voltage excitation are investigated in this section.

Simplified Maxwell electrostatic 2D models with metal and ceramic baseplates are built. The substrate thickness is 0.635 mm, and the copper thickness is 0.2 mm. The baseplate total height is 12 mm, and the pin height is 9 mm. The distance between the substrate top Cu traces is 1 mm. The module is designed for 1200 V SiC MOSFETs, so the DM excitation voltage is selected as 900 V. And the CM excitation voltage is 2,400 V according to standard IEC 60950.

Figure 4.7to Figure 4.10 illustrate the electric field distribution for conventional power module structure and the proposed 1200 V power module structure with ceramic baseplates. In both structures the electric field concentrates at the triple point where copper, ceramic and encapsulation gel join, and at the location inside the substrate ceramic layer near the triple point. In these figures, the critical points are labeled as P1 and P2. P1 is inside the encapsulation gel, 50 μm away from the adjacent edges of the Cu trace and the substrate insulation layer. P2 is inside the substrate insulation layer, right beneath the Cu trace edge and 50 μm away from insulation layer edge. The corresponding electric field strength at those critical points are summarized in Table 4.4.

The simulation results in Figure 4.7 and Figure 4.8 show that in the conventional power module structure, both DM and CM voltage isolations are provided by the substrate insulation layer. As shown in Table 4.4, the electric field strength under CM voltage is three times of that under DM voltage, so the substrate insulation layer thickness is determined by the maximum electric field strength under CM voltage.

The simulation results in Figure 4.9 and Figure 4.10 show that in the proposed power module structure, the DM voltage isolation is provided by the substrate insulation layer. The CM voltage is sustained by the ceramic baseplate. The decoupling of these two factors brings benefits and simplicity of the power module design. Lower insulation voltage requirement on the substrate leads to cost-effective choices of the substrate. In the proposed structure, the substrate insulation layer thickness is determined by the maximum electric field strength under DM voltage, which is about 50% of the value required in the conventional structure. Furthermore, thanks to the larger thickness of the ceramic baseplate than that of the substrate, CM electric field strength is largely reduced and easily controlled in the proposed structure.

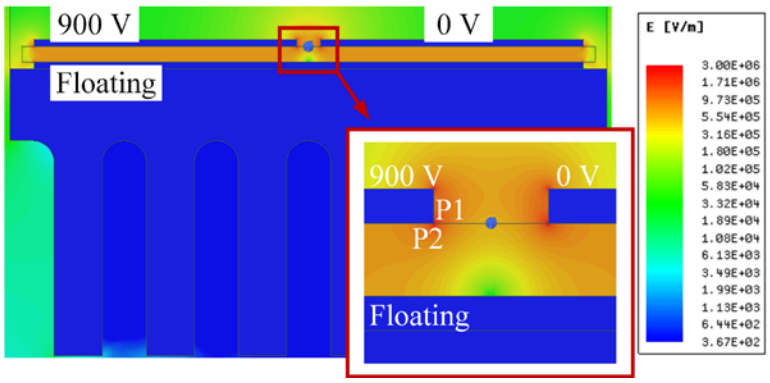


Figure 4.7 Conventional power module structure DM electric field distribution under 900 V.

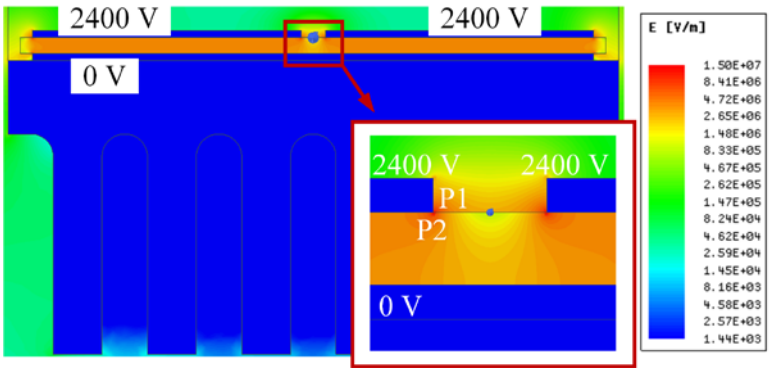


Figure 4.8 Conventional power module structure CM electric field distribution under 2,400 V.

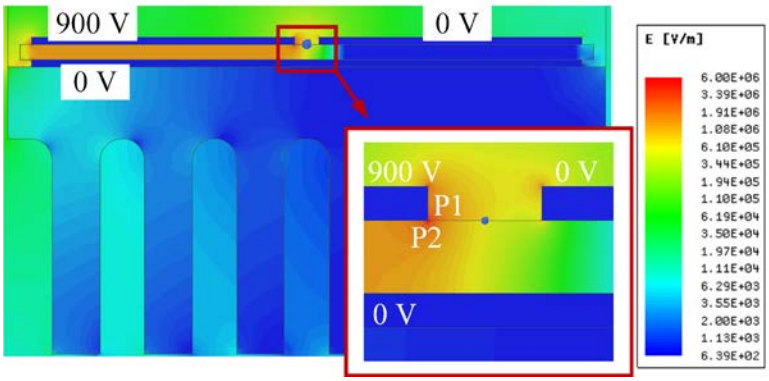


Figure 4.9 Vertical loop power module structure DM electric field distribution under 900 V.

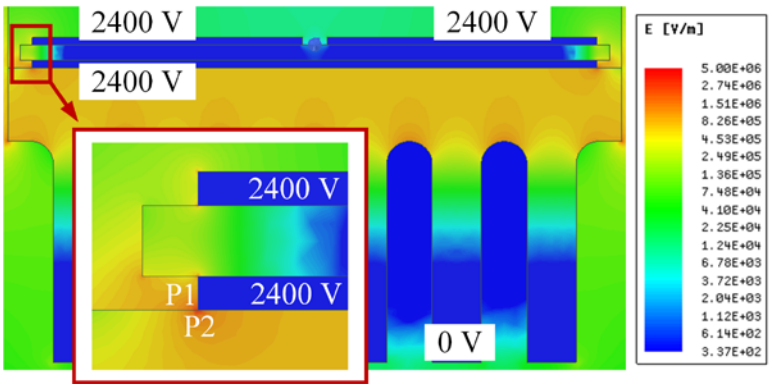


Figure 4.10 Vertical loop power module structure with the ceramic baseplate CM electric field distribution under 2,400 V.

Table 4.4 Comparison of Electric Field Strength for Both Structures

Structure and Excitation	**P1 [kV/mm]**	**P2 [kV/mm]**
Conventional, DM 900 V	1.55	1.38
Conventional, CM 2400 V	5.31	5.68
Proposed, DM 900 V	2.53	2.44
Proposed, CM 2400 V	1.59	1.50

This benefit is very attractive to the 3,300 V and higher rated SiC MOSFET package. With the vertical loop layout proposed in Figure 3.2, the bottom copper layer is connected to the half dc bus voltage potential. The electric field distribution under DM and CM voltage stress are simulated and shown in Figure 4.11to Figure 4.14. In the DM electric field simulation, the voltage excitation is the device rated voltage, 3300 V for both cases. The applied CM voltage is 7,600 V. The electric field stress under the four conditions is summarized in Table 4.5.

With the split dc bus design, under the DM voltage excitation, mid dc voltage return trace help reduce the electric field strength across the DBC insulation layer. The simulated electric field strength is identical to that of the conventional structure. The CM electric

field strength of the 3,300 V power module is shown in Figure 4.14. Due to relatively large size of the ceramic baseplate, the electric field strength is largely reduced. In the area where the base and fin joins, the electric field strength is larger, around 4.6 kV/mm.

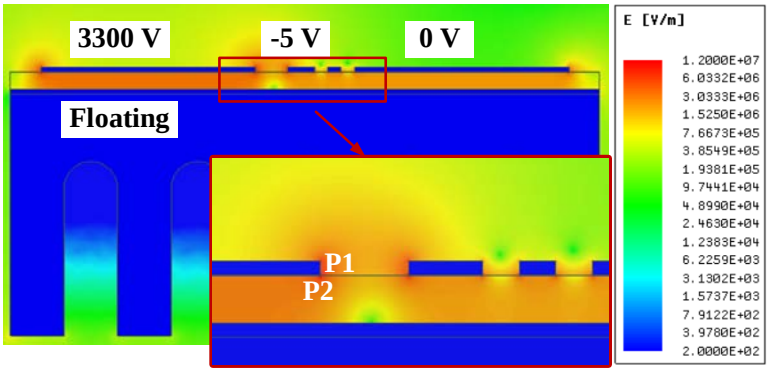


Figure 4.11 Conventional power module structure DM electric field distribution under 3,300 V.

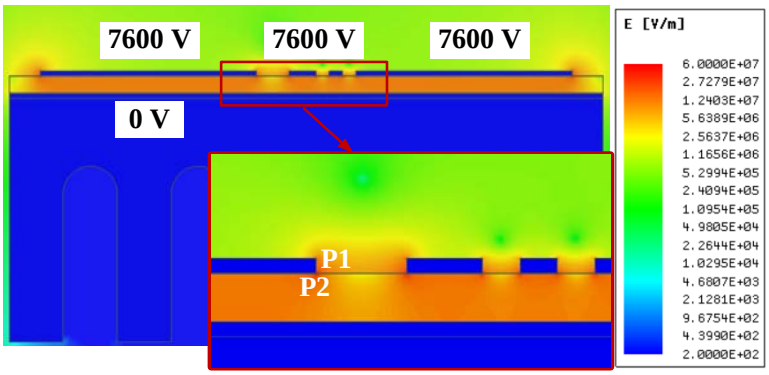


Figure 4.12 Conventional power module structure CM electric field distribution under 7,600 V.

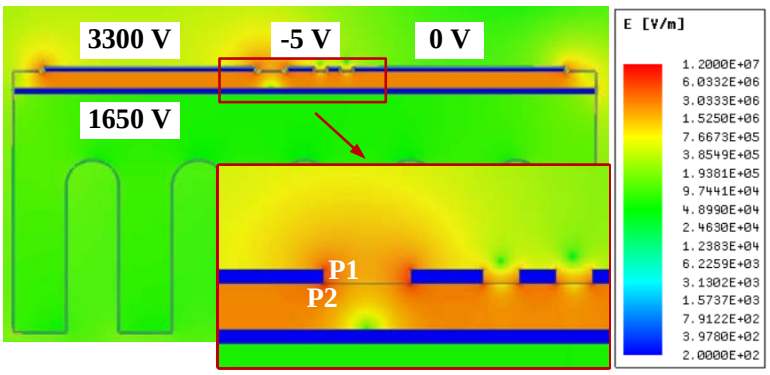


Figure 4.13 Vertical loop power module structure with AlN baseplate DM electric field distribution under 3,300 V.

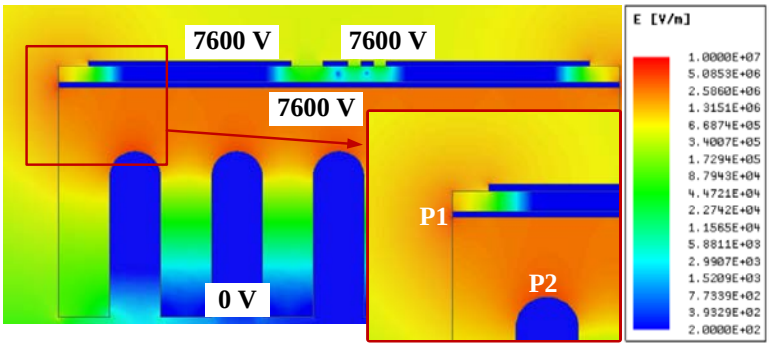


Figure 4.14 Vertical loop power module structure with AlN baseplate CM electric field distribution under 7,600 V.

Table 4.5 Comparison of Electric Field Strength for 3300 V Power Module Design

Structure and Excitation	P1 [kV/mm]	P2 [kV/mm]
Conventional, DM 3300 V	5.46	4.85
Conventional, CM 7600 V	17.83	19.27
Proposed, DM 3300 V	5.46	4.85
Proposed, CM 7600 V	2.28	4.6

4.4. Advantages in Leakage Current Reduction

The parasitic capacitance between substrate top surface electric circuitry and earth ground provides a path for the CM current. Reducing this parasitic capacitance can reduce the common current during converter operation.

Power module designs in [44]-[45] and [49] include an additional layer as integrated electromagnetic interference (EMI) shielding. Between the shielding layer and conductive heatsink, another insulation layer has been added. The electric field distribution and the common mode noise improvement using these three designs are discussed. However, detailed modeling of parasitic capacitance and the analysis on their influence are not available.

In conventional power modules, the baseplate and heatsink are metal, and the TIM layer are typically electrically conductive for better thermal conductivity. Since the heatsink and baseplate are grounded to earth, the parasitic capacitances are distributed between the substrate top copper pads and bottom copper pad, as shown in Figure 4.15 (a). The corresponding CM equivalent circuit of this structure is shown in Figure 4.15 (c).

In the proposed vertical loop structure with the ceramic baseplate, the ceramic baseplate is insulated. This additional insulation layer forms the serial connected capacitance between the substrate bottom copper pad and the earth ground. Besides, the parasitic capacitance between substrate top DC negative Cu trace and substrate bottom Cu trace is eliminated. The CM equivalent circuit of this structure is shown in Figure 4.15 (d).

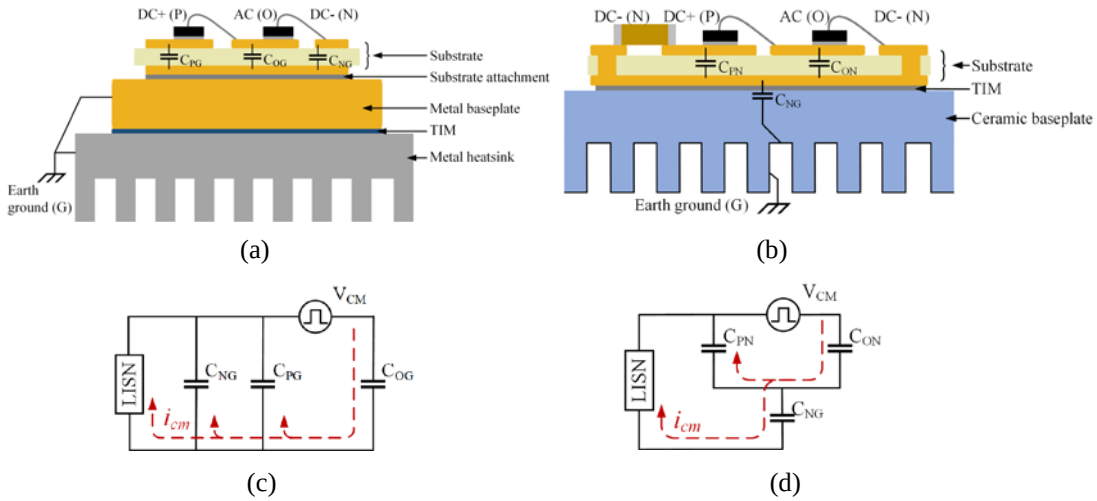


Figure 4.15 Package parasitic capacitance distribution and CM equivalent circuits (a) the parasitic capacitance in the conventional structure (b) the parasitic capacitance in the proposed structure (c) the CM equivalent circuit of the conventional structure (d) the CM equivalent circuit of the proposed structure

To reduce the parasitic capacitance, thicker insulation layers are preferred. FEA models of both the conventional power module structure and the proposed structure are imported into the Maxwell Q3D to extract the parasitic capacitance values. The dimensions of substrate Cu pads are shown in Figure 4.16. The traces for gate connections are not included. The conventional substrate layout is circled with the dashed lines. In the proposed structure, an extra DC negative trace (25 mm by 6.5 mm) is added to form the vertical loop. Based on the CM equivalent circuit in Figure 4.15, the relationship between the CM leakage current (i_{cm}) and the insulation layer thickness is derived and plotted in Figure 4.17. When calculating the CM leakage current, the thickness of the ceramic baseplate is adjusted, and the parasitic capacitance changes correspondingly. A CM voltage source with 1 V amplitude and 35 MHz frequency is used. The impedance of the line impedance stabilization network (LISN) refers to the IEC standard CISPER 25.

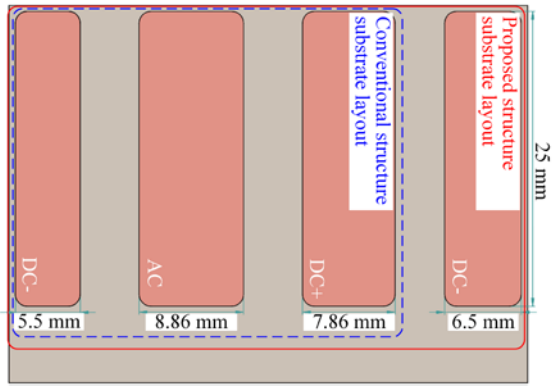


Figure 4.16 Dimensions of the substrate layout

In Figure 4.17, the dashed line is the leakage current of the conventional structure. In the proposed structure, the thicker the insulation layer, the smaller parasitic capacitance, and the smaller leakage current. The insertion of the insulation layer does not necessarily reduce the CM leakage current. There is a minimum thickness of the insulation layer to achieve leakage current reduction for a specific material. Additionally, the insulation material with smaller dielectric constant (ε) requires thinner insulation layer for leakage current reduction.

Then, the CM leakage current is investigated across the frequency range of 150 kHz to 108 MHz. The dimension of the AlN baseplate is 50 mm long, 34 mm width, 12 mm high. The heatsink in the conventional structure is identical to the ceramic baseplate in the proposed structure. The substrate insulation material is also AlN. The extracted parasitic capacitance of both structures is summarized in Table 4.6.

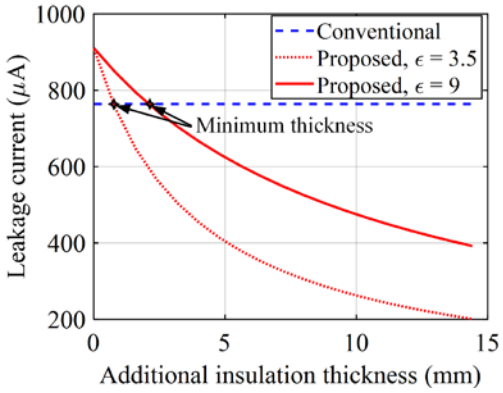


Figure 4.17 Comparison of the CM leakage current with different insulation materials under varying insulation layer thicknesses.

Table 4.6 Summary of the Package Parasitic Capacitance

Conventional		**Proposed**	
C_{PG} [pF]	26.68	C_{PN} [pF]	27.35
C_{OG} [pF]	29.81	C_{ON} [pF]	30.48
C_{NG} [pF]	17.25	C_{NG} [pF]	6.22

Shown in Table 4.6, with the AlN baseplate, the parasitic capacitance between CM noise source to earth ground, C_{OG}, is reduced by 89.5%. The CM leakage current across 150 kHz to 108 MHz of both structures is shown in Figure 4.18. At higher frequency, the leakage current increases. In the range of 3.5 MHz to 35 MHz, At least 47.3 % CM leakage current reduction is observed in the proposed structure. Thus, the utilization of ceramic baseplate is an effective way to reduce the CM leakage current.

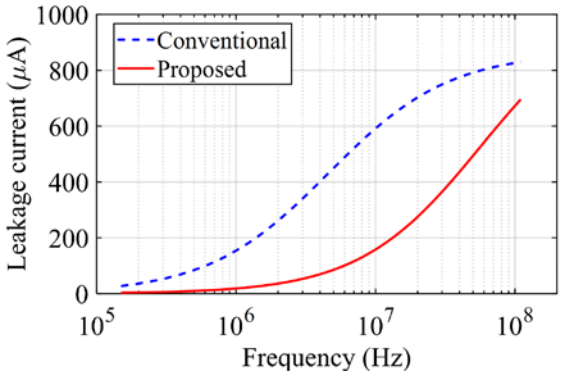


Figure 4.18 Comparison of the CM leakage current under varying frequency.

4.5. Power Module Liquid Cool Assembly Design

To achieve low weight high power density design, the power module with the AlN baseplate adopts direct liquid cooling. The liquid cooling housing is also integrated with the power module. Steel and Al are the common sink material for liquid cool system. To reduce the weight of the cooling housing, high temperature plastic materials are reviewed. To expedite the design process, the housing is 3D printed. Among the common 3D printer filament, Nylon melt temperature is around 200 °C. During the test, the semiconductor die junction temperature is controlled below 150 °C, so Nylon can meet the temperature requirement. Also, the material density of Nylon is only 43% of Al, which provides smaller total weight of the whole assembly. During 3D printing, a relatively high percentage fill is recommended for waterproof design. Coolant will penetrate through the walls with less than 40 % fill.

The power module assembly is shown in Figure 4.19, including the dedicated gate drive board, the power stage, the layer of liquid metal based thermal interface material (TIM), the graphite layer, the AlN baseplate, and the integrated liquid cooling housing.

Figure 4.20 shows the integrated gate drive board design. On this gate drive board, isolated dc-dc power supply and isolated gate drive IC are integrated. The common mode transient immunity is 100 V/ns, which can cover most medium voltage SiC MOSFET high speed operation. To power up the designed half-bridge power module, only a 5 V power supply is needed. The PWM control signals can be directly connected to the low voltage controller. This design could simply the power supply structure and signal isolation of the whole converter system.

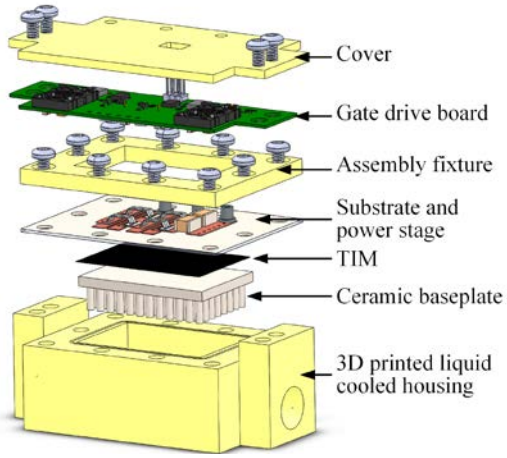


Figure 4.19 Liquid cooled power module assembly design.

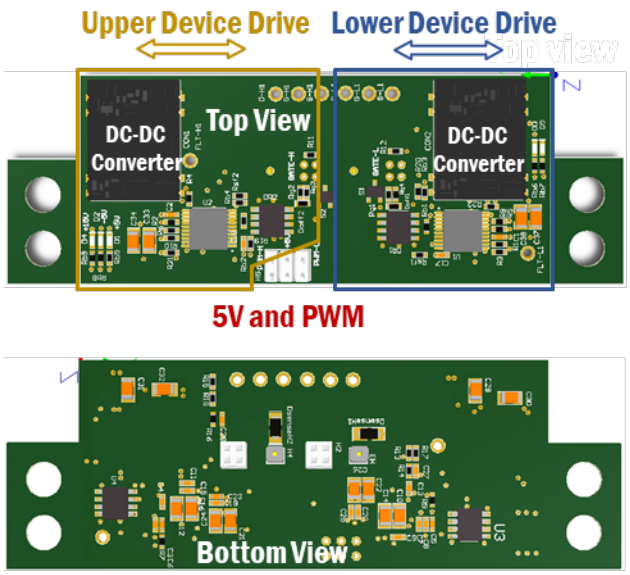


Figure 4.20 Integrated gate drive board design.

4.6. Summary

In this chapter, the ceramic material is assessed to be used as the baseplate in the power module design. As the integrated baseplate, AlN and BeO can provide equivalent or better thermal performance than the widely used aluminum alloy. At the same time, ceramic baseplate can provide electrical insulation, making the DBC layout to be flexible. Simulation results show that the utilization of the ceramic baseplate reduces the maximum electric field strength, simplifies the power module internal isolation design, and mitigates the CM leakage current. The impact of DBC thickness and baseplate fin type are discussed with simulation results. For this specific case, 1 mm AlN DBC gives the best cooling performance. To achieve low weight high power density power module design, direct liquid cooling is also integrated. The liquid cooling housing material selection is also discussed. The final power module assembly is shown at the end of this chapter. This

proposed design is a simple and beneficial package method for medium voltage SiC MOSFETs.

Chapter 5. Super-Cascode Structure Circuit Analysis and Dynamic Voltage Balancing

The medium voltage SiC discrete MOSFETs and power modules have drawn more and more attention to various medium voltage and high voltage application. The design and manufacture process need to be improved to enhance devices' reliability under harsh operation conditions. However, the adoption of the medium voltage SiC power devices has been impeded by its high cost. An economic alternative for medium voltage power switch is the super-cascode structure. The super-cascode structure is composed of series connected low voltage MOSFET and normally-on junction gate field-effect transistors (JFETs). The voltage balancing among series connected devices is realized by the added capacitors and diodes. Circuit models during the switching transients are built. Based on the developed models, a method to optimize the voltage balancing circuit parameters is proposed. The analysis and optimization method are verified by the experimental results. Sensitivity analysis is conducted to see the impact of the capacitance tolerance.

5.1. Review of Cascode Structure

The super-cascode structure was first proposed in 2008 [60]. To improve switching speed, a structure with active gate voltage control circuit for all the series-connected discrete package JFETs was proposed and demonstrated [63]-[64]. To reduce static leakage current under high blocking voltage, an improved structure is proposed [65]. Even though more attention is typically drawn to the super-cascode structure, the investigation of voltage distribution across series connected JFETs remains incomplete.

This chapter focuses on voltage balancing of JFETs inside super-cascode switches, which has not been sufficiently addressed in earlier publications. The necessity and function of the voltage balancing circuit was first discussed in [63], but the method for voltage balancing capacitance selection is not discussed in detail. Even though mathematical models of the single cascode structure are explained in [68] for the super-cascode structure, the process presents complicated mathematical expression and tremendous calculation efforts, preventing the model's use for the voltage balancing capacitance selection.

The typical SCPS voltage balancing circuit is composed of clamping diodes, current limiting resistors and voltage balancing capacitors, as shown in Figure 5.1. Within each, the voltage balancing capacitors determine the voltage distribution among internal JFETs, affecting the switching loss during switching transients. Correct capacitance selection can also reduce the avalanche loss of the diodes in the balancing circuits and the JFET voltage overshoot. Thus, it is critical to have an analytical model to enable the optimization of the capacitance.

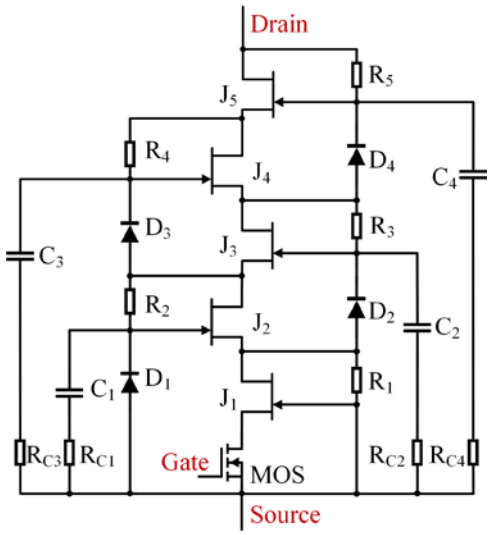


Figure 5.1 The super-cascode structure

Section 5.2 of this chapter explains the turn-off process of the SCPS, and the impact of the voltage balancing capacitors. The Section 5.3 explains the turn-on process of the SCPS and the potential top JFET overvoltage issue. Section 5.4 proposes the SCPS voltage balancing capacitor selection method and discusses the impact of the capacitance variation on the voltage distribution. In Section 5.5, the test results demonstrate the effectiveness of the proposed capacitance optimization method. The last section summarizes the work.

5.2. Super-Cascode Power Switch Dynamic Voltage Distribution

The typical 5-stage super-cascode structure contains series-connected normally-on SiC JFETs, J1 to J5, is shown in Figure 5.1. The bottom device in the structure is a low voltage silicon MOSFET. The clamping diodes D1 to D4 limit the JFET drain to source voltage to the diode's avalanche voltage V_{aval}. C1 to C4 are connected between JFETs' gate terminals, and the source of the MOSFET through resistors R_{C1}, R_{C2}, R_{C3} and R_{C4}.

5.2.1. Super-Cascode Power Switch Turn-off Process

The turn-off process of the SCPS is divided into two stages:

Stage I: This stage starts when V_{gs_SCPS} is below its threshold voltage. The MOSFET turns off and starts to block the voltage applied to the SCPS. The voltage across the MOSFET becomes negative bias between the gate and source of J1. J1 turns off, and V_{ds_J1} increases. C1 is then charged through C_{iss_J2}, reducing V_{gs_J2}. The charging path is shown as red solid line in Figure 5.2 (a). Meanwhile, since J2 to J5 are still on, C2 to C4 are charged through D2 to D4. The capacitor charging paths are shown as blue dashed lines in Figure 5.2 (a). When V_{ds_J2} starts to increase, this stage ends.

Stage II: This stage begins when V_{ds_J2} starts to increase, charging C1 through the reverse transfer capacitance of J2, C_{rss_J2}. C1 voltage follows V_{ds_J1}, thus the drain to source voltage ratio of J1 and J2 is determined by C1. C2 is charged through C_{iss_J3}, reducing V_{gs_J3}. The charging path is shown as red solid lines in Figure 5.2 (b). Since J3 to J5 are still on, C3 and C4 are charged through D3 and D4. The capacitor charging paths are shown as blue dashed lines in Figure 5.2 (b). When V_{gs_J3} drops beneath the threshold voltage, V_{ds_J3} starts to increase. The same process repeats until J5 fully turns off.

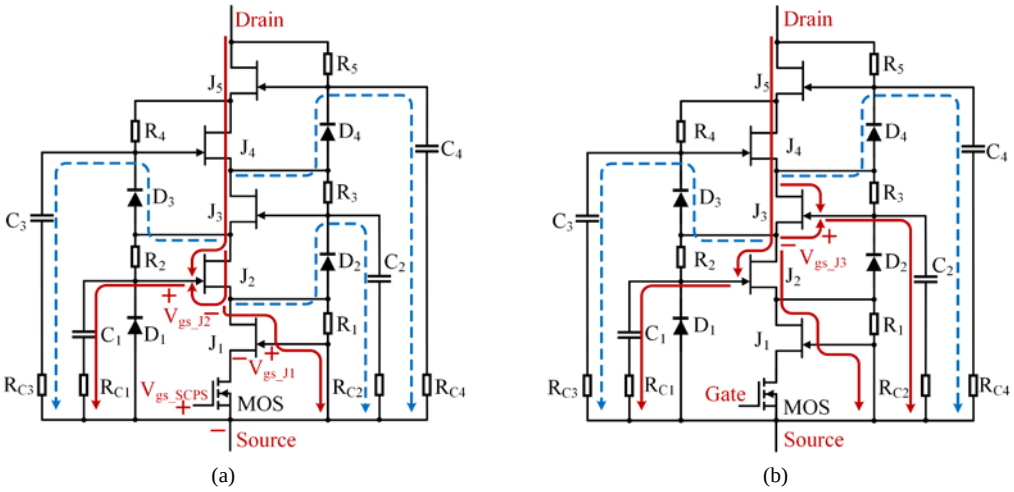


Figure 5.2 The voltage balancing capacitor charging path (a) Stage I, MOSFET and J1 turns off (b) Stage II, J2 to J5 turns off.

5.2.2. Modeling of Dynamic Voltage Distribution During Turn-off Transients

The voltage balancing capacitors have significant impact on the JFET voltage distribution. In this section, a mathematical model is proposed to quantify the effect of the voltage balancing capacitors. As shown in Figure 5.2, the added voltage balancing capacitor C_1 and clamping diode junction capacitance C_{D1} are in series with J_2's input capacitor, C_{iss_J2}. The change of J_1's drain to source voltage and the change of J_2's gate to source voltage is expressed as:

$$\left(\Delta V_{ds\_J1\_I} + \Delta V_{gs\_J2}\right) \times \left(C_1 + C_{D_1}\right) = -\Delta V_{gs\_J2} \times C_{iss\_J2} \qquad (5\text{-}1)$$

$$\Delta V_{gs\_J2} = V_{gs\_on} - V_{gs\_miller} \qquad (5\text{-}2)$$

$\Delta V_{ds\_J1\_I}$ is the J_1 drain to source voltage change during Stage I, before V_{ds_J2} starts to increase. V_{gs_on} is the JFET gate to source voltage during the on state. V_{gs_miller} is the JFET miller plateau voltage. Since ΔV_{gs_J2} is much smaller than $\Delta V_{ds\_J1\_I}$, the equation (5-1) can be rewritten as

$$\Delta V_{ds\_J1\_I} = \frac{-\Delta V_{gs\_J2} \times C_{iss\_J2}}{C_1 + C_{D_1}} \quad (5\text{-}3)$$

Thus, before V_{ds_J2} starts to increase, $\Delta V_{ds\_J1\_I}$ is determined by C1 capacitance.

In Stage II, the charging current of C1 and C_{D1} flows through J2's reverse transfer capacitor C_{rss_J2}. Omitting the voltage increase of the low voltage MOSFET, the voltage increase on C1 is the same as the voltage increase on J1. Thus, the drain to source voltage change of J1 and the drain to source voltage change of J2 is expressed as:

$$\frac{\Delta V_{ds\_J1\_II}}{\Delta V_{ds\_J2\_II}} = \frac{C_{rss\_J2}}{C_1 + C_{D_1}} \quad (5\text{-}4)$$

$\Delta V_{ds\_J1\_II}$ is J1 drain to source voltage change during Stage II, as V_{ds_J2} increases. $\Delta V_{ds\_J2\_II}$ is J2 drain to source voltage change during Stage II. Thus, knowing JFET reverse transfer capacitor, the ratio between J1 and J2 drain to source voltage change can be adjusted by properly selecting C1.

Similarly, as V_{ds_J2} increases, J3's input capacitance is charged. In a N-stage super-cascode structure, before V_{ds_Ji} increases, the relationship between ΔV_{gs_Ji} and $\Delta V_{ds\_J(i-1)}$ is expressed as:

$$\Delta V_{gs_{Ji}} \times C_{iss_{Ji}} = C_{(i-1)} \times \left(\sum_{k=1}^{k=i-1} \Delta V_{ds_{Jk}} + \Delta V_{gs_{Ji}} \right) + C_{D_{(i-1)}} \times \left(\Delta V_{ds\_J(i-1)} + \Delta V_{gs\_Ji} \right) \quad (5\text{-}5)$$

$$\Delta V_{gs\_Ji} = V_{gs\_on} - V_{gs\_miller} \quad (5\text{-}6)$$

During the time when V_{ds_Ji} increases, ΔV_{ds_Ji} can be expressed by equation (5-7).

$$C_{rss\_Ji} \times \Delta V_{ds\_Ji} = C_{(i-1)} \times \sum_{k=1}^{k=i-1} \Delta V_{ds\_Jk} + C_{D(i-1)} \times \Delta V_{ds\_J(i-1)} \quad (5\text{-}7)$$

By omitting the junction capacitance of the clamping diode, the voltage range ratio between adjacent JFETs can be calculated with

$$\frac{\Delta V_{ds\_Ji}}{\Delta V_{ds\_J(i-1)}} = \frac{C_{(i-1)}}{C_{rss\_Ji}} \times \left(\frac{C_{rss\_J(i-1)}}{C_{(i-2)}} + 1 \right) \tag{5-8}$$

The total blocking voltage of the super-cascode module is the summary of the voltage increase of all JFETs during all the stages. Therefore, the voltage distribution of the internal JFETs is effectively adjusted by the voltage balancing capacitors.

5.3. Super-Cascode Power Switch Overvoltage Issue During Turn-on Transients

So further improve the converter efficiency and to extend the life time of those higher cost power

5.3.1. Super-Cascode Power Switch Turn-on Process and Overvoltage Issue

Without proper voltage balancing circuit design, the top JFET can be damaged by overvoltage during the SCPS turn-on transient. The overvoltage issue is illustrated in this part by explaining and modeling the turn-on process.

The turn-on of the JFETs is also a sequential process, which is described next.

Stage I: this stage begins when V_{gs_SCPS} is above its threshold voltage and ends when V_{gs_J2} is above its threshold voltage. During this stage, J2 to J5 remain off. As V_{ds_J1} decreases, the discharging current of C1 and C_{D1} flows through C_{gs_J2}. V_{ds_J2}, V_{ds_J3}, V_{ds_J4}, and V_{ds_J5} increase to compensate the decrease of V_{ds_J1} before SCPS drain to source voltage decreases.

Stage II: this stage begins when V_{gs_J2} is above the threshold voltage. During this stage, V_{ds_J2} starts to decrease, and V_{ds_J3}, V_{ds_J4}, and V_{ds_J5} increase to compensate the decrease

of V_{ds_J2} and V_{ds_J1}. J3 source voltage decreases and C2 and C_{D2} discharge through C_{gs_J3}, increasing V_{gs_J3}. A similar turn-on process repeats for J3 to J5.

During Stage II, whether the diode avalanches or not determines the effectiveness of voltage balancing capacitors. Taking the example of the turn-on process of J2, there are two possible scenarios:

Scenario 1): When V_{gs_J2} is below the threshold voltage, V_{ds_J2} increases to the avalanche voltage of the clamping diode. With D2 avalanching, as V_{ds_J1} and V_{ds_J2} decrease, the discharging current of C2 flows through D2, and C_{gs_J3} is not charged, as shown in Figure 5.3 (a). Until V_{ds_J2} decreases below J3's gate threshold voltage, J3 starts to turn on. Thus, there is a long delay between the turn-on of J2 and J3.

Scenario 2): V_{ds_J2} stays below the avalanche voltage of the clamping diode. When V_{gs_J2} is above the threshold voltage, V_{ds_J2} starts to decrease, and C2 and C_{D2} discharging current flows through C_{gs_J3} and increases V_{gs_J3}, as shown in Figure 5.3 (b). In this scenario, the voltage balancing capacitor accelerates the JFET turn-on. If the clamping diodes do not avalanche, a similar turn-on process occurs with J4 and J5. C3 and C4 then help to charge V_{gs_J4} and V_{gs_J5}, respectively, and accelerate the turn-on of J4 and J5. With the assistance of voltage balancing capacitors, the delay between JFETs during the sequential turn-on process is reduced, leading to a shorter total turn-on time of the SCPS.

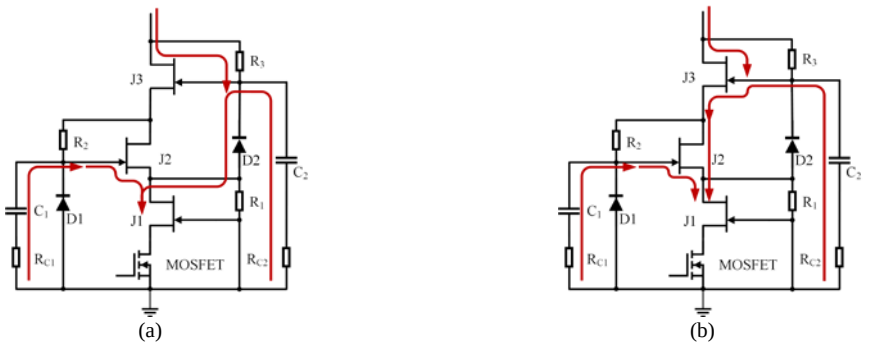
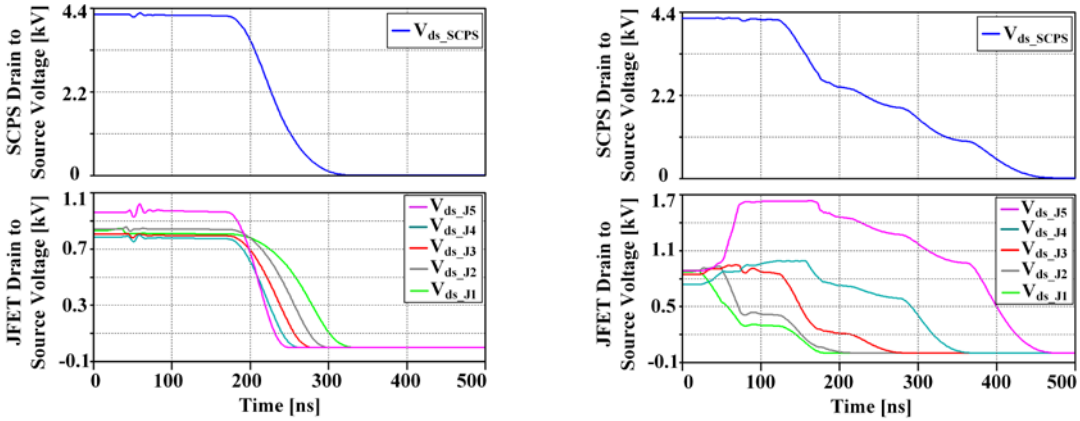


Figure 5.3 Voltage balancing capacitor discharging current path (a) Scenario 1, D2 avalanches (b) Scenario 2, D2 does not avalanche.

The overvoltage issue happens when D4 avalanches during the turn-on process. J5 stay off until V_{ds_J4} decreases below J5's gate threshold voltage. J5 has to withstand a large portion of the blocking voltage as the drain to source voltage of J1 to J4 decreases. The overvoltage on J5 can be eliminated by simply paralleling an avalanche diode with J5. However, under Scenario 1, the added diode may experience long avalanche time, which can lead to high thermal stress and early degradation of the clamping diode. To reduce thermal stress and ensure reliable operation of the SCPS, it is necessary for V_{ds_J5} to fall below its rated voltage during the turn-on process.

The simulation results in Figure 5.4 show the comparison between Scenario 1 and 2. Here, the SCPS switches at 4,250 V dc bus voltage and 30 A load current. The upper plot is the SCPS module's overall drain to source voltage, and the lower plot contains the drain to source voltages of J1 to J5. As V_{ds_J1} decreases, upper JFETs drain to source voltages increase and reach the avalanche voltage of the clamping diodes. V_{ds_J5} stays above 1200 V for more than 250 ns in every turn-on transient. Figure 5.4 (b) represents Scenario 2 with optimized voltage balancing capacitors. When none of the clamping diodes avalanches,

the voltage balancing capacitors help increase JFET gate to source voltage, and the voltage on all JFETs decreases simultaneously. This greatly reduces the turn-on delay between JFETs. The SCPS total drain to source voltage fall-time is shortened to 1/3 of the fall time under avalanche condition.



(a) Clamping diodes avalanche

(b) Clamping diodes do not avalanche

Figure 5.4 Simulated SCPS and JFET drain to source voltage during the turn-on transient

5.3.2. Analytical Modeling of the Dynamic Voltage Change During Turn-on Transients

Based on the circuit diagram shown in Figure 5.1 and Figure 5.3 (b), when the SCPS turns on, V_{ds_J5} increases, the relationship between voltage changes of V_{ds_J5} and V_{gs_J5} is found based on capacitance charge balance.

$$\left(C_{rss\_J5} + C_4\right) \times \left(\Delta V_{ds\_J5} - \Delta V_{gs\_J5}\right) = C_{gs\_J5} \times \Delta V_{gs\_J5} \tag{5-9}$$

The voltage change of V_{gs_J5} is calculated as

$$\Delta V_{gs\_J5} = \Delta V_{ds\_J5} \times \frac{C_{rss\_J5}+C_4}{C_{iss\_J5}+C_4} \tag{5-10}$$

From Equation (5-10), it reveals a larger C4 can lead to quicker V_{gs_J5} change, meaning earlier turn-on of J5.

Meanwhile, the equivalent circuit to quantify the voltage change ratio between V_{ds_J5} and V_{D4} is shown in Figure 5.5 (a). When the JFETs are under high blocking voltage, Cgs is above 10 times of C_{rss}, and C_{rss} is above 10 times of C_{ds}. The equivalent circuit in Figure 5.5 (a) is simplified to the circuit in Figure 5.5 (b). Compared to ΔV_{ds_J5}, ΔV_{gs_J5} and ΔV_{gs_J4} are neglected, and ΔV_{D4} equals ΔV_{ds_J4}. The relationship between ΔV_{ds_J5} and ΔV_{D4} are expressed as:

$$\Delta V_{D4} \times C_{rss\_J4} = \left(C_{rss\_J5} + C_4\right) \times \Delta V_{ds\_J5} \tag{5-11}$$

When J5 starts to turn on, D4 voltage is below its avalanche voltage, and V_{ds_J5} is below 1,200 V. The initial voltage of D4 is the voltage during off state.

Similarly, the gate to source voltage of J_i, ΔV_{gs_Ji}, and the drain to source voltage change, $\Delta V_{ds\_J(i-1)}$, are also derived as:

$$\Delta V_{gs\_Ji} = \Delta V_{ds\_Ji} \times \frac{C_{rss\_Ji} + C_{(i-1)}}{C_{iss\_Ji} + C_{(i-1)}} \tag{5-12}$$

$$\Delta V_{ds\_J(i-1)} = \Delta V_{ds\_Ji} \times \frac{C_{rss\_Ji} + C_{(i-1)}}{C_{iss\_J(i-1)}} \tag{5-13}$$

For a SCPS with *N* JFETs, in equations (12) and (13), index *i* is between 2 and *N*.

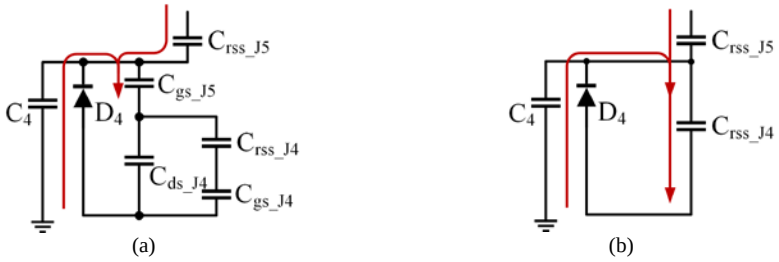


Figure 5.5 Current path during turn-on transient (a) in equivalent circuit (b) in simplified equivalent circuit.

5.4. Super-Cascode Power Switch Balancing Circuit Parameter Optimization

This part proposes the SCPS balancing circuit parameter optimization method and analyzes the influence of capacitor tolerance on the dynamic voltage distribution.

5.4.1. Super-Cascode Power Switch Balancing Circuit Parameter Optimization Method

The purpose of the optimization is to realize internal voltage balance during the turn-off transient and avoid overvoltage on the top JFET during the turn-on transient. Thus, the optimization constraint is the voltage increase on J5 during the turn-on process. The optimization cost function is the summation of differences between JFETs' blocking voltage and the diodes' avalanche voltage. The optimization inputs are the SCPS rated voltage, diode avalanche voltage, and JFET gate threshold voltage.

The first step in the optimization procedure is to calculate the voltage distribution during the turn-off transient with an initial set of the voltage balancing capacitance. With Equation (5-5) and (5-6) and the threshold voltage, the on/off status of each JFET is decided. Based on the on/off state of the JFET, the voltage change on each JFETs can be calculated one by one.

The second step is to calculate the J5 gate to source voltage increase and the J2 to J4 drain to source voltage increase during the turn-on process with equation (5-3) and (5-4).

If the calculated V_{ds_J5} is above the JFET rated voltage during the turn-on transient, or V_{D4} is above avalanche voltage, the capacitance set is discarded. If not, the capacitance set is recorded, and the cost function defined below is calculated.

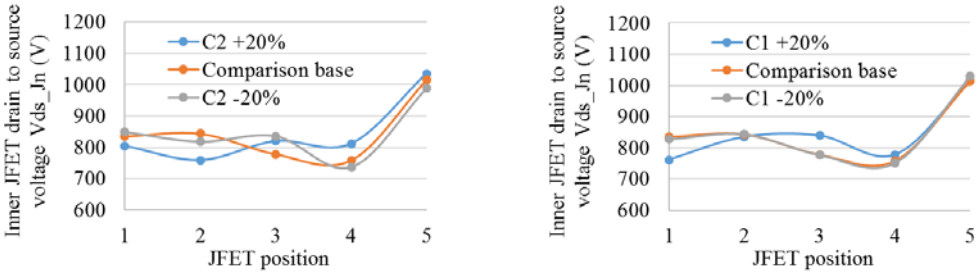
$$Cost(C_2, \dots, C_{n-1}) = \sum_{i=1}^{i=n} \left(V_{ds\_Ji} - V_{aval}\right)^2 \tag{14}$$

The cost function makes sure the difference between the voltage stress on the JFETs and the avalanche voltage of the clamping diodes is minimized, ensuring uniform voltage distribution in the SCPS.

With the optimization program and parameters of 1200 V 38 A rated JFETs, the calculated capacitance of C1 to C4 respectively are 263 pF, 146 pF, 108 pF and 89 pF.

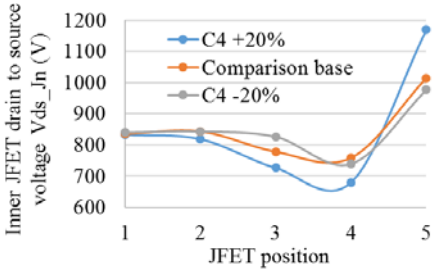
5.4.2. Sensitivity Analysis of the Capacitance Tolerance on the Voltage Distribution

When selecting the voltage balancing capacitors, the impact of the capacitance tolerance to the voltage distribution is considered. For off-the-shelf ceramic capacitors, ± 20% tolerance is common. Thus, the impact of ± 20% capacitance tolerance is first simulated, with the SCPS switching at 4,250 V with a current of 30 A. The voltage distribution with optimal voltage balancing capacitors then becomes the comparison base. With 20% capacitance tolerance, V_{ds_J1} to V_{ds_J5} in the off-state are recorded and shown in Figure 5.6. Here the capacitance variance of C1 and C2 is less critical to the voltage distribution, and do not cause overvoltage on J5. The C3 and C4 capacitance tolerance have higher impact. With 20% capacitance decrease of C3 or C4, overvoltage on J5 happens during the turn-on transient.

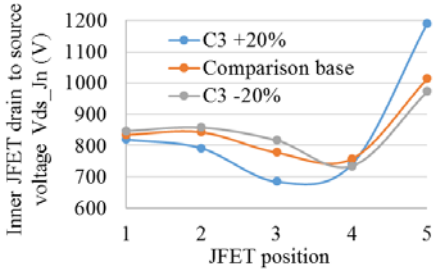


(a) ± 20 % change of C_1

(b) ± 20 % change of C_2



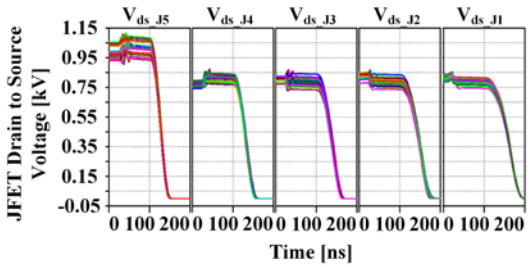
(c) ± 20 % change of C_3



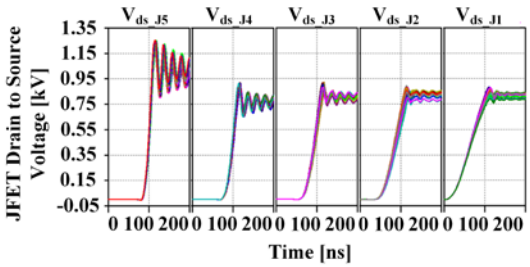
(d) ± 20 % change of C_4

Figure 5.6 Voltage distribution change due to 20 % capacitance change of the voltage balancing capacitors during off state.

After simulation iterations, to avoid J5 overvoltage, the tolerance of C1 to C4 are selected as 10%, 5%, 5% and 2%, respectively. The profile of the switching waveforms of both the SCPS and JFETs' drain to source voltages within selected tolerance are shown in Figure 5.7. The voltage distribution among JFETs during the off state is similar, and no overvoltage happens on J5 during the turn-on transient. The final selection of C1 to C4 for the prototype shown in the next section are 275 pF, 150 pF, 112 pF and 87.7 pF. The Class I ceramic capacitors, with low temperature coefficients, low voltage coefficients and low aging rates, are preferred in the SCPS design.



(a) Turn-off transient



(b) Turn-on transient

Figure 5.7 Switching waveforms under selected voltage balancing capacitor tolerance.

5.4.3. Considerations on the Avalanche Diodes

The diodes D1 to D4 avalanches when its parallel connected JFET drain to source voltage exceeds the diode avalanche voltage. The diode avalanche voltage limits the total power switch blocking voltage. The matching between the JFET blocking voltage and the diode avalanche voltage is preferred to maximize the performance of the whole power switch. The JFET blocking voltage is 1,200 V. To protect the JFET from overvoltage, the diode avalanche voltage is selected to be between 850 V and 1,200 V.

The junction capacitance of the diodes will change the effective capacitance of the voltage balancing capacitors C1 to C4, and eventually affect the dynamic voltage distribution. A smaller junction capacitance is preferred. It is recommended that the diode junction capacitance is 10 times smaller than the minimum capacitance of the voltage balancing capacitors.

The third precaution is the target blocking voltage. In the optimization cost function, the average voltage can be selected a little lower than the diode avalanche voltage. When the JFETs reach the average voltage, there are still some voltage margin before the diodes avalanche.

Based on these considerations, the avalanche diodes could help the super-cascode power switch to have a good static and dynamic performance with less thermal concerns.

5.5. Experimental Results

Two 4,500 V rated 5-stage super-cascode power switch prototypes are built to verify the proposed voltage balancing circuit design. Both prototypes utilize 1200 V / 38 A commercial JFETs in TO-247 package [70]. Prototype I is constructed without voltage balancing capacitors, and Prototype II contains the optimized balancing circuit. The 4,500 V prototype and the inductive load switching test setup are shown in Figure 5.8. The high voltage isolation design and safety clearance consideration in the test platform follow the design guidance specified in [71].

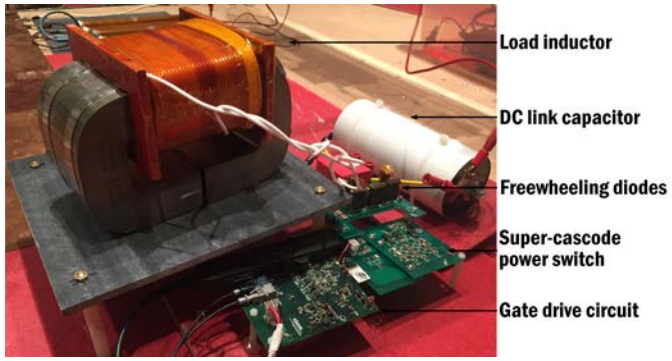


Figure 5.8 The 4,500 V super-cascode power switch double pulse test setup.

The turn-off waveforms of Prototype I are shown in Figure 5.9. Figure 5.9 (a) shows the SCPS drain to source voltage and load current. When the SCPS blocking voltage increases to about 1,200 V, there are glitches on both voltage and current waveforms. This is due to the clamping diode avalanching and J2 starting to turn off. As shown in Figure 5.9 (b), J2 starts to turn off when V_{ds_J1} is above 1,200 V. J3 starts to turn off when V_{ds_J2} is above 1,100 V. The avalanche diode takes several hundreds of nanoseconds to clamp

JFET drain to source voltage close to its avalanche voltage. Without the voltage balancing capacitors, the devices inside the SCPS suffer from high voltage stress and high thermal stress during the turn off transient.

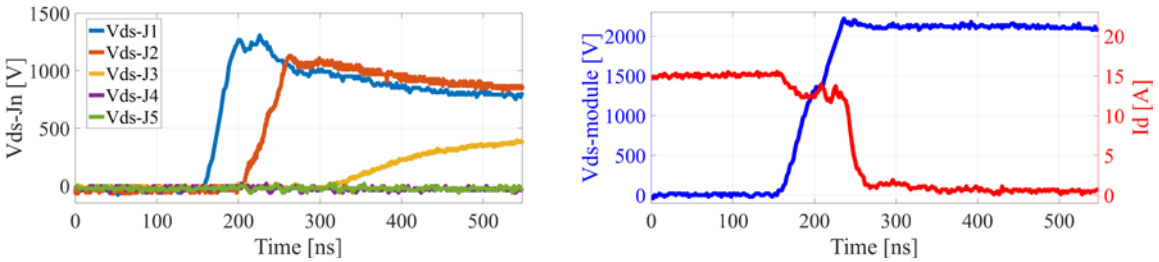


Figure 5.9 Experiment turn-off waveforms of the prototype without voltage balancing capacitors at 2,100 V dc voltage and 15 A load. (a) SCPS drain to source voltage and drain current. (b) drain to source voltage of inner JFETs.

The turn-off waveforms of Prototype II are shown in Figure 5.10. In Figure 5.10 (a), the turn-off time is reduced to 71 ns from 105 ns in Figure 5.9 (a). The glitches on the SCPS drain to source voltage disappear. The drain current decreases smoothly, and J2 starts to turn off when V_{ds_J1} is around 300 V during the turn-off transient. With optimized capacitors, the charging current of the voltage balancing capacitors decreases JFET gate to source voltage and let the upper JFETs turn off earlier. In Figure 5.10 (b), V_{ds_J1} to V_{ds_J5} increase simultaneously with no overvoltage on any JFET. J3 withstands higher voltage than that without capacitors.

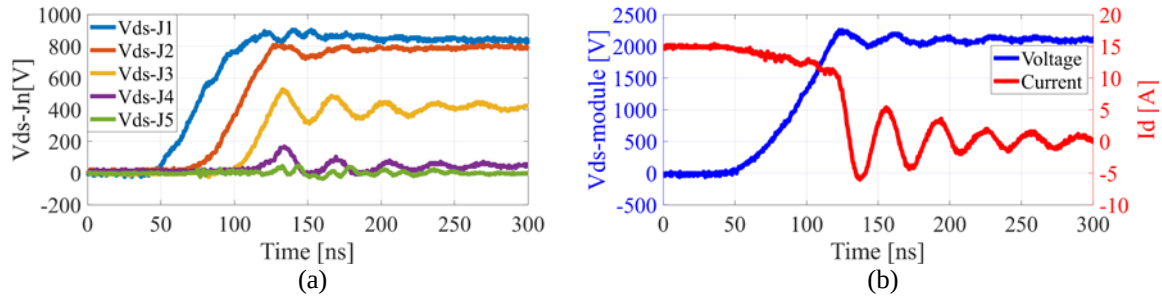


Figure 5.10 Experiment turn-off waveforms of the prototype with optimized voltage balancing capacitors at 2,100 V dc voltage and 15 A load. (a) SCPS drain to source voltage and drain current. (b) drain to source voltage of inner JFETs.

The turn-on waveforms of Prototype I are shown in Figure 5.11. Figure 5.11 (a) shows the SCPS drain to source voltage and the device drain current. The SCPS drain current fluctuates during the turn-on process. Figure 5.11 (b) shows the drain to source voltages of J1 to J5. As the drain current increases, V_{ds_J1} to V_{ds_J5} first increase one by one, maintaining a constant SCPS drain to source voltage. During this process, V_{ds_J5} increases as V_{ds_J3} decreases, and stays above 1200 V until V_{ds_J4} drops near 0 V. This asynchronized switching leads to long turn-on time, high switching loss, and overvoltage on J5, limiting the operation of Prototype I to 2,100 V.

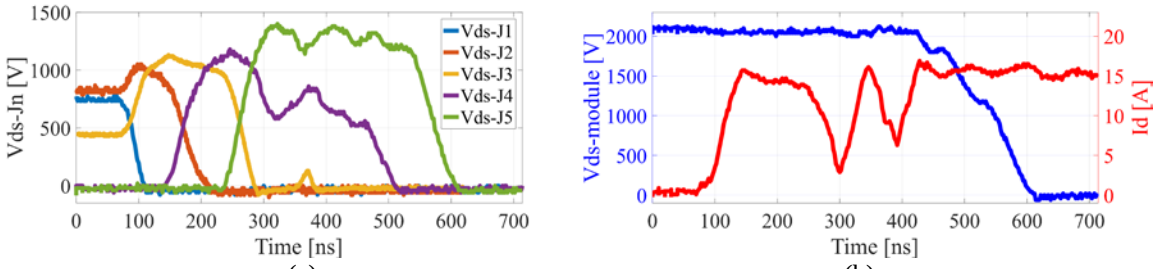


Figure 5.11 Experiment turn-on waveforms of the prototype without voltage balancing capacitors at 2,100 V dc voltage and 15 A load. (a) SCPS drain to source voltage and drain current. (b) drain to source voltage of inner JFETs.

The turn-on waveforms of Prototype II are shown in Figure 5.12, with Figure 5.12 (a) displaying the turn-on time reduction to 60 ns from 518 ns in Figure 5.11 (a). The drain current increases quickly and smoothly during the turn-on transient. In Figure 5.12 (b), V_{ds_J1} to V_{ds_J5} do not block total dc voltage in turn, but decrease together. As explained in Section 5.3, when the J5 source voltage drops, the C4 charging current increases V_{gs_J5} and

let J5 turn on earlier. V_{ds_J5} keeps below 1200 V during the turn-on process. With the optimized voltage balancing capacitors, the overvoltage issue on J5 is eliminated.

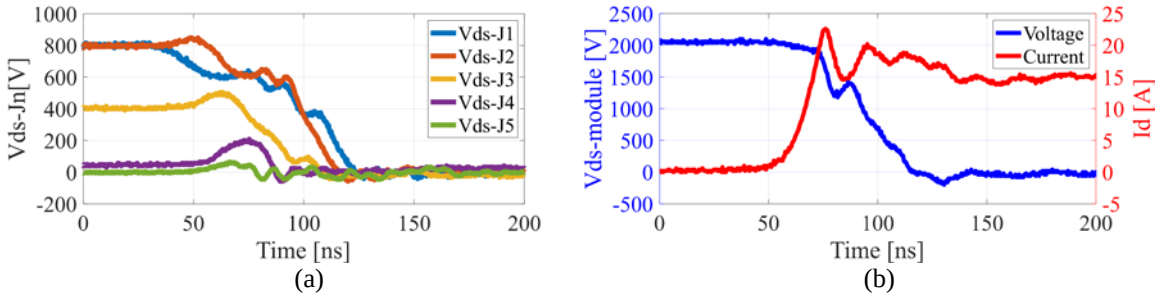


Figure 5.12 Experiment turn-on waveforms of the prototype with optimized voltage balancing capacitors at 2,100 V dc voltage and 15 A load. (a) SCPS drain to source voltage and drain current. (b) drain to source voltage of inner JFETs.

Switching time and switching loss at 2,100 V, 15 A condition are compared between the two cases, which are concluded in Table 5.1. With optimized voltage balancing capacitors, the turn-on time is reduced by 88%, and the turn-off time reduced by 32%. The turn-on loss is reduced from 11.3 mJ to 1 mJ, and the turn-off loss is reduced from 1.9 mJ to 0.92 mJ.

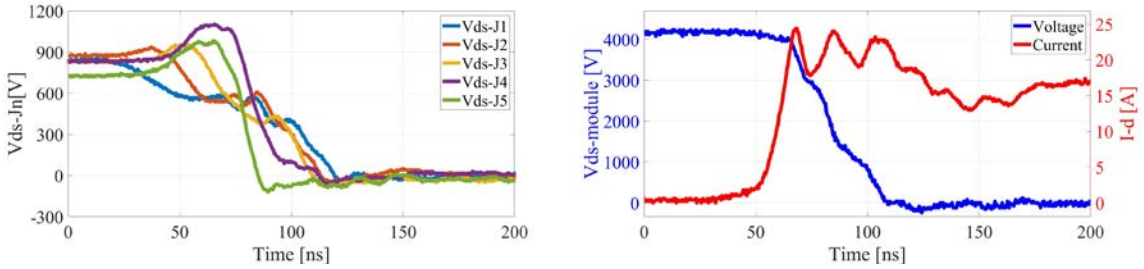
Table 5.1 Switching Time and Loss Comparison

	Turn-on Time	**Turn-on loss**	**Turn-off time**	**Turn-off loss**	**Total loss**
Without capacitors	518 ns	11.3 mJ	105 ns	1.9 mJ	13.2 mJ
Optimized capacitors	60 ns	1 mJ	71 ns	0.92 mJ	1.92 mJ

In most of the applications, 40 % voltage headroom is reserved for the semiconductor device. Due to the voltage overshoot, which may occur across the device drain and source

terminals under heavy load conditions, voltage headroom is especially needed for SiC and GaN devices. In this cascode structure, the loop inductance is even higher due to the larger switch size. For this 4,500 V rated device, 3,000 V is the recommended maximum operation voltage. To verify the voltage stress across all JFET drain to source terminals, a DPT test under 4,200 V condition is performed, leaving 10% headroom for the device rating. The test results are shown below.

As shown in Figure 5.13 and Figure 5.14, under 4,200 V / 15 A switching, the turn-on time is 64 ns, and turn-off time 84 ns. The drain to source voltage of all JFETs are below 1200 V during switching transients. With proper selection of the voltage balancing capacitor selection, the overvoltage issue of the internal JFETs during switching transients is eliminated.



(a) (b)

Figure 5.13 Experiment turn-on waveforms of the prototype with optimized voltage balancing capacitors at 4,200 V dc voltage and 15 A load. (a) super-cascode power switch drain to source voltage and current. (b) drain to source voltage of inner JFETs.

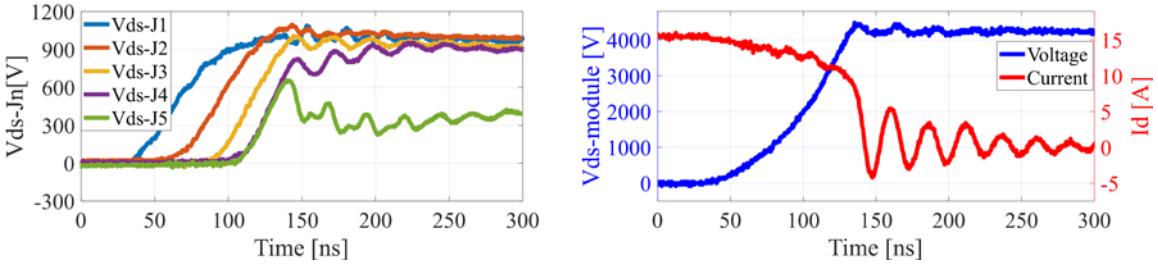


Figure 5.14 Experiment turn-off waveforms of the prototype with optimized voltage balancing capacitors at 4,200 V dc voltage and 15 A load. (a) super-cascode power switch drain to source voltage and current. (b) drain to source voltage of inner JFETs.

5.6. Summary

In this chapter, the feasibility to reduce the medium voltage SiC power switch is investigated. The super-cascode structure are reviewed as an alternative solution for medium voltage device with low voltage rating devices. The function of the voltage balancing circuit of high voltage SCPS is thoroughly reviewed. A circuit modeling method is proposed to study the optimization of the voltage distribution among series-connected JFETs, and to avoid overvoltage on the top JFET. Based on the optimization results, a SiC JFET based 4,500 V super-cascode power switch is built. Experimental results verify the analysis. The overvoltage on the top JFET is also eliminated. The turn-on loss is reduced to 8.85%, and the turn-off loss drops to 48.4%. With simple gate drive circuit design, the SCPS prototype achieves high speed switching under 4,200 V dc bus voltage.

Chapter 6. Conclusions and Future Work

6.1. Conclusions

This dissertation studies medium voltage SiC device reliability, packaging, and circuit realization, aiming to achieve high power density and high reliability power module design.

This work first reviewed the short circuit capability and the degradation under short circuit events of the medium voltage SiC MOSFETs. Based on the device short circuit characteristics, a three-step short circuit protection method with ultra-fast detection and protection circuit is analyzed and verified. The voltage dip on the phase-leg voltage is a clear and quick fault indicator during short circuit events. The detection circuit and the gate voltage clamping circuit together are used to limit the 3300 V SiC MOSFET short circuit energy and protect the devices through short circuit events. Experimental results verify that the short circuit condition can be detected within 100 ns. As soon as the short circuit fault is detected, the device gate voltage is successfully clamped to 14 V. After 2.2 μs the desaturation circuit confirms the fault condition and then soft turns off the device. The detection and protection circuit have good noise immunity, and are not mis-triggered under heavy load operations. The proposed protection method successfully extends the short circuit capability of 3,300 V SiC MOSFET without sacrificing the efficiency of the circuit during normal operation. The test results show that it is an effective and reliable way to protect the medium voltage SiC MOSFETs.

The exploration on the medium voltage SiC MOSFET packaging follows. To further increase the power density, the medium voltage SiC device packaging becomes a multi-disciplinary subject involving electrical, thermal, and mechanical design. Multi-functional

package components are desired to deal with more than one concerns in the application. The relationship between electrical, thermal, and mechanical properties needs to be understood and carefully designed to achieve a fully integrated high-performance power module. To maximize the advantages of the SiC MOSFET, high voltage blocking capability and high switching speed, the DBC design and overall power module structure are reconsidered. Vertical power loop and the possibility and advantages of ceramic material utilization as the baseplate material in the medium voltage SiC device package are discussed. The adoption of ceramic baseplate is assessed in the aspects of the insulation design, the thermal design, the power loop layout, the electromagnetic interference considerations, respectively. Mathematical models, simulations, and experimental results are presented to verify the analysis.

As the integrated baseplate, AlN and BeO can provide equivalent or better thermal performance than the widely used aluminum alloy. At the same time, ceramic baseplate can provide electrical insulation, making the DBC layout to be flexible. The impact of DBC thickness and baseplate fin type are discussed with simulation results. For this specific case, 1 mm AlN DBC gives the best cooling performance. To achieve low weight high power density power module design, direct liquid cooling is also integrated. The liquid cooling housing material selection is also discussed.

Two case studies for the 1,200 V DBC layout and 3,300 V DBC layout are conducted. In the 1,200 V prototype, the vertical loop structure realizes 1.1 nH power loop inductance. Experimental results show 4.3% voltage overshoot during the 700 V 25 A turn-off transient. Simulation results show that the utilization of the ceramic baseplate reduces the

maximum electric field strength, simplifies the power module internal isolation design, and mitigates the CM leakage current. This proposed power module structure is a simple and beneficial package method for medium voltage SiC MOSFETs.

The effort to reduce the cost of the medium voltage and even high voltage SiC device are made by investigating the circuit design with series-connected low voltage rating devices. The super-cascode structure features simple gate drive design by eliminating the isolation design in the gate drive circuit of the series connected devices. The super-cascode structure can benefit the medium voltage device area in two perspectives. First, medium voltage devices can be fabricated with low voltage rating devices, which will reduce the device cost and get more semiconductor manufactures involved in the medium voltage market. Secondly, higher voltage SiC devices can be built with lower cost, and the potential application areas of the medium voltage devices are widened. In this work, the function of the voltage balancing circuit of high voltage SCPS is thoroughly reviewed. A circuit modeling method is proposed to study the optimization of the voltage distribution among series-connected JFETs, and to avoid overvoltage on the top JFET. Based on the optimization results, a SiC JFET based 4,500 V super-cascode power switch is built. Experimental results verify the analysis. The overvoltage on the top JFET is also eliminated. The turn-on loss is reduced to 8.85%, and the turn-off loss drops to 48.4%.

6.1. Recommendations for Future Work

The SiC devices are attractive to the growing medium voltage market with its high blocking voltage, the high operation temperature, and high switching speed. There are still challenges in the development and wide adoption of medium voltage SiC devices. In the

harsh operation environment, effective protection strategy for the medium voltage SiC devices is necessary. The package for high voltage high temperature and high speed operation needs to be further investigated to highlight the superior performance of the SiC devices. Also, the cost for the medium voltage device needs to be more competitive in the medium voltage market. Reliable high efficiency high power density economic power electronic converter designs will help accelerate the transition of the current power system to a smart and green configuration.

The three major barriers have been attacked and solutions have been proposed and experimentally verified. About the medium voltage protection, a reliable ultra-fast protection strategy is proposed and verified. In the field applications, the status monitoring and life-span indication of the medium voltage devices will be helpful in the equipment status reporting and maintenance. To power up the control structure of the medium voltage devices, laser or optical power supply could be further investigated thanks to its good insulation capability, portability, and easiness to work with the electrical circuits.

About the medium voltage package, the vertical loop design and power module structure with ceramic baseplates are proposed and discussed. Light weight high power density design will be a challenging topic for a long period. Researchers need to continue the exploration of new materials and new structures, which could provide multiple conventional functions.

With the research progress on semiconductor device, packaging technology, system integration technology, dc link capacitor technology, and reliability test standards. Mediu voltage SiC devices will be finally accepted and widely adopted. Their inherently high

efficiency and low volume/weight feature will let them replace the Si MOSFET and Si IGBT based solutions in near future.

References

[1] Anant Agarwal, Jeremy Haley, Howard Bartlow, Bill McCalpin, Sumi Krishnaswami, Craig Capell, Sei-Hyung Ryu and John W. Palmour, "First Demonstra5on of 2100 W Output Power at 425 MHz Using 4H‐SiC RF Power BJTs," in the *Proceedings of the International Conference. on Silicon Carbide and Related Materials*, September 18‐23, 2005, Pitsburgh, Pennsylvania.

[2] Jun Wang, Yu Du, S. Bhattacharya and A. Q. Huang, "Characterization, modeling of 10-kV SiC JBS diodes and their application prospect in X-ray generators," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, San Jose, CA, 2009, pp. 1488-1493.

[3] Wolfspeed, High-Voltage SiC Power Modules for 10-25 kV Applications https://www.wolfspeed.com/downloads/dl/file/id/854/product/0/high_voltage_sic_power_modules_for_10_25_kv_applications.pdf

[4] J. W. Palmour et al., "Silicon carbide power MOSFETs: Breakthrough performance from 900 V up to 15 kV," in *IEEE 26th International Symposium on Power Semiconductor Devices & IC's (ISPSD)*, Waikoloa, HI, 2014, pp. 79-82.

[5] V. Pala et al., "10 kV and 15 kV silicon carbide power MOSFETs for next-generation energy conversion and transmission systems," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, Pittsburgh, PA, 2014, pp. 449-454.

[6] K. Vechalapu, S. Bhattacharya, E. Van Brunt, S. Ryu, D. Grider and J. W. Palmour, "Comparative Evaluation of 15-kV SiC MOSFET and 15-kV SiC IGBT for Medium-

Voltage Converter Under the Same dv/dt Conditions," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*、, vol. 5, no. 1, pp. 469-489, March 2017.

[7] M. Hinojosa, H. O'Brien, E. Van Brunt, A. Ogunniyi and C. Scozzie, "Solid-state Marx generator with 24 KV 4H-SIC IGBTs," in *IEEE Pulsed Power Conference (PPC)*, Austin, TX, 2015, pp. 1-5.

[8] L. Zhang, R. Woodley, X. Song, S. Sen, X. Zhao and A. Q. Huang, "High current medium voltage solid state circuit breaker using paralleled 15kV SiC ETO," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, San Antonio, TX, 2018, pp. 1706-1709.

[9] M. A. Rezaei, G. Wang, A. Q. Huang, L. Cheng and C. Scozzie, "Static and dynamic characterization of a >13kV SiC p-ETO device," in *IEEE 26th International Symposium on Power Semiconductor Devices & IC's (ISPSD)*, Waikoloa, HI, 2014, pp. 354-357.

[10] S. Ryu et al., "Impact of carrier lifetime enhancement using high temperature oxidation on 15 kV 4H-SiC P-GTO thyristor," in *European Conference on Silicon Carbide & Related Materials (ECSCRM)*, Halkidiki, 2016, pp. 1-1.

[11] R. J. Kaplar, A. A. Allerman, A. M. Armstrong, M. H. Crawford, J. R. Dickerson, A. J. Fischer, A. G. Baca, and E. A. Douglas. "Ultra-Wide-Bandgap AlGaN Power Electronic Devices," in *ECS Journal of Solid State Science and Technology*, vol. 6, no. 2, pp. 3061-3066, 2017.

[12] A. O. Adan, H. Nakagawa, Y. Kakizaki and L. Burgyan, "Benchmarking power transistors and power modules for high-temperature operation (Tj~200°C)," in *IEEE*

Transportation Electrification Conference and Expo (ITEC), Chicago, IL, 2017, pp. 662-667.

[13] https://www.wolfspeed.com/downloads/dl/file/id/854/product/0/high_voltage_sic_power_modules_for_10_25_kv_applications.pdf

[14] http://www.shmj.or.jp/english/pdf/dis/exhibi1000E.pdf

[15] https://www.psma.com/sites/default/files/uploads/tech-forums-semiconductor/presentations/is96-towards-medium-voltage-33-%E2%80%9315kv-sic-devices.pdf

[16] https://www.fujielectric.com/company/tech/pdf/63-04/FER63-04-209-2017.pdf

[17] FS820R08A6P2, Infineon HybridPACK drive module, https://www.infineon.com/cms/en/product/power/igbt/igbt-modules/fs820r08a6p2/

[18] FS770R08A6P2B, Infineon HybridPACK drive module, https://www.infineon.com/cms/en/product/power/igbt/automotive-qualified-igbts/automotive-igbt-modules/fs770r08a6p2b/#

[19] B. McPherson, B. McGee, D. Simco, K. Olejniczak and B. Passmore, "Direct liquid cooling of high performance Silicon Carbide (SiC) power modules," in *IEEE International Workshop On Integrated Power Packaging (IWIPP)*, Delft, 2017, pp. 1-5.

[20] K. Hussein et al., “New compact, high performance 7 th Generation IGBT module with direct liquid cooling for EV/HEV inverters,” in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2015 IEEE, IEEE, 2015, pp. 1343-1346.

[21] Z. Liang, “Integrated double sided cooling packaging of planar SiC power modules,” in *IEEE Energy Conversion Congress and Exposition (ECCE)*, IEEE, 2015, pp. 4907-4912.

[22] L. M. Boteler, S. M. Miner and M. Hinojosa, "Co-Designed High Voltage Module," in *Proc. of 17th IEEE Intersociety Conference on Thermal and Thermomechanical* Phenomena in Electronic Systems (ITherm), San Diego, CA, 2018, pp. 824-830.

[23] C. M. DiMarino, B. Mouawad, C. M. Johnson, D. Boroyevich and R. Burgos, "10-kV SiC MOSFET Power Module With Reduced Common-Mode Noise and Electric Field," in *IEEE Transactions on Power Electronics*, vol. 35, no. 6, pp. 6050-6060, June 2020.

[24] C. Yuan, M. Illindala, K. Ramamoorthy, and O. Alkhouli "Nine-Phase Induction Machine with Electric Pole Change for Emerging Heavy-Duty and Off-Road Micro/Mild Hybrid Vehicle Applications" *in Proc. of IEEE Industry Applications Society Annual Meeting*, Cincinnati, OH, 1-5 Oct. 2017.

[25] F. Chen, R. Burgos and D. Boroyevich, "A transformerless single-phase utility interface converter to attenuate common-mode voltage for DC microgrid," *2017 IEEE 3rd International Future Energy Electronics Conference and ECCE Asia (IFEEC 2017 - ECCE Asia)*, Kaohsiung, 2017, pp. 157-162.

[26] Mao, Daijiafan. "Integration of Plug-in Electric Vehicles into Power Grid: Impact Analysis and Infrastructure Planning." Electronic Thesis or Dissertation. Ohio State University, 2019.

[27] X. Huang, L. Vursin, A. Bhalla, W. Simon and J. C. Dries, "Design and fabrication of 3.3kV SiC MOSFETs for industrial applications, "2017 29th International Symposium on Power Semiconductor Devicesies, and IC's (ISPSD), Sapporo, 2017, pp. 255-258.

[28] V. Mulpuri, S. Jadav, S. Sundaresan and R. Singh, "Characterization and Robustness Evaluation of 3.3 kV/40 mΩ SiC DMOSFETs," 2019 IEEE 7th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Raleigh, NC, USA, 2019, pp. 130-136.

[29] H. Chen et al., "Investigation on Short Circuit Test of 3300V SiC MOSFET," 2019 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC), Xi'an, China, 2019, pp. 1-3.

[30] K. Tani, J. Sakano and A. Shima, "Analysis of short-circuit break-down point in 3.3 kV SiC-MOSFETs," 2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD), Chicago, IL, 2018, pp. 383-386.

[31] G. Romano, L. Maresca, M. Riccio, V. d'Alessandro, G. Breglio, A. Irace, A. Fayyaz, and A. Castellazzi, "Short-circuit Failure Mechanism of SiC Power MOSFETs, " in proceedings of the 27th International Symposium on Power Semiconductor Devices (ISPSD), pp. 345-348, 2015.

[32] G. Romano, A. Fayyaz, M. Eiccio, L. Maresca, G. Breglio, A. Castellazzi, and A. Irace, "A Comprehensive Study of Short Circuit Ruggedness of Silicon Carbide Power MOSFETs, " in the *Journal of Emerging and Selected Topics in Power Electron*., vol. 4, no. 3, pp. 978-987, 2016.

[33] Z. Wang, X. Shi, L. M. Tolbert, F. Wang, Z. Liang, D. Costinet, and B. J. Blalock, "Temperature-Dependent Short-Circuit Capability of Silicon Carbide Power MOSFETs, " IEEE Trans. Power Electron. Vol. 31, no. 2, pp. 1555-1566, 2016.

[34] A. März, T. Bertelshofer, R. Horff, M. Helsper, and M. M. Bakran, "Explaining the short-circuit capability of SiC MOSFETs by using a simple thermal transmission-line model," in proceedings of the 18th European Conference on Power Electronics and Application (EPE'16 ECCE Europe), pp. 1-10, 2016.

[35] R. Tanaka, Y. Kagawa, N. Fujiwara, K. Sugawara, Y. Fukui, N. Miura, M. Imaizumi, and S. Yamakawa, "Impact of Grounding the Bottom Oxide Protection Layer on the Short-Circuit Ruggedness of 4H-SiC Trench MOSFETs," in proceedings of the 26th International Symposium on Power Semiconductor Devices (ISPSD), pp.75-78, 2014.

[36] K. Han, A. Kanale, B. J. Baliga, B. Ballard, A. Morgan and D. C. Hopkins, "New Short Circuit Failure Mechanism for 1.2kV 4H-SiC MOSFETs and JBSFETs," in proceedings of 2018 IEEE 6th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Atlanta, GA, 2018, pp. 108-113.

[37] E. Eni, S. Bęczkowski, S. Munk-Nielsen, T. Kerekes, R. Teodorescu, R. Juluri, B. Julsgaard, E. VanBrunt, B. Hull, S. Sabri, D. Grider, and C. Uhrenfeldt, "Short-Circuit Degradation of 10-kV 10-A SiC MOSFET," in proceedings of *IEEE Transactions on Power Electronics*, vol. 32, no. 12, pp. 9342-9354, Dec. 2017.

[38] H. Li, X. Lyu, K. Wang, Y. Abdullah, B. Hu, Z. Yang, J. Wang, L. Liu, and S. Bala, "An Ultra-Fast Short Circuit Protection Solution for E-mode GaN HEMTs," *in*

proceedings of the 1st Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia), Xi'an, China, 2018, pp. 187-192.

[39] B. McPherson, M. Schupbach, S. Seal, A. Dutta, B. Passmore, A. Lostetter, T. McNutt, J. Casady, "A Modular and Scalable High Performance Power Module for Silicon Carbide Devices," in procedings of the *Applied Power Electronics Conference and Exposition (APEC)*, Anaheim, CA, Mar. 2019.

[40] T. McNutt, K. Olejniczak, D. Martin and G. Moxey, "DC Bus Switching Performance as Determined by Commutation Loop Parasitics and Switching Dynamics," in procedings of *2018 Power Electronics Europe*, Issue 3.

[41] C. DiMarino, W. Zhang, N. Haryani, Q. Wang, R. Burgos and D. Boroyevich, "A high-density, high-efficiency 1.2 kV SiC MOSFET module and gate drive circuit," in IEEE 4th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Fayetteville, AR, 2016, pp. 47-52.

[42] S. Guo, L. Zhang, Y. Lei, X. Li, W. Yu and A. Q. Huang, "Design and application of a 1200V ultra-fast integrated Silicon Carbide MOSFET module," in IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, 2016, pp. 2063-2070.

[43] M. Wang, F. Luo and L. Xu, "A Double-End Sourced Wire-Bonded Multichip SiC MOSFET Power Module With Improved Dynamic Current Sharing," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 5, no. 4, pp. 1828-1836, Dec. 2017.

[44] C. DiMarino, B. Mouawad, C. Johnson, M. Wang, Y. Tan, G. Lu, D. Boroyevich, and R. Burgos, "Design and Experimental Validation of a Wire-bond-less 10 kV SiC MOSFET Power Module," in IEEE Journal of Emerging and Selected Topics in Power Electronics, in press.

[45] T. Huber, A. Kleimaier and R. Kennel, "Ultra-low inductive power module design with integrated common mode noise shielding," in proceedings of *the19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)*, Warsaw, 2017, pp. P.1-P.9.

[46] H. You, Z. Wei, M. Aldawsari, B. Hu, R. Na and J. Wang, “Partial Discharge Behaviors in Power Module under Very High Dv/dt Repetitive Square Voltages,” in proceddings of *2019 IEEE Electrical Insulation Conference (EIC)*, Calgary, AB, Canada, 2019, pp. 489-492.

[47] H. You, Z. Wei, B. Hu, Z. Zhao, R. Na and J. Wang, "Partial Discharge Behaviors in Power Modules Under Square Pulses With Ultrafast dv/dt," in IEEE Transactions on Power Electronics, vol. 36, no. 3, pp. 2611-2620, March 2021.

[48] Direct bond copper introduction by Rogers Corporation, https://rogerscorp.com/power-electronics-solutions/technical-expertise/direct-bond-copper

[49] T. Huber, A. Kleimaier, S. Polster and O. Mathieu, "Low Inductive SiC Power Module Design Using Ceramic Multilayer Substrates," PCIM Europe 2018; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, Germany, 2018, pp. 1-8.

[50] W. Sheng, R. Colino, Power Electronic Modules Design and Manufacturing, Boca Raton, Florida: CRC Press LLC, 2005

[51] M. Olszewski, "Evaluation of the 2010 Toyota Prius hybrid synergy drive system," March 2011.

[52] Wolfspeed 1200 V 325 A SiC power module, CAS325M12HM2.

[53] M. A. Occhionero and R. W. Adams, "AlSiC, and AlSiC Hybrid Composites for Flip Chips, Optoelectronics, Power, and High Brightness LED Thermal Management Solutions," 2005 6th International Conference on Electronic Packaging Technology, Shenzhen, 2005, pp. 1-5.

[54] Aluminum alloy 6061 datasheet from United Performance Metals https://www.upmet.com/sites/default/files/datasheets/6061.pdf

[55] D. Pawlik, " Ceramic Substrates and Laminated Busbars Solutioins for Power Electronics, " in IEEE Applied Power Electronics Conference and Exposition (APEC), Anaheim, CA, 2019

[56] A. Kosar and Y. Peles, "TCPT-2006-096.R2: Micro Scale pin fin Heat Sinks - Parametric Performance Evaluation Study," in IEEE Transactions on Components and Packaging Technologies, vol. 30, no. 4, pp. 855-865, Dec. 2007.

[57] Z. Chen, Y. Yao, D. Boroyevich, K. D. T. Ngo, P. Mattavelli and K. Rajashekara, "A 1200-V, 60-A SiC MOSFET Multichip Phase-Leg Module for High-Temperature, High-Frequency Applications," in IEEE Transactions on Power Electronics, vol. 29, no. 5, pp. 2307-2320, May 2014.

[58] J. Biela, D. Aggeler, D. Bortis and J. W. Kolar, "5kV/200ns Pulsed Power Switch based on a SiC-JFET Super Cascode," in Proc. IEEE International Power Modulators and High-Voltage Conference, Las Vegas, NE, 2008, pp. 358-361.

[59] J. Biela, D. Aggeler, D. Bortis and J. W. Kolar, "Balancing Circuit for a 5-kV/50-ns Pulsed-Power Switch Based on SiC-JFET Super Cascode," in IEEE Transactions on Plasma Science, vol. 40, no. 10, pp. 2554-2560, Oct. 2012.

[60] X. Ni, R. Gao, X. Song, A. Q. Huang and W. Yu, "Development of 6kV SiC hybrid power switch based on 1200V SiC JFET and MOSFET," in Proc. IEEE Energy Conversion Congress and Exposition (ECCE), Montreal, QC, 2015, pp. 4113-4118.

[61] X. Song, A. Q. Huang, L. Zhang, P. Liu and X. Ni, "15kV/40A FREEDM super-cascode: A cost effective SiC high voltage and high frequency power switch," in the IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, 2016, pp. 1-8.

[62] B. Gao, A. J. Morgan, Y. Xu, X. Zhao and D. C. Hopkins, "6.0kV, 100A, 175kHz super cascode power module for medium voltage, high power applications," in Proc. 2018 IEEE Applied Power Electronics Conference and Exposition (APEC), San Antonio, TX, 2018, pp. 1288-1293.

[63] X. Li, H. Zhang, P. Alexandrov and A. Bhalla, "Medium voltage power switch based on SiC JFETs," in the IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, 2016, pp. 2973-2980.

[64] U.S. patent No. 9190993.

[65] X. Lyu, H. Li, B. Hu, Z. Ma and J. Wang, "High voltage SiC super-cascode power switch parameter optimization for loss reduction," in Proc. 2018 IEEE Applied Power Electronics Conference and Exposition (APEC), San Antonio, TX, 2018, pp. 1701-1705.

[66] X. Huang, Q. Li, Z. Liu and F. C. Lee, "Analytical Loss Model of High Voltage GaN HEMT in Cascode Configuration," in IEEE Transactions on Power Electronics, vol. 29, no. 5, pp. 2208-2219, May 2014.

[67] H. Li, L. Liu, J. Wang, “Paralleled Operation of High Voltage Cascode GaN HEMTs” IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 4, no. 3, pp. 815-823, Sept. 2016.

[68] Datasheet UJN1205K, United Silicon Carbide Inc., https://www.mouser.com/datasheet/2/827/DS_UJN1205K-1085697.pdf

[69] L. Fu, X. Zhang, H. Li, X. Lu, and J. Wang, “The development of a high-voltage power device evaluation platform,” in Proc. 2nd IEEE workshop on wide bandgap power devices and applications (WiPDA), pp. 13-17, Knoxville, TN., Oct. 13-15, 2014.