Short Circuit Capability and Degradation Mechanism Analysis of E-mode GaN HEMT

THESIS

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Abstract

Gallium Nitride High Electron Mobility Transistor (GaN HEMT) has become one of the most attractive power transistors in recent years due to its superior electrical and thermal performance. While GaN devices have been used in more and more applications, short circuit capability of GaN HEMT and the method to qualify its reliability still worth discussion.

This report presents the short circuit behavior of discrete 650 V/ 30 A large current rating Enhancement-mode (E-mode) GaN HEMT devices under single and repetitive short circuit operations. Firstly, structure and characteristics of GaN HEMT are introduced. Both cross-section structure of the lateral power transistor and gate structure of normally-off GaN HEMT are presented. Next, detailed test platform design is presented. The platform is established based on hard switching fault (HSF) circuit, and the turn-off transient is evaluated, which proved that soft turn-off is required for GaN HEMT short circuit tests. Besides, a system level thermal model based on FEA simulation and Cauer thermal network is established to have an accurate prediction of devices junction temperature. Then, short circuit roughness has been explored through designed tests, from these tests, maximum short circuit time, short circuit critical energy, as well as short circuit failure behavior and the mechanism is explored and analyzed. For the repetitive short circuit degradation tests, a series of experimental tests are carried out to determine the number of short circuit operations the devices can support before obvious degradation

happens under different dissipated energies. More importantly, device static characteristics are explored and monitored during the degradation tests, and the characteristics shifting has been investigated and acts as the indicators of devices degradation. For different kinds of test, including failure condition, test waveforms are presented together with detailed analysis and mechanism discussion.

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Chapter 1. Introduction

1.1. Overview of E-mode GaN HEMT

For a quite long time, Silicon (Si) based devices have dominated in the power electronic application, however, as the development of power electronics, Si power devices show their limitation in many situations, especially in those areas that require high voltage or high frequency devices. Faced with these challenges, some other materials with better intrinsic properties are required, which leads to the emerging and rapid development of wide bandgap (WBG) devices, such as Gallium Nitride (GaN) and Silicon Carbide (SiC). To have a better understanding of the advantages of WBG devices over conventional Si power devices, five critical physical properties are shown in Figure 1.1 [1]. Featuring higher band gap energy, the WBG devices usually have lower leakage current and could operate at higher temperature. Besides, because of higher breakdown field of the WBG semiconductors, WBG devices could operate at a certain voltage with a thinner die, which helps to achieve a smaller on- resistance and smaller die size. Moreover, saturation velocity, the maximum obtainable velocity of carriers, is higher for WBG devices than Si devices. This advantage together with smaller input and output capacitance enables WBG devices to operate at a higher frequency [2].

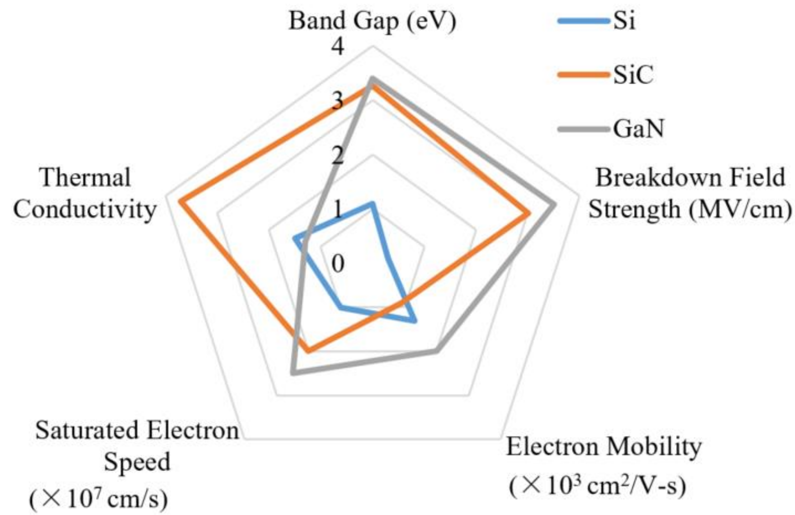


Figure 1.1 Comparison of Si, SiC and GaN based on physical property

Compared with GaN devices, SiC devices could be applied at higher voltage and a higher temperature application, however, GaN devices could achieve higher frequency and higher efficiency than its SiC counterparts. Most commonly used GaN power device is fabricated in a lateral structure, known as the high electron mobility transistors (HEMTs) or heterojunction field effect transistors (HFETs).

Although vertical GaN based devices may have better use of material advantages, there still exists several difficulties in building a GaN based vertical device. some progress has been reported by several companies and universities, like the GaN on GaN diodes and FET developed by Avogy [3][4], and the GaN on Si FET published by Cambridge Electronics, Inc. (CEI) [5]. However, as none of these devices have become commercially available, lateral structure HEMTs are still the most promising candidates

for GaN devices application by now. As the totally different structure with the conventional power devices, like MOSFET and IGBT, previous short circuit test experience and conclusions could not be applied to GaN HEMTs directly. The cross-section of GaN HEMT is shown in Figure 1.2.

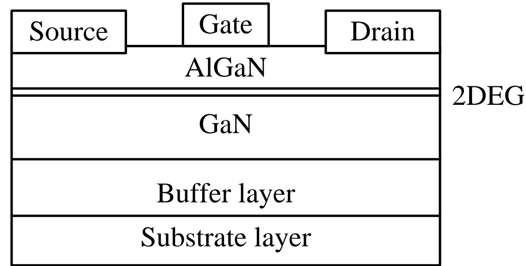


Figure 1.2 Cross-section of lateral GaN HEMT

As is shown in Figure 1.2, the most basic feature of lateral devices is the heterojunction between different materials. By growing a thin layer AlGaN on top of GaN, a channel for high mobility electrons would be created at the interface of two layers. This conduction channel is called two-dimensional electron gas (2DEG), which is formed as result of crystal polarity, and is intensified by lattice mismatch between two materials [2]. The 2DEG channel is controlled by the gate voltage, with a different gate signal, the thickness and density of electrons in this channel will be different, and the turn-on and turn-off could be controlled.

As the polarization field discontinuity natively exists between the AlGaN and GaN, 2DEG layer natively exists between drain and source terminal, meaning that GaN HEMTs are inherently depletion mode (normally on) devices. The threshold voltage of

D-mode devices is negative and a negative voltage needs to be applied between gate and source to turn off the device. Normally on is not desirable in the voltage source converter circuit, as it requires a more complex circuit and leads to higher power loss. Thus, some methods have been developed to realize normally off device. The first method is through cascode structure, in this case, a d-mode GaN HEMT is in series with a normally off Si MOSFET, and the gate-to-source voltage of GaN HEMT equals to the source-to-drain voltage of MOSFET. While the Si MOSFET could provide protection for GaN HEMT to avoid breakdown, the performance of cascode devices depend heavily on the parasitic inductance between two dies. The other method to realize normally off device is to change the gate structure, namely the enhancement-mode GaN HEMT. There are several published gate structures that are usually used, including recess gate [6], MIS-HEMT, pGaN, GIT and so on [2].

1.2. Research motivation and objectives

Reliability has always been a big concern during transistor fabrication and circuit design, and it is important to understand devices' characteristics and abilities before any application. Short circuit capability and lifetime of a device would have a big influence on its widespread acceptance and use, while GaN HEMTs are becoming an indispensable component in power electronics area, there are still many challenges regarding its reliability.

Published JEDEC standards are usually used on vertical devices, like Si and SiC MOSFET, however, commercialization of vertical GaN devices are limited by the development of GaN wafer and heteroepitaxial fabrication [2]. For the lateral GaN

HEMT, the completely different structure would lead to different short circuit and degradation mechanism, thus previous results cannot from to the GaN based converter design. So far, only one paper discusses the short circuit behavior of the commercial 600 V cascode depletion mode (D-mode) GaN power transistor [7]. Few papers discuss the pulse current capability of the 100 V E-mode GaN HEMT [8][9]. However, the short circuit roughness of 600-class larger current E-mode GaN HEMT has not been explored yet. Thus, it is important to investigate the short circuit behavior of E-mode GaN HEMTs, especially for high voltage, large current rating chips. The information gained will not only benefit device manufacturers, but will also enable protective function design in converters.

1.3. Thesis organization

This thesis focuses on the reliability and roughness analysis of a high voltage single chip e-mode GaN HEMT, device short circuit performance and characteristics are presented. Firstly, Chapter 2 presents an overview of e-mode GaN HEMT characteristics, besides short circuit test platform design, optimization of turn-off procedure and system thermal model are given in this section. Then, Chapter 3 presents the device short circuit performance under 25 ℃ and elevated temperature. Critical energy and short circuit withstand time are calculated and compared. In Chapter 4, device degradation characteristics are investigated, several static characteristics serve as the degradation indicators and are recorded and compared throughout the test. Degradation mechanism is analyzed based on the test results and publications. Chapter 5 concludes the thesis with a summary.

Chapter 2. Short circuit test platform design and thermal model development

To evaluate the roughness and short circuit capability of GaN HEMT, a two-layer test platform is designed based on hard switching fault (HSF) to generate short circuit pulses. Given the influence of test platform on the system temperature distribution, an accurate thermal model including junction to ambient thermal impedance is implemented to simulate the device junction temperature.

2.1. Introduction

Nowadays, there are two kinds of fault conditions usually used to test the short circuit capability of power devices, and the schematic is shown in Figure 2.1. The first one is called fault under load (FUL), it simulates the short circuit condition that happened while the device works under normal conduction. The second kind of circuit is called hard switch fault (HSF). Unlike the FUL, of which the overcurrent happens during the on-state condition, the overcurrent of second fault condition happened during turn-on transient [3].

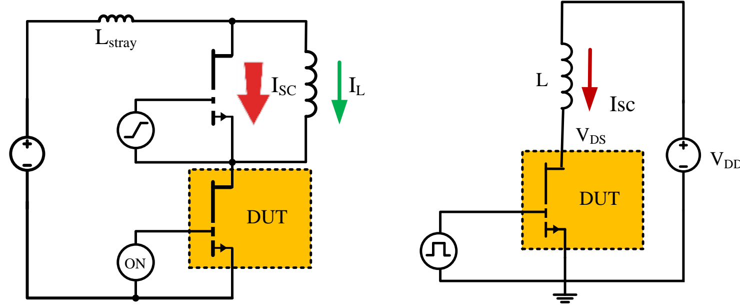


Figure 2.1 Schematic of the short-circuit test circuit (a) Hard-switching Fault (b) Fault under load

A lot of work has been done involving the power device short-circuit characteristics under two different fault conditions, generally short circuit current under FUL is larger than HSF condition. Most of previous contributions focus on the insulated gate bipolar transistors (IGBT) devices [3], [10], [11], [12], and Silicon Carbide (SiC) metal-oxide semiconductor field-effect transistor (MOSFET) [13], [14]. As is shown in [14], an overcurrent testing circuit is proposed, with which both kinds of fault conditions could be achieved by controlling the time sequence of turn-on signals sent to control switches. Some experiments also did on the GaN HEMT [7], [8], [9]. The test results published in the [8], [9] is based on a RLC Pulse Ring Down Board, and the test schematic is similar to HSF circuit with some protection method added.

2.2. Device under test and its thermal model

The device evaluated in this work is the enhancement-mode (e-mode) GaN HEMT GS66516T from GaN System [15], rating at 650V/ 60A, which is the highest rated GaN HEMT among devices that commercially available. A preliminary datasheet is provided

by GaN System, from which typical characteristics could get. Besides, some publications have worked on similar devices with a lower current rating for a full range of performance data and loss estimation [16].

GaN Systems has not published its gate structure, but some publications report that these devices have an insulated gate [17], like plasma treatment, insulated recess gate, or hybrid MIS-HFET[2], [15], [16], [18].

As junction temperature is an important parameter determining the reliability of device during the short circuit transient, making an accurate prediction of junction temperature under a certain dissipated energy is quite crucial during the result analysis.
A detailed thermal network is provided in the application note from GaN System [19]. The four-layer Cauer type thermal model is established based on the device physical property and package structure, to be specific, DUT is divided into four parts from the junction to package, as is shown in Figure 2.2.

#1 GaN
#2 Si
#3 Attachment
#4 Cu Base

Figure 2.2 GaN HEMT physical layer of Cauer type thermal model

The Cauer model for each level is represented by a thermal resistance R_θ and a thermal capacitance C_θ. Then the thermal model of the device could be represented as a series of RC network, for each junction of the network stands for the temperature of each layer. Detailed network structure and parameters are shown in Figure 2.3.

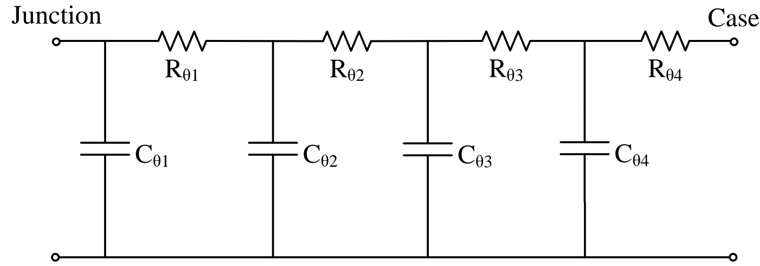


Figure 2.3 GaN HEMT Cauer thermal model

With an RC network, the time dependent temperature distribution of the device could be calculated. Layer thermal resistance was derived from the thermal simulation and calculated using the equation (1), and the layer thermal capacitance was calculated based on the active area of the device using equation (2).

$$R_{\theta 1} = \frac{\Delta T}{P} = \frac{T_J - T_1}{P} \quad (1)$$

$$C_{\theta 1} = C_{p1} \cdot \rho_{p1} \cdot L_1 \cdot A_{active} \quad (2)$$

Where ΔT is the temperature rise of each layer, and L means the layer thickness, while C_{p1} and A_{active} represents the pressure specific heat capacity and device active area correspondingly. The calculation results are shown in Table 2.1.

Table 2.1 GaN HEMT Cauer thermal network parameters

R_θ (°C/W)	$R_{\theta 1} = 0.007$	$R_{\theta 2} = 0.139$	$R_{\theta 3} = 0.140$	$R_{\theta 4} = 0.014$
C_θ (W·s/°C)	$C_{\theta 1} = 8.03\times10^{-5}$	$C_{\theta 2} = 5.59\times10^{-3}$	$C_{\theta 3} = 1.26\times10^{-3}$	$C_{\theta 4} = 1.90\times10^{-3}$

2.3. Investigation of minimum gate resistance

The slew rate of the GaN HEMT could be controlled by using different gate resistors R_g, which usually need to be optimized based on specific requirements, like switching loss, EMI and overshoot. In this work, the emphasis is put on the electrical stress induced by turn-off transient, which requires a careful design of turn-off resistor.

Generally, a larger gate resistance means slower switching and lower switching noise, while a smaller gate resistance would result in a faster switching and lower switching losses. In GaN System high voltage GaN HEMT application, the turn-on resistor usually selected from 10 Ω to 20 Ω [18]. In this work, a 10 Ω resistor is used for the turn-on gate loop. The turn-off resistor usually used in the GaN-based inverter design is 1-2 Ω, however, during the short circuit test, the turn-on transient is quite short and the stray inductance will induce high overshoot in the V_{ds} waveform if the turn-off resistance is too small. Figure 2.4 shows an example waveform when DC link bus voltage equals to 50V, while turn-off resistance is 10 Ω and the short circuit transient is 100 ns.

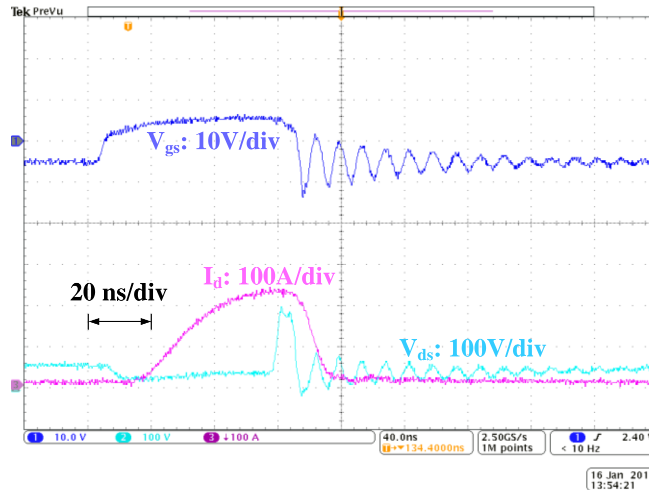


Figure 2.4 Example waveform with low turn-off resistance

In order to explore the device roughness under short circuit condition without inducing other stress in the tests, the drain to source overshoot voltage must remain lower than the breakdown voltage within the specified safe operation area (SOA). As indicated in the above Figure 2.4, the maximum V_{ds} overshoot is about 200 V when V_{ds} = 50 V, which could be quite dangerous if the V_{ds} keeps increase. To avoid undesirable damage result from drain to source voltage overshoot, a bigger turn off resistor is needed in the gate loop. Faced with this problem, several tests are carried out to verify the influence of the turn-off resistance. The resistance in these tests vary from 1 Ω to 20 Ω, and the relationship between resistance and V_{ds} overshoot is shown in Figure 2.5.

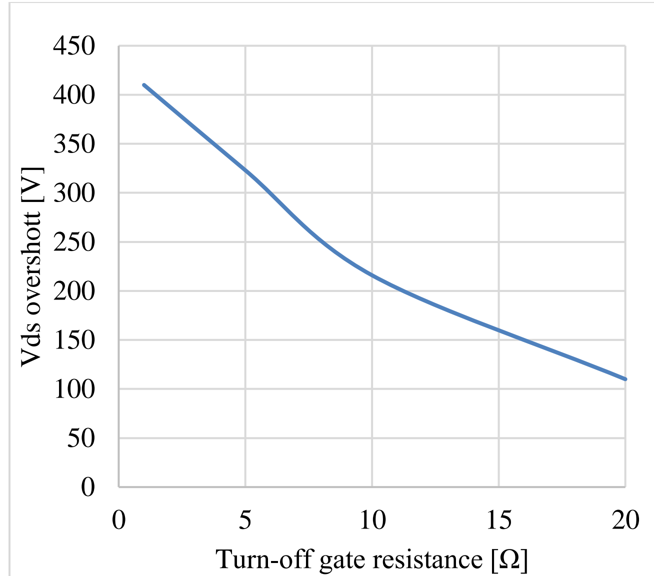


Figure 2.5 Influence of turn-off resistance on the drain to source voltage

In case of breakdown induced by V_{ds} overshoot, short circuit turn-off gate resistance should be no less than 15 Ω. In other words, soft turn off is required for E-mode GaN HEMT short circuit tests. In this work, turn-off resistor is selected as 20 Ω, and Figure 2.6 shows the gate loop structure.

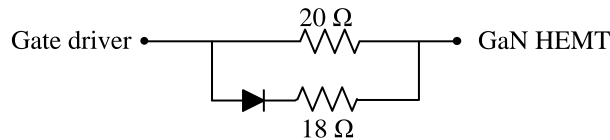


Figure 2.6 GaN HEMT gate loop design

2.4. Test platform and its thermal model

To evaluate the GaN HEMT's ruggedness under electrical stress, the HSF short circuit is used in this work to generate the transient overcurrent. The testing circuit is shown in Figure 2.7, the stray inductance L_{stray1}, L_{stray2}, L_{stray3}, device parasitic capacitance C_{gd}, C_{ds}, C_{gs}, gate loop design and test points are included.

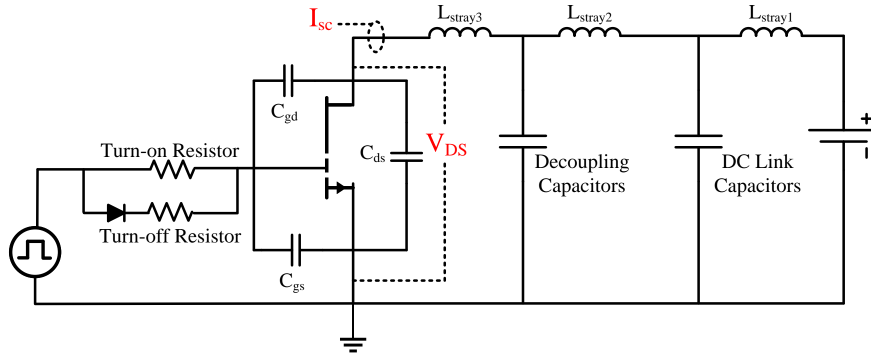


Figure 2.7 Detailed short circuit test schematic

To realize the designed fault condition and make the experiment more convenience, a two-layer PCB is designed to generate the transient overcurrent and act as the fixture during the static tests.

To be specific, the hardware test bed consists of a mother board and a daughter board. The mother board consists of high voltage power loop, capacitor bank, the gate driver and is designed to be able to test three devices at same time, which is quite convenient during the repetitive pulses tests. While GaN HEMTs could achieve higher switching speed in the applications, it requires more attention on the gate loop inductance design. As the gate

voltage limitation is about ±10 V, both the ringing and peak voltage may exceed the maximum rating under fast switching with the influence of loop inductance. For the gate driver design in this work, the turn-on voltage is +6 V to minimize the conduction power loss, and STMicroelectronics STGAP1S is selected as the gate driver in this work.

The daughter board is a specially designed fixture for the device, on the one hand, the surface mounted device could be soldered on the PCB during the short circuit test. to minimize the overshoot during the turn off and emulate the realistic short circuit condition of the GaN converter, 0.7 μF decoupling capacitors are placed on the daughter board close to the device to minimize the equivalent stray inductance. On the other hand, the daughter board could serve as the fixture during the static test. Four separate terminals are provided to drain and source, and through these terminals, the DUTs could be connected to curve tracer with Kelvin connection. Figure 2.8 shows the platform design into details.

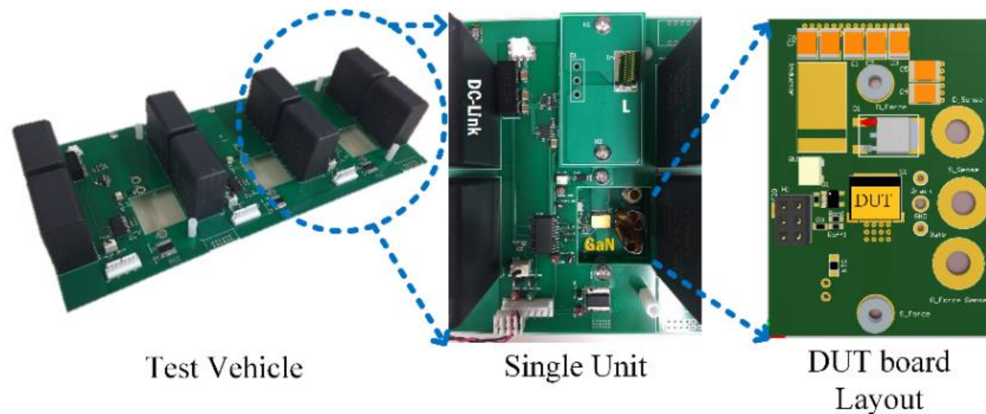


Figure 2.8 Hardware implementation of the test circuit

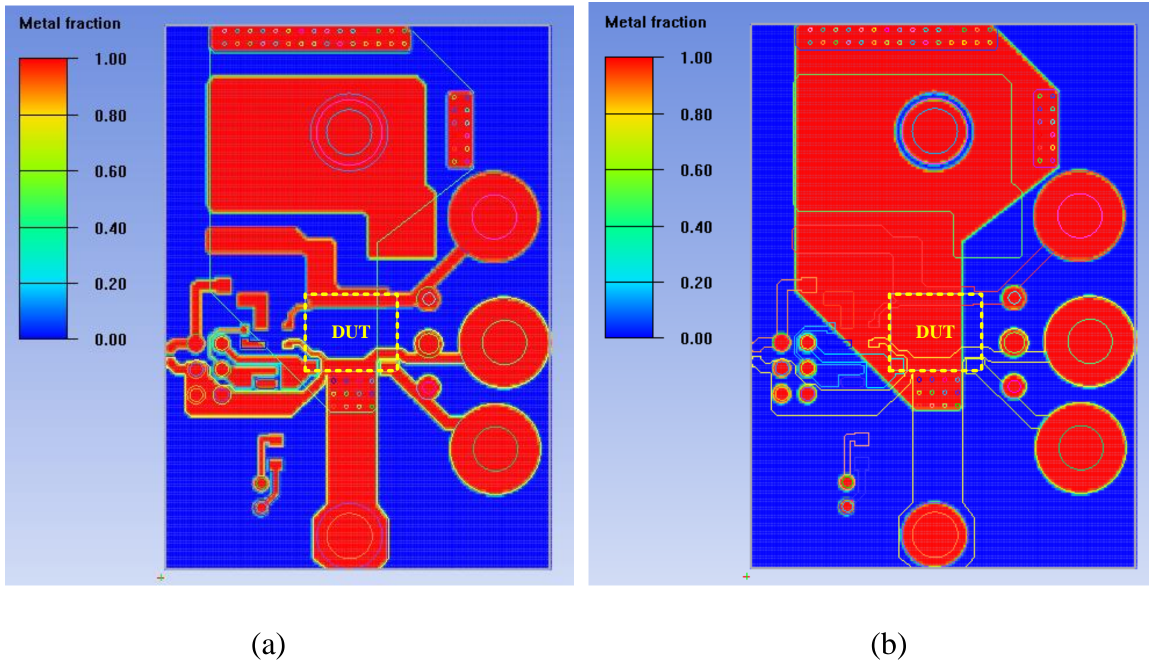
As the PCB would also have much influence on the system thermal distribution, the cauer network of the GaN HEMT introduced in the Chapter 2.2 is extended with PCB thermal model, which is established with the help of ANSYS Icepak.

ANSYS Icepak is a kind of thermal simulation software based on finite element analysis (FEA), providing accurate predict on airflow, temperature and heat transfer in various electronic components and PCBs. In this work, the system thermal model, which contains the daughter board and GaN HEMT, is established to extract the thermal impedance for further analysis.

Two parts are considered while establishing the system thermal model. The first one is the DUT, acting as a power dissipation source. It is modeled as a two-level network block, and it has a junction in the center and two thermal resistance, namely junction to case impedance R_{jc} and junction to bottom impedance R_{jb}. Then both dissipated power and thermal resistance of the GaN HEMTs could be set as parameters of the block. In order to have a better emulation of the system physical structure, solder pads are added on the bottom side of the GaN HEMT according to the device footprint. In this case, junction temperature and case temperature could be monitored throughout the simulation procedure, and the temperature behavior could be recorded as a time dependent curve.

The second part of the thermal model is the 2-layer daughter board. The PCB is designed in Altium designer, then the PCB file could be imported into Icepak together with information about traces, vias, and material of each PCB layer. Afterward, trace distribution for each layer could be clearly observed through metal fraction, as is shown

in the Figure 2.9, traces are represented as the red parts, while the blue parts is the FR4 layer.



(a) (b)

Figure 2.9 System Icepak thermal model. (a) Top layer. (b) Bottom Layer

With the detailed thermal model, the temperature distribution could be simulated and recorded as is shown in the Figure 2.10. As is indicated by Figure 2.9 and Figure 2.10, the temperature distribution is highly dependent on the metal distribution of the PCB, and the more heat would concentrate on the solder pad.

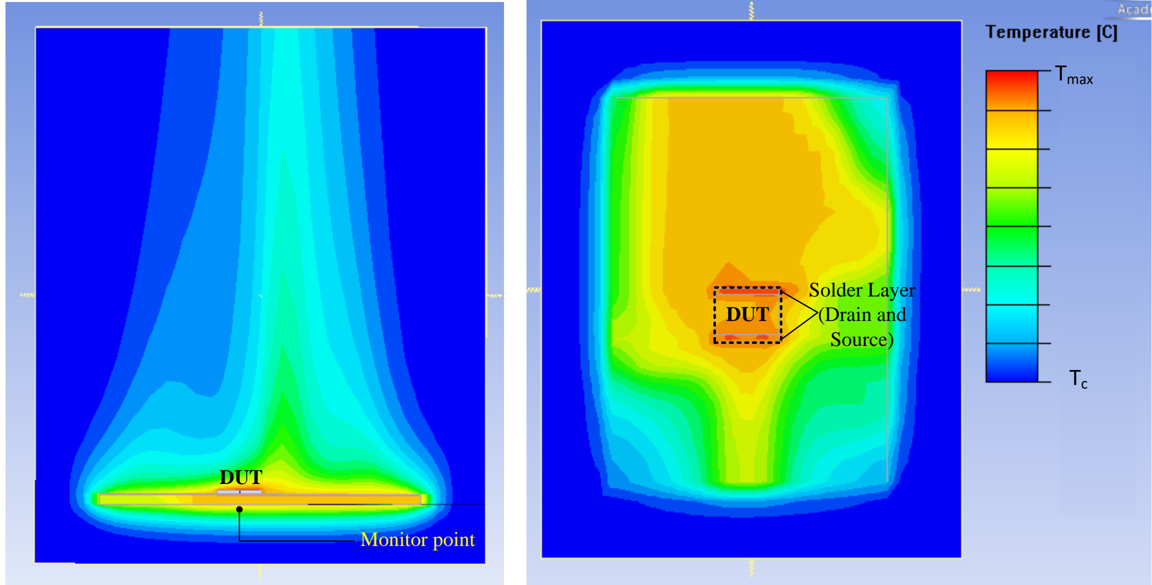


Figure 2.10 PCB temperature distribution. (a) Side view. (b) Top view

During the simulation, a monitor point is added on the bottom side of PCB, then the temperature of this point could be simulated as a time dependent curve. Afterward the Foster type thermal network and its RC parameters can be extracted by curve-fitting with the following equation (3) [20].

$$Z_{jc}(t) = \frac{T_j(t) - T_c(t)}{P_{in}} = \sum_{n=1}^{X} R_\theta \cdot \left(1 - e^{-t(R_\theta \cdot C_\theta)}\right) \tag{3}$$

Where R_θ and C_θ represent the thermal resistance and thermal capacitance of the thermal network, and are connected as is shown in the Figure 2.11. X in the equation (3) means the number of pairs of RC. In this work, a five-level thermal network is implemented to realize an accurate fitting.

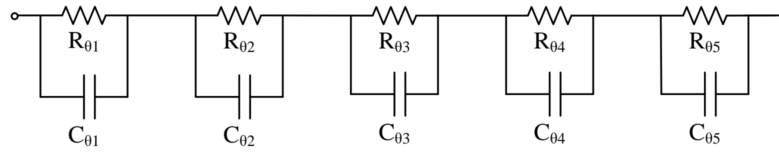


Figure 2.11 Five level Foster thermal network

As the thermal network of device is given as Cauer type, the foster network derived from curve fitting needs to be converted into Cauer network before connected together. The calculation results are shown in Table 2.2.

Table 2.2 PCB Cauer thermal network parameters

R_θ (°C/W)	$R_{\theta 1} = 9.743$	$R_{\theta 2} =19.116$	$R_{\theta 3} =30.991$	$R_{\theta 4} = 0.610$	$R_{\theta 5} = 4.389$
C_θ (W·s/°C)	$C_{\theta 1} = 0.131$	$C_{\theta 2} = 0.751$	$C_{\theta 3} = 2.814$	$C_{\theta 4} =176.3$	$C_{\theta 5} = 3\times10^6$

As Foster network is a simulation result of temperature dynamic of the power device, the Cauer network that derived from Foster model no longer have the physical meaning but just the temperature of two terminals could be guaranteed. Then the system thermal network is established as is shown in the Figure 2.12. The time dependent temperature distribution of the system could get with the help of LTspice, the software that could simulate the circuit transient response.

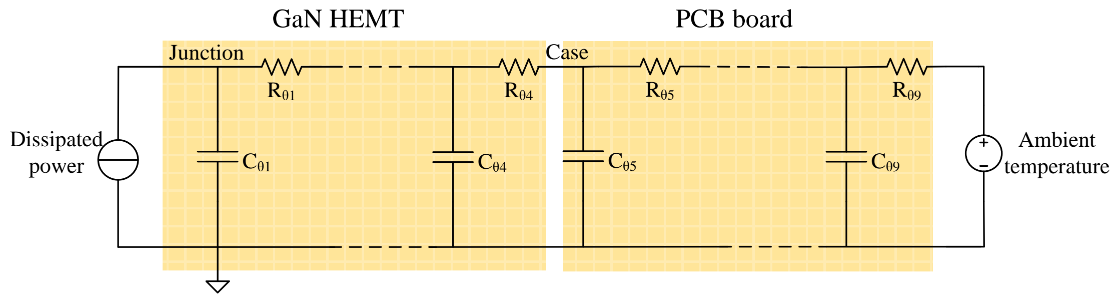


Figure 2.12 System Cauer thermal model

Chapter 3. GaN HEMT critical energy calculation and failure mechanism

In this section, DUTs are subjected to a single pulse, and the short circuit behavior of 650V GaN HEMT under 25℃ and elevated temperature is investigated. Besides, destructive short circuit tests are carried out to determine the critical energy and short circuit withstand time.

3.1. Review of 600 V/ 650 V class power transistors short circuit capability

Traditional power transistors, such as SiC MOSFET and Si IGBT, are usually tested according to Joint Electron Device Engineering Council (JEDEC) standards, which requires that the qualification tests are designed to simulate their operation conditions throughout lifetime.

In recent years, many papers have been published on the topic of the short circuit behavior of Si IGBT [11], [21] and SiC MOSFET [7], [13], [14] under different fault conditions. Delayed failure mode could be observed in both of IGBT and MOSFET short circuit test, which means that due to tail current or leakage current, DUTs could fail after the device turn-off. In general, bipolar devices, like IGBT, could be protected by the state-of-the-art de-saturation protection circuits with 10 μs decision time. For SiC MOSFET, as reported in [7], [22], the short circuit withstand time is about 13 μs under 400V V_{dc} for a 600V rated device. Besides the de-saturation protection method, some other methods are being explored like solid-state circuit breaker (SSCB) and fault current evaluation scheme [14].

Short circuit capabilities of 600 V/ 650 V class GaN power devices are reported in [7]. The short circuit withstand time for 600V E-mode GaN HEMT is 4.5 µs when V_{ds} equals to 150 V, while for the 600 V cascode GaN HEMT, the failure time is only 1.8 µs at 300V V_{dc}.

Previous short circuit tests results indicate that the critical energy and fault time of all kinds of devices are voltage dependent. GaN based device shows the lowest roughness when subjected to short circuit stress, and more tests are needed under different test conditions.

3.2. GaN HEMT short circuit behavior analysis

In order to explore the short circuit behavior of the GaN HEMT under HSF condition, the devices are subjected to single pulse stress with different dissipate energy.

Firstly, the tests are performed under room temperature (25 ^{o}C), and the DC bus voltage V_{dc} is selected from 100 V to 400 V. DUTs are tested with increased short circuit time T_{sc} at certain V_{dc}. T_{sc} starts from 100 ns, and the test is repeated with 100 ns as a step until the device failure. Time interval between two short circuit pulses is 1 minute.

One typical output waveforms are shown in the Figure 3.1. The test condition is V_{dc} = 400 V, T_{sc} = 300 ns, while the case temperature T_c is 25 ℃.

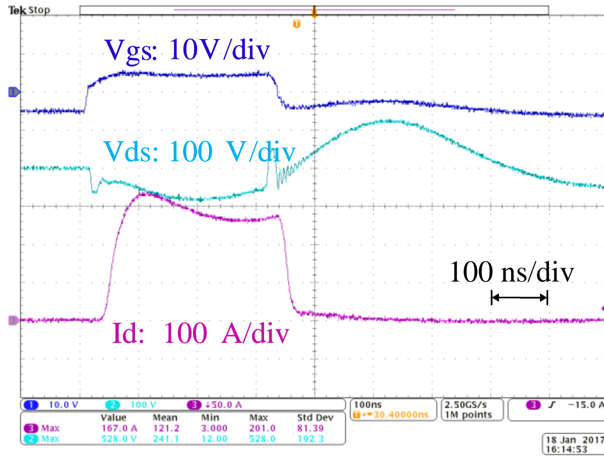


Figure 3.1 Example short-circuit waveform under HSF condition

In order have a better understanding of device performance under different conditions, drain to source current I_d and gate voltage V_{gs} are extracted from the oscilloscope, filtered and compared separately. Figure 3.3 shows the drain current I_d under different V_{dc} while the T_{sc} equals to 500 ns and the corresponding V_{gs} is shown in Figure 3.4.

From Figure 3.3, the current waveforms indicate that the device output behaviors are similar under different DC bus voltage and could be divided into three stage. Firstly, from t_1 to t_2, the transistor works in the linear region, and the output current increase quickly due to the low inductance in the main power loop. At the point t_2, the output current reaches the saturation region. As indicated by different peak current values under elevated voltage, the saturation current decreases as the DC bus voltage increase. This phenomenon is because of the higher junction temperature under higher DC bus voltage, at which the dissipated energy would be higher, leading to higher junction temperature due to self-heating.

Then the second stage begins at t_2 and last to t_3. During this period, the saturation current of the GaN HEMT is influenced by gate to source voltage V_{gs}. As is shown in Figure 3.4, there exists a valley in the V_{gs} waveform after the device fully turn on, and as saturation current increase with V_{gs}, the output current will show a similar feature as the V_{gs} waveform.

Next, the device is turned off at t_3. With a turn-off signal from gate voltage, drain current decrease quickly. During the turn-off transient, oscillation happens between decoupling capacitors, device parasitic capacitors and stray inductance. As the measured current value also includes the current flows in the device parasitic capacitance, like C_{ds} and C_{gd}, before the measured current reaches zero, a small current occurs under different V_{dc} and different T_{sc}, as is shown in Figure 3.5. The tail currents induced by oscillation under different test conditions have similar peak value. The reason for the tail current is quite different with the tail current observed in the IGBTs, which is induced by minority carriers, and could cause thermal runaway phenomenon and lead to delayed failure eventually [21].

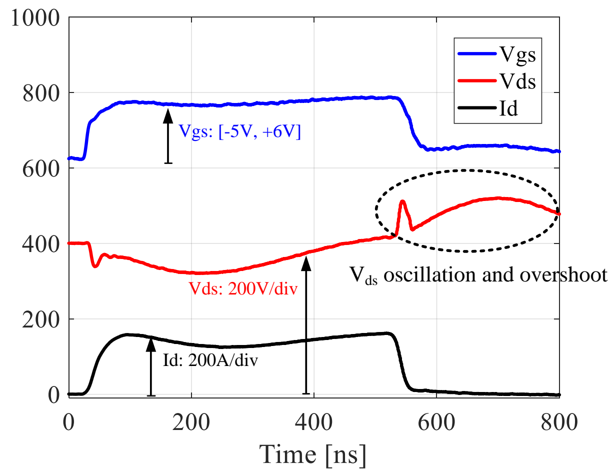


Figure 3.2 GaN HEMT short circuit waveform

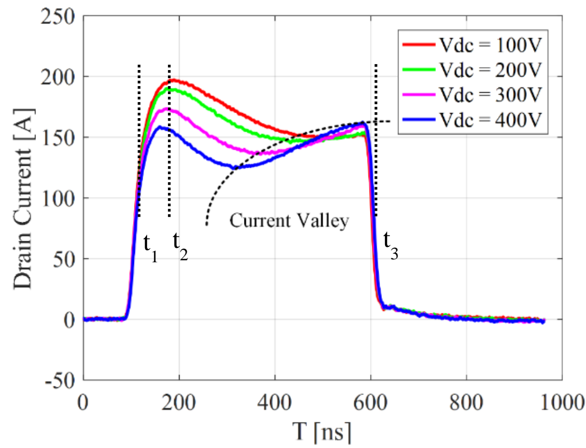


Figure 3.3 GaN HEMT short circuit current at 500 ns with different V_{dc}

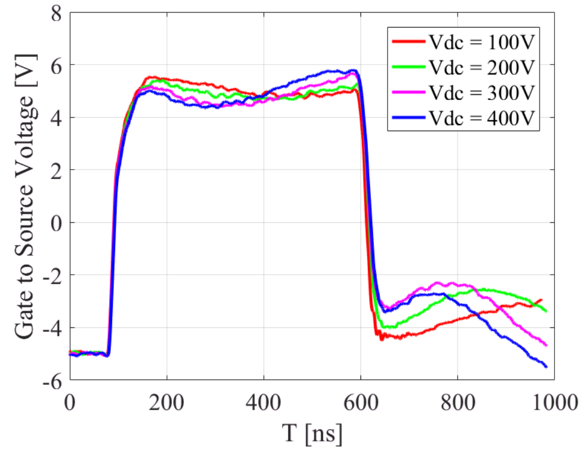


Figure 3.4 GaN HEMT gate to source voltage at 500 ns with different V_{dc}

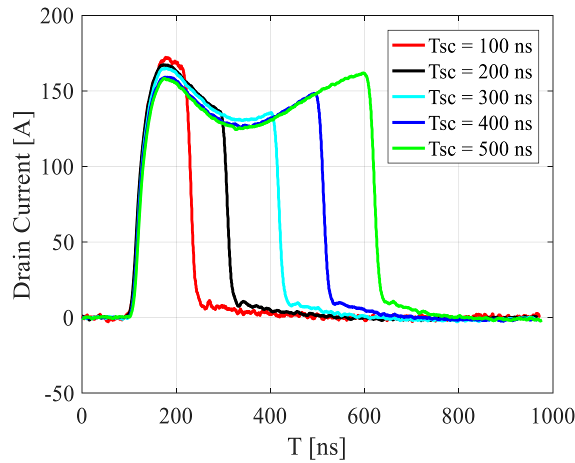


Figure 3.5 GaN HEMT short circuit current at 400 V with different Tsc

GaN HEMT short circuit behavior under longer duration and high temperature are also evaluated in this work. During the elevated temperature tests, DUT is placed on a hot plate and the thermal grease is used to make sure a good contact between PCB and hot plate. Chip temperature is measured from the top side of GaN HEMT using a thermal coupler. The test setup is shown in Figure 3.6, and the tests are conducted under V_{dc} =

300V, T_{sc} = 3.2 μs. Figure 3.7 and Figure 3.8 show the test results under 25 ºC and 125 ºC correspondingly.

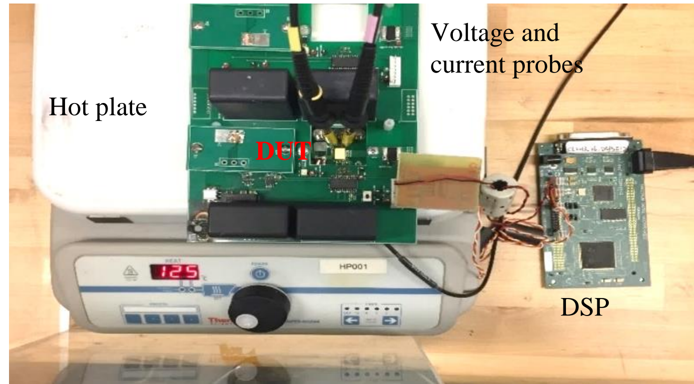


Figure 3.6 Elevated temperature short circuit test set up

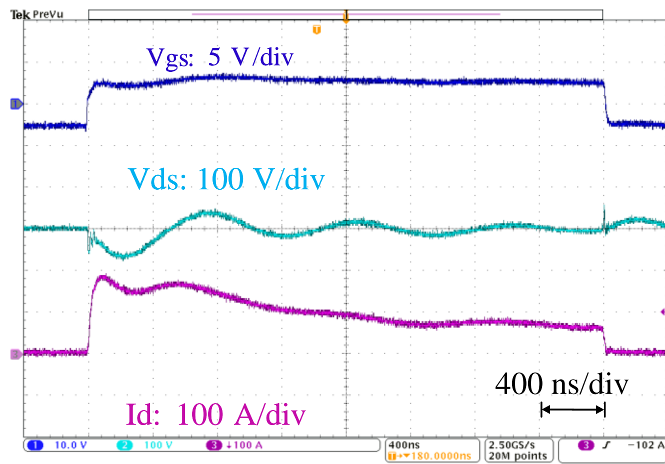


Figure 3.7 GaN HEMT short circuit waveform under 25 ºC

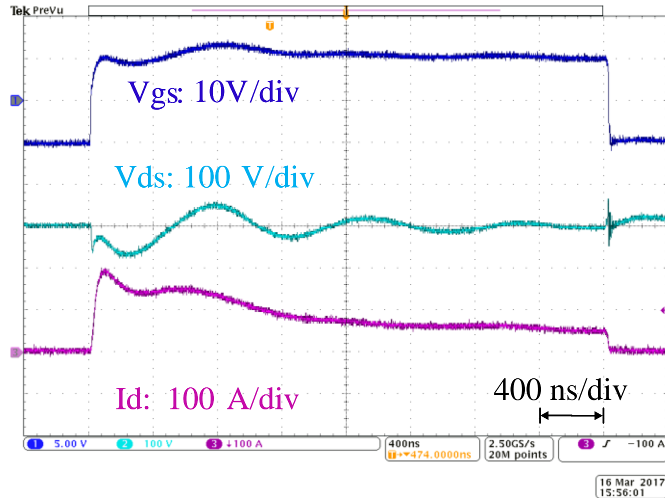


Figure 3.8 GaN HEMT short circuit waveform under 125 °C

Time dependent dissipated power is calculated based on the test waveform for each test condition, then the junction temperature could be simulated based on LTspice thermal model. The results are shown in Figure 3.9.

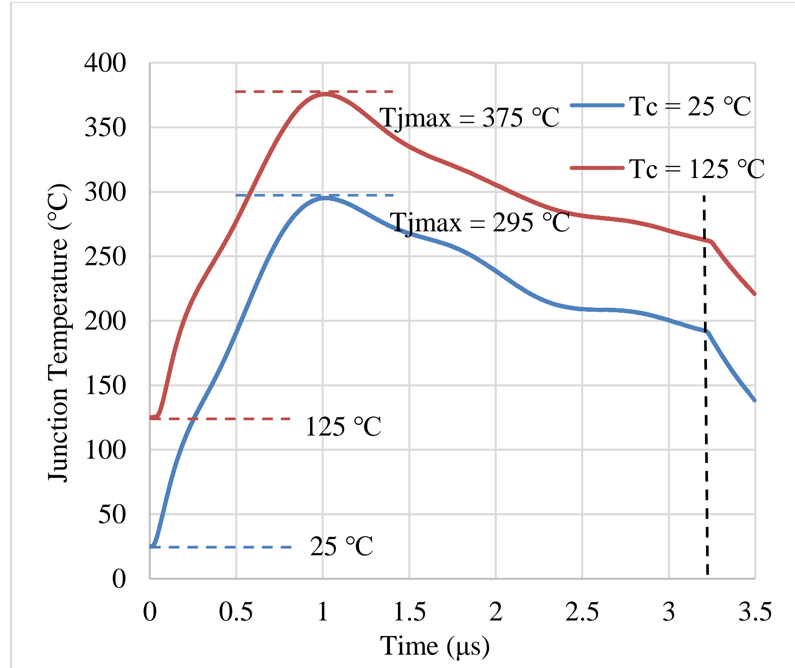


Figure 3.9 Simulated device junction temperature. V_{dc} = 300V, T_{sc} = 3.2 μs

For the short-circuit current waveform, besides the fluctuation influenced by V_{gs}, it shows a decreasing trend as the temperature keeps increase during the short circuit period. As results, the dissipated power would decrease as the current become smaller. For the device temperature distribution under these test conditions, the maximum temperature occurs at about 1μs after the device turn-on, this is because that it takes a response time for RC network to reflect the change in the input power to the output temperature.

3.3. GaN HEMT short circuit capability

Short circuit reliability of a power device usually is evaluated by the critical energy E_c, which is defined as the minimum energy that could lead to the device failure [7]. In order to determine the E_c of DUT under different condition, destructive short circuit tests are

repeated under 400 V at both 25 ℃ and 125 ℃. The test results are shown in Figure 3.10 and Figure 3.11.

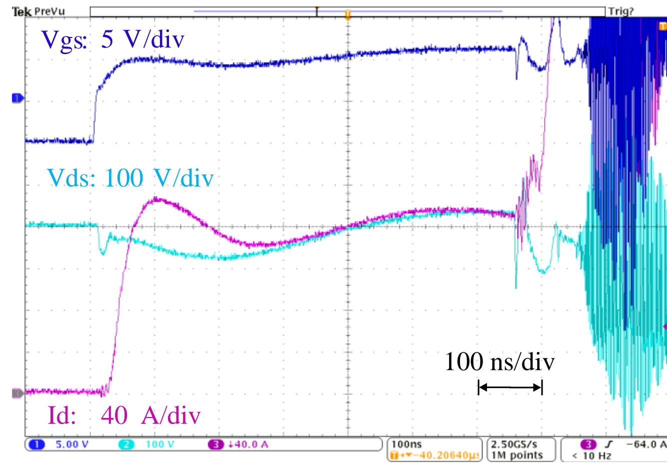


Figure 3.10 E-mode GaN HEMT failure waveforms in short circuit test. V_{dc} = 400 V, R_{goff} = 20 Ω, Tc = 25 ℃.

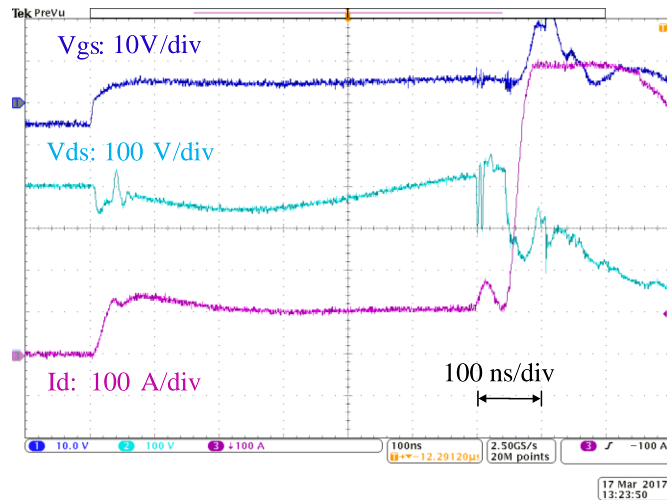


Figure 3.11 E-mode GaN HEMT failure waveforms in short circuit test. V_{dc} = 400 V, R_{goff} = 20 Ω, T_c = 125 ℃.

The device critical energy is defined by equation (4)

$$E_c = \int_{t_1}^{t_2} V_{DS} \cdot I_{SC} \cdot dt \qquad (4)$$

To investigate the influence of maximum junction temperature on the device failure, time dependent temperature distribution is simulated based on the thermal model discussed in Chapter 2.5.

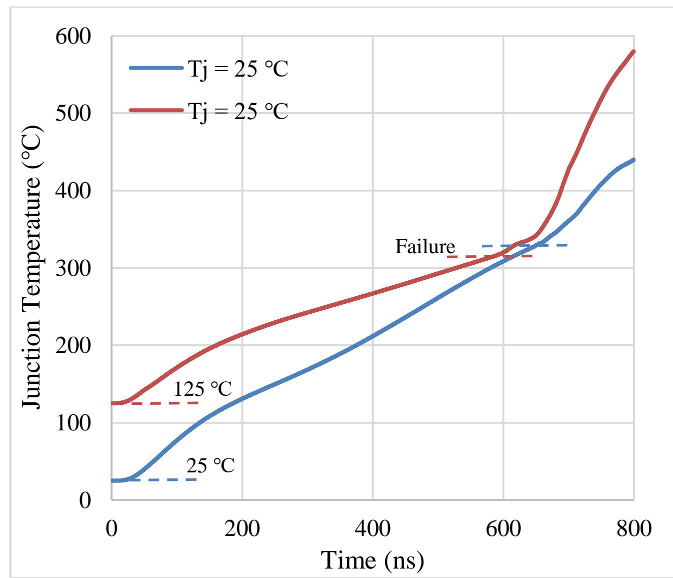


Figure 3.12 Simulated device junction temperature under failure condition. V_{dc} = 400V

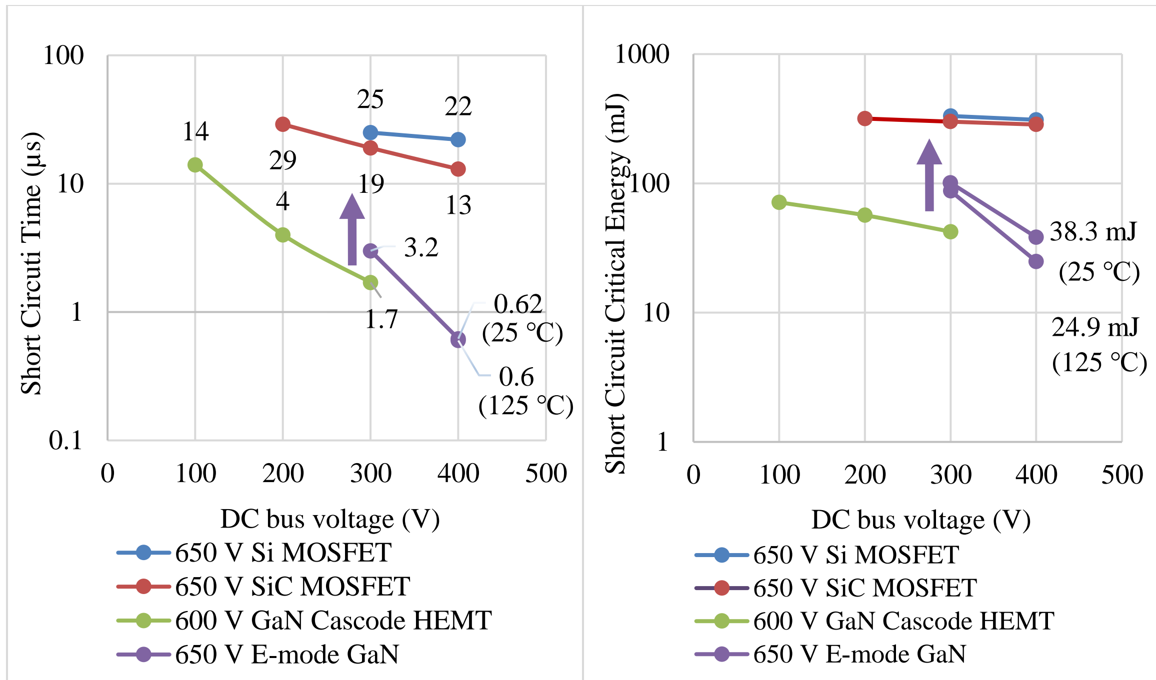
Table 3.1 summarizes the test condition and results, indicating the Critical energy E_c, Maximum short circuit current I_{peak}, maximum junction temperature T_j, and the failure time T_{sc}.

Table 3.1 Critical energy tests specification

Voltage	Case temp.	T_{sc}	I_{peak}	T_j	E_c
400 V	25 °C	630 ns	188 A	332.7 °C	38.3 mJ
	125 °C	600 ns	150 A	315.8 °C	24.9 mJ

As indicated in Table 3.1, higher case temperature leads to lower device critical energy and shorter short circuit time before failure. the maximum junction temperature before failure is similar under different case temperature. This is because that high case temperature limited the short circuit current, which leads to a lower dissipated power and lower temperature rise in the same time period.

The critical energy and failure time under 400V V_{dc} are calculated and compared with other types of power transistor reported in [7] as shown in Figure 3.13. It can be observed that E-mode GaN HEMT capability is in line with the commercially available cascode D-mode GaN HEMT and much smaller than Si and SiC MOSFET. The T_{sc} is about 630 ns at V_{dc} equals to 400 V, which bring great challenge to the existing overcurrent protection method. Total dissipated energy and short circuit time under 300V V_{dc}, 3.2 μs T_{sc} are calculated and included in these figures.



(a) (b)

Figure 3.13 Power device short circuit capability comparison (a) Critical energy (b) short circuit withstand time

3.4. E-mode GaN HEMT failure mechanism

A detailed failure waveform is given to have a better understanding of the fault transient. Figure 3.14 and Figure 3.15 shows the test waveform under 400 V V_{dc} and case temperature is 25 ℃ and 125 ℃.

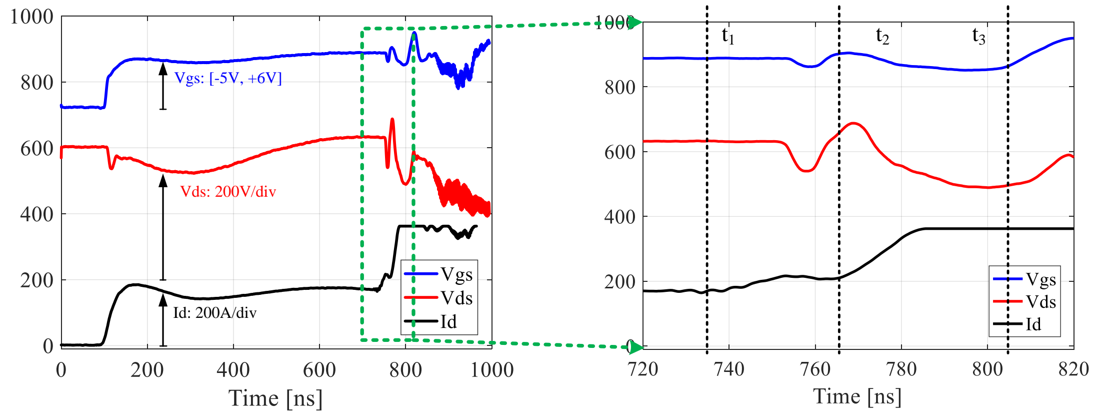


Figure 3.14 Failure waveforms with detailed failure transient. V_{dc} = 400 V, T_c = 25℃

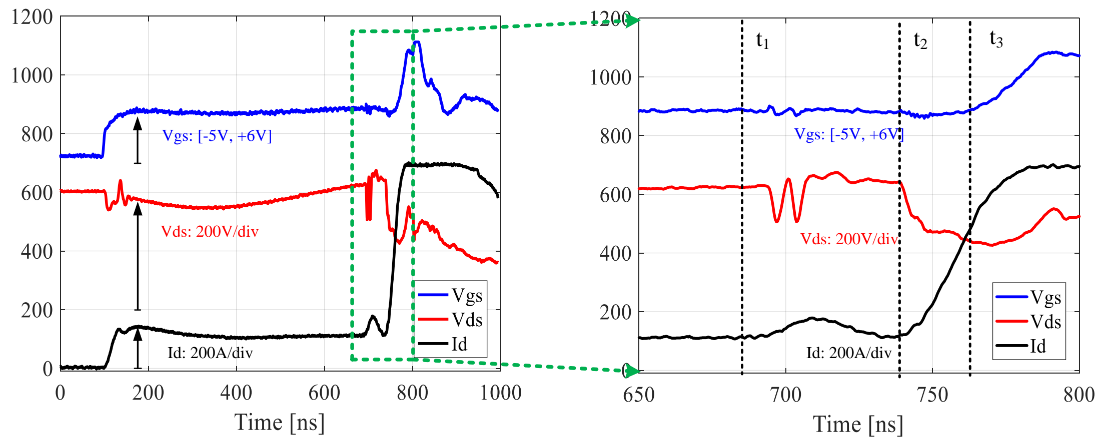


Figure 3.15 Failure waveforms with detailed failure transient. V_{dc} = 400 V, T_c = 125℃

As is shown in Figure 3.14 and Figure3.15, the failure transient is similar in both cases. Firstly, device failure happened at point t_1, and the critical energy is calculated from the turn on point to t_1, which corresponding to the critical energy of 38.3 mJ and 24.9 mJ under different case temperature. Then, an oscillation occurs on the V_{ds} from t_1 to t_2, and at the same time, a voltage dip could be observed on V_{gs} as it is influenced by V_{ds}. Finally, the device completely failure happened at point t_3, at which the short circuit

current is above four times larger than the normal value. Then V_{gs} begin to increase as the failure current keeps increasing, which may result from gate dielectric breakdown.

N. Badawi, et, al. [7] reports a kind of failure mechanism based on 600V e-mode GaN HEMT short circuit test. According to the published results and conclusion, device main channel over-temperature and drain-to-gate dielectric breakdown are likely to be the major failure mechanisms.

Chapter 4. E-mode GaN HEMT short circuit degradation

Besides the critical energy and failure time of the device, another critical parameter determining the roughness of the device is the reliability under repetitive electrical stress. In this section, e-mode GaN HEMTs are subjected to repetitive short circuit pulses and several static characteristics are tested after each group of pulses by curve tracer. Among the characteristics recorded and compared, the shifting ones could be regarded as the degradation indicators.

4.1. Overview of power device degradation mechanism and indicators

During years of practice, degradation behaviors of some power devices are well investigated, like the Si IGBT and SiC MOSFET. The degradation indicators include but not limited to larger gate to source leakage current, drain to source leakage current and reduced channel conductivity. The repetitive short circuit capability of 600-class Si IGBT and MOSFET are close to 40 thousand times at Vdc equals 400 V with 3 s intervals, as long as the short circuit energy is less than the critical energy [21].

100 V/ 90A E-mode GaN HEMT degradation performance is tested and reported in [8], [9]. When device is subjected to pulsed overcurrent up to 310% rated current, the gate structure would suffer significant degradation, shown as lower gate to source voltage and larger gate current [9]. Besides, device forward characteristics and transconductance is monitored in the long-term reliability test, which turned out that the only slight decreasing of transconductance is observed after 50,000 pulses.

4.2. Degradation tests and degradation indicators

In this section, the tests are performed under repetitive pulses with different dissipated energy, and the static characteristics are monitored before any stressors and after each group of pulses to testify the changes and find out the degradation indicator. Tested items include 1st and 3rd quadrant IV family curves, threshold voltage V_{th}, gate to source leakage current I_{gss}, and drain to source leakage current I_{dss}.

Four cases with different stressors were selected to investigated the device ruggedness. The first group of tests is carried out at V_{dc} = 20 V and T_{sc} = 200 ns, which is used to evaluate the device reliability under low voltage and low junction temperature, and the only stressor subjected to device is high current in this case. Then the second group of tests is conducted under same T_{sc} but a higher DC bus voltage, which equals to 300 V. In this case, the short circuit energy is relatively low but high voltage could act as a new stressor. Next, case three and case four is carried out to observe the device short circuit behavior under high dissipated energy and high case temperature, to be specific, the DC bus voltage keeps at 300 V, but the short circuit duration is lengthened to 3200 ns. Case temperature of first three cases is 25 ℃ and the case four is finished under 125 ℃. Enough time interval was waited between pulses to make sure that the junction temperature could drop back to case temperature.

Among these tests, all the DUTs could successfully turned off after the pulses, no failure condition is observed but only the degradation characteristics are concerned. Static characteristics are tested after each group of pulses until significant degradation could be observed through one or more parameters.

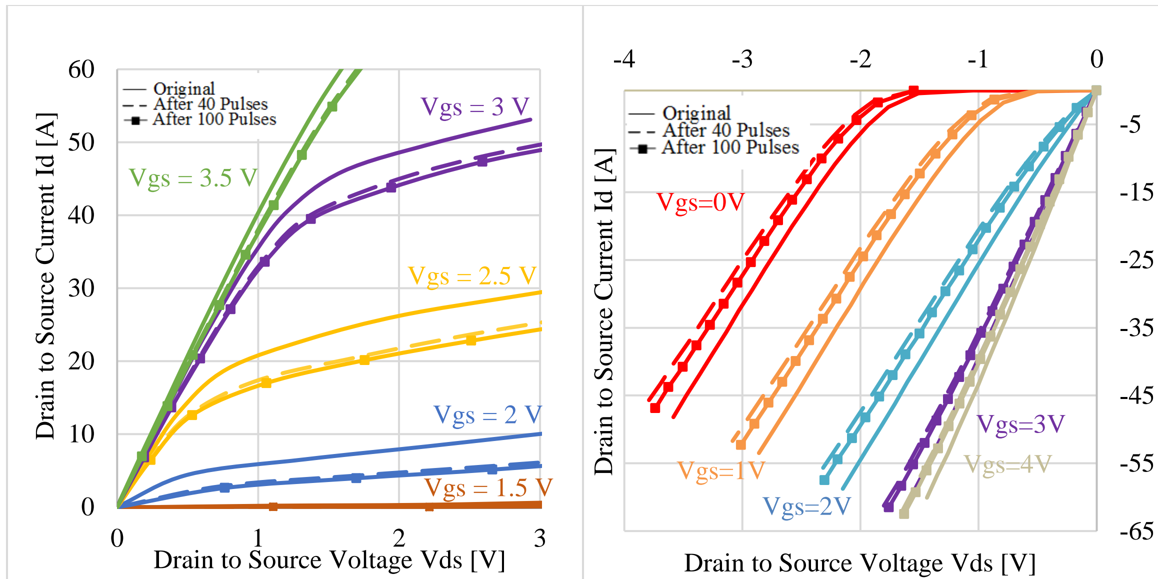
Test details and static tests result after one pulse are summarized in Table 4.1. Peak current I_{peak}, total dissipated energy E_{sc} of each case and maximum junction temperature T_j are also included.

From Table 4.1, some phenomena and conclusion could be derived. Firstly, the short circuit current is quite high in four cases when compared with the device rate current, which means the high current stress always exist in the short circuit test. Then, from case one to case four, the short circuit energy changed a lot from 0.1 mJ to 115.7 mJ, and influenced by the dissipated energy, the peak junction temperature also varies a lot from 26.1℃ to 375 ℃. For the degradation indicators, threshold voltage and gate to source leakage current are selected as the gate performance indicator, while the main channel performance is reflected by on state resistance and drain to source leakage current. As indicated in Table 4.1, for gate performance under electrical stress, V_{th} would become larger while I_{dss} is smaller than the original status, this means that it is more difficult to turn on the degraded device. For the main channel performance, I_{dss} shows a decreasing trend, and the on-state resistance shift mainly happens in the low V_{gs} condition. To sum up, when more stressors are involved and short circuit energy is higher, the degradation is more obvious.

Table 4.1 Summary of GaN HEMT short circuit degradation tests

Parameters		Case 1	Case2	Case 3	Case 4
V_{dc} [V]		20	300	300	300
T_{sc} [ns]		200	200	3,200	3,200
I_{peak} [A]		166	234	216	202
T_j [ºC]		26.1	110	343	375
T_c [ºC]		25	25	25	125
E_{sc} [mJ]		0.1	9.2	115.7	87.4
Gate Performance	V_{th} (V_{ds} = 10 V)	Negligible change after 1 SC	Negligible change after 1 SC	Positive Shifting +4% after 1 SC	Positive Shifting +7% after 1 SC
	I_{gss} (V_{gs} = 6 V)	Negligible change after 1 SC	Negative Shifting -18% after 1 SC	Negative Shifting -61% after 1 SC	Negative Shifting -18% after 1 SC
Main Channel Performance	R_{dson} (V_{gs}=2.5 V, I=30 A)	Negligible change after 1 SC	Negligible change after 1 SC	Positive Shifting +5% after 1 SC	Positive Shifting +86% after 1 SC
	R_{dson} (V_{gs}=6 V, I=30 A)	Negligible change after 1 SC	Negligible change after 1 SC	Negligible change after 1 SC	Negligible change after 1 SC
	I_{dss} (V_{ds}=650 V)	Negligible change after 1 SC	Negative Shifting -19% after 1 SC	Negative Shifting -39% after 1 SC	Negative Shifting -40% after 1 SC
Stressors		Current	Voltage, Current,	Voltage, Current, Energy, Temp.	Voltage, Current, Temp., Energy

For case one, which refers to the low stress and slow degradation case, DUT is subjected to 100 short circuit pulses altogether, and static characteristics are tested after each 20 pulses to observe how the characteristics shift happens during the degradation procedure. Figure 4.1 to Figure 4.3 shows the selected parameters, including IV family curves, leakage current, and threshold voltage.



(a) (b)

Figure 4.1 GaN HEMT output characteristics comparison under 25 ℃. (a) 1st quadrant I_d vs. V_{ds}. (b) 3rd quadrant I_d vs. V_{ds}

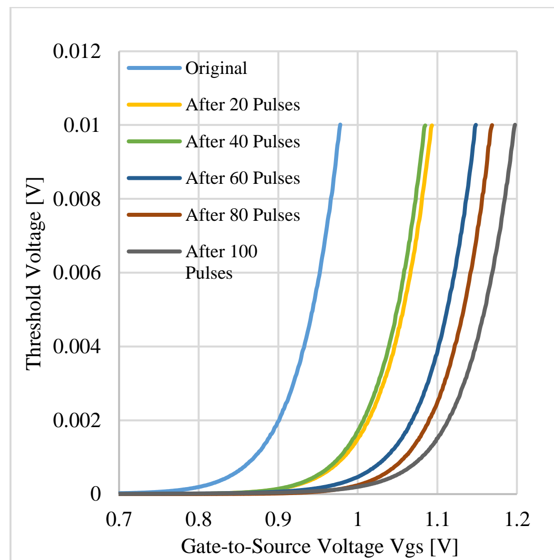
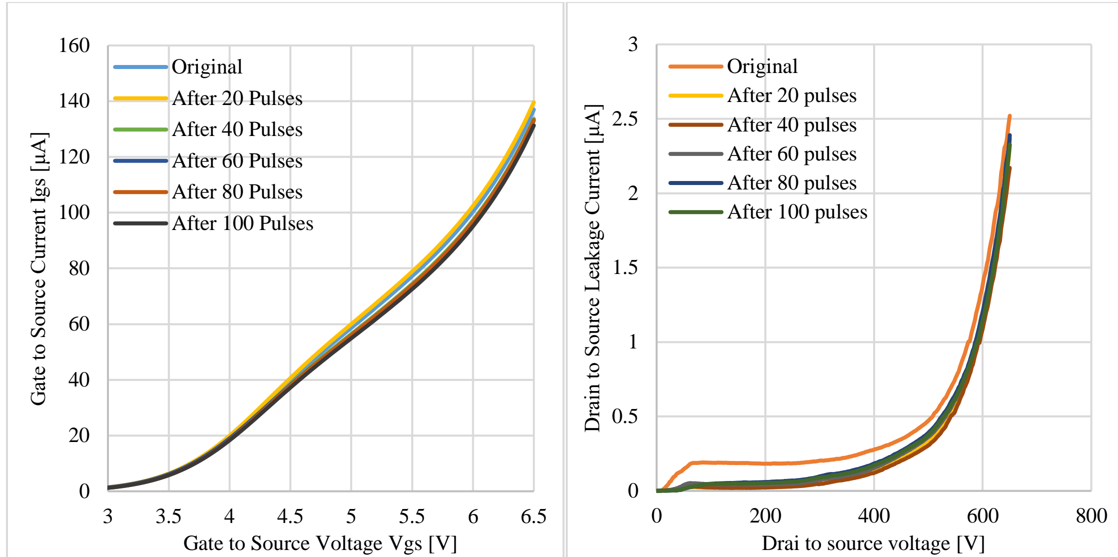


Figure 4.2 GaN HEMT threshold voltage comparison under 25 ℃



(a) (b)

Figure 4.3 GaN HEMT leakage current comparison under 25 ℃. (a) Gate to source leakage current (b) Drain to source leakage current

4.3. Degradation mechanism

The shifting parameters shown in Chapter 4.2 indicates that the e-mode GaN HEMT devices short circuit degradation mainly happens in the main channel, and reflected as decreasing conduction capability.

Decreasing output current and a positive shift of threshold voltage have be reported in several publications focusing on RF power applications [23], [24], [25]. According to some hypothesis, after high power DC stress, the permanent output capability drop may because of the AlGaN relaxation, like the inverse piezoelectric effect, which could reduce the 2DEG density and therefore the output current [23]. Another publication tested the reliability of the devices under different stressor, and two mechanisms and two trapping

effect are provided. The trapping effects discussed in [23] focuses on the recoverable process, which is inconsistent with the test results in this work. However, for the high current stress, it attributes the positive threshold voltage shift to the gate sinking, which is result from the high temperature around the gate terminal, especially on the drain side.

Chapter 5. Summary

This paper presents the short circuit behavior and roughness of a commercially available 650 V/60 A E-mode GaN HEMT. Similar to Si IGBT, soft turn-off is recommended to terminate the E-mode GaN HEMT short circuit condition. Additionally, recommended turn-off conditions, device critical energy, short circuit time are provided and are compared to other types of power transistor. Degradation indicators and repetitive short circuit capability of the E-mode GaN HEMT have been calculated. As one of the earliest work exploring high voltage large current E-mode GaN HEMT short circuit roughness, this work provides information to both GaN HEMT and GaN converter designers for the device performance improvement and the circuit protective function design.

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