INFORMATION TO USERS

This manuscript has been reproduced from the microfilm master. UMI films the text directly from the original or copy submitted. Thus, some thesis and dissertation copies are in typewriter face, while others may be from any type of computer printer.

The quality of this reproduction is dependent upon the quality of the copy submitted. Broken or indistinct print, colored or poor quality illustrations and photographs, print bleedthrough, substandard margins, and improper alignment can adversely affect reproduction.

In the unlikely event that the author did not send UMI a complete manuscript and there are missing pages, these will be noted. Also, if unauthorized copyright material had to be removed, a note will indicate the deletion.

Oversize materials (e.g., maps, drawings, charts) are reproduced by sectioning the original, beginning at the upper left-hand corner and continuing from left to right in equal sections with small overlaps.

Photographs included in the original manuscript have been reproduced xerographically in this copy. Higher quality 6" x 9" black and white photographic prints are available for any photographs or illustrations appearing in this copy for an additional charge. Contact UMI directly to order.

Bell & Howell Information and Learning
300 North Zeeb Road, Ann Arbor, MI 48106-1346 USA
800-521-0600

UMI®

MODELING OF RF POWER TRANSISTORS FOR POWER AMPLIFIER DESIGN

DISSERTATION

Presented in Partial Fulfillment of the Requirements for

the Degree Doctor of Philosophy in the

Graduate School of The Ohio State University

By

Siraj Akhtar, B.S.E.E., M.S.E.E.

* * * * *

The Ohio State University

2000

Doctoral Committee:

Professor Patrick Roblin, Adviser

Professor Steven Bibyk

Professor Roberto Rojas

Approved by

Adviser

Department of Electrical Engineering

Bell & Howell Information and Learning Company
300 North Zeeb Road
P.O. Box 1346
Ann Arbor, MI 48106-1346

ABSTRACT

Presented is a large/small signal, non-quasi-static, charge conserving, MOSFET modeling technique suitable for DC and high frequency circuit design. The technique is theoretically developed for a SOI MOSFET on a physical device simulator and is applied to a LDMOSFET device.

A DC electro-thermal model is developed by using a single thermal resistance to map the thermal response of the device. A novel and inexpensive automated approach to measuring iso-thermal IVs and microwave scattering parameters is discussed as an alternative to using expensive pulsed IV, pulsed RF measurements. The iso-thermal IV is used by the device in establishing its DC point of operation. The iso-thermal s-parameters are used to extract temperature dependent small signal model parameters. A novel extraction technique utilizing analytical expressions is presented. The extraction procedure yields a continuum of solutions as a function of the source parasitic resistances, R_s. A multi-bias analysis is used to determine the final R_s. g_m, C_{11}, and C_{21} are found to vary with temperature while g_d, C_{12}, and C_{22} are found to exhibit much less temperature variation.

Hot and cold pulsed IVs are compared with iso-thermal IVs. Their associated transconductances are compared to RF g_m obtained from microwave measurements. The existence of low frequency dispersion in LDMOSFETs, in spite of the $p+$ sinker,

is demonstrated. It is verified that globally over temperature, the iso-thermal IVs still agree the best with $g_{m,RF}$.

A temperature dependent large signal model is generated by integrating temperature dependent $g_{m,RF}$ and $g_{d,RF}$. 3D Tensor Product B-Splines (TPS) utilizing an optimum knot placement scheme, are used to represent the IV and it's associate derivatives. Optimum knot placement is necessary to handle areas of large derivative variation in data. Optimized TPS is used to represent the capacitances and extract the gate and drain charges.

The large signal model is implemented in ADS as a user defined model. In the process of doing so, a number of bugs in ADS were reported to Agilent. Harmonic balance simulations are conducted on a power amplifier and amplifier matrices such as fundamental, second and third harmonic power, drain current, temperature and two tone intermodulation distortion predicted by the model are compared to measured results. The impact on the model of temperature dependent drain and gate charge is investigated. Higher temperature is found to introduce more profound sweet spots. The model, in spite of its simplifications, is found to compare well with the existing MET model, which is based on pulsed IV and pulsed RF. For two tone IMD simulations, the developed model is found to out perform the MET model.

In memory of my late father

ACKNOWLEDGMENTS

I would like to express my sincere appreciation to my adviser Professor Patrick Roblin for his wonderful support, advice and encouragement rendered during the entire length of my graduate studies. The many hours of thoughtful discussions we had, have had an enormous bearing on the completion of this work. I would also like to thank Professors Steven Bibyk and Roberto Rojas for their suggestions and participation on my Doctoral Examination Committee.

Lucent Technologies and Jeff Strahler have provided continuous financial support and technical guidance for this work. Their contribution is greatly appreciated.

A number of students in the Microwave Lab deserve mention for helping in this work. In particular, Sunyoung Lee (pulsed IVs), Xiaohui Ding (amplifier testing), Shuang Yu (power amplifier design), and Julie Kasick (conversion of FORTRAN code to C). I am also indebted to many of my friends, from near and far, who have helped and supported me, in some way or the other, throughout my studies.

I would like to thank my mother, brothers and sister, for their endless support and encouragement, that has always been a profound source of inspiration throughout my life. Finally, a most special appreciation is due to my wife for the wonderful person she has been to me by being a pillar of immense support.

VITA

March 14, 1974	Born - Peshawar, Pakistan
May 1993	B.S., Electrical Engineering University of Mississippi University, Mississippi
September 1993 - August 1994	NEC/Litton Graduate Fellow, Dept. of Electrical Engineering, The Ohio State University Columbus, Ohio
September 1994 - August 1995	Graduate Research Associate, Dept. of Electrical Engineering, The Ohio State University Columbus, Ohio
September 1995 - March 1996	Graduate Research and Teaching Associate, Dept. of Electrical Engineering, The Ohio State University Columbus, Ohio
March 1996	M.S., Electrical Engineering Ohio State University Columbus, Ohio
March 1996 - December 1999	Graduate Research and Teaching Associate, Dept. of Electrical Engineering, The Ohio State University Columbus, Ohio
December 1999 - Present	Lucent Fellow, Dept. of Electrical Engineering, The Ohio State University Columbus, Ohio

PUBLICATION LIST

1. P. Roblin, S. Akhtar, R. Potter and A. Fathimulla, "Analysis and measurement of the capacitance-voltage characteristic of a resonant tunneling diode," *American Physical Society, March 1995 meeting, San Jose, CA.*

2. S. Akhtar and P. Roblin, "B-spline Based, Large-signal DC and Microwave-model for SOI-MOSFETs," accepted for publication, *Analog Integrated Circuits and Signal Processing*, Kluwer Academic Publishers, Norwell, MA.

3. S. Akhtar, P. Roblin, and J. Strahler, "Electro-thermal and Iso-thermal Characterizations of Power RF Silicon LDMOSFETs," *IEEE Electron Device Letters*, submitted for publication.

4. P. Roblin, S. Akhtar, and J. Strahler, "New Non-Quasi-Static Theory for Extracting Small-Signal Parameters Applied to LDMOSFETs," *IEEE Microwave and Guided Wave Letters*, accepted for publication.

5. S. Akhtar and P. Roblin, "Microwave FET Device Modeling," Book chapter in *High Speed Heterostructure Devices*, P. Roblin, Cambridge University Press, Cambridge, UK.

6. S. Akhtar, P. Roblin, and J. Strahler, "Electro-thermal RF Modeling of LDMOSFETs for Power Amplifier Design," *IEEE Transactions on Microwave Theory and Techniques*, submitted for publication.

FIELDS OF STUDY

Major Field	: Electrical Engineering
Major Area of Specialization	: Microwave and Microelectronics
Minor Area of Specialization	: Mathematics

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

CHAPTER 1

Introduction

1.1 Device Modeling

Silicon MOSFETs have in recent years experienced a substantial growth in popularity for power RF and microwave circuit applications. The increasing use of these devices has led to substantial effort being undertaken to develop accurate analytical device models. From a design perspective, a microwave circuit can only be as good as the device models and computer simulation tools that are available to the designer. Accurate and computationally efficient device models that are easy to extract from measured data and can easily be incorporated into a circuit simulator environment are essential for the design and optimization of microwave circuits.

Although a model can come close, it can never exactly reproduce the performance of a device. Hence it is important to realize that the modeling effort may need to be tailored towards the kinds of circuits being simulated. This can be very important

given the fact that not only accuracy, but also speed and convergence are important factors that a model needs to address.

1.2 Physical Versus Table Based Models

SPICE based FET models, such as versions of BISIM, use physics based equations to model the device [1] [2]. In order to account for any additional physical effect, a new equation is added in. This leads to an increasing number of different, and some what complex, equations that have to be accounted for by the model.

In the table modeling approach, a generic set of equations is used to interpolate between model parameters. This can lead to a reduction in complexity of the equations while allowing for charge conservations [7],[8] and continuity of derivatives, provided that the original set of generic equations can handle this. Table modeling begins by picking the right model topology for the device. The problem however is that often times model parameters extracted do not have physical meanings to the values and are simply chosen to give the best fit.

Physics based models have found increasing use for bipolar type devices while FET modeling, particularly at high power, is dominated by table modeling approaches. Yet, perhaps it is the combination of these two methods that will yield the best results. In this Thesis, emphasize is given to on deriving and using table based approaches for device modeling that incorporate physical constraints.

1.3 SOI MOSFET Devices and Modeling

Silicon on Insulator (SOI) MOSFETs are gaining tremendous appeal for low power RF CMOS applications that integrate RF and digital circuitry on a single chip. Additionally, SOI MOSFETs are considered a leading candidate to replace bulk CMOS in future ULSI systems [3]. SOI technology has actually been around for decades, but was initially only considered as a replacement to Silicon on Sapphire (SOS) technology in some very selected applications. In recent years, substantial research efforts have been made in order to better understand and implement SOI technology to microwave circuit design. Particularly with the development of the commercial SIMOX (Silicon isolated by IMplanted OXygen) and MICROX^{TM} (Microwave SIMOX) processes [4], SOI fabrication technology has established a strong foothold.

Because of the isolation of a SOI device due to the Silicon dioxide layer, parasitic capacitances are greatly reduced, compared to bulk silicon devices. This leads to the SOI device having a better high-frequency performance and thus makes it a better candidate for microwave circuit applications. Further, the presence of the insulating Silicon dioxide layer, eliminates any current path to the substrate. This removes the possibility of latch-up problems limiting device performance [17].

However, the insulating oxide layer gives rise to floating body effects in partially depleted SOI MOSFETs [5]. These however, can be eliminated by using body ties. Another problem that limits the performance of SOI devices is a phenomena called

self-heating [16]. This effect is caused by the inability of the device to optimally dissipate due to the presence of the insulating film, the internal heat generated. Particularly at high drain and gate voltages, self-heating effects are prominent due to the large drain current. The heat build up within the device causes the mobility of the charge carriers to fall. This leads to a decrease in drain current thereby implying a negative transconductance.

A charge based, large-signal, SOI MOSFET model using analytical expressions was reported by Lim and Fossum [6]. Charge based large-signal techniques have been applied to the modeling of ordinary FETs [7] and other high frequency FET type devices, such as MESFETs and HEMTs [8]. Recently, Daniels *et. al.* [9] implemented a Tensor Product Spline (TPS) charged-based technique that includes non-quasi-static effects to the modeling of a 3-terminal HFET device. The TPS method using B-splines was first introduced by Bischoff [10] as a novel approach for device modeling and latter various modifications were used by others [11],[12],[13]. The inclusion of non-quasi-static effects [14], [15] accounts for characteristic charge redistribution time constants, necessary for accurate modeling at frequencies above f_t.

While essentially resembling the modeling of FET devices, SOI MOSFET modeling differs in that self heating, floating body effects, and the associated low frequency dispersions have a significant bearing on the device performance [16], [17]. A number of works on estimating and modeling these effects have been published [18]. However, for the most part, the two constraints mentioned have relatively large time constants

and hence have more impact at lower frequencies. For microwave operation, it can be argued that the device voltages and currents change fast enough such that self heating and floating body effects do not have time to significantly alter the device performance around a fixed bias point. The added complexity and decrease in computational speed caused by the incorporation of low frequency effects into the model may be an unnecessary complication in light of the fact that a microwave model is desired. It is this fact that has led to growing interest in transient IV measurements [19],[20],[21] and derivation of device models using such measurements [22].

1.4 LDMOSFET Devices and Modeling

When it comes to microwave circuit design, MESFETs (Metal Semiconductor FETs) had been a leading candidate in the past. However, due to limitations in their high frequency performance, MESFETs are being challenged by Pseudomorphic High Electron Mobility transistors (PHEMTs) and Hetrojuction Bipolar Transistors (HBTs). HBTs are normally fabricated from III-V compounds such as GaAs and InP. Recent advances have led to the use of InGaP (considered an improvement over the traditional AlGaAs HBT), while for higher power, SiC and GaN are showing much promise [23]. However, the large high order intermodulation distortion (IMD) and the need for ballasting to stabilize minority carrier devices are factors that are pushing for adoption of FETs. Due to thermal runaway in BJTs increasing temperature causes

an increase in gain and hence current consumption, causing the DC biasing network to become complex.

MOSFETs for RF applications differ from those for VLSI applications by featuring larger channel length, greater junction depths and thicker gate oxides to handle the large power. Such devices are being fabricated to give better gain and IMD performance over bipolars.

For high power applications under 2.3 GHz, silicon Laterally Diffused MOSFETs (LDMOSFETs) are now taking over the market from GaAs and Si bipolar for linear power amplification [23]. A number of semiconductor manufacturers are working on these devices for base station applications, with Motorola already on its fifth generation.

Fig. 1.1 shows a cross sectional view of a basic LDMOS structure, which is predominantly a lateral surface effect device [24] with horizontal current flow. At least three factors differentiate a LDMOSFET from the more traditional Doubly Diffused MOSFET (DDMOS). The $p+$ source sinker shorts the source to the body. This has a number of advantages. The sinker acts as a resistive metallic body tie, greatly reducing floating body effects as a result of the parasitic bipolar. Since it eliminates the need for parasitic wire bonds, it minimizes the source inductances, hence minimizing loss in the high frequency gain due to negative feedback. Additionally, the sinker brings the source contact to the bottom of the transistor allowing for easy flange mounting and thermal sinking [25].

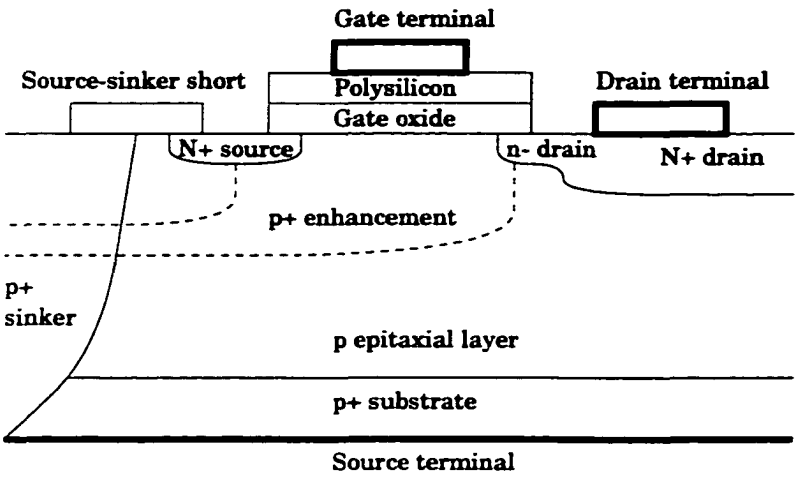


Figure 1.1: Cross sectional view of a LDMOSFET

The n-channel LDMOSFET shown contains a n lightly doped drain region which acts as a Junction FET, turning on at higher drain source voltages [26]. The length and doping in this drain extension, together with the epi-layer thickness and resistivity, determine the breakdown voltage of the device [24]. Last, but not least, a laterally diffused $p+$ channel implant is used to prevent punch through at high drain source voltages. Because of the high power dissipated in the device, thermal effects are considerable. In particular, the channel resistance increases with temperature, causing a reduction in RF power gain.

By combining dies in parallel, LDMOSFETs with CW output power as high as 155 W at the 3 dB compression point at 2.12 Ghz have been achieved [27]. Total gate periphery lengths for the highest power device are approaching a kilometer!

Modeling of LDMOSFETs incorporates many of the factors already discussed for SOI and universal 3 terminal FET devices, with some exceptions. Because of the presence of the $p+$ sinker, low frequency dispersion effects are expected to be smaller than those observed in III-IV devices. The most significant and comprehensive effort for the electro-thermal modeling of LDMOSFETs has been undertaken by Motorola [28] for the development of their MET (Motorola Electro-Thermal) model. Their approach relies on using a variant of the Curtice model [29]. Device characterization is done using a pulsed IV (under cold bias), pulsed RF [30] system, that allows for pulsed s-parameters to be acquired. Probing is done on a single die which is then used to construct a model for any device that is formed from a parallel combination of such a die. Table based modeling using pulsed IVs and approximation B-Splines have been carried out by Collantes *et. al.* [31]. Their model however does not incorporate thermal effects.

Most small scale laboratories unfortunately do not posses the expensive equipment needed for pulsed IV, pulsed RF measurements and hence need to use other approaches to extract device models. It is with this point in mind that this work presents an alternative approach to LDMOSFET modeling.

1.5 Modeling for Power Amplifier Design

For low cost, low power, hand held, mobile applications (cellular phones and pagers), monolithic microwave integrated circuits (MMICs) and RF CMOS, are used to completely integrate the sub components of a transceiver system. These components include power amplifiers (PA), low noise amplifiers (LNA), mixers and voltage controlled oscillators (VCO). Because power consumption is the driving element in such designs, class C and higher amplifiers are used. These amplifiers give high power added efficiency (PAE) (50% to 60%) but tend to be very non-linear [32].

For RF CMOS technologies, power amplifiers for transmitters are designed using "low frequency techniques" where the aspect ratio of the transistor is varied until a certain gain is achieved. For matching purposes, the output resistance of the transistor is transformed to 50 Ω and the capacitance may be canceled by an inductor. For receivers, noise performance is of higher concern than maximizing gain. In such designs where low cost mass production is essential, it would be very impracticable to extract a device model from measured data for each transistor. In general the approach has been to try and use available transistor models (such as BISIM3). Once a good design has been achieved, the circuit can be mass produced. As long as device parameter fluctuations are small enough, the circuit performance will be acceptable due to the low power of the signals.

For power amplifiers that go into expensive and large infrastructure applications (cellular base stations and high power transmitters), maximizing output power and linearity is highly important since a number of channels are simultaneously combined and amplified before being sent to the antenna. Since both high linearity and PAE are important in such applications, class A or AB biasing is preferred. This inherently implies that DC power consumption will be high (PAE from 12% to 40%) and hence the temperature of the PA will significantly increase necessitating the need for cooling units. The high power and RF current densities imply that packaged devices and microstrip technology has to be used in such applications. "Microwave design techniques" that rely on measuring the s-parameters of the transistor at the desired bias point and frequency and then building an input and output matching circuit are used for these amplifiers. Load pull techniques can also be used to obtain data for building matching networks giving constant power gain. Because maximizing gain is very difficult in light of the high power and very low inherent device impedance, the matching circuits must be individually tuned to optimize performance [33]. Further, since there may be significant performance variations across devices, knowing the s-parameters for one transistor will not help much. Each device has to be individually measured and matching circuits accordingly built and tuned for best performance.

Extensive circuit simulations are almost always not performed for such amplifiers due to the unavailability of models that can accurately predict important PA characteristics such as power harmonics, PAE, two-tone intermodulation distortion (for

FDMA AMPS cellular systems), spectral regrowth and adjacent channel power (for CDMA) over a wide bias, temperature and frequency range. Hence, the need for such device models is essential to streamline the design of power amplifiers and provide a virtual testbed for the designer to carry out all sorts of tests on the amplifier and optimize the performance accordingly.

Such a model will have to be extracted from measured device data. The substantial variation in transistor parameters calls for a scheme where by the model extracted for one device can be fitted to another device with the smallest amount of additional measurements.

1.6 Problem Statement and Research Outline

From the previous section, it is clear that there is a pressing need for accurate and robust transistor models to improve the design and optimization of power amplifiers. Motorola, a manufacturer of a wide variety of high power silicon RF MOSFETs, is leading in house efforts to develop such models. End users of these power RF MOSFETs, such as Lucent Technologies, a manufacturer of power amplifiers for base stations, are supporting independent efforts in this front.

The focus of this research is to come up with accurate table based device models that can easily be extracted from measured data and can be used by PA manufacturers to simulate, enhance and optimize their designs.

This work begins by fully developing and verifying a model for a SOI MOSFET on a physical device simulator. The SOI MOSFET is chosen because of the self heating and low frequency dispersions that it suffers from. These phenomena are very important for other power RF devices. Using a physical device simulator means that no measurement uncertainty can be the origin of any deviation in the model performance. Any deviation is therefore due to the model topology or extraction procedure. The model developed is then applied to Motorola's MRF 181 RF power LDMOSFET.

In this work, presented is a large/small signal, charge conserving, non-quasi-static technique optimized for DC and microwave modeling of MOSFETs using the TPS formulation. Such a model is suitable for simulating self-biasing microwave circuits such as PAs and VCOs, but is not suitable for mixers and other circuits with IF signals below the low frequency dispersion transition. Models generated with and without the use of pulsed IVs are presented for comparison purposes. For SOI MOSFETs, it will be shown that to eliminate low frequency effects, pulsed IVs have to be used. For LDMOSFETs, a technique that totally bypasses pulsed IV and pulsed RF is discussed and implemented.

The developed and verified model is then applied to a real RF silicon power transistor. Instruments under computer control are used to measure DC, temperature, pulsed and microwave device characteristics. This data is used to extract a full electro-thermal model which is then implemented in the ADS microwave circuit simulator

and used to design PAs. Predicted performance matrices, such as compression and IMD, are compared with those measured for the designed amplifier in the Lab.

1.7 Thesis Outline

Chapter 2 contains the theoretical development of the table based empiric MOSFET model for SOI devices. Device characterization and small signal parameter extraction is discussed. This leads to the development of two large signal models generated using TPS–the first is bias depended and would need to be re-extracted for each bias, while the second is self biasing. A completer electro-thermal DC and microwave model is then developed and verified in the MISIM circuit simulator.

Chapter 3 is focused on the device characterization and small signal modeling of LDMOSFETs. Measurement tools under computer control are developed for measuring DC IVT, iso-thermal DC IVs and pulsed IVs. DC thermal characterizations are undertaken to extract the thermal resistance of the device. The iso-thermal DC IV tool is used to measure iso-thermal s-parameters at different device temperatures. This is necessitated due to absence of a pulsed IV, pulsed RF system. Novel techniques for parasitic deembedding are presented. The small signal model is then extracted and the small signal model parameters are compared as a function of device temperature.

Chapter 4 deals with the large signal modeling of the LDMOSFET and implementation of the model in ADS, followed by its verification. The Chapter begins by comparing iso-thermal measurements with hot and cold pulsed measurements. The three resulting transcoductances are also compared. This leads to the development of a distinct temperature dependent large signal models, one bypassing pulsed IVs and pulsed RF. The model is implemented using 3D TPS techniques relying on knot optimization. Model development and implementation on ADS is covered with particular emphasis on the out of bound regions. Harmonics and IMD simulations performed on a power amplifier designed on ADS are then compared with measurements made on the fabricated amplifier. The effect of temperature dependent charge is investigated.

Chapter 5 concludes this thesis and in particular addresses the issues of using the developed model for different devices. Finally, suggestions for future work are presented.

CHAPTER 2

Theoretical SOI MOSFET Model Development and Verification

This Chapter [34] presents the theoretical formation of the table based empiric MOSFET model for SOI devices in a totally simulated environment and prepares the stage for applying the model to a real device.

2.1 Device Characterization

A n-channel, partially depleted SOI MOSFET with gate length of 0.8 μm was simulated on the PISCES 2-D physical device simulator [35]. The device has no body contact, hence the body is floating. PISCES was used to obtain iso-thermal (300K), intrinsic Y-parameter data for the SOI MOSFET at 210 bias points ranging from V_{GS} = 0.5 to 5.0 V (in increments of 0.5 V), V_{DS} = 0 to 4.0 V (in increments of 0.2 V) and 20 frequencies from 1 to 20 GHz (in steps of 1 GHz). These measurements were used

for the high frequency characterization of the device. Additional Y-parameter data was obtained at each of the 210 bias points for 21 frequencies ranging from 1 MHz to 1.001 GHz in steps of 50 MHz. This set of data was used for the low frequency characterization of the device. The intrinsic device studied has a peak unity gain cut-off frequency, f_T, of about 17 GHz and a threshold voltage, V_T, of about 0.65 V.

Three different device 300 K iso-thermal IV characteristics were obtained, as shown in Fig. 2.1. First, a regular DC simulation was performed on PISCES to obtain the drain current, $I_{D,iso}$ (dashed lines with hollow circles). The second set of iso-thermal IV characteristics were also obtained using a regular iso-thermal DC simulation, however the impact ionization electron-hole generation model was turned off (dashed lines with crosses). Lastly, an iso-thermal transient IV, with impact ionization turned on, was obtained using a fixed DC bias point of V_{GS} = 3.0 V and V_{DS} = 2.6 V (solid lines). In this simulation, the voltage was pulsed, in 20 ps, to the bias point (v_{GS}, v_{DS}) where it is desired to obtain the drain current, and held constant for 80 ps. The drain current was then recorded (at time, t = 100 ps). It should be noted that the drain current at the original bias point is exactly equal to that obtained in the first iso-thermal DC IV simulation at the same bias point. All PISCES data are for a device width of 1 μm. From Fig. 2.1, it is clear that impact ionization has a strong effect on the iso-thermal DC IV, particularly at high drain voltages. The iso-thermal transient IV, which are important for microwave simulations, do not feature

the high drain conductance (g_d) that characterizes the regular DC IV (with impact ionization effects turned on) at high drain biases.

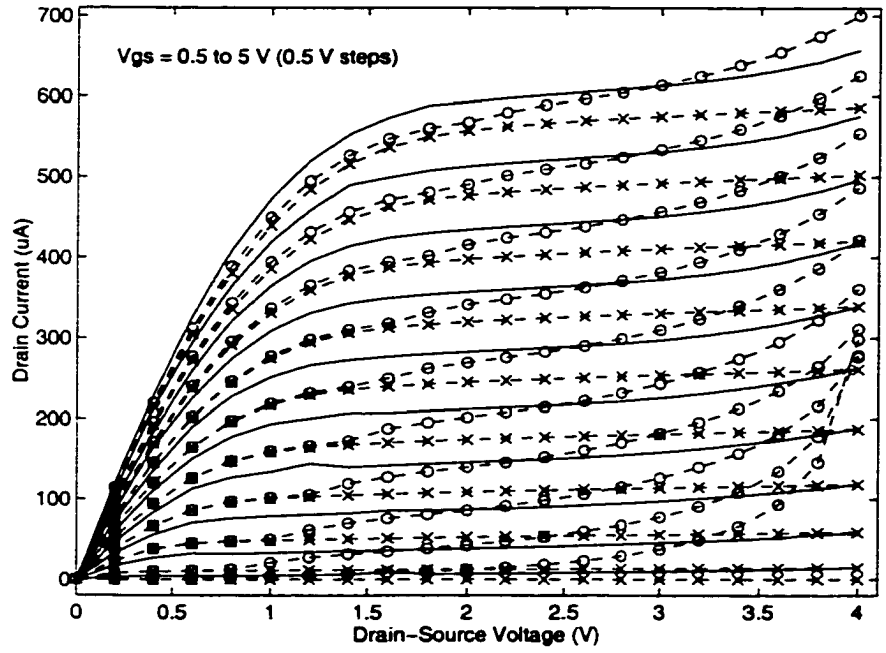


Figure 2.1: The three different device IV curves obtained on PISCES. The dashed lines with hollow circles are the regular DC IV (with impact ionization), the dashed lines with crosses are the DC IV without impact ionization and the solid line is the transient IV with impact ionization. V_{GS} ranges from 0.5V (lowest curve) to 5V (highest curve) in steps of 0.5V

2.2 Small Signal Parameter Extraction

The intrinsic SOI MOSFET Y-parameter data obtained from the 300K iso-thermal PISCES simulations are used to extract a small signal RC equivalent circuit model.

The first order RC circuit topology used is a modified version of that proposed in [15] and is given in Fig. 2.2a.

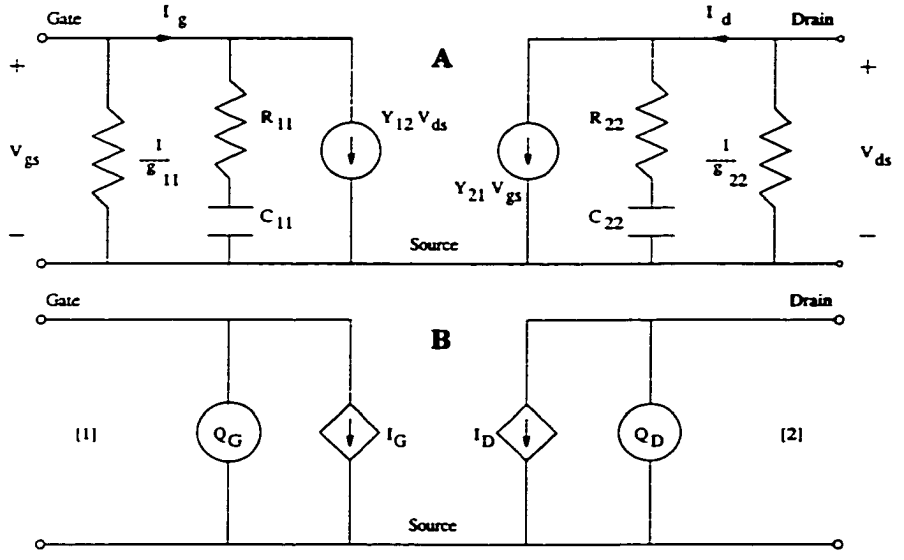


Figure 2.2: The small signal RC equivalent circuit model (A) and Intrinsic large-signal circuit model (B)

The Y-parameters of this circuit can be written as follows:

$$Y_{ij} = g_{ij} + \frac{j\omega C_{ij}}{1 + j\omega\tau_{ij}} \tag{2.1}$$

The Y-parameter equations of the small signal RC circuit (2.1) are fitted to the iso-thermal Y-parameter data obtained from PISCES. A least squares technique is used to fit the iso-thermal Y-parameter data over the high frequency range to extract *AC* g_{ij}, C_{ij} and τ_{ij}, small signal fitting parameters at each bias point.

Fig. 2.3 shows the plots of the fit of the real parts of Y_{21} and Y_{22} for a fixed V_{DS} of 2.6 V and a V_{GS} range from 0.5 to 5 V in steps of 0.5 V. The solid lines represent the least square fitting results, while the plus marks represent the original Y-parameter data obtained from PISCES. It is clear that an excellent fit is obtained. However, at higher drain bias voltages, the quality of the fit does deteriorate somewhat.

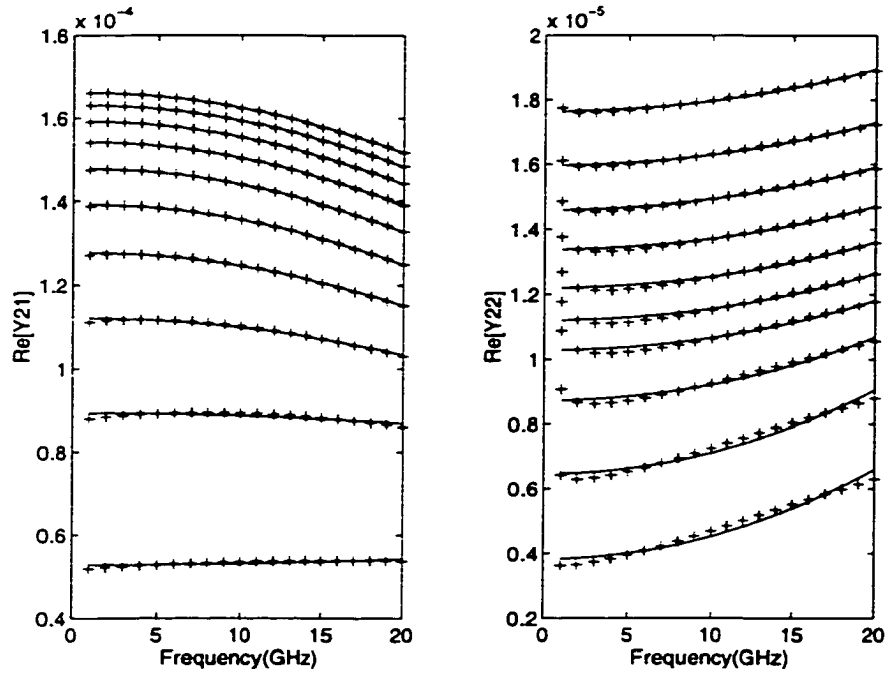


Figure 2.3: Small signal RC fit of the real part of Y for $V_{DS} = 2.6$ and V_{GS} from 0.5 (lowest curve) to 5 V (highest curve) in steps of 0.5 V

As was mentioned in Section II, Y-parameter data was obtained for both a high and low frequency range. By comparing the percentage difference between the DCg_m (defined as the real part of Y_{21} at 1 MHz) and the ACg_m (defined as g_{21} obtained from

the least squares Y_{21} parameter fit over the 1 to 20 GHz high frequency range) for a particular bias point, it is observed that there is considerable low frequency dispersion in the device. The amount of low frequency dispersion is observed to vary greatly with the bias voltage such that there is little or no dispersion in the triode region, while substantial dispersion exists in the saturation region. Larger drain biases lead to greater dispersion. A similar observation is made on comparing DCg_d (real part of Y_{22} at 1 MHz) and ACg_d (g_{22} obtained from the least squares fit of the microwave Y_{22} data).

In general, discrepancies between DCg_m (DCg_d) and ACg_m (ACg_d) are attributed to the presence of traps and self heating effects [15]. However, in the PISCES simulation, no traps are present. Further, the simulations are performed in an iso-thermal environment and hence temperature related effects are not to be expected to alter the results. Larger percentage differences between DCg_m (DCg_d) and ACg_m (ACg_d) are observed at higher drain bias voltages. Impact ionization effects, related to the parasitic NPN bipolar transistor in the SOI MOSFET, are more dominant in the higher drain bias region [17]. Turning off impact ionization effects in PISCES, can have a significant effect on the obtained iso-thermal IV data, as was observed in Fig. 2.1. From Fig. 2.1, it is observed that the IV curves obtained without impact ionization, do not exhibit the kink-effect (Somerville *et. al.* have experimentally shown a direct relationship between impact ionization and the kink effect for InAlAS/InGaAs HEMTs [37]). Further, they do not show a substantial increase in the drain conductance (g_d) at

high drain biases, compared to the regular iso-thermal DC IV with impact ionization effects turned on. It can be concluded that impact ionization effects related to the floating base parasitic NPN bipolar transistor, are a major cause of iso-thermal low frequency dispersions.

From the above results and the discussion in Section I, it can be seen that there are two major constraints that effect SOI MOSFET device modeling in comparison to that of ordinary FETs. The first constraint is the presence of low frequency dispersion effects related to parasitic effects, such as the kink effect and the floating body effect. The second constraint is the presence of low frequency dispersions due to self heating effects.

Low frequency dispersions and self heating effects have been directly modeled as a function of frequency by a number of researchers [18], [38]. However, the added model complexity, the increased computation and parameter extraction requirements and the potential decrease in model accuracy resulting from the requirement of fitting both low and high (microwave) frequency characteristics, is not necessary, when it is only desired to simulate a self-biasing, microwave circuit. Indeed for such microwave circuits the operating device temperature, the traps or parasitic bipolar transistor responsible for the low-frequency dispersion, are physical processes which are too slow to respond directly to the microwave signals and hence the only concern is with their contribution to the DC operating point under large-signal microwave drive [39].

The initial approach (Chapter 2.3.1) is therefore tailored around a fixed bias point at which the device is to be operated and which initially sets the device temperature, T_{dev}, given a substrate temperature, T_{sub}. The argument then is that the circuit will be switching at high enough speeds, that for the most part, it exceeds the time constants of the major parasitic bipolar effects and thermal effects (the thermal time constant of the device is about 1 μs, Le Neel and Haond reported a time constant of 4.8 μs for the self-heating [40]). Thus the temperature in the device does not have time to respond to the changes in currents and voltages and the operation is iso-thermal. However under large-signal microwave operation, both the operating point and the iso-thermal device temperature, of the FET can depart from the iso-thermal device temperature and operating point established by the biasing circuit under small-signal microwave drive. The modeling will therefor be initiated by assuming that the operating point and the iso-thermal temperature are known. The FET model topology will then be subsequently extended to automatically calculate the operating point and the iso-thermal temperature (Chapter 2.3.2 and 2.5 respectively).

2.3 Large-Signal Model Generation Using B-splines

2.3.1 Iso-Thermal Transient I-V (Bias-Dependent) Microwave Model

As stated in the previous section, developed first is a large-signal microwave model assuming that the bias point (DC currents and voltages) and the temperature, T_{dev}, of the FET are known given a substrate temperature, T_{sub}. Fig. 2.2b shows the intrinsic large-signal model used for this purpose [15], [9].

The iso-thermal IV characteristics, $I_{D,trans}(v_{GS}, v_{DS}, V_{GS}, V_{DS}, T_{dev})$, used by this microwave model should conform with the transient IV measurements made on PISCES, Fig. 2.1, by pulsing the gate and drain voltages, v_{GS} and v_{DS}, to various values, starting from the DC biasing point (Fig. 2.1 uses $V_{GS} = 3.0$ V, $V_{DS} = 2.6$ V, $T_{dev} =$ 300K). In this case, the drain current, $I_{D,trans}$, is measured after the non-quasi-static relaxation (several τ_{ij}) and before low frequency effects, including self heating effects, have had time to settle.

The measurement of such a microwave transient IV might be difficult to perform accurately in practice. Therefore it is desired to directly recover the large-signal model of the SOI MOSFET from the conductances and capacitances extracted by fitting Y-parameter equations (2.1) to the iso-thermal Y-parameters measured.

The large-signal model can then be obtained by using the following relationships between small signal and large-signal model parameters [15], [9]:

$$
\begin{aligned}
&I_{G,trans}(v_{GS}, v_{DS}, V_{GS}, V_{DS}, T_{dev}) = \int g_{11}(V_{GS}, V_{DS}, T_{dev})dV_{GS} + \\
&\int g_{12}(V_{GS}, V_{DS}, T_{dev})dV_{DS} \\
&I_{D,trans}(v_{GS}, v_{DS}, V_{GS}, V_{DS}, T_{dev}) = \int g_{21}(V_{GS}, V_{DS}, T_{dev})dV_{GS} + \\
&\int g_{22}(V_{GS}, V_{DS}, T_{dev})dV_{DS} \\
&\text{with} \quad I_{D,trans}(V_{GS}, V_{DS}, V_{GS}, V_{DS}, T_{dev}) \simeq I_D(V_{GS}, V_{DS}, T_{sub}) \\
&Q_G(v_{GS}, v_{DS}, T_{dev}) = \int C_{11}(V_{GS}, V_{DS}, T_{dev})dV_{GS} + \int C_{12}(V_{GS}, V_{DS}, T_{dev})dV_{DS} \\
&Q_D(v_{GS}, v_{DS}, T_{dev}) = \int C_{21}(V_{GS}, V_{DS}, T_{dev})dV_{GS} + \int C_{22}(V_{GS}, V_{DS}, T_{dev})dV_{DS}
\end{aligned}
\tag{2.2}
$$

Note that this model neglects the possible DC bias dependence (V_{GS}, V_{DS}) of the isothermal gate charge Q_G and drain charge Q_D. Also neglected is the dependence of $I_{D,trans}$ on the internal body to source voltage, V_{BS}. The accuracy of this approximation will be verified below. Also in the SOI-MOSFET, I_G can be taken as zero, unlike in other FETs such as MESFETs and HEMTs.

The total non-quasi-static current flowing through the charge elements Q_G or Q_D of Fig. 2.2b are written as (using i for G or D):

$$
i_{disp,i}(t) = \frac{dQ_i(v_{GS}, v_{DS}, T_{dev})}{dt} - \frac{d}{dt}\left[\tau_i(v_{GS}, v_{DS}, T_{dev}) i_{disp,i}\right] \tag{2.3}
$$

where τ_i is the non-quasi-static charge redistribution time associated with the particular charge element, Q_i [15]. The non-quasi-static corrections introduce by τ_i become important at operation frequencies above f_t. Note however that only two τ's are used

instead of the four extracted in the previous Section as it is desired to implement a charge model (see [15]). In the next Section, it will be verified that the resulting degradation of the small-signal scattering parameters is acceptable.

The total gate and drain currents can then be written as:

$$\begin{aligned} i_G(t) &= I_{G,trans}(t) + i_{disp,G}(t) \\ i_D(t) &= I_{D,trans}(t) + i_{disp,D}(t) \end{aligned} \tag{2.4}$$

In order to extract the large-signal model parameters, the small signal parameter data (AC g and C) need to be fitted over the entire bias range and integrated as given in (2.2). The Tensor Product Spline (TPS) method is used to accomplish this task [10], [9]. TPS can be used to represent a bi-variate function as follows [41]:

$$S(V_{GS}, V_{DS}) = \sum_{i=1}^{m}\sum_{j=1}^{n} a_{ij} \; B_{i,k_{V_{GS}},t_{V_{GS}}}(V_{GS}) B_{j,k_{V_{DS}},t_{V_{DS}}}(V_{DS}) \tag{2.5}$$

where $k_{V_{GS}}$ and $k_{V_{DS}}$ are the B-spline orders in the V_{GS} and V_{DS} directions, respectively. $t_{V_{GS}}$ and $t_{V_{DS}}$ are the knot sequences in the V_{GS} and V_{DS} directions, respectively. $B_{i,k_{V_{GS}},t_{V_{GS}}}$ and $B_{j,k_{V_{DS}},t_{V_{DS}}}$ are one-dimensional B-spline polynomial functions, and a_{ij} are the TPS coefficients that need to be determined.

Storage requirements for the TPS method are very reasonable, since for $m = 20$ and $n = 20$, only 400 a_{ij} coefficients are required. For $k_{VG} = 4$ and $k_{VD} = 4$, only 16 coefficients are required to compute functional and derivative values at any

particular bias point, due to the variation diminishing property of B-splines. Hence computation proceeds rapidly. By using B-splines of order 4, second order continuity is guaranteed. Also, mixed derivatives match, ensuring that the TPS method will be charge conserving. The TPS method has been used in a least squares approach to extract the a_{ij} coefficients from small signal gradient data. Using the least squares technique leads to a unique solution.

The drain current of the device can be extracted from the integration of ACg_m (ACg_{21}) and ACg_d (ACg_{22}) using the TPS method. Additionally, a forcing condition is desired to ensure that the DC drain current at the original bias point, (V_{GS} = 3.0 V, V_{DS} = 2.6 V, T = bias point temperature), agrees closely with that obtained from DC (and hence transient IV) simulations at the same bias point (2.2) [42]. Fig. 2.4 is a plot of the obtained drain current. The dashed lines represent the recovered drain current, while the circles represent the drain current of the SOI MOSFET obtained from PISCES transient IV measurements.

From Fig. 2.4, it can be seen that the fit is very good. Clearly, the integration has yielded the iso-thermal transient IV ($I_{D,trans}$) and not the iso-thermal DC IV. This result justifies neglecting the dependence of $I_{D,trans}$ on the internal body to source voltage, V_{BS} (see Appendix A). Fig. 2.5 is a plot of the fitted ACg_m. The solid lines represent the fitting results while the circles represent the ACg_m values obtained from the least square small signal fit of the high frequency Y_{21} parameters performed in

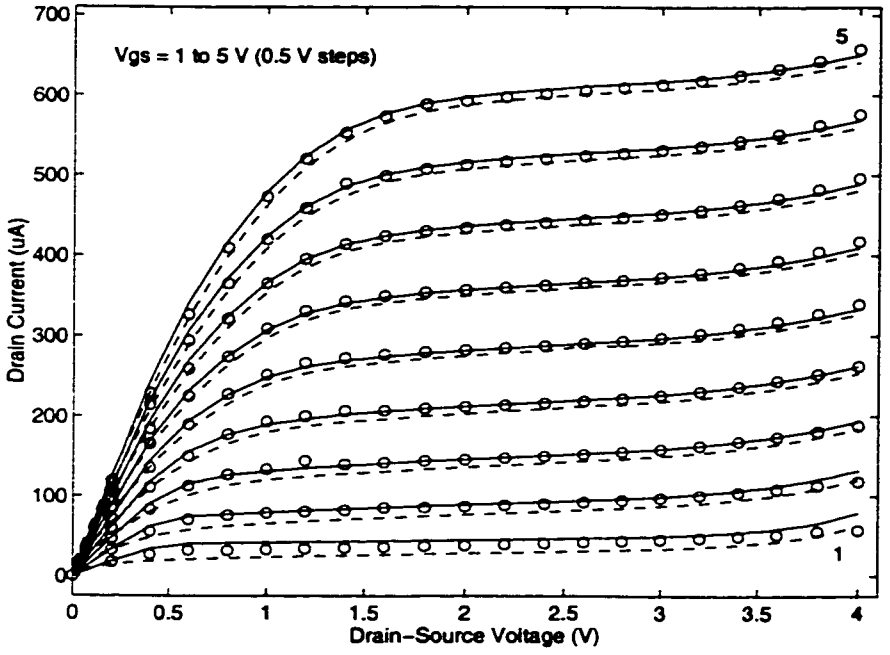


Figure 2.4: Transient IV recovered from ACg_m and ACg_d integration and bias point force (dashed lines), transient IV characteristics generated by the self-biasing microwave model (solid lines), and transient IV measured in PISCES (for $V_{GS} = 3.0$ V and $V_{DS} = 2.6$ V) (circles). V_{GS} ranges from 1V (lowest curve) to 5V (highest curve) in steps of 0.5V

Section III. It can be seen that the quality of the fit is excellent. A similar excellent fit is obtained for the ACg_d.

The iso-thermal gate charge, Q_G, is extracted by fitting C_{11} and C_{12} to the derivatives of the B-splines and is plotted in Fig. 2.6a. For comparison, the gate charge obtained from PISCES measurements is given in Fig. 2.6b. Excellent agreement is observed between the recovered and measured gate charge. Likewise, the drain charge, Q_D is extracted by fitting C_{21} and C_{22} to the derivatives of the B-splines.

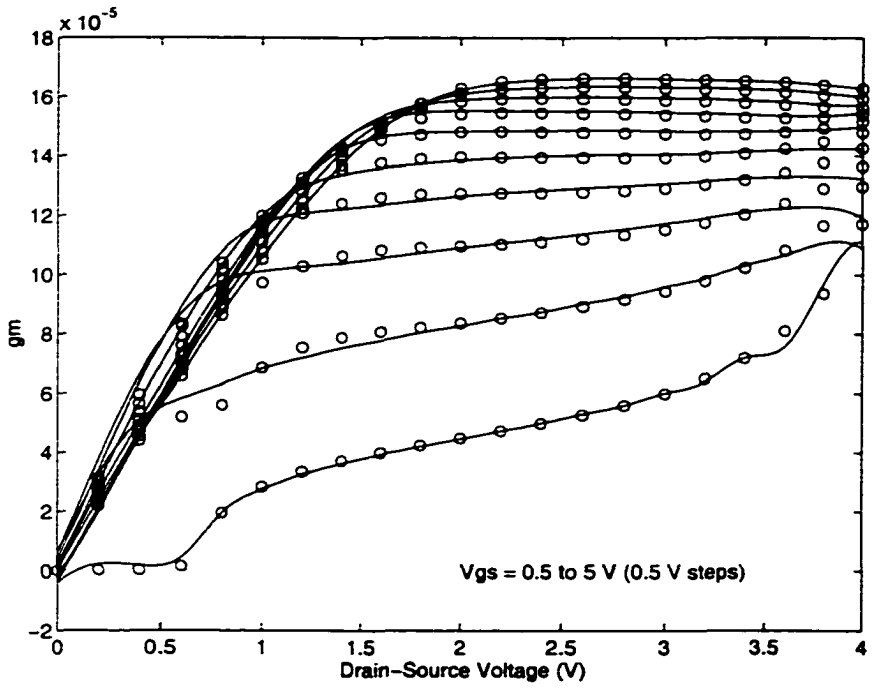
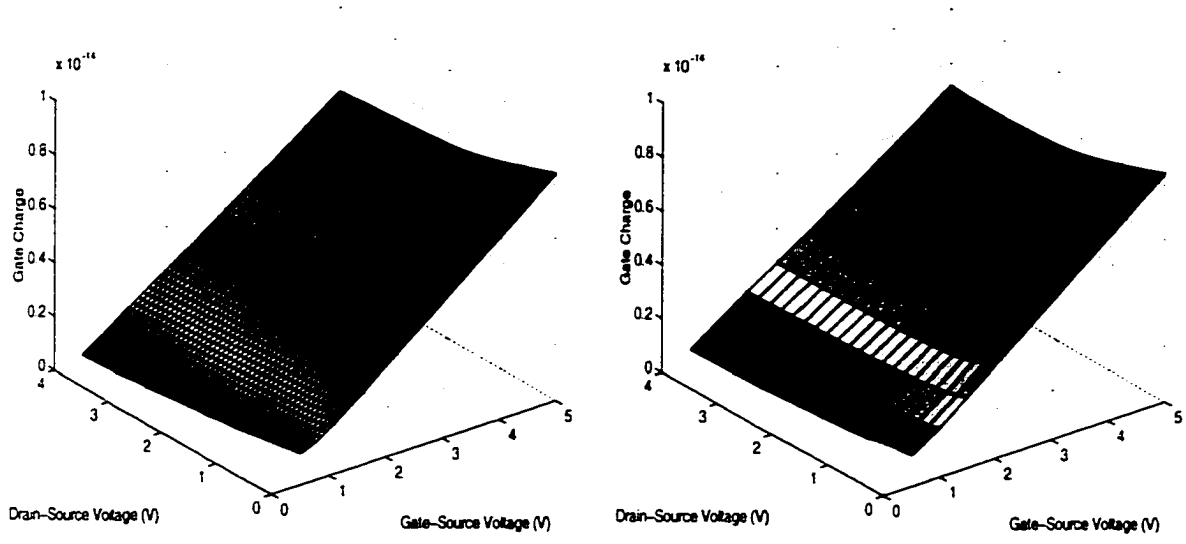


Figure 2.5: Comparison of ACg_m obtained from TPS (solid lines), with those obtained from the small signal RC fit (data points). V_{GS} ranges from 1V (lowest curve) to 5V (highest curve) in steps of 0.5V

The non-quasi-static time constants, τ_{11-22}, are fitted using TPS in order to provide interpolation between data points.

2.3.2 Self-Biasing Iso-Thermal Microwave Model

The major limiting factor of the large-signal model presented above is that it assumes that the device operating point (DC voltage, current and temperature) is known and fixed. This constraint is very undesirable since the device operating point



(a) (b)

Figure 2.6: Comparison of gate charge obtained from TPS (a) and PISCES (b)

is not always known. This is the case for circuits that are self-biasing, such as oscillators and amplifiers which operate with large-signal microwave excitations. Also if the operating point is changed, the transient IV characteristic must be regenerated by using the TPS extraction method; a task one would rather avoid in a circuit simulator.

Here, presented is an enhanced microwave model topology that automatically fits both the DC and microwave characteristics of the device and therefore allows for self-biasing. Other approaches using a filter [43] or two partial FETs [44] have been reported. This approach is based upon a physical topology combining a FET model

with a parasitic bipolar transistor [45] with a floating base driven by the impact ionization current. The parasitic bipolar transistor present in the SOI MOSFET, which introduces low-frequency dispersions, performs therefore the seem-less integration between the iso-thermal DC IV characteristics, $I_{D,iso}(v_{GS}, v_{DS}, T_{dev})$, and the high frequency (above the low frequency dispersion transition frequency) IV characteristics, $I_{D,RF}(v_{GS}, v_{DS}, T_{dev})$ (defined latter). This model in effect automatically generates the appropriate transient IV characteristics, $I_{D,trans}(v_{GS}, v_{DS}, V_{GS}, V_{DS}, T_{dev})$, from $I_{D,iso}(v_{GS}, v_{DS}, T_{dev})$ and $I_{D,RF}(v_{GS}, v_{DS}, T_{dev})$ for any bias V_{GS}, V_{DS}.

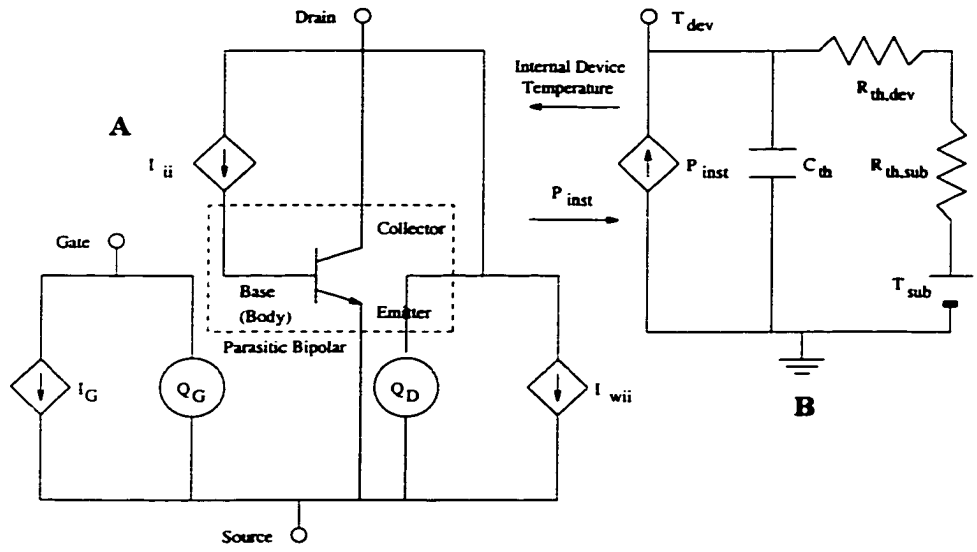


Figure 2.7: Self-biasing model topology to fit both DC and RF (A) and Electrical network representing the thermal network model for the thermal boundary conditions used in PISCES (B)

The model topology is shown in Fig. 2.7a, where I_{wii} is the FET channel current without impact ionization effects, and where I_{ii}, the current due to impact ionization effects, drives the parasitic bipolar transistor, which has a current gain factor of α.

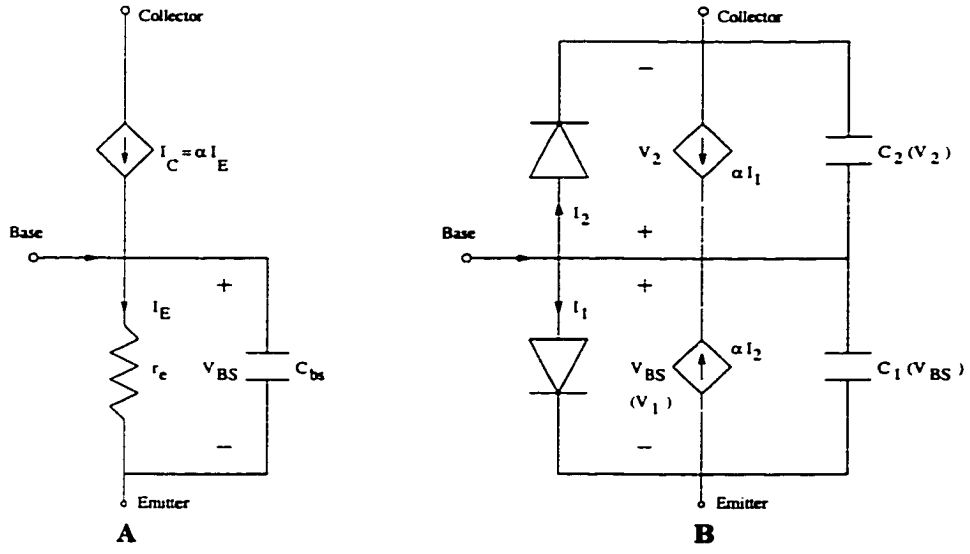


Figure 2.8: Parasitic bipolar model topologies. Model A is a simple model not valid in cut-off while Model B is valid in entire bias range

Model topologies for the internal parasitic bipolar transistor are presented in Fig. 2.8. For a wide range of drain to source voltages, the internal BJT operates in the active mode, for which model A in Fig. 2.8 can be used to represent the BJT. The collector current is given by the simple relation $I_C = \alpha I_E$, with α the current gain of the parasitic bipolar transistor.

At DC, the capacitor C_{bs} is an open and the total iso-thermal DC drain current is given by:

$$I_{D,iso} = I_{wii} + \frac{I_{ii}}{1-\alpha} \tag{2.6}$$

At microwave frequencies, the capacitor C_{bs} shorts the AC component of the current I_{ii} and the parasitic bipolar transistor cannot respond to the time variation of I_{ii}. At microwave frequencies, the iso-thermal RF IV (defined in Section IV B) is therefore given by:

$$I_{D,RF} = I_{wii} + I_{ii} \tag{2.7}$$

Inverting the relationships above permits us to express I_{wii} and I_{ii} in terms of $I_{D,iso}(v_{GS}, v_{DS}, T_{dev})$ and $I_{D,RF}(v_{GS}, v_{DS}, T_{dev})$:

$$I_{wii}(v_{GS}, v_{DS}, T_{dev}) = \frac{1}{\alpha}\left[I_{D,RF}(v_{GS}, v_{DS}, T_{dev} - I_{D,iso}(v_{GS}, v_{DS}, T_{dev})\right] + I_{D,iso}(v_{GS}, v_{DS}, T_{dev}) \tag{2.8}$$

$$I_{ii}(v_{GS}, v_{DS}, T_{dev}) = \frac{1-\alpha}{\alpha}\left[I_{D,is}(v_{GS}, v_{DS}, T_{dev}) - I_{D,RF}(v_{GS}, v_{DS}, T_{dev})\right] \tag{2.9}$$

Since C_{bs} is large, it will hold its DC operating point voltage (V_{BS}) for short (less than the RC time constant of $r_e C_{bs}$) transient simulations. The transient IV associated with this model can then be written as:

$$I_{D,trans}(v_{GS}, v_{DS}, V_{GS}, V_{DS}, T_{dev}) = I_{wii}(v_{GS}, v_{DS}, T_{dev}) + I_{ii}(v_{GS}, v_{DS}, T_{dev}) + \frac{\alpha}{1-\alpha} I_{ii}(V_{GS}, V_{DS}, T_{dev}) \tag{2.10}$$

where V_{GS}, V_{DS} and T_{dev} are the DC bias point around which the transient IV is generated.

From (2.10), it is clear that $I_{D,trans}(v_{GS} = 0, v_{DS} = 0, V_{GS}, V_{DS}, T_{dev})$ is not zero, although this is what is measured from PISCES (Fig. 2.1) [44]. The reason for this is that model A does not hold when the parasitic BJT goes into cut-off ($v_{DS} < 0.5$ V).

In order to correct for this small deviation for V_{DS} below 0.5 V, we must use a more general model that holds for the entire bias range. In model B in Fig. 2.8, the diodes represent typical DC diode IV characteristics ($I_i = I_s(\exp(qV_i/kT) - 1)$, for i = 1 and 2). The two dependent current sources are αI_1 and αI_2 respectively. Care must be placed to select α and I_s such that $I_1(V_{BS}) = \frac{1}{1-\alpha} I_{ii}(V_{GS}, V_{DS}, T_{dev})$ yields $V_{BS} < V_{DS}$, which guarantees that when the BJT operates in the active mode, the model reduces to model A. Resistors can be introduced in series with the diode to achieve a smoother relaxation to zero for $v_{GS} = v_{DS} = 0$. The capacitors are voltage dependent ($Q_i = \tau I_i$ and $C_i = dQ_i/dV_i$, for $i = 1$ and 2) such that when they are reversed biased, their values are much smaller than in forward bias, thus allowing for model B to relax to model A.

The expressions for I_{wii} and I_{ii} then remain the same as those for model A. The transient IV for this model can be obtained from:

$$I_{D,trans}(v_{GS}, v_{DS}, V_{GS}, V_{DS}, T_{dev}) = I_{wii}(v_{GS}, v_{DS}, T_{dev}) + I_{ii}(v_{GS}, v_{DS}, T_{dev}) - \frac{C_2(v_{BS}-v_{DS})}{C_1(v_{BS})+C_2(v_{BS}-v_{DS})}[I_{ii}(v_{GS}, v_{DS}, T_{dev}) + (\alpha-1)I_1(v_{BS}) + (\alpha-1)I_2(v_{BS}-v_{DS})] + \alpha I_1(v_{BS}) - I_2(v_{BS}-v_{DS}) \quad (2.11)$$

using $Q_1(V_{BS}) + Q_2(V_{BS} - V_{DS}) = Q_1(v_{BS}) + Q_2(v_{BS} - v_{DS})$.

For $v_{GS} = v_{DS} = 0$, $I_2(v_{BS}) = I_1(v_{BS})$ and $C_1(v_{BS}) = C_2(v_{BS})$. Hence the model symmetry will ensure that $I_{D,trans}(v_{GS} = 0, v_{DS} = 0, V_{GS}, V_{DS}, T_{dev})$ is zero.

$I_{D,iso}$, is obtained from direct iso-thermal PISCES simulations, where $I_{D,RF}$ is obtained by fitting the extracted iso-thermal ACg_m and AC_{gd}. An additional constraint on $I_{D,RF}$ is that it equals $I_{D,iso}$ until the kink effect kicks in, after which, its slope follows the ACg_m and AC_{gd}. $I_{D,RF}$ is fitted using TPS and is given by the solid lines in Fig. 2.9. For comparison purposes, the TPS fitted $I_{D,iso}$ (dashed lines) is superimposed on Fig. 2.9, where the circles are iso-thermal DC data from PISCES.

2.4 Model Incorporation and Verification in MISIM

In order to verify the accuracy and versatility of the iso-thermal model, it has been incorporated in the MISIM (Model Independent SIMulator) circuit simulator [46], [47]. MISIM is a SPICE compatible circuit simulator designed so as to allow

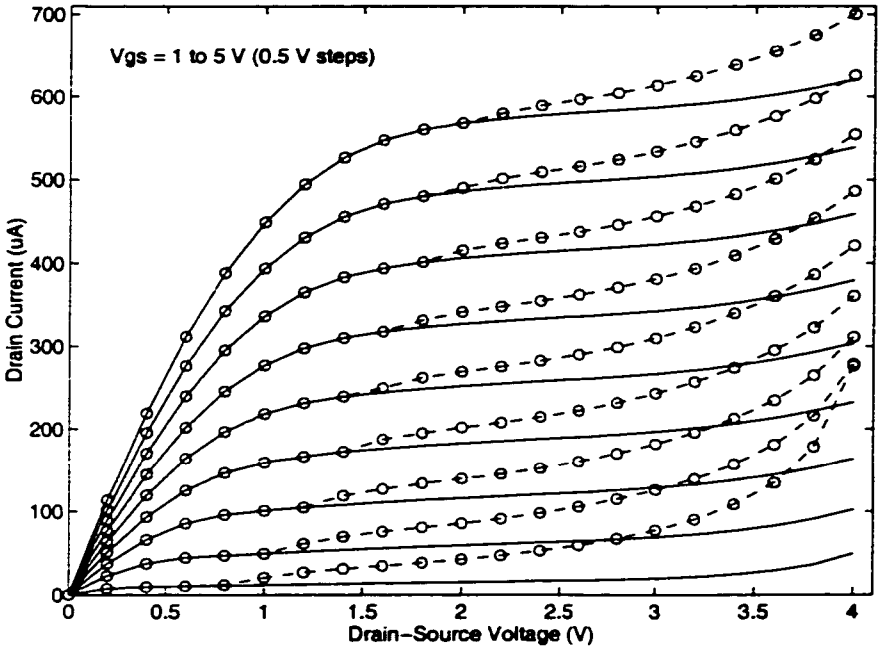


Figure 2.9: The fitted RF (solid lines) and DC (dashed dashed) IV characteristics. The circles are DC data from PISCES. V_{GS} ranges from 1V (lowest curve) to 5V (highest curve) in steps of 0.5V

easy incorporation of complex user defined models. Since it possess a harmonic balance simulator, it is an excellent choice for microwave circuit design and simulation. Available on MISIM is a non-quasi-static charge element, which is necessary for a complete description of the SOI MOSFET model.

The self-biasing large-signal model of Section IV B (Fig. 2.7) together with model B of Appendix A (Fig. 2.8), is implemented on MISIM using an α value of 0.9. Associated with the two charge elements is a characteristic charge redistribution time, τ. The small signal extraction technique led to 4 time constants (τ_{ij}), τ_{11-22}. However, the large-signal model topology can only handle two.τ_{11} is chosen for the gate charge

and τ_{21} for the drain charge. This will cause a degradation in the fit of Y_{12} and Y_{22}, and in the process will effect all four scattering parameters.

The resulting errors in the S-parameter fit have been computed to be largest for S_{21}; 0.0258 for the four tau model and 0.0364 for the two tau model. The unilateral power gain error changes from 0.728 dB for the four tau model to 3.347 dB for the two tau model, while the error in the current gain remains at 0.16 dB. All errors are computed over the entire frequency and bias range [48]. The bulk of the error incurred when going from four tau's to two tau's is at higher frequencies, since it is at these frequencies that accurate modeling of the non-quasi-static time constants is critical. This is illustrated by plotting in Fig. 2.10 the S-parameter fits for a 200 μm device at $V_{GS} = 2.5$ V and $V_{DS} = 2.0$ V, where the plus marks represent PISCES obtained S-parameter data, the solid lines are the four tau fit and the dashed lines are the two tau fit.

A number of tests are carried out in order to validate the model. First, a transient IV simulation (as defined in Section II) using a fixed DC bias point of $V_{GS} = 3$ V and $V_{DS} = 2.6$ V is performed. In Fig. 2.4, the simulated transient IV obtained is represented by solid lines, while that measured on PISCES is given by circles. The two results compare very well, however, there are some small deviations that are primarily caused by the neglected dependence of the transient IV on V_{BS}. A better fit of the bipolar model could help achieve even better results.

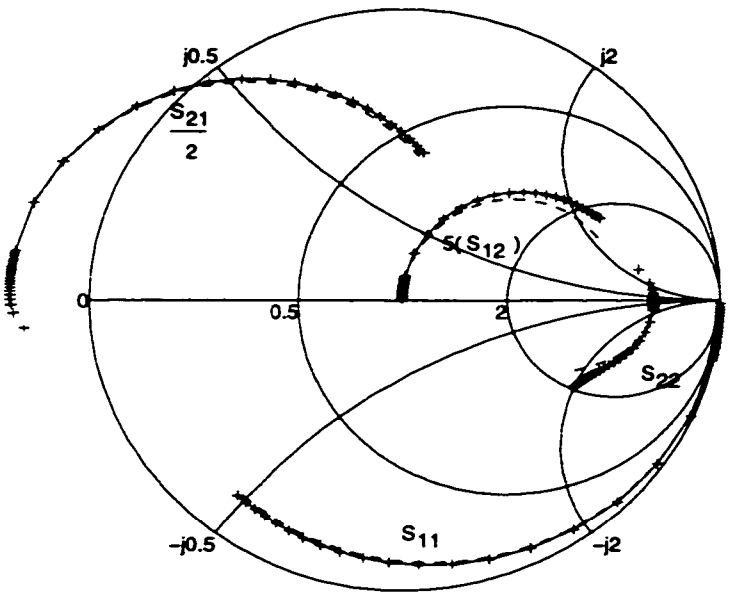


Figure 2.10: Comparison of the four tau and two tau fits at $V_{GS} = 2.5$ V and $V_{DS} = 2.0$ V. The plus marks represent PISCES measured S-parameter data, the solid lines are the four tau fit and the dashed lines are the two tau fit

Next, a large-signal, 10 GHz sinusoidal voltage pulse is applied on the gate of a 1 μm gate width DC biased cold (300 K) SOI MOSFET, with realistic parasitic resistances ($R_d = R_s = 570\Omega/W_g$, and $R_g = 333\Omega/W_g$) on the contacts of the device and a load resistance, R_l, of $3.2517K\Omega$. A large-signal transient simulation is performed on MISIM. The gate, source and drain currents obtained are given in Fig. 2.11 (dashed lines). Processor time on a Sun SPARC 2 for the entire simulation of the circuit (DC and five cycles of large signal time domain) was less than 10 seconds. A similar, iso-thermal, simulation is carried out on PISCES/MIXEDMODE. The currents obtained are plotted in Fig. 2.11 (solid lines). Processor time on the HP

Apollo Model 715/75 for simulating the circuit was over 6 hours. It is clear that the two simulations compare very well.

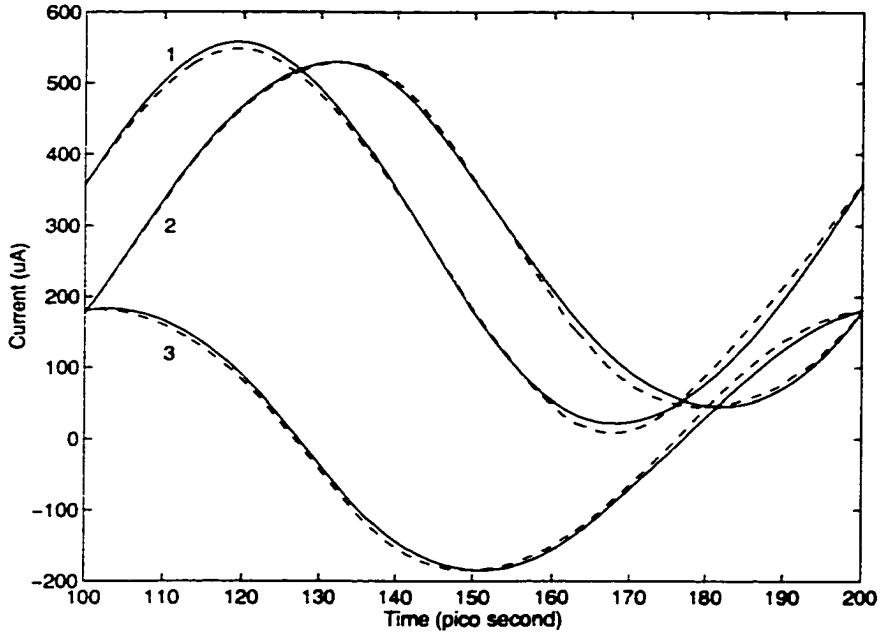


Figure 2.11: Transient simulation on MISIM (dashed lines) versus PISCES (solid lines). 1 denotes the source currents, 2 denotes the drain currents and 3 denotes the gate currents

Finally, a power amplifier is simulated using a 200 μm device biased for class A operation at a fundamental frequency of 2 GHz. A matching circuit is used to conjugately match the 50 Ω output load to the output impedance of the amplifier. The parasitics resistances used are $R_s = R_d = 2.85\Omega$ and $R_g = 1.665\Omega$. The MISIM and PISCES simulation are started with a cold FET at 300 K biased at approximately $V_{GS} = 3.0$ V and $V_{DS} = 2.4$ V. MISIM predictions (solid lines) of the amplifier power

characteristics are compared with those obtained from PISCES (dashed lines) in Figs. 2.12-2.14 [49].

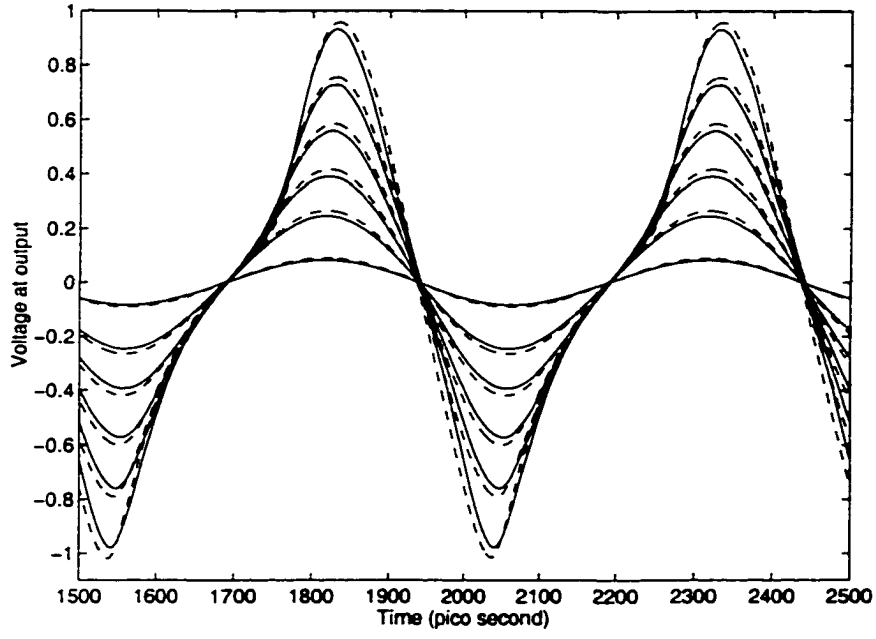


Figure 2.12: Output voltage across 50 Ω load resistance for input power levels from around -15dBm (smallest amplitude) to around 8dBm (largest amplitude) on MISIM (solid lines) versus PISCES (dashed lines)

Fig 2.12 compares the output voltage across the 50 Ω load resistance for various input power levels P_{in}(dBm) obtained with MISIM (solid lines) and PISCES (dashed lines). Fig 2.13 compares the output power and power gain (right axis) and power-added efficiency (left axis) for various input power levels P_{in}(dBm) obtained with MISIM (solid lines) and PISCES (dashed lines with circles). Fig 2.14 compares the first three output power harmonics for various input power levels P_{in}(dBm) obtained with MISIM (solid lines) and PISCES (dashed lines with circles).

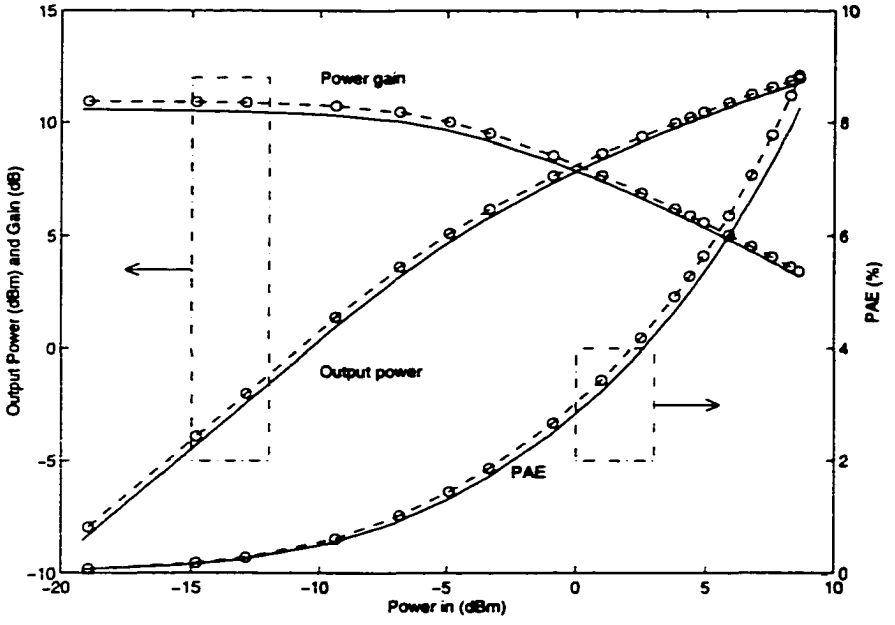


Figure 2.13: Output power and power gain (right axis) and power-added efficiency (left axis) on MISIM (solid lines) versus PISCES (dashed lines)

It is clear from Figs. 2.12-2.14 that the self-biasing microwave model is able to predict the non-linear power characteristics of the amplifier fairly well. In Fig. 2.14, for input power levels greater than the dashed vertical line, the range of the model is exceeded. In this region, the model uses linear extrapolation, which leads to a graceful degradation in the model predictions. The range of the model can be increased, provided additional data is obtained from PISCES.

In the simulations described above the self-biasing model automatically calculates the starting DC operating point. Note that this same model will also automatically calculate the change of the operating point which arises under large-signal operation

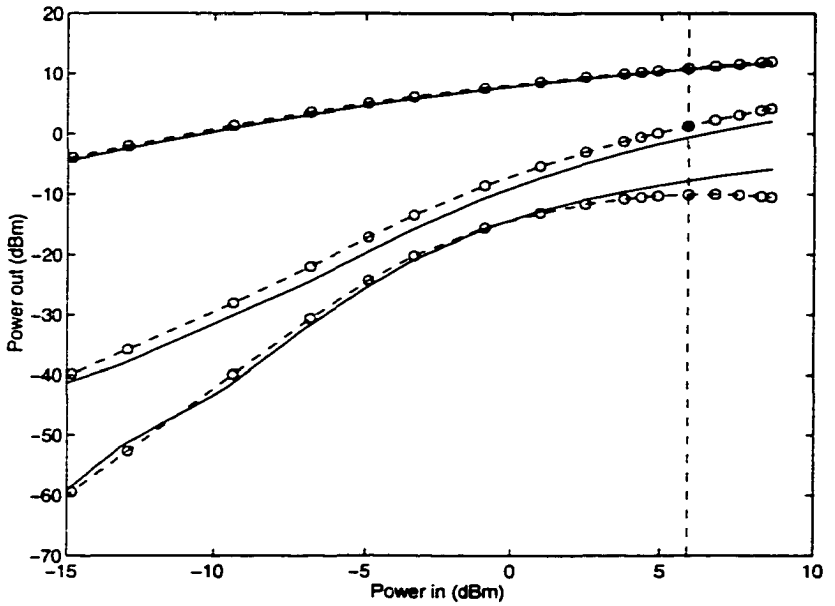


Figure 2.14: First three output power harmonics on MISIM (solid lines) versus PISCES (dashed lines). Model range is limited to input power levels less than dashed vertical line. The fundamental is the uppermost curve, the second harmonic is the middle curve and the third harmonic is the lowest curve

from the non-linear characteristics of the FET. Due to the long time constant of the bipolar transistor (on the order of 100 μs) the steady-state operation under large-signal excitation is best analyzed using harmonic balance simulations. For 8.6 dBm RF input power, the average $v_{DS}(t)$ is found using harmonic balance to increase by about 2% from its DC value V_{DS}, while the average drain current decreases by about 2% from its DC value.

2.5 Complete Electro-Thermal DC and Microwave Model

In the large-signal model presented above it was assumed that the temperature of operation of the device, T_{dev}, was known. This was indeed the case in the test simulations of the previous section which considered an initially cold (300 K) device for which the substrate temperature and the device operating temperature were equal and known ($T_{sub} = T_{dev} = 300$ K). This approach is also well suited for SOI-MOSFETs realized with a high-thermal conductivity oxide for which no self-heating is expected. However, in the SiO_2 SOI-MOSFET, after a time larger than the thermal or parasitic bipolar time constants, the device will warm-up depending on the power dissipated by the FET. The consequence of an increased temperature on the SOI-MOSFET IV characteristics, I_D, compared to an iso-thermal IV, $I_{D,iso}$, is to decrease the drain current (due to a decrease in mobility), except in the breakdown region where the current increases for higher drain voltage (due to increased impact ionization). Presented in this Section is an electro-thermal extension to the microwave model which calculates the correct DC operation point, internal device temperature and associated transient IV.

Fig. 2.7b shows a simple thermal network topology (compatible for the thermal boundary condition described below) which calculates the steady state iso-thermal

temperature of the FET as a function of the power dissipated by the FET. Based on this thermal topology, the thermal response is given by:

$$P_{inst}(t) = C_{th}\frac{dT_{dev}(t)}{dt} + \frac{T_{dev}(t) - T_{sub}}{R_{th,dev}(T_{sub}) + R_{th,sub}} = v_{DS}(t)i_D(t) + v_{GS}(t)i_G(t) \quad (2.12)$$

where $P_{inst}(t)$ is the instantaneous device power dissipated by the FET, $R_{th,dev}(T_{sub})$ the device thermal resistance, $R_{th,sub}(T_{sub})$ the substrate thermal resistance, and C_{th} the device thermal capacitance. Note that the contribution of the thermal capacitance is to average the instantaneous power dissipation in the FET. It has been verified using transient PISCES/GIGA thermal simulations that the thermal constant, $R_{th,dev}C_{th}$, of the simulated FET is on the order of 1 μs. T_{dev} calculated by the thermal model is then used in $I_{D,iso}$ to predict the non iso-thermal drain current, I_D, using the simple equation:

$$I_D(V_{GS}, V_{DS}, T_{sub}) = I_{D,iso}(V_{GS}, V_{DS}, T_{dev}) \quad (2.13)$$

Presented next is the extraction of the thermal resistance and the verification of the electro-thermal model. The dashed lines in Fig. 2.15 show the steady-state maximum device temperature, $T_{dev,MAX}$, in the FET as a function of V_{GS} and V_{DS}, for a T_{sub} of 300 K and infinite thermal resistance at the drain, source and gate and zero substrate thermal resistance. These curves are obtained by using PISCES with the GIGA thermal simulator turned on. $T_{dev,MAX}$ varies from 300 K to around 550 K. Note that the maximum device temperature obtained from PISCES/GIGA gives a good estimate of the average temperature in the channel.

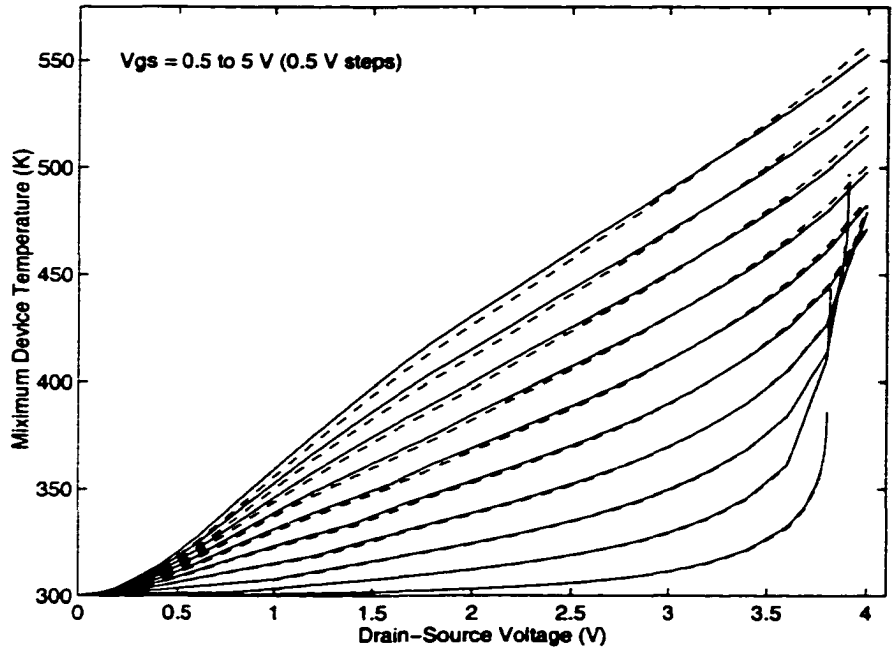


Figure 2.15: Maximum device temperature obtained from PISCES/GIGA (dashed lines) compared with that predicted from $R_{th,dev}$ (solid lines)

Under such thermal boundary conditions, the self-heating present in the device can be very large, as is manifested from Fig. 2.15. For the SOI MOSFET, the maximum device temperature is verified to be linearly related to the average power dissipated in the device ($T_{dev,MAX} = R_{th,dev}Power_{AVG}$), where $R_{th,dev}$ is to a high accuracy independent of the biasing condition. The thermal resistances of the SOI MOSFET is found to be 137.03°C/mW for a 1 μm gate width. Using this single value, the device temperature can be computed over the entire bias range, as is given by the solid lines in Fig. 2.15. Clearly, $R_{th,dev}$ is able to predict very well the maximum device temperature over the bias range.

Let us verify that the device temperature computed by the thermal circuit gives an excellent prediction of the average device temperature ($T_{dev} = T_{dev,MAX}$). Curve 1 in Fig. 2.16 shows the DC IV, I_D, obtained with GIGA on (non iso-thermal) for a fixed T_{sub} of 300 K and $V_{GS} = 3$ V. From Fig. 2.15 it can be seen that for $V_{GS} = 3$ V and V_{DS} varying from 0 to 4 V, $T_{dev,MAX}$ varies from T_{sub} (300 K) to around 485 K. Curve 2 is an iso-thermal IV (GIGA off), $I_{D,iso}$, for $V_{GS} = 3$ V and a fixed device temperature, T_{dev}, of 385 K. The point of intersection of curves 1 and 2 represents the effective device temperature of operation, $T_{dev}(V_{GS}, V_{DS}, T_{sub})$, which is a function of the DC bias and substrate temperature. At the point of intersection, ($V_{GS} = 3$ V, $V_{DS} = 2.442$ V), $T_{dev,MAX}$ for the non iso-thermal DC IV must be 385 K. Indeed, this is confirmed from Fig. 2.15, where $T_{dev,MAX}(3, 2.442, 300) = 385.28$ K. This demonstrates that the electro-thermal model is able to predict the correct device temperature.

The ability of the self-biasing electro-thermal model to predict transient IV behavior is verified by using it to obtain $I_{D,trans}(v_{GS} = 3, v_{DS}, V_{GS} = 3, V_{DS} = 2.442, T_{dev} = 385)$. For this calculation, $I_{D,iso}$ is represented by curve 2 while $I_{D,RF}$ is given by curve 3 in Fig. 2.16. $I_{D,RF}$ for this computation is defined as the transient IV around $V_{GS} = 3$ V and $V_{DS} = 1.5$ V (biased below kink) for a fixed T_{dev} of 385 K (GIGA off). The obtained transient IV from the electro-thermal model is plotted as the plus signs in Fig. 2.16. The measured transient IV for the same bias conditions on PISCES/GIGA, is given by the circles in Fig. 2.16. Clearly, the proposed electro-thermal model has been able to successfully predict the transient IV in the presence

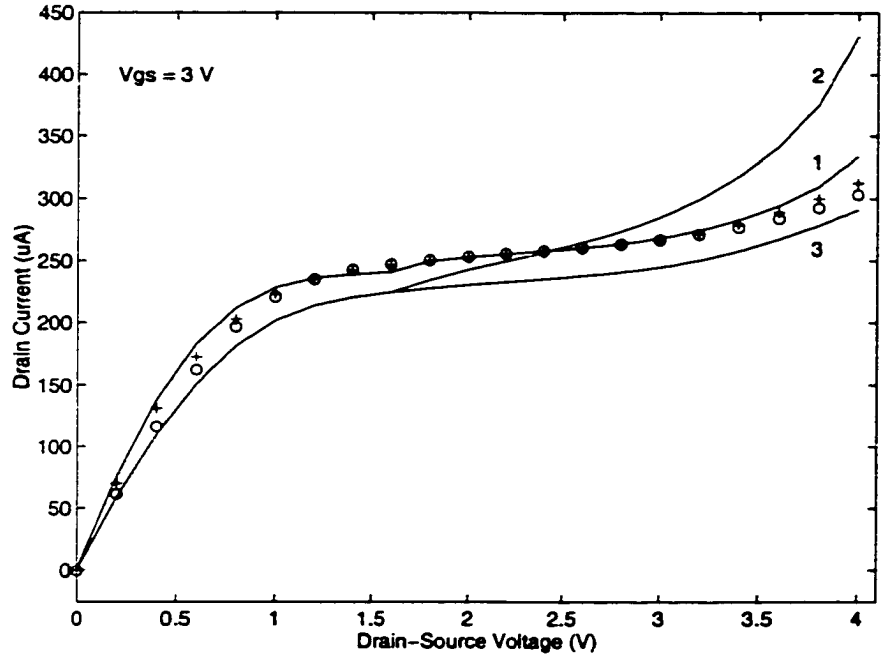


Figure 2.16: 1 - DC IV obtained with GIGA on (non iso-thermal) for a fixed T_{sub} of 300 K and $V_{GS} = 3$ V, 2 - iso-thermal IV (GIGA off) for $V_{GS} = 3$ V and a fixed device temperature of 385 K, 3 - $I_{D,RF}$, defined as the transient IV around $V_{GS} = 3$ V and $V_{DS} = 1.5$ V (biased below kink) for a fixed T_{dev} of 385 K (GIGA off), plus signs are $I_{D,trans}(v_{GS} = 3, v_{DS}, V_{GS} = 3, V_{DS} = 2.442, T_{dev} = 385)$ predicted by self-biasing model, while circles give measured $I_{D,trans}$ obtained from PISCES/GIGA

of a large DC self heating ($T_{dev} = 385$ K and $T_{sub} = 300$ K). The small deviations are due to the neglected dependence of $I_{D,trans}$ on V_{BS}. Note that a more complex thermal topology might be required to model large devices in order to account for the distributed thermal effects along the gate width and the thermal boundary conditions associated with the interconnect layout.

CHAPTER 3

LDMOSFET Device Characterization and Small Signal Model Extraction

The large signal DC and RF model presented and verified on the PISCES device simulator is applied to the Motorola MRF 181 RF power, n-channel enhancement mode, laterally diffused MOSFET. The MRF 181 is designed for broadband commercial and industrial applications for frequencies up to 1.0 GHz. The high gain and broadband performance of this transistor makes it suitable for large signal, common source amplifier applications in 12.5 and 28 V mobile, portable, and base station equipment. The MRF 181 has 4 cells, each containing 56 fingers of 90 μm finger width. At 945 MHz (GSM), the MRF 181 can deliver an output power of 4 W at a power gain of 13dB and efficiency of 30% [50].

Motorola manufactures an entire line of RF power transistors in the MRF 18X markings. The higher the number for X, the more output power the transistor can deliver. These transistors are simply made up by connecting a larger number of basic

cells. Hence modeling techniques used for the MRF 181 can easily be extended to other higher power transistor in the MRF 18X family.

3.1 Computer Controlled Data Acquisition

For modeling to be successful, accurate data acquisition is vital. This includes not only current and voltage information, but also microwave and temperature data. Device probing is the best way to acquire accurate data for on chip devices. However for large devices that are formed by the parallel combination of many small devices, current crowding and the inherent low impedance of the device makes it difficult to simply combine the extracted model for a unit device. For large packaged devices, DC measurements can be very difficult due to thermal instability, while microwave measurements can be challenging due to the low impedance of the device. It is therefor necessary to ensure that the biasing methodology used for both measurement and circuit design are the same.

In order to automatically gather the current, voltage, temperature and microwave data for the MRF 181, LabWindows is used to design an automated data acquisition system [51]. LabWindows allows for code to be written in C to control the various measuring instruments using GPIB, and to down-load and process data. The complete electro-thermal and microwave measurement setup is shown in Fig. 3.1.

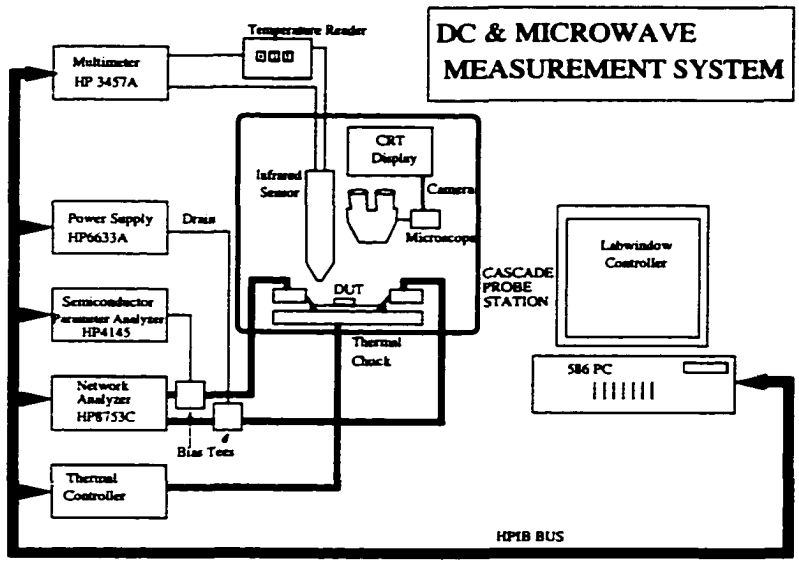


Figure 3.1: Electro-thermal and microwave measurement setup

3.1.1 Test Bed Design and Temperature Calibration

A mechanical test bed has been designed to allow for the mounting and clamping of the MRF 181. The test bed is made from steel and is platted with electrolyte nickel to prevent rusting while providing an excellent electrical and thermal interface.

Two dielectric caps are screwed in at the drain and gate respectively to establish electrical contact. The top of the device is pressed on with a metal bar so as to establish source contact. The top part of the packaging of the MRF 181 has a small hole drilled through using a Silicon Carbide drill bit. This allows for access to the device surface. The metal bar cover pressing on the top of the device has a hole drilled through to allow the infra red thermometer to focus on the device surface. The MRF

181 is a relative large device (1 mm^2) and the germanium lens of the IR thermometer and the thermometer position can be easily adjusted so as to focus the targeted measurement area of the IR thermometer (indicated by a ring) on the FET die. This enables the average device temperature, $T_{dev,avg}$, to be computed by measuring the current flowing through the thermometer using the HP 3457A multimeter. The data measured are very reproducible from measurement to measurement indicating that the focus, alignment and elevation of the thermometer is well established.

The infra red thermometer has to be calibrated by correctly setting the emissivity of the device surface. This is discussed later.

The test bed has to be as flat as possible so as to make an excellent thermal contact with the thermal chuck that is used to control the substrate temperature, T_{sub}. The Temptronic TP0315 Thermo-Chuck temperature controller and heater is used to raise the temperature of the chuck from room temperature (about 29°C) to over 100°C. A Temptronic chiller using water cooling, is used to bring T_{sub} to as low as 10°C.

The emissivity of the infra red thermometer is determined by setting T_{sub} with a cold device (without bias) mounted on the test bed, waiting for 240 seconds to allow for the system to reach a thermal steady state condition (equilibrium) and then measuring the device temperature. Note that this time delay is in excess of the thermal time constant of the test system (substrate heater, testbed and substrate to mount device) and is much larger than the thermal time constant of the device.

The emissivity value is correct when $T_{dev,avg} = T_{sub}$. The procedure is repeated for various T_{sub}'s until a consistent emissivity value can be found that enables the equality to hold over the anticipated substrate temperature range. For the MRF 181, an emissivity value of 73 has been found to measure the device temperature within 1.2 % for a substrate temperature range from 20°C to 95°C. The calibration verification curve appears in Figure 3.2.

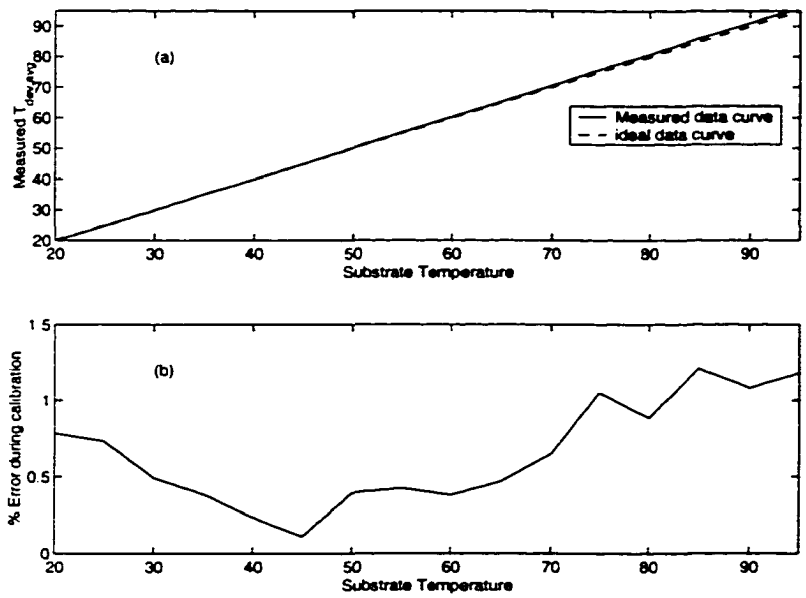


Figure 3.2: IR thermometer calibration verification. Solid line in (a) is measured $T_{dev,avg}$ for a given T_{sub} for a cold device, while the dashed line is the ideal curve. (b) shows the percentage error between the set T_{sub} and the measured $T_{dev,avg}$

The IR thermometer is focused to cover the device surface. The device consists of 224 fingers. Hence when the device is biased, there will indeed be a gradient in device temperature, with the finger temperature differing from the immediate surrounding

area and from finger to finger [26]. In essence what the IR sensor measures is an average device temperature.

3.2 DC and Thermal Characterizations

In order to obtain a complete DC and thermal profile of the device, LabWindows is used to vary V_{GS} (using the HP 4145), V_{DS} (using the HP 6633A) and T_{sub} (using the TP0315). The resulting I_D and $T_{dev,avg}$ is measured. The program sets T_{sub} and V_{GS} and sweeps V_{DS}. When all gate voltages are done, the substrate temperature is changed. When $T_{dev,avg}$ exceeds 190°C, V_{DS} is not increased further for that particular gate voltage. This prevents the device from suffering from destructible thermal damage. Further, a 0.9A limit is set on the drain current while V_{DS} and V_{GS} are limited such that the DC power ($V_{DS}I_D$) remains in a safe operation range while making measurements.

Fig. 3.3 shows the measured I_D (dashed line) and $T_{dev,avg}$ (solid line) as a function of V_{GS} for a V_{DS} of 16V and a T_{sub} of 30°C . A threshold voltage of about 3.8V is observed. Other devices were observed to have different threshold volatges. According to the manufactures own data specs, the threshold voltage can vary from a minimum of 1V to a maximum of 4V from device to device. A threshold curve is important to decide the gate voltage range on which the device is to be measured. The drain voltage range is set to between 30 to 40V (depending upon the device) to accommodate

biasing a power amplifier from between 15 to 20V. This is due to the fact that the maximum voltage swing experienced by the power amplifier is twice V_{DD}.

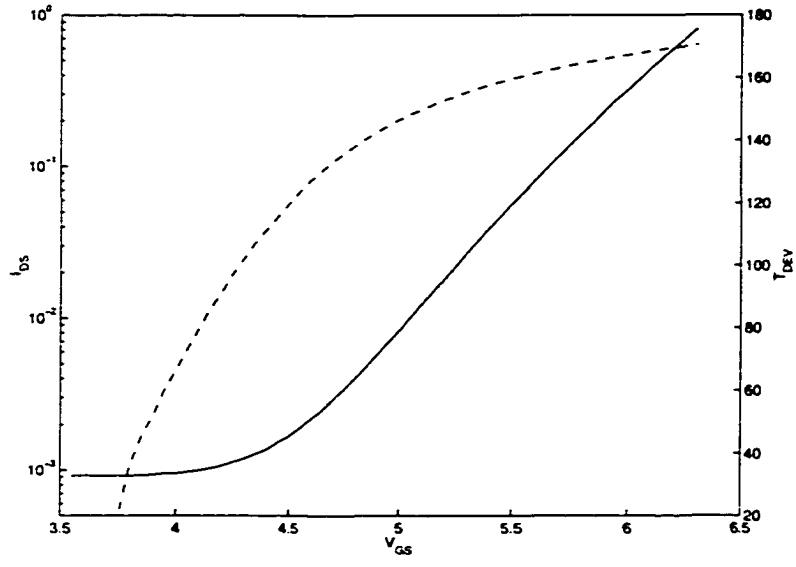


Figure 3.3: Measured I_D (dashed line) and $T_{dev,avg}$ (solid line) as a function of V_{GS} for a fixed V_{DS} of 16V and T_{sub} of 30°C

Fig. 3.4 shows the measured IV for a T_{sub} of 29°C. The resulting device temperature is super imposed at each bias point. From Fig. 3.4, $T_{dev,avg}$ is seen to exceed 180°C for high bias values. Also at high bias, the drain current is observed to decrease as a result of the self-heating in the device. The higher device temperatures cause the carrier mobility value to decrease, leading to negative drain conductance. Fig. 3.5 shows a similar plot for a T_{sub} of 99°C. The drain voltage plotted in both measurements is the extrinsic voltage, in this case defined as the voltage reading on the power supply. By deembedding the 2.1Ω parasitic resistance associated with the

drain biasing network, the intrinsic drain voltage can be obtained. Note that a further correction is required to obtain the actual intrinsic voltage seen at the drain. This is obtained be removing the drain parasitic resistance associated with the FET.

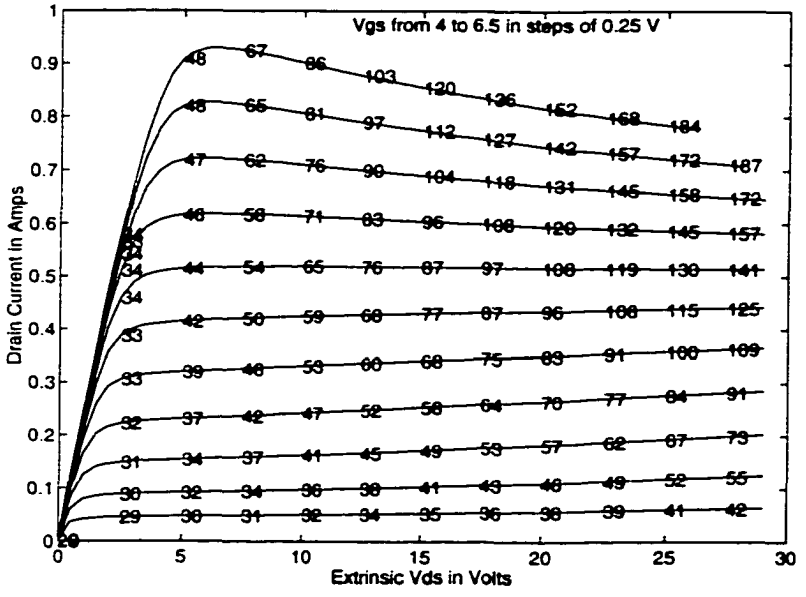


Figure 3.4: Measured IV, with $T_{dev,avg}$ super imposed, for constant substrate temperature of 29°C. V_{GS} ranges from 4V (lowest curve) to 6.5V (highest curve) in steps 0f 0.25V

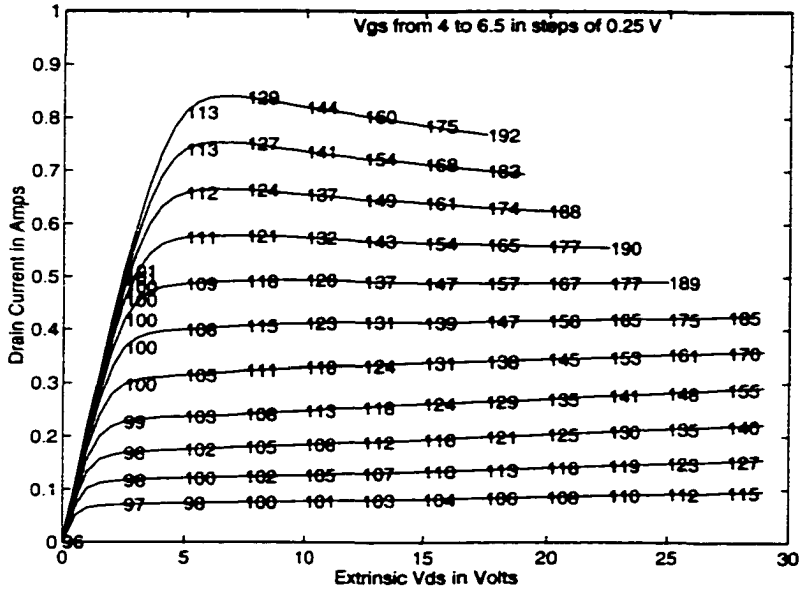


Figure 3.5: Measured IV, with $T_{dev,avg}$ super imposed, for constant substrate temperature of 99°C. V_{GS} ranges from 4V (lowest curve) to 6.5V (highest curve) in steps 0f 0.25V

3.2.1 Thermal resistance extraction

A single thermal resistance, R_{th}, as shown in the electro-thermal model in Fig. 2.7, can be obtained by using a least squares fit on the temperature versus intrinsic device power characteristics. R_{th} is given as:

$$R_{th} = \frac{T_{dev} - T_{sub}}{P_{DC}} \tag{3.1}$$

A single R_{th} value is extracted for each T_{sub} and is found to be 8.45°C/W for T_{sub} = 29°C. At T_{sub} = 99°C, R_{th} equals 7.75°C/W. The thermal resistance is observed to be monotonously decreasing with increasing substrate temperature. Different devices

were found to have quite different R_{th} values. It is important to note that the R_{th} obtained in this computation is not just that for the device, but includes the thermal resistance contribution from the substrate (which is expected to be small).

Using this R_{th} value, the device temperature for a given bias can be computed. The solid lines in Figs. 3.6 and 3.7 show the predicted $T_{dev,avg}$ for a T_{sub} of 29°C and 99°C respectively. The circles give the measured $T_{dev,avg}$. Clearly then, a single R_{th} can predict the entire thermal map of the device.

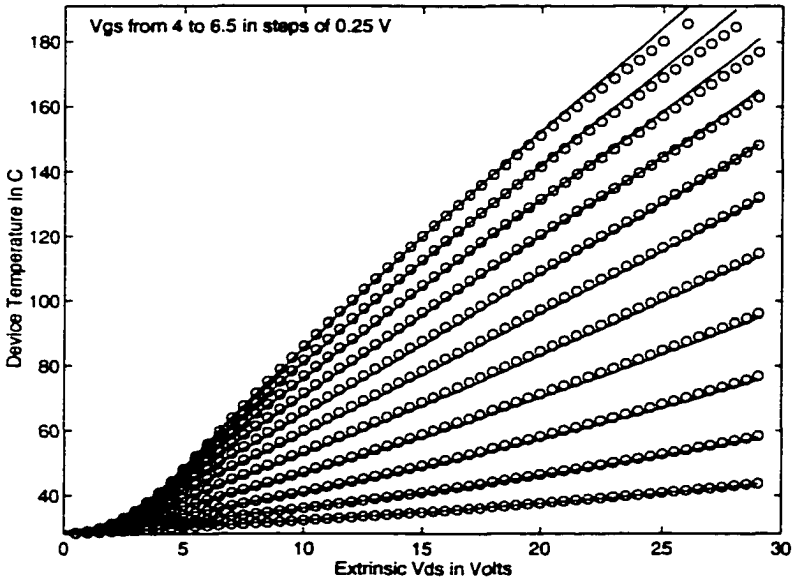


Figure 3.6: Prediction of device temperature (solid lines) compared with measured values (circles) using a single R_{th} for a given T_{sub} of 29°C. V_{GS} ranges from 4V (lowest curve) to 6.5V (highest curve) in steps 0f 0.25V

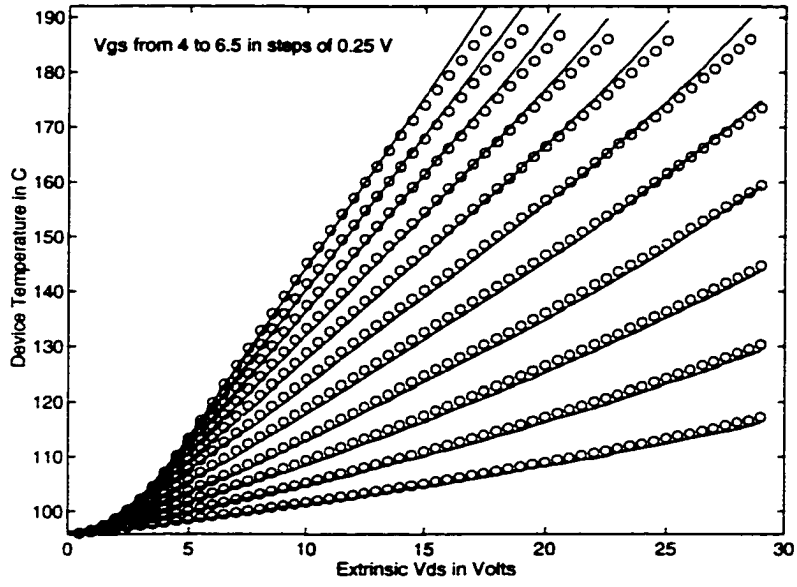


Figure 3.7: Prediction of device temperature (solid lines) compared with measured values (circles) using a single R_{th} for a given T_{sub} of 99°C. V_{GS} ranges from 4V (lowest curve) to 6.5V (highest curve) in steps 0f 0.25V

3.2.2 B-spline extractions of iso-thermal IVs

Using 3-D Tensor Product Splines (TPS), a function of three variables can be represented as:

$$S(V_{GS}, V_{DS}, T_{DEV}) = \sum_{i=1}^{m}\sum_{j=1}^{n}\sum_{l=1}^{p} a_{ijk}\ B_{i,k_{GS},t_{GS}}(V_{GS})B_{j,k_{DS},t_{DS}}(V_{DS})\ B_{l,k_{DEV},t_{DEV}}(T_{DEV}) \quad (3.2)$$

Hence the TPS method can be used to extract a complete IV characteristic for a given device temperature. Such an IV curve will be essentially iso-thermal since the device temperature at each bias point will be the same. In Figs. 3.8 the TPS extracted iso-thermal IV (solid lines) is compared against the measured (circles) iso-thermal IV at $T_{dev,avg}$ of 60°C. The measured data is obtained by searching through

the entire electro-thermal data file and grabbing only those bias points that yield the required device temperature. The iso-thermal IVs clearly do not contain the self heating effects observed in the non iso-thermal IV. The TPS method is able to do an excellent job in extracting the iso-thermal IV.

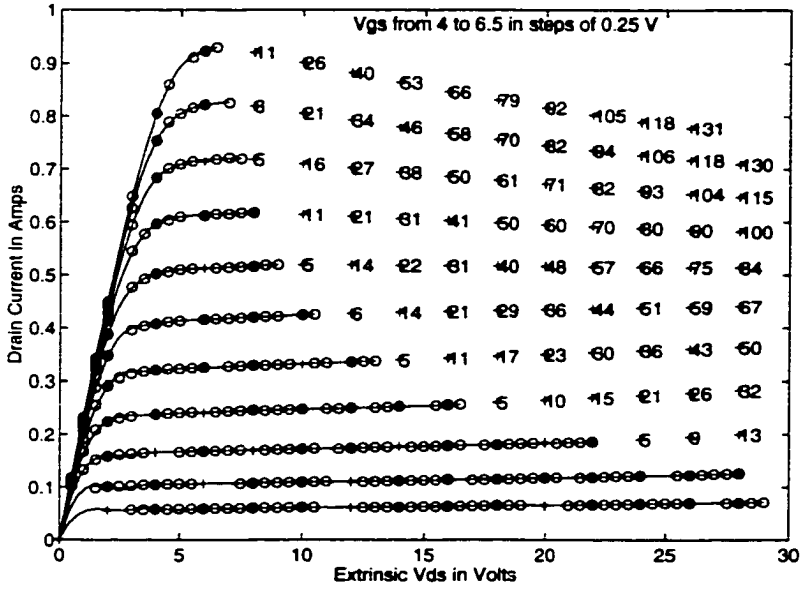


Figure 3.8: Iso-thermal IV extraction using TPS (solid lines) compared with measured values (circles). Super imposed temperature values indicate needed device cooling to access bias point. $T_{dev,avg} = 60°C$. V_{GS} ranges from 4V (lowest curve) to 6.5V (highest curve) in steps 0f 0.25V

It should be noted that these are the curves that a power amplifier will use to determine its' DC biasing point. The range of the data predicted by the TPS method is limited to that of the data that is available. Lowering the substrate temperature will allow for data at higher biases to be available for a given $T_{dev,avg}$. In Fig. 3.8, for those points that do not have drain current data, the required temperature that the

substrate needs to be lowered by, is superimposed. This is estimated by measuring the temperature difference between the nearest temperature data at a particular bias point and the targeted device temperature.

Drain current data at higher biases can also be obtained using transient IVs. It should be noted that while transient IVs are iso-thermal (device temperature has not changed), they are not the same as the iso-thermal IVs discussed above. Transient IVs bypass not only self-heating, but also traps, defects and impact ionization effects. These are the IVs that form the RF load line of a power amplifier. The iso-thermal IV on the other hand bypass only the self heating of the device and form the DC biasing loadline of a power amplifier.

At low biases where theses effects are minimal, the iso-thermal and transient IVs for the same $T_{dev,avg}$ will have a better agreement. This criterion can be used to obtain a RF IV. Further, due to the expected low dispersion in LDMOSFETs, the iso-thermal and pulsed IVs are expected to be in better agreement than for SOI MOSFETs.

3.2.3 Direct Iso-thermal IV Measurement Using Heating and Cooling

A novel approach to directly measure an iso-thermal IV has been implemented in LabWindows [52]. In this approach, the substrate is set to the lowest temperature (in

this case cooled to 18°C) and V_{GS} is set to its highest value. V_{DS} is then swept and the drain current at all data points within +/- 2°C of the targeted $T_{dev,avg}$ are recorded after establishing thermal equilibrium. A time delay in excess of 5 seconds is sufficient when going from one bias point to another. Note that the thermal time constant of the channel self-heating is in the micro second range (minimum required for acquiring valid pulse measurements). V_{GS} is then lowered and the process continues.

Once the data has been acquired for the lowest V_{GS}, the substrate temperature is increased each time (in this case by 4°C) and the process is repeated. A 240 second delay is administered from one T_{sub} to the other to permit the packaging (metallic source contact and the entire system) to reach thermal equilibrium with the substrate. By performing transient temperature measurements, the thermal time constant of the entire system can be measured. This is demonstrated in Fig. 3.9 which shows transient measurements for $T_{dev,avg}$ on changing T_{sub} for a cold device from 25°C to 30°C (a), 30°C to 35°C (b), and 35°C to 40°C (c). Clearly 240 seconds is a sufficient delay for the system to reach thermal equilibrium given the 1.2 % accuracy of the thermometer.

The higher the substrate temperature, the lower the bias point that will give the targeted $T_{dev,avg}$. This novel approach permits a rapid data acquisition since all data are acquired in a single sweep of the substrate temperature from its lowest to highest value. This procedure minimizes the impact of the thermal inertia of the substrate on the measurement time and is fully reproducible from measurement to measurement.

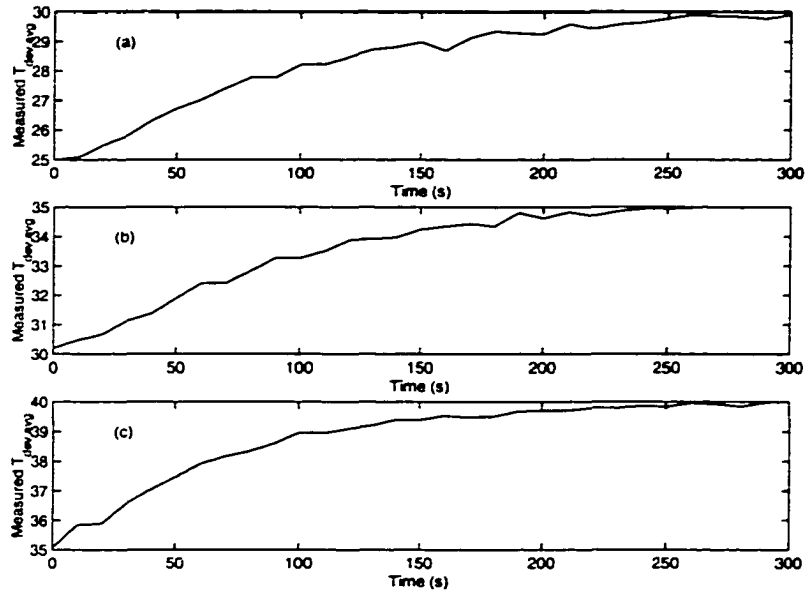


Figure 3.9: Transient measurements for $T_{dev,avg}$ on changing T_{sub} for a cold device from 25°C to 30°C (a), 30°C to 35°C (b), and 35°C to 40°C (c)

The circles in Fig. 3.10 shows the directly measured 90°C iso-thermal IV, which is in excellent agreement with that extracted using TPS (solid lines).

By cooling the substrate, the range of the iso-thermal IV acquired can be increased since for a cooler substrate, a higher bias point will give the targeted $T_{dev,avg}$, compared to a warmer substrate. Cooling is accomplished using a chiller unit that circulates cooled water through the thermochuck. The chiller also allows for a much more accurate control of T_{sub} at higher biases, where the large $T_{dev,avg}$ can cause the substrate temperature to increase.

Fig. 3.11 shows the constant T_{sub} contours (dashed lines) for directly measuring a 90°C iso-thermal IV. T_{sub} ranges from 18°C to 86°C in steps of 4°C (all contours are

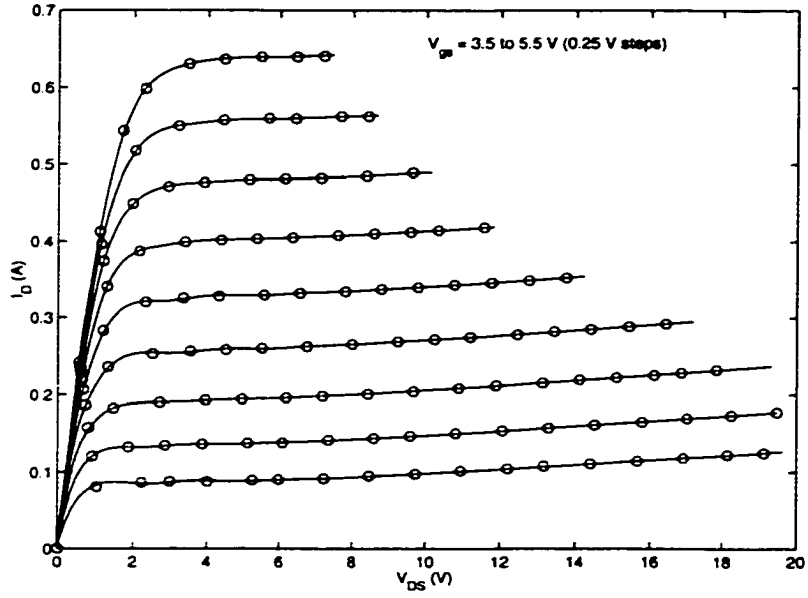


Figure 3.10: TPS extracted (solid lines) and directly measured (circles) iso-thermal IV for $T_{dev,avg}$ = 90°C with both device cooling and heating. V_{GS} ranges from 3.5V (lowest curve) to 5.5V (highest curve) in steps 0f 0.25V

not shown). The solid line is the measured iso-thermal IV for V_{GS} from 3.5V to 6V in steps of 0.5V. Fig. 3.11 highlights the implementation of the efficient T_{sub} sweeping algorithm and shows the need for device cooling to access more IV points giving the targeted $T_{dev,avg}$.

3.2.4 Choice of Testbed Material

In order to extract an iso-thermal model of the LDMOS, iso-thermal IVs and s-parameters are measured as discussed earlier. This technique relies on setting a T_{sub} and efficiently searching for all bias points giving the targeted $T_{dev,avg}$. The technique

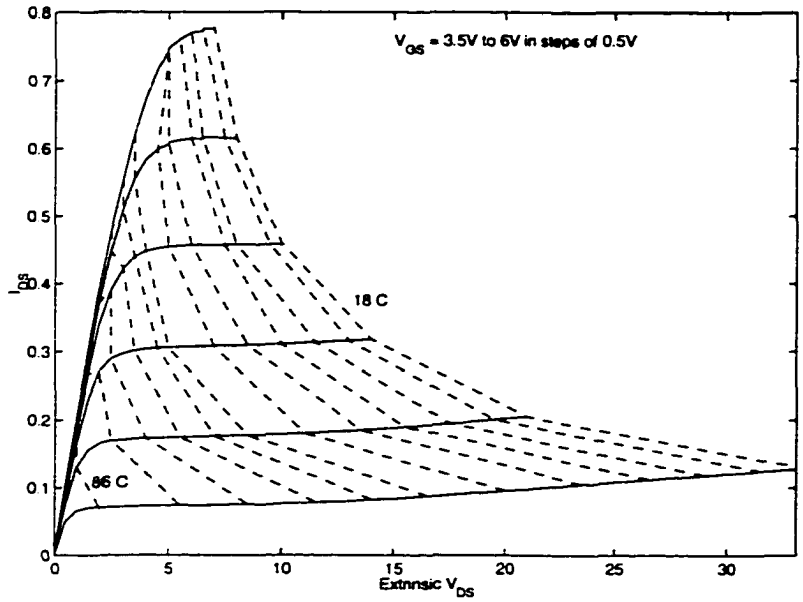


Figure 3.11: Constant T_{sub} contours (dashed lines) for directly measuring a 90°C iso-thermal IV. T_{sub} ranges from 18°C to 86°C in steps of 4°C (all contours are not shown). Solid line is measured IV. V_{GS} ranges from 3.5V (lowest curve) to 6V (highest curve) in steps of 0.5V

is limited by the fact that to access bias points in high gate and drain voltage regions (hot), device cooling has to be used to get the targeted $T_{dev,avg}$. The more the cooling, the more the data available in this region.

From a measurement point of view, the cooling of the substrate is limited. However it is important to realize that on setting a particular T_{sub} value on the thermo-chuck, what is actually being set is the temperature on the under side of the metal testbed plate, on which the device is mounted. The device itself is sandwiched between two circuit boards with its source directly contacting the top side of the metal testbed plate.

Hence depending upon the thermal resistance of the testbed plate itself, the device source substrate will see a temperature different from that set by the thermo-chuck controller. If the R_{th} of the material used is high, the temperature drop across the testbed plate is larger, hence the temperature seen by the device source contact is higher, for a constant device temperature. Therefor the lower the R_{th} of the metal substrate plate, the closer the device substrate temperature is to that set by the thermo-chuck, and hence the greater the number of bias points accessed for the targeted constant $T_{dev,avg}$.

Based upon this fact, an aluminum plate, that has a smaller R_{th} compared to that of steel, has been used to gather iso-thermal IV and s-parameter data. Iso-thermal data is acquired for different device temperatures corresponding to the expected range of operation of the designed power amplifier.

3.3 Microwave Characterizations

In order to obtain a DC and RF model, iso-thermal s-parameter data for the LDMOSFET has to be acquired. In the presence of strong dispersion effects, pulsed IV, pulsed RF measurements are needed to obtain such data [30]. Such measurement systems are very expensive and normally inaccessible to academic laboratories. However in the absence of strong dispersion effects, the technique presented earlier for acquiring iso-thermal IVs, can be used to acquire iso-thermal s-parameters. Once

pulsed IV data has been acquired, it can be differentiated to obtain the AC g_m and g_d, which can be compared with that obtained from iso-thermal microwave data to access how feasible this approach is for LDMOSFETs.

The iso-thermal microwave data are obtained by using the HP 8753E network analyzer and measuring all the s-parameters of the device for each bias point corresponding to the desired $T_{dev,avg}$. This is programmed in LabWindows to work in concert with the automatic iso-thermal IV acquisition and ensures that all scattering parameters measured are at the targeted $T_{dev,avg}$.

Due to the high gain of the MRF 181 at lower frequencies, the drain current associated with a particular DC bias point can change while measuring the s-parameters. To counter this, a three band calibration scheme has been used. In the first two bands from 0.3 MHz to 450 MHz and 400 MHz to 3 GHz, a 20 dB attenuation is introduced at port 1 of the network analyzer. The third band from 2.5 GHz to 6 GHz does not contain any attenuation factor. When measuring the forward transmission parameter (S_{21}), the drain current is monitored at the lowest and highest frequency to ensure that there is at most an insignificant change in its value.

3.3.1 TRL calibrations

The most ubiquitous calibration scheme used to remove errors from measured s-parameters data is SOLT (Short, Open, Load and Thru). However because of the

difficulty in fabricating a good load standard, SOLT is not very desirable. The TRL (Thru, Reflect and Line) technique is instead used since it does not rely on known standard loads but rather uses simple connections to allow for the error boxes to be characterized completely [53]. The Thru is a direct connection between the two ports at the desired reference plane. The Reflect uses a load with a large reflection coefficient, such as a short or an open. It is not necessary to know the reflection coefficient since it is extracted during the TRL calibration procedure. This then gives an additional verification to the accuracy of the TRL calibration performed. In the Line connection, a length of matched transmission line is connected between the two ports. The length of the line need not be know and it needs not to be lossless, since these parameters will be determined by the TRL procedure [54]. However, the length of the lines used determines the frequency band of validity for the TRL calibration. Further loss has been shown to increase the calibration accuracy, hence a lossy line can provide a usable calibration over a broader band.

In order to attempt to span the entire band, two separate lines are used. A small line for higher frequencies and a long line for lower frequencies. In this approach, the two separate lines span two non overlapping frequency bands. A multiline method using a linearized covariance matrix utilizes out of band data of the two lines to further reduce the overall error. This technique has been implemented to process the obtained s-parameters [55].

The TRL approach is verified for acceptability of performance prior to using it on transistor data. The big line is used as the line standard and the small line is measured. Fig. 3.12 shows the corrected s-parameters of the small line using both the big line (solid lines) and the multiline technique (dashed lines). Both the forward and reverse match (S_{11} and S_{22}) and the forward and reverse transmission (S_{21} and S_{22}) from both the big line (solid lines) and the multiline technique (dashed lines) do a good job at low frequencies (less than 2 GHz). At intermediate frequencies (from 2 to 3 GHz) the multiline techniques still does a decent job while the big line fails. At higher frequencies, both methods get in trouble with the forward and reverse transmission.

Next the small line (solid lines) is used as the line standard and the big line is measured as shown in Fig. 3.13. Here the multiline technique (dashed lines) does a better job in the low frequency and intermediate frequency range (less than 3 GHz), especially for the forward and reverse match. At higher frequencies (greater than 3 GHz), both techniques yield similar results. However there are some isolated problems in the forward and reverse transmission. Additionally, the forward and reverse match are not as good.

Based upon these observations, the big line is used as the standard for the first band, the multiline for the second band and the small line for the third band. Further the quality of the data in the third band is expected to be not as good. This is clear given that at higher frequencies, fabrication errors in the calibration standards are

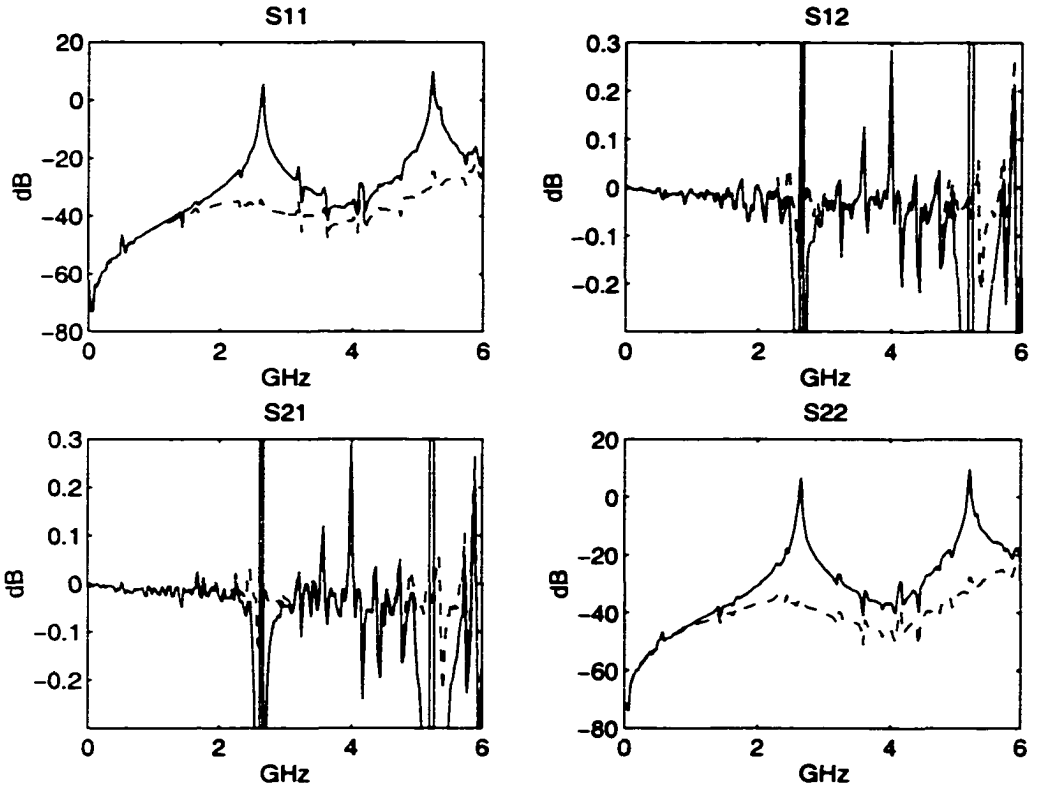


Figure 3.12: TRL prediction of small line using big line (solid lines) and covariance technique (dashed lines)

more pronounced. A way around this is to use an external foundry to more accurately fabricate the calibration standards.

The TRL approach is applied to the iso-thermal transistor data. Fig. 3.14 shows the extracted reflect standard (open). It is apparent that the higher frequency data is not as good as the lower frequency data, as expected.

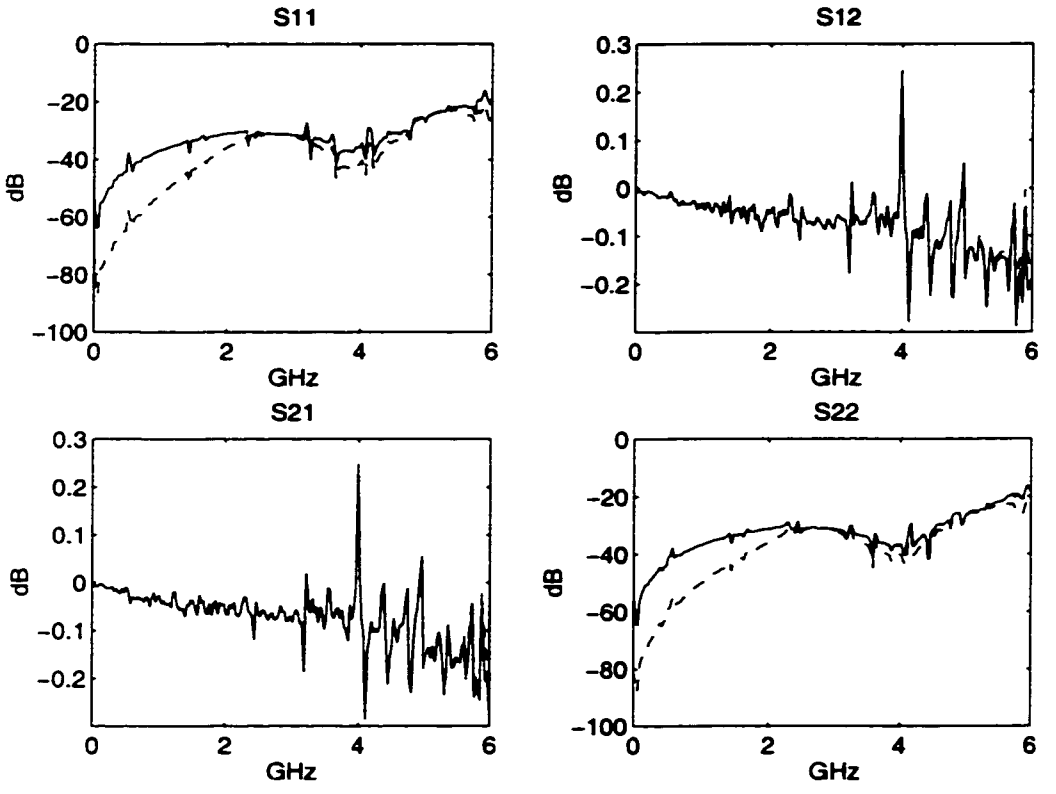


Figure 3.13: TRL Prediction of big line using small line (solid lines) and covariance technique (dashed lines)

3.3.2 Final Data Acquisition

Once the iso-thermal measurement tools are ready, data necessary to extract the device model is measured. For the device for while much of the small and large signal extraction are to be presented, V_{GS} ranges from 4V to 6.5V in steps of 0.25V. V_{DS} ranges from 0 to 40V (which will depend on the $T_{dev,avg}$ and V_{GS}). Five iso-thermal IVs, and hence corresponding scattering parameters, are measured for $T_{dev,avg}$ from 45°C to 105°C in steps of 15°C. S-parameters are acquired in the 400MHz to 3GHz

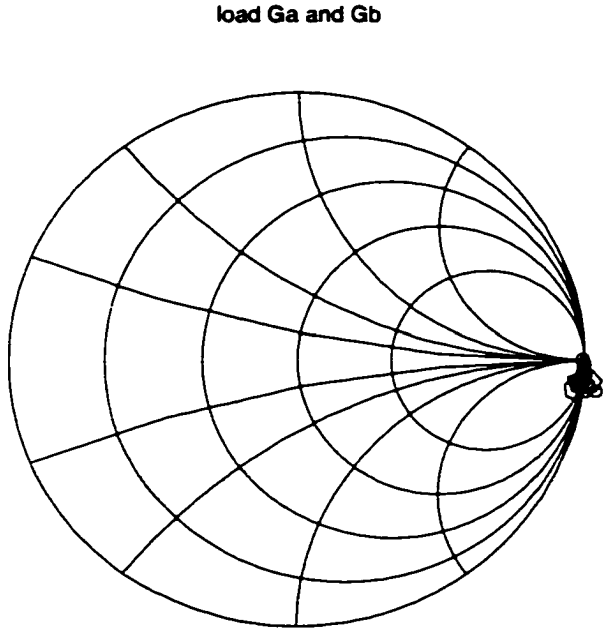


Figure 3.14: Load extraction using TRL

range. For s-parameter measurements, a two step calibration process is used. First a 7mm SOLT calibration is performed on the ports of the Network Analyzer s-parameter test set. Secondly, the TRL calibration is administered on the gate and drain planes of the transistor.

3.4 Parasitic Deembedding

Fig. 2.2a shows the small signal model used in this work together with the associated device parasitic resistances and inductances. The Y-parameters of the intrinsic topology can be written as;

$$Y_{ij} = g_{ij} + \frac{j\omega C_{ij}}{1 + j\omega\tau_{ij}} \tag{3.3}$$

where C_{ij}, g_{ij} and τ_{ij} are the bias depended capacitance (trans-capacitance), conductance (trans-conductance) and non-quasi static times constants, respectively. Note that $g_{11}= g_{12} = 0$ and that $g_{21} = g_{m,RF}$ and $g_{22} = g_{d,RF}$. The non quasi static time constants introduce a redistribution time for the charge, which becomes important at frequencies approaching f_{max} [14], [15]. A two τ approximation can be made such that $\tau_{11} = \tau_{12} = \tau_G$ and $\tau_{21} = \tau_{22} = \tau_D$.

The inductances represent contributions from both the device and the package (bond wires). It can be shown that the complex representation of the device package inductances (composed of mutual and self inductors) can be reduced to three distinct inductors. Parasitic capacitances are considered to be absorbed within the small signal model of the device.

Although the intrinsic model is quite simple, the extrinsic model is quite complicated because of a transformation from Y to Z parameters. Deembedding of the

parasitics associated with the FET and the package does not have an easy solution because of the fact that a DC gate current does not flow in many FETs.

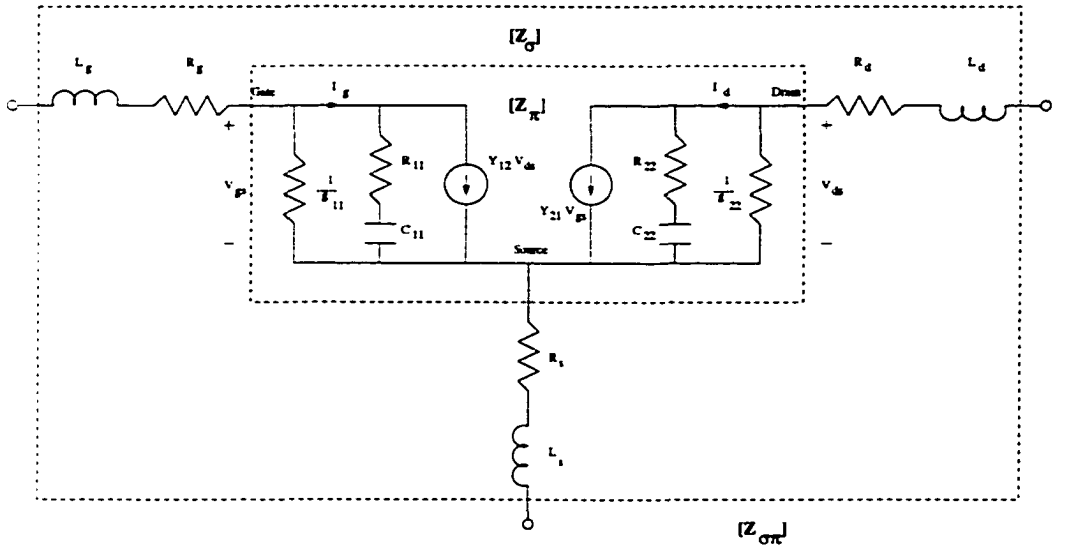


Figure 3.15: Small signal model with external parasitics

3.4.1 Cold Measurements

In order to obtain values for the parasitic inductances, cold s-parameter measurements (under zero bias on the gate) are performed. Under cold bias, g_m and g_d are zero. Further, C_{12} and C_{21} are assumed symmetric and hence equal. The reduced small signal model is fitted to the cold data to extract the parasitic inductors. This procedure also yields values for the parasitic resistances. However, while it was found that the values of the parasitic inductors stayed almost constant for different

cold bias points, the values of the parasitic resistors varied quite a bit. It has been demonstrated that cold measurements cannot give accurate values for parasitic resistances [57]. Values of the parasitic inductances extracted are: $L_g = 728.57$pH, $L_d = 563.29$pH and $L_s = 63.46$pH. The source inductance is normally rather difficult to extract, due to its small value, which is especially so in LDMOSFETs.

3.4.2 Quasi Static Approximation Extraction of Resistances

Assuming only two time constants non-quasi static model (NQS), the resulting extrinsic Z parameters ($Z_{\sigma\pi ij}$) can be written as [56]:

$$Re(Z_{\sigma\pi ij}) = Re(Z_{\sigma ij}) + \Delta R_{ij} + \frac{A_{ij}}{\omega^2 + B_\tau^2} \tag{3.4}$$

$$\frac{1}{\omega} Im(Z_{\sigma\pi ij}) = Im(Z_{\sigma ij}) + \Delta L_{ij} - \frac{B_{ij}}{\omega^2 + B_\tau^2} - \frac{G_{ij}}{\omega^2(\omega^2 + B_\tau^2)} \tag{3.5}$$

where $Re(Z_{\sigma ij})$ contains only the parasitic resistances and $Im(Z_{\sigma ij})$ contains the parasitic inductances, while the rest of the elements are analytical expressions containing the small signal model elements.

From Eqs. 3.4 and 3.5, it is observed that the denominator is common across all the Z-parameters. This fact can be used to obtain parametric curves between two extrinsic Z-parameters [56]. If the model topology holds true, liner regressions should be observed. Fig. 3.16 shows the parametric plot obtained on $Re(Z\sigma\pi 21)$ and $Re(Z\sigma\pi 11)$ while Fig. 3.17 shows the parametric plots obtained when plotting

$\frac{1}{\omega}Im(Z_{\sigma 22})$ and $\frac{1}{\omega}Im(Z_{\sigma 12})$. In both figures, the solid line represents the liner fit, while the plus signs are measured data points.

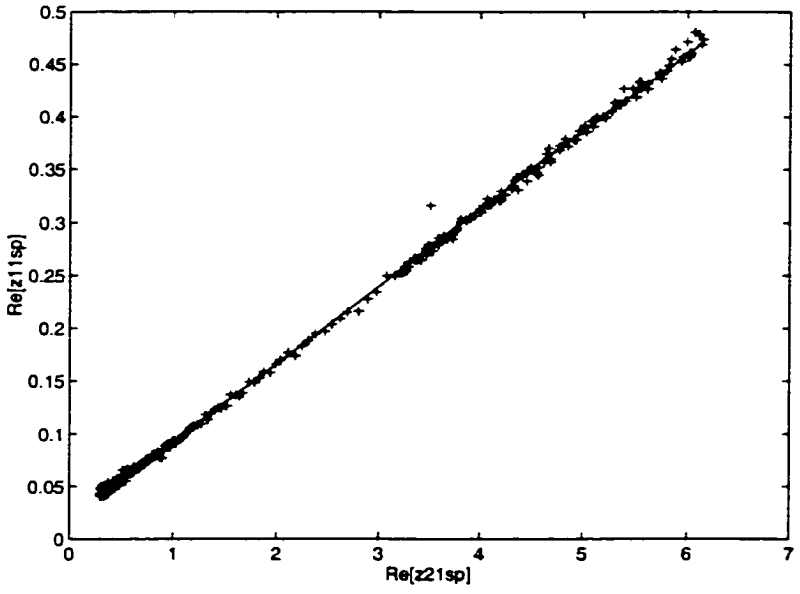


Figure 3.16: Linear parametric regressions (solid lines) to extract relationship between parasitic resistances. Plus signs are measured data

For these plots, low frequency data (which contain dispersive effects not predicted by the small signal model) and high frequency data (which can not be accurately obtained due to inaccuracies in the TRL procedure) have not been used. Clearly, the parametric curves are linear in nature. The slope and intercepts of these curves, together with a least squares approach can be used to determine the values of the coefficients of Eqs. 3.4 and 3.5. These values can then be used to fit the extrinsic Z-parameters.

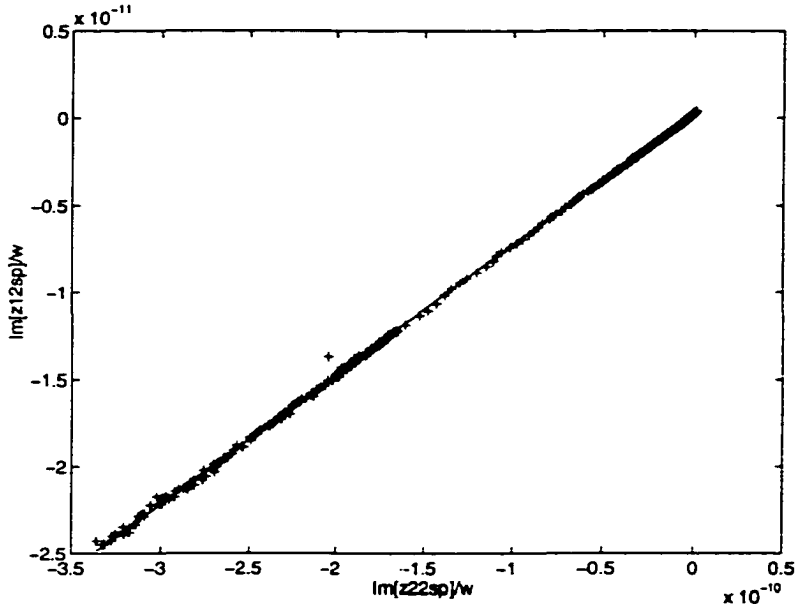


Figure 3.17: Linear parametric regressions (solid lines) to extract relationship between parasitic inductances. Plus signs are measured data

If a quasi static (QS) approximation is made, τ_G and τ_D are assumed to be zero, Eqs. 3.4 and 3.5 still hold with the exception that ΔR_{ij} and ΔL_{ij} are zero. These corrections are as a result of the NQS model. Hence for the QS approximation the parasitic resistors can be approximately directly obtained by parameterizing three sets of $Re(Z_{ij})$ with $Re(Z_{kl})$ [57]. The parametric representations are performed on a bias point in the saturation region of the device and the QS parasitics are averaged over a number of bias points. Obtained values are found to be some what bias dependent. In particular R_d is observed to increase with I_D. However given the relatively small values of these parasitics, R_d is approximated to be bias independent.

$$A = -C_{11}C_{22} - g_d\tau_D C_{11} + C_{12}C_{21} + C_{12}g_m\tau_D$$

$L_{11} = L_g + L_s$	$L_{22} = L_d + L_s$
$L_{12} = L_{21} = L_s$	$G_{22} = G_{12} = 0$
$B = C_{11}g_d - C_{12}g_m$	$B_r = \frac{B}{A}$
$R_{12} = R_s + \delta R_{12}$	$\delta R_{12} = \frac{C_{12}\tau_D}{A}$
$R_{22} = R_s + R_d + \delta R_{22}$	$\delta R_{22} = -\frac{C_{11}\tau_D}{A}$
$R_{11} = R_s + R_g + \delta R_{11}$	$\delta R_{11} = \frac{-(\tau_G\tau_D g_d + C_{22}\tau_G)}{A}$
$R_{21} = R_{se} + \delta R_{21}$	$\delta R_{21} = \frac{-(\tau_G\tau_D g_m + C_{21}\tau_G)}{A}$
$A_{12} = B_r B_{12}$	$B_{12} = -B_r\delta R_{12} - \frac{C_{12}}{A}$
$A_{22} = B_r * B_{22}$	$B_{22} = \frac{C_{11}}{A^2}(B\tau_D + A)$
$I_{p11} = (\tau_G + \tau_D)g_d + C_{22}$	$I_{p21} = -(\tau_G + \tau_D)g_m - C_{21}$
$A_{11} = \frac{g_d}{A} + B_r B_{11}$	$B_{11} = -B_r\delta R_{11} + \frac{I_{p11}}{A}$
$A_{21} = -(\frac{g_m}{A} + B_r B_{21})$	$B_{21} = -B_r\delta R_{21} + \frac{I_{p21}}{A}$
$G_{11} = \frac{-Bg_d}{A^2}$	$G_{21} = \frac{Bg_m}{A^2}$

Table 3.1: Model parameters in terms of the Z_{ij} fit parameters

3.4.3 Full Non Quasi Static Extraction of Resistances

Eqs. 3.4 and 3.5 for the two τ NQS model can be rewritten as follows:

$$Re(Z_{\sigma\pi ij}) = R_{ij} + \frac{A_{ij}}{\omega^2 + B_r^2} \tag{3.6}$$

$$\frac{1}{\omega}Im(Z_{\sigma\pi ij}) = L_{ij} - \frac{B_{ij}}{\omega^2 + B_r^2} - \frac{G_{ij}}{\omega^2(\omega^2 + B_r^2)} \tag{3.7}$$

where the various coefficients are given in terms of model parameters in Table 3.1 [58].

The formula give in Table 3.1 can be inverted to obtain the values of the model parameters from the fitting coefficients of Eqs. 3.6 and 3.7 (A_{ij}, R_{ij}, L_{ij}, B_{ij} and G_{ij}. The resulting equations are given in Table 3.2 [58].

$L_s = L_{12}$	$L_g = L_{11} - L_s$
$L_d = L_{22} - L_s$	$B_r = \frac{B_{11}B_r^2 - G_{11}}{A_{11}}$
$C_{11} = \left\{ -\frac{G_{11}}{B_r^2} + \frac{A_{12}}{A_{22}}\frac{G_{21}}{B_r^2} \right\}^{-1}$	$C_{12} = \left\{ -\frac{G_{21}}{B_r^2} + \frac{A_{22}}{A_{12}}\frac{G_{11}}{B_r^2} \right\}^{-1}$
$g_M = \frac{-G_{21}}{G_{11}(R_{22}+A_{22}/B_r^2) - G_{21}(B_{12}+A_{12}/B_r^2)}$	$g_D = \frac{G_{11}}{G_{11}(R_{22}+A_{22}/B_r^2) - G_{21}(B_{12}+A_{12}/B_r^2)}$
$R_d = \left(-1 + \frac{A_{22}}{A_{12}}\right) R_s + \left(R_{22} - R_{12}\frac{A_{22}}{A_{12}}\right)$	$\tau_D = \frac{R_{12} - R_s}{B_r\left(R_{12} - R_s + \frac{A_{12}}{B_r^2}\right)}$
$c_{11p} = -\frac{A_{22}}{A_{12}}R_s + \left[\frac{A_{22}}{B_r^2} + R_{12}\frac{A_{22}}{A_{12}}\right]$	$c_{12p} = R_s - \left[R_{12} + \frac{A_{12}}{B_r^2}\right]$
$B = -\frac{B_r^2}{c_{11p}G_{11} + c_{12p}G_{21}}$	$\tau_G = -\frac{I_{p21}}{2g_m} \pm \left(\left(\frac{I_{p21}}{2g_m}\right)^2 + \frac{R_{p21}}{g_m}\right)^{1/2}$
$g_m = \frac{BG_{21}}{B_r^2}$	$g_d = -\frac{BG_{11}}{B_r^2}$
$R_{p21} = (R_s - R_{21})B/B_r$	$I_{p21} = B/B_r B_{21} + B(R_{21} - R_s)$
$C_{21} = -[I_{p21} + (\tau_D + \tau_G)g_m]$	$C_{22} = -\frac{B}{C_{11}}\left(\frac{1}{B_r} - \frac{C_{12}C_{21}}{B} + \tau_D\right)$
$R_{p11} = \tau_G\tau_D g_d + \tau_G C_{22}$	$R_g = R_{11} + \frac{R_{p11}B_r}{B} - R_s$

Table 3.2: Model parameters in terms of the Z_{ij} fit parameters. The first rows are for extracted parameters independent on R_s.

From Table 3.2, it can be seen that there exists a continuum of solutions as a function of R_s, the source parasitic resistance, that gives the same fit of the extrinsic Z_{ij} and hence S_{ij} parameters. Note however that C_{11} and C_{12}, the extrinsic conductance g_D and transconductance g_M and all parasitic inductors are independent of R_s and can be uniquely determined for each bias point.

Note that in order to get good results with this method it is important that the fitting coefficients, A_{ij}, R_{ij}, L_{ij}, B_{ij} and G_{ij} are well determined. Different numerical processing can lead to different results. The approach followed was to first establish liner relationships between R_{ij} and L_{ij} [57]. This was followed by obtaining R_{11}, A_{ij} and B_r^2 from a simultaneous least square fit of $Re[Z_{ij}]$. lastly G_{21} and L_{12} were

computed from a simultaneous fit of $Im[Z_{ij}]$ wile using equality constraints (given in Table 3.1) and linear constraints between the L_{ij}.

A range analysis is performed to constrain R_s to values that lead to physical solutions (all positive parameters except for C_{12} and C_{21}). A multibias analysis, in the saturation region is performed, to determine the NQS values of the parasitic resistances. The idea behind this is that the parasitics are generally constant with bias, in particular for constant I_D. Then R_d and R_g can be plotted as a function of R_s. A point of intersection will indicate a valid solution.

Fig. 3.18 shows the obtained loci of R_g and R_d as a function of R_s. An intersection is clearly observed for $R_s = 0.297\ \Omega$ and $R_d = 1.95\ \Omega$. However R_g does not appear to have a clear intercept. This may be due to the fact that R_g ends up being the last parameter extracted and is further observed to be rather insensitive to R_s. R_g can be approximated to be around 2.35 Ω. Note that Fig. 3.18 shows the resulting trajectories for a constant V_{GS} (constant I_{DS}). Plotting these curves for a higher V_{GS} value yields a different intercept. R_s and hence R_d, are found to increase as a function of I_{DS}. In the interest of simplifying the model, parasitics obtained from $V_{GS} = 4.5$V are used, for a V_{DS} range from 10V to 15V.

As a further simplification to the extraction process, the possible temperature dependence of the parasitics was not investigated.

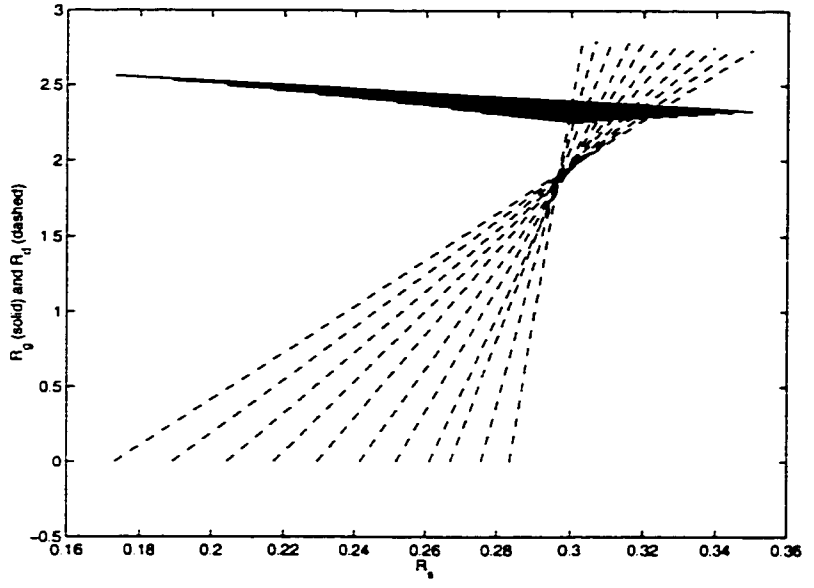


Figure 3.18: Trajectories of R_g (solid lines) and R_d (dashed lines) as a function of R_s for constant I_{DS}

3.5 Small Signal Model Extractions

Once the values of the parasitics have been established, they are deembedded to access intrinsic device data. By using a least squares technique, C_{ij}, g_{ij} and τ_{ij} can be extracted over all bias points. The frequency range from 400 MHz to 2 GHz has been used in this work. Fig. 3.19 shows the resulting s-parameter fits at $V_{GS} = 5.5$V and $V_{DS} = 15$V, while Fig. 3.20 shows the fit for $V_{GS} = 4.5$V and $V_{DS} = 20$V. In the two figures, the solid lines show the fitted results, while the plus signs show the measured data. Over the entire bias range considered, the magnitude error between fitted s-parameters and measured data was found to not exceed 10% for any given bias point.

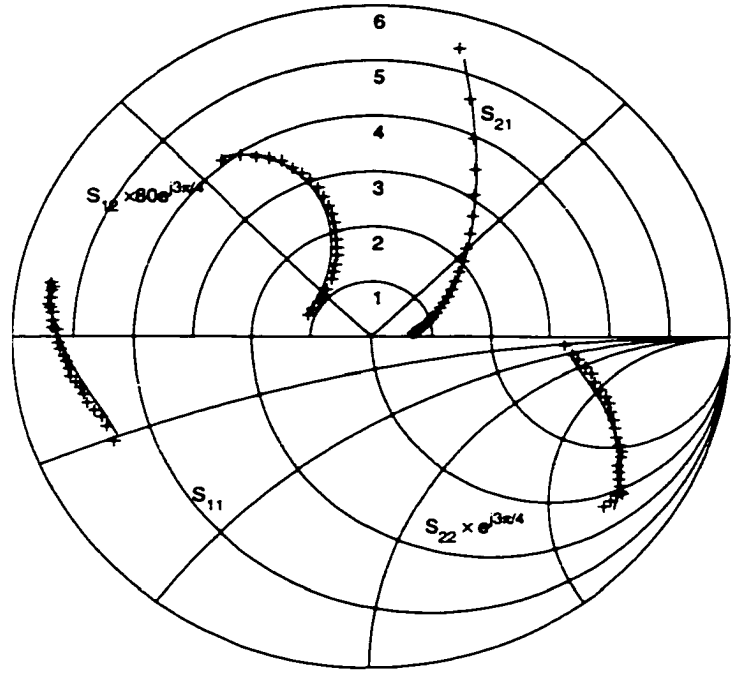


Figure 3.19: Comparison between fitted s-parameters (solid lines) and measured data (plus signs) for V_{GS} = 5.5V, V_{DS} = 15V and $T_{dev,avg}$ of 90°C

Small signal parameters are extracted for each of the five iso-thermal s-parameter data set. This process yields temperature depended small signal parameters. Figs. 3.21 and 3.22 show the variation in the raw extracted g_m and g_d as function of device temperature over all measured bias points. The V_{DS} values are extrinsic values, as defined earlier. V_{GS} is from 4V to 6.5V in steps of 0.5V. Solid lines are for a $T_{dev,avg}$ of 105°C, dashed lines are a $T_{dev,avg}$ of 90°C, dashed dotted lines are for a $T_{dev,avg}$ of 75°C, dotted lines are for a $T_{dev,avg}$ of 60°C and plus signs are for a $T_{dev,avg}$ of 45°C respectively.

It can be seen from Figs. 3.21 and 3.22 that while g_d is relatively temperature independent, g_m is quite sensitive to temperature.

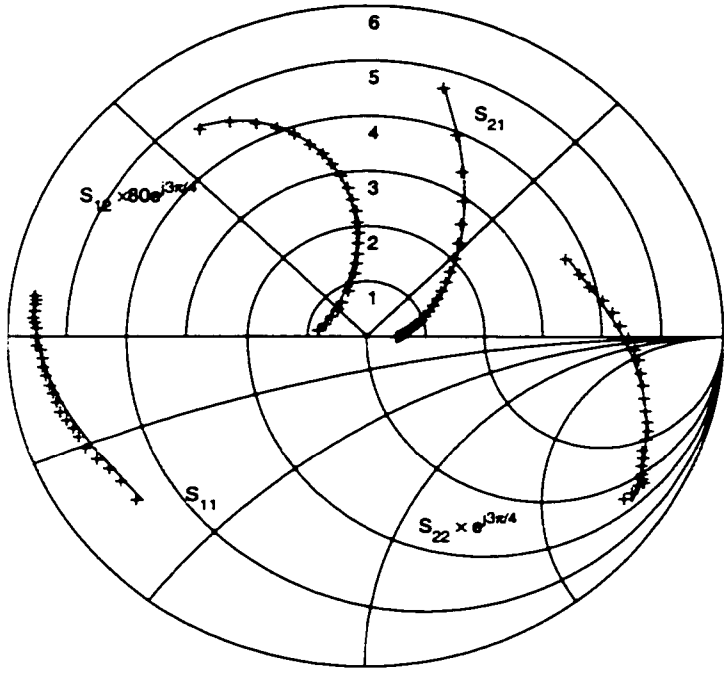


Figure 3.20: Comparison between fitted s-parameters (solid lines) and measured data (plus signs) for V_{GS} = 4.5V, V_{DS} = 20V and $T_{dev,avg}$ of 90°C

Figs. 3.23 through 3.26 show the variation in the raw extracted C_{11}, C_{12}, C_{21} and C_{22} as function of device temperature over all measured bias points. The plot line styles to denote different temperature values used before have been used for these parameters. Also, the V_{DS} and V_{GS} ranges are as before.

It can be seen from Figs. 3.23 through 3.26 that while C_{12} and C_{22} are relatively temperature independent, C_{12} and C_{22} are temperature depended. This fact can be used to simply the charge extraction.

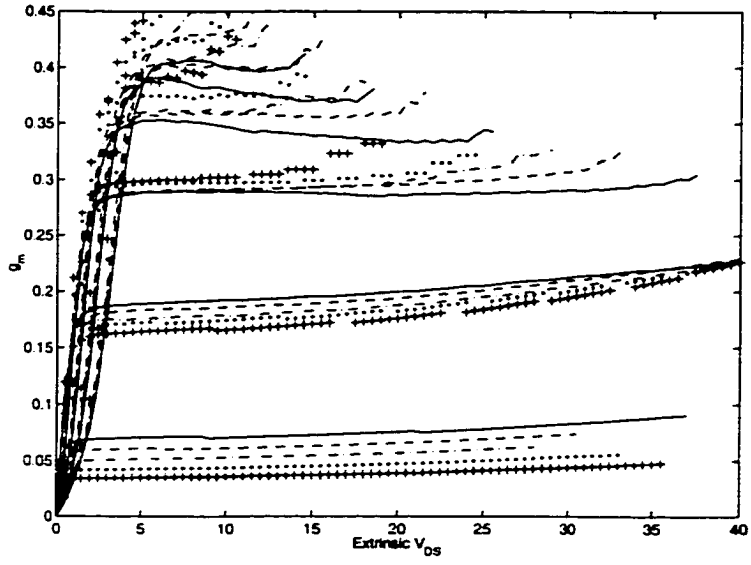


Figure 3.21: Extracted g_m for V_{GS} = 4V (lowest set of curves) to 6.5V (highest set of curves) in steps of 0.5V for different $T_{dev,avg}$: $T_{dev,avg}$ = 105°C (solid lines), $T_{dev,avg}$ = 90°C (dashed lines), $T_{dev,avg}$ = 75°C (dashed dotted lines), $T_{dev,avg}$ = 60°C (dotted lines) and $T_{dev,avg}$ = 45°C (plus signs)

Finally, Figs. 3.27 and 3.28 show the variation in the raw extracted τ_G and τ_D as function of device temperature over all measured bias points.

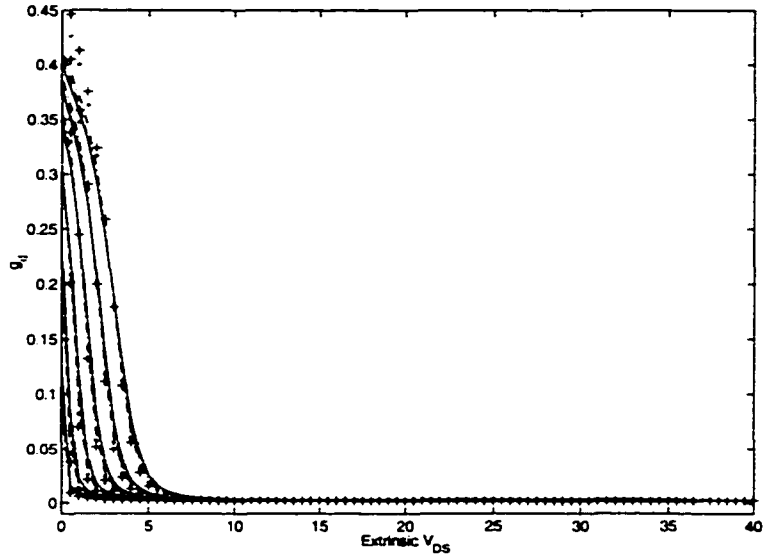


Figure 3.22: Extracted g_d for V_{GS} = 4V to 6.5V in steps of 0.5V for different $T_{dev,avg}$: $T_{dev,avg}$ = 105°C (solid lines), $T_{dev,avg}$ = 90°C (dashed lines), $T_{dev,avg}$ = 75°C (dashed dotted lines), $T_{dev,avg}$ = 60°C (dotted lines) and $T_{dev,avg}$ = 45°C (plus signs)

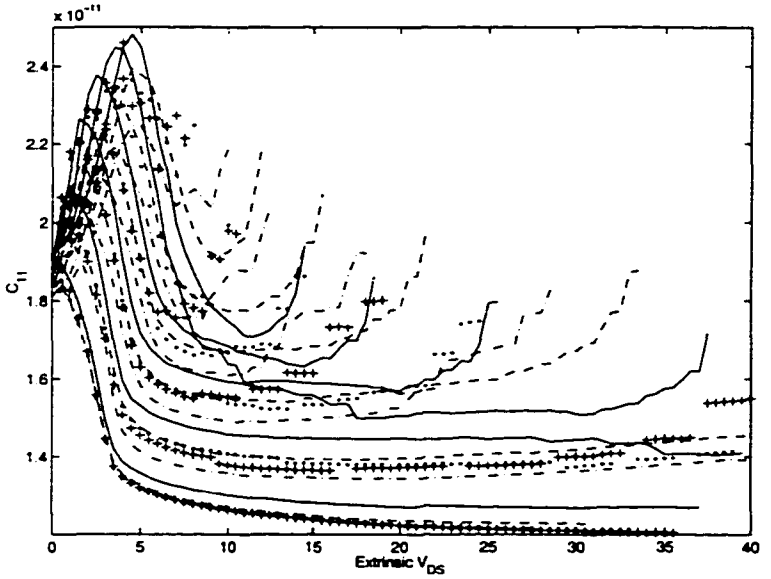


Figure 3.23: Extracted C_{11} for V_{GS} = 4V (lowest set of curves) to 6.5V (highest set of curves) in steps of 0.5V for different $T_{dev,avg}$: $T_{dev,avg}$ = 105°C (solid lines), $T_{dev,avg}$ = 90°C (dashed lines), $T_{dev,avg}$ = 75°C (dashed dotted lines), $T_{dev,avg}$ = 60°C (dotted lines) and $T_{dev,avg}$ = 45°C (plus signs)

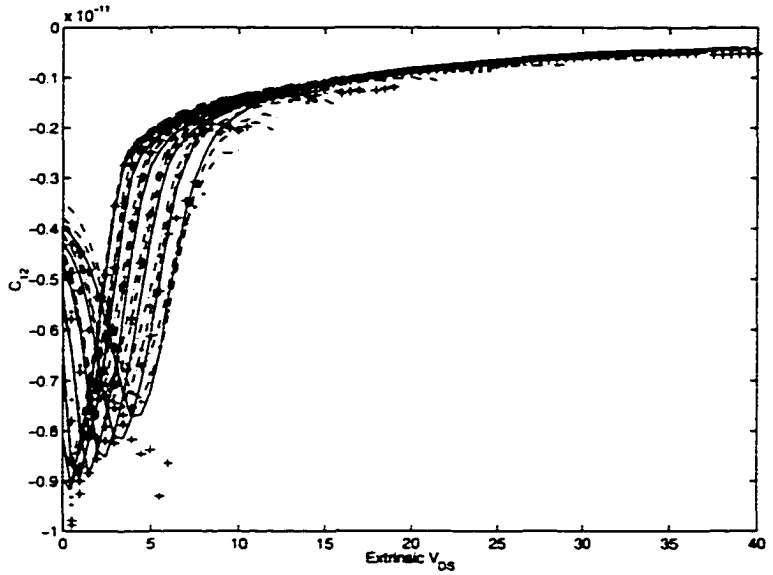


Figure 3.24: Extracted C_{12} for V_{GS} = 4V (highest set of curves) to 6.5V (lowest set of curves) in steps of 0.5V for different $T_{dev,avg}$: $T_{dev,avg}$ = 105°C (solid lines), $T_{dev,avg}$ = 90°C (dashed lines), $T_{dev,avg}$ = 75°C (dashed dotted lines), $T_{dev,avg}$ = 60°C (dotted lines) and $T_{dev,avg}$ = 45°C (plus signs)

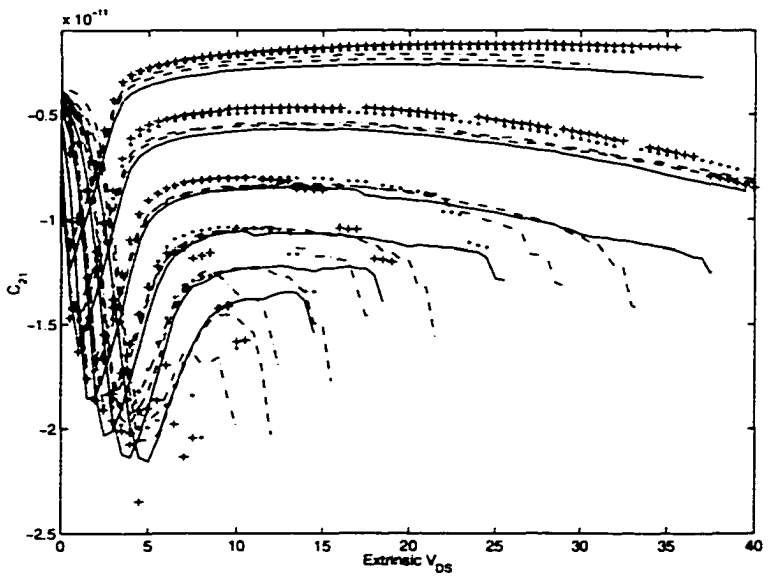


Figure 3.25: Extracted C_{21} for V_{GS} = 4V (highest set of curves) to 6.5V (lowest set of curves) in steps of 0.5V for different $T_{dev,avg}$: $T_{dev,avg}$ = 105°C (solid lines), $T_{dev,avg}$ = 90°C (dashed lines), $T_{dev,avg}$ = 75°C (dashed dotted lines), $T_{dev,avg}$ = 60°C (dotted lines) and $T_{dev,avg}$ = 45°C (plus signs)

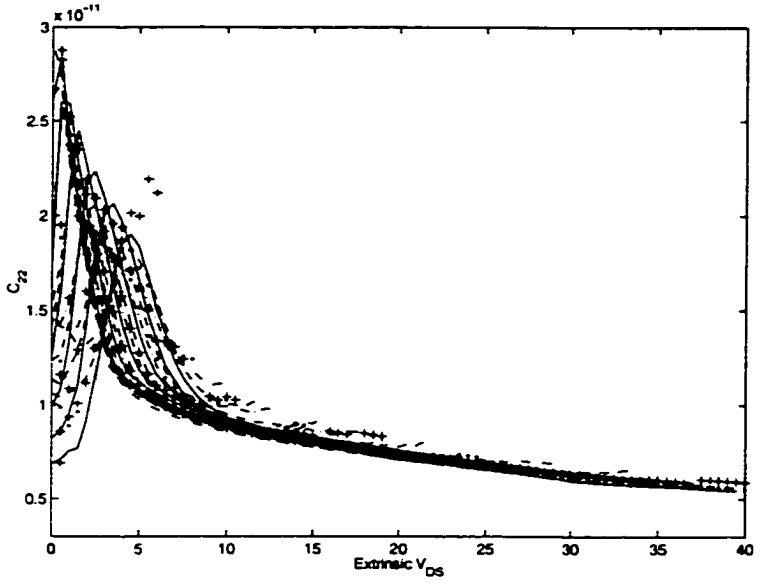


Figure 3.26: Extracted C_{22} for V_{GS} = 4V (lowest set of curves) to 6.5V (highest set of curves) in steps of 0.5V for different $T_{dev,avg}$: $T_{dev,avg}$ = 105°C (solid lines), $T_{dev,avg}$ = 90°C (dashed lines), $T_{dev,avg}$ = 75°C (dashed dotted lines), $T_{dev,avg}$ = 60°C (dotted lines) and $T_{dev,avg}$ = 45°C (plus signs)

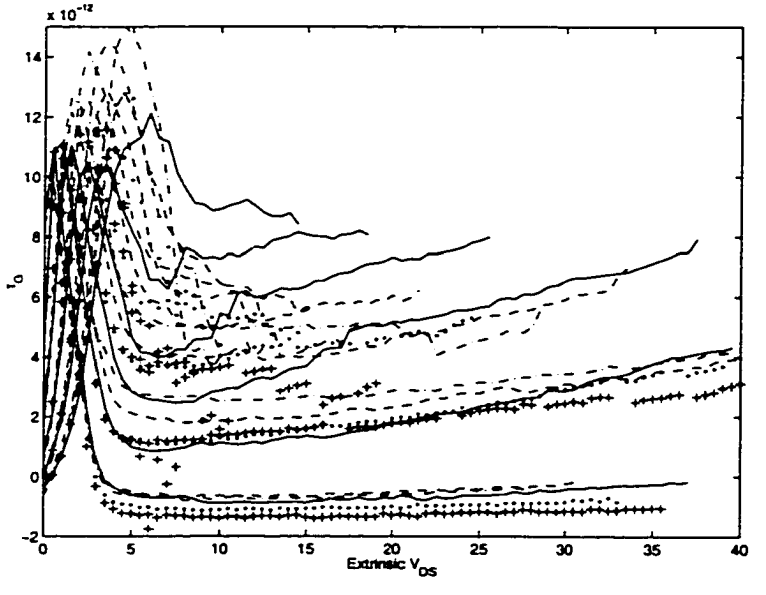


Figure 3.27: Extracted τ_G for V_{GS} = 4V (lowest set of curves) to 6.5V (highest set of curves) in steps of 0.5V for different $T_{dev,avg}$: $T_{dev,avg}$ = 105°C (solid lines), $T_{dev,avg}$ = 90°C (dashed lines), $T_{dev,avg}$ = 75°C (dashed dotted lines), $T_{dev,avg}$ = 60°C (dotted lines) and $T_{dev,avg}$ = 45°C (plus signs)

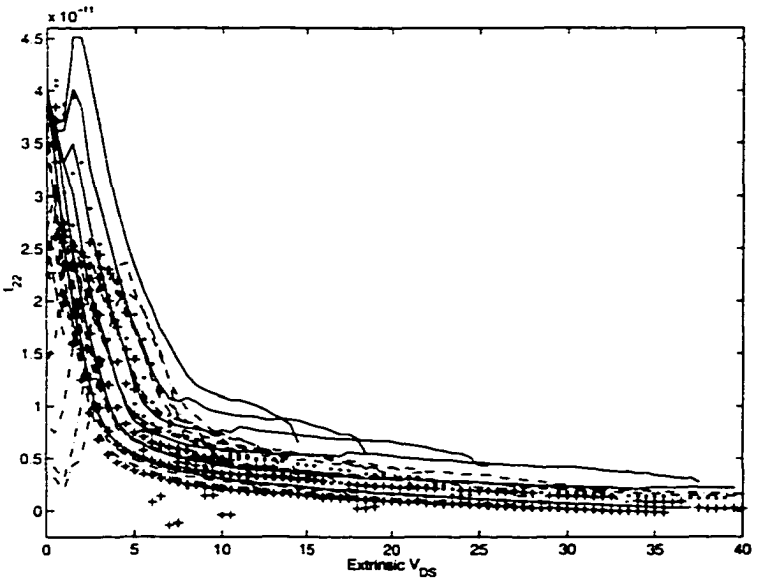


Figure 3.28: Extracted τ_D for V_{GS} = 4V (lowest set of curves) to 6.5V (highest set of curves) in steps of 0.5V for different $T_{dev,avg}$: $T_{dev,avg}$ = 105°C (solid lines), $T_{dev,avg}$ = 90°C (dashed lines), $T_{dev,avg}$ = 75°C (dashed dotted lines), $T_{dev,avg}$ = 60°C (dotted lines) and $T_{dev,avg}$ = 45°C (plus signs)

CHAPTER 4

Large Signal Modeling and Model Implementation and Verification

A model suitable for DC and RF simulations of MOSFETs has been presented and verified on a physical device simulator. DC, thermal and small signal extraction over a wide bias and temperature range have been performed on measured data for a LDMOSFET device. This Chapter is focused on the large signal modeling of the LDMOSFET. In particular, issues related to the difference between iso-thermal and pulsed IVs will be considered so as to extract a large signal model. The extracted model by-passes the need for using pulsed IV, pulsed RF measurements and is implemented and compared with measured results and the existing MET model.

4.1 Iso-thermal and Pulsed IVs

While iso-thermal IVs predict the DC biasing of an amplifier, the pulsed IVs $I_{D,tran}(v_{GS}, v_{DS}, V_{GS}, V_{DS}, T_{dev,avg})$ are the effective IVs followed by a power amplifier

under RF drive. Iso-thermal IVs and pulsed IVs agree at the bias point V_{GS},V_{DS},$T_{dev,avg}$. Both pulsed and iso-thermal IVs are important in understanding the behavior of RF circuits such as power amplifiers. In such a circuit, the iso-thermal IV establishes the device bias point, while the pulsed IVs are an indication of the device response under RF drive. As the RF power output increases, non-linearities will cause the device operating point and temperature to change. Hence a new iso-thermal IV (one with a different $T_{dev,avg}$), establishes the new bias point and a different pulsed IV predicts the RF behavior.

Transient IVs are measured by first biasing the device and then applying short voltage pulses (typically 1ns) at the gate and drain. The duty cycle of the pulses is kept low (around 1 %) so as to prevent the device from heating up. A pulse IV measurement system under computer control is given in Fig. 4.1.

The pulsed IV system is used to acquire pulsed IVs for a cold LDMOSFET (biased at V_{DS} = 0V and V_{GS} = 0V) for T_{sub} values from 45°C to 105°C is steps of 15°C. Since the device is cold, $T_{dev,avg}$ will equal T_{sub}. Under such a measurement condition, very little temperature gradient is expected in the device. The obtained pulsed IV are deembedded of the parasitic resistances to give the intrinsic pulsed IVs. This process skews the gate voltage, which becomes a function of the drain current due to the presence of R_s. Hence for a meaningful comparison to be made with iso-thermal IVs, the pulsed IVs need to be fitted and computed over the voltages of the iso-thermal

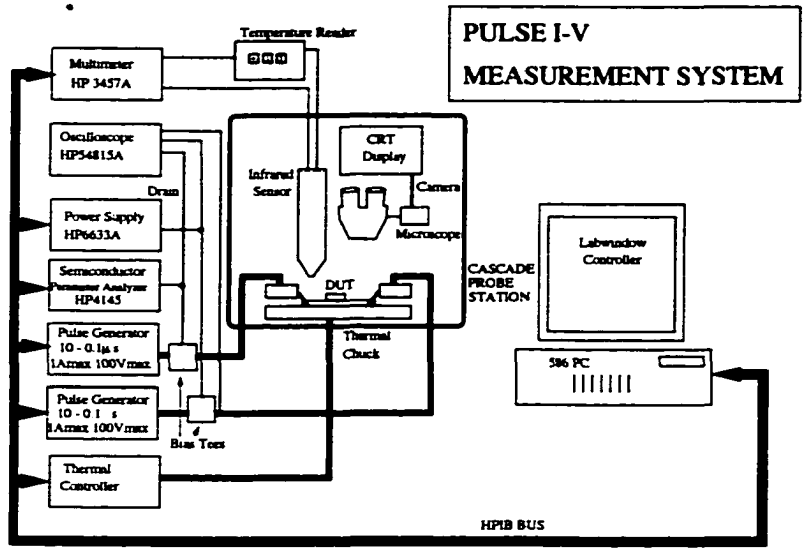


Figure 4.1: Pulse IV measurement setup

IVs (themselves skewed by the parasitics). 2D TPS techniques are used to perform this procedure.

Further it is desired to compare cold pulsed measurements with those obtained under DC bias. For biasing these hot measurements, T_{sub} is set at 35°C, V_{DS} is set at 20V and V_{GS} is adjusted until the desired device temperature is reached. Pulsed IVs are then acquired. Such a measurement condition will cause a substantial temperature gradient in the device. Bias points corresponding to the temperature values specified earlier are used. Again a refit is necessary so as to make a comparison with cold pulsed IVs and iso-thermal IVs.

Figs. 4.2 compares the obtained intrinsic iso-thermal (solid lines), cold pulsed IVs (dashed lines) and hot pulsed IVs (dash dotted) for a $T_{dev,avg}$ of 105°C. For this figure,

the intrinsic V_{GS} is from 4V to 6.5V in steps of 0.5V such that ◁ denotes V_{GS} = 4V, ▫ denotes V_{GS} = 4.5V, ◇ denotes V_{GS} = 5V, ▷ denotes V_{GS} = 5.5V, ○ denotes V_{GS} = 5.5V, and △ denotes V_{GS} = 6V. Fig. 4.3 compares the three IVs using the same plot line style for $T_{dev,avg}$ of 90°C, 75°C, 60°C and 45°C respectively.

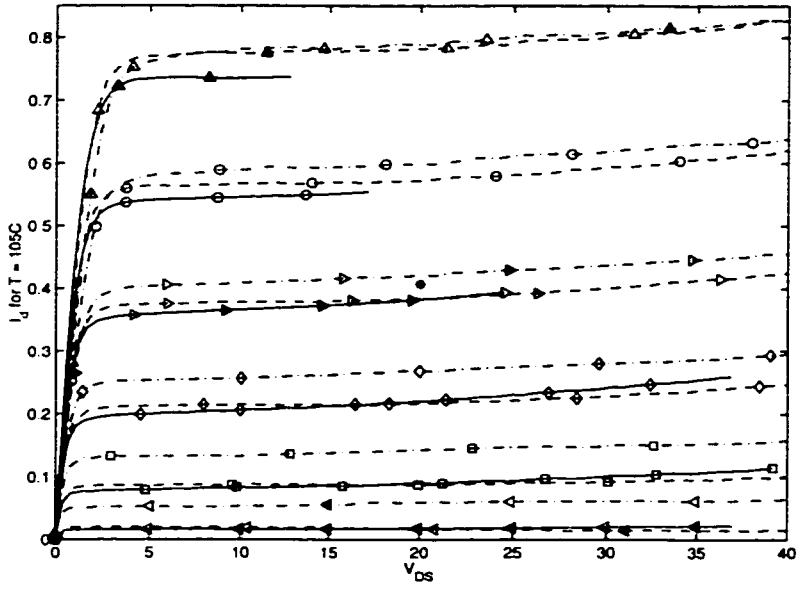


Figure 4.2: Comparison between iso-thermal IV (solid lines), cold pulsed IV (dashed lines) and hot pulsed IV (dash dotted line) for $T_{dev,avg}$ is 105°C. Star denotes bias point used for hot pulsed IV. V_{GS} ranges from 4V to 6.5V in steps of 0.5V.◁ denotes V_{GS} = 4V, ▫ denotes V_{GS} = 4.5V, ◇ denotes V_{GS} = 5V, ▷ denotes V_{GS} = 5.5V, ○ denotes V_{GS} = 5.5V, and △ denotes V_{GS} = 6V

From Figs. 4.2 and 4.3 a couple of points can be be observed. The iso-thermal and cold pulsed IVs agree well at low currents. However at high gate source voltage there can be considerable departure between the two. Both of these points are seemingly device temperature independent. This could be perhaps as a result of the small

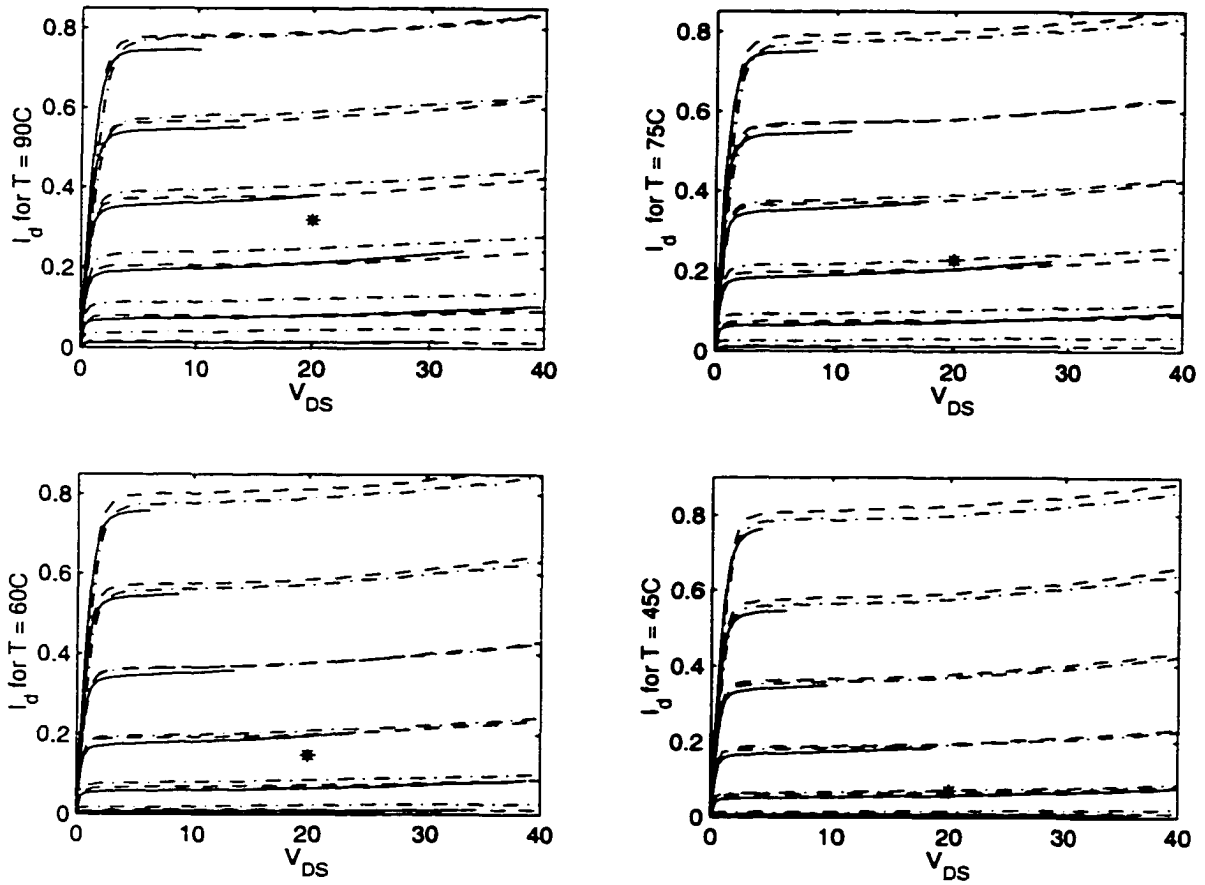


Figure 4.3: Comparison between iso-thermal IV (dashed lines), cold pulsed Iv (solid lines) and hot pulsed IV (dash dotted line) for $T_{dev,avg}$s of 90°C, 75°C, 60°C and 45°C. Star denotes bias point used for hot pulsed IV. V_{GS} ranges from 4V to 6.5V in steps of 0.5V

temperature gradient that may exist in the device in the regions of agreement. For a cold pulsed IV, $T_{dev,avg}$ is equal to T_{sub}. For an iso-thermal IV at low currents, $T_{dev,avg}$ is closer to T_{sub}, but $T_{dev,avg}$ and T_{sub} get further apart at high current and high drain source voltage.

The hot and cold pulsed IVs differ quite bit, however these differences exhibit temperature dependence. For high temperature and high gate source voltage, the two agree well, but depart substantially at low gate source voltage. In particular, there almost appears to be a threshold shift between the two. For low temperature, there is better agreement at low and medium gate source voltage, while there is greater departure at high gate source voltages. Hence for these temperature and voltage ranges, all three IVs agree fairly well.

In order to gain further insight, it is worth while comparing the extracted microwave g_m ($g_{m,RF}$) with the g_m obtained through differentiating the iso-thermal IV ($g_{m,iso}$), the cold pulsed ($g_{m,cp}$) and the hot pulsed ($g_{m,hp}$) IVs. Figs. 4.4 to 4.6 compare the extracted microwave g_m (circles) with the g_m from the iso-thermal IV (solid lines) and the cold pulsed IVs (dashed lines) for $T_{dev,avg}$ of 105°C, 90°C and 60°C respectively. For these figures, V_{GS} extrinsic is from 4V to 6V in steps of 0.25V.

From Figs. 4.4 to 4.6 it can be observed that $g_{m,RF}$ microwave agrees well with $g_{m,iso}$ and $g_{m,cp}$ at low gate source voltages. At higher gate source voltages, $g_{m,RF}$ microwave agrees well only $g_{m,iso}$ and not $g_{m,cp}$. Another interesting point is that $g_{m,RF}$ and $g_{m,iso}$ agree well over all temperature at low drain source voltages, but depart at higher drain source voltages over all temperatures. This is indicative of low frequency dispersion arising from other than thermal effects.

Figs. 4.7 to 4.9 compare the extracted microwave g_m ($g_{m,RF}$) (circles) with the g_m from the iso-thermal IV (solid lines) and g_m from the the hot pulsed IVs ($g_{m,hp}$) (dash

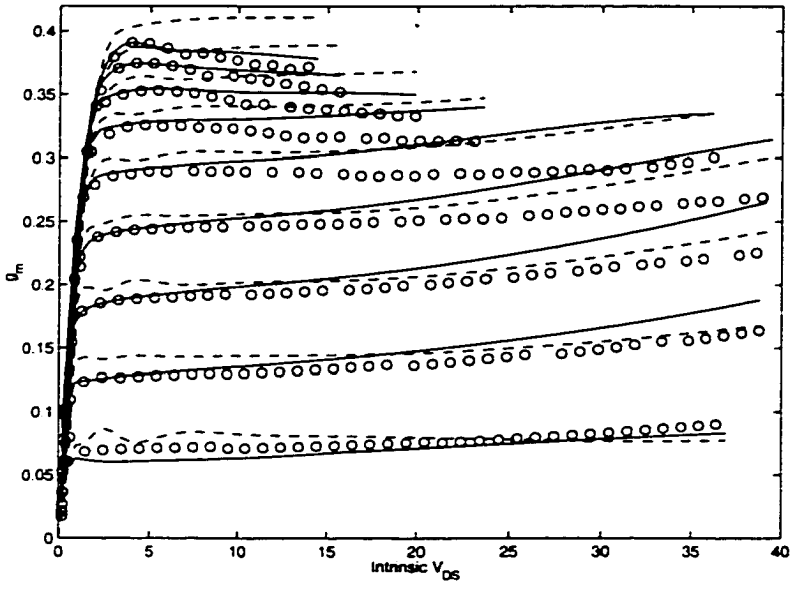


Figure 4.4: Comparison between microwave extracted $g_{m,RF}$ (circles) with $g_{m,DC}$ (solid lines) and $g_{m,cp}$ (dashed lines) for $T_{dev,avg}$ of 105°C. V_{GS} ranges from 4V (lowest curve) to 6V (highest curve) in steps of 0.5V

dotted lines) for $T_{dev,avg}$ of 105°C, 90°C and 60°C respectively. For these figures, V_{GS} extrinsic is from 4V to 6V in steps of 0.25V.

From Figs. 4.7 to 4.9 it can be observed that for 90°C, $g_{m,RF}$ and $g_{m,hp}$ are agree quite well. However for lower temperatures, such as 60°C the agreement is quite off. For higher temperatures, such as 105°C, there is a better agreement between the two. From Figs 4.8, it can be seen that at higher V_{DS} values, the $g_{m,iso}$ begin to depart from $g_{m,RF}$, while $g_{m,hp}$ continues to agree well, indicating the presence of low frequency dispersion.

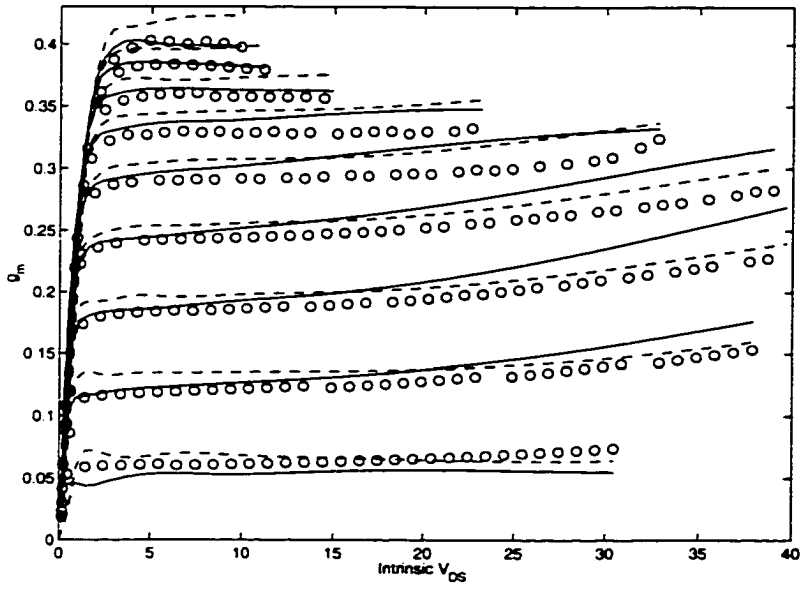


Figure 4.5: Comparison between microwave extracted $g_{m,RF}$ (circles) with $g_{m,DC}$ (solid lines) and $g_{m,cp}$ (dashed lines) for $T_{dev,avg}$ of 90°C. V_{GS} ranges from 4V (lowest curve) to 6V (highest curve) in steps of 0.5V

From the analysis presented earlier, it is safe to conclude that the LDMOSFET does indeed suffer from some dispersion effects. Further it can be concluded that the $g_{m,iso}$ does globally over all temperatures considered agree better with $g_{m,RF}$ than does the $g_{m,cp}$ and $g_{m,hp}$. It is true that $g_{m,hp}$ is what gives the device RF loadline. But because this quantity is bias depended and the bias of the device will change under RF drive, to make use of this would be very difficult.

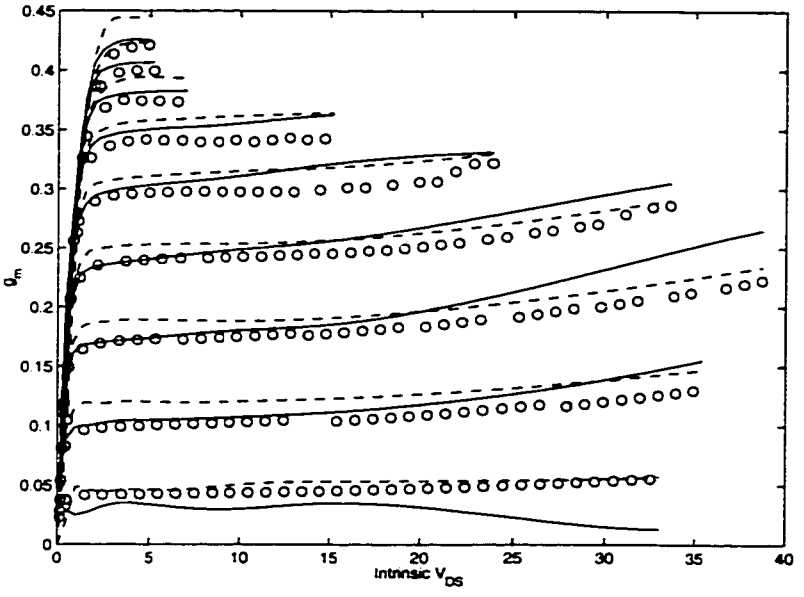


Figure 4.6: Comparison between microwave extracted $g_{m,RF}$ (circles) with $g_{m,DC}$ (solid lines) and $g_{m,cp}$ (dashed lines) for $T_{dev,avg}$ of 60°C. V_{GS} ranges from 4V (lowest curve) to 6V (highest curve) in steps of 0.5V

4.2 Modeling Details

In light of the discussion presented earlier, the strategy for developing the electro-thermal model will involve simplifying the earlier presented large signal model in Fig. 2.7 by removing the floating base parasitic transistor. The iso-thermal IV will be fitted together with the extracted microwave $g_{m,RF}$ and $g_{d,RF}$ over the entire bias and temperature range using 3D TPS. Hence the IV, $g_{m,RF}$ and $g_{d,RF}$ will be functions of both drain source and gate source voltage and device temperature, to be computed

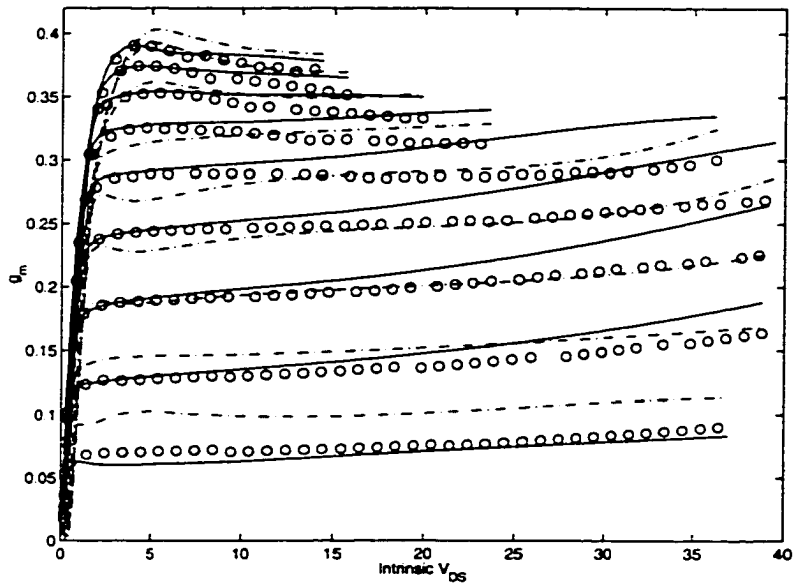


Figure 4.7: Comparison between microwave extracted $g_{m,RF}$ (circles) with $g_{m,DC}$ (solid lines) and $g_{m,hp}$ (dash dotted lines) for $T_{dev,avg}$ of 105°C. V_{GS} ranges from 4V (lowest curve) to 6V (highest curve) in steps of 0.5V

by the thermal subcircuit. Using 3D Tensor Product Splines (TPS), a function of three variables can be represented as:

$$S(V_{GS}, V_{DS}, T_{DEV}) = \sum_{i=1}^{m}\sum_{j=1}^{n}\sum_{l=1}^{p} a_{ijk}\ B_{i,k_{GS},t_{GS}}(V_{GS})B_{j,k_{DS},t_{DS}}(V_{DS})\ B_{l,k_{DEV},t_{DEV}}(T_{DEV}) \quad (4.1)$$

From Chapter 3, it was observed that C_{12} and C_{22} are relatively temperature independent, C_{12} and C_{22} are temperature depended. In order to simplify the large signal model, the 60°C C_{12} and C_{22} are used and the charge is made device temperature independent. This can be justified given the still comparatively small temperature variation in capacitance, given their large values (in the order of 10^{-11}F). However,

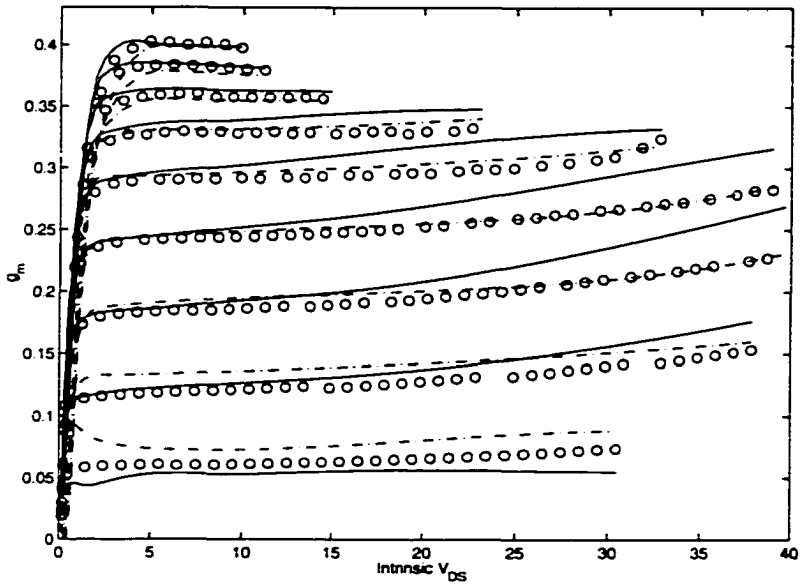


Figure 4.8: Comparison between microwave extracted $g_{m,RF}$ (circles) with $g_{m,DC}$ (solid lines) and $g_{m,hp}$ (dash dotted lines) for $T_{dev,avg}$ of 90°C. V_{GS} ranges from 4V (lowest curve) to 6V (highest curve) in steps of 0.5V

what this will mean is that at higher RF power, as the device temperature increases substantially, the accuracy of the model will begin to degrade.

A further simplification is made to average out the NQS times such that 1ps is used for the gate charge and 0.1ps for the drain charge. Since the NQS times have most impact at frequencies approaching f_{max}, this should have a relatively small impact on the model.

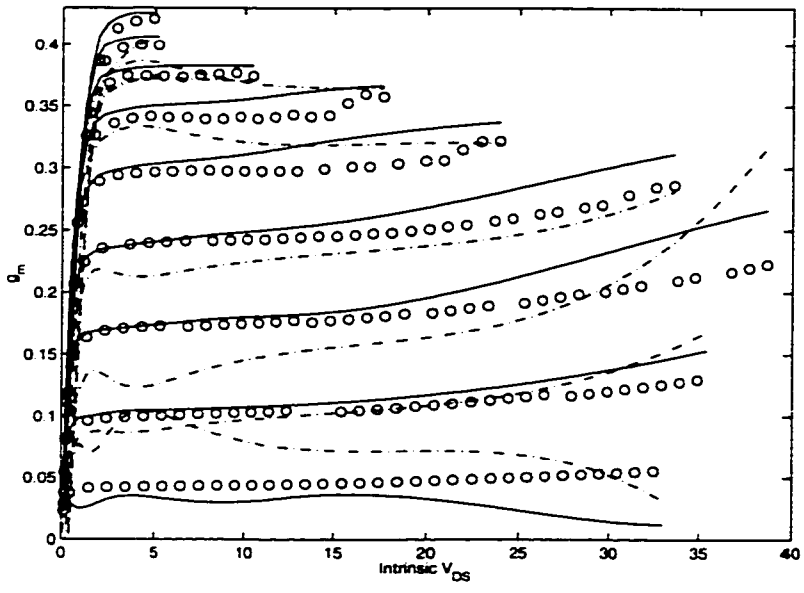


Figure 4.9: Comparison between microwave extracted $g_{m,RF}$ (circles) with $g_{m,DC}$ (solid lines) and $g_{m,hp}$ (dash dotted lines) for $T_{dev,avg}$ of 60°C. V_{GS} ranges from 4V (lowest curve) to 6V (highest curve) in steps of 0.5V

4.3 Data Extrapolation

Because the method used to measure iso-thermal s-parameters does not give data for high gate and drain voltages, small signal data is unavailable in this region. Ideally, a pulsed DC and pulsed RF technique can be used to access this region. However, in the absence of the equipment needed to perform these measurements, other approaches have to be considered.

In this work, data extrapolation of the small signal parameters has been used. The drain conductance, g_d, is assumed to be constant over the missing V_{DS} range, holding its minimum value for the particular gate voltage. The extrapolation on

g_m is similar, with the exception that the minimum value for V_{DS} greater than 5V has been used. Both C_{21} and C_{22} are observed to have small variation with V_{GS} for high V_{DS}. This fact has been used to perform a polynomial fit on the last few data points available for a given V_{GS}. These functions are then used to extrapolate into the missing data region. The value of C_{11} is assumed to be constant over the missing V_{DS} range, holding its minimum value for the particular gate voltage, for V_{DS} greater than 5 V. The same approach has been used for extrapolating C_{22}, except that it is made to hold its maximum value for each gate voltage for V_{DS} greater than 5V.

At first glance, it may appear that such an extrapolation can not do justice to the accuracy intended for the model. Although this in general is true, it is important to understand exactly how the model may be used in a power amplifier simulation. For a PA, the device is generally biased on a DC load-line at high V_{DS} and low V_{GS}. For higher classes of operation, V_{GS} is near, at, or below threshold. From a RF point of operation, the device will never really enter those regions of the IVs that have been assembled by extrapolating data. Hence while this region is important from the point of view of continuity in the model, it need not be accurately modeled to predict device performance under RF drive.

4.4 Large Signal Model Implementation

4.4.1 Parameter Extraction

Fig. 2.7 shows the large signal model topology proposed for this work. The large signal representations can be obtained from the extracted small signal model parameters using the following equations:

$$
\begin{aligned}
& I_{D,trans}(v_{GS}, v_{DS}, V_{GS}, V_{DS}, T_{dev}) = \int g_{21}(V_{GS}, V_{DS}, T_{dev})dV_{GS} + \int g_{22}(V_{GS}, V_{DS}, T_{dev})dV_{DS} \\
& \text{with} \quad I_{D,trans}(V_{GS}, V_{DS}, V_{GS}, V_{DS}, T_{dev}) \simeq I_D(V_{GS}, V_{DS}, T_{sub}) \\
& Q_G(v_{GS}, v_{DS}) = \int C_{11}(V_{GS}, V_{DS})dV_{GS} + \int C_{12}(V_{GS}, V_{DS})dV_{DS} \\
& Q_D(v_{GS}, v_{DS}) = \int C_{21}(V_{GS}, V_{DS})dV_{GS} + \int C_{22}(V_{GS}, V_{DS})dV_{DS}
\end{aligned}
\tag{4.2}
$$

The extracted small signal parameters are fitted using an optimized 3D Tensor Product B-Splines technique. Use of this technique that optimizes the B-Spline knot placements, is necessary light of the steep knee in the intrinsic device drain current. Non optimized Tensor Product B-Splines are unable to handle this region and give rise to oscillatory behavior.

In the optimized knot placement technique, an error function is computed to determine how close a fit is to original data. The knot placement is then readjusted so that the knot concentration in the higher error region is increased, while reducing the concentration in the lower error region. Note that the overall number of knots in a particular bias direction (in this case, V_{DS}) are kept the same. It is only the knot

distribution that is changed. With every new distribution, the error is recomputed and a decision is made whether to accept the new placement or not. The process continues until an optimum placement is found. This is then used for all other quantities.

4.4.2 Current

By integrating the $g_{m.RF}$ and $g_{d,RF}$ and simultaneously fitting the iso-thermal IV over all temperature, a 3D representation of these functions can be obtained. Figs. 4.10 and 4.11 show the fits of the intrinsic g_m and g_d at a device temperature of 90°C. The circles give the extracted values from the small signal analysis. Fig. 4.12 shows the 3D TPS represented iso-thermal IV at a $T_{dev,avg}$ of 90°C (solid lines) compared with measured values (circles).

Figs. 4.13 and 4.14 shows the 3D represented $g_{m,RF}$ and iso-thermal IV as a function of $T_{dev,avg}$ (solid lines) respectively. The circles in Fig. 4.13 are the extracted g_m while those in Fig. 4.14 are the measured iso-thermal current. Both figures are for a V_{DS} of 10V and V_{GS} ranges from 4V to 6.5V in steps of 0.25V.

4.4.3 Charge

The integration of C_{11} and C_{12} yields the gate charge, while the integration of C_{21} and C_{22} yields the drain charge. Figs. 4.15 and 4.16 show the fitted C_{11} and C_{12} respectively. The bottom portion of Fig. 4.16 zooms into the low V_{DS} region to

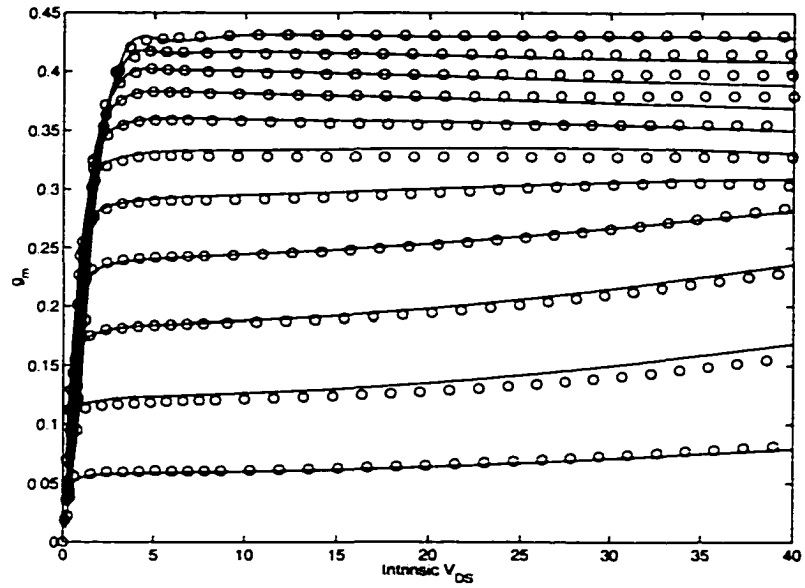


Figure 4.10: Comparison of 3D TPS fitted g_m (solid lines) with values extracted from the small signal fit (circles) for $T_{dev,avg}$ of 90°C. V_{GS} ranges from 4V (lowest curve) to 6.5V (highest curve) in steps of 0.25V

highlight the fit. The solid lines are the TPS fitted data, while the circles are values extracted from the small signal fit. V_{GS} ranges from 4V to 6.25V in steps of 0.25V. Note that the extrapolation scheme discussed earlier has been used on the capacitance data. Further, the temperature dependency of the capacitance has been neglected, as discussed earlier.

The TPS extracted gate charge is given Fig. 4.17.

Figs. 4.18 and 4.19 show the fitted C_{21} and C_{22} respectively in a manner similar to that used to plot the previous capacitance fits. The solid lines are the TPS fitted

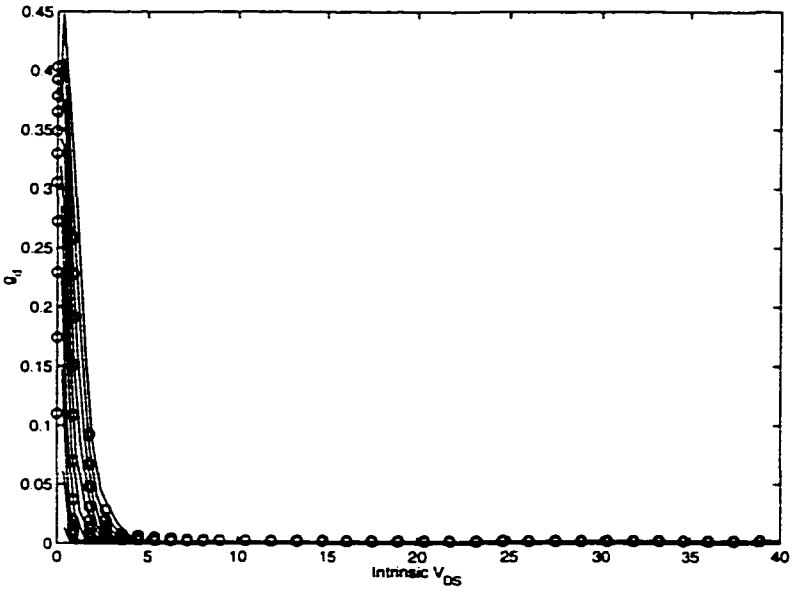


Figure 4.11: Comparison of 3D TPS fitted g_d (solid lines) with values extracted from the small signal fit (circles) for $T_{dev,avg}$ of 90°C. V_{GS} ranges from 4V to 6.5V in steps of 0.25V

data, while the circles are values extracted from the small signal fit. The extracted drain charge is given in Fig. 4.20

4.5 Model Incorporation in ADS

After obtaining representations for all elements in the large signal model given in Fig. 2.7, the model is implemented as a user defined model in ADS. A model data file in generated in MATLAB. The data file contains the TPS order, knots and coefficient values, such that each column is associated with a different element of

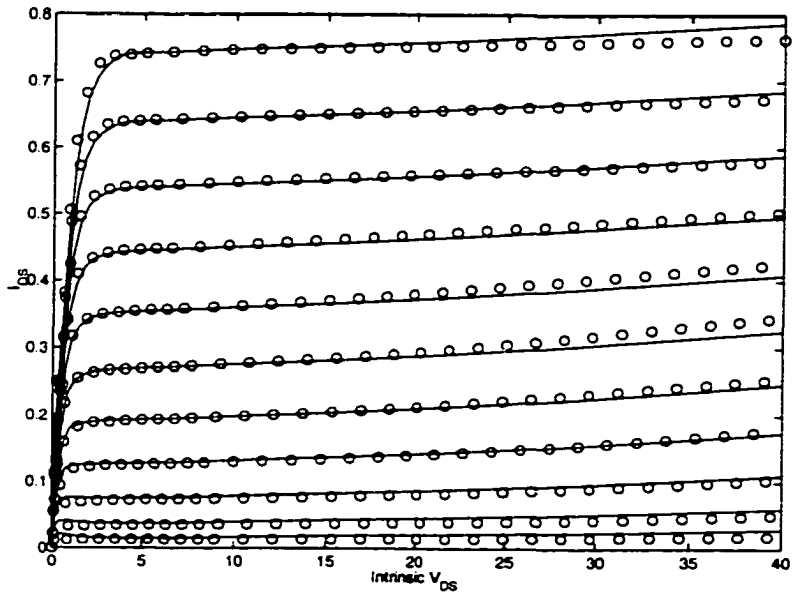


Figure 4.12: Comparison of 3D TPS fitted $I_{D,iso}$ (solid lines) with measured values (circles) for $T_{dev,avg}$ of 90°C. V_{GS} ranges from 4V (lowest curve) to 6.5V (highest curve) in steps of 0.25V

the large signal model. The model in ADS reads this file, decodes it, and uses it to compute the associated functional and derivative values for a given bias point.

The model has been implemented in ADS with two simplifications. Firstly, the parasitic bi-polar has been removed to reflect the low level of dispersion in the LD-MOSFET. Secondly, it is assumed that the charge elements are temperature independent so as to reduce the complexity associated with implementing the model.

While the parasitic resistances are included in the model, the parasitic inductances are attached externally. For some unknown reason ADS has convergence problems if the inductors are included in the model, yet runs fine for the same simulation on

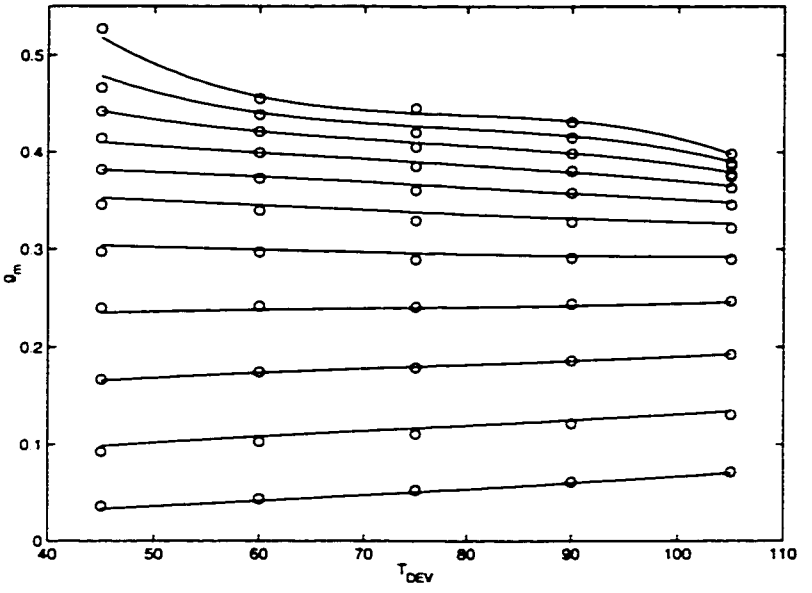


Figure 4.13: Comparison of 3D TPS fitted g_m (solid lines) with values extracted from the small signal fit (circles) for V_{DS} = 10V. V_{GS} ranges from 4V (lowest curve) to 6.5V (highest curve) in steps of 0.25V

placing the inductors externally. Additionally, for some unknown reason, the ground associated with the thermal subcircuit could not be implemented in the ADS User defined model. Hence an external pin had be used, which is attached to ground in the simulation file.

It is worth noting that HP/Agilent provides very littler documentation on user defined models in ADS. Further, earlier releases of ADS contained quite a few bugs which were reported to Agilent in the process of implementing the devopled model. Hopefully future releases of ADS will make writing user defined models easier.

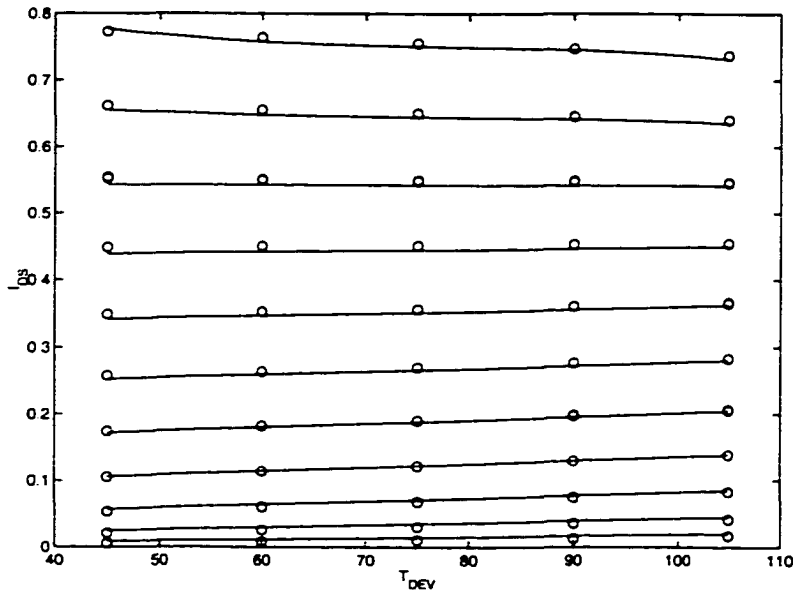


Figure 4.14: Comparison of 3D TPS fitted I_d (solid lines) with measured values (circles) for V_{DS} = 10V. V_{GS} ranges from 4V (lowest curve) to 6.5V (highest curve) in steps of 0.25V

The model implementation in ADS involves writing out the charges and currents at each node, followed by the derivatives of these elements. The derivatives are written in the form of a Jacobian matrix which gives the derivative of each element at a particular node, with all other nodes. Of course those node points on which the element value does not depend, will have a zero Jacobian entry.

ADS isolates all aspects of the model, such that the small signal AC, transient, linear, and non-linear portions are implemented separately. This in essence implies a lot of repetition in terms of reentering the same parameters using a different calling function. Of course it is essential that all these aspects of the model are consistent.

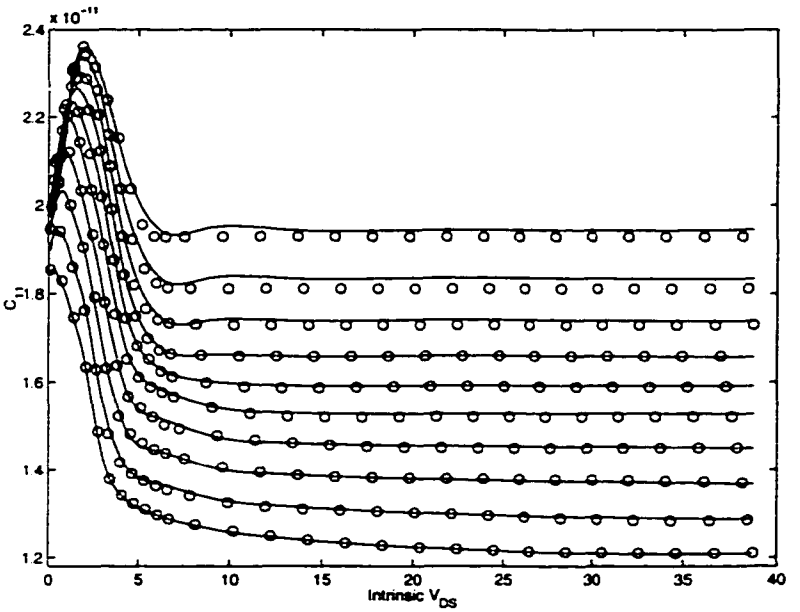


Figure 4.15: Comparison of TPS fitted C_{11} (solid lines) with values extracted from the small signal fit (circles). V_{GS} ranges from 4V (lowest curve) to 6.25V (highest curve) in steps of 0.25V

4.5.1 Out of Range Regions

One of the problem with 3D TPS is that I_{DS} is not exactly 0 for $V_{DS} = 0$V (for all V_{GS} and $T_{dev,avg}$). This is because of the fact that B-Splines only approximate a value, they can not agree exactly. It has been observed that this can lead to convergence problems in ADS. In order to address this, g_m, g_d and I_D are computed using TPS till only as low as V_{DS} of 0.3V. Below this, a quadratic approximation is used:

$$I_{DS} = a(V_{GS}, T_{dev,avg})V_{DS}^2 + b(V_{GS}, T_{dev,avg})V_{DS} \tag{4.3}$$

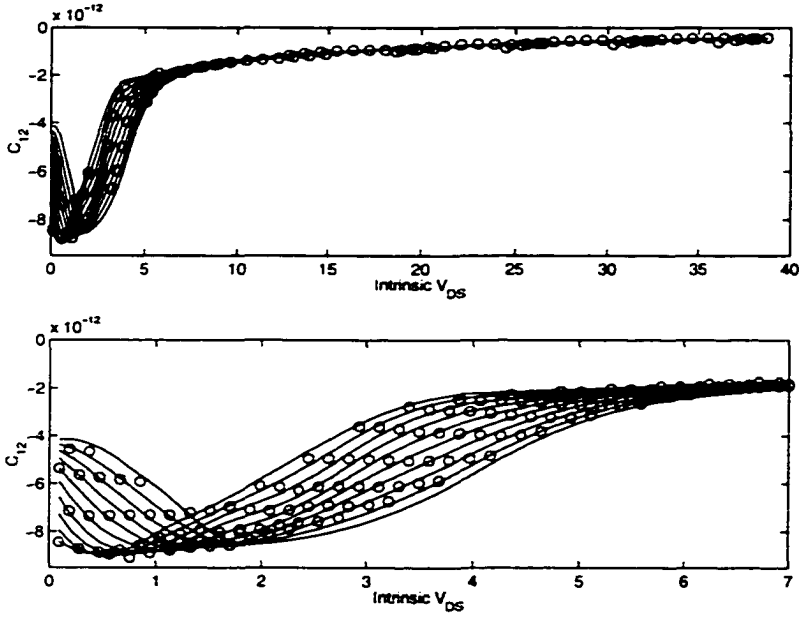


Figure 4.16: Comparison of TPS fitted C_{12} at a $T_{dev,avg}$ (solid lines) with values extracted from the small signal fit (circles). V_{GS} ranges from 4V (highest curve) to 6.25V (lowest curve) in steps of 0.25V

where a and b are temperature and gate source voltage dependent and are computed so that there is continuity in current and g_d. This ensures continuity in g_m and g_t.

When V_{DS} exceeds $V_{max,drain}$ (which is about 40V), g_d is assumed to hold it's value at $V_{max,drain}$. Similarly when V_{GS} exceeds $V_{max,gate}$ (which is about 6.5V), g_m is assumed to hold it's value at $V_{max,gate}$. Like wise when $T_{dev,avg}$ goes below it's minimum value of 45°C or above it's maximum value of 105°C, g_t (the derivative of the drain current with respect to the device temperature) is held to it's value at 45°C or 105°C accordingly.

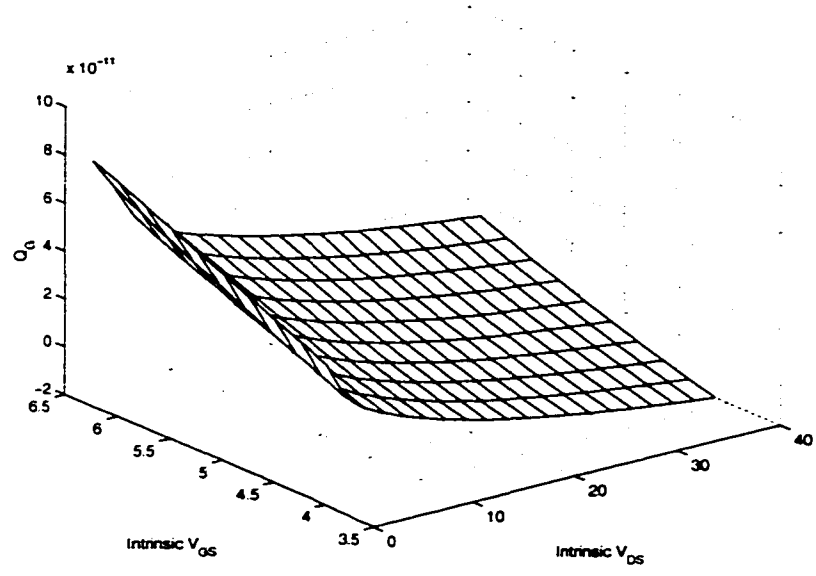


Figure 4.17: TPS extracted gate charge

For V_{DS} less than 0, the device is assumed symmetric. This is not entirely correct, since for negative voltages, the drain and source are switched. However, given the fact that the maximum swing for a power amplifier is between V_{knee} to $2V_{DD}$, this region will not be entered into by the amp. Hence while such an approximation guarantees continuity, it does not provide for accuracy.

4.5.2 Threshold voltage

For the LDMOS implemented in ADS, V_{GS} data has been gathered from 4V to 6.5V. Based upon threshold measurements, V_{th} was determined to be around 3.8V. It

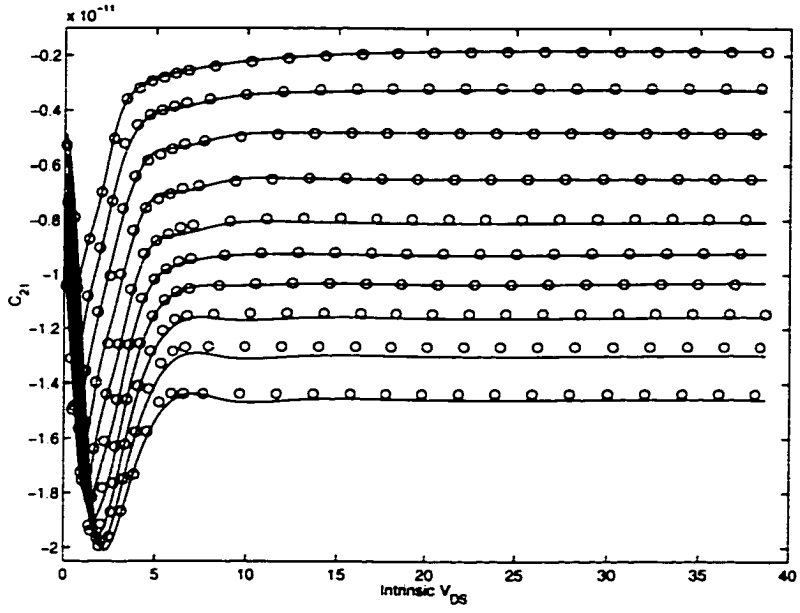


Figure 4.18: Comparison of TPS fitted C_{21} (solid lines) with values extracted from the small signal fit (circles). V_{GS} ranges from 4V (highest curve) to 6.25V (lowest curve) in steps of 0.25V

is essential for the region below 4V to be modeled well in ADS, for this is the region where clipping will occur in a power amplifier under RF drive.

This region has been modeled by using an exponential function such that there is no slope discontinuity from the B-Splines to the exponential function. Then for V_{GS} less than 4V:

$$I_{DS} = I_{DS}(V_{GS} = 4V, V_{DS}) e^{\left[\frac{g_m(V_{GS}=4V,V_{DS})}{I_{DS}(V_{GS}=4V,V_{DS})}(V_{GS}-4)\right]} \tag{4.4}$$

Fig. 4.21 shows the measured drain current for a constant drain voltage of 15V, while sweeping the gate voltage from 3 to 6.5V in a DC simulation on ADS. The

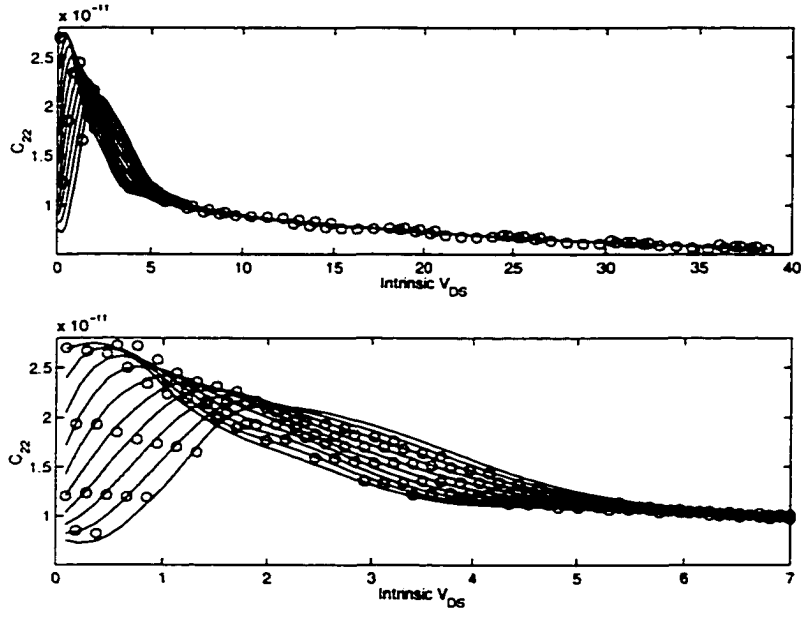


Figure 4.19: Comparison of TPS fitted C_{22} at a $T_{dev,avg}$ (solid lines) with values extracted from the small signal fit (circles). V_{GS} ranges from 4V (lowest curve) to 6.25V (highest curve) in steps of 0.25V

figure clearly shows the ability of the model to handle sub threshold current, while maintaining continuity, and compares with measured results. For a power amplifier simulation, the exact current value in this region is not as critical as the need for continuity in functional and derivative values.

A complete DC IV simulation on ADS is carried out. The results agree with those obtained from the optimized Tensor Product B-Splines extraction on MATLAB. This step is used to confirm that the ADS model is properly handling the Tensor Product B-spline data table associated with the current element in the large signal model.

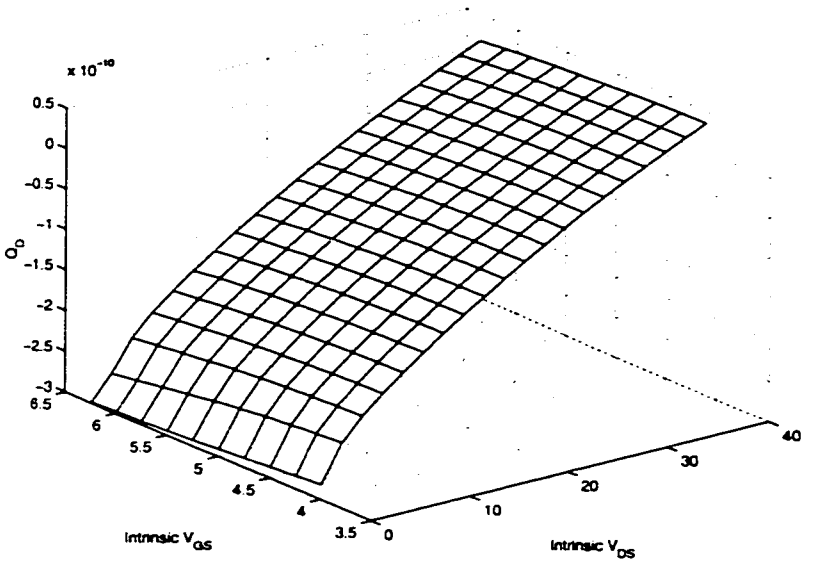


Figure 4.20: TPS extracted drain charge

4.6 Power Amplifier Design and Testing

A power amplifier was designed with a fully balanced input and output matching network [61] using microstrip transmission lines. The amplifier designed to work at 945MHz and is biased for class AB operation at a V_{DS} of 20V and an I_{DSS} of 76mA for a T_{sub} of 35°C . The amplifier was simulated using the full electro-thermal model in ADS as shown in Fig. 4.22.

For comparison purposes, the amplifier was also simulated using the MET (Motorola Electro-thermal Model) model from Motorola [28]. Initial simulations using the default R_{th} in the MET model showed a thermal response way off. The experimentally determined R_{th} was instead used in the MET model simulations. The

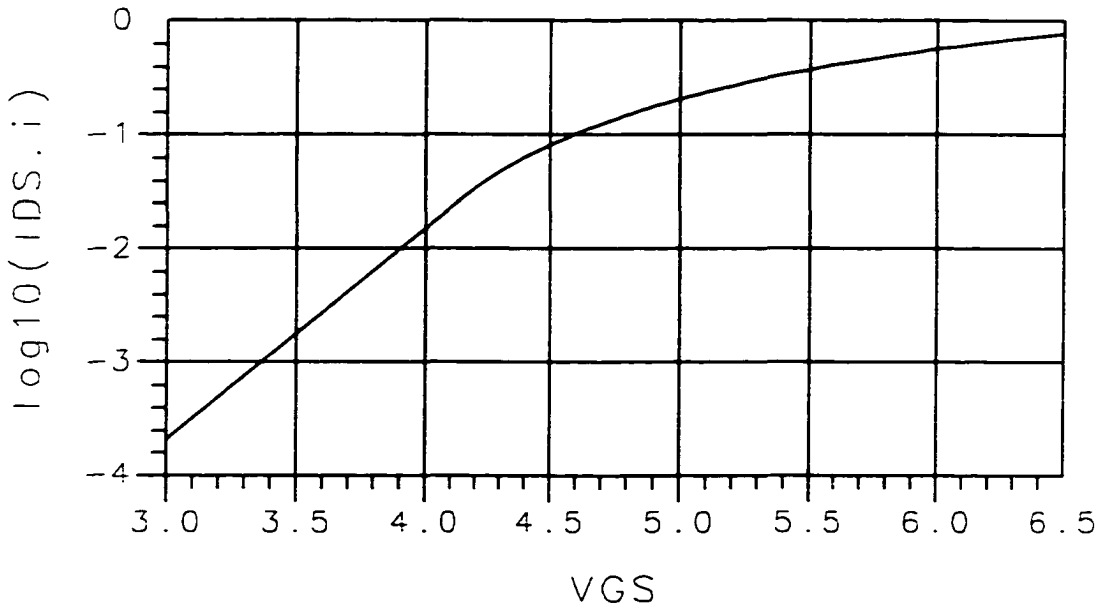


Figure 4.21: Log of drain current as a function of V_{GS} for $V_{DS} = 15$V

amplifier was then built and tested in the lab and simulated and measured results were compared.

Fig. 4.23 shows the comparison between the simulated (solid lines), measured (circles) and MET model (dashed lines) fundamental, second harmonic and third harmonic response of the power amplifier. Note that this plot line style will be used for all figures given in this section. It can be seen that the developed electro-thermal model does a very good job in predicting the power harmonics. It compares to, and exceeds the MET model. Discrepancies appear at higher power where the model

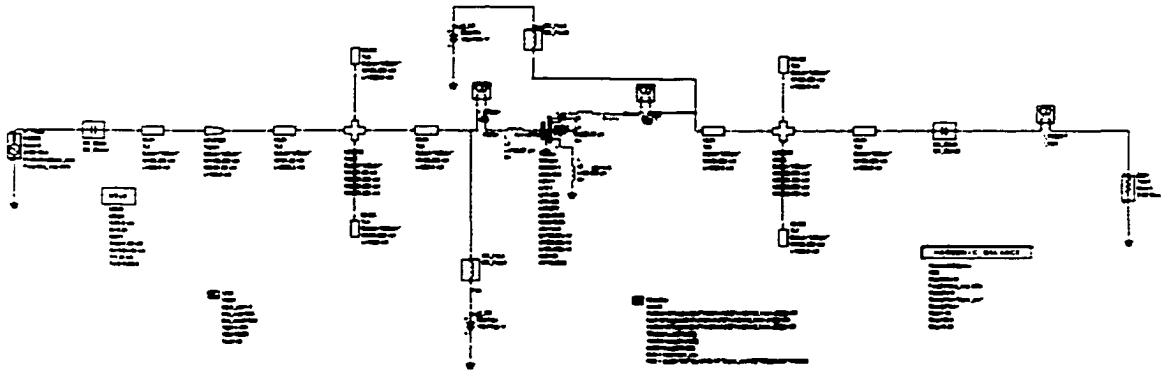


Figure 4.22: Power Amplifier simulated on ADS using full electro-thermal model

seems to predict a sweet spot in the second harmonic at input power levels below what the measurement gives. This sweet spot has been found to be very sensitive to the gate parasitic inductance L_g. The MET model seems to also predict an earlier sweet spot.

Fig. 4.24 shows the DC drain current during operation as the input power is increased. Clearly this large increase is indicative of the dynamic change in DC biasing with the application of RF power. Both the new electro-thermal model and the MET model do a similar job in predicting the drain current increase and both compare well with measured results. Fig. 4.25 shows the average device temperature measured during large signal drive. Clearly, there is substantial increase in $T_{dev,avg}$

with RF power. Fig. 4.26 shows the PAE of the amplifier as a function of input power. The low PAE is indicative of the biasing in class AB. In both Figs. 4.25 and 4.26, the MET model outperforms the developed electro-thermal model at higher power.

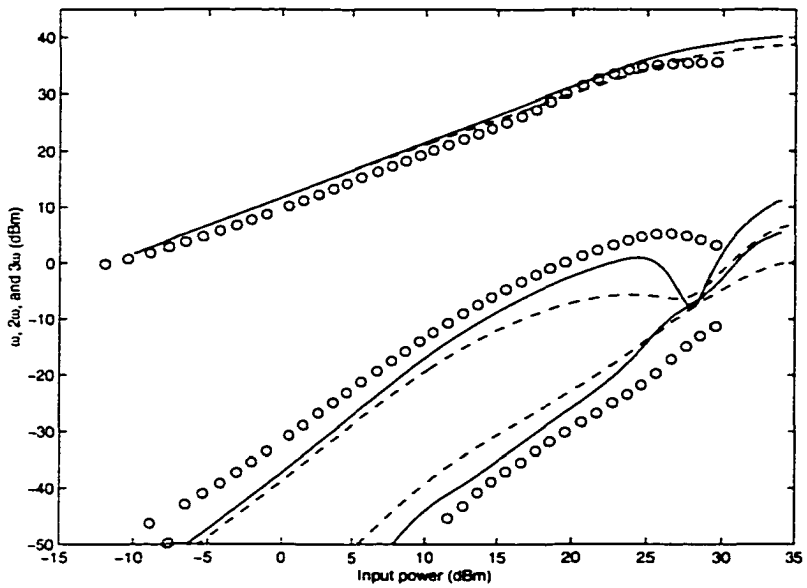


Figure 4.23: Comparison of fundamental (top most curves), second harmonic (middle curves) and third harmonic (lowest most curves) power response of PA for the new electro-thermal model (solid lines), the MET model (dashed lines) and measured results (circles)

From Fig. 4.23 to 4.26 it can be observed that the new electro-thermal model does a very good job in predicting the power amplifier performance. Deviations are more pronounced at higher power, especially in temperature and PAE, where the model goes out of range and relies on extrapolation, both in V_{GS} and V_{DS}. It should also be acknowledged that the MET model does a very good job in predicting the amplifier behavior after the experimentally determined thermal resistance value is used.

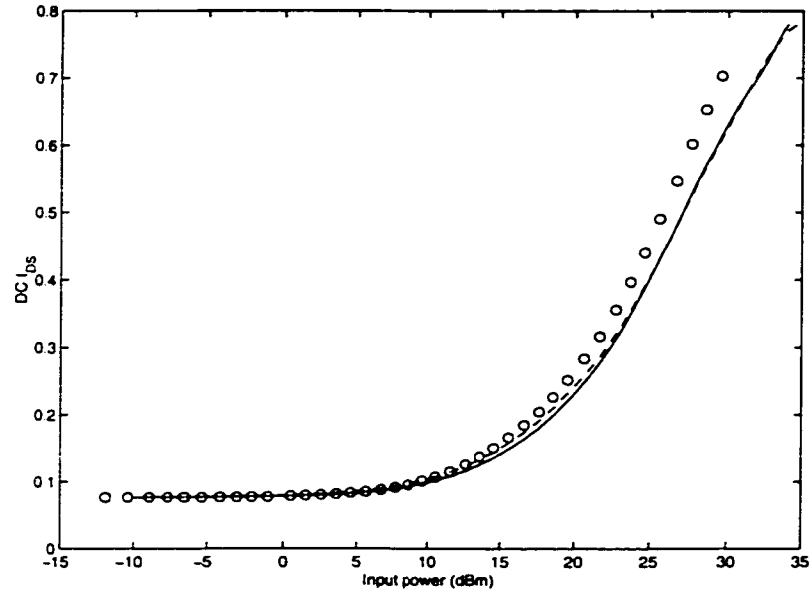


Figure 4.24: Comparison of DC drain current of PA for the new electro-thermal model (solid lines), the MET model (dashed lines) and measured results (circles)

Fig. 4.27 to 4.28 show the time domain drain voltage and current and gate voltage and current respectively, for different input power levels. The solid line is for 30dBm, the dashed dotted line is for 20dBm and the dashed line is for 10dBm. Fig. 4.29 shows the dynamic loadline (voltage trajectories followed) as a function of input power. The plot line style used before has been used to plot this figure. From this figure it can be seen that for high power, the extrapolated data regions (those regions that are inaccessible due to the iso-thermal measurement technique) are entered into by the device. Hence amplifier simulations at high input power are prone to more error. These are the regions in which pulsed IVs can provide more accurate data.

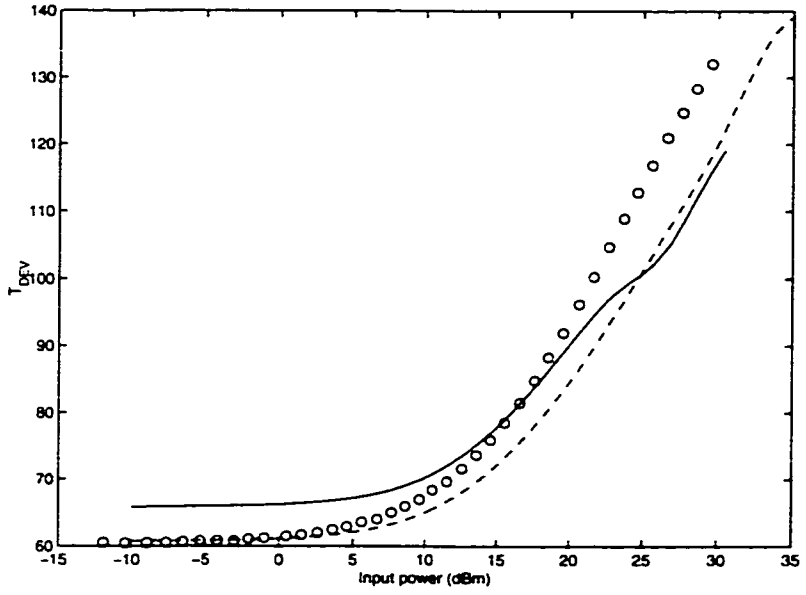


Figure 4.25: Comparison of average device temperature of PA for the new electro-thermal model (solid lines), the MET model (dashed lines) and measured results (circles)

Lastly a two tone intermodulation test was performed on the amplifier at 945MHz and 946MHz. Fig 4.30 shows the $2\omega_2$-ω_1 power as a function of input power. The solid line is the simulated IMD, the circles are measured while the dashed line is the IMD obtained from the MET model. The measured data's noise floor is at around -55dBm of output power. Clearly the developed electro-thermal model does a very good job in predicting this important matrix and performs comparatively better than the MET model.

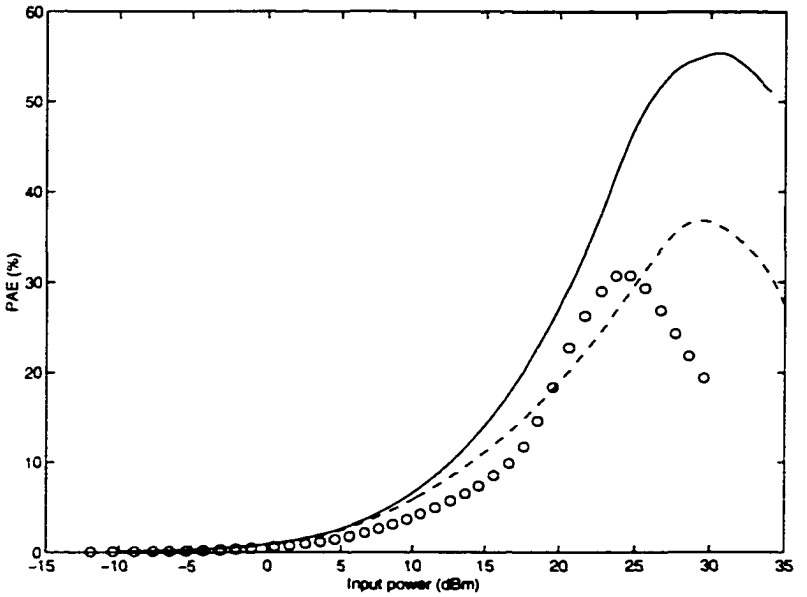


Figure 4.26: Comparison of PAE of PA for the new electro-thermal model (solid lines), the MET model (dashed lines) and measured results (circles)

4.6.1 Effect of Temperature Dependent Charge

While the electro-thermal model presented relied on temperature dependent current, the 60°C C_{12} and C_{22} were used to extract the temperature independent charge. In order to examine the impact of the temperature variation of charge, a 90°C and a 105°C charge representation is generated and used for amplifier simulations respectively. Fig. 4.31 shows the obtained fundamental, second harmonic and third harmonic power response for 60°C (sold lines), 90°C (dashed line) and 105°C (dashed dotted lines) charge representations respectively. Measured data is indicated with circles. From Fig. 4.31 it can be seen that the higher temperature simulations show a more profound sweet spot in the second harmonic. This sweet spot is not quite what

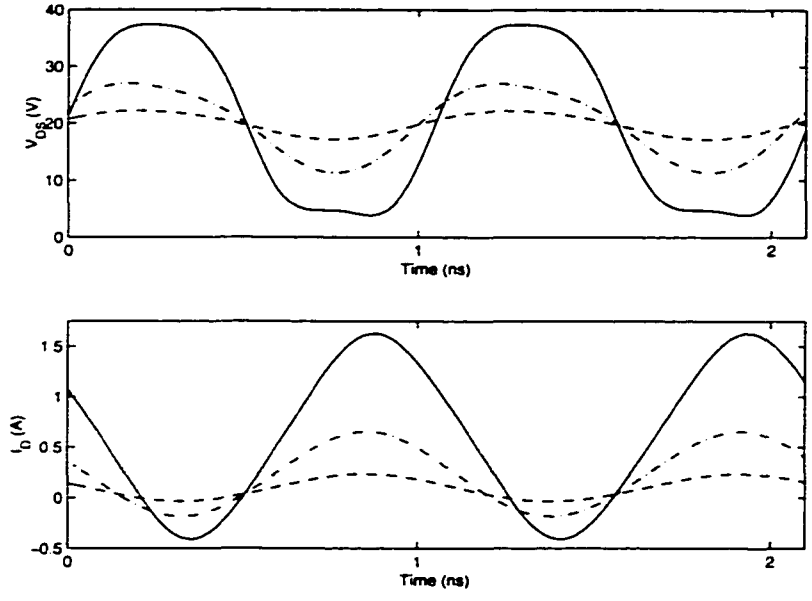


Figure 4.27: Time domain drain voltage and current as a function of input power. The solid line is for 30dBm, the dashed dotted line is for 20dBm and the dashed line is for 10dBm

is measured and indeed sweet spots can be difficult to measure. Note however that due to measurement limitations harmonic values could only be measured on 1dBm input power intervals. The formation of the sweet spots are in regions where the average device temperature departs substantially from the bias condition.

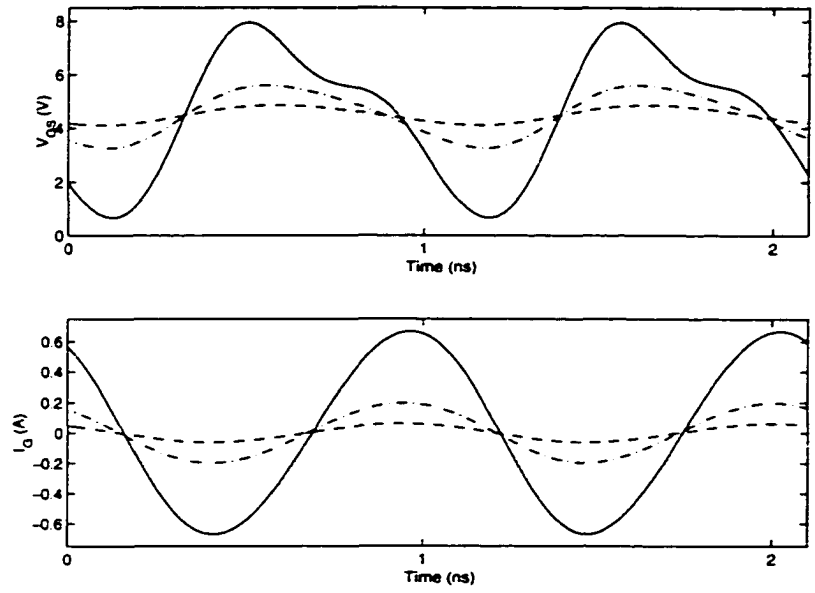


Figure 4.28: Time domain gate voltage and current as a function of input power. The solid line is for 30dBm, the dashed dotted line is for 20dBm and the dashed line is for 10dBm

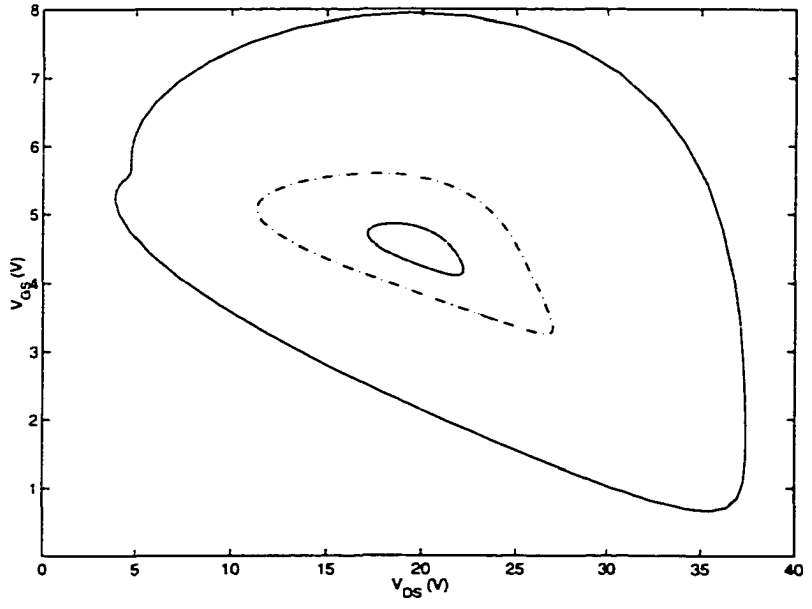


Figure 4.29: Dynamic loadline showing voltage trajectories as a function of input power. The solid line is for 30dBm, the dashed dotted line is for 20dBm and the dashed line is for 10dBm

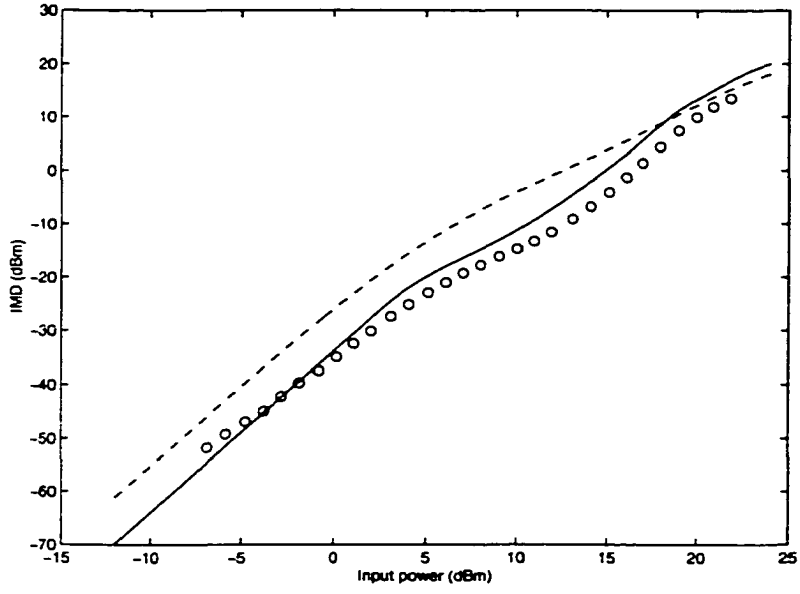


Figure 4.30: Comparison of two tone IMD response of PA for the new electro-thermal model (solid lines), the MET model (dashed lines) and measured results (circles).

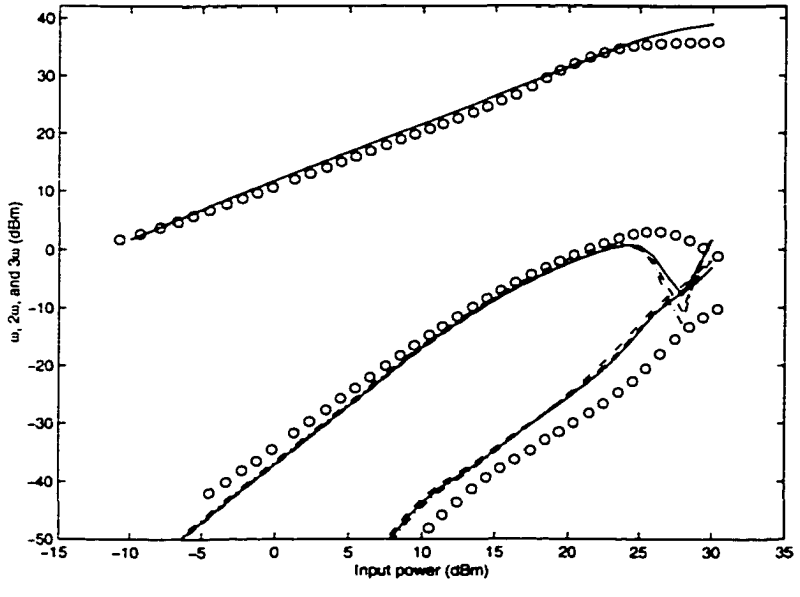


Figure 4.31: Comparison of fundamental (top most curves), second harmonic (middle curves) and third harmonic (lowest most curves) power response of PA for charges of 60°C (sold lines), 90°C (dashed line) and 105°C (dashed dotted lines) respectively compared with measured results (circles)

CHAPTER 5

Conclusions

A robust technique for the large/small signal, non-quasi-static, charge conserving, DC and microwave modeling of universal 3 terminal FET type devices has been presented. The techniques have been developed theoretically for a SOI MOSFET on the PISCES/GIGA physical device simulator and have been applied to modeling a high power LDMOSFET.

A single thermal resistance is found to map the entire electro-thermal response of the device. A low cost automated approach to measuring iso-thermal IVs and microwave scattering parameters using device heating and cooling is discussed. This novel and inexpensive measurement scheme is an alternative to using expensive pulsed IV, pulsed RF measurement equipment. Such equipment is generally unavailable to most academic and start up research labs.

A TRL calibration scheme is developed and utilized to obtain corrected microwave data. The iso-thermal s-parameters are used to extract small signal device parameters. A novel extraction technique utilizing analytical expressions is presented. The extraction procedure is found to yield a continuum of solutions as a function of the source parasitic resistances, R_s. A multi-bias analysis is used to determine the final R_s value. The temperature dependence of the conductances and trans-conductances and capacitances and trans-capacitances is demonstrated. g_m, C_{11}, and C_{21} are found to vary with temperature while g_d, C_{12}, and C_{22} were found to exhibit much less temperature variation.

By comparing hot and cold pulsed IVs with iso-thermal IVs and their associated transconductance with those obtained from small signal extractions, the presence of dispersions in LDMOSFETs, in spite of the $p+$ sinker, is demonstrated. Due to temperature and biasing variations in measuring pulsed IVs, iso-thermal IVs are simultaneously fitted with microwave $g_{m,RF}$ and $g_{d,RF}$ to extract the large signal current element. 3D Tensor Product B-Splines (TPS) utilizing an optimum knot placement scheme, are used to represent the IV and its associated derivatives. Optimized TPS are also used to represent the capacitances and extract the gate and drain charges. Optimum knot placement is necessary to handle areas of large derivative variation in data such as an IV knee.

The large signal model is implemented in the newly released ADS microwave simulator as a user defined model. In the process of doing so, a number of bugs were reported to HP/Agilent and were fixed by them.

Harmonic balance simulations are conducted on a power amplifier with input and output matching, using the developed model. Amplifier matrices such as fundamental, second and third harmonic power, drain current, temperature and two tone intermodulation distortion predicted by the model are compared to measured results. The impact on the model of temperature dependent drain and gate charge has been investigated. Higher temperature is found to introduce more profound sweet spots.

The model, in spite of its simplifications, is found to compare well with the existing MET model, which is based on pulsed IV and pulsed RF. When it comes to two tone intermodulation predictions, the new model is found to perform even better than the MET model. The model suffers with problems at higher input power which corresponds to areas in which extrapolation is used to obtain data. This is due to the shortcoming in the iso-thermal measurement technique that requires more cooling to access these regions.

5.1 Model Use in Other Devices of the Same Type

Indeed the device characterization and model extraction procedure is quite complicated and time consuming. It would be difficult to extract a new model for every new

device of the same type. Unfortunately, due to the manufacturing process, there can be quite a substantial variation in devices of the same kind. For example, Motorola gives a 2V tolerance in the value of the threshold voltage of the MRF 181.

Fig. 5.1 shows the IV characteristics for three different MRF 181 transistors for a T_{sub} = 34°C, while Fig. 5.2 shows the corresponding electro-thermal characteristics. From both Fig. 5.1 and 5.2 it is evident that there is considerable variation in the threshold voltage and thermal resistance of different MRF 181 transistors.

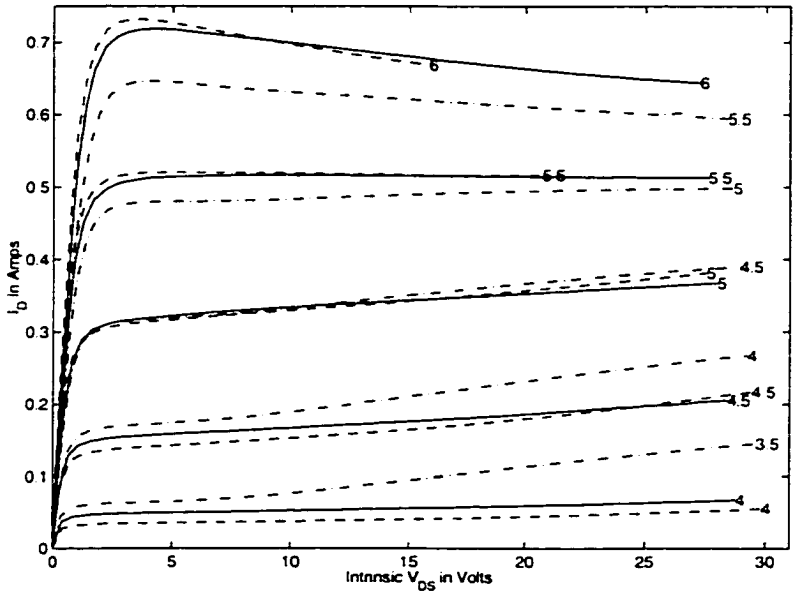


Figure 5.1: Comparison of IV characteristics of three different MRF 181 transistors (solid, dashed and dashed doted lines) for a T_{sub} = 34°C. The corresponding V_{GS} values appear on the plots

The model developed can however easily by applied to other devices. In-spite of the large variation in parameters of different LDMOSFETs, different devices of the

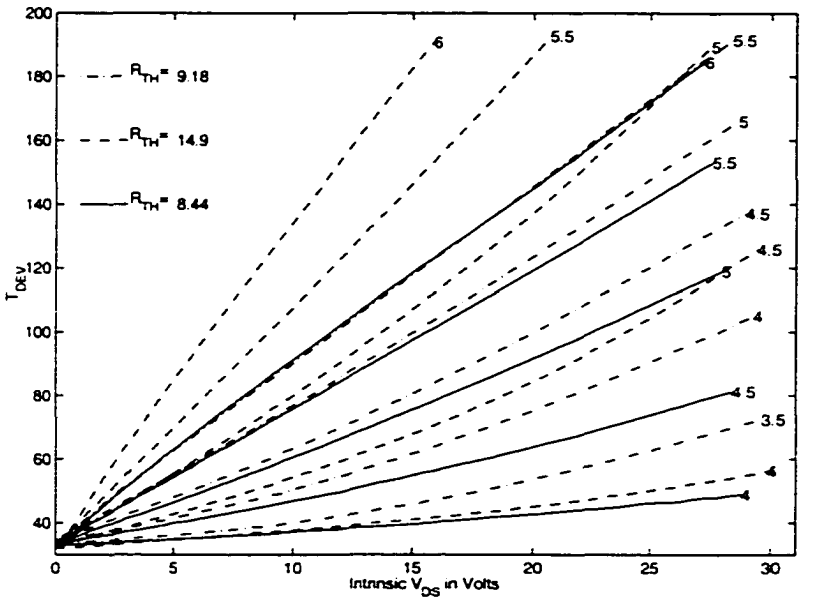


Figure 5.2: Comparison of electro-thermal characteristics of three different MRF 181 transistors (solid, dashed and dashed doted lines) for a $T_{sub} = 34°C$. The corresponding V_{GS} values appear on the plots

same type can be handled by simply adjusting the threshold voltage and thermal resistance parameters of the model. This is what was done in order to get the MET model to give a good a prediction for the amplifier performance. The thermal resistance was changed as a model parameter and the threshold voltage difference was implemented by adjusting the V_{GS} value to obtain the desired I_{DS}. As a matter of fact, for such devices, biasing is always specified as a V_{DS}, I_{DS} point.

5.2 Directions for Future Work

One of the major simplifications involved in the model was that of making the capacitances temperature independent. It was found that higher temperature yields more profound sweet spots. This issue needs to be revisited and 3D TPS can be used to implement the temperature dependent charge.

For different devices used, it was found that under high power drive, the device temperature increase was around 30°C from its low power value. It was this fact that was used in order to decide that iso-thermal s-parameters should be acquired from 45°C to 105°C. However in retrospect, it would have been better to acquire more data at even higher temperatures given the immense temperature rise observed in this device. Data at 120°C and 135°C can also be acquired.

The device performance for negative V_{DS} needs to be addressed. At the moment, the device is assumed symmetric, although this is not the case in reality. A scheme to switch the source and drain in ADS could be implemented to address this issue.

While the two-tone IMD of the power amplifier has been seen to compare very well, its behavior in the presence of CDMA signals often times is very different. CDMA amplifiers suffer from spectral re-growth that can distort the output. Hence, in order to further qualify the model, the PAs simulated response in the presence of a CDMA signal on ADS would need to be compared with that measured using a commercial digitally modulated source and observing the output on a spectrum analyzer [62].

As has already been mentioned, there can be substantial variations in performance among different LDMOSFETs of the same kind due to manufacturing limitations. A scheme was proposed to use the same model for different devices by simply adjusting the thermal resistance and threshold voltage. This now needs to be applied experimentally.

The developed electro-thermal model was found to under perform the MET model at high power in predicting device temperature and PAE. The reason given for this was the data extrapolation used. Pulsed IVs however give access to these regions. Hence it would be very instructive to build a model using the existing charge and a simultaneous fit of existing g_m with measured pulsed IVs. Such a model can be quickly developed using all existing code.

Last but not least, it was found that the gate parasitic inductance seems to play a substantial role in establishing the onset of sweet spots. This deserves further investigation since sweet spots can be exploited for better amplifier design.

BIBLIOGRAPHY

[1] P. Antognetti and G. Massobrio, *Semiconductor Device Modeling with SPICE*, New York, NY: McGraw-Hill, 1988.

[2] H. C. de Graaff and F. M. Klaassen, *Compact Transistor Modelling for Circuit Design*, New York, NY: Springer-Verlar Wien, 1990.

[3] G. Shahidi, *et al.*, "A room temperature 0.1 μm CMOS on SOI," *IEEE Transactions on Electron Devices*, vol. 41, no. 12, pp. 2405-2412, 1994.

[4] M. Hanes, *et al.*, "MICROX^{TM}–An all-silicon technology for monolithic microwave integrated circuits," *IEEE Electron Device Letters*, vol. 14, no. 5, pp. 219-221, May 1993.

[5] J. Tihanyi and H. Schlotterer, "Properties of ESFI MOS transistors due to the floating substrate and the finite volume," *IEEE Transactions on Electron Devices*, vol. ED-22, p. 1017, 1975.

[6] H. K. Lim and J. G. Fossum, "A charge-based large-signal model for thin-film SOI MOSFET's," *IEEE Transactions on Electron Devices*, vol. ED-32, no. 2, pp. 446-457, Feb. 1985.

[7] D. E. Ward, "Charge-based modeling of capacitance in MOS transistors," Doctoral Dissertation, Stanford University, June 1981.

[8] D. E. Root and B. Hughes, "Principles of nonlinear active device modeling for circuit simulation," *Proceedings 32nd ARFTG Conference*, Tempe, AZ, 1988, pp. 3-26.

[9] R. R. Daniels, A. T. Yang, and J. P. Harrang, "A universal large/small signal 3-terminal FET model using a non-quasi-static charge-based approach," *IEEE Transactions on Electron Devices*, vol. 40, no. 10, pp. 1723-1729, Oct. 1993.

[10] G. Bischoff and J. P. Krusius, "Technology independent device modeling for simulation of integrated circuits for FET technologies," *IEEE Transactions on Computer-Aided Design*, CAD-4(1): pp. 99-110, Jan. 1985.

[11] W. M. Coughran, W. Fichtner, and E. Grosse, "Extracting transistor charges from device simulations by gradient fitting," *IEEE Transactions on Electron Devices*, 8(4): pp. 380-394, April 1989.

[12] E. J. Prendergast, P. Lloyd, and H. Dirks, "The extraction of terminal charges from two-dimensional device simulations of MOS transistors," *The International Journal for Computation and Mathematics in Electrical and Electronic Engineering*, 6(2): pp. 107-114, 1987.

[13] S. Sulistio, "Small-Signal and Large-Signal Modeling of MODFETs Based on Analytical and Table methods," Master's Thesis, The Ohio State University, Sept 1993.

[14] K.-W. Chai and J. J. Paulos. "Unified non-quasi-static modeling of the long channel four-terminal MOSFET for large and small-signal analyses in all operating regimes," *IEEE Transactions on Electron Devices*, vol. ED-36, pp. 2513-2520, November 1989.

[15] P. Roblin, S. C. Kang, and W. R. Liou, "Improved small-signal equivalent circuit model and large-signal state equations for the MOSFET/MODFET wave equation," *IEEE Transactions on Electron Devices*, vol. 38, no. 8, pp. 1706-1718, Aug. 1991.

[16] L. McDaid, S. Hall, P. Mellor, and W. Eccleston, "Physical origin of negative differential resistance in SOI transistors," *Electronics Lett.*, vol. 25, no. 13, pp. 827-828, June 1989.

[17] J.-P. Colinge, *Silicon-on-Insulator Technology: Materials to VLSI*, Norwell, MA: Kluwer, 1991.

[18] J. Bielefeld, G. Pelz, H. B. Abel, and G. Zimmer, "Dynamic SPICE-simulation of the electrothermal behavior of SOI MOSFET's," *IEEE Transactions on Electron Devices*, vol. 42, no. 11, pp. 1968-1974, Nov. 1995.

[19] K. A. Jenkins and J. Y.-C. Sun, "Measurement of $I - V$ curves of silicon-on-insulator (SOI) MOSFET's without self-heating," *IEEE Electron Device Letters*, vol. 16, no. 4, pp. 145-147, April 1995.

[20] A. Wei, M. J. Sherony, and D. A. Antoniadis, "Transient behavior of the kink effect in partially-depleted SOI MOSFET's," *IEEE Electron Device Letters*, vol. 16, no. 11, pp. 494-496, November 1995.

[21] J. Gautier and J. Y.-C. Sun, "On the transient operation of partially depleted SOI nMOSFET's," *IEEE Electron Device Letters*, vol. 16, no. 11, pp. 497-499, November 1995.

[22] K. Fuji, "The novel nonlinear model and the model parameter extraction technique," Japan Radio Co., Ltd., Publishing status unknown, 1995.

[23] G. Heftman, "GaAs, MOS, bipolar vie for power applications," *Microwaves & RF*, vol. 37, no. 7, pp. 31-39, July 1998.

[24] A. Wood, "LDMOS transistor powers base-station amplifiers," *Microwaves & RF*, vol. 37, no. 3, pp. 69-80, March 1998.

[25] J. Pritiskutch and B. Hanson, "Understanding LDMOS device fundamentals," *Microwaves & RF*, vol. 37, no. 8, pp. 114-116, August 1996.

[26] P. Khandelwal, M. Trivedi, K. Shenai, and S. K. Leong, "Thermal and Package Performance Limitations in LDMOSFET's for RFIC Applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 47, no. 5, pp. 575-585, May 1999.

[27] C. P. Dragon, W. R. Burger, B. Davidson, E. Krvavac, N. Dixit, and D. Joersz, "High power RF-LDMOS transistors for base station applications," *RF Design*, pp. 20-26, March 2000.

[28] W. R. Curtice, J. A. Pla, D. Bridges, T. Liang, and E. E. Shumate, "A new dynamic electro-thermal nonlinear model for silicon RF LDMOS FETs," *Microwave Symposium 99*, pp. 419-422, Vol 2, 1999.

[29] W. R. Curtice, "A MESFET model for use in the design of GaAs integrated circuits," *IEEE Transactions on Microwave Theory and Techniques*, 28(5), pp. 448-456, 1980.

[30] Agilent Technologies, "Test and Measurement 2000 Catalog". Specifications.

[31] J. M. Collantes, J. J. Raoux, R. Quere, and A. Suarez, "New measurement-based technique for RF LDMOS nonlinear modeling," *IEEE Microwave and Guided Wave Letters*, vol. 8, no. 10, pp. 345-347, October 1198.

[32] B. Razavi, *RF Microelectronics*, Upper Saddle River, NJ: Pentice Hall, 1998.

[33] T. Ruttan, "Designing Amplifiers for Wireless Systems," *Microwaves & RF*, pp. 89-100, January 1998.

[34] S. Akhtar and P. Roblin, "B-spline Based, Large-signal DC and Microwave-model for SOI-MOSFETs," accepted for publication, *Analog Integrated Circuits and Signal Processing*, Kluwer Academic Publishers, Norwell, MA.

[35] *Atlas 2D Device Simulation Framework: User's Manual*, Silvaco International, March 1994.

[36] S. Selberherr, *Analysis and Simulation of Semiconductor Devices*, Wien-New York: Springer-Verlag, 1984.

[37] M. H. Somerville, J. A. del Alamo, and W. Hoke, "Direct Correlation Between Impact Ionization and the Kink Effect in InAlAs/InGaAs HEMT's," *IEEE Electron Device Letters*, vol. 17, no. 10, pp. 473-475, October 1996.

[38] A. L. Caviglia, "Development and modeling of microwave SOI MOSFETs," Doctoral Dissertation, The University of Maryland, 1995.

[39] B. M. Tenbroek, M. S. L. Lee, W. Redman-White, R. J. T. Bunyan, and M. J. Uren, "Self-Heating Effects in SOI MOSFET's and Their Measurement by Small Signal Conductance Techniques," *IEEE Transactions on Electron Devices*, vol. 43, no. 12, pp. 2240-2248, December 1996.

[40] O. Le Neel and M. Haond, "Electrical transient study of negative resistance in SOI MOS transistors," *Electron. Lett.*, vol. 26, no. 1, pp. 73-74, 1990.

[41] C. de Boor, *A Practical Guide to Splines*, New York: Springer-Verlag, 1978.

[42] S. Akhtar, "Highly Accurate Large-signal Microwave-model for SOI-MOSFET's," Master's Thesis, The Ohio State University, Feb 1996.

[43] D. E. Root, S. Fan, and J. Meyer, "Technology Independent Large Signal Non Quasi-Static FET Models by Direct Construction from Automatically Characterized Device Data," *Proceedings 21st European Microwave Conference*, Stuttgart, Germany, 1991, pp. 927-932.

[44] K. Jeon, Y. Kwon, and S. Hong, "A Frequency Dispersion Model of GaAs MESFET for Large-Signal Applications," *IEEE Microwave and Guided Wave Letters*, vol. 7, no. 3, pp. 78-80, March 1997.

[45] D. Suh, and J. G. Fossum, "A Physical Charge-Based Model for Non-Fully Depleted SOI MOSFET's and Its Use in Assessing Floating-Body Effects in SOI CMOS Circuit's," *IEEE Transactions on Electron Devices*, vol. 42, no. 4, pp. 728-737, April 1995.

[46] A. T. Yang, C. H. Chan, J. T. Yao, R. R. Daniels, and J. P. Harrang, "Modeling and simulation of high-frequency integrated circuits based on scattering parameters," *Proceedings of The IEEE Design Automation Conference*, pp. 752-757, 1991.

[47] *MISIM Version 2.2: User's Manual*, The University of Washington, March 1993.

[48] P. Roblin, S. C. Kang, and H. Morkoc, "Analytic Solution of the Velocity-Saturated MOSFET/MODFET Wave Equation and Its Application to the Prediction of the Microwave Characteristics of MODFET's," *IEEE Transactions on Electron Devices*, vol. 37, no. 7, pp. 1608-1621, July 1990.

[49] R. Hajji, A. B. Kouki, S. El-Rabaie, and F. M. Ghannouchi, "Systematic DC/Small-Signal/Large-Signal Analysis of Heterojunction Bipolar Transistors Using a New Consistent Nonlinear Model," *IEEE Transactions on Microwave Theory and Techniques*, vol. 44, no. 2, pp. 233-241, Feb. 1996.

[50] Motorola "The RF MOSFET Line: RF Power Field Effect Transistor: N-Channel Enhancement-Mode Lateral MOSFET", Motorola Semiconductor Technical Data.

[51] *LabWindows/CVI: Getting Started with LabWindows/CVI*, National Instruments, July 1996.

[52] S. Akhtar, P. Roblin, and J. Strahler, "Electro-thermal and Iso-thermal Characterizations of Power RF Silicon LDMOSFETs," *IEEE Electron Device Letters*, submitted for publication.

[53] G. Engen, and C. Hoer, "Thru-Reflect-Line: An Improved Technique for Calibrating the Dual Six-Port Automatic Network Analyzer," *IEEE Transactions on Microwave Theory and Techniques*, vol. MTT-27, no. 12, pp. 987-993, Dec. 1979.

[54] D. Pozar, *Microwave Engineering*, Reading, MA: Addison Wesley, 1997.

[55] R. Marks, "A Multiline Method of Network Analyzer Calibration," *IEEE Transactions on Microwave Theory and Techniques*, vol. 39, no. 7, pp. 1205-1215, July. 1991.

[56] J.-P. Raskin, R. Gillon, J. Chen, D. Vanhoenacker-Janvier, and J.-P. Colinge, "Accurate SOI MOSFET Characterization at Microwave Frequencies for Device Performance Optimization and Analog Modeling," *IEEE Transactions on Microwave Theory and Techniques*, vol. 45, no. 5, pp. 1017-1025, May. 1998.

[57] J.-P. Raskin, "Modeling, characterization and optimization of MOSFETs and passive elements for the synthesis of SOI MMICs," *Ph.D. Thesis*, University Catholique de Louvain, Laboratoire d'Hyperfrequence, December 1997.

[58] P. Roblin, S. Akhtar, and J. Strahler, "New Non-Quasi-Static Theory for Extracting Small-Signal Parameters Applied to LDMOSFETs," *IEEE Microwave and Guided Wave Letters*, accepted for publication.

[59] J.-P. Tayssier, P. Bouysse, Z. Ouarch, D. Barataud, T. Peyretaillade, and R. Quere, "40-GHz/150-ns Versatile Pulsed Measurement System for Microwave Transistor Isothermal Characterization," *IEEE Transactions on Microwave Theory and Techniques*, vol. 46, no. 12, pp. 2043-2052, Dec. 1998.

[60] Hewlett Packard, "HP 8753E RF Vector Network Analyzer", HP Technical Specifications.

[61] G. Gonzalez, *Microwave Transistor Amplifiers*, Englewood Cliffs, NJ: Prentice-Hall, 1984.

[62] Hewlett Packard, "Testing CDMA Base Station Amplifiers", HP Application Note 1307.

[63] J. L. B. Walker, *High Power GaAs FET Amplifiers*, Norwood, MA: Artech House, 1993.