Design of a Digitally Enhanced, Low Power, High Gain, High Linearity CMOS Mixer and CppSim Evaluation

THESIS

Presented in Partial Fulfillment of the Requirements for the Degree Master of Science in the Graduate School of The Ohio State University

By

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Abstract

The objective of this work is to develop a new technique of digitally controlled, second order linearization of an active mixer, along with incorporation of other standard linearization techniques. The performance of various techniques was studied and the one suitable for this design was chosen. The digital control stems from the fact that the second order non linearity is a result of the mismatch introduced in the switching pair. The system level design tool CppSim was also explored to conclude the ability to transfer the cadence design points to CppSim. Various simulations were done to check the performance of the mixer. The choice of bias points for optimal gain and linearity were explored.

Dedication

Dedicated to my family for their unconditional love and guidance

Acknowledgements

My experiences as a Master's student at The Ohio State University wouldn't have been possible without the help of my Professors, friends and family.

I thank my advisor, Prof. Steven Bibyk, for his guidance from the day I joined this school. His courses have played a big role in laying the foundation for Digital, Analog, Mixed Signal and RF circuits. He helped me zero in on this idea for my thesis through many conversations, for which I am very grateful. He has always pushed me to work harder and expand my research to what it is today.

I thank Prof. Wladimiro Villarroel for his help in planning my Master's education efficiently and his help during my thesis defense.

I thank Prof. Waleed Khalil and Prof. Ayman Fayed for their rigorous coursework which gave me valuable insight on the challenges faced by an engineer during circuit design and taught me the importance of time management.

I thank my friends and relatives for helping me overcome home sickness. Living in a country, halfway around the world from India, would have been impossible without them.

Finally, I thank my parents for their love, support, innumerable sacrifices and unwavering belief in me. Without them, I would not have been able to reach where I am today.

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Major Field: Electrical and Computer Engineering

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List of Abbreviations

RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
Rx	Receiver
Tx	Transmitter
DSB	Double Side Band
SSB	Single Side Band
dB	Decibels
GMSK	Gaussian Minimum Shift Keying
LO	Local Oscillator
IF	Intermediate Frequency
IM	Inter Modulation Products
IIP3	Input Referred Third Order Intercept Point
IIP2	Input Referred Second Order Intercept Point
P1-dB	1 dB Compression Point
NF	Noise Figure
CMOS	Complementary Metal Oxide Semiconductor
NMOS	N-Type Metal Oxide Semiconductor

PMOS	P-Type Metal Oxide Semiconductor
LNA	Low Noise Amplifier
PA	Power Amplifier
VCO	Voltage Controlled Oscillator
PLL	Phase Locked Loop
CCPD	Cross Coupled Post Distortion
PAC	Periodic AC
PSS	Periodic Steady State
PNoise	Periodic Noise
PXF	Periodic Transfer Function
QPSS	Quasi-Periodic Steady State
QPAC	Quasi-Periodic AC
EN	Enable
CLK	Clock
g_m	Transconductance
BalUn	Balanced Unbalanced
VCVS	Voltage Controlled Voltage Source
PTAT	Proportional To Absolute Temperature
CTAT	Complementary To Absolute Temperature

Chapter 1: Introduction

Evolution in technology has led to miniaturization of all the chips, with billions of transistors being fit in a single chip, as compared to a fraction of that number a decade ago. Mobile technology has come a long way too. Every component that goes in the device has one goal: to incorporate as many features in as little space as possible. Performance is now joined by cost and area as the top priorities by any manufacturer.

Another area of great evolution is automation. Any process that has a possibility of automation is being explored and automated. This includes modeling of analog, RF and digital circuits. A digital circuit can be shrunk with newer technology, enabling designers to fit billions of transistors on a chip. However, the same cannot be said about the RF and analog circuits.

This research is aimed at a specific component of a wireless transceiver: the mixer.

A mixer is an important part of the transceiver chain as it is followed by the ADC in the receiver and by the PA in the transmitter, ignoring the filters in between stages. This crucial position of the mixer means that it has to be designed very carefully, because any noise introduced in this component can corrupt either the ADC or the signal to be transmitted through the PA.

The main goal of this research is to develop a high linearity mixer that consumes low power. Area considerations have been made as far as possible. However, presence of inductors and large number of transistors leads this design to occupy a fairly large area, considering the area standards these days. The following chapters describe in detail the mathematical modeling and the design of the proposed circuit. The pros and cons of the proposed circuit have also been discussed to be able to evaluate the usability of any this design in any given circuit.

Keeping automation in mind, a simulation tool, CppSim, has been explored as the second part of this research. The main aim behind automation is to minimize the work to be done when moving from one process node to another or when moving from one circuit to another. Behavioral models in CppSim were explored and it was determined that it is not an ideal tool to be used in this case, as is explained in the following chapters.

1.1 Mixer Fundamentals:

Mixer is a time variant device that performs frequency translations from lower to higher frequency and vice versa. This functionality of the mixer makes it a vital part of every wireless system. The frequency translation is done by the mixer by making use of the LO signal it receives from an oscillator. The incoming RF frequency signal is multiplied with the LO signal. This multiplication results in the IF output signal. This conversion can be described by the following equation:

$$f_{out} = \pm f_{in} \pm f_{LO}$$

Where,

f_{out} is the signal frequency at the output port

f_{in} is the signal frequency at the input port

f_{LO} is the signal frequency at the LO port

Figure 1.1 represents the basic symbol of a three port mixer, showing the positions of the input RF port, the LO port and the output IF port.

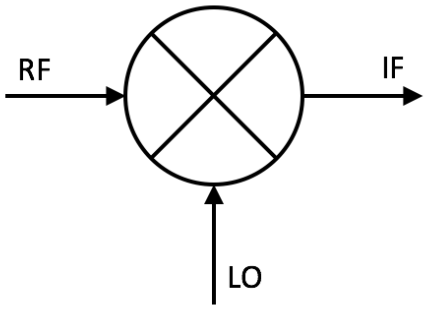

Figure 1.1: Basic Symbol of a Three-Port Mixer

The mixer is considered to be linear with respect to RF port, and non-linear with respect to LO port. Ideally, the output amplitude and phase at the IF port is dependent on the amplitude and phase of the signal at the RF port and independent of the same at the LO port. However, depending on the port-to-port isolation, the output dependency on the LO signal characteristics varies.

During up conversion, the IF port is considered as input and the RF port is considered as the output, while on the other hand, during down conversion, the RF port is considered as the input port and the IF port is considered as the output port.

Figure 1.2 represents the mixer down conversion and the Figure 1.3 represents the mixer up conversion. The frequency up conversion in a mixer can be either a single sideband (SSB) or a double sideband (DSB) conversion. A double sideband up conversion (shown in Figure 1.3) means that both the $[f_{RF1} = f_{LO} - f_{IF}]$ and the $[f_{RF2} = f_{LO} + f_{IF}]$ products are utilized at the output. On the other hand, a single sideband conversion means that only one of the two products are utilized while the other is filtered out in the mixer. This filtering is highly sophisticated and makes the entire mixer design complicated.

More information on the fundamentals of a mixer can be found in [16, 17, 23, 32, 37, 38].

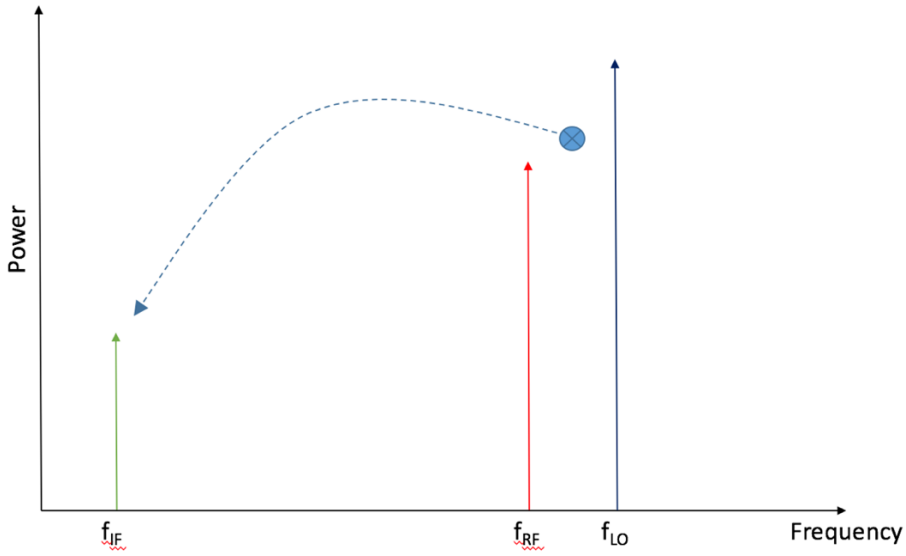

Figure 1.2: Mixer down conversion

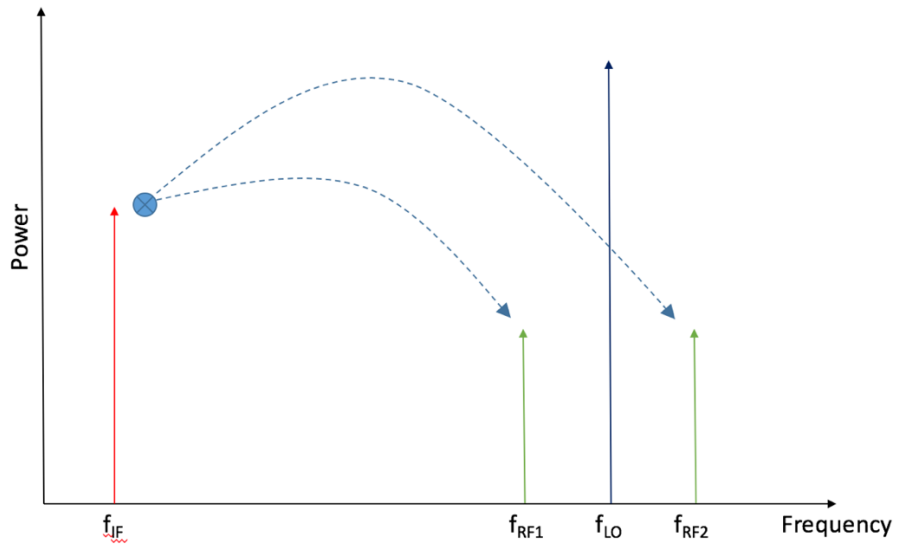

Figure 1.3 Mixer up conversion

The IF/RF signals are called the information bearing signals. During frequency conversion, the information carried by the RF signal is up/down converted and translated to the IF output. This converted signal is then fed to the ADC (in case of a receiver) or a filter (in case of a transmitter). Due to this critical position, mixer is considered as one of the more important blocks in the transceiver chain and a proper design is very crucial.

In theory, any nonlinear device can be used to design a mixer circuit. However, the challenge is to design a high performance mixer. For this reason, only a few nonlinear devices can be used. For modern mixers, the weapons of choice are Schottky diodes, GaAs FETs and CMOS transistors. Based on the application, the choice is made and the design is carried out. FET and CMOS mixers are typically used in high volume applications where the cost is the critical driving point and performance takes the second preference. Keeping this in mind, most of the transceivers used in mobile devices today

utilize the CMOS mixer. On the other hand, the more challenging and high performance applications are dealt with the Schottky diode mixer. In this thesis, the CMOS transistor has been used.

1.2 Types of Mixers:

The mixer can be broadly classified into two subcategories:

- Passive and Active Mixers
- Unbalanced and Balanced Mixers

1.2.1 Passive and Active Mixers:

The two major types of mixers are the active and passive mixers. The main difference between these two types of mixers is the power consumption.

Passive mixers, also known as switching mixers, are the simplest mixers in terms of design. These mixers do not consume any DC power during conversion. Due to the absence of a transconductance stage, the conversion gain of passive mixers is very low. In fact, the gain is negative in these mixers, due to which it is termed as a conversion loss. The mixer performs a multiplication between the RF and LO ports and the ideal equation is as below [25]:

$$\cos(\omega_{RF}t)\,.\cos(\omega_{LO}t) = \frac{1}{2}\cos(\omega_{RF}t + \omega_{LO}t) + \frac{1}{2}\cos(\omega_{RF}t - \omega_{LO}t)$$

Passive mixers require good switches with minimum on-resistance to reduce the conversion loss. Also, they require maximum high resistance when off to provide good isolation. Another disadvantage of this type of mixer, apart from the conversion loss, is the high LO signal needed to completely turn the LO switches ON/OFF.

MOS transistors are very good switches during high frequency applications. It turns completely on in the saturation region and completely turns off in the cut off region. For accurate switching, the DC bias voltage, V_{GS}, is set equal to the threshold voltage, V_T.

Single balanced and double balanced passive mixers have been discussed in the next section.

Active mixers, on the other hand, consist of two stages: switching stage and transconductance stage. The transconductance stage converts the RF signal to current. This is fed to the LO switching transistors. The large LO signal is multiplied to the tail current. This is then fed to the load, which converts the current back to voltage and the output is taken at this stage. Due to the presence of the transconductance stage, the conversion gain of the active mixer is positive. This stage is also the reason for power consumption in this kind of mixer, thus giving it the name active. However, this stage also leads to a higher noise figure of the mixer. Also, the non-linear characteristics of this stage also lead to the over all linearity degradation of the mixer. Similar to the passive mixer, the active mixer can be single balanced or double balanced, which will be discussed in the next section.

The most common type of active mixer is the Gilbert cell mixer. The equations involved with this type of mixer have been discussed in later sections, as this is the mixer that has been implemented in this thesis.

1.2.2 Unbalanced and Balanced Mixers:

An unbalanced mixer is the simplest kind of mixer with the lowest noise figure. Figure 1.4 represents a single transistor unbalanced mixer, also known as a square law mixer.

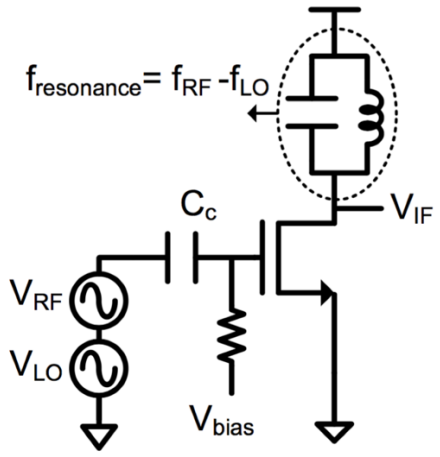

Figure 1.4 Square Law Mixer [16]

The conversion gain of this mixer is given by [16]:

$$G_C = \frac{(\mu_n C_{OX} W)}{2L} . V_{LO}$$

The resonance circuit can also be a parallel RLC tank. The mixing operation is performed by modulation of the transconductance of the driver stage with a large LO signal. The LO signal varies the V_{DS} of the transistor, thus modulating the transconductance. The bias is at the edge of triode and saturation region to maximize the transconductance variation due to the LO signal.

The unbalanced mixers have a very poor port to port isolation, since the LO and the RF signals are fed at the same port. This means that the noise at IF can easily mix with the DC component of the LO signal, thus increasing the noise at the output port. On the other

hand, the resonance tank removes most of the intermodulation products, thus improving the linearity of the mixer.

A balanced mixer, whether active or passive, provides a better isolation than the unbalanced mixer. It is of two types: single balanced and double balanced.

Discussing the passive mixers first, Figure 1.5 represents the single balanced passive mixer.

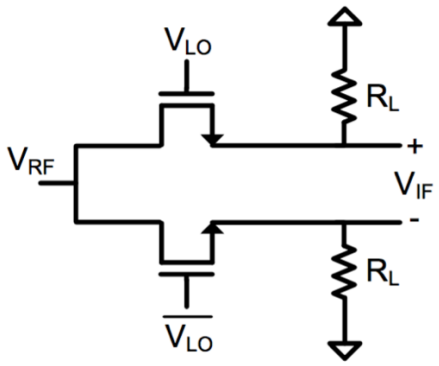

Figure 1.5 Single Balanced Passive Mixer [16]

The voltage gain (conversion loss) of this mixer is given by [16]:

$$A_v = \frac{2}{\pi} \approx -4\ dB$$

This topology balances the RF signal at the output, leaving only the LO signal present at the output. The conversion loss is also much better than an unbalanced passive mixer ($A_v \approx -10\ dB$).

Figure 1.6 represents a double balanced passive mixer.

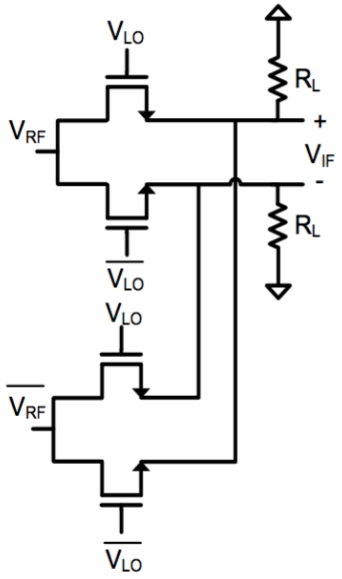

Figure 1.6 Double Balanced Passive Mixer [16]

The conversion loss of this mixer is same as the single balanced passive mixer. However, the advantage lies in the better isolation. Now, neither the RF nor the LO signal is present at the IF output.

A single balanced active mixer is represented in Figure 1.7.

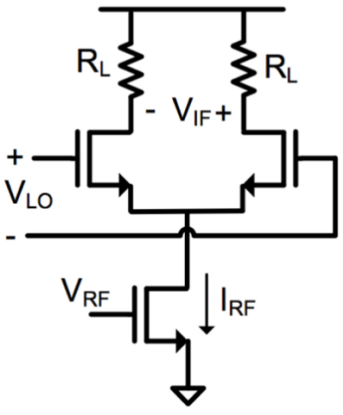

Figure 1.7 Single Balanced Active Mixer [16]

Conversion gain of this circuit is as given as [16]:

$$A_v = \frac{2g_m R_L}{\pi}$$

As seen from the equation above, the conversion gain is positive in this case. This topology has a lower NF than the double balanced mixer due to lesser noise contributors in the circuit. On the other hand, the linearity of the circuit depends on the transconductance stage, the more linear the g_m device, the better the linearity of the circuit.

Similar to the single balanced passive mixer, this mixer also balances the RF signal and only the LO signal is present at the output.

Figure 1.8 represents a double balanced active mixer.

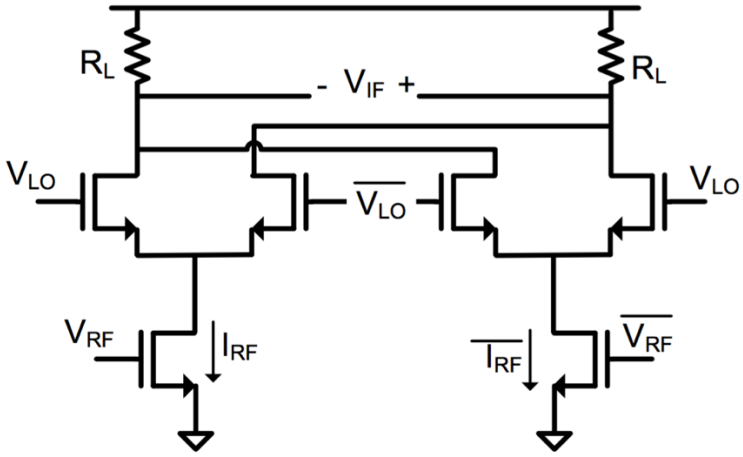

Figure 1.8 Double Balanced Active Mixer [16]

The conversion gain of this mixer is same as the single balanced mixer. However, similar to the double balanced passive mixer, this mixer has a better isolation as both the LO and

the RF components are balanced out. This also means that the absence of the common mode leads to the cancellation of all the even order harmonics. On the negative side, the NF of this circuit is worse due to larger number of components and also consumption of higher power.

1.3 Comparators:

A comparator is a decision making device that is used to compare two voltages or currents and outputs a digital signal which can be interpreted to determine the relation between the two signals. Usually, an operational amplifier with a high gain in its open loop configuration is used as a voltage comparator. It compares one analog voltage level with another analog voltage level, generally known as a reference voltage V_{REF}, and produces an output signal based on this voltage comparison. In other words, this type of a voltage comparator takes two voltage signals as input and determines which is the larger of the two. Due to the high open loop gain of the op-amp, the voltage either swings to positive rail, $+V_{CC}$, or negative rail, $-V_{CC}$, depending on the two voltage levels. Mathematically, this is given by:

$$V_{Out} = \begin{cases} +V_{CC} \; ; \; V_{In} > V_{REF} \\ -V_{CC} \; ; \; V_{In} < V_{REF} \end{cases}$$

Figure 1.9 shows the configuration of an op-amp as a voltage comparator and Figure 1.10 represents the output curve of the comparator.

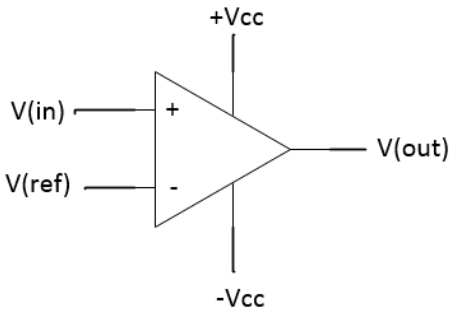

Figure 1.9 Op-amp as a Voltage Comparator

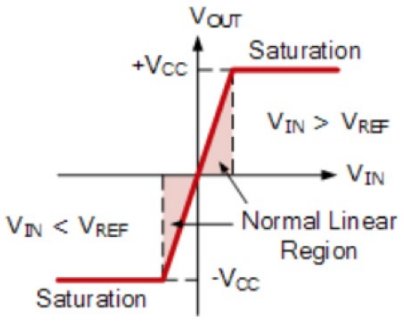

Figure 1.10 Comparator output [34]

It can be clearly seen that if V_{In} is greater than V_{REF}, the output is positive and if V_{In} is less than V_{REF}, the output is negative.

Ideally, the linear region should be as small as possible. Practically, it can only be achieved up to a certain limit and the circuit designed around the op-amp takes this rise and fall time into consideration to avoid non-linear behavior due to this delay.

Another thing to be noticed is that the output of the comparator is dependent on the supply voltage. Theoretically, since the op-amp has very high open loop gain, the output

can go as far as $\pm\infty$. However, practically, which is also obvious from the circuit, the output can only swing as high as $V_{Out} = \pm V_{CC}$.

The V_{REF} is usually generated by a resistive voltage divider circuit. Some other options to generate V_{REF} are a separate battery source, a Zener diode or a potentiometer for a variable reference voltage.

1.4 Types of Comparators:

The most common type of comparator used is a voltage comparator. Bearing this in mind, different types of voltage comparators have been discussed below are:

- Positive Voltage Comparator
- Negative Voltage Comparator
- Window Comparator

1.4.1 Positive Voltage Comparator:

The basic configuration of a positive voltage comparator, also known as a non-inverting comparator circuit, is mathematically written as follows:

$$V_{Out} = \begin{cases} +V_{CC}\ ;\ V_{In} > V_{REF} \\ 0\ ;\ V_{In} < V_{REF} \end{cases}$$

As can be seen from the above equation, V_{Out} is high if $V_{In} > V_{REF}$ and zero if the other way round. The key points to be kept in mind while designing this circuit is that the reference voltage is fed to the inverting terminal and the input is connected to the non-inverting terminal, hence the name non-inverting comparator. Also, the negative supply is

fed to the ground. Figure 1.11 shows the basic configuration of a positive voltage comparator and Figure 1.12 shows the output plot of the comparator.

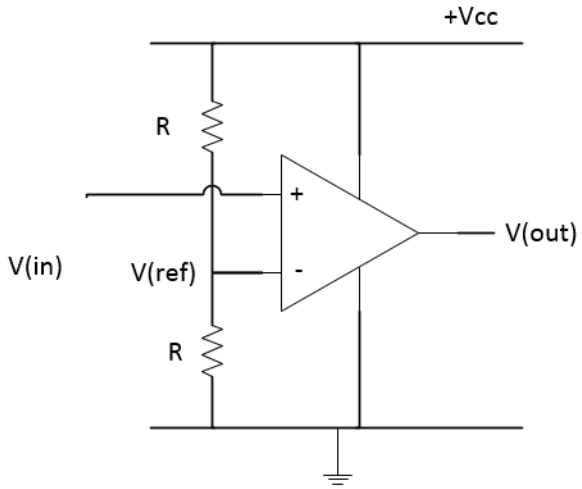

Figure 1.11 Positive Voltage Comparator

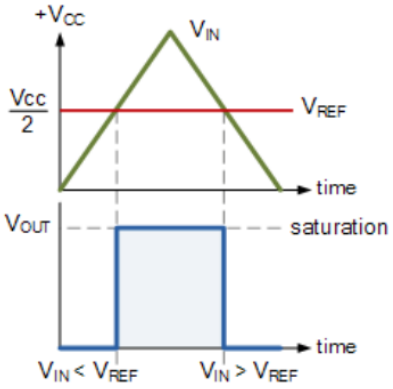

Figure 1.12 Output Plot [34]

1.4.2 Negative Voltage Comparator:

The basic configuration of a negative voltage comparator, also known as an inverting comparator, is mathematically written as follows:

$$V_{Out} = \begin{cases} 0\ ;\ V_{In} > V_{REF} \\ +V_{CC}\ ;\ V_{In} < V_{REF} \end{cases}$$

Clearly, the output of the negative voltage comparator is the opposite of the positive voltage comparator. This is achieved by setting the V_{REF} to the non-inverting terminal and the V_{In} to the inverting terminal, hence the name inverting comparator.

Depending on the requirement of the circuit, either a positive edge detector or a negative edge detector, one of the positive or negative voltage comparator is used.

Figure 1.13 shows the basic configuration of the negative comparator and Figure 1.14 shows the output plot of the circuit.

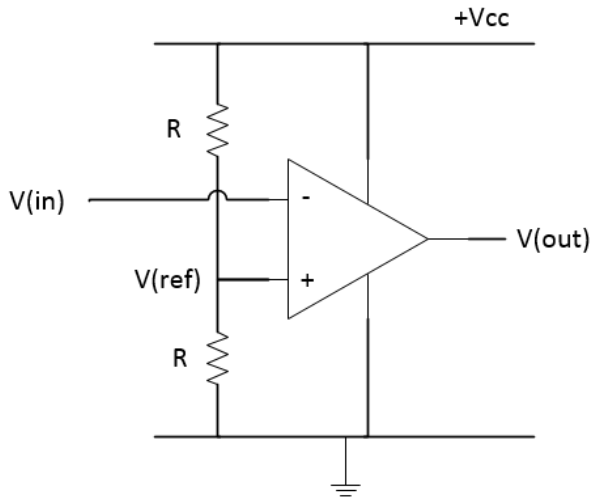

Figure 1.13 Negative Voltage Comparator

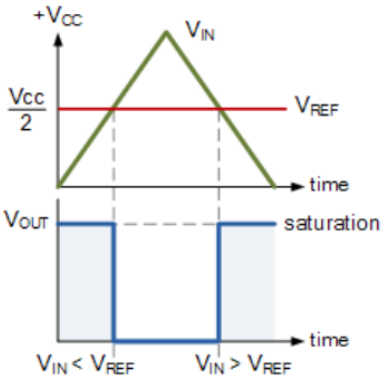

Figure 1.14 Output Plot [34]

1.4.3 Window Comparator:

As the name suggests, this comparator compares within a window of two reference voltages. To achieve this, two op-amps are used, each feeding a separate V_{REF} but the same input. Mathematically, the configuration can be written as:

$$V_{Out} = \begin{cases} +V_{CC}\ ;\ V_{In} > V_{REF,Lower}\ and\ V_{In} < V_{REF,Upper} \\ 0\ ;\ V_{In} < V_{REF,Lower}\ or\ V_{In} > V_{REF,Upper} \end{cases}$$

Figure 1.15 shows the basic configuration of a window comparator and Figure 1.16 shows the output plot of the circuit.

To understand the operation of this comparator, a step-by-step approach is taken.

First, it is to be noted that the first op-amp, A_1, is an inverting comparator and the second op-amp, A_2, is a non-inverting comparator.

When $V_{In} < V_{REF,Lower}$, the output is low. When $V_{In} > V_{REF,Lower}$, the output of A_2 is high. However, at the same time, $V_{In} < V_{REF,Upper}$, which means that the output of the A_1 is also high. The result is a high at the output.

When V_{In} is further increased, it eventually becomes greater than $V_{REF,Upper}$. This means that the output of A_1 becomes low. Therefore, the overall output of the system is low.

This concept can be taken one step further to create multiple windows by adding more stages to this circuit.

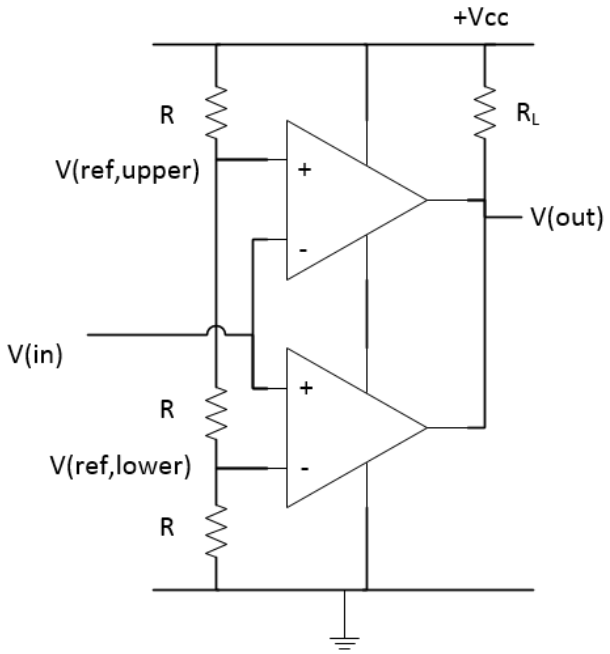

Figure 1.15 Window Comparator

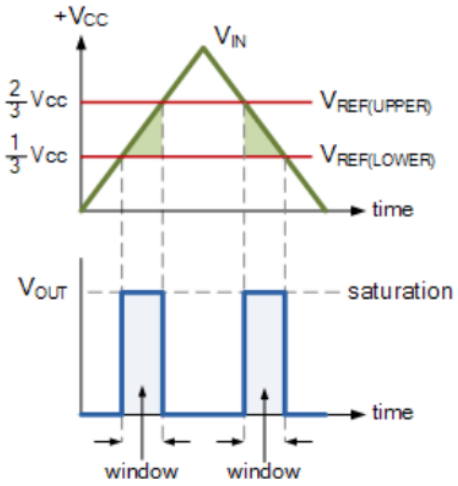

Figure 1.16 Output Plot [34]

1.5 Counters:

A counter is a device which stores and displays the number of times any event has occurred. Often, this number is in relationship to a clock signal. The frequency of the clock signal usually varies with applications. The output is usually in a binary number system. Each pulse applied to the clock input increases or decreases the output of the counter depending on the type of counter.

Usually, a counter circuit is constructed using a number of flip-flops in cascade.

Each output of the counter represents one bit of the output word. For example, in a 74 series counter IC, the output is 4 bits long. This represents 2^0, 2^1, 2^2, and 2^3, or, 1, 2, 4, and 8 respectively. These outputs are usually shown in schematics in the reverse order, that is, the LSB is at the left and the MSB is at the right.

The sequence of outputs is usually tabulated in the form of a truth table. It consists of the number of the pulse, followed by the output of the various bits of the counter.

1.6 Types of Counters:

Counters are broadly classified into the following categories:

- Asynchronous Counters
- Synchronous Counters

1.6.1 Asynchronous Counters:

Asynchronous counter is the type of counter that uses a D Flip-Flop in the counter circuit. The clock input is applied to only the first stage of the circuit, which makes it slower than a synchronous counter. Also, an asynchronous counter has a clock ripple problem. This basically means that a delay gets propagated and added as we go from stage to stage. This delay is created by the gate of each flip-flop. The addition of the delay means that there is a significant amount of delay between the output change in the first stage and the last stage. Figure 1.17 shows the timing diagram for the clock ripple delay:

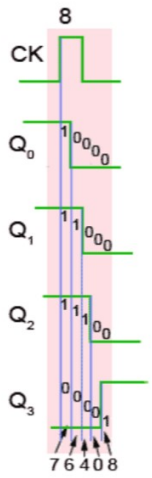

Figure 1.17 Clock Ripple Delay [33]

This clock ripple sometimes causes a different output for a very short time than what should appear. Also, these short lived values cause a series of very short spikes at the output. Even though these spikes are short lived, they affect the output. These are called runt spikes and are considered as interferences at the output.

Even though the above problem deems the asynchronous counter unreliable, this type of counter is still considered as a very simple and effective frequency divider, where the input is derived from a high frequency oscillator and each stage divides the frequency by two. However, this type of counter is not used in case the circuit demands a large number of flip-flops.

Asynchronous counters can further be classified into two categories:

- Asynchronous up counter
- Asynchronous down counter

1.6.1.1 Asynchronous Up Counter:

Figure 1.18 shows a 4-bit asynchronous up counter and figure 1.19 shows the waveforms related to the up counter.

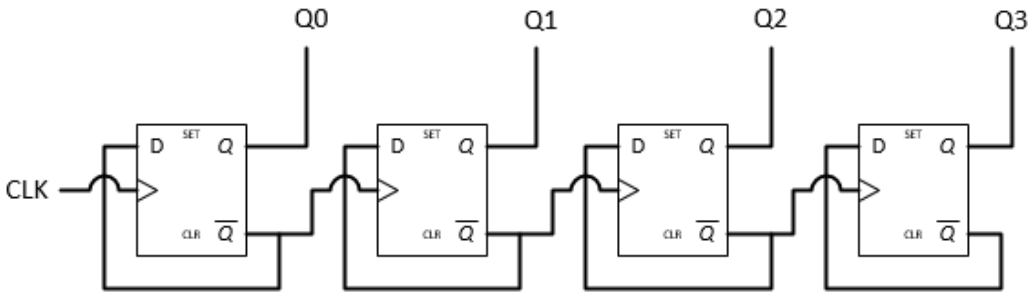

Figure 1.18 Four Bit Asynchronous Up Counter

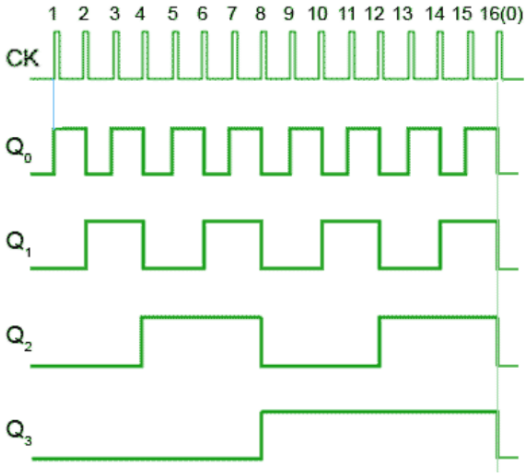

Figure 1.19 Output Waveforms [33]

As seen from the figures 1.18 and 1.19, the clock signal, CK, is fed to FF0. The rising edge of $\overline{Q_0}$ of FF0 triggers FF1 and so on.

Assuming the four outputs as 0000 initially, the rising edge of the first CK pulse triggers FF0 and the output Q_0 goes to logic 1. At the same time, $\overline{Q_0}$ goes to logic 0. At the next CK pulse, Q_0 goes to 0 and $\overline{Q_0}$ goes to 1. This triggers FF1 and Q_1 goes to 1. At the third

CK pulse, Q_0 again goes to 1 and at the subsequent CK pulse, $\overline{Q_0}$ goes to 1, thus triggering FF1 to toggle Q_1 to 0. This in turn toggles $\overline{Q_1}$ to 1, hence triggering FF2. This process continues till Q_0, Q_1, Q_2 and Q_3 all go to logic 0 again at CK (16).

1.6.1.2 Asynchronous Down Counter:

Figure 1.20 shows the block diagram of an asynchronous down counter.

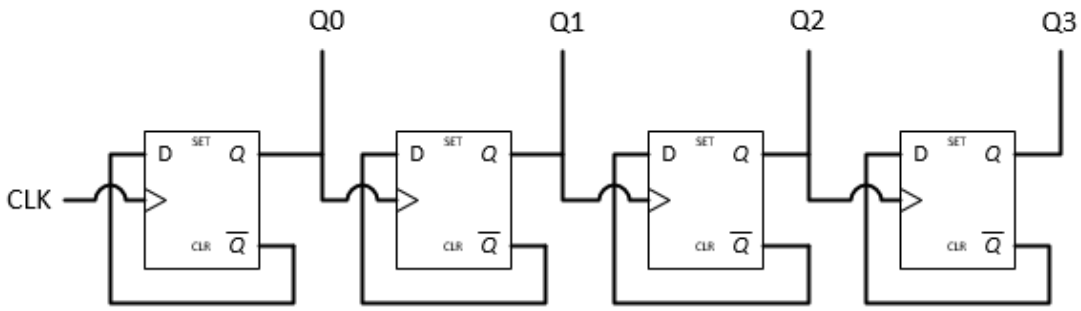

Figure 1.20 Four Bit Asynchronous Down Counter

As seen from the figure, the down counter is just a small modification of the up counter. The clock trigger to the consequent stages is Q instead of $\overline{Q}$. This means the first CK pulse will trigger the output to 1111 and the counter will count down to 0000.

1.6.2 Synchronous Counters:

Synchronous counters are similar to asynchronous counters in that it uses flip-flops to realize up and down counters. But, the similarities end there. On one hand, the asynchronous counters use D flip-flops to realize the counters, while synchronous

counters use JK flip-flops. The reason behind the use of this flip-flop is that the programmable J and K inputs allow easier enable and disable of individual flip-flops at various stages of the count. Also, each flip-flop is fed with the CK signal, which makes this counter much faster than the asynchronous counters. Another advantage of these characteristics of the synchronous counters is the elimination of the clock ripple problem, as the operation is not dependent on the individual flip-flop outputs, rather, it is dependent on the clock pulse that triggers each block.

Synchronous counters can also be sub-categorized into up, down and up/down counters.

1.6.2.1 Synchronous Up Counters:

Figure 1.21 shows the diagram of a 4-bit synchronous up counter.

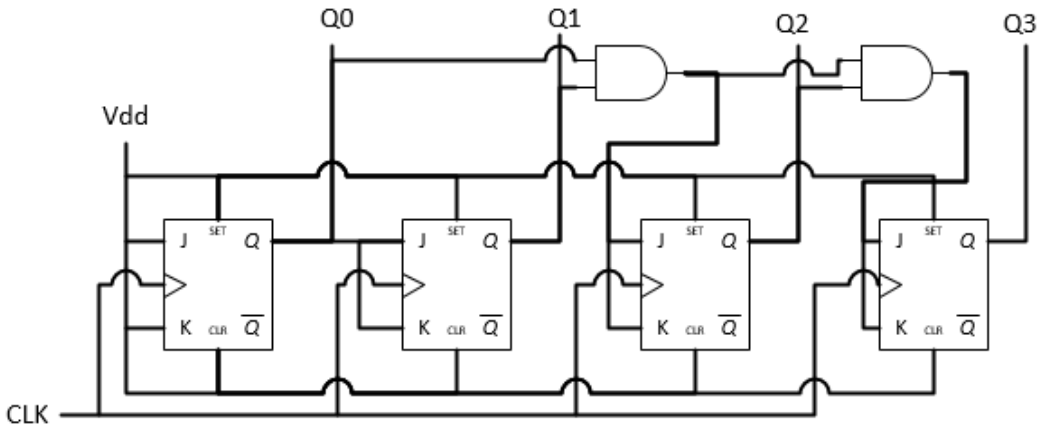

Figure 1.21 Four Bit Synchronous Up Counter

The truth table of this counter looks exactly like the asynchronous counter, just eliminating the propagation delays.

As seen clearly from the figure, the CK pulse is applied to all the flip-flops in parallel. Thus, all flip-flops would have changed their state if D flip-flops had been used as in the asynchronous counters. To avoid this, JK flip-flops have been used. The JK flip-flops toggle their output only if both J and K are at logic 1.

Note that FF0 inputs are permanently kept at logic 1. Now, when the first CK pulse is applied, J1 and K1 are at 0. This means, Q_1 will remain at 0. But, since J0 and K0 are at 1, Q_0 toggle to 1. This toggles J1 and K1 to 1, thus enabling them for the next CK pulse. When the next CK pulse is applied, Q_0 toggles to 0 and Q_1 toggles to 1. This means that the J1 and K1 are now at 0, disabling them for the next CK pulse, on which Q_0 toggles to 1. This enables J2 and K2 for the next CK pulse, upon whose application, the output is now 0100. Similarly, J3 and K3 are enabled if Q_0, Q_1, and Q_2 are all 1 at the same time.

Also to be noted is that the $\overline{PR}$ and $\overline{CLR}$ inputs are also kept at 1 to keep them inactive throughout the count.

1.6.2.2 Synchronous Down Counter:

Figure 1.22 shows the four bit synchronous down counter.

As seen from the figure, the synchronous down counter is just a small modified version of the up counter. The only difference being the triggering of J and K inputs of subsequent blocks is done by the $\bar{Q}$ instead of Q. This means that the counter will act in the exactly opposite way to the up counter.

Assuming the initial state to be 0000, all the four flip-flops are activated since their $\bar{Q}$ is set at logic 1. This means that at the first CK pulse, all four outputs toggle to logic 1 and the output of the system is 1111. It then systematically goes all the way down to 0000.

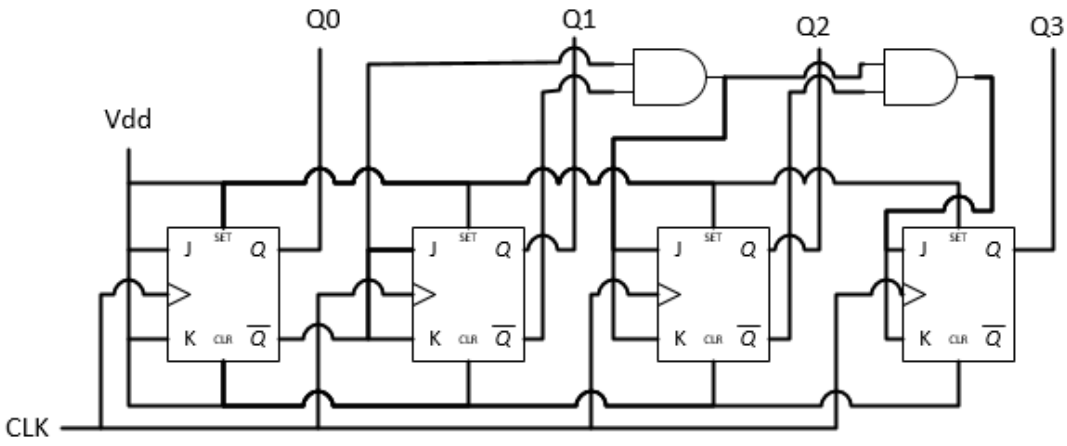

Figure 1.22 Four Bit Synchronous Down Counter

1.6.2.3 Synchronous Up/Down Counter:

Figure 1.23 shows the four bit synchronous up/down counter.

As seen from the figure, the J and K of each block is triggered through a logic diagram which is controlled by the UP/$\overline{\text{DOWN}}$ input. The counter acts as an up or down counter depending on the logic state of this input. If the UP/$\overline{\text{DOWN}}$ is at a logic state 1, the J and K pulse to the next flip-flop is fed through the Q output, thus making it an up counter. On the other hand, if the logic state of UP/$\overline{\text{DOWN}}$ is 0, the J and K pulse to the next flip-flop is fed through the $\bar{Q}$ output, which makes it a down counter.

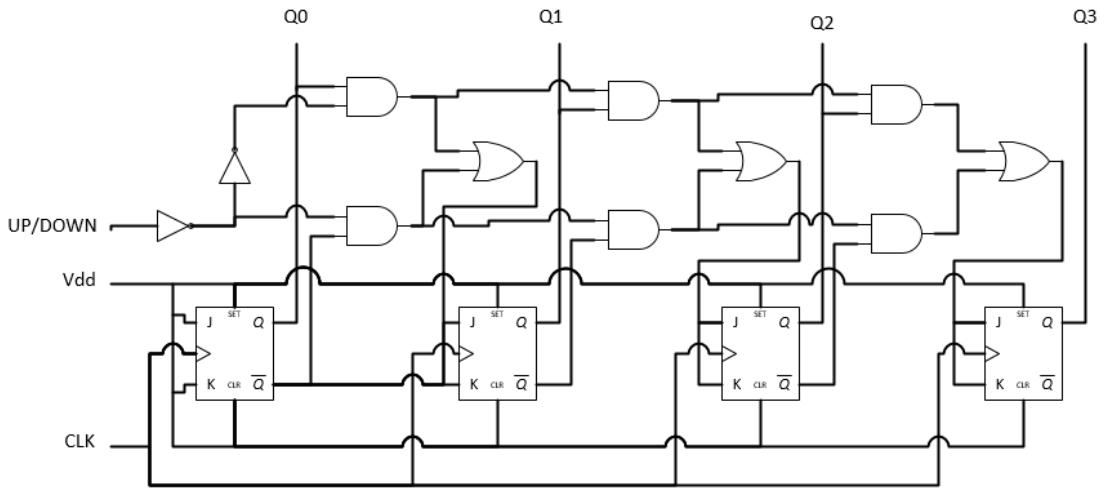

Figure 1.23 Four Bit Synchronous Up/Down Counter

1.7 Research Motivation:

All the recent research and the overall trend of the semiconductor industry suggests the urge to have a digital control of some sort over all their circuits. This was the first motivation to think of something new that can be done digitally. To dwell deeper, the basics of the mixer had to be revisited and each cause and effect had to be studied carefully. Upon further evaluation, the cause of the second order intermodulation distortion discovered as the mismatch between the two branches of the mixer. This meant that a calibration technique was needed that could detect this mismatch and then rectify it.

The most work that had been done in this was to have a digitally controlled resistive load [2, 4]. This wasn't an option as the PMOS load was an essential part of the linearity and

noise improvements. Thus, the only option was to implement a calibration technique that would vary the load by varying the PMOS bias.

One way of achieving this was to digitally turn ON various bias circuits. This would have been too complex to achieve as a switch would have to be implemented to select which circuit to use at the gate of the PMOS.

The second way of achieving this has been implemented in this research. The answer was in current mirrors and its operation. A current mirror sets the current in a transistor by varying the load in the bias circuit. This leads to variation in the current in the bias circuit and eventually leads to a variation in the bias point of the transistor. The PMOS bias is provided through a current mirror. The load for the current mirror circuit is varied digitally. This variation in the load leads to a variation in the bias point of the PMOS and hence provides the leverage to counter act the mismatch in the circuit to improve the IIP2.

Apart from the digital enhancement, this research work houses several third order intermodulation distortion, noise figure and conversion gain improvements. The aim behind employing these techniques was to extract a better performance than a typical mixer topology. As discussed in the following sections, these techniques were largely successful and the specifications achieved in this research were better than the typical mixer. Finally, the merits and demerits of these enhancements will be discussed while suggesting future work possible in this field.

Chapter 2: Mixer Analysis

2.1 Mixer Performance Parameters:

A mixer is rated on its performance based on a few parameters. Depending on these parameters, it is decided whether or not to use the mixer for any specific application. The most important parameters are:

- Conversion Gain
- Port-to-Port Isolation
- 1-dB Compression
- Third Order Intercept Point
- Noise Figure

These parameters depend on various aspects of the mixer, such as the degree of balance in the mixer, the number of noise contributing components in the mixer, input and output matching of the mixer, etc. The following sections discuss each in detail.

2.1.1 Conversion Gain:

The most important parameter determining the performance of a mixer is the conversion gain. Conversion gain is the difference between the output power and the input power. Mathematically, it can be given as:

$$CG = P_{IF} - P_{RF}$$

Where, P_{IF} is the output IF power in dBm,

P_{RF} is the input RF power in dBm,

CG is the conversion gain in dB

The conversion gain is sometimes also written in terms of the voltage. In that case, the conversion gain is written as:

$$CG = V_{IF} - V_{RF}$$

Where, V_{IF} is the output IF voltage in dBV,

V_{RF} is the input RF voltage in dBV,

CG is the conversion gain in dB

If the mixer has a good input and output match, this gain is ideally equal to power gain. This value is negative for passive mixers and positive for active mixers. This is one of the main reasons to choose an active mixer above the passive mixer. Typically, its value is around 9-10dB.

For an active mixer, the conversion gain is given by [16]:

$$A_v = \frac{2g_m R_L}{\pi}$$

On the other hand, the conversion gain for a passive mixer is given by

$A_v = \frac{2}{\pi} \approx -4\ dB$ for a single or double balanced mixer;

$A_v = \frac{1}{\pi} \approx -10\ dB$ for a single balanced mixer

The conversion gain is also dependent on the bandwidth. Larger the bandwidth, lower the conversion gain as it becomes even more difficult to maintain the balance throughout the bandwidth.

Conversion gain is one of the most important mixer metric because it is closely related to isolation and 1-dB compression. Knowing the conversion gain alone, a skilled designer can estimate the performance of the mixer in other tests.

2.1.2 Port-to-Port Isolation:

Isolation is the measure of how much power leaks form one port to another. Port isolation is better if the mixer is balanced. Better the balance, better the isolation. However, this does not prevent isolation altogether. There will always be some isolation present between ports. The challenge is to minimize this isolation as much as possible due to the adverse effects discussed ahead. Generally, three types of isolation parameters are measured:

- LO-RF isolation
- LO-IF isolation
- RF-IF isolation

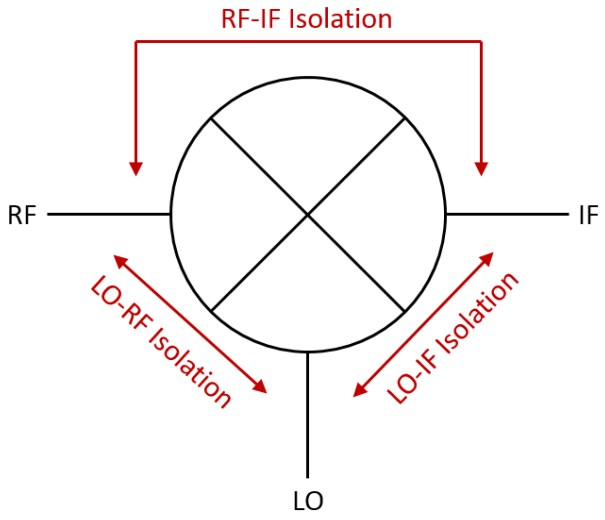

Figure 2.1 Port-to-Port Isolation

Figure 2.1 shows the three different isolation types that pose a challenge while designing the mixer.

First is the LO-RF isolation. This is the measure of the amount of LO signal leaked in the RF terminal. In other words, it can be measured by measuring the signal at the LO frequency at the RF port. Typically, an LO-RF isolation of -20 to -30dB is considered ideal. This isolation is critical because the LO signal can leak through the RF port to cause many scenarios. Firstly, it can reflect back to the mixer RF port to appear as DC component at the output. This causes the ADC present after the mixer to saturate and that will corrupt the analog to digital conversion in terms of resolution. Secondly, it can go further to the LNA present before the mixer and contaminate its output to appear as noise. Thirdly, it can leak to the input of the LNA and reflect back to increase the noise floor. Finally, it can go beyond the LNA to the antenna. Once this happens, the signal can interfere with other signals, or distort the incoming signal at the antenna due to difference in phase and polarization to the signal incoming at the antenna. No matter which scenario occurs, this isolation causes corruption of the signal in one way or the other.

The second isolation is the LO-IF isolation. This means the LO signal leaked into the IF port. This is especially bad problem if the IF and LO frequencies are close. If that is the case, it will contaminate the IF signal and thus the circuitry coming after the mixer, in a similar way as in case of the LO-RF isolation. Beyond this, poor LO-IF isolation leads to reduction in conversion gain. Typically, a value of -20 to -30dB is considered good enough.

Final isolation metric is the RF-IF isolation. Usually, this isolation is not a major problem for system designers as the IF and RF frequencies are usually far apart and the RF signal is filtered out. Also, the amplitude of the RF and IF signals are usually magnitudes smaller than the LO signal and don't cause a lot of problems. Typically, its value lies between -20 to -30dB. However, RF-IF isolation does cause problems for a mixer designer. Poor isolation can cause a drastic effect on the conversion efficiency. On the other hand, a good RF-IF isolation leads to a boost in the conversion gain.

2.1.3 1-dB Compression:

1-dB compression point is one of the measures of the linearity of a mixer. Under linear conditions, the conversion gain of the mixer doesn't vary with variation in the input power. However, as the input is further increased, the mixer moves to non-linear region and the conversion gain begins to drop. The point where the conversion gain drops by 1 dB is called the 1-dB compression point. It is usually written mathematically as [25]:

$$P_{1-dB} = 10 * log\left(\frac{0.145|\alpha_1|}{|\alpha_3|}\right)$$

This equation has a complex solution due to difficulty in measurement of the constants. Thus, it is typically measured graphically. Figure 2.2 shows how this is done.

As can be clearly seen from the graph, the curve behaves linearly in the initial phases. As the input is further increased, this becomes non-linear and eventually, the gain reduces by 1dB. This point is the 1-dB compression point.

Theoretically, this point occurs when the input RF signal can no longer be considered as a small signal. Under the linear region, the LO power totally overpowers the RF signal and

controls the switching pair totally. However, as the RF power increases further, it competes with the LO power and leads to some non linear behavior. At this point, it is assumed that the switching action is compromised. It is said that the mixer input can be a maximum of 3 dB below the 1-dB compression point.

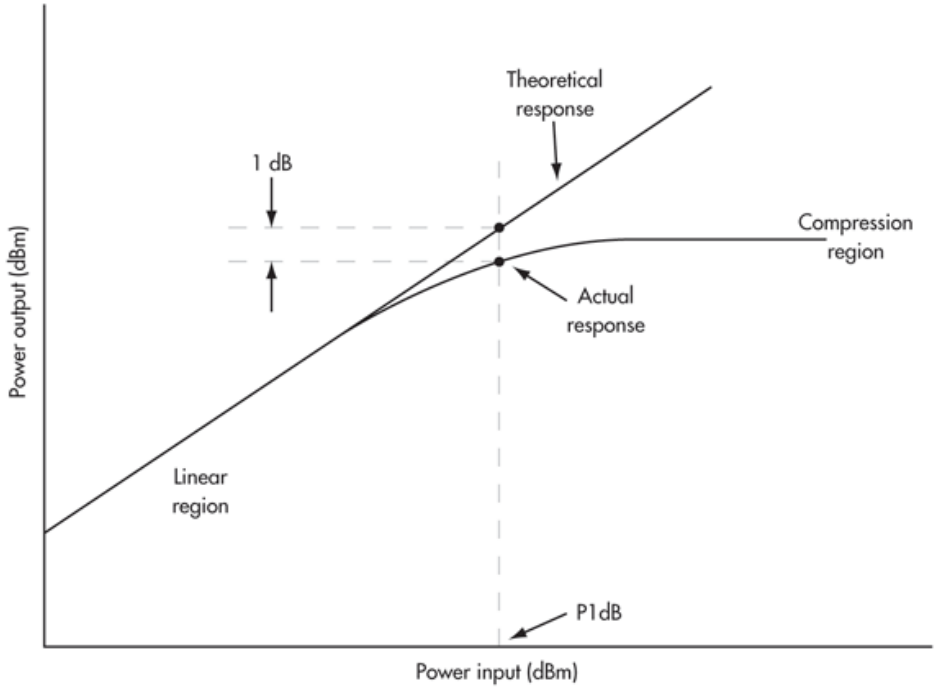

Figure 2.2 1-dB Compression Point Measurement [36]

As the mixer nears the 1-dB compression point, among other effects, increased levels of intermodulation distortion are noticed and the conversion gain drops. Also, any mixer imbalance is exacerbated and it leads to overall degradation in the conversion efficiency. This can be improved by increasing the LO swing so that more and more RF power is needed to overpower the LO signal. However, the LO signal can't be increased infinitely

as that would lead to tremendous loss of headroom and will affect the mixer more than helping it.

2.1.4 Third Order Intercept Point:

The other linearity parameter to be considered apart from 1-dB compression point is the IIP3 of the mixer. This non linearity occurs due to the third order intermodulation products, which are in the vicinity of the RF or LO frequencies. These components are $(\pm n * \omega_1 \pm m * \omega_2)$, where $(n + m) = 3$. The components close to the RF or LO frequency is $(2 * \omega_1 \pm \omega_2)$ and $(2 * \omega_2 \pm \omega_1)$, given that the interferer is close to the RF or LO frequency. This means that the presence of a strong interferer can cause major distortions.

Graphically, IIP3 point is defined as the intersection point of the extrapolated output curve and the third intermodulation curve. Figure 2.3 shows the measurement of the IIP3.

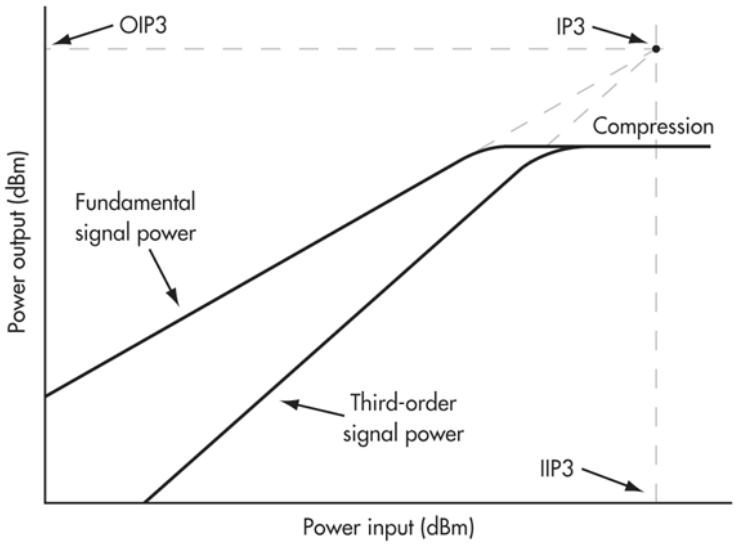

Figure 2.3 IIP3 Measurement [36]

Another reason that this is an important parameter due to the fact that the third order intermodulation product rises at a rate of 30 dB/decade, which is three times the rate of increase of the fundamental output power.

Usually, IIP3 of a system is about 10 dB away from the 1-dB compression point.

2.1.5 Noise Figure:

Noise figure is defined as the signal to noise ratio of the input to that of the output. Mathematically, it can be given as:

$$NF = \frac{S_{in}/N_{in}}{S_{out}/N_{out}} = \frac{SNR_{in}}{SNR_{out}}$$

This noise figure can be specified as either single sideband (SSB) or a double sideband (DSB) noise figure. As discussed earlier, the SSB noise figure is for the SSB conversion mixers, and the DSB noise figure is for the DSB conversion mixers. Typically, the SSB noise figure is greater than the DSB noise figure by 3 dB [16], that is,

$$NF_{SSB} \cong NF_{DSB} + 3dB$$

The RF transistor noise is characterized as a current source and is characterized mathematically as [25]

$\overline{\iota_{nd}^2} = 4KT\gamma g_{d0}\Delta f$ for the drain thermal noise,

$\overline{\iota_{ng}^2} = 4KT\delta g_g\Delta f$ for the gate thermal noise

Where, g_g is given as [25]:

$$g_g = \frac{\omega^2 C_{gs}^2}{5 g_{d0}}$$

The gate thermal noise is also correlated to the drain thermal noise through a correlation factor, c, which is given as [25]:

$$c = \frac{\overline{i_{ng}} * \overline{i_{nd}}}{\sqrt{\overline{i_{ng}^2} * \overline{i_{nd}^2}}}$$

In an active mixer, there are two types of noise present:

- Flicker Noise
- White Noise

Flicker or $1/f$ noise is the noise that is dominant at extremely low frequencies. This noise is reduced by using a PMOS load rather than an NMOS load. Another alternative is to use a polysilicon resistor, which doesn't have $1/f$ noise. However, large loads can not be realized using this resistor. This noise is critical in DC or low IF architectures. The major flicker noise contributors are the switching pair transistors. It can be improved by higher device f_t.

White noise or thermal noise is contributed by the gate and drain of each transistor. More the number of transistors, higher the white noise. This noise is proportional to the transconductance of the g_m stage, load resistance and DC bias current. However, large g_m and load resistance are desirable to boost the conversion gain. Thus, a compromise has to be arrived upon.

2.2 Nonlinearities in Mixers:

Two major nonlinearities in mixers are:

- Single-Tone Intermodulation Distortion
- Multi-Tone Intermodulation Distortion

2.2.1 Single-Tone Intermodulation Distortion:

These are the harmonic mixing products caused by nonlinear mixing of RF and LO signals, that is the period where the conversion gain is lower than that in the linear region. One of the major goals in mixer design is to limit the strength of this nonlinearity.

An important equation to keep in mind while discussing this distortion is the frequency conversion by a mixer:

$$f_{IF} = n * f_{RF} \pm m * f_{LO}$$

The key features of a single-tone intermodulation distortion are in double and triple balanced active and passive mixers are [32]:

- Balancing improved the even n by even m, even n by odd m and odd n by even n harmonic levels by about 25-30 dB
- Only the odd n by m terms exist at the IF port
- The single-tone intermodulation distortion improves with lower RF power
- Increasing the LO power does not necessarily improve this distortion

2.2.2 Multi-Tone Intermodulation Distortion:

Multi-tone intermodulation distortion means that multiple tones enter the mixer a specific port. It is a form of common mode mixing between multiple tones entering the RF port and between the tones and LO, which creates massive distortion. Thus, this is a serious

problem from a system point of view as it generates distortion that lie within the IF band of interest of the receiver.

The generation of this distortion depends on the nonlinearities of the transistors and the overall balance of the mixer. The figure of merit for the multi-tone performance of a mixer is specified by its IIP3. As specified earlier, this is especially harmful due to the increased rate of increase of the intermodulation power with respect to the fundamental power.

2.3 Highly Linear Active Mixer Architectures:

This section details the popular linear active mixer architectures. Three of the linear active mixers have been discussed:

- Source Degenerated Gilbert Cell Mixer
- Common Gate Transconductor Mixer
- Resistive Switch Mixer

Each mixer configuration has positives and negatives. Each has been discussed below.

2.3.1 Source Degenerated Gilbert Cell Mixer:

A standard double balanced Gilbert cell mixer provides good port-to-port isolation along with decent conversion gain. To improve the linearity of this mixer, the source of the transconductor stage is degenerated. A high inductive reactance is inserted between the source and ground through a current source. Figure 2.4 represents the proposed mixer:

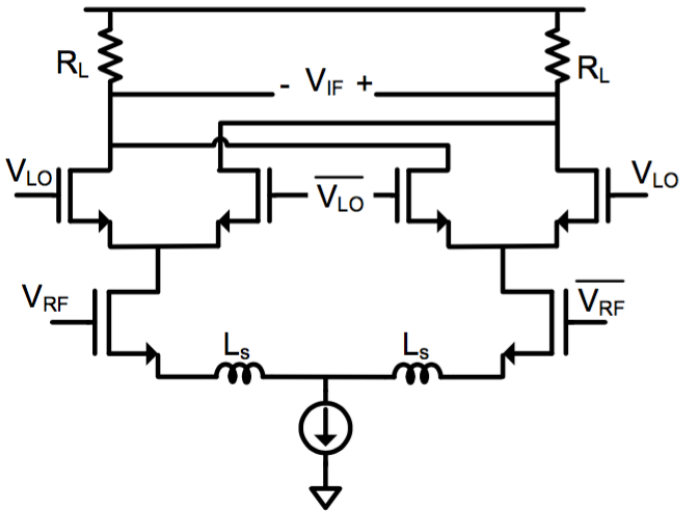

Figure 2.4 Source Degenerated Gilbert Cell Mixer [17]

The connection of an inductor at the source of the transconductor leading to a current source helps improve the PSRR. Also, the current source provides a high impedance at all frequencies. This helps in improving the common mode rejection drastically. This improves the single-tone intermodulation distortion of the mixer. However, this affects the voltage headroom of the transistor and also costs a lot of area due to the two large inductors.

2.3.2 Common Gate Transconductor Mixer:

Common gate transconductor mixer is another example of a highly linear active mixer. The most useful property of a common gate transconductor is a broadband input matching. However, this is not as useful when used in a mixer as it is driven on-chip and matching isn't a big concern for designers. However, the linearity of this mixer configuration is very high. On the flip side, the noise figure of a common gate

transconductor mixer is high. Also, isolation is not as good as a common source configuration. Figure 2.5 shows a schematic of a common gate transconductor mixer.

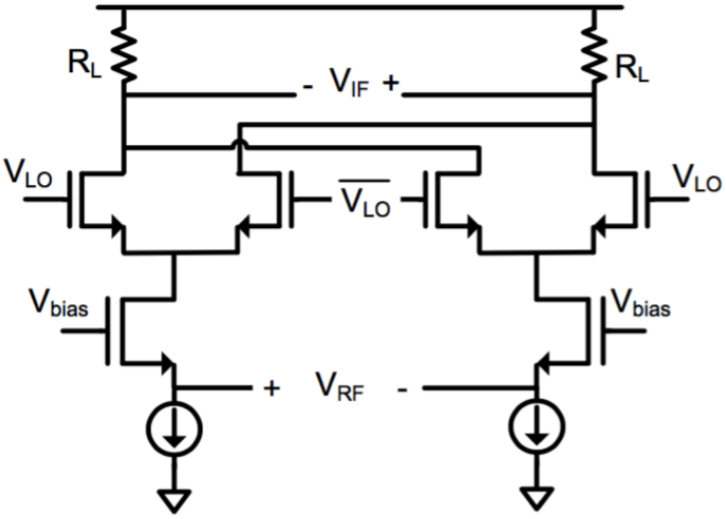

Figure 2.5 Common Gate Transconductor Mixer [17]

2.3.3 Resistive Switch Mixer:

This is the third type of mixer configuration for linearity. The main difference in this configuration is that the switching transistors operate in the linear region. This topology makes use of an op-amp to improve linearity. Use of the op-amp limits the bandwidth of operation of the mixer. It also employs low pass filters to cater to this limit in the region of operation. Figure 2.6 shows the schematic of the resistive switch mixer.

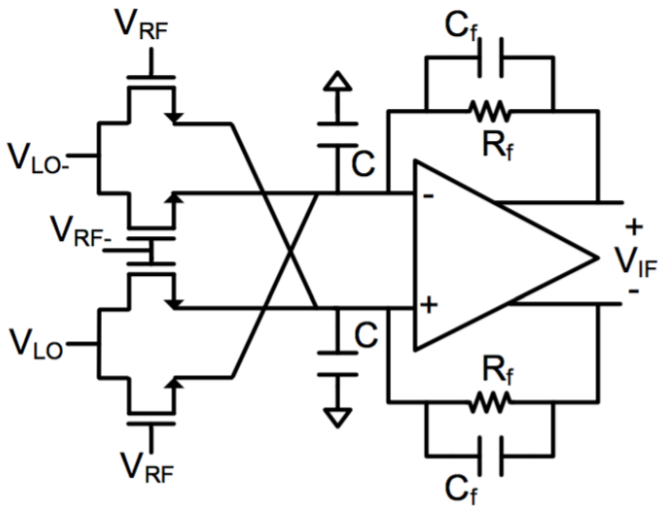

Figure 2.6 Resistive Switch Mixer [17]

The two capacitances form the low pass filter with the resistors to allow only low frequency signals through the op-amp and filter out other high frequency signals.

The linearity of this mixer is much better than the Gilbert cell mixer and the conversion gain is better as well. However, as can be guessed by looking at the design, the increased number of resistive components and the inclusion of the op-amp affects the noise figure of the mixer. Also, the isolation is reduced due to capacitive coupling of LO and RF signals.

Chapter 3: Mathematical Modeling and Calculations

3.1 Mixer:

As seen in the previous section, multiple mixer schematics were evaluated. Based on the evaluations, the double balanced Gilbert cell mixer was chosen as the design to be implemented. The reason behind this decision was the fact that the double balanced Gilbert Cell mixer provides a good gain, decent linearity and good port to port isolation. However, a few modifications were made to account for added linearity and lower noise while at the same time produce higher gain [1]. Figure 3.1 shows the mixer design that was implemented.

The first modification is the implementation of a PMOS load. As discussed earlier, the PMOS load has a better flicker noise performance than an NMOS load. The key parameter to be kept in mind while designing the PMOS is to increase the R_{OUT} of the PMOS.

The second modification is the implementation of C_P. This capacitor along with the R_{OUT} of the PMOS forms a low pass filter to filter out all high frequency components.

The third modification is the LC filter [1]. The second order modulation distortion and the $1/f$ noise of the switching pair makes the design challenging. The fact that the second order intermodulation products down converted from the side-bands at LO

frequency add up at the mixer output make the design even more challenging. To improve the IIP2 performance, the LC tank is employed. The inductor and the parasitic capacitor are chosen to resonate at the LO frequency. This reduces the down converted IM2 current by a factor of Q. This leads to a significant improvement in the IIP2 of the circuit. The LC filter also improves the $1/f$ performance as the inductor cancels out the parasitic capacitor responsible for $1/f$ noise transfer to the output.

The next modification is the implementation of the CCPD [6]. The IIP3 of the mixer is affected by the g_m'' of the input transistor. The role of the CCPD is to cancel this effect. This is achieved by maintaining the CCPD transistors in cut-off region. This is done due to the negative value of g_m'' of an NMOS transistor in its cut-off region. Theoretically, an ideal CCPD would lead to an infinite IIP3. However, this is not possible practically. In reality, the IIP3 improves by about 20-30 dB if the design is done carefully.

Finally, a transconductor stage has been added to generate the current in the differential branches instead of using the input transistors as the current setting transistors [1]. This is done to improve the IIP2 of the system. The high IIP2 of a fully differential transconductor is owed to the fact that it has low common mode gain at low frequency. At low frequency, the current generators degenerate the input transistors, thus providing a low gain at low frequency, leading to a high IIP2. At RF, the capacitors C_{TC}, ground the two current sources. This is helpful as it reduces the third order intermodulation distortion, thus improving the IIP3.

The following sections describe the mathematical modeling of the different components of the mixer.

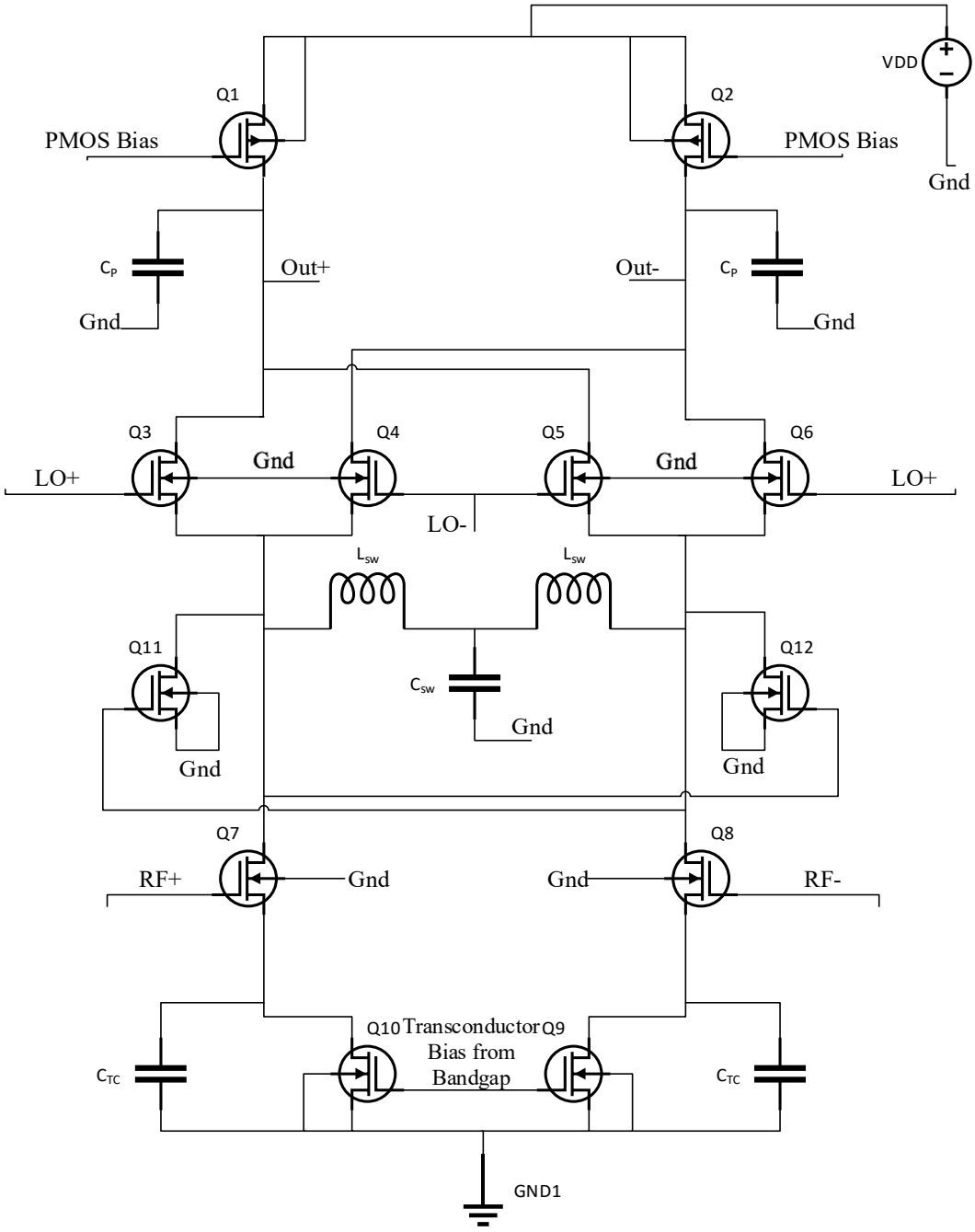

Figure 3.1 Mixer Circuit Diagram

3.1.1 PMOS Load:

The main aim behind designing the PMOS load is to improve the R_{OUT} of the circuit. This is achieved by increasing the length and keeping the width low. The second advantage of this design is that the overdrive voltage is low. This means that more voltage is available for the subsequent stages, thus ensuring operation in saturation region for all the transistors. The size chosen is 187.5µm/600nm with a bias of 610mV. The second advantage of increasing the length is that the device now a long channel device, thus reducing the short channel effects that might affect the circuit performance. The g_{ds} achieved is around 1mS, that is, the R_{OUT} is around 1k Ω.

3.1.2 Switching Pair:

The main idea behind designing the switching pair is to keep the length low. This has two fold advantages. First is that the f_t of the device is high, thus reducing the $1/f$ noise performance. Secondly, this increases the $V_{d,sat}$ of the transistors. The advantage of the increased saturation voltage is that this increases the voltage swing at the LO port. As discussed earlier, the increased voltage swing leads to higher linearity. The ideal voltage swing at the LO port is given by:

$$V_p = \sqrt{2} * V_{d,sat}$$

This means that the higher the saturation voltage, higher the allowable swing. However, after one point, the high voltage swing starts hurting the mixer. Keeping this in mind, the sizing of the transistor is kept as 510µm/300nm. This helps achieve a saturation voltage of about 100mV. This value is around the sweet spot as it gives us 280mV peak-to-peak LO swing.

3.1.3 LC Filter:

As discussed earlier, the role of the LC filter is to reduce the IM2 currents by a factor of Q and also reduce the noise figure of the switching pair and the input transistor. To achieve this, the inductor is made to resonate out the parasitic capacitance at the LO frequency [1]. Each of the two inductors is kept at 10nH at 2GHz and 3.1nH at DC. The inductor simulations have been shown in the results section. The capacitance has been set to 3.6pF to provide the AC ground to provide a path for the IM2 currents to pass.

3.1.4 Input Transistor:

The g_m of the input transistor is the only factor to be considered while sizing the input stage. To achieve a high g_m for the given current of 2mA, the sizing of the input transistors is 325.5µm/250nm. The low length also helps to improve the flicker noise performance. The g_m achieved by this is round 37mS.

3.1.5 Transconductor Stage:

The transconductor stage affects the common mode second order intermodulation distortion. The common mode second order transconductance of a fully differential transconductor stage is given by [1]:

$$G_2^{CM}(\omega, \omega) \cong \frac{g_{2,rf}}{2(1 + g_{m,rf} * r_{ds,tc})}$$

Where, $g_{2,rf}$ is the second order transconductance of the input transistor

$r_{ds,tc}$ is the output resistance of the transconductor stage

From this equation, a low transconductance and a low output resistance is required. However, looking at the equation for the transconductance of this stage, it is written as [1]:

$$G_m(\omega) = \frac{g_{m,rf}}{1 + g_{m,rf} * r_{ds,tc}} * \frac{1 + j\omega * C_{TC} * r_{ds,tc}}{1 + j\omega * \frac{C_{TC} * r_{ds,tc}}{1 + g_{m,rf} * r_{ds,tc}}}$$

From the above equation, it can be seen that increasing the transconductance of the input transistors and reducing the output resistance of the transconductance stage improves the overall transconductance. To compromise between the two, the transconductance of the input transistor is set at 37mS and the output resistance is set at 150Ω. This was done keeping in mind that the other, more effective linearization enhancement stages used in the circuit can compensate for this stage.

The sizing of this stage is set at 798.1µm/700nm to set a current of 2mA in each branch of the mixer.

3.1.6 CCPD:

The design of the CCPD that is employed achieves a negative g_m'' which is almost equal in magnitude as the g_m'' of the input transistors [6]. In order to do this, sizing of 300µm/500nm and a DC bias of 197mV has been set. The gates of the CCPD have been AC coupled with the drain of the input transistor. The output of the CCPD is fed back to the drain of the RF transistor. This leads to cancellation of the g_m'' and its effect can be seen from the plots in the results section.

3.2 Folded Cascode Amplifier:

A folded cascode amplifier with a very high open loop gain was used to implement the comparator. Figure 3.2 shows the circuit implemented in the design.

The transistors Q1 and Q2 are to take the differential inputs, in this case the IF differential outputs. The following equations were used to design this circuit.

Assuming the unity bandwidth as 200 MHz [37],

$$BW = 2\pi * g_m$$

This gives the value of g_m as 3.2mS. Calculating the current by the following equation [37]:

$$I_d = \frac{1}{2} * g_m(V_{GS} - V_t)$$

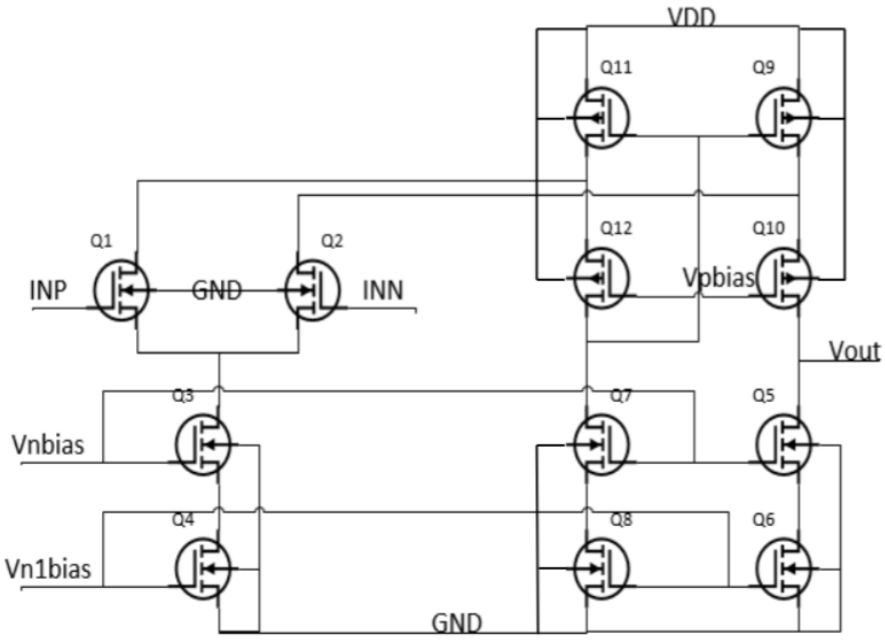

Figure 3.2 Folded Cascode Amplifier Circuit

The current is calculated as 160µA, considering the overdrive voltage as 0.1V.

This gives the W/L ratio of the input NMOS transistors as 40.

The total current through the tail NMOS is, thus, 320µA. This gives the W/L ratio of the tail NMOS as 112.

Further, the tail current is 90% of the current through the PMOS transistors. This gives the W/L ratio of the PMOS as 360.

The remaining of the current goes through the differential NMOS pair. Their W/L ratio is thus calculated as 56.

These values gave the unity gain bandwidth as 235MHz and the phase margin as 66˚.

3.3 Up Counter:

Figure 3.3 shows the up counter circuit that was implemented. Clearly, it is a synchronous up counter. The clock signal is generated at a frequency of 39MHz. This value was obtained from the wireless standards, that state the clock frequencies for various bands.

The EN bit is the output of the comparator. When there is a mismatch, this bit goes high and activates the up counter. The counter counts till the EN bit goes low. In other words, when the mismatch is within acceptable limits, the EN bit goes low and this ensures the counter stops counting and this state is held.

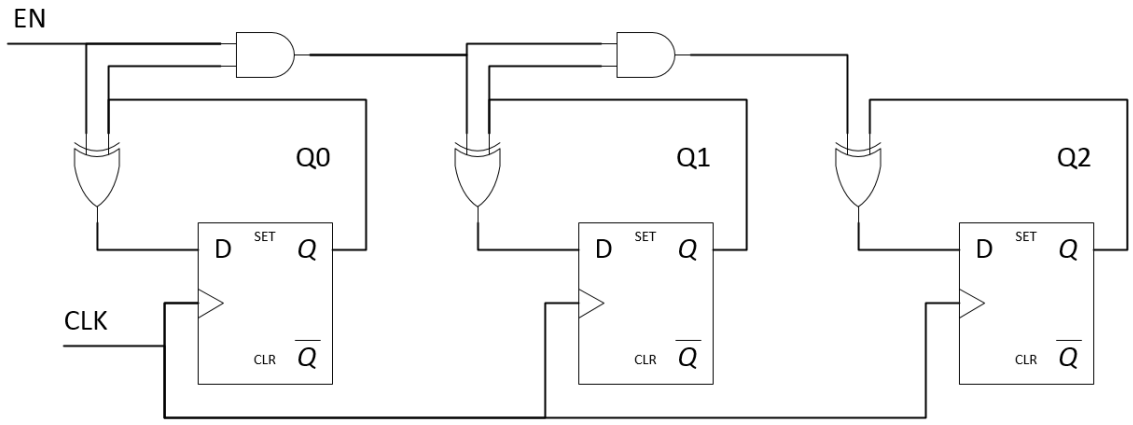

Figure 3.3 Up Counter Circuit

3.4 Digitally Controlled Linearity Enhancement Stage:

This stage makes use of the comparator and the counter described in the previous sections. A point to be noted is that the research in this thesis accounts for the voltage mismatch between the two branches of the mixer and a technique to reduce this mismatch. The main idea behind the enhancement is that when a mismatch occurs, the PMOS load bias point is varied, which leads to a reduction in the mismatch between the two branches of the mixer. This is done by switching the comparator output to logic 1 upon the introduction of a mismatch. This enables the counter, which starts counting from 000 to 111. When the EN bit settles at 0, the counter stops counting and the final state is maintained. Figure 3.4 is the block diagram representing the enhancement process.

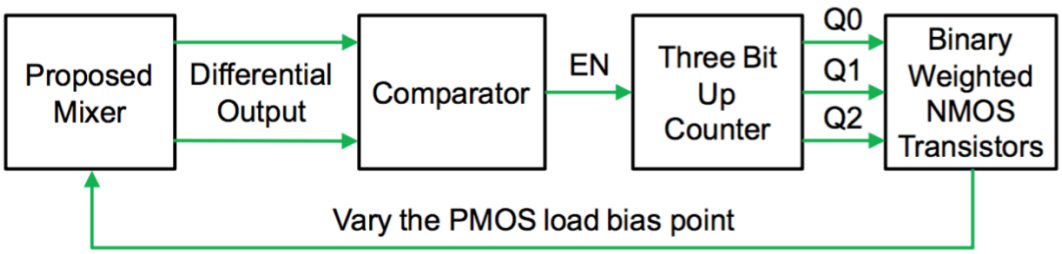

Figure 3.4 Digitally Controlled Linearity Enhancement Stage

As seen from the block diagram, the output of the up counter is connected to a series of three binary weighted NMOS transistors. These NMOS transistors are connected to the load of the current mirror used to bias the PMOS loads. Depending on the final count of the counter, the load of the current mirror settles on one value. This leads to the current being settled to one value, or in other words, the bias of the PMOS transistors get fixed.

Figures 3.5 and 3.6 show the outputs of the comparator and the counter for a sample offset introduced in the circuit.

It is to be noted that figure 3.6 has been intentionally offset to compare the behavior of the three bits with respect to each other. As it can be seen, the final output is 100. This means that the third transistor is turned ON. This maintains the PMOS bias at some point and this improves the IIP2 of the system.

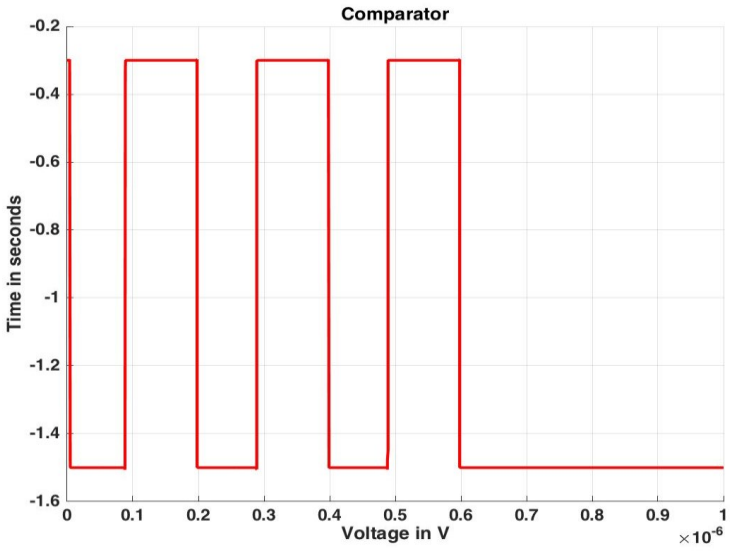

Figure 3.5 Comparator Output

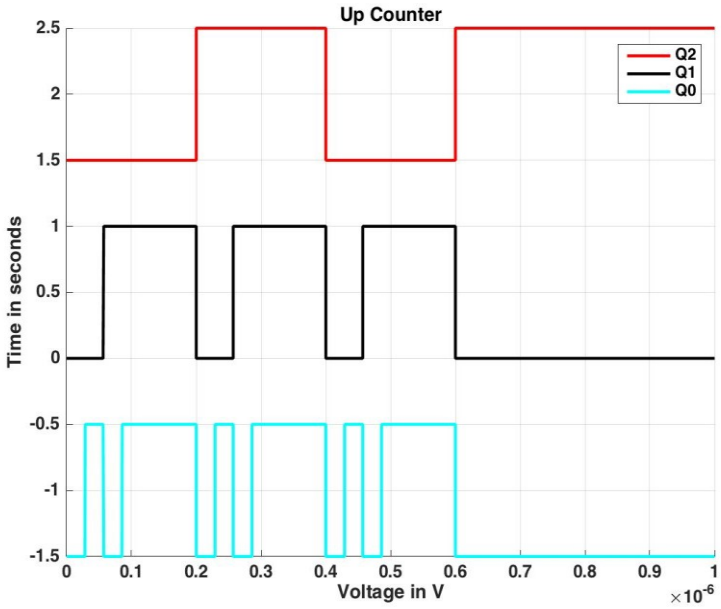

Figure 3.6 Up Counter Output

Chapter 4: CppSim Analysis

4.1 Behavioral Modeling and Verilog AMS:

SPICE has long been the simulator of choice when it came to simulation of analog or mixed signal circuits. With all the digital simulations being done in Verilog or HDL, the simulation time has always been an issue. The bigger issue, however, has been the integration of digital and mixed signal systems. Thus, there was always a gap between modeling the circuits and integrating the modeled results with the physical design. The older interface of SPICE also makes simulation time longer, as well as the design being exclusive to the designer. Along with this, debugging SPICE models becomes a big issue. Another issue with SPICE was that it was technology independent at the time of release. This meant that new SPICE models had to be developed with evolving technology. These problems were responsible in BSIM4 transistor level model development and an adoption of HDL as the primary hardware language [22].

In the meantime, the digital industry grew exponentially, especially with Electronic Design Automation (EDA) techniques improving the simulation speeds tremendously. Automation of the design flow was possible and soon, working with millions of transistors was no longer an issue. On the other end of the spectrum, analog design couldn't be automated, even though the scale of transistor use is much less. This also

meant that relative error to digital simulations became high [22].

This led to the development of Verilog AMS. Verilog AMS is a version of VHDL and is used to model and describe analog mixed signal and digital subsystems, even though VHDL is used to mainly preferred for digital modeling. The main advantage of Verilog AMS is its ability to provide a co-simulator system to analog, mixed signal and system modeling. This also has a superior speed as compared to Verilog. This makes it an attractive choice in simulations of high speed, complex circuits, not just limiting it to PLLs, but also ADCs, Clock Trees, RF Digital Control Modules, etc. The only drawback is its inability to account for the non-linearity introduced by the transistor at the physical level and the difficulty in synthesizing code into schematics. However, this is the drawback of behavioral modeling and HDL as a whole, not just Verilog AMS. Nonetheless, it has simplified designing in any domain, so much so that designers prefer to implement the circuits in Verilog before the actual transistor design is taken up [22].

Thus, it can be said that, if a design is implemented as a behavior model before diving into transistor level design, it will become more transferrable. The designs can be verified at the behavioral level and later, the changes that need to be done can be executed at the transistor level. The behavioral model performed with all the possible nonlinearities in the circuit will especially be useful if the design is to be transferred from one node to the other, say 90nm to 45nm. This also allows the opportunity to propel innovations in the existing designs without deeming the effort too complicated. The performance improvement is now an easy function of the additional non-linearity introduced by the device, rather than designing the circuit with a large number of error sources, as the

behavioral model will give the designer an insight on what to look for when debugging the error sources [22].

4.2 GMSK Transceiver Modeling:

A GMSK (Gaussian Minimum Shift Keying) Transceiver was modeled as an example of the capabilities of CppSim. The architectural evaluation was done in CppSim and the behavioral models were realized using Verilog. These models are ideal and don't have any nonlinearity associated with them.

Figure 4.1 shows the model of the transceiver in CppSim.

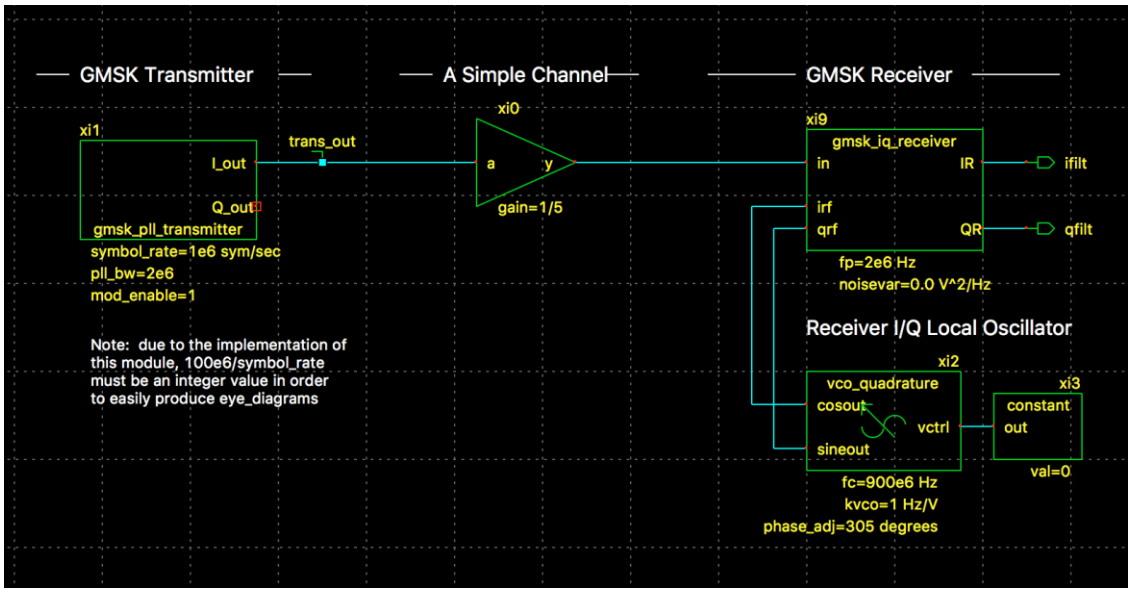

Figure 4.1 GMSK Transceiver Model

The model simulated in CppSim consists of a transmitter, a model of a channel with some

loss and a receiver. The receiver receives the clock from a Local Oscillator.

Each of these models have their own architectural block diagram and their own behavioral model. Each block has a basic set of parameters that can be varied to obtain the desired result. The following section dwells into each model closely.

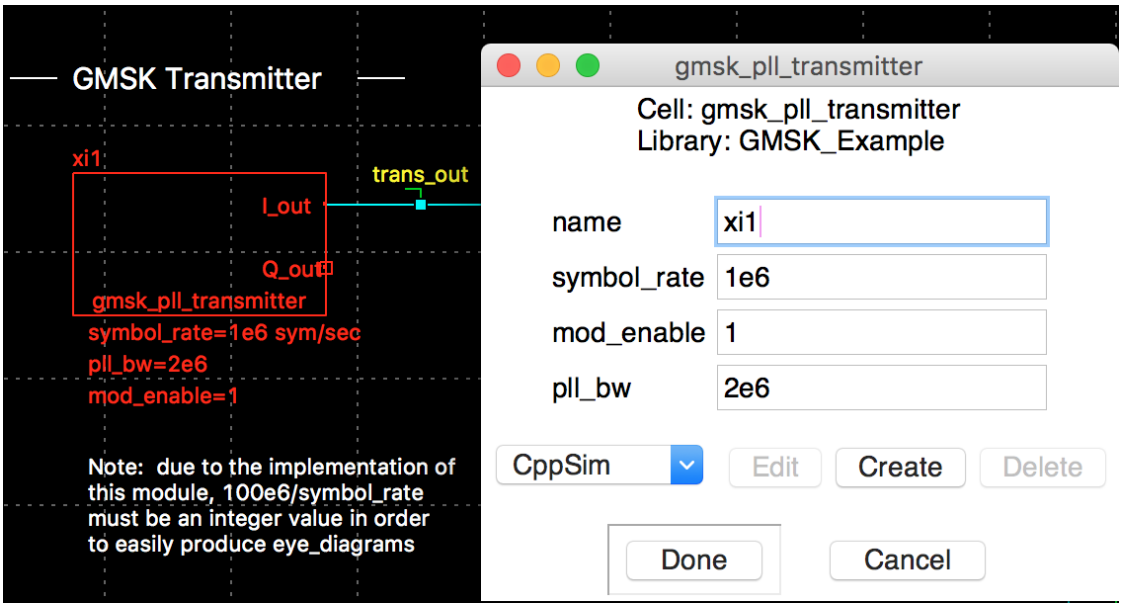

Figure 4.2 Transmitter Modeling

Figure 4.2 shows the modeling of the transmitter. As can be seen, the symbol rate, enable and the PLL bandwidth can be varied in this model. The architecture of the transmitter is as shown in figure 4.3.

The architecture employed is a PLL with an I/Q mixer in its feedback loop. The function of the I/Q mixer is to vary the phase at the transmitter output in accordance with the I/Q signals generated by an I/Q generator block.

The I/Q generator generates this signal by having a binary data generator. The bits

generated in this block are then smoothened using a Gaussian filter. The stream is then accumulated to result in a frequency modulation signal, f_{mod}, which forms a modulated phase signal, Φ_{mod}. This modulated signal is then used to generate the sine and cosine functions in order to create the I/Q signals [40].

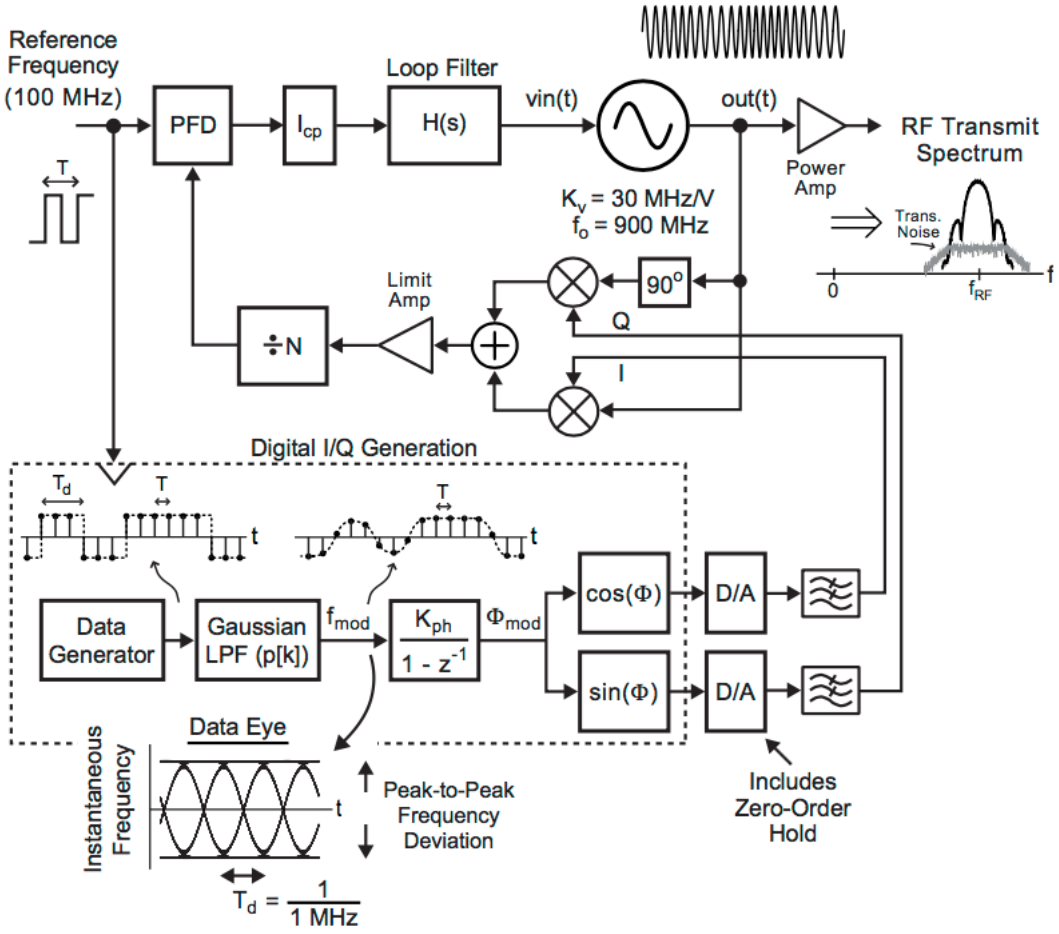

Figure 4.3 Transmitter Architecture [40]

The feedback loop consists of an adder that adds the I/Q signals after mixing. This is passed through a limit amplifier, divided by a constant N, and fed to the PFD. A loop

filter is employed to remove any doubled frequency component. This filter is usually a low pass filter. The output is then fed to the VCO, whose output is amplified by a power amplifier and then transmitted [40].

Figure 4.4 shows the modeling of the receiver. As seen from the figure, the parameters available to change the behavior of the receiver are frequency and noise of the receiver in V^2/Hz.

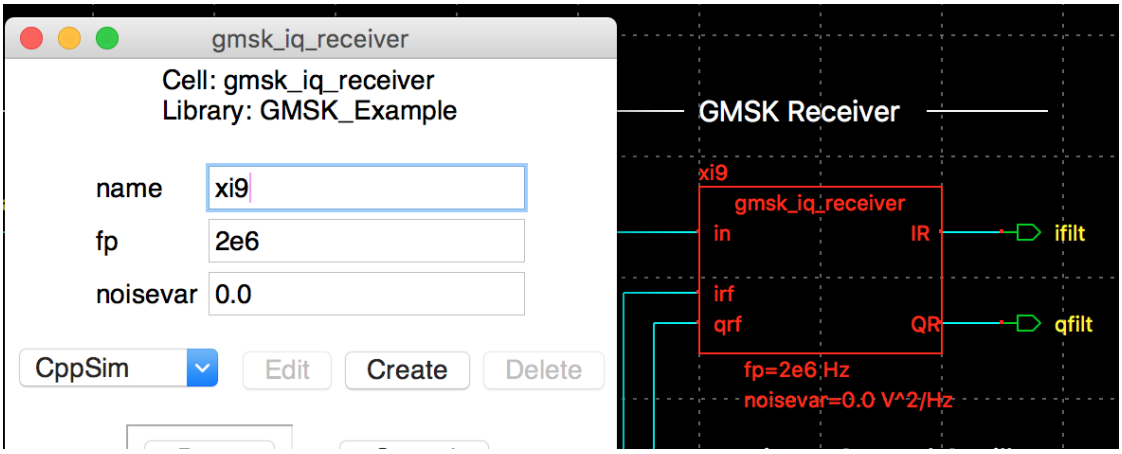

Figure 4.4 Receiver Modeling

The architecture of the receiver is as shown in Figure 4.5.

As can be seen from the model, the receiver architecture is that of a direct conversion receiver. This model, however, doesn't include DC offsets, impedance variations, matching, or the port to port isolations.

The N_R block adds the receiver noise model to the received spectrum to account for the noise from all the components together. This signal is then passed through a band pass filter to filter all the out of band interferences. The selected band is passed through an

LNA and is split to be sent to the mixers. Once down-converted, the channel select filter removes the up converted signal and other interferers. The baseband spectrum thus contains the modulated signal along with the modeled receiver and transmitter noise [40].

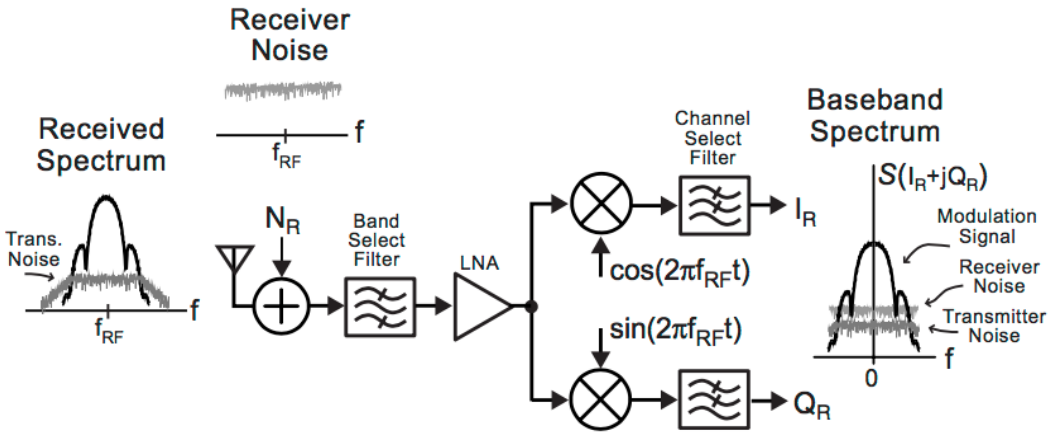

Figure 4.5 Receiver Architecture [40]

To evaluate the performance of the model, the eye diagrams for the transceiver was plotted.

To begin with, the eye diagram of the I/Q branches of an ideal transmitter was plotted, as shown in figure 4.6.

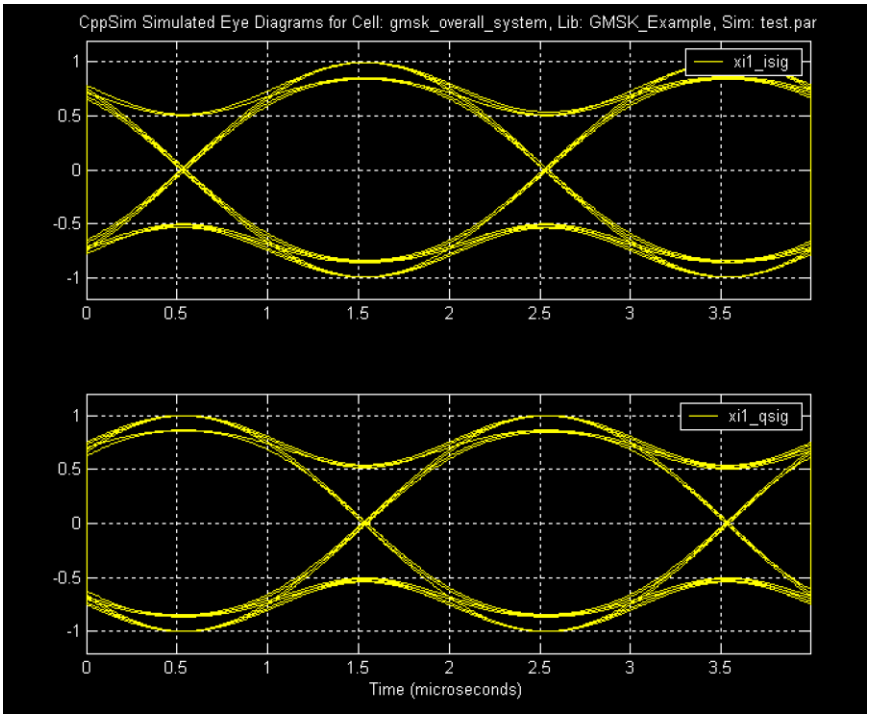

Figure 4.6 Eye Diagram of I/Q Branches of an Ideal Transmitter

Further, the eye diagram of an ideal receiver was simulated. Figure 4.7 shows the eye diagram of the I/Q branches of an ideal receiver.

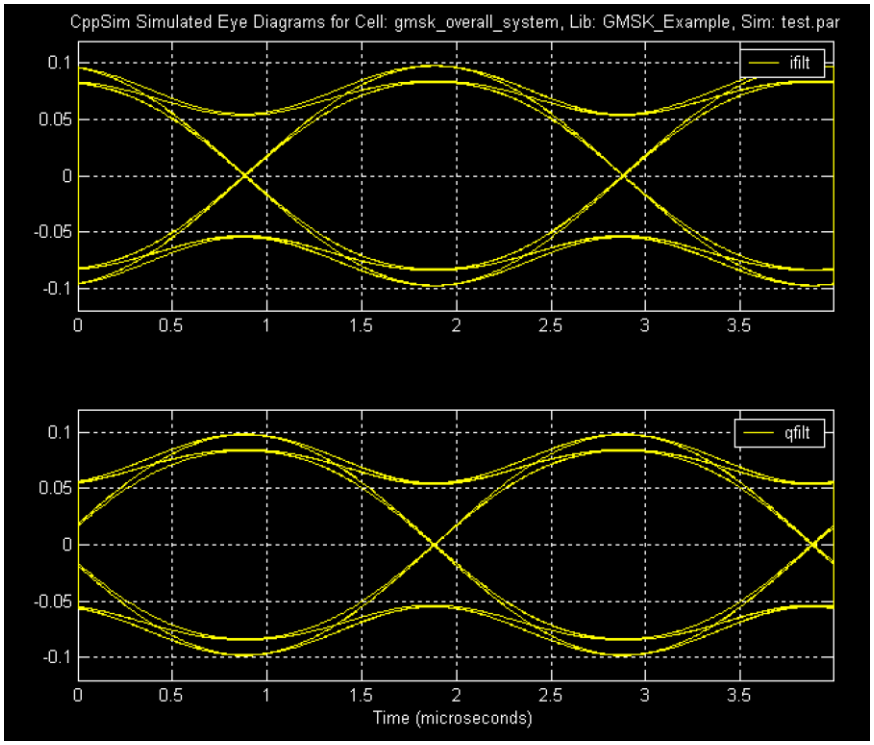

Figure 4.7 Eye Diagram of I/Q Branches of an Ideal Receiver

The performance of the system was evaluated for inter symbol interference and phase mismatch.

Figure 4.8 shows the receiver eye diagram due to a transmitter induced inter symbol interference.

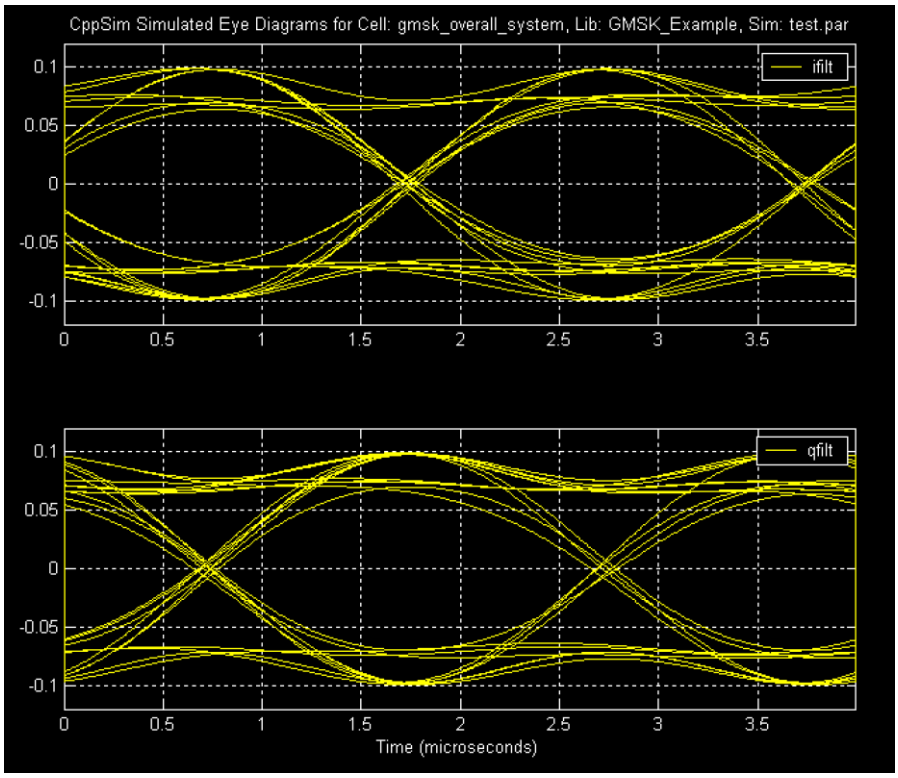

Figure 4.8 Eye Diagram for Transmitter Induced Inter Symbol Interference

To simulate this eye diagram, the PLL bandwidth was set to 250kHz. This means that the filter bandwidth of the PLL was changed. The PLL employs a second order lowpass filter with an asymptotic bandwidth. This means that the gain of the filter rolls off at a rate of 20 dB/decade at the 3dB bandwidth specified, which in this case is set as 250kHz [41].

On further examination of the inter symbol interference, it was noticed that improving the bandwidth of the PLL improves the performance of the transceiver for inter symbol interference. This behavior is completely in line with the expected eye diagrams.

Figure 4.9 shows the eye diagram of the receiver for a phase mismatch.

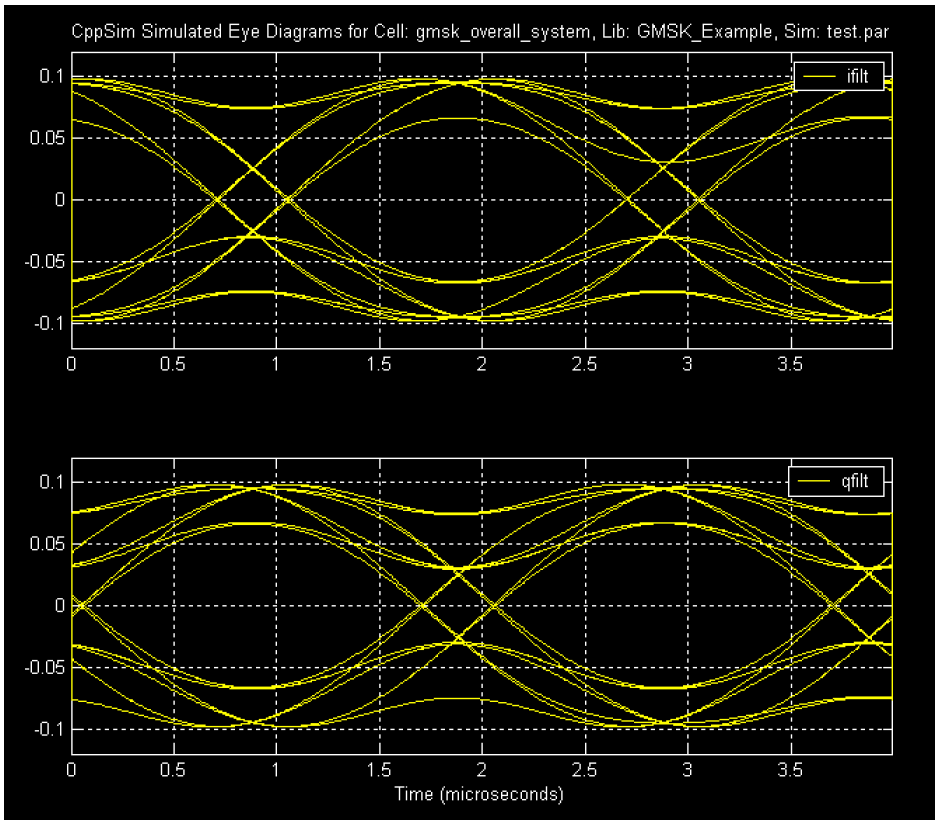

Figure 4.9 Eye Diagram for Receiver I/Q Phase Mismatch

As seen, a mismatch between the I and Q branches of the receiver also impacts the receiver performance. This plot was simulated for an offset of 290˚. The ideal value for the receiver being simulated is 305˚. As this value is varied, the performance goes down. On further analysis, the performance of the receiver becomes worse as the offset is farther away from the ideal value.

4.3 Simulator Evaluation:

As it has been discussed before, the modeling of the transmitter and receiver model only the noise of the components. The nonlinearities have not been modeled. The mixer

model, for example, has been shown in figure 4.10.

```
module: mixer
parameters:
inputs: double a double b
outputs: double y
static_variables:
classes:
init:
code:
y=a*b;
```

Figure 4.10 Mixer Modeling

As seen, the mixer has been modeled as an ideal multiplier. The noise of the mixer is considered while modeling the noise of the entire receiver and transmitter in the models. However, the nonlinearities, such as second order and third order intermodulation distortion have not been modeled. Along with this, the port to port isolation has also not been modeled. Although mathematical models for IIP2 and IIP3 are possible, it is quite complex to do so in Verilog. Also, the isolation can not be modelled behaviorally. This makes transfer of the mixer from Cadence, which is a circuit design tool, to CppSim not possible. Although this model works properly, the results obtained are very close to the ideal model and not close to the practical model.

On the other hand, this modeling is very useful as it can help prove that a particular architecture can work in a system. Thus, once the system is modeled behaviorally, it can prove the use of that model in the system. There will always be a degree of error between the performances of the behavioral model and the circuit design model, but the behavioral

model gives an insight if the hard work to be put in the circuit design is worth it. That in itself is an achievement, and CppSim shines in that regard.

Chapter 5: Mixer Simulation Results

5.1 Conversion Gain and Bandwidth of Operation:

The voltage conversion gain of a mixer is given by the following equation:

$$A_v = \left(\frac{2}{\pi}\right) * g_m * R_o$$

From the above equation, the voltage conversion gain depends on the output load resistance (PMOS load resistance) and the transconductance of the RF transistors. Therefore, voltage conversion gain is improved by optimizing the g_m of the RF transistors while at the same time improving the R_o of the PMOS load. The length of the transistors is kept constant as the variation in the length can cause a variation in the loading of the transistors at various frequencies. To improve the gain, optimum LO input swing is also desirable. A suitable swing is chosen for the LO to achieve high gain while not compromising on the linearity performance of the mixer, as there is a trade-off between the gain and the linearity of the mixer. At the same time, care is taken that the sizing of the RF transistors is not increased in such a manner that the current consumption exceeds 4 mA. The PSS and the Periodic Transfer Function (PXF) analysis are utilized to simulate the voltage conversion gain of the mixer. The PXF analysis is implemented by sweeping the frequency in the range of 1 Hz to 100 MHz for low band, mid band and

high band. On an average, the gain is greater than 11 dB for all three bands and is constant throughout the band of interest. Figure 5.1 depicts the conversion gain plot vs the IF frequency, while Figure 5.1.2 depicts the conversion gain as a function of the IF frequency.

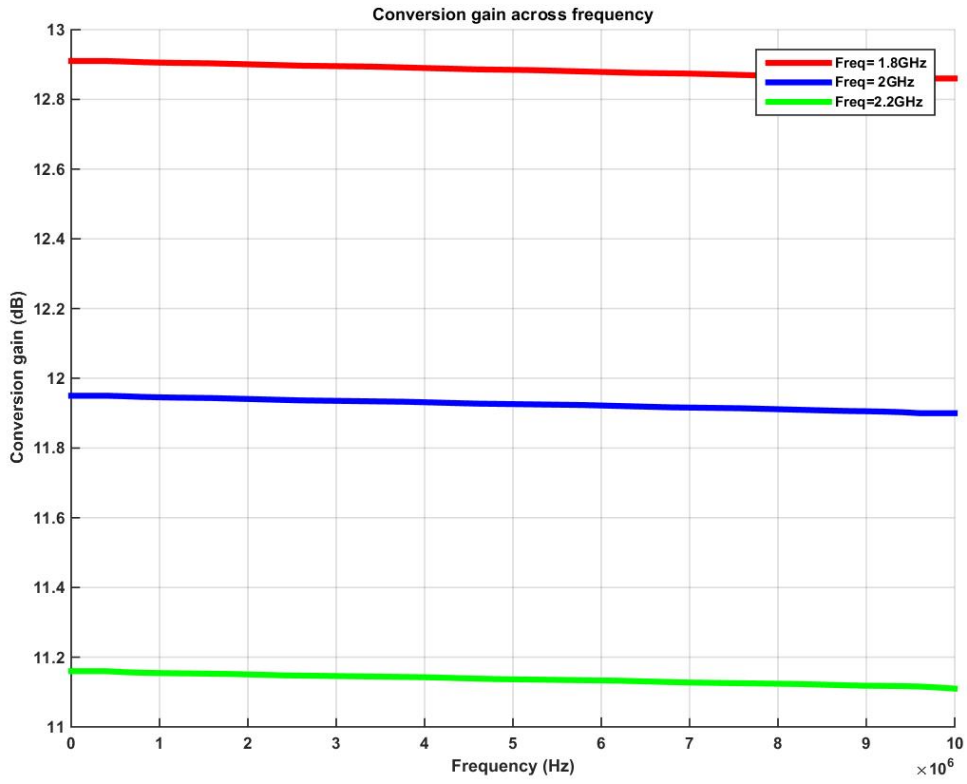

Figure 5.1 Conversion Gain vs IF Frequency

5.2 Isolation:

The amount of power coupled from one port to the other in a mixer is measured as the isolation between the two ports. The important isolations to be taken into consideration

are the LO-to-IF isolation, the LO-to-RF isolation and the RF-to-IF isolation. The LO-to-IF isolation, also known as the LO feed through, is a measure of the signal coupled from the LO port to the IF port, the LO-to-RF isolation is the measure of the signal coupled from the LO port to the RF port and the RF-to-IF isolation is the same measure from the RF port to the IF port. For good performance in terms of the sensitivity of the mixer, these parameters should be as low as possible to avoid any coupling between two ports. This coupling could be due to wanted or unwanted capacitances between any two ports and can be improved by implementing filters. The LC tank filter implemented with the switching pair is one such example. The advantage of the LC tank filter is two fold- it filters out the LO-to-RF port while at the same filtering the second order harmonics to improve the IIP2 of the circuit. The interactions of the RF port is the most difficult to suppress due to the wide separation between the RF and the IF frequencies. The LO-to-RF isolation usually results in a leakage into the antenna if the mixer is used as the first down converter in the wireless receiver.

Figures 5.2, 5.3 and 5.4 depict the three isolations in the proposed mixer.

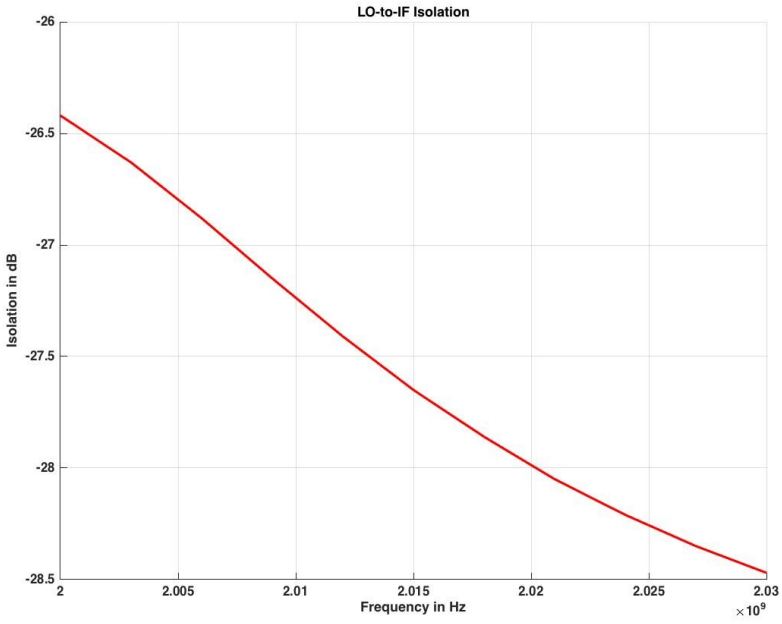

Figure 5.2 LO-to-IF Isolation

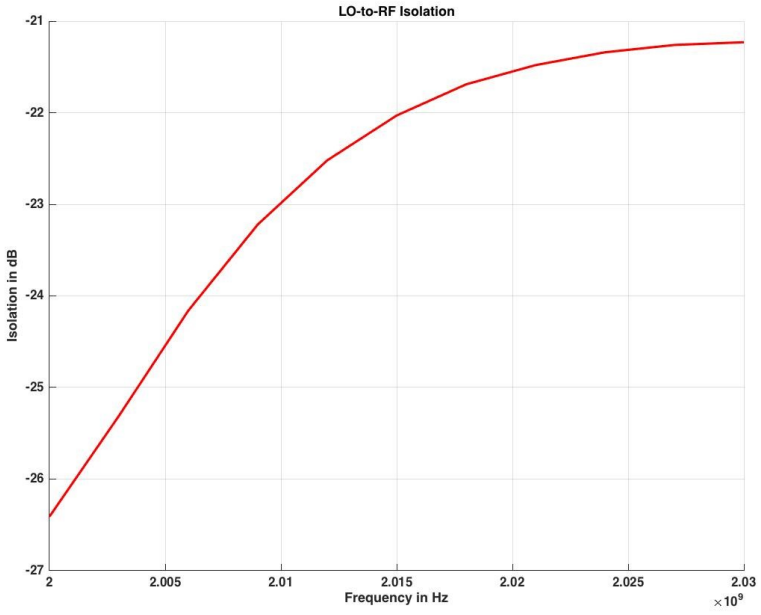

Figure 5.3 LO-to-RF Isolation

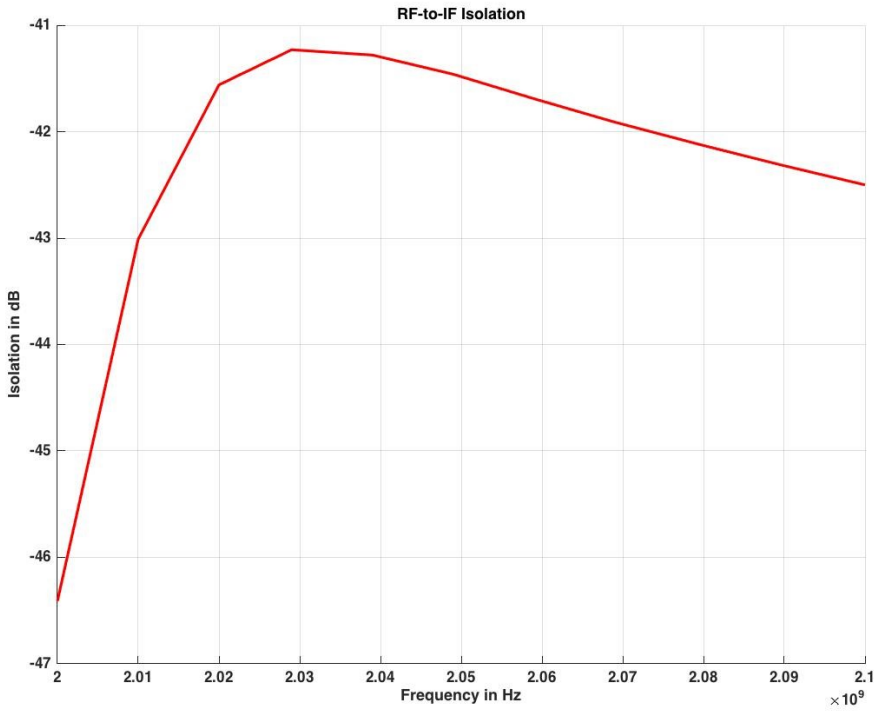

Figure 5.4 RF-to-IF Isolation

From the three figures, it can be seen that the isolation of the proposed circuit is at acceptable levels.

5.3 Noise Simulation:

The noise at the output of the mixer dominates at higher frequencies and degrades the linearity of the mixer. Improving the noise performance of the mixer leads to better linearity. The switching transistors produce the majority of the noise in the circuit. The major noise contributed by the switching pair is the drain thermal noise. This noise can be suppressed by implementing low g_m LO switching pair, as the drain thermal noise is

dependent on the transconductance of a given transistor. Several filters have been incorporated in the design to optimize the noise performance. The LC tank filters out the noise due to the switching pair and the RF transistors, C_{TC} filters out the noise due to the transconductance transistors and the C_L filters out the noise due to the PMOS load. Due to these efforts, the noise at the output of the mixer is around the 10 dB mark, which is remarkable, given the other specs of the design.

Using the PSS and Pnoise analyses, the SSB and the DSB noise can be obtained. Usually, DSB noise performance is better than the SSB by a few dB's, due to which the choice of noise simulation is SSB. Figure 5.5 shows the SSB noise performance of the mixer.

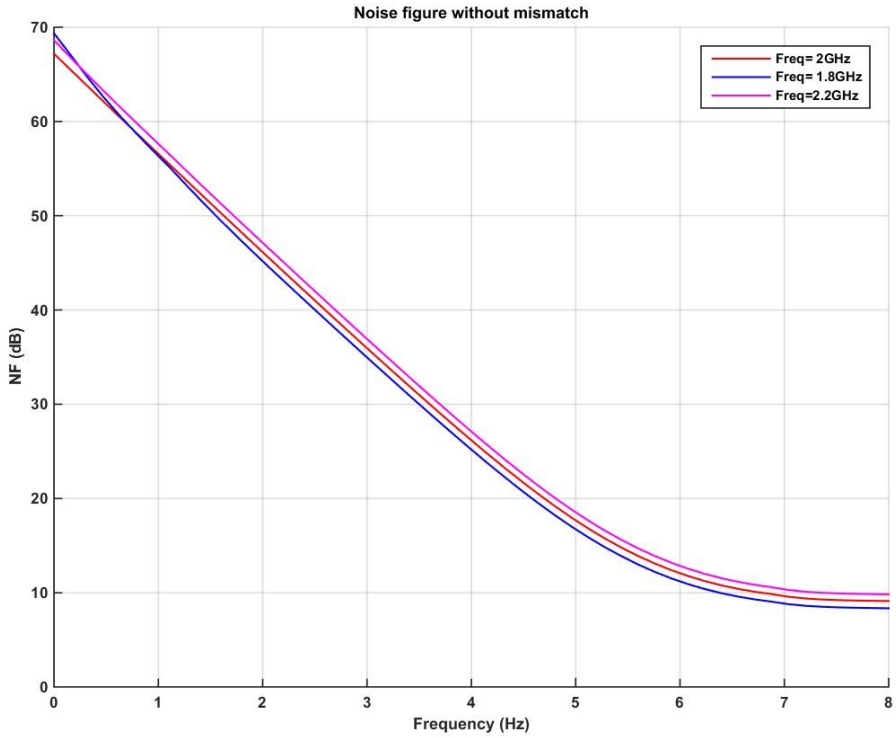

Figure 5.5 Noise Performance of the Mixer

5.4 Linearity Simulations:

5.4.1 IIP3:

The 3rd order inter-modulations are observed a few MHz away from the original signal. Added to this, the third order harmonic rises at a slope of 3 dB/decade, which is three times the slope of the output signal. Due to these facts, IIP3 is a very important simulation parameter. In the proposed design, a CCPD is implemented to improve the IIP3 performance of the mixer.

A well designed CCPD cancels the third harmonics caused by the RF transistor due to the presence of a blocker right next to the desired signal. The g_{m2} of the RF transistors is the main cause of the third order harmonics. Theoretically, cancellation of this contributor should result in an infinite IIP3. Practically, however, it can be cancelled only to an extent. The role of the CCPD is to generate a g_{m2} of the same magnitude as the RF stage, but with opposite sign. This can be achieved by optimum sizing and operation in the triode region of the transistor.

The effect of the CCPD is shown in the following sections.

5.4.1.1 Without CCPD:

The first simulation is done without the CCPD connection. As seen in Figure 5.6, the IIP3 at 2 GHz is close to -4 dBm. This means that the mixer is highly susceptible to an external blocker.

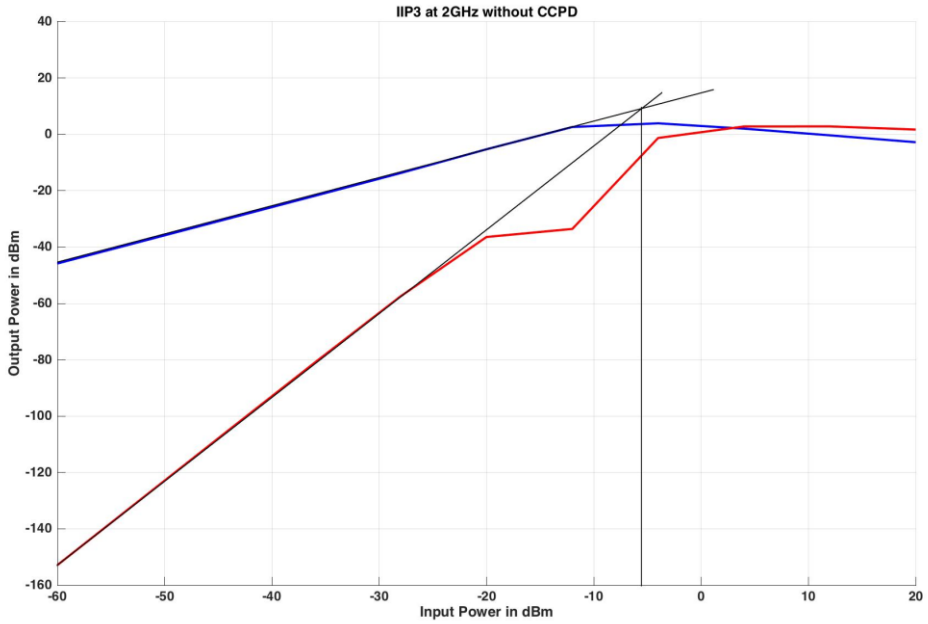

Figure 5.6 IIP3 at 2 GHz without CCPD

The other values have been tabulated below:

Frequency	IIP3
1.8 GHz	-5 dBm
2.2 GHz	-5 dBm

Table 1: IIP3 without CCPD

5.4.1.2 With CCPD:

The second simulation is done after connecting the CCPD. As seen in Figure 5.7, the IIP3 at 2 GHz is around 16.7 dBm, which is an improvement of almost 20dB. Since the CCPD

was designed at 2 GHz, a similar but not so dramatic improvement is observed in the high and low bands as well.

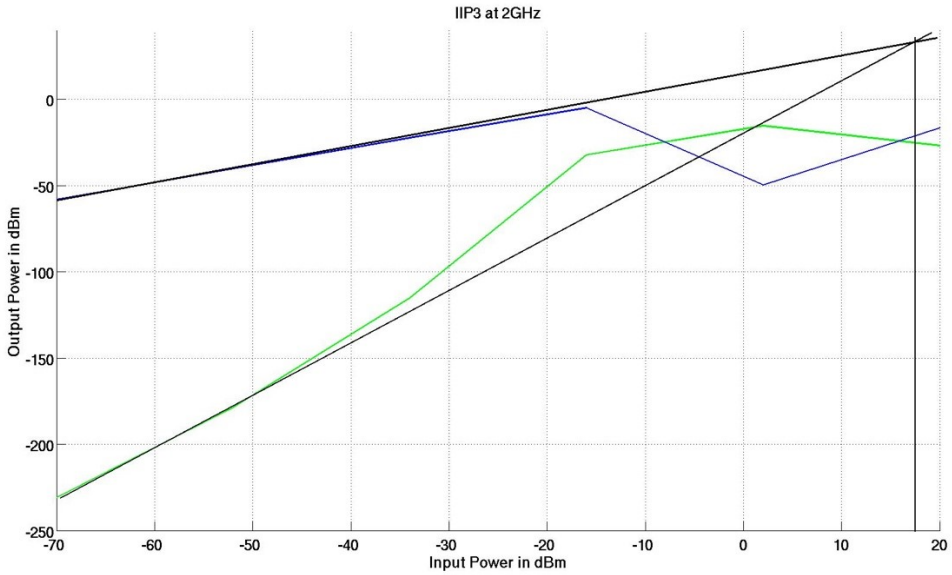

Figure 5.7 IIP3 at 2 GHz with CCPD

The IIP3 values at 1.8 and 2.2 GHz have been tabulated below:

Frequency	IIP3
1.8 GHz	11 dBm
2.2 GHz	12 dBm

Table 2: IIP3 with CCPD

5.4.2 IIP2:

IIP2 is another linearity issue in the mixer. This issue rises when there is a mismatch between the two branches of the mixer. When the mismatch is not present, the IIP2 is generally very high, sometimes even greater than 100 dBm if the right filter is designed. In the proposed mixer design, the LC tank filter at the switching pair is designed to address this issue. The idea is to filter out the fundamental LO frequency, together with the sidebands. This leads to an improvement in the IIP2 performance, thus leading to an IIP2 of 127 dBm under 0 mismatch.

The inductor, L_{SW} is chosen to resonate with the capacitor C_{PAR} at the LO frequency. The IM2 current, therefore, is reduced by a factor Q when down-converted, where Q is the quality factor of this tank. The input-output current relation is thus more linear. Along with the IIP2, the LC filter improves the 1/f noise performance also.

The following sections describe the IIP2 under mismatch without the digital enhancement and under mismatch with the digital improvement incorporated.

5.4.2.1 IIP2 Under Mismatch:

The effect of the LC tank is more pronounced under mismatch. The IM2 currents are usually very high at the down-converted output under mismatch conditions. Due to a high Q filter designed at LO frequency, this current goes down by the same factor, thus giving a better performance. However, the performance still isn't as good as expected. Figure 5.8 shows that at 2 GHz, the IIP2 is 42 dBm, which is quite low. However, the digital improvement helps with this and makes the IIP2 better, as shall be seen in the next section.

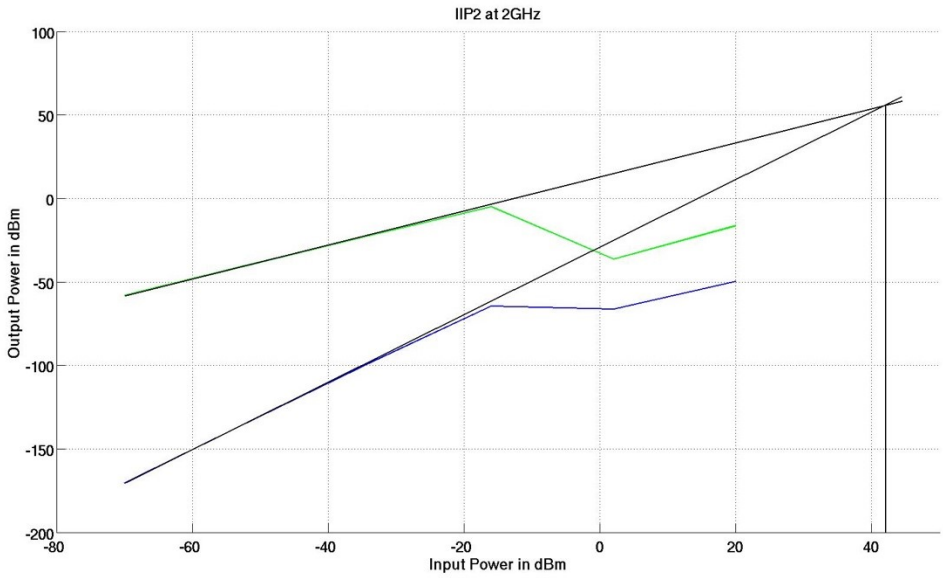

Figure 5.8 IIP2 at 2 GHz under 10mV mismatch

The values of IIP2 under 10 mV mismatch at low and high band have been tabulated as follows:

Frequency	IIP2
1.8 GHz	40 dBm
2.2 GHz	41 dBm

Table 3: IIP2 under 10 mV mismatch

5.4.2.2 IIP2 Under Mismatch with Digital Enhancement:

The final improvement made in the IIP2 of the mixer is by the digital enhancement. When a mismatch occurs, the comparator output goes high, thus enabling the up-counter.

This up counter enables the NMOS loads for the PMOS current mirror attached to the PMOS loads. This leads to variation in the bias voltage of the PMOS loads, thus reducing the mismatch. Once the mismatch reaches the desired level, the comparator output goes low, the hold bit to the up counter goes high and the current state is held. This leads to a significant improvement in the IIP2 of the mixer. Figure 5.9 shows the IIP2 of the mixer under 10mV mismatch at 2 GHz to show the improvement as compared to the previous section. Figure 5.10 shows the comparison between the IIP2 performance under mismatch with and without the digital enhancement at 2 GHz. As seen, the minimum improvement is around 14 dB and it goes up to north of 20dB. Similar performance can be seen at 1.8 and 2.2 GHz bands also.

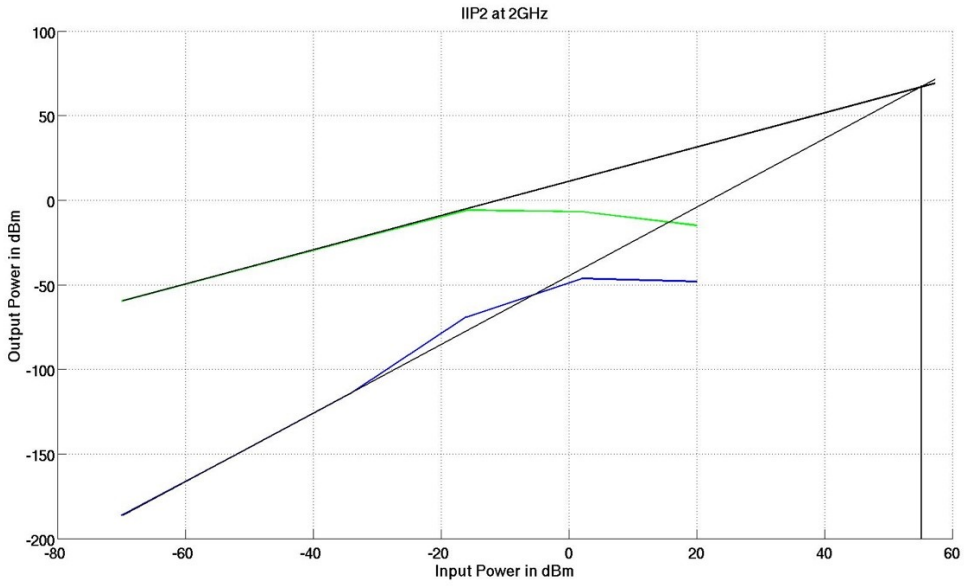

Figure 5.9 IIP2 under mismatch with digital enhancement at 2 GHz

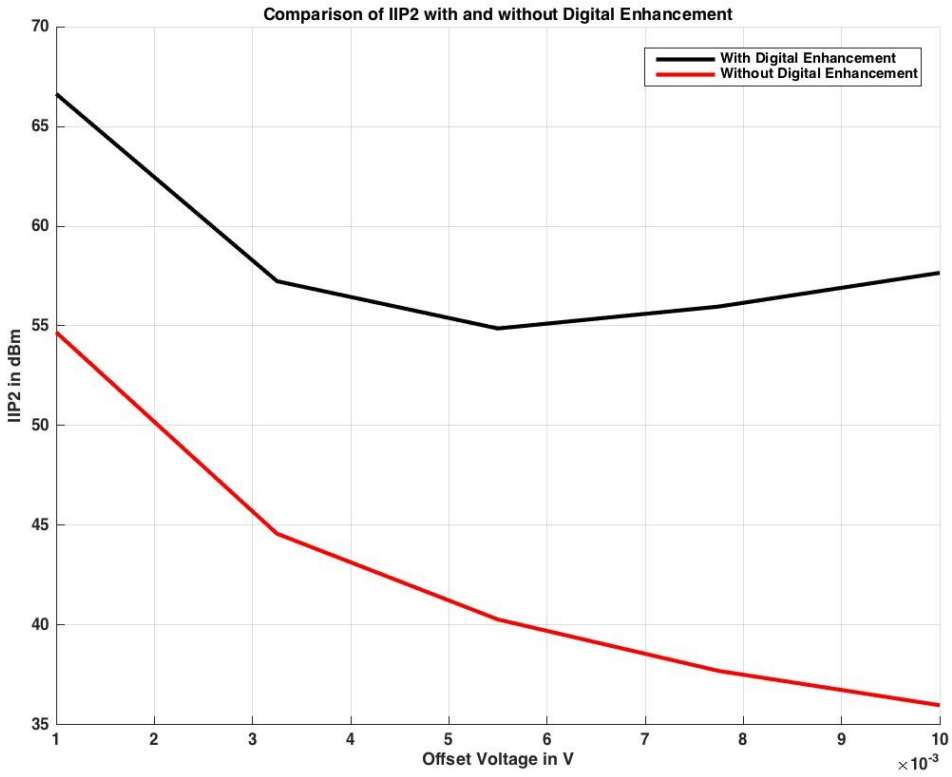

Figure 5.10 Comparison of IIP2 under mismatch with and without Digital Enhancement

5.5 P1-dB:

P1-dB of the mixer is another measure of linearity as already discussed. The higher the P1-dB, the more linear the mixer is. Figure 5.11 shows the P1-dB for the proposed mixer. This measurement was done by sweeping the input RF power in the QPSS analysis and measuring the output compression point. As seen, the P1-dB of the proposed mixer is around -14dBm.

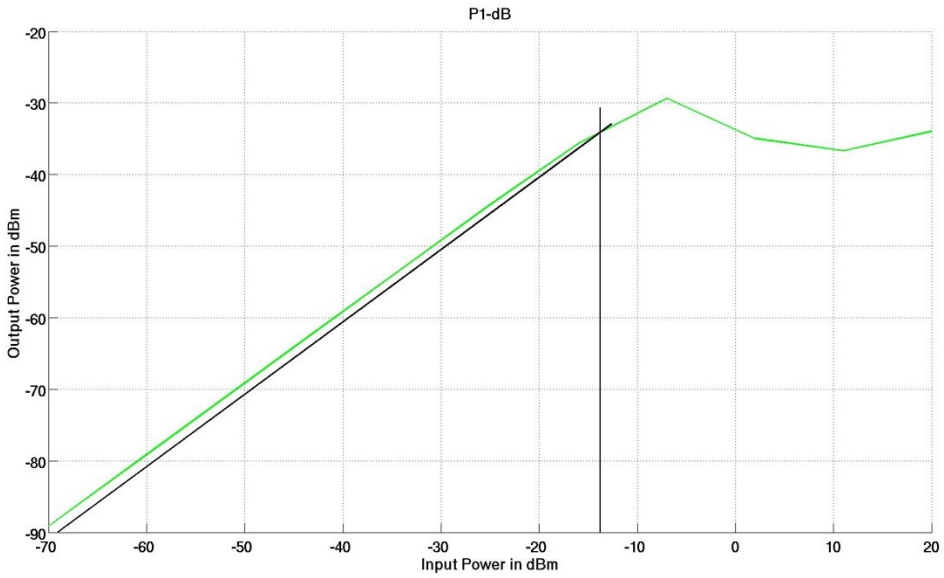

Figure 5.11 P1-dB

5.6 Bandgap Temperature Stability:

Figure 5.12 shows the circuit of the Bandgap current reference. The function of the Bandgap circuit is to provide a stable current across variation in temperature and also maintain acceptable levels of current at the corners. This means that under different temperatures, the current through the circuit remains the same.

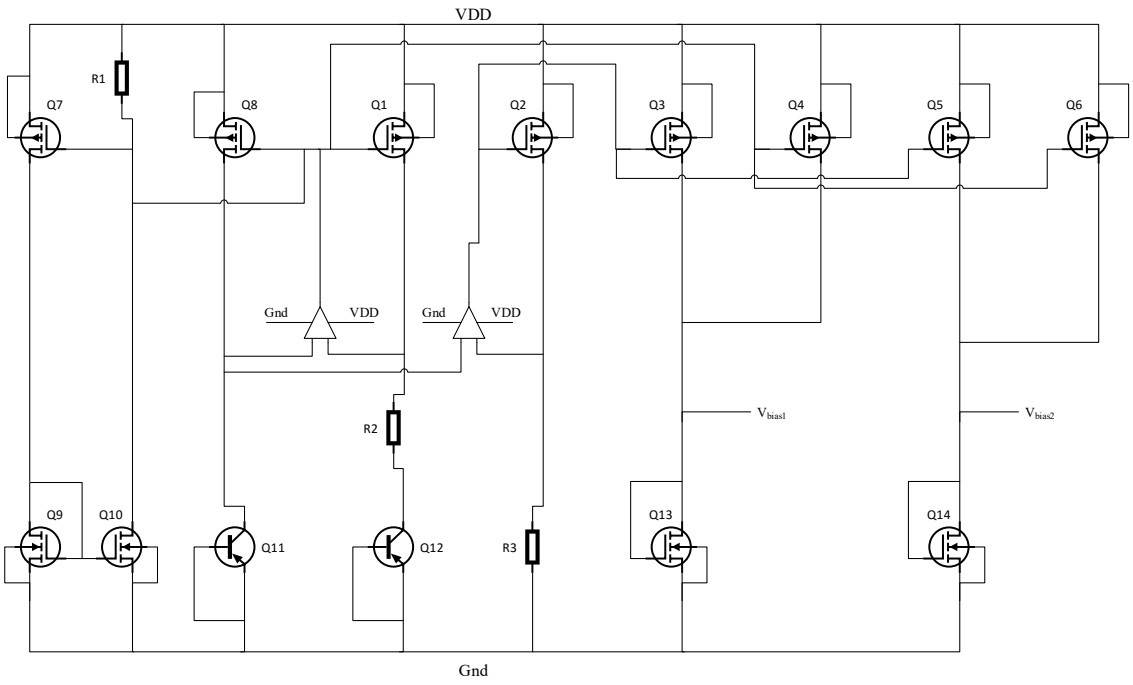

Figure 5.12 Bandgap Current Reference Circuit

For the designed Bandgap, a folded cascode amplifier was designed with a phase margin of 66˚ at 256mV. The input offset of the amplifier is 3mV. As seen from Figure 5.13, the variation in the current across temperature is in the order of a few Nano-Amperes. This translates to a less than 5µA variation in the current in the mixer circuit. With the variation in the supply voltage, the current varies by a few µA, which results in a significant improvement in the performance of the mixer at corners. The effect of adding the Bandgap is evident while simulating the process corners. The current variation is minimal, which otherwise would have been of the order of a few hundred micro amperes.

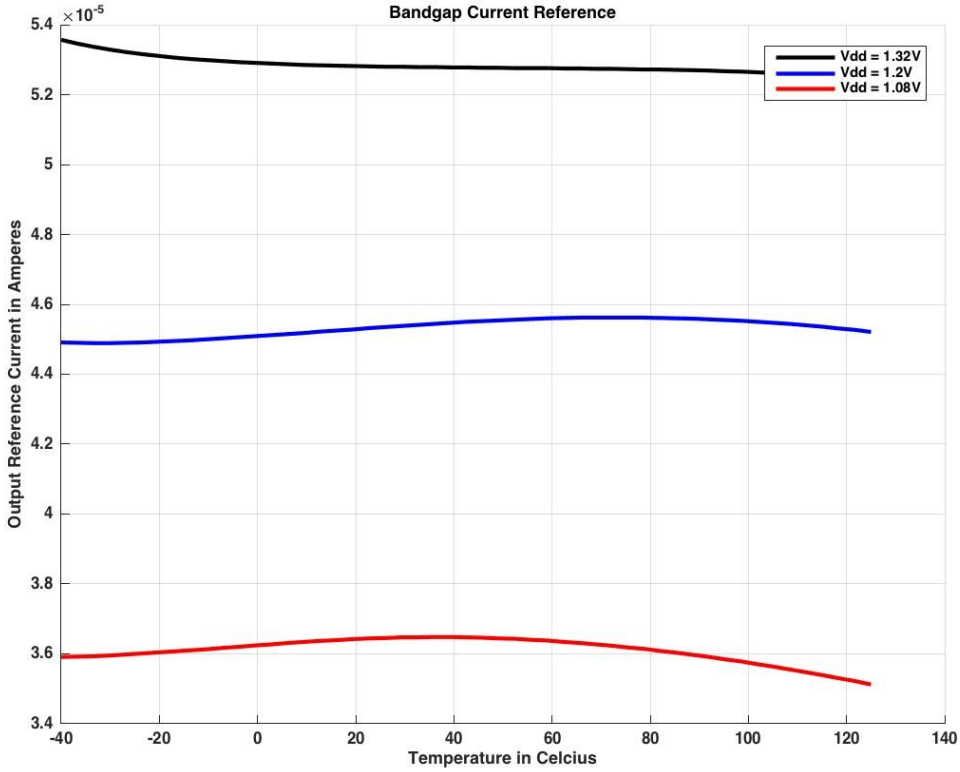

Figure 5.13 Variation in Current Across Temperature at Different Supply Voltages

5.7 Inductor Quality Factor and Self Resonant Frequency:

Inductor quality factor and self resonant frequency are two very important factors contributing to a good filter design. Higher the Q at the given frequency, better the filter, and better the noise cancellation and IM2 current reduction. The inductor is designed to have a SRF off at least 2X the operation frequency, to have a consistent filter performance throughout the band. Figures 5.14 and 5.15 show the Q and the SRF of the inductor designed in the proposed mixer. As seen from the figures, the quality factor of

the inductor at 2 GHz is around 9.5 and the self resonant frequency of the inductor is around 4.2 GHz. This ensures good performance throughout our band of interest.

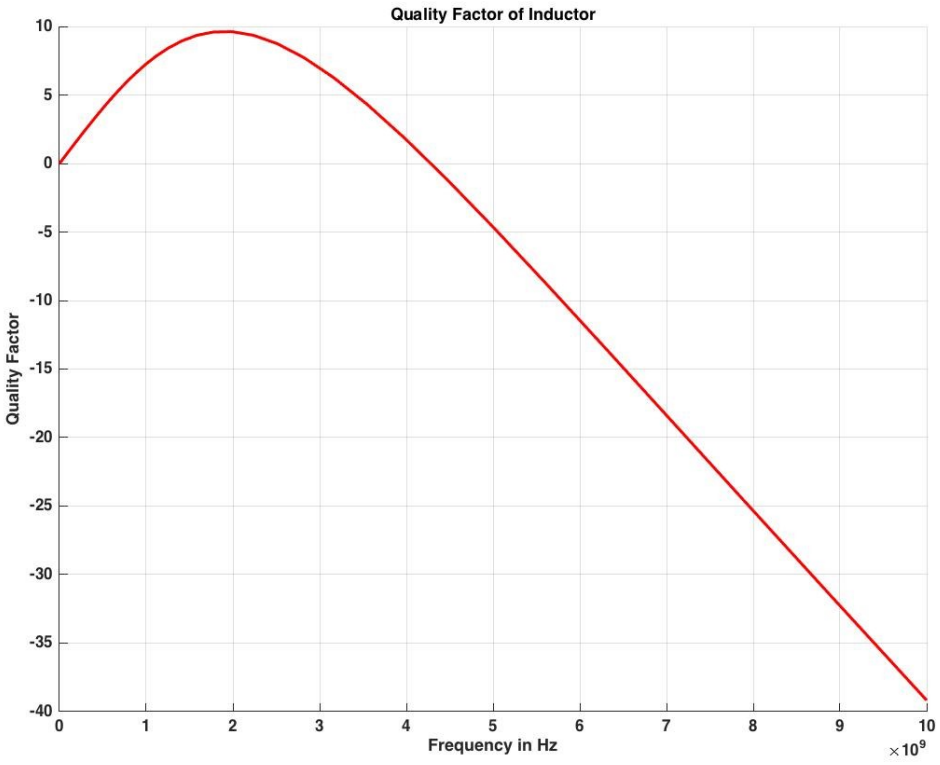

Figure 5.14 Inductor *Q* Factor

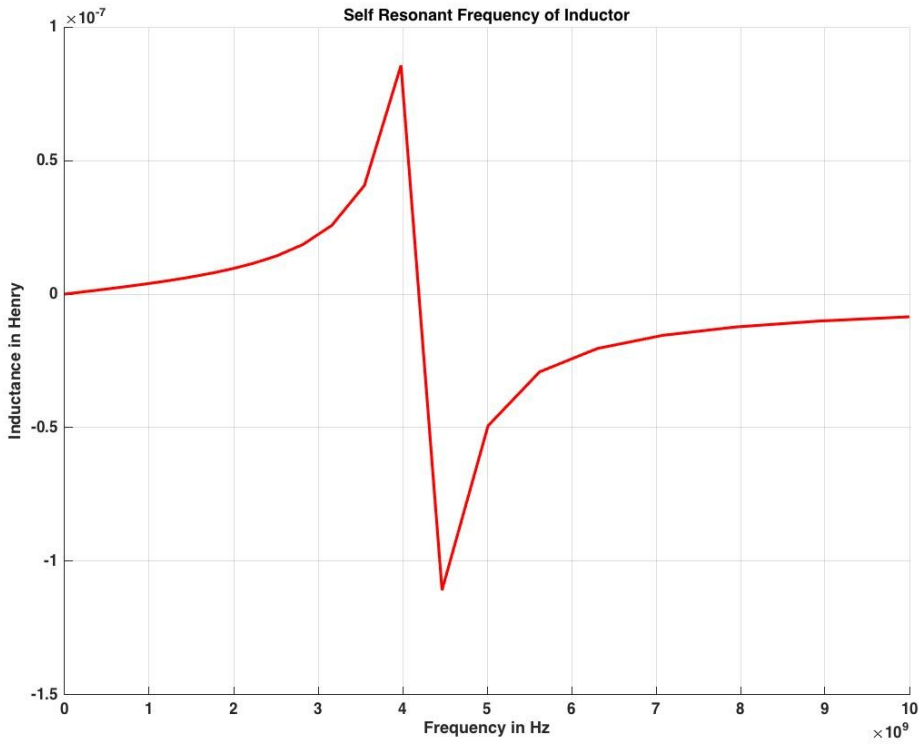

Figure 5.15 Inductor Self Resonant Frequency

5.8 Overall Specifications:

Table 4 tabulates the overall specs achieved in this design. Columns 2 and 3 show the typical and the achieved specs respectively.

As it can be seen from the table above, there is a significant improvement in the conversion gain compared to the typical specifications. This improvement leads to a drop in the linearity, which is evident from the P-1dB.Thus, there is a significant difference between the typical P-1dB and the P-1dB of the proposed design. To compensate the loss in linearity, the CCPD was designed along with the fully differential transconductance stage. That is evident from the IIP3 values of the two columns. Keeping a lower

conversion gain could have led to a further increase in the linearity of the circuit. Also, due to the various steps taken to reduce noise figure and improve IIP2, it can be noticed that the noise figure is still under acceptable limits and the IIP2 is much better than the typical specifications. The circuit is also properly balanced which can be seen from the three isolation factors.

PARAMETER	TYPICAL SPECIFICATIONS	ACHIEVED SPECIFICATIONS	COMPARISON
Conversion Gain	5 to 7 dB	11 to 13 dB	Improved
LO-RF Isolation	-20 to -30 dB	-21 to -26 dB	Nominal
LO-IF Isolation	-20 to -30 dB	-26 to -29 dB	Nominal
RF-IF Isolation	-20 to -30 dB	-41 to -46 dB	Nominal
P-1dB	-5 dBm	-14 dBm	Deteriorated
IIP2 without mismatch	120 dBm	125 to 127 dBm	Improved
IIP2 under mismatch	40 dBm	55 to 68 dBm	Improved
IIP3	5 dBm	11 to 17 dBm	Improved
Noise Figure	8-12 dB	11 dB	Nominal

Table 4: Overall Specifications Achieved

Chapter 6: Conclusion and Recommendations

6.1 Conclusion:

The proposed mixer was implemented with various enhancements to boost the overall performance for certain parameters, such as conversion gain, IIP3 and IIP2 of the circuit. The motivation of the research was obtained from the moving trend of the industry to implement more digital control over circuits. Simulations show that this design has the potential to be taken forward to fine tune and achieve more stability and better results. The trade offs can be taken into consideration to boost one or the other facet of the mixer, according to the specific requirements.

The design implements the concepts of a CCPD to enhance the IIP3 of the system. A PMOS load is implemented to improve the load resistance and reduce the noise figure. A fully differential transconductor stage is implemented to improve the second and third order intermodulation distortions. Low pass filters and LC filters have been implemented to further improve the performance of the mixer. A digital enhancement has been implemented to detect a voltage mismatch in the system and automatically vary the Q-point of the PMOS loads to compensate for the mismatch in the system and boost the second order intermodulation distortion performance of the system.

A behavioral modeling tool, CppSim was evaluated. Verilog models were used to characterize the components of the system. A GMSK transceiver model was used to evaluate the tool. It was concluded that the model can not take into consideration the nonlinearities and the isolation of the mixer and thus cannot be relied on to give accurate results. It was also concluded that the mixer cannot be transferred from Cadence to CppSim. On the other hand, it was also concluded that CppSim gives an option to evaluate the potential use of an architecture in a system. This was particularly useful when it came to determining if any proposed architecture can be used in a system.

6.2 Recommendations:

The mixer performance can be fine tuned further to improve the stability of the system. Also, fine tuning can be done to try and save more area by trying to optimize the design further. The digital optimization only takes into account the voltage mismatch. Mismatches due to temperature variation can be taken into account in an innovative design. More performance enhancement techniques can be explored to further improve the performance of the circuit while saving area.

Based on the evaluation of CppSim, the tool does not include nonlinearities of the components. To account for the nonlinearities, separate models have to be made in Verilog. This modeling has to be done manually and is a bit complex due to the different number of equations and constraints in modeling nonlinearities.

Since CppSim was not an ideal tool to transfer the mixer design from Cadence, more tools can be explored to use a tool that is more inclined towards IC design than

behavioral modeling. This will allow perfect transfer of the design specifications from Cadence to the design tool and can ensure easy transition from one design node to another while accurately modeling what changes are to be made.

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APPENDIX

A.1 Cadence Simulations:

Measurement	Analysis
Conversion Gain	PSS and PXF
Isolation	PSS, PAC and PXF
Noise Figure	PSS and PNoise
IIP3	QPSS and QPAC
IIP2	QPSS and QPAC
P1-dB	QPSS
Digital Logic Waveforms	Transient Analysis
Bandgap Current Curves	DC Analysis

Table 5: Cadence Simulations

A.2 CppSim Simulations:

Analysis	Modifications To The Model
Inter Symbol Interference	Modify filter bandwidth
Phase Mismatch	Modify VCO phase offset
Noise	Add Noise value in the noise block

Table 6: CppSim Simulations