Comparison of Interface State Spectroscopy Techniques by Characterizing Dielectric – InGaAs Interfaces

THESIS

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By

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ABSTRACT

Highly scaled III-V compound semiconductors, particularly n-$In_{0,53}Ga_{0,47}As$ in conjunction with a suitable high-κ dielectric, has been regarded as a promising channel material for high performance metal-oxide-semiconductor field effect transistors (MOSFETs). The high intrinsic electron mobility and small band gap of n-$In_{0,53}Ga_{0,47}As$ offers the possibility of developing MOSFETs with higher drive currents at low operation voltages. However, the high density of interface states (D_{it}) at the high-κ/n-$In_{0,53}Ga_{0,47}As$ interface degrades the device performance. Therefore, accurate and quantitative characterization of the interface states is an important issue in the continued development of high quality interfaces to track changes induced by processing and growth optimization. This work demonstrates that high D_{it} concentrations from high-κ/semiconductor interfaces can be accurately characterized using constant capacitance deep level transient spectroscopy and low temperature C-V (LTCV) method. This is compared with the conductance method, which underestimates D_{it} magnitude and shows energy dependent distribution.

DEDICATION

Dedicated to my parents

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CHAPTER 1: INTRODUCTION

1.1 Motivation for Studying Interfaces of High-κ Dielectrics/III-V Semiconductors

Silicon metal-oxide-semiconductor field-effect transistors (MOSFETs) are the principal building block of the today's integrated circuit technology. The continuous downscaling in key feature dimensions (e.g. gate length, gate oxide thickness) of MOSFET boosted its switching speed and reduced the operation voltages over time [1,2]. Figure 1.1 presents the schematic of a MOSFET with key components labeled. In addition to improved logic characteristics, the density of MOSFETs per area increased accordingly with further downscaling which allowed accommodating extra analog, RF, and system-on-chip (SoC) features while the total size of a chip sustained in the required limits [1]. However, the scaling reached to a point where the power density that needs to be dissipated becomes significant as a result of increased density of MOSFETs. The absence of cost-effective cooling systems prevents the use of such chips feasible for many applications. The operating voltage which bottomed out around 1V for a while must be even further reduced to overcome the power constrained scaling limit. This cannot be achieved without degrading the switching properties of silicon MOSFETs [1,3,4] . Therefore, non-traditional channel materials with higher carrier mobility; such as

III-V or Ge, need to be implemented to acquire sufficient drive currents at lower operating voltages [5].

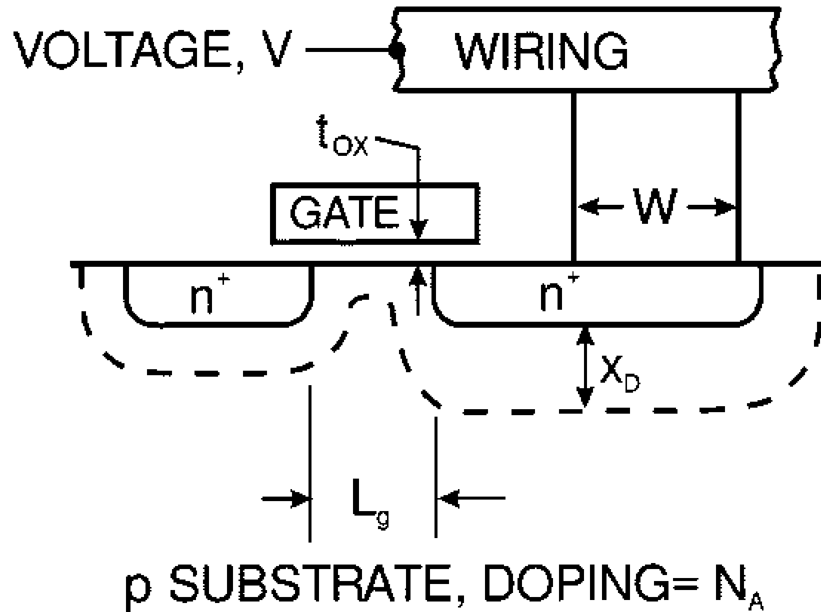


Figure 1.1: Schematic illustration of a Si MOSFET. The key components of MOSFET that affects its performance labeled [2]

The III-V compound semiconductors such as GaAs, InGaAs, InAs, have superior electron mobility compared to silicon and have been considered as channel materials that can improve switching speed while lowering down the operating power. However, the integration of high transport channel materials on a silicon platform to realize reliable highly scaled MOSFETs is challenging due to many factors, among which one of the most important is the fact that these materials lack a very high electronic quality native oxide [6]. The most important reason behind the success of silicon is to have a native

insulator, SiO_2, which meets the requirements of reliable device operation. SiO_2 forms an interface with low concentration of interface states (~10^9 cm^2eV^{-1} [7]) with high electrical and thermal stability. Unlike the Si/SiO_2 material system which have robust interface, native oxides of III-V compound semiconductors are not sufficient for reliable device operation. High-κ dielectrics such as Al_2O_3, HfO_2, ZrO_2, and La_2O_3 deposited by atomic layer deposition (ALD) have proven to be promising candidates for highly scaled III-V MOSFET applications [8,9,10,11]. However, the interface state density (Dit) is still significantly higher (and not well characterized) compared to dominant Si/SiO_2 material system and this has detrimental effects on device operation such as, insufficient Fermi level response, lower carrier mobility due to scattering process in the channel, large sub-threshold swing voltage, and surface generation – recombination leakage current in MOSFETs.

In this respect, accurate and quantitative characterization of the interface states is an important issue in the continued development of high quality high-κ/III-V compound semiconductor interfaces to track changes induced by processing and growth optimization. In the early stages of CMOS progression, characterization techniques such as the Berglund method, the Terman method, the Castagne – Vapaille method and conductance method were developed to assess the quality of Si/SiO_2 interface [12,13,14,15]. These techniques have been applied to high-κ/III-V interfaces, but the reported interface state concentrations and their energy distribution throughout the band gap were quite different despite the admittance behaviors being analogous. Because these techniques did not develop with due consideration of the complex nature of high-κ/III-V

interfaces, several assumptions that are valid for Si/SiO_2 interface may not be so for III-V systems, and this may introduce very large errors in the extraction of Dit, particularly for large Dit values; a fact which is being explored by other research groups as well [16,17,18].

This work focuses on developing and applying more accurate and appropriate methods to measure and quantify interface states of concentrations substantially larger than that seen for SiO_2/Si, and hence more appropriate for III-V devices. In particular, the research effort explores the development and application of constant capacitance deep level transient spectroscopy (CC-DLTS) and low-temperature capacitance-voltage (LT-CV) methods to characterize dielectric/InGaAs interefaces. Comparisons with the commonly used conductance method are made in order to baseline and calibrate the findings, so that Dit spectrum comparisons can be made by these techniques.

1.2 Review of Atomic Layer Deposition (ALD) of High-κ Dielectrics on III-V Semiconductors

Native oxides of III-V semiconductors were shown to be not stable and leaky with low breakdown strength compared with SiO_2/Si. Indeed, the exposure of III-V surface to oxygen leads to the formation of native oxides As_2O_3 and As_2O_5, elemental As, As-As dimers, Ga dangling bonds that results Fermi-level pinning [19]. Along with inadvertent impurity incorporation (e.g. carbon) these are thought to be among the sources of high concentration of interface states distributed within the bandgap and as a result hinder effective Fermi level modulation which is undesirable for proper MOSFET operation.

The first high-κ dielectric/III-V interface with an unpinned Fermi level was achieved by in-situ deposition of Ga_2O_3 dielectric layer on molecular beam epitaxy (MBE) grown (100) GaAs and Dit was measured on fabricated p-type and n-type metal-oxide-semiconductor capacitors (MOSCaps) [20]. This study was a milestone which proved that minimizing the formation of native sub-oxides is the key to achieve high quality interface for dielectric/III-V structures. Depletion mode and enhancement mode GaAs MOSFETs were demonstrated by using the same dielectric deposition approach [21,22]. However, demonstration of the first GaAs MOSFET with an Al_2O_3 dielectric layer deposited by the atomic layer deposition (ALD) technique was the actual breakthrough [23]. The advent of atomic layer deposition (ALD) technique was a major leap towards realizing III-V MOSFETs and resulted successful device demonstration on other III-V compounds, such as InGaAs[24,25,26,27].

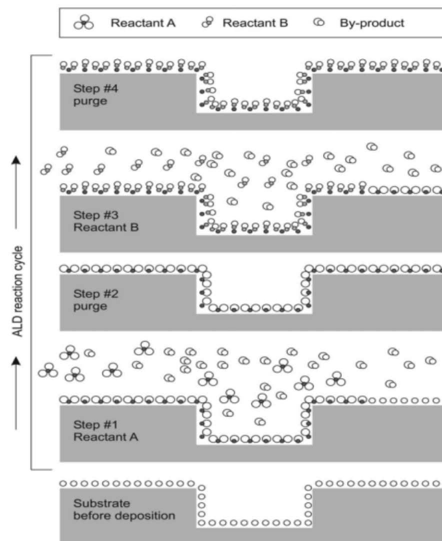


Figure 1.2: Illustration of a single ALD cycle that indicates self-terminating reaction steps and subsequent purging steps [28]

ALD is an ex-situ technique that allows depositing conformal layers of inorganic materials with thicknesses on the order of nanometers. The deposition process consists of self-terminating chemical reactions between precursors and the semiconductor to be coated with dielectric [28,29]. Figure 1.2 illustrates the single cycle of ALD process where the single layer of an inorganic material is deposited after subsequent self-terminating reactions. Even though ALD is an ex-situ process and the surface of III-V semiconductors are exposed to air prior to dielectric deposition, obtaining high quality interfaces are possible thanks to "self-cleaning" reactions that occur in the first cycle of deposition. Studies via x-ray photoelectron spectroscopy (XPS) revealed that the native surface oxides are removed substantially subsequent to exposure of metal organic precursors [19,31]. Hinkle et al. performed in-situ XPS analysis on GaAs surfaces to observe elimination of surface oxides with deposition of Al_2O_3 and HfO_2. The As *2p* and Ga *2p* spectra for GaAs substrates before and after the ALD deposition of dielectrics are presented in Figure 1.3. The As *2p* surface spectrum of untreated GaAs substrate has characteristic peaks of As^{+3} and As^{+5} states that refers to As_2O_3, As_2O_5 native oxides, respectively. The Ga *2p* spectrum of same substrate has a Ga-O peak was considered as convoluted feature of multiple oxidation states. The intensity of these peaks significantly decreased subsequent to deposition of 1 nm Al_2O_3 and HfO_2 dielectric layers. However, it is evident that the reduction in intensity of Ga-O peak is less which was attributed to more thermodynamically stable nature of Ga oxides compared to As oxides. Similar self-cleaning effect was observed with deposition of Al_2O_3 dielectric layers on InGaAs substrates [31].

To further improve the quality of high-κ/III-V interfaces, effects of various surface pretreatments were investigated extensively by other research groups [32,33,34]. The treatment of III-V surfaces with aqueous $(NH_4)_2S$ solutions have been frequently used for removal of native oxides . In addition to elimination of native oxides, this treatment leads to formation of sulfur monolayers that effectively passivates surface and protects it from further oxidation. This passivation layer vaporizes during the heating up the ALD chamber to deposition temperature. Diluted solutions of HCl and NH_4OH have also been extensively used for removal of native surface oxides [6]. Although wet etching techniques are proven to be efficient, the hydrogen plasma cleaning of III-V surfaces have also been investigated to meet the requirements MOSFET processing [33]. The hydrogen plasma cleaning can be used in the MOSFET process flow prior to gate dielectric deposition. The advantage of plasma treatment lies in cleaning of areas with small features; which is an important characteristic of technique providing compatibility with decreasing feature size. Carter et al. showed that hydrogen plasma treatment coupled with self-cleaning effect reduces Dit significantly which indicates that efficient removal of native surface oxides.

Al_2O_3 and HfO_2 are both the most promising dielectric candidates and deposition of these dielectric materials by ALD have been studied extensively. The interface properties of Al_2O_3/III-V structures are superior to HfO_2/III-V structures by means of low interface state density and less frequency dispersion in accumulation. However, the high dielectric constant of HfO_2 is intriguing for maintaining the required critical constant capacitance in highly scaled MOSFETs. Therefore, the deposition of Al_2O_3/HfO_2

dielectric stacks where the thin Al_2O_3 was used as interfacial layer due to its better quality of interface has been investigated [35]. The MOSCap structures with equivalent oxide thickness (EOT) of 1 nm was demonstrated by depositing thin layer of Al_2O_3 that followed by deposition of HfO_2. Suzuki et al. reported that a critical thickness of Al_2O_3 must be deposited before deposition of HfO_2 layer. The Dit decreased until critical thickness of Al_2O_3 was reached. Although Al_2O_3 and HfO_2 dielectrics in the center of the high-κ/III-V research, there are other alternative high-κ dielectrics with appealing properties, such as ZrO_2 , $TaSiO_x$, and La_2O_3 [10,11,36]. However, the electrical property of MOSCap structures fabricated with these dielectric materials are considerably poor due to high Dit.

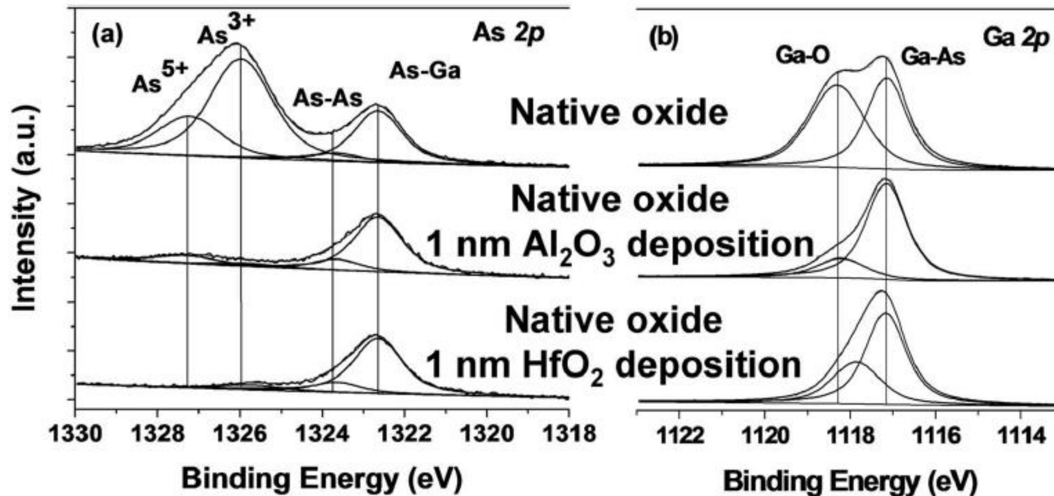


Figure 1.3: (a) As 2p 3/2 and (b) Ga 2p 3/2 XPS spectra presenting the reduction in peak intensity of native surface oxide with self-cleaning effect [19]

In this study MBE grown $In_{0.53}Ga_{0.47}As$ semiconductors coated by ALD with a HfO_2/Al_2O_3 dielectric bilayer were used to study interface properties. The surface clean process and deposition conditions of dielectric layers are given in detail in the Chapter 2

1.3 Review of Techniques to Quantify Interface States

Interface states arise from structural defects (vacancies, anti-site defects etc.), dangling bonds and impurities that are located at the dielectric/semiconductor interface. These defects at the interface introduce energy states into the bandgap which are spatially localized but distributed continuously in energy. These states can electrically communicate with conduction band or valence band of semiconductor depending on the surface potential and Fermi level. For example, in case of n-type semiconductor, interface states located below the Fermi level are completely occupied by electrons. These states may be negatively charged or neutral depending on their position in energy. Therefore, the negatively charge states show acceptor-like behavior. The Figure 1.4 shows the occupancy of interface states depending on the position of the Fermi level for n-type MOSCap at accumulation, flat band, and depletion regions, respectively.

The charge contribution from interface states is observable through electrical measurements and quantitative determination Dit is possible under well-defined circumstances. As explained the interface states can be charged and discharged by modulating the surface potential, we can now discuss the ways of modulating surface potential to change the occupancy of interface states. Interface states can respond to slow variation of the applied DC bias which provides adequate time for interface states

equilibrate at a given surface potential by capturing or emitting carriers. On the other hand, interface states can also follow the AC signal as long as the frequency of AC signal is lower than the emission rate of the interface states.. These properties of interfaces states were employed to develop different quantitative characterization techniques to determine their concentrations.

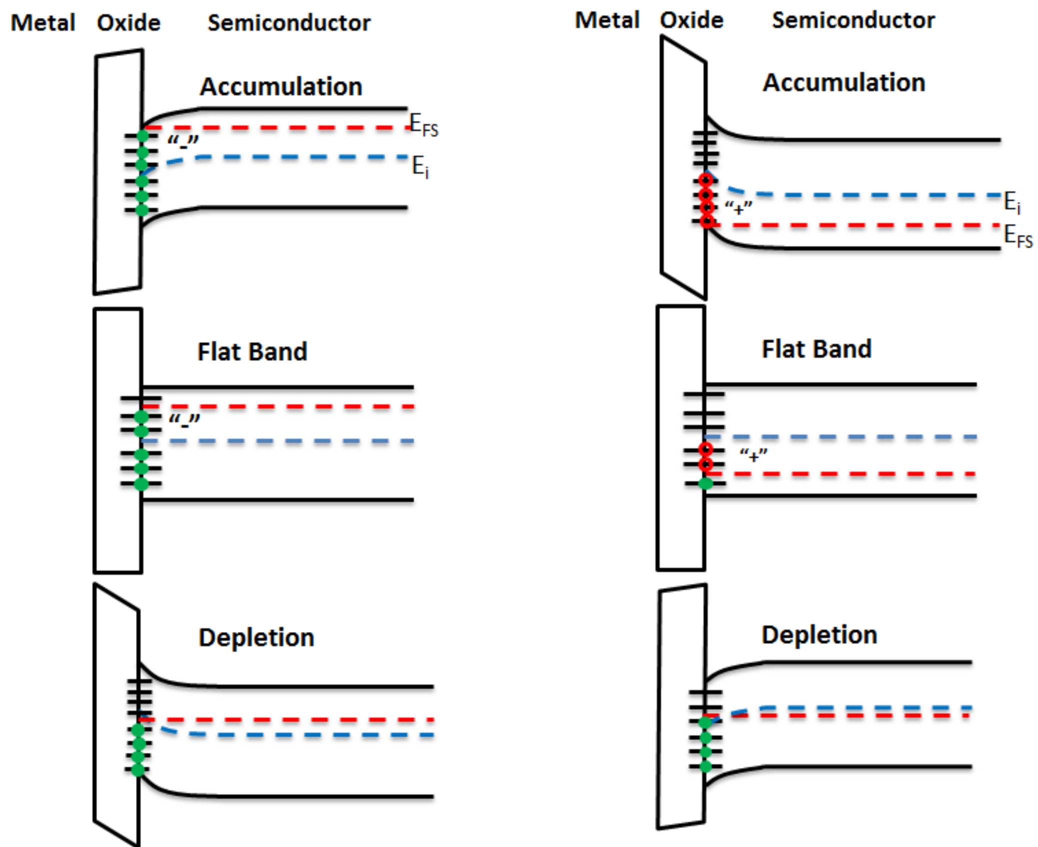


Figure 1.4: The occupancy of interface states relative to the position of Fermi level at the interface for n-type (on left) and p-type (on right). The charge states of interface states depending on their occupancy labeled by ("-") and ("+") which states

A series of techniques were developed to characterize the interface state density at the dielectric/semiconductor interface [12,13,14,15]. These techniques were used successfully to determine Dit values of SiO_2/Si system. Now, we are going to discuss technique and material related issues which may cause errors in the extracted Dit profiles. In general, the quantitative Dit characterization methods depend on capacitance or impedance measurements performed on MOSCaps. The measured capacitance of a MOSCap is directly related to total electrical charge and interface states may or may not contribute to total charge depending on the DC bias sweep rate or AC signal frequency. The comparison between a C-V curve that contains information on interface states and a C-V curve that lacks of any interface state information can give an estimate of the Dit. A series of techniques, such as Berglund method (low-frequency C-V method), Castagne-Vapaille Method (high-low frequency C-V method), and Terman method were developed to extract Dit from capacitance based measurements.

Interface states are able to follow an AC signal with low frequency and thus they contribute to total measured capacitance of a MOSCap. The capacitance contribution of interface states is given as $C_{it} = q^2 Dit$. However, at sufficiently high AC signal frequencies interface states cannot respond the AC signal and their contribution to total capacitance becomes zero. The difference in the total charge density alters the measured capacitance and this can be used to determine the total Dit as proposed by Castagne and Vapaille. In Berglund method, instead of using an experimental high frequency C-V curve for comparison, a calculated ideal C-V curve is utilized. The ideal C-V curve is calculated by assuming no interface states exist. In the Terman method, the high

frequency C-V curve is measured by varying DC gate bias with a slow rate. Although the AC signal is high and interface states are not able to follow it, they can follow the slow variation in the gate bias. The change in the occupancy of the interface states with variation of DC bias leads to stretch-out in the C-V curve along the voltage axis. Therefore, the required gate bias to acquire a constant surface potential changes with the change in occupancy of the interface states. The difference in the gate bias at a constant surface potential is used in calculating Dit. The detailed information on Terman method can be found in Chapter 2.

There are number of drawbacks of capacitance based techniques that may cause errors in the extracted Dit. The frequency of the AC signal for both low and high frequency C-V measurements is a crucial parameter which determines the degree of contribution from interface states to the measured capacitance. In the case of low frequency C-V measurements, the frequency of AC signal should be low enough to allow emission from interface states located relatively deep in the bandgap. On the contrary, the frequency of AC signal must be sufficiently high to avoid capacitance contribution from the interface states located closer to the band edges that have very short emission time constants. Therefore, both high and low frequency C-V measurements may not be able to provide true frequency dependent behavior that aimed to be acquired [7]. The accurate calculation of ideal C-V curve relies on realistic modeling of the semiconductor. The calculated ideal C-V curve may not represent the realistic behavior, if any invalid approximations or assumptions are used in calculations and cause error in the extracted Dit.

In the conductance method, the impedance of interface states is measured as a function of frequency while the DC bias is kept constant. The DC bias is used to acquire a desired band bending that determines the Fermi level position at the interface. The AC signal superimposed on the DC bias induces periodic variation in band bending which results change in Fermi level position within the energy range of a few kT/q at the interface. These oscillations in the Fermi level position lead to change in the occupancy of interface states within the energy range defined by the amplitude of AC signal. This variation in occupancy of traps results loss in the total energy of carriers and it can be measured as parallel conductance [15]. Therefore, the Dit can directly be calculated from the measured parallel conductance. The extraction of Dit will be discussed in Chapter 2.

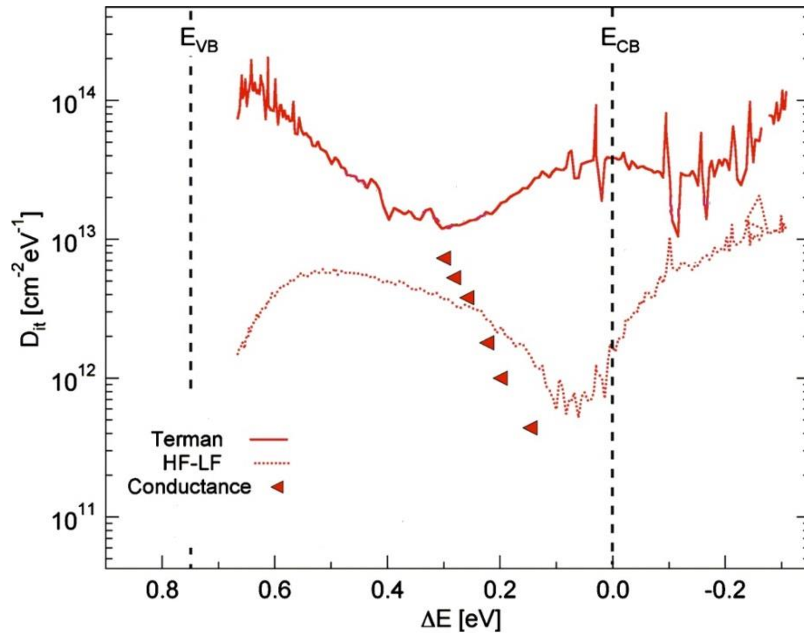


Figure 1.5: Dit spectra obtained from different techniques for 9 nm HfO_2/*n*-$In_{0.53}Ga_{0.47}As$ interface [16]

Now with the brief overview on techniques were provided, we can turn to discuss material specific issues. To discuss inconsistencies that arise from material specific issues in Dit spectra obtained from different techniques, results from literature will be presented next. Figure 1.2 presents the Dit distribution obtained from conductance method, high-low frequency method, and Terman method on the same HfO_2/n-$In_{0.53}Ga_{0.47}As$ MOSCap device that was annealed in forming gas ambient [16]. The discrepancy among the reported Dit spectra from different techniques is evident for this particular device. There is two orders magnitude difference between the extracted Dit near the conduction band edge. The shapes of distribution spectra obtained from each technique are also inconsistent. Conductance method yielded a distribution of interface traps which peaks towards the mid-gap. The extracted Dit is decreases from high-10^{12} to mid-10^{11} $cm^{-2}eV^{-1}$ within ~0.2eV range towards the conduction band. Lin et al. showed that conductance method provides erroneous results when C_{it} becomes larger than $4C_{ox}$. In such case, measured impedance is dominated by C_{ox} and leads to underestimated values of Dit. The Dit obtained from high-low frequency method falls from mid-10^{12} to high-10^{11} $cm^{-2}eV^{-1}$ towards to conduction band edge. This decreasing trend in Dit is probably observed due to the AC signal frequency of 1 MHz wasn't able to suppress emission from interface states located close to the conduction band. Therefore, the true high frequency C-V behavior could not be achieved and cause an artificial reduction in calculated Dit near the band edges. On the other hand, Terman method provided U-shaped distribution of interface states throughout the semiconductor bandgap. The ideal C-V curve was calculated by considering low conduction band density of states and non-parabolicity of

Γ valley in order to accurate modeling of semiconductor [15]. However, the extracted Dit may be inaccurate due to errors in doping concentration and C_{ox} that are used in the calculation of the ideal C-V curve. Dit is underestimated in case of the doping concentration that is used in calculation is high. On the contrary, using large C_{ox} value in calculation of ideal C-V curve will result that Dit to be overestimated. Therefore, the accurate determination of doping profile and C_{ox} values is crucial to accurately quantify Dit with Terman method.

Given the importance of determining the true Dit, including the energy distribution, the variance above gives pause as to what method is appropriate, and if the methods need to be modified. This provides motivation for the research conducted in this thesis where alternative methods are explored and applied to high-κ/III-V interfaces.

1.4 Research Objectives

It has been established that interface states hamper the realization of highly scaled high-κ/$In_{0.53}Ga_{0.47}As$ MOSFETs by means of degrading channel mobility of carriers, leading to insufficient Fermi level response and large sub-threshold swing voltage. The characterization techniques originally developed for Si/SiO_2 system, such as conductance, Terman, high-low frequency, and low-frequency methods provide wide range of interface states concentrations with wide variations in the distribution of states. The considerable differences on reported Dit; even on the same device, from different techniques indicates that the applicability of these techniques for characterizing high-κ/$In_{0.53}Ga_{0.47}As$ interfaces is questionable. The motivation of this study is the accurate

quantitative characterization of Dit at high-κ/$In_{0.53}Ga_{0.47}As$ interfaces and explaining discrepancies among the results by considering method and material related issues.

1.5 Outline of Thesis

This chapter has elucidated the importance of studying high-κ/III-V semiconductor interface properties along with techniques that utilized for characterization of high-κ/III-V semiconductor interfaces and provided background information on atomic layer deposition of high-κ dielectrics. In the second chapter, physics of carrier capture and emission process are summarized and detailed derivation of fundamental equations for both constant voltage and constant capacitance deep level transient spectroscopy are presented. Moreover, the second chapter introduces comprehensive analysis of frequently used conductance method and describes foundations of low temperature capacitance voltage (LTCV) method. The third chapter presents the interface state spectra obtained from each technique and addresses the discrepancies among the results. The fourth chapter concludes this study and proposes research path ways for future.

1.6 References

[1] C.H. Jan, "CMOS technology scaling for system-on-chip integration-past, present and future", *ECS Trans.*, vol.44, pp 451-470, 2012.

[2] D.J. Frank, R.H. Dennard, E. Nowak, P.M. Solomon, Y. Taur, and H.S.P. Wong, "Device scaling limits of Si MOSFETs and their application dependencies", *Proceedings of the IEEE*, vol. 89, no. 3, pp. 260-288, 2001.

[3] J.A. del Alamo, "Nanometer-scale electronics with III-V compound semiconductors", *Nature*, vol. 479, pp. 317-323, 2011.

[4] I.Thayne, X. Li, W. Jansen, I. Povey, E. O'Connor, M. Pemble, P. Hurley, J. Ahn, P. McIntyre, "III-V MOSFETs for sub-15 nm technology generation CMOS: some observations, Issues and Solutions", *CS MANTECH Conference Proceedings*, 2012.

[5] http://www.itrs.net/Links/2011ITRS/Home2011.htm

[6] S. Oktyabrsky, P.D. Ye, *Fundamentals of III-V semiconductor MOSFETs.* New York: Springer, 2010.

[7] D. K. Schroder, *Semiconductor material and device characterization*. New York: Wiley, 1990.

[8] E.J. Kim, E. Chagarov, J. Cagnon, Y. Yuan, A.C. Kummel et al. , "Atomically abrupt and unpinned $Al_2O_3/In_{0.53}Ga_{0.47}As$ interfaces:Experiment and simulation" *J. Appl. Phys.*, vol. 106, 124508, 2009.

[9] D. Zade, K. Kakushima, T. Kanda, Y.C. Lin, P. Ahmet, K. Tsutsui, A. Nishiyama, N. Sugii, E.Y. Chang, K. Natori, T. Hattori, H. Iwai, "Improving electrical characteristics of $W/HfO_2/In_{0.53}Ga_{0.47}As$ gate stacks by altering deposition techniques" *Microelectron. Eng.*, vol. 88, pp. 1109-1112, 2011.

[10] S. Koveshnikov, N. Goel, P. Majhi, H.Wen, M.B. Santosh, "$In_{0.53}Ga_{0.47}As$ based metal oxide semiconductor capacitors with atomic layer deposition ZrO_2 gate oxide demonstrating low gate leakage current and equivalent oxide thickness less than 1nm" *Appl. Phys. Lett.*, vol. 92, 222904, 2008.

[11] X. Wang, L. Dong, J. Zhang, Y. Liu, P. D. Ye, and R. G. Gordon, "Heteroepitaxy of La_2O_3 and $La_{2-x}Y_xO_3$ on GaAs (111) by atomic layer deposition: Achieving low interface trap density", *Nano Lett.* , vol. 13, pp. 594-599, 2013.

[12] C.N. Berglund, "Surface states at steam-grown silicon-silicon dioxide interfaces", *IEEE Trans. Electron Devices*, vol.13, no.10, 1966.

[13] L. M. Terman, “An investigation of surface states at a silicon/silicon oxide interface employing metal-oxide-silicon diodes,” *Solid-State Electron.*, vol. 5, pp. 285-299, 1962.

[14] R. Castagne, and A. Vapaille, “Description of the SiO_2-Si interface properties by means of very low frequency MOS capacitance measurements”, *Surf. Sci.*, vol. 28, pp. 157-193, 1971.

[15] E. H. Nicollian and J. R. Brews, *MOS (metal oxide semiconductor) physics and technology*. New York: Wiley, 1982.

[16] R. Engel-Herbert, Y. Hwang, and S. Stemmer, “Comparison of methods to quantify interface trap densities at dielectric/III-V semiconductor interfaces”, *J. Appl. Phys.*, vol. 50, 121101, December 2010.

[17] H.C. Lin, G. Brammertz, K. Martens, G. de Valicourt, and L. Negre et al., “The Fermi-level efficiency method and its applications on high interface trap density oxide-semiconductor interfaces”, *Appl. Phys. Lett.*, vol. 94, 153508, 2009.

[18] K. Martens, C.O. Chui, G. Brammertz, B.D. Jaeger, D. Kuzum, M. Meuris, M.M. Heyns, T. Krshnamohan, K. Saraswat, H.E. Maes, G. Groeseneken, “On the correct extraction of interface trap density of MOS devices with high mobility semiconductor substrates”, *IEEE Trans. Electron Devices*, vol. 55, no. 2, pp. 547-556, 2008.

[19] C.L. Hinkle, A.M. Sonnet, E.M. Vogel, S. McDonnell, G.J. Hughes et al. “GaAs interfacial self-cleaning by atomic layer deposition”, *Appl. Phys. Lett.*, vol. 92, 071901, 2008.

[20] M. Passlack, M. Hong, and C.P. Mannaerts, “Quasistatic and high frequency capacitance–voltage characterization of Ga_2O_3–GaAs structures fabricated by in situ molecular beam epitaxy”, *Appl. Phys. Lett.*, vol. 68, 1099, 1996.

[21] F. Ren, M. Hong, V.S. Hobson, J.M. Kuo, J.R. Lothian, J.P. Mannaerts, J. Kwo, S.G. Chu, Y.K. Chen, and A.Y. Cho, “Demonstration of enhancement-mode p- and n-channel GaAs MOSFETs with $Ga_2O_3(Gd_2O_3)$ as gate oxide” , *Solid-State Electron.*, vol.41, pp. 1751-1753, 1997.

[22] Y.C. Wang, M. Hong, J.M.Kuo, J.P. Mannaerts, J. Kwo, H.S. Tsai, J.J. Krajevski, Y.K. Chen, A.Y. Cho, “Demonstration of submicron depletion-mode GaAs MOSFETs with negligible drain current drift and hysteresis”, *IEEE Electron Device Lett.*, vol. 20, 457, 1999.

[23] P.D. Ye, G. D. Wilk, J. Kwo, B. Yang, H-J. L. Gossman, M. Frei, S. N. G. Chu, J. P. Mannaerts, M. Sergent, M. Hong, K. K. Ng, and J. Bude, “GaAs MOSFET with oxide gate dielectric grown by atomic layer deposition”, IEEE Electron Device Lett., vol. 24, no. 4, 2003.

[24] P.D. Ye, Y. Xuan, Y.Q. Wu, and M. Xu, "Inversion-mode $In_xGa_{1-x}As$ MOSFETs (x=0.53, 0.65, 0.75) with atomic-layer-deposited high-κ dielectrics", *ECS Trans.*, vol. 19, no.2, pp. 605-614, 2009.

[25] Y. Xuan, H.C. Lin, P.D. Ye, and G.D. Wilk, "Capacitance-voltage studies on enhancement-mode InGaAs metal-oxidesemiconductor field-effect transistor using atomic-layer-deposited Al_2O_3 gate dielectric", *Appl. Phys. Lett.*, vol. 88, 263518, 2006.

[26] H. Ishii, N. Miyata, Y. Urabe, T. Itatani, T. Yasuda et al., "High electron mobility metal-insulator-semiconductor field-effect transistors fabricated on (111)-oriented InGaAs channels", *Appl. Phys. Exp*., vol. 2, 121101, 2009.

[27] M. A. Negara, N. Goel, D. Bauza, G. Ghibaudo, and P.K. Hurley, "Interface state denisities, low frequency noise and electron mobility in surface channel $In_{0.53}Ga_{0.47}As$ n-MOSFETs with ZrO_2 gate dielectric", *Microelectron. Eng.*, vol. 88, pp. 1095-1097, 2011.

[28] R.L. Puurunen, "Surface chemistry of atomic layer deposition: A case study for the trimethylaluminum/water process", *J. Appl. Phys.*, vol. 97, 121301, 2005.

[29] M. Leskela, and M. Ritala, "Atomic layer deposition chemistry: Recent developments and future challenges", *Angew. Chem. Int. Ed*., vol. 42, pp. 5548-5554, 2003.

[30] M. Milojevic, C.L. Hinkle, F.S. Aguirre-Tostado, H.C. Kim, E.M. Vogel et al., "Half-cycle atomic layer deposition reaction studies of Al_2O_3 on $(NH_4)_2S$ passivated GaAs(100) surfaces" *Appl. Phys. Lett.*, vol. 93, 252905, 2008.

[31] M.L. Huang, Y.C. Chang, C.H. Chang, Y.J. Lee, P.Chang et al., "Surface passivation of III-V compound semiconductors using atomic-layerdeposition-grown Al_2O_3", *Appl. Phys. Lett.*, vol. 87, 252104, 2005.

[32] E. O'Connor, B. Brennan, V. Djara, K. Cherkaoui, S. Monaghan et al., "A systematic study of $(NH_4)_2S$ passivation (22%, 10%, 5%, or 1%) on the interface properties of the $Al_2O_3/In_{0.53}Ga_{0.47}As$/InP system for n-type and p-type $In_{0.53}Ga_{0.47}As$ epitaxial layers", *J. Appl. Phys.*, vol. 109, 024101, 2011.

[33] A.D. Carter, W.J. Mitchell, B.J. Thibeault, J.J.M. Law, and M.J.W. Rodwell, "Al_2O_3 growth on (100) $In_{0.53}Ga_{0.47}As$ initiated by cyclic trimethylaluminum and hydrogen plasma exposures", *Appl. Phys. Exp.*, vol. 4, 091102, 2011.

[34] E. O'Connor, S. Monaghan, K. Cherkaoui, I.M. Povey, and P.K. Hurley, "Analysis of the minority carrier response of n-type and p-type $Au/Ni/Al_2O_3/In_{0.53}Ga_{0.47}As$/InP

capacitors following an optimized $(NH_4)_2S$ treatment", *Appl. Phys. Lett.*, vol. 99, 212901, 2011

[35] R. Suzuki, N. Taoka, M. Yokoyama, S. Lee, S.H. Kim et al., "1-nm-capacitance-equivalent-thickness HfO_2/Al_2O_3/InGaAs metal-oxidesemiconductor structure with low interface trap density and low gate leakage current density", *Appl. Phys. Lett.*, vol. 100, 132906, 2012.

[36] C. Adelman, D. Lin, L. Nyns, B. Schepers, A. Delabie, S. Van Elshocht, M. Caymax, "Atomic layer deposited tantalum silicate as gate dielectric for III-V MOS devices", *Microelectron. Eng.*, vol. 88, pp. 1098-1100, 2011.

CHAPTER 2: EXPERIMENTAL TECHNIQUES AND BACKGROUND

2.1 Current Density-Voltage (J-V) Characteristics

A gate insulator is not expected to conduct electrical current during the device operation. However, in reality, some excessive leakage current may be observed due to the electric field across the gate oxide, defects and edge effects. Ideally, the amount of leakage current depends on the oxide thickness (t_{ox}), the applied gate bias (V_g), and the tunneling mechanisms which take place during the device operation. From the viewpoint of this research, high leakage currents can cause erroneous capacitance-voltage measurements results inaccurate doping profiles. Therefore, it is essential to perform J-V measurements on various devices to evaluate the quality of metal-oxide-semiconductor capacitor (MOSCap) structures. J-V characteristics were measured by using an Agilent 33220A Function/Arbitrary Waveform Generator as voltage supply and a Keithley 6485 Picoammeter as a current meter.

2.2 Capacitance-Voltage (C-V) Characteristics

Capacitance-voltage (C-V) profiling is a fast and convenient method to assess the quality of MOSCap structures. C-V measurements were employed to determine net carrier concentration and its depth profile in the semiconductor layer. Depth profiling of

charges was achieved by recording capacitance as a function of applied gate bias. The range of the applied gate bias is determined from the J-V measurements.

C-V measurements were performed on MOSCap structures by using Boonton 7200 capacitance meter with a sweep rate of 0.01V/s to obtain high frequency behavior. An AC signal of 50 mV with a 1MHz frequency was superimposed on DC bias throughout the C-V measurement. The C-V curve was used to define the accumulation, flat band, and depletion regions for MOSCap structure. In addition, the carrier concentration (N_D) was extracted from the derivative of high frequency C-V curve by using the following Eq (2.1)

$$N_D = -\frac{C^3}{q\varepsilon_s A^2 (dC/dV)} \quad \textbf{(2.1)}$$

where A is the surface area of the MOS capacitor and ε_s is the dielectric constant of semiconductor material. The depth profile of carrier concentration is expressed by means of

$$x_d = \frac{\varepsilon_s A}{C_m} \quad \textbf{(2.2)}$$

where x_d is the depletion depth and C_m is the measured capacitance. However, depletion depth calculation must be corrected for oxide capacitance (C_{ox}), since part of the applied gate bias drops across the oxide layer. Thus, the depletion depth values were corrected by using the Eq. (2.3) given below

$$W = \varepsilon_s A \left(\frac{1}{C} - \frac{1}{C_{ox}}\right) \quad \textbf{(2.3)}$$

An InGaAs MOSCap sample with an average carrier concentration of ~$2x10^{17}$ cm^{-3} was used in this study.

2.3 Deep Level Transient Spectroscopy

Deep level transient spectroscopy, originally developed by Lang (1974), is a highly sensitive electrical characterization technique used to determine concentration, activation energy, and capture rates of majority- or minority-carrier trap states located within the band gap of semiconductor materials [1]. Fundamentally, DLTS provides information on properties of discrete deep states within the depletion region of a Schottky or p-n junction by measuring capacitance transients. The transient behavior of capacitance is the result of thermal emission of trapped carriers from deep states under quiescent bias.

2.3.1 Physics of Carrier Emission

The deep states can communicate with the conduction band and valence band by exchanging carriers through four different processes. Namely, these are electron capture, electron emission, hole capture, and hole emission that are schematically given in Figure 2.1 from (a) to (d), respectively.

The rate equations can be derived for trapping events involving deep states. Following the literature [2], assume that the total density of trap states is

$$N_T = n_T + p_T \quad \textbf{(2.4)}$$

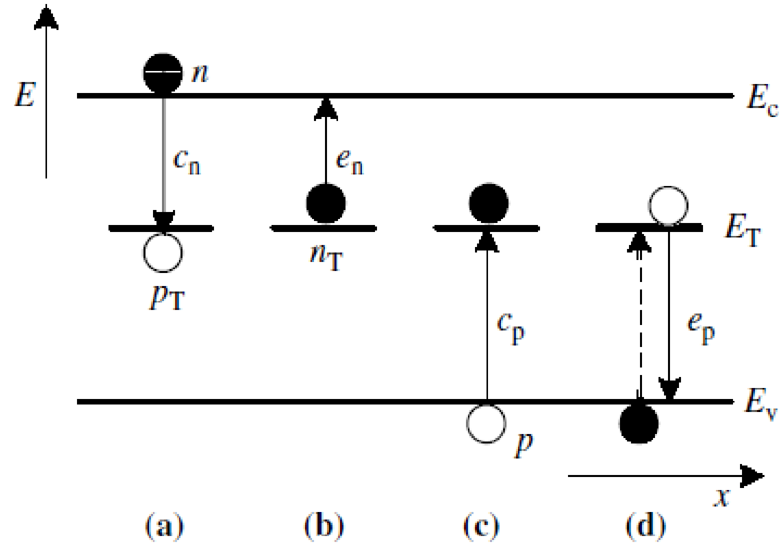


Figure 2.1: The possible capture-emission processes through deep states (a) electron capture (b) electron emission to conduction band (c) hole capture and (d) hole emission to valence band [3]

where n_T is the density of traps occupied by electrons and p_T is the density of traps empty of electrons. The rate equations for change in concentration of carriers in conduction band and valance band are given by

$$\left(\frac{dn}{dt}\right)_{G-R} = e_n n_T - c_n n p_T \qquad \textbf{(2.5.a)}$$

$$\left(\frac{dp}{dt}\right)_{G-R} = e_p p_T - c_p p n_T \qquad \textbf{(2.5.b)}$$

where c_n, c_p and e_n, e_p are the capture and emission rates of electrons and holes. The emission coefficients (e_n, e_p) have units of s^{-1}, while the capture coefficients (c_n, c_p) have the units of $cm^{-3}s^{-1}$. Auger and radiative processes are neglected and only emission and capture processes through trap states are considered for deriving rate equations [3]. The

rate of change in trap occupancy is described from difference in rate of change of both electron and hole concentrations in conduction and valence band

$$\frac{dn_T}{dt} = (c_n n + e_p)(N_T - n_T) - (c_p p + e_n)n_T \qquad \textbf{(2.6)}$$

This differential equation can be simplified to solve for two cases indicated by following assumptions; (1) n and p are negligibly small in a reverse-biased depletion space charge region, (2) n and p are constant in quasi-neutral regions. Solving Eq. (2.6) for the case (2) yields $n_T(t)$ as

$$n_T(t) = n_T(0)\exp\left(-\frac{t}{\tau}\right) + \frac{(e_p + c_n n)N_T}{e_n + c_n n + e_p + c_p p}\left(1 - \exp\left(-\frac{t}{\tau}\right)\right) \qquad \textbf{(2.7)}$$

where $n_T(0)$ is the concentration of trap states occupied by electrons at $t = 0$ and the emission time constant τ given

$$\tau = \frac{1}{e_n + c_n n + e_p + c_p p} \qquad \textbf{(2.8)}$$

The steady-state occupancy of the trap state can be determined from Eq. (2.7) as $t \rightarrow \infty$ and results

$$n_T(t = \infty) = \frac{(e_p + c_n n)}{e_n + c_n n + e_p + c_p p}N_T \qquad \textbf{(2.9)}$$

Eq. (2.9) has variables such as capture and emission rates that are unknown. This expression can be further simplified by considering an asymmetrical p^+-n junction or Schottky barrier on an n-type semiconductor where $n \gg p$, and p can be neglected. Thus, Eq. (2.7) becomes

$$n_T(t) = n_T(0)\exp\left(-\frac{t}{\tau}\right) + \frac{(e_p + c_n n)N_T}{e_n + c_n n + e_p}\left(1 - \exp\left(-\frac{t}{\tau}\right)\right) \quad \textbf{(2.10)}$$

and τ becomes

$$\tau = \frac{1}{e_n + c_n n + e_p} \quad \textbf{(2.11)}$$

Now, considering deep states located in quasi-neutral bulk region filled with electrons given schematically in Figure 2.2.(a). This is identical to applying a fill pulse during DLTS measurement to reduce the width of space charge region and for providing free carriers that can be captured by empty deep states. In this case, capture process overwhelms the emission process and so that $n_T \approx N_T$. Now, if a reverse bias is applied

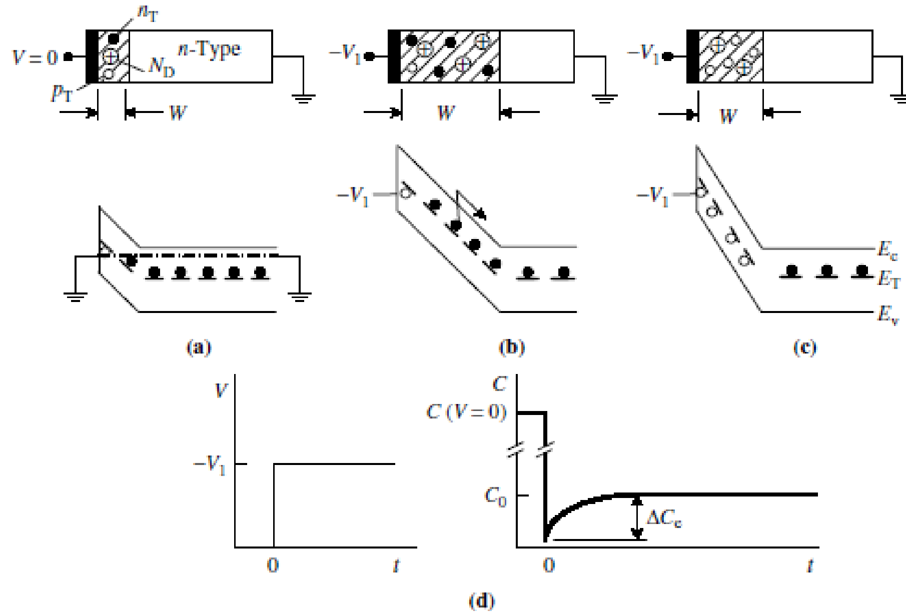


Figure 2.2: A Schottky diode for (a) Filling bias at 0V (b) quiescent bias at t=0 (c) quiescent bias at t=∞ (d) The applied voltage and resultant capacitance transient [3]

as shown in Figure 2.2.(b), the space charge region will expand. Since the space charge region is absent of free carriers, the emission process becomes dominant and emitted electrons swept out of the depletion region rapidly by the electric field. The swept time is significantly shorter than capture times, thus it is not possible to an electron to be recaptured. If the deep state is assumed to be located in the upper half of the band gap which means trapping event only involves conduction band. Therefore, $e_n \gg e_p$ and e_p can be neglected since the carrier emission to valance band is energetically unfavorable. In such a case, Eq. (2.10) can be simplified even further and it becomes

$$n_T(t) = n_T(0) \exp\left(-\frac{t}{\tau_e}\right) \approx N_T \exp\left(-\frac{t}{\tau_e}\right) \qquad \textbf{(2.12)}$$

where $\tau_e = 1/e_n$. The steady state trap density n_T in the reversed biased depletion region is

$$n_T(t = \infty) = \frac{e_p}{e_n + e_p} N_T \qquad \textbf{(2.13)}$$

Eq. (2.13) describes time dependence of n_T. The time variation of carrier population in deep states leads to change in depletion region capacitance of Schottky barrier or p^+-n junction. The electron emission causes increase in fixed positive charge in space charge region and results decrease in width of space charge region at constant voltage. The smaller the width of depletion region, larger the capacitance which can be expressed mathematically by

$$C = \frac{\epsilon A}{x_d} = \epsilon A \left[\frac{q N_D}{2\epsilon(V_{bi} - V)}\right]^{1/2} = \epsilon A \left[\frac{q(N_D - n_T)}{2\epsilon(V_{bi} - V)}\right]^{1/2} \qquad \textbf{(2.14)}$$

where N_D is the doping concentration of n-type semiconductor, V_{bi} is the built-in voltage, and V is the applied voltage. Eq (2.14) can be rewritten as

$$C = C_\infty \left(1 - \frac{n_T}{N_D}\right)^{1/2} \quad \textbf{(2.15)}$$

where C_∞ which is the steady state capacitance with no trap contribution is given as

$$C_\infty = \epsilon A \left[\frac{qN_D}{2\epsilon(V_{bi} - V)}\right]^{1/2} \quad \textbf{(2.16)}$$

We can assume that $N_T \ll N_D$, since deep level impurities are only a small portion of the charge density in depletion region and simplify Eq (2.15) by using first-order expansion

$$C(t) = C_\infty \left(1 - \frac{n_T(t)}{2N_D}\right) \quad \textbf{(2.17)}$$

Eq. (2.17) describes the time variation of capacitance in the presence of carrier capture or emission through a deep state. Defining steady state change in capacitance as $\Delta C = C(\infty) - C(0)$ we can rearrange Eq. (2.17) by using Eq. (2.12) to

$$\frac{\Delta C}{C_\infty} = \frac{n_T(0) - n_T(\infty)}{2N_D} \quad \textbf{(2.18)}$$

Since $N_T = n_T(0) - n_T(\infty)$, total trap concentration of a deep state can be expressed as

$$N_T = \frac{2N_D \Delta C}{C_\infty} \quad \textbf{(2.19)}$$

Now, the relationship between capacitance and deep state density is established, we can mathematically describe the capture and emission processes under equilibrium condition by using *principle of detailed balance* which indicates the rate of any process

and its inverse to each band must equal to zero. By using Eq. (2.5.a) we can determine relationship between capture coefficient and emission rate for the conduction band

$$\frac{dn}{dt} = 0 = e_n n_T - c_n n p_T \qquad \textbf{(2.20)}$$

and rearranging this

$$e_n = c_n n \frac{p_T}{n_T} = c_n n \left(\frac{N_T}{n_T} - 1\right) \qquad \textbf{(2.21)}$$

Under equilibrium conditions, according to the Fermi-Dirac statistics the relationship between n_T and N_T is given as

$$\frac{n_T}{N_T} = \frac{1}{1 + \exp\left(\frac{E_T - E_F}{kT}\right)} \qquad \textbf{(2.22)}$$

The n and n_i is depends on the position of Fermi level which are mathematically described by

$$n = n_i \exp\left(\frac{E_F - E_i}{kT}\right) \qquad \textbf{(2.23)}$$

and

$$n_i = N_C \exp\left(\frac{E_i - E_C}{kT}\right) \qquad \textbf{(2.24)}$$

where k is Boltzmann's constant, T is the temperature, and N_C is the *effective density of states in the conduction band*. Thus, incorporating Eq. (2.22), Eq. (2.23) and Eq. (2.24) into Eq. (2.21)

$$e_n = c_n N_C \exp\left(\frac{E_T - E_C}{kT}\right) \qquad \textbf{(2.25)}$$

The capture coefficient for electrons is defined as

$$c_n = \sigma_n v_{th} \tag{2.26}$$

where σ_n is the *electron capture cross section* and v_{th} is the *average thermal velocity* given as

$$v_{th} = \left(\frac{3kT}{m_n}\right)^{1/2} \tag{2.27}$$

where $m_n$is the *electron effective mass*. Additionally, the N_C is given as

$$N_C = 2\left(\frac{2\pi m_n kT}{h^2}\right)^{3/2} \tag{2.28}$$

Where h is the *Planck's constant*. The electron emission time constant; τ_n, of a deep state can be defined by substituting all into Eq. (2.25)

$$\tau_e = \frac{\exp\left(\frac{E_C - E_T}{kT}\right)}{\sigma_n v_{th} N_C} \tag{2.29}$$

We can introduce a new temperature independent material constant γ to simplify Eq. (2.29) which yields

$$\tau_e T^2 = \frac{\exp\left(\frac{E_C - E_T}{kT}\right)}{\gamma \sigma_n} \text{ where } \gamma = \left(\frac{v_{th}}{T^{1/2}}\right)\left(\frac{N_C}{T^{3/2}}\right) \tag{2.30}$$

which can be rearranged as follows

$$\ln(\tau_e T^2) = \exp\left(\frac{E_C - E_T}{kT}\right) - \ln(\gamma \sigma_n) \tag{2.31}$$

Eq. (2.31) is the fundamental DLTS equation used to determine activation energy of trap in its capture cross section. Arrhenius plot of $\ln(\tau_e T^2)$ vs. 1/kT provides a slope and intercept that required in the extraction of $E_C - E_T$ and σ_n values for individual deep state.

2.3.2 Double Boxcar Deep Level Transient Spectroscopy

Double boxcar approach, also developed by Lang, is automated data acquisition method used to determine characteristic emission rate of deep trap at a corresponding temperature. Basically, boxcar DLTS determines the capacitance difference over the measured capacitance transient in a time interval which is a fixed value between two times [1]. The difference in two capacitance value on transient can be described mathematically

$$\Delta C_0 = C(t_1) - C(t_2) = \frac{C_\infty N_T}{2N_D}\left[\exp\left(-\frac{t_2}{\tau_e}\right) - \exp\left(-\frac{t_1}{\tau_e}\right)\right] \qquad \textbf{(2.32)}$$

We can clarify the advantage of boxcar method by considering behavior of a trap at extremely low and high temperatures. At low temperatures, the thermal energy is not sufficient for emission of trapped carrier; therefore the charge state of trap is preserved. Since the occupancy of the trap is conserved, the change in capacitance between t_1 and t_2 is approximately zero. At elevated temperatures, the excessive thermal energy leads to rapid change in occupancy of the trap and trap emits the carrier quickly. Consequently, the difference in capacitance again is infinitesimally small. However, ΔC reaches to a maximum value somewhere in the range of these two temperature conditions for the fixed time interval between t_1 and t_2. The Figure 2.3 represents this phenomenon [ref].

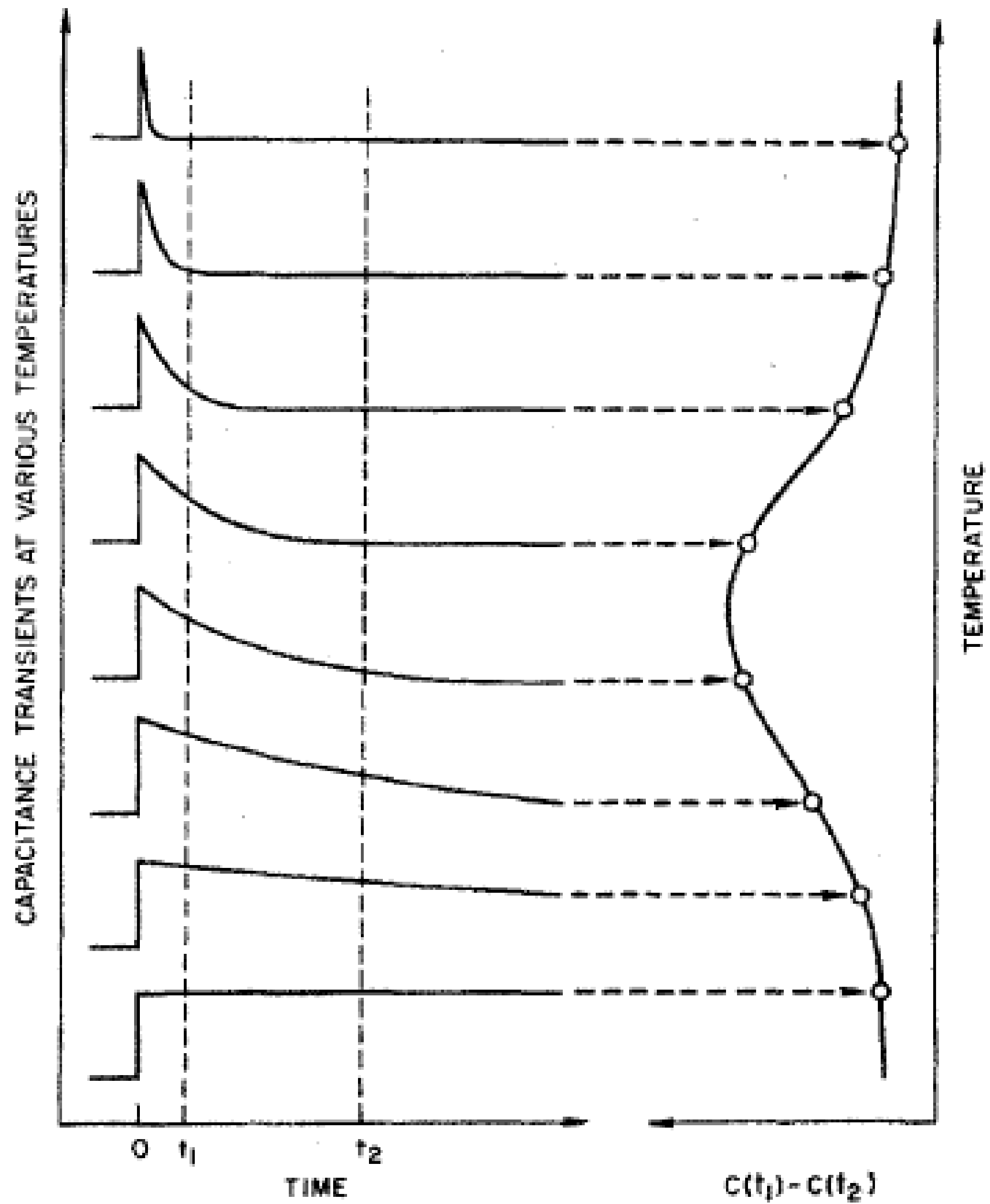


Figure 2.3: Illustration of how a typical DLTS trap spectrum is determined from the various capacitance transients measured at different temperatures [1]

The characteristic emission time constant can be determined from the peak in ΔC by taking the derivative of Eq. (2.32) and setting its derivative to zero

$$\tau_e = \frac{t_2 - t_1}{\ln(t_2/t_1)} \quad \textbf{(2.33)}$$

The fixed time interval defined from t_1 and t_2 times is generally called *rate window* and essentially used to sample different portions of the capacitance transients to determine ΔC_{max} as a function of temperature. By using various rate windows, one can obtain a set of $\tau_{e,max}$ values and peak temperatures which corresponds to data points on Arrhenius plot used to determine trap characteristics. In our system the rate windows were determined by fixing the $\beta = t_2/t_1$ ratio constant value of 2.5 and varying t_1 and t_2 values in order to keep peak height constant and avoid any variation from one rate window to another. We can also calculate the peak height from the ΔC_{max} by recalling Eq. (2.19) and correcting it for particular rate window:

$$N_T = \frac{2N_D\Delta C_{max}}{C_\infty}\left(\frac{\beta^{\beta/(\beta-1)}}{\beta - 1}\right) \quad \textbf{(2.34)}$$

where the uniform correction factor $r = \left(\frac{\beta^{\beta/(\beta-1)}}{\beta-1}\right)$ equals to 3.07. The identical signal-to-noise ratio can be acquired by keeping the r constant.

Now, the fundamental concepts derived for constant voltage deep level transient spectroscopy, we can move on to constant capacitance mode of DLTS and related physics.

2.3.3 Constant Capacitance Deep Level Transient Spectroscopy

In constant capacitance mode of DLTS, developed by Johnson et al, the capacitance of the device is kept constant and applied voltage is varied instantaneously by employing a feedback circuitry during the carrier emission [4,5]. Fundamentally, the width of the space charge region is held constant while the transients are recorded at different temperatures. Since the constant capacitance value is maintained throughout the measurement, the voltage transients are recorded and evaluated to extract trap properties. CC-DLTS is powerful electrical characterization technique that was employed to determine spatial distribution of discrete deep levels [5]. CC-DLTS has advantages over constant voltage DLTS described in the previous section. The most important advantage of CC-DLTS is that it is suitable for measuring high trap concentrations. The approximate capacitance transient is valid only for the case of $N_T \ll N_D$. However, for $N_T > 0.1N_D$, the exponential nature of capacitance transients vanish, since the variation in width of space charge region is significantly large [3]. However, the voltage transients conserve their exponential nature and more accurate defect profiling becomes possible.

CC-DLTS was also utilized in characterization interface states which are located at insulator-semiconductor interface. In nature interface states are spatially localized, but distributed in energy closely; therefore it is challenging to determine these states individually, yet profile of states can be obtained. CC-DLTS is suitable for characterization of interface states due to its high energy resolution and minimum signal distortion at high defect densities [4].

Now, we can introduce fundamentals of measuring voltage transients which contains interface state information. Figure 2.4 shows energy-band diagrams of a metal-oxide-semiconductor capacitor (MOSCap) with n-type substrate for depletion and accumulation conditions. In order to fill these states, the MOSCap is pulsed into accumulation which is the equilibrium condition. The interface states become filled with electrons due to increased population of electrons at the interface (Figure 2.4.(a)). When the device is biased back to depletion condition which is non-equilibrium condition, charge in interface states relaxes back to their equilibrium conditions (Figure 2.4.(b)). At depletion bias, band bending at the interface is downward and the Fermi level moves deep into the bandgap. The carriers do not reside at interface states with energies above the E_F. The emission rate can be monitored as a function of temperature and interface trap distribution over energy can be extracted. The capacitance and voltage behavior during in a CC-DLTS measurement is given schematically in Figure 2.4.(c).

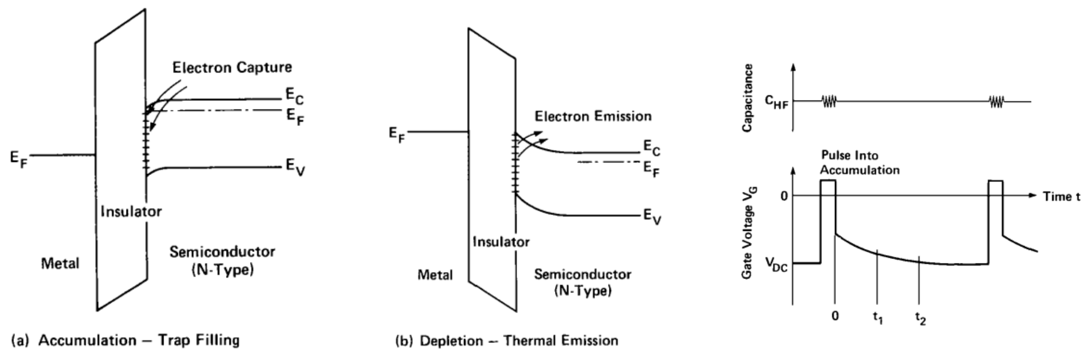


Figure 2.4: Energy band diagrams for MOSCap structure with n-type semiconductor (a) pulsed accumulation bias (b) non-equilibrium depletion bias (c) capacitance and gate voltage waveforms in CC-DLTS measurement [4]

Next, we need to derive the equations that are used to determine density of interface states and its energy distribution. The subsequent derivation follows treatment by Johnson et al, 1982. The recorded CC-DLTS signal ΔV_G is determined for different rate windows by measuring applied gate bias at two different times

$$\Delta V_G = V_G(t_1) - V_G(t_2) \quad \textbf{(2.35)}$$

There is linear dependency between ΔV_G and difference in net charge of interface states. The total high frequency capacitance of MOSCap in depletion is defined as

$$C_{total} = \frac{C_{ox}C_D}{C_{ox} + C_D} = constant \quad \textbf{(2.36)}$$

where C_{ox} is the oxide capacitance and C_D is the capacitance associated with the depletion layer in semiconductor. C_{ox} and C_D are considered as two parallel plate capacitor connected in series. During the transient response, the capacitance is kept constant by actually maintaining a constant depletion layer capacitance, since the C_{ox} is independent of bias. Let's consider the constituents of the applied gate bias

$$V_G = V_{ox} + \varphi_s \quad \textbf{(2.37)}$$

where V_{ox} is the voltage drop on oxide layer and φ_s is the surface potential. Since V_{ox} depends on interface state and depletion layer charge, from Gauss' law

$$V_{ox} = \frac{-A(Q_s + Q_{it})}{C_{ox}} \quad \textbf{(2.38)}$$

We can assume that depletion layer capacitance and surface potential are both constant during the transient response. Therefore, only observable voltage change is

reflected by the voltage drop across the oxide layer. Thus, from Eq. (2.35), Eq. (2.37), and Eq. (2.38)

$$\Delta V_G = \left(\frac{A}{C_{ox}}\right)[Q_{it}(t_1) - Q_{it}(t_2)] \quad \textbf{(2.39)}$$

The Eq. (2.39) indicates that there is a linear relationship between CC-DLTS signal and differences in net interface charge densities at times of t_1 and t_2 with a proportionality factor which is the inverse oxide capacitance per unit area.

The emission rate of majority carriers trapped in interface states located at E_C-E_T and at a time t is given by

$$\frac{dn_{it}}{dt} = -e_n n_{it}(E,t) \quad \textbf{(2.40)}$$

where e_n is the emission coefficient. Applying the principle of detailed balance, the emission coefficient can be described as

$$e_n = (\sigma_n v_{th} N_C/g)\exp\left(\frac{-(E_C - E_T)}{kT}\right) \quad \textbf{(2.41)}$$

where g is the spin degeneracy factor. The g is assumed to be unity, since the nature of the interface states are not well known.

ΔV_G signal must be integrated over an energy interval where the dominant charge redistribution process at the interface is due to majority carrier emission from interface states. This is required, since interface states are continuously distributed in energy so closely throughout the semiconductor band gap. The integration of Eq. (2.39) results

$$\Delta V_G = \left(\frac{A}{C_{ox}}\right) \int qD_{it}(E)[\exp(-e_n t_1) - \exp(-e_n t_2)]dE \qquad \textbf{(2.42)}$$

where q is the elementary charge. The distribution of emission can be extracted by evaluating the exponential terms in the integrand. The distribution of emission is peaked at an emission rate or in other words at a characteristic time constant. The emission rate is given as

$$e = \frac{1}{\tau_{max}} = \frac{\ln(t_2/t_1)}{(t_2 - t_1)} \qquad \textbf{(2.43)}$$

This is substituted in Eq. (2.41) and rearranged to obtain corresponding energy which states the location of interface states in bandgap

$$E_0 = kT \ln(\sigma_n v_{th} N_C / e) \qquad \textbf{(2.44)}$$

The capture cross section of interface states is assumed to be independent of energy and $\sigma_n = 1 \times 10^{-16} cm^2$ [6] is used as constant value in this study. In case of linear variation of interface state density Dit over energy interval, Dit can assumed to be constant can be taken out from the integrand in Eq. (2.42) which provides an effective energy interval expressed as

$$\Delta E_n \equiv \int_{-\infty}^{\infty} [\exp(-e_n t_1) - \exp(-e_n t_2)]dE \qquad \textbf{(2.45)}$$

Since the capture cross section is independent of energy, the effective energy interval simplified to

$$\Delta E_n = kT \ln(t_2/t_1) \qquad \textbf{(2.46)}$$

which indicates the effective energy interval depends on the fixed ratio that is used for defining rate windows. The assumption of linear variation of Dit in ΔE_n Eq. (2.42) becomes

$$\Delta V_G = \frac{qAD_{it}(E)\Delta E_n}{C_{ox}} \qquad \textbf{(2.47)}$$

or

$$D_{it}(E) = \frac{\Delta V_G C_{ox}}{qAkT \ln(t_2/t_1)} \qquad \textbf{(2.48)}$$

If we put it into words, ΔV_G emerges from the emission of carriers located in the effective energy interval of ΔE_n with a mean energy of E_m. The mean energy E_m defines the properties of interface states and it does not correspond to peak value of the emission peak which is defined by Eq. (2.46).

2.4 Low Temperature Capacitance Voltage Method

Low Temperature Capacitance-Voltage (LT-CV) method is essentially a modified Terman Method. LT-CV method eliminates the necessity of employing various approximations and assumptions which may lead to errors in extraction of interface states (Dit) in Terman Method.

In Terman method [7], a theoretical C-V curve without interface state contribution is compared to quasi-static high frequency C-V curve to obtain interface state distribution. The experimental C-V measurement is performed at a frequency where the interface states are not able to follow the superimposed AC signal. Although the interface states do not respond to the AC signal, they can respond to a slowly varying DC bias.

Due to change in trap occupancy based on slow DC bias sweeping rate, C-V curve shifts along the voltage axis.

In order to calculate the Dit, first, surface potential (φ_s) must be calculated for a corresponding high frequency capacitance value from Eq (2.4) given below;

$$q\varphi_s = \frac{q\varepsilon_s N_D}{2C_m^2} \tag{2.49}$$

After the calculation of relevant φ_s, V_g values that correspond to every constant capacitance (or constant φ_s) are determined from both theoretical and experimental C-V curves and then plotted against the calculated φ_s. Since the experimental V_g vs. φ_s curve contains the information on interface states, Dit can be calculated by

$$D_{it}(\varphi_s) = \frac{C_{ox}}{q^2 A}\frac{\partial(\Delta V_{G,T})}{\partial \varphi_S} \tag{2.50}$$

where $\Delta V_{G,T} = V_{G,exp} - V_{g,ideal}$ is the shift in gate bias due to contribution from interface states.

The Terman method can be used to determine Dit of 10^{10} $cm^{-2}eV^{-1}$ and above [3]. However, the method has number of limitations which can significantly affect the extracted interface state concentrations. As stated previously in section 2.2, high leakage current can alter the measured capacitance which may result inaccurate carrier profiles. Since the surface potential, φ_s, directly depends on carrier concentration extracted Dit will be wrong. Another error in extracted Dit may arise due to ac probe frequency. In order to avoid any ac trap contribution to experimental C-V curve, small signal frequency is required to be high enough to overcome response of interface states with minimum

characteristic time constant. Otherwise, it is not possible to obtain real quasi-static high frequency C-V curve and the extracted Dit is inaccurate.

Above all limitations, the most important issue which can introduce error in extraction of Dit is the realistic modeling of the C-V behavior of MOSCap structure. The calculation of theoretical C-V curve for semiconductor materials whose Fermi level does not move out of the band gap at all applied V_g can be achieved through classical approximation [6]. In classical approximation, the charge carrier density at the surface of semiconductor material which is defined by a Boltzmann distribution function is utilized to calculate theoretical C-V curve. Although the classical approximation is valid for MOSCaps with SiO_2/Si or high-κ dielectric/Si interfaces, it is not suitable for calculating theoretical C-V curves of MOSCap structures with high-κ dielectric/InGaAs interface. Since InGaAs has low conduction band density of states accompanying with non-parabolicity of lowest conduction band valley, classical approximation does not provide reliable theoretical C-V curves.

In order to overcome these limitations, we developed the LT-CV method. The LT – CV measurement was performed at 77 K. First, the MOS capacitor was biased into depletion at 295K to empty interface states and then it was cooled down to 77K while the depletion bias was maintained. Then a slow C-V was measured by ramping the DC bias from the depletion to accumulation in ~8hr. Since the carrier capture probability decreases due to low majority carrier density at 77K, such a low bias ramping rate was employed to ensure the capture of electrons by interface states. The capacitance was verified to reach equilibrium by monitoring the capacitance transient after each bias

change (0.01V/step), and had reached steady state before recording the capacitance and moving to the next bias. This ensured that the traps had equilibrated to the new bias and the resultant Dit spectrum was correct. Following the slow C-V measurement, a fast C-V measurement was performed in 10 ms sweeping the DC bias from accumulation to depletion and back to accumulation to prevent any electron emission from interface states. The low measurement temperature and high DC bias ramping rate is limited the emission of electrons from the filled states and the charge contribution from the trapped electrons result a significant shift on the CV curve. To extract the concentration of interface states and their distribution throughout the bandgap, slow C-V curve is compared to a theoretical C-V [6] curve and fast C-V curve by using Terman method.

The slow C-V measurement was performed by using Boonton 7200 capacitance meter with a superimposed AC signal of 50 mV at 1MHz frequency. The fast C-V curve is measured by using Agilent 33220A Function/Arbitrary Waveform Generator as voltage supply and recording capacitance through NI BNC221 data acquisition card connected to Boonton 7200.

2.5 Conductance Method

The conductance method was developed by Nicollian and Goetzberger in 1967. Fundamentally, a small AC voltage is superimposed on the DC gate bias in order to modulate interface states within the energy range of a few kT/q wide centered on the Fermi level. The occupancy of interface states that are located in this energy range changes, since the position of the Fermi level moves respect to position of interface states

in energy. This change in occupancy of interface states results an energy loss that can be measured as parallel conductance, G_P. The energy loss occurs, because the interface traps are not able to follow the AC signal immediately, instead lag behind it. On the other hand, energy loss is not observed at very low frequencies and very high frequencies, since interface states respond the AC signal immediately or not able to respond at all [8].

Let's consider the energy loss process through interface states in MOSCap structure with n-type semiconductor which is biased into depletion. The positive half cycle of the AC signal moves the conduction band towards the Fermi level at the interface. This causes increase in the average total energy of electrons at semiconductor surface. Thus, there are unoccupied interface states located below the Fermi level, since they are not able to follow the AC signal instantaneously. These empty interface states capture electrons with higher average energy that causes energy loss. The energy loss also occurs during the negative half cycle of the AC signal. The conduction band moves away from the Fermi level and the trapped electrons will be at higher energy than the free electrons inside the semiconductor. As electrons are emitted from these interface states into the semiconductor, electrons lose energy until the energy of trapped electrons and free electrons equilibrated. The energy loss that occurs in both halves of the cycle is dissipated into the lattice by phonons [8].

The conductance method is performed in the depletion, because the dominant capture and emission processes involve only the majority carriers. The Figure 2.5(a) shows the total equivalent circuit of a MOSCap in depletion for a single level interface trap. The total equivalent circuit is the series combination of semiconductor admittance Y_s

and oxide capacitance $j\omega C_{ox}$. The analysis of the equivalent circuit yields semiconductor admittance Y_s [8],

$$Y_s = j\omega C_D + \frac{j\omega C_{it} G_n}{G_n + j\omega C_{it}} \quad \textbf{(2.51)}$$

where C_{it} is the interface trap capacitance, C_D semiconductor depletion layer capacitance, and G_n the conductance associated with capture-emission of electrons. The equivalent parallel conductance G_P and capacitance C_P corresponding to Eq. (2.51) are

$$\frac{G_P}{\omega} = \frac{C_{it}\omega\tau}{1 + (\omega\tau)^2} \quad \textbf{(2.52)}$$

and

$$C_P = \frac{C_{it}}{1 + (\omega\tau)^2} + C_D \quad \textbf{(2.53)}$$

where

$$\tau = \frac{C_T}{G_n} \quad \textbf{(2.54)}$$

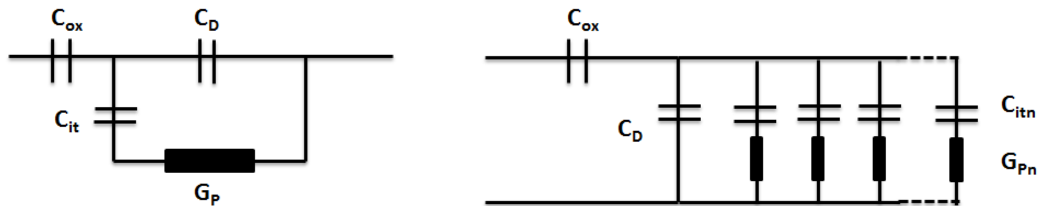


Figure 2.5: (a) The equivalent circuit of single-level interface trap (b) The equivalent circuit of distribution of single-level interface traps [8,9]

However, the interface states are continuously distributed in energy that forms a continuum of states throughout the semiconductor bandgap. The equivalent circuit for a single level interface trap can be extended into parallel combination of single interface states as schematically shown in Figure 2.5(b). The parallel conductance G_P and capacitance C_P for continuously distributed interface states are defined as [8,9]

$$C_P \equiv \frac{C_D}{C_{it}(\omega\tau_n)\tan(\omega\tau_n)} \tag{2.55}$$

And

$$\frac{G_P}{\omega} \equiv \frac{\ln[1+(\omega\tau_n)^2]}{C_{it}(\omega\tau_n)} \tag{2.56}$$

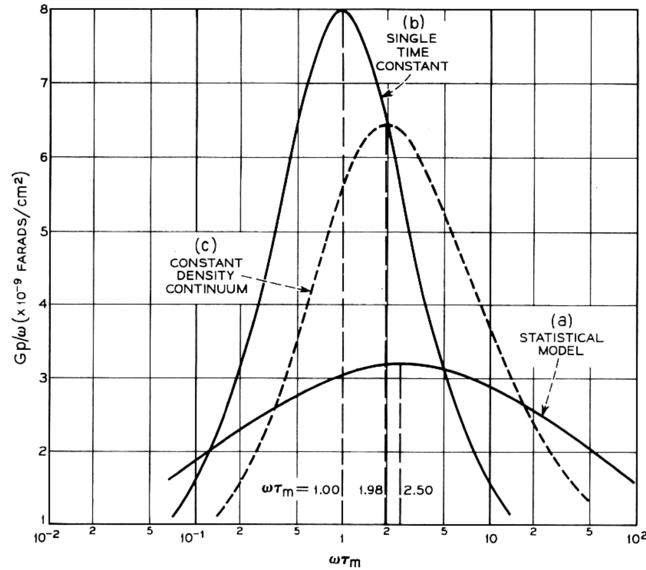


Figure 2.6: G_P/ω curves obtained by using different models(a) Fit to experimental data using Eq. 2.57 (Dit was estimated for best fitting) (b) single-level interface trap from Eq. 2.52 (c) Continuum of interface states from Eq. 2.56 [8]

The G_P/ω curves that are obtained from Eq. (2.53) and Eq. (2.56) for $\tau_n = 7 \times 10^{-5}\, s$ and $D_{it} = 1.9 \times 10^9 cm^{-2} eV^{-1}$ are given in Figure 2.6. The continuous distribution of interface states results time constant dispersion due to response of interface traps located in the modulation range of the AC signal.

The Figure 2.6 also shows experimental G_P/ω data was obtained as function of frequency at constant gate bias. The experimental curve is much broader and the peak height is lower compared to curve for continuum of states. This phenomenon was associated with surface potential fluctuations due to non-uniform distribution of interface states, oxide charges and doping concentration. If the band bending fluctuations are considered, the Eq. (2.56) becomes

$$\frac{G_P}{\omega} = \frac{q}{2}\int_{-\infty}^{\infty} \frac{D_{it}}{\omega\tau_n} \ln(1 + (\omega\tau_n)^2) P(v_s) dv_s \qquad \textbf{(2.57)}$$

where, $P(v_s)$ is the probability density function as a function of band bending fluctuations. $P(v_s)$ is defined as

$$P(v_s) = \frac{1}{\sqrt{2\pi\sigma_s^2}} \exp\left(-\frac{(v_s - \overline{v_s})^2}{2\sigma_s^2}\right) \qquad \textbf{(2.58)}$$

where $\overline{v_s}$ is the mean band bending fluctuation and σ_s^2 is the variance of band bending in units of eV. The mathematical treatment of Eq. (2.57) leads to more explicit form of this equation that reveals effect of band bending fluctuations on extracted D_{it}. We start by recalling expression for the characteristic time constant of electrons $\tau_n^{-1} = c_n N_D$. Then, substituting this and Eq. (2.58) into Eq. (2.57) gives

$$\frac{\overline{G_P}}{\omega} = \frac{1}{2} q D_{it} (2\pi\sigma_s^2)^{-1/2} \left(\frac{c_n N_D}{\omega}\right) \int_{-\infty}^{\infty} \exp\left[-\frac{(v_s - \overline{v_s})^2}{2\sigma_s^2}\right] \exp(-v_s) \times \ln[1 + \omega^2 (c_n N_D)^{-2} \exp(2v_s)] dv_s \quad \textbf{(2.59)}$$

where the mean bend bending fluctuation becomes equivalent to the measured characteristic time constant

$$\tau_n = \frac{1}{c_n N_D} \exp(-\overline{v_s}) \quad \textbf{(2.60)}$$

and by redefining $\omega\tau_n$ as

$$\xi = \omega\tau_n \cong \frac{\omega}{c_n N_D} \exp(-\overline{v_s}) \quad \textbf{(2.61)}$$

and making required substitutions in Eq. (2.59) yields

$$\frac{\overline{G_P}}{\omega} = \frac{q D_{it} (2\pi\sigma_s^2)^{-1/2}}{2\xi} \int_{-\infty}^{\infty} \exp\left(-\frac{\eta^2}{2\sigma_s^2}\right) \exp(-\eta) \ln(1 + \xi^2 \exp(2\eta))\, d\eta \quad \textbf{(2.62)}$$

where $\eta = v_s - \overline{v_s}$. We can solve Eq. (2.62) at the peak value of G_P/ω to get the D_{it}

$$D_{it} = \left(\frac{\overline{G_P}}{\omega}\right)_{max} f_D(\sigma_s) \quad \textbf{(2.63)}$$

where $f_D(\sigma_s)$ is a universal function of standard deviation of band bending given as

$$f_D(\sigma_s) = \left\{\frac{q (2\pi\sigma_s^2)^{-1/2}}{2\xi} \int_{-\infty}^{\infty} \exp\left(-\frac{\eta^2}{2\sigma_s^2}\right) \exp(-\eta) \ln(1 + \xi^2 \exp(2\eta))\, d\eta\right\}^{-1} \quad \textbf{(2.64)}$$

$f_D(\sigma_s)$ provides a constant value that is calculated by using standard deviation of band bending, σ_s. The Figure 2.7 shows the plot of $f_D(\sigma_s)$ as a function of σ_s.

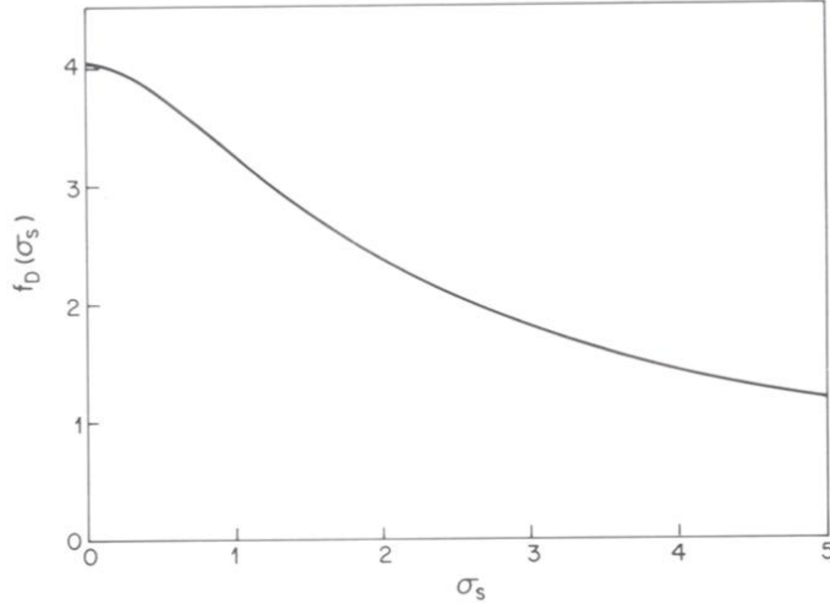


Figure 2.7: Plot of universal function $f_D(\sigma_s)$ as a function of σ_s. $f_D(\sigma_s)$ is used to calculate Dit [8]

In order to determine $f_D(\sigma_s)$ value, we should evaluate the width of the experimental G_P/ω calculated by

$$\frac{\overline{G_P}}{\omega} = \frac{\omega C_{ox}^2 G_m}{G_m^2 + \omega^2 (C_{ox} - C_m)^2} \qquad \textbf{(2.65)}$$

which is obtained from the circuit translation given in Figure 2.8. Fundamentally, Eq. (2.65) corrects the measured G_P/ω for oxide capacitance assuming negligible series

resistance. The width of the experimental curve is solely the measure of the σ_s, if the measurement is performed as a function of frequency at constant bias [8,10].

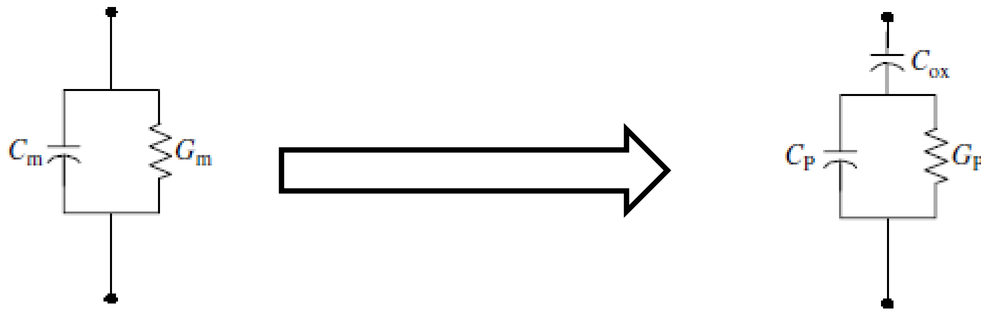


Figure 2.8: The circuit translation required to calculate curves G_P/ω from the measured admittance [3]

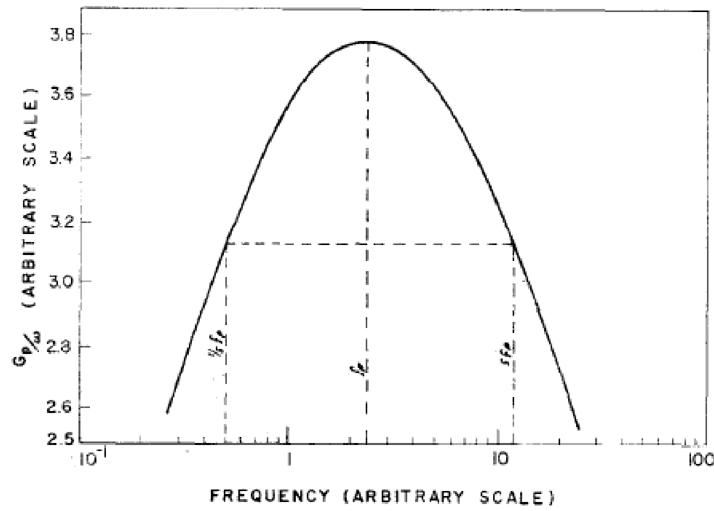


Figure 2.9: A typical $\boldsymbol{G_P/\omega}$ versus log frequency curve calculated from Eq. (2.65) [10]

Let's consider the G_P/ω versus frequency curve given in Figure 2.9. In order to determine σ_s, the change in amplitude must be measured between the f_P and f_P/n or between f_P and nf_P. The f_P is the frequency AC signal frequency at $(G_P/\omega)_{max}$. By proportioning the G_P/ω values at f_P and f_P/n

$$\frac{(\overline{G_P}/\omega)_{f_P/n}}{(\overline{G_P}/\omega)_{f_P}} = n\frac{\int_{-x}^{x} \exp\left(-\frac{\eta^2}{2\sigma_s^2}\right) \exp(-\eta) \ln(1+\xi^2 \exp(2\eta)/n^2)\, d\eta}{\int_{-x}^{x} \exp\left(-\frac{\eta^2}{2\sigma_s^2}\right) \exp(-\eta) \ln(1+\xi^2 \exp(2\eta))\, d\eta} \quad \textbf{(2.66)}$$

and similarly at f_P and nf_P

$$\frac{(\overline{G_P}/\omega)_{nf_P}}{(\overline{G_P}/\omega)_{f_P}} = n\frac{\int_{-x}^{x} \exp\left(-\frac{\eta^2}{2\sigma_s^2}\right) \exp(-\eta) \ln(1+\xi^2 \exp(2\eta)/n^2)\, d\eta}{\int_{-x}^{x} \exp\left(-\frac{\eta^2}{2\sigma_s^2}\right) \exp(-\eta) \ln(1+\xi^2 \exp(2\eta))\, d\eta} \quad \textbf{(2.67)}$$

These ratios are the single-valued functions of σ_s where they plotted in Figure 2.10 for n=5. The$(\overline{G_P}/\omega)/(\overline{G_P}/\omega)_{f_P}$versus σ_s plot is obtained by using ratios from the experimental curves that are measured for various constant gate bias conditions [8].

For $\sigma_s < 1.8$, the G_P/ω curves becomes asymmetrical indicated by variation of ratios for low and high frequency parts of the curves. For $\sigma_s > 1.8$, Gaussian weight factor given by Eq. (2.58) becomes dominant and as a result G_P/ω curves are symmetrical. The $f_F(1.8) = 2.5$ can be extracted from the plot of $f_D(\sigma_s)$ versus σ_s given as Figure 2.7. Since the σ_s does not vary significantly for Si, the an approximate expression for extraction of D_{it} is defined as

$$D_{it} = 2.5\left(\frac{\overline{G_P}}{\omega}\right)_{max} \quad \textbf{(2.68)}$$

The Eq. (2.68) is valid, if only the interface state density and band bending fluctuation slowly varying within the potential range of $\sim 2.5kT/q$. However, this may not be the case for high-κ dielectric/III-V interfaces. Therefore, $f_D(\sigma_s)$ value must be calculated for each G_P/ω curve measured at different gate bias to determine D_{it} accurately [10]. The variable frequency C-V and G-*f* measurements were performed by using Agilent E4980A LCR meter. The AC signal amplitude of 25 mV was used for all measurements. The G-*f* measurements were performed at constant DC bias ranging from 0V to -0.9V. The C-V measurements were conducted at various small signal frequencies from 20 Hz to 1MHz to observe effect of interface trap response on capacitance.

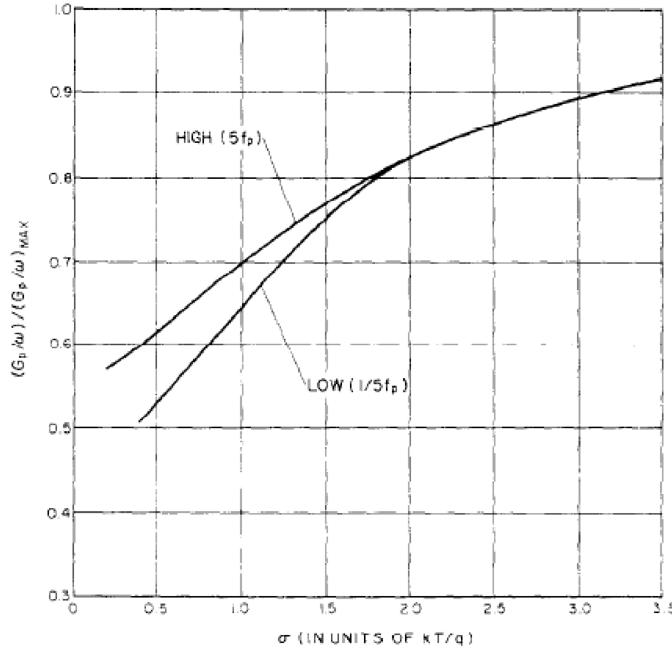


Figure 2.10: The $(\overline{G_P}/\omega)/(\overline{G_P}/\omega)_{f_P}$ versus σ_s plot. This curve is used to get σ_s from the width of a G_P/ω versus log f curve measured at constant gate bias [8]

2.6 Sample Description and Device Processing

For this study, metal-oxide-semiconductor capacitor (MOSCAP) structures were used to characterize the interface state density of an ALD HfO_2/Al_2O_3 dielectric stack deposited on an epitaxial n-type $In_{0.53}Ga_{0.47}As$ layer on lattice matched InP. The semiconductor was 300 nm thick n-$In_{0.53}Ga_{0.47}As$ with Si doping of $1x10^{17}$ cm^{-3} grown by molecular beam epitaxy on an n^{+}InP substrate. Prior to dielectric deposition, the sample was dipped in HCl:DI [1:1] for 2 min. to remove surface oxides and clean the surface. Then, the sample was loaded into Oxford Instruments FlexAL ALD reactor, where Al_2O_3 and HfO_2 precursors were trimethylaluminum, tetrakis[ethylmethylamino]hafnium (TEMAH), and deionized H_2O, and heated up to 300˚C under the pressure of 200 mTorr. The sample surface was exposed to hydrogen plasma/TMA/hydrogen plasma cycle in order to improve oxide removal and increase the quality of initial Al layer. After the initial cycle, the growth proceeded with the typical pulse water, purge, pulse TMA or TEMAH, purge cycle.The final dielectric thicknesses consisted of 2 nm of HfO_2 deposited on 3 nm of Al_2O_3 and had an equivalent oxide thickness of 1.9 nm. All ALD processing was done via our UCSB collaboration. Subsequent device processing occurred at OSU. MOSCaps were formed by depositing 80 nm thick Ni contacts using e-beam deposition through a shadow mask on top of the dielectric stack and a Cr (20 nm) /Au(100 nm) e-beam deposited Ohmic contact to the back of the InP substrate. After the metal deposition, the devices were annealed in forming gas (95% of N_2 and 5% of H_2) for 50 min at 400 °C to further improve the interface quality.

2.7 References

[1] D. V. Lang, "Deep level transient spectroscopy: a new method to characterize traps in semiconductors," *J. Appl. Phys.,* vol. 45, pp. 3023-3032, 1974.

[2] P. Blood and J. W. Orton, *The electrical characterization of semiconductors: majority carriers and electron states*. San Diego:Academic Press, 1992.

[3] D. K. Schroder, *Semiconductor material and device characterization*. New York: Wiley, 1990.

[4] N. M. Johnson, "Measurement of semiconductor-insulator interface states by constant-capacitance, deep-level transient spectroscopy," *J. Vac. Sci. Technol.*, vol. 21, no. 2, pp. 303-314, 1982.

[5] N. M. Johnson and D. J. Bartelink, "Constant-capacitance DLTS measurement of defect-density profiles in semiconductors," *J. Appl. Phys.*, vol. 50, no. 7, pp. 4828-4833, 1979.

[6] R. Engel-Herbert, Y. Hwang, and S. Stemmer, "Comparison of methods to quantify interface trap densities at dielectric/III-V semiconductor interfaces" *J. Appl. Phys.*, vol. 50, 121101, 2010.

[7] L. M. Terman, "An investigation of surface states at a silicon/silicon oxide interface employing metal-oxide-silicon diodes," *Solid-State Electron.*, vol. 5, pp. 285-299, 1962.

[8] E. H. Nicollian and J. R. Brews, *MOS (metal oxide semiconductor) physics and technology*. New York: Wiley, 1982.

[9] K. Lehovec, "Frequency dependence of the impedance of distributed surface states in MOS structures," *Appl. Phys. Lett.*, vol. 8, no. 2, pp. 48-50, Jan 1966.

[10] E.H. Nicollian, A. Goetzberger, and A.D. Lopez "Expedient method of obtaining interface state properties from MIS conductance measurements", *Solid-State Electron.*, vol. 12, pp. 937-944, 1969.

CHAPTER 3: RESULTS AND DISCUSSION

3.1 Frequency Dependent Capacitance-Voltage Characteristics

Capacitance-voltage (C-V) characteristics of 2nm HfO_2/ 3 nm Al_2O_3/ *n*-$In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor capacitor (MOSCap) structures were measured at 300K and 200K for the small-signal (AC) frequencies ranging from 20 Hz to 1 MHz. C-V measurements that were performed as function of small-signal frequency at 300K are presented in Figure 2.(a). A large dispersion in the measured depletion capacitance of MOSCap structures was observed due to different AC signal frequencies at 300K. The upturn in the measured capacitance within the voltage range of -2V to 0V became more prominent while reducing the applied AC frequency from 1MHz to 20Hz. This behavior is typically observed in $In_{0.53}Ga_{0.47}As$ MOSCap structures and called false inversion [1,2,3,4,5]. The false inversion arises due to increase in the number of interface states that are able to respond applied AC signal and it can be distinguished from the true inversion by considering the voltage dependency of measured capacitance. The capacitance becomes constant in case of true inversion, since the generation of minority carriers at constant test frequency is independent of applied DC gate bias [6,7].

The degree of false inversion depends on both the frequency of AC signal and the position of Fermi level determined by the DC bias at the dielectric/semiconductor

interface. Therefore, the capacitance contribution from interface states that are distributed in energy varies with AC signal for a specific DC bias. In other words, the characteristic time constants of traps becomes longer away from the conduction band edge which means deep traps are not able to follow high AC signal frequencies, even if the Fermi level resides around these deep states. Therefore, deep traps can only contribute the measured capacitance, when DC bias positions the Fermi level around them and AC signal oscillates at sufficiently low frequency. This can be verified by analyzing the false inversion behavior from Figure 2.(a). The false inversion curves broadened to more negative gate biases and measured capacitance increased with the lower AC signal frequencies allow more and deeper interface states with longer time constants to respond. The Figure 2.(b) shows the C-V curves measured as function of small-signal frequency at 200K. The lower measurement temperature significantly suppressed the false inversion observed at 300K. As can be deduced from the suppression of false inversion, the number of interface states are able to respond AC signal decreases dramatically at low temperatures.

The increase in the number of traps responding to lower test frequencies led to larger ΔQ/ΔV ratio that results higher capacitance in depletion. Hence, false inversion capacitance can be correlated to the total number of charges changing occupancy through interface states. The total number of interface states per area can be approximately calculated from the false inversion capacitance measured at 20 Hz. Using the relation of ΔQ= CΔV and using a ΔV test signal amplitude of 50 mV, the number of charges per area for minimum and maximum change in capacitance were calculated as `$\sim 1 \times 10^{8}$

and $\sim 4.2 \times 10^{11} cm^{-2}$, respectively. Dit was estimated from a very simple relation which assumes interface states uniformly distributed around position of the Fermi level at the interface

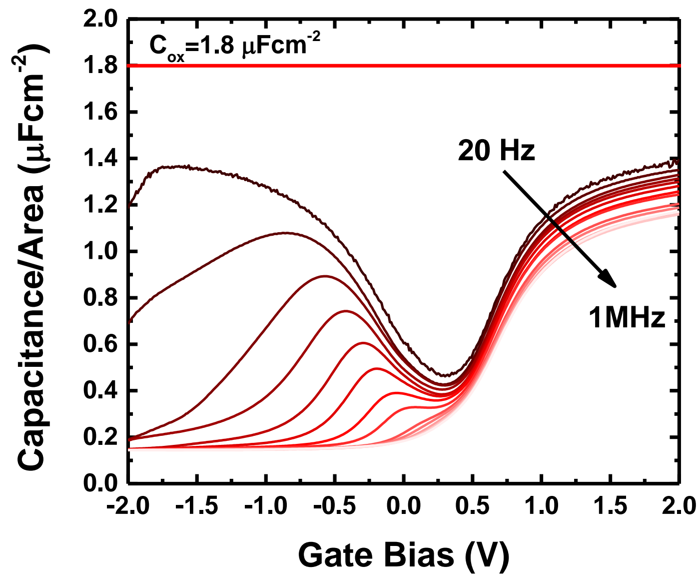
$$D_{it}(q\Phi_{if}) \geq \frac{\Delta Q}{qA\Delta\Phi_{if}} \quad \textbf{(3.1)}$$

where A is the device area, q is the elementary charge, and $q\Delta\Phi_{if}$ is the energy of the Fermi level from the conduction band edge at Al_2O_3/ n-$In_{0.53}Ga_{0.47}As$ interface. Because the $\Delta\Phi_{if}$ is unknown and depends on Fermi level pinning and other factors, the maximum possible value which is 50 mV was used to estimate Dit. A minimum value of Dit was calculated to $\geq 8 \times 10^{12} cm^{-2} eV^{-1}$. However, this calculation only provides a lower limit for actual interface state density due to Fermi level pinning and insufficient modulation of the interface states.

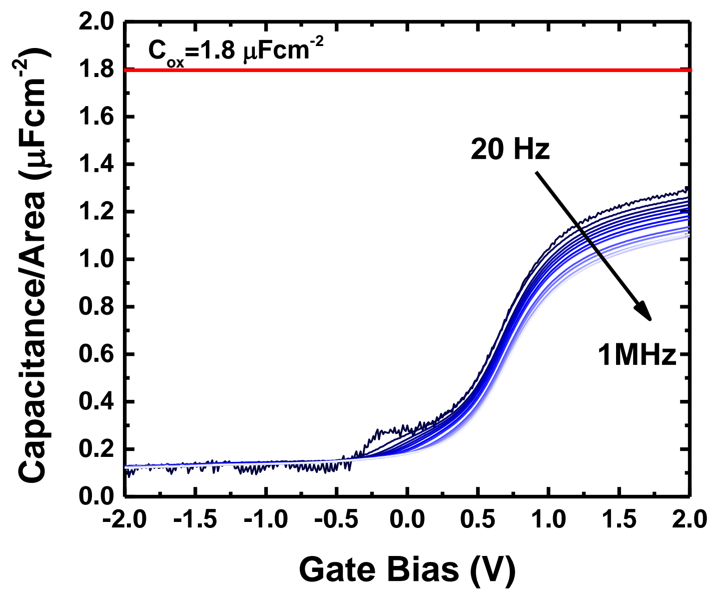
With the false inversion behavior in depletion region explained, we can now turn to investigating accumulation behavior of the MOSCap structures. The measured accumulation capacitance is well below the theoretical oxide capacitance (C_{ox}) which is labeled in Figure 3.1 (a) and (b). The slope in accumulation region is observed due to the low effective conduction band density of states and is called the density of states bottleneck [8,9]. III-V semiconductors have high electron mobility due to small electron effective mass in the Γ-valley of the conduction band that results low effective density of states in the conduction band ($N_C = 2.2 \times 10^{17} cm^{-3}$ at 300K). Therefore, to invert III-V surface and to reach the theoretical C_{ox} value, a gate voltage large enough to move Fermi level deep into the conduction band is required [8].

The other interesting behavior observed in the accumulation region is frequency dispersion. The large frequency dispersion in accumulation is observed for various III-V semiconductors with different dielectrics [1,2,3]. The dispersion behavior observed in the depletion region emerges due to communication of interface states with conduction band at AC signal frequencies comparable to their characteristic emission time constants. However, in accumulation where the Fermi level is located in the conduction band, interface states located around the Fermi level must have very short time constants. Therefore, the response of these interface states shouldn't be responsible of observed frequency dispersion.

From Figure 3.1, the measured accumulation capacitance increases by reducing AC signal frequency at both temperatures. Because, the measurement temperature does not have any effect on the degree of dispersion which means tunneling related process may be responsible of dispersion. A plausible explanation for frequency dispersion in accumulation is border traps which are defined as trap states located in the insulator at a close proximity to the interface [10,11]. The time constants of border traps depend on their distance from the dielectric/semiconductor interface and do not show any temperature dependence since capture and emission processes occur through a tunneling process. However, the presence of these traps are questionable, because similar admittance behavior was observed for different dielectrics deposited by various techniques [1] which would suggest that the type and spatial distribution of these defects are similar for each dielectric material. While this is possible, it is by no means proven.



(a)



(b)

Figure 3. 1: Typically observed frequency dispersion phenomena in III-V MOSCaps (a) C-V characteristics of MOSCap as function of frequency measured at 300K (b) C-V characteristics of MOSCap as function of frequency measured at 200K. False inversion behavior due to interface trap response that was observed at 300K suppressed at 200K suggests thermally activated process such as majority carrier trapping causes this phenomenon

3.2 Conductance Method

Conductance – frequency (G_m-f) measurements were performed under constant gate bias at 300K. The G_P/ω curves were calculated by correcting measured admittance for series resistance (R_s) and oxide capacitance (C_{ox}). First, measured conductance (G_m) and capacitance (C_m) values were corrected for series resistance, since high R_s limits the sensitivity of the method and result erroneous Dit [12]. In order to perform correction, Eq. 3.2.a and 3.2.b given below were used

$$C_c = \frac{(G_m^2 + \omega^2 C_m^2)C_m}{[G_m - (G_m^2 + \omega^2 C_m^2)R_s]^2 + \omega^2 C_m^2} \qquad \textbf{(3.2.a)}$$

$$G_c = \frac{(G_m^2 + \omega^2 C_m^2)[G_m - (G_m^2 + \omega^2 C_m^2)R_s]}{[G_m - (G_m^2 + \omega^2 C_m^2)R_s]^2 + \omega^2 C_m^2} \qquad \textbf{(3.2.b)}$$

and R_s is determined from the accumulation impedance by using Eq. 3.3

$$R_s = \frac{G_{m,a}}{G_{m,a}^2 + \omega^2 C_{m,a}^2} \qquad \textbf{(3.3)}$$

where $G_{m,a}$ and $C_{m,a}$ are measured accumulation conductance and capacitance. The $G_{m,a}$ and $C_{m,a}$ were determined to be $1.21 \times 10^{-4} S$ and $3.68 \times 10^{-10} F$, respectively. These numbers were measured at gate bias of 2V with AC signal frequency of 1MHz. Using Eq. 3.3, calculation yielded value of 22.6 Ω for series resistance. The calculated R_s is very small to induce any significant error on extracted Dit profile [12], yet it was used to correct C_m and G_m to observe the effects on G_P/ω at first hand.

Next, G_P/ω curves were calculated from Eq. 2.65 by using G_c and C_c along with C_{ox}. Prior to presenting the extracted G_P/ω curves the effects of correction for R_s on measured admittance is discussed. Figure 3.2 shows G_P/ω curve for gate bias of -0.1V which is corrected for R_s and C_{ox}. The correcting C_m and G_m for series resistance did not produce any noteworthy change in $(G_P/\omega)_{max}$ and corresponding frequency of peak. We can confidently say that R_s does not introduce any significant error to our calculations, since it is considerably small.

The effect of correction for C_{ox} is shown in Figure 3.3. Instead of using G_m/ω curves in the extraction of Dit, corrected G_P/ω curves must be used due to the fact that C_{ox} shortens the time constant measured across the terminals of the circuits. Indeed, the interface trap branch of the equivalent circuit has longer time constant, since C_{it}/G_P is larger than C_m/G_m [12]. Hence, the G_P/ω curve peaks at a lower frequency and has a higher peak magnitude compared to G_m/ω. From Figure 3.3, the $(G_P/\omega)_{max}$ point is ~3.5 times higher than the $(G_m/\omega)_{max}$ point. This significant increase in the magnitude of the peak is important to note, since extracted Dit directly depends on value of $(G_P/\omega)_{max}$ that can be clearly seen from the Eq. 2.68. In addition, the peak point of curve shifted to lower frequencies slightly which means position of the interface state is actually closer to the conduction band edge. To conclude, using $(G_m/\omega)_{max}$ curves result inaccurate calculation of density of interface states and their distribution in energy.

The C_{ox} can be determined from the strong accumulation capacitance experimentally for SiO_2/Si MOSCap structures. However, the C_{ox} cannot be extracted from the accumulation portion of the C-V curves of high-κ/$In_{0.53}Ga_{0.47}As$ MOSCap

structures, since the total capacitance never reaches to C_{ox} due to the low effective conduction band density of states. Incorrect C_{ox} values lead to inaccurate estimation of G_P/ω and Dit may be overestimated or underestimated. In Figure 3.4, comparison of the G_P/ω curves calculated by using theoretical oxide capacitance and experimentally measured accumulation capacitance are presented. It is evident from the comparison of curves that $(G_P/\omega)_{max}$ increases ~10 times and shifts to lower frequencies.

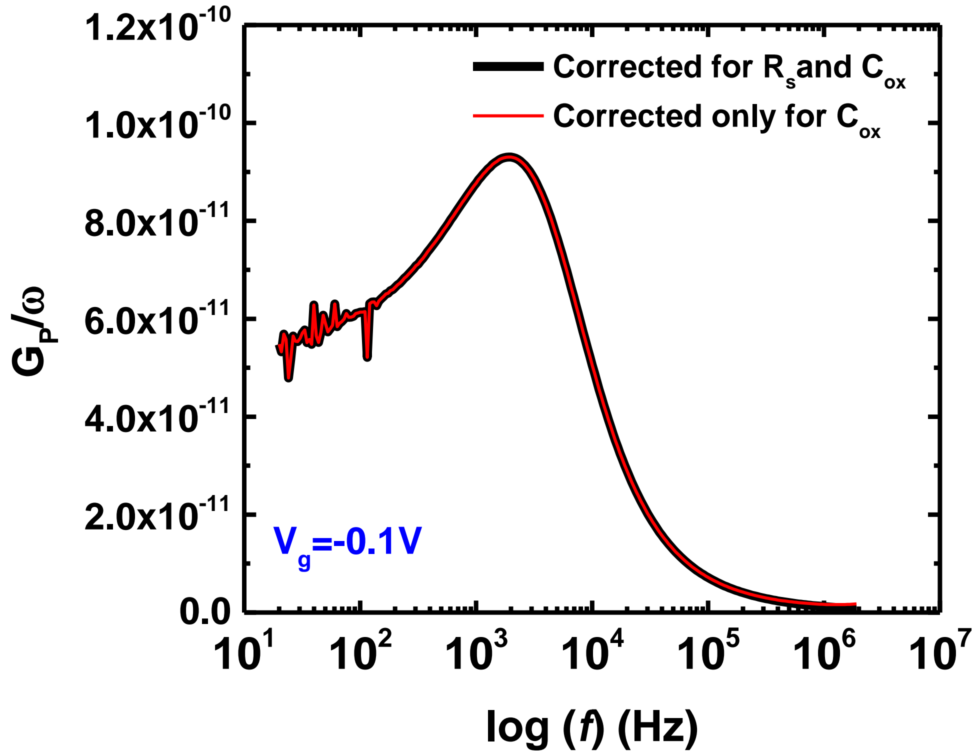


Figure 3. 2: Effect of correction for R_s on the properties of calculated G_P/ω curve measured at -0.1V

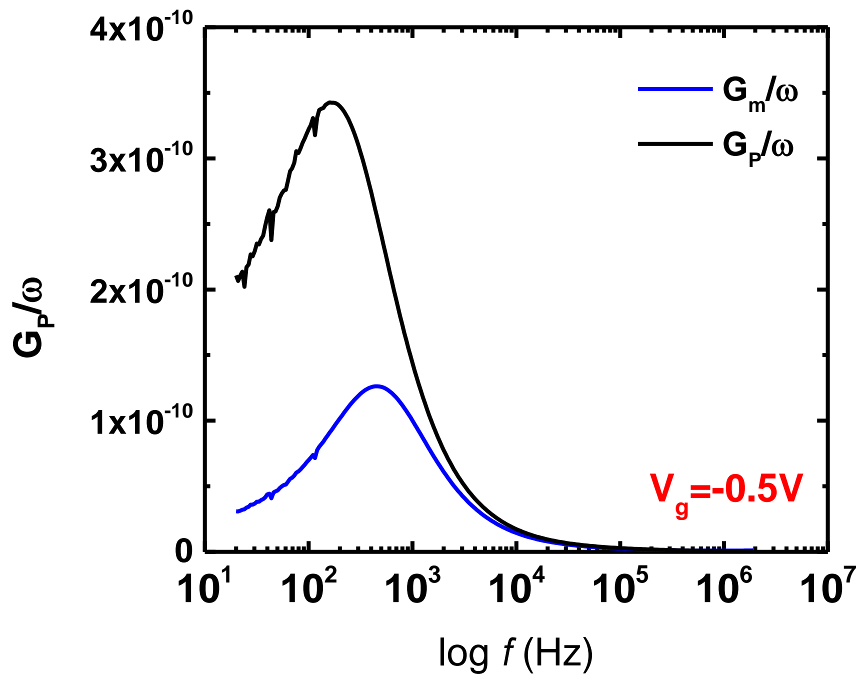


Figure 3. 3: The comparison of G_m/ω (blue) versus G_P/ω (black) curves for gate bias -0.5V

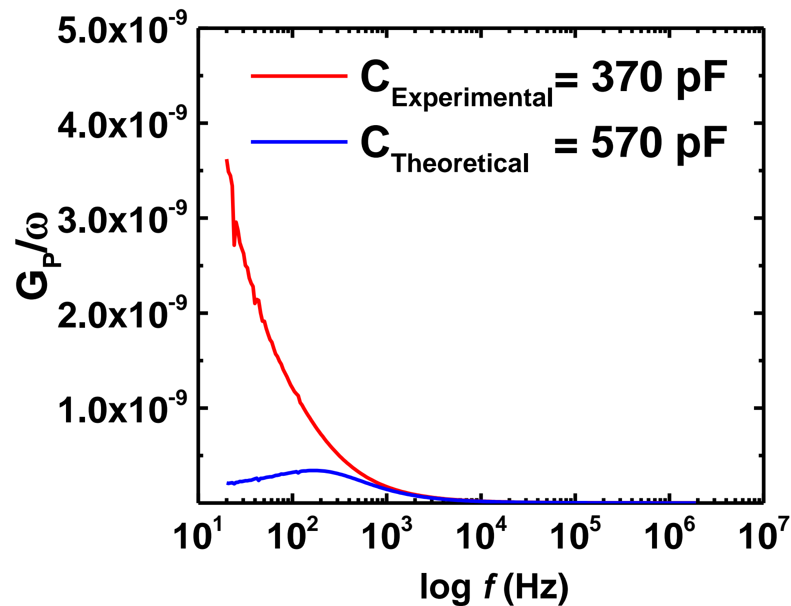


Figure 3. 4: The effect of decrease in the oxide capacitance on the peak height

Figure 3.5 shows the calculated G_P/ω curves from the admittance measurements which were performed as a function of frequency at constant gate bias. $(G_P/\omega)_{max}$ values shift to higher frequencies as the gate bias gets closer to 0V. The shift in $(G_P/\omega)_{max}$ is expected, since each increment of the gate bias moves the Fermi level toward the conduction band edge at the interface. The closer the Fermi level to the conduction band edge, the loss through interface states with shorter time constants dominates and G_P/ω peaks at higher frequencies. Therefore, the shift of $(G_P/\omega)_{max}$ in frequency is the characteristic outcome for measuring the admittance of interface states distributed throughout the semiconductor band gap.

From Figure 3.5, the G_P/ω curves exhibit strong asymmetry about $(G_P/\omega)_{max}$. The asymmetry is indicative of rapid variation of Dit within a potential range equal to the several standard deviation of band bending σ_s. The σ_s is the measure of the width of the G_P/ω curve which is measured at a constant gate bias. The exact determination of σ_s for $Al_2O_3/In_{0.53}Ga_{0.47}As$ interfaces requires statistical analysis of band bending variation which is beyond the scope of this study. However, the effect of asymmetrical behavior can be evaluated by considering $(\overline{G_P}/\omega)/(\overline{G_P}/\omega)_{f_P}$ versus σ_s relationship given in Figure 2.10. The plot was obtained based on admittance measurements on SiO_2/Si MOSCap structures. Essentially, the plot shows that for σ_s values below the 1.8 (in units of kT/q), high and low frequency ratios differ from each other which means G_P/ω curves becomes asymmetrical. Therefore, it is reasonable to expect small band bending deviations due to observed strong asymmetrical behavior in our G_P/ω curves. This may

cause underestimation of calculated Dit from the Eq. 2.68, since it is valid for only $\sigma_s >$ 1.8 kT/q where low and high frequency ratios become equal.

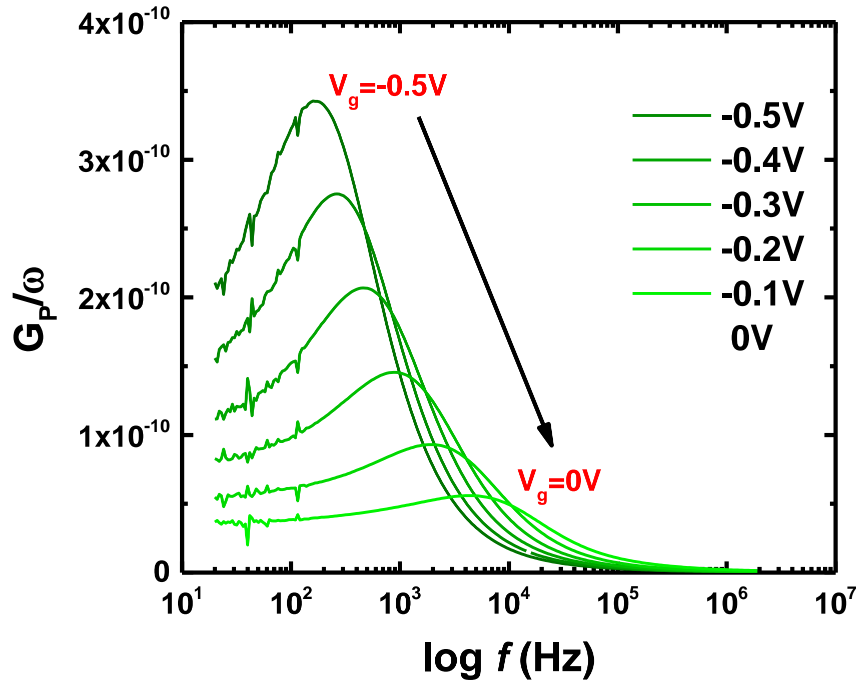


Figure 3. 5: The calculated G_P/ω versus log f curves from G_m measured at constant gate biases ranging from 0V to -0.5V

Next, Dit and energy distribution of states in the band gap were calculated from $(G_P/\omega)_{max}$ values and from corresponding characteristic frequencies by using Eq. 2.68 and Eq. 2.29, respectively. The Dit versus E_C-E_T is plotted in Figure 3.6 and provides the distribution of interface states within the accessible band gap range at 300K. The Dit peaks at ~1.75×10^{13} $cm^{-2}eV^{-1}$ at the mid-gap. Interface state distribution with similar

shape around the midgap was previously reported from conductance method and such peak was originated to high concentration of intrinsic mid-gap interface states [1]. However, accurate determination of the σ_s for each G_P/ω curve at different bias and calculation of individual $f_D(\sigma_s)$ values may alter the shape of interface state distribution.

The admittance measurements were performed at 200K, yet obtained data were not qualified to quantify Dit closer to the conduction band. The calculated G_P/ω curves did not peak at a characteristic frequency which makes impossible to extract any information on interface states.

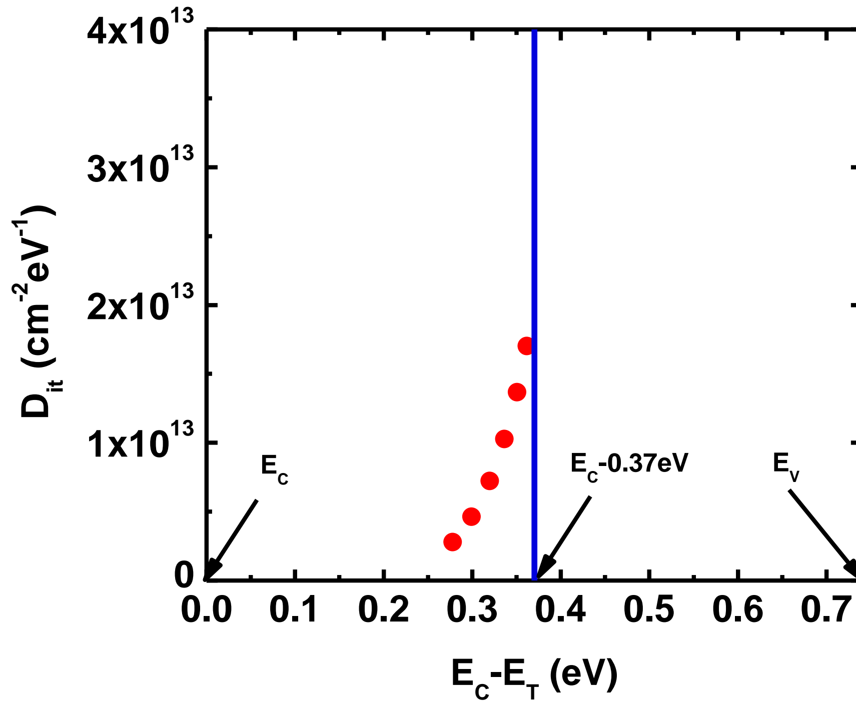


Figure 3. 6: 2nm HfO_2/ 3 nm Al_2O_3/ n-$In_{0.53}Ga_{0.47}As$ MOSCap interface state distribution determined from the G_P/ω curves

3.3 Low Temperature Capacitance-Voltage (LT-CV) Method

As described in chapter 2, the LT-CV method uses high AC signal frequency and low measurement temperature to prevent any carrier emission from interface states and Dit spectrum is obtained from the steady state capacitance. At high AC signal frequencies, $C_{it}(\omega)$ becomes zero and the equivalent circuit of MOSCap reduces to series combination of oxide capacitance (C_{ox}) and semiconductor capacitance (C_s). However, the slowly varying DC bias allows the interface states to capture carriers during the voltage sweep from depletion to accumulation. Following the slow C-V, performing another high frequency C-V with fast DC bias sweeping rate obstructs the emission of captured carriers from the interface states. As a consequence, these captured carriers placed extra charge on the gate that induced change in the depletion layer charge. The difference in depletion layer charge led to shift in the applied gate bias for a given surface potential (i.e. constant capacitance). This can be understood easily from the gate bias relationship for MOSCap

$$V_G = V_{FB} + \varphi_s - \frac{Q_s}{C_{ox}} \qquad \textbf{(3.5)}$$

where V_{FB} is flatband voltage, φ_s surface potential and Q_s total semiconductor charge. It is explicit that the gate bias is altered by any change in the Q_s for a given surface potential. Therefore, the difference in the applied gate bias at a constant surface potential is directly associated with interface state density.

Figure 3.7.(a) presents the high frequency slow C-V and fast C-V curves that were measured at 77K, along with the calculated ideal C-V curve which was obtained by

taking into account variations in the material parameters at 77K. In reference [13], the detailed explanation is given about calculation of ideal C-V curve. The occupancy of the interface states changes as a response to slowly varying gate bias. This causes distortion in the shape of the slow C-V curve and it stretched out along the voltage axis compared to fast and ideal C-V curves.

The fast C-V curve has a higher slope than the slow C-V curve due to limited change in the occupancy of interface states. The slope difference between the fast C-V and calculated ideal C-V curves is evident. This difference is the result of carrier emission from shallow states located in a close proximity to the conduction band edge and it cannot be avoided at 77K. The emission from interface states can be limited very near to band edges, if the measurement temperature lowered down further.

The theoretical depletion capacitance couldn't be attained during the slow C-V measurement which points out insufficient band bending due to high Dit. However, the depletion capacitance measured during the fast C-V dropped below the theoretical value between the voltage range of -0.3V to -1.5V. This is most likely due to the traps are not able to respond either the AC signal or DC sweep. Therefore, the MOSCaps cannot preserve the thermal equilibrium conditions and deep depletion behavior was observed [13]. Figure 3.7.(b) shows extracted Dit spectra using Eq. 2.49 and Eq.2.50 by comparing the slow C-V with fast and calculated ideal C-V curves. The Dit spectrum obtained from the comparison of slow and fast C-V curves labeled as experimental spectrum, where the other is labeled as theoretical spectrum. Both Dit spectra show

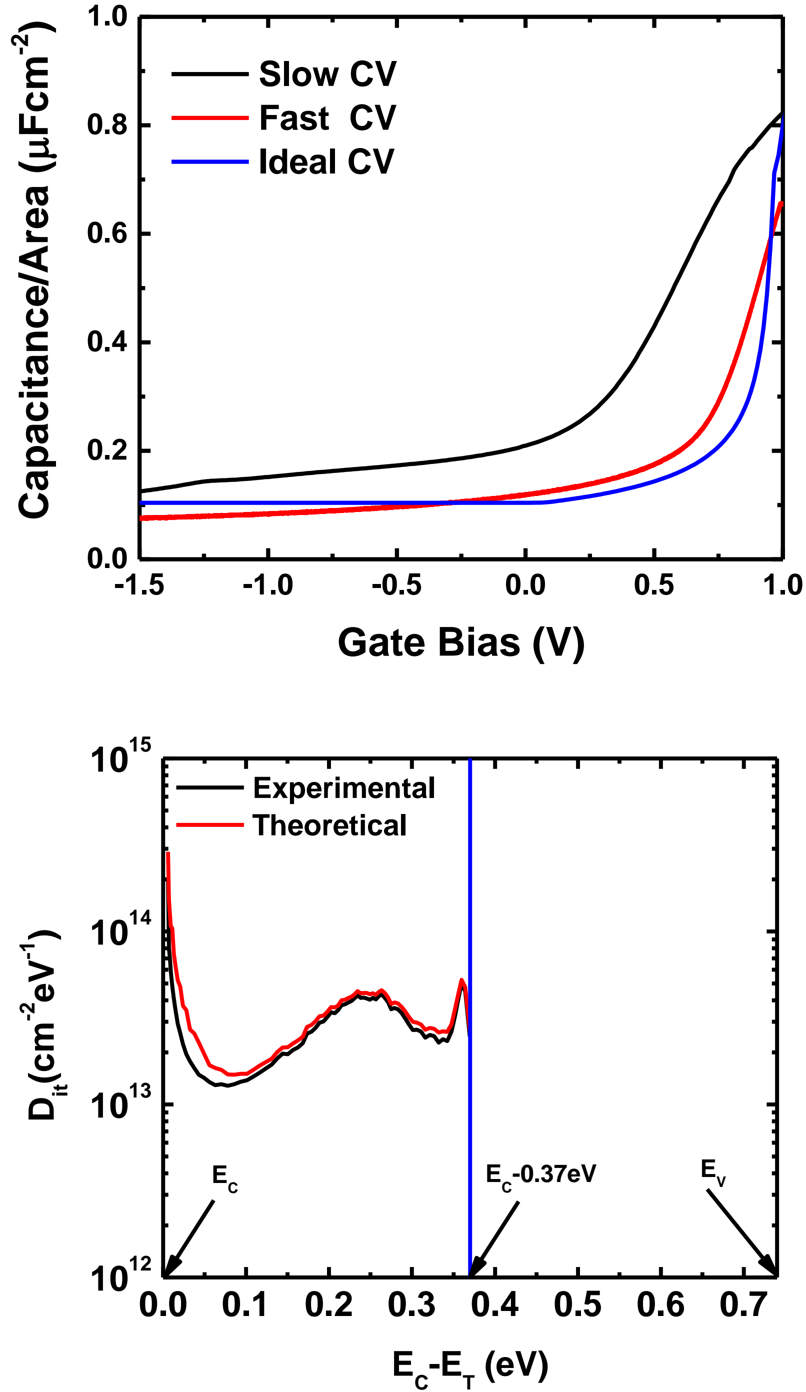


Figure 3. 7: (a) Comparison of slow, fast and ideal C-V curves. (b) Comparison of Dit distributions extracted experimentally and theoretically for 2nm HfO_2/ 3 nm Al_2O_3/ n-$In_{0.53}Ga_{0.47}As$ MOSCap structures

non-uniform distribution of interface states and provide average Dit of $\sim 3 \times 10^{13} cm^{-2} eV^{-1}$above the mid-gap. The interface state density from the theoretical spectrum is slightly higher than interface state density from the experimental spectrum within the range of 0.1eV below the conduction band. Moreover, the difference in Dit increases towards to conduction band edge which indicates electron emission from shallow states cannot be avoided during the fast C-V measurement.

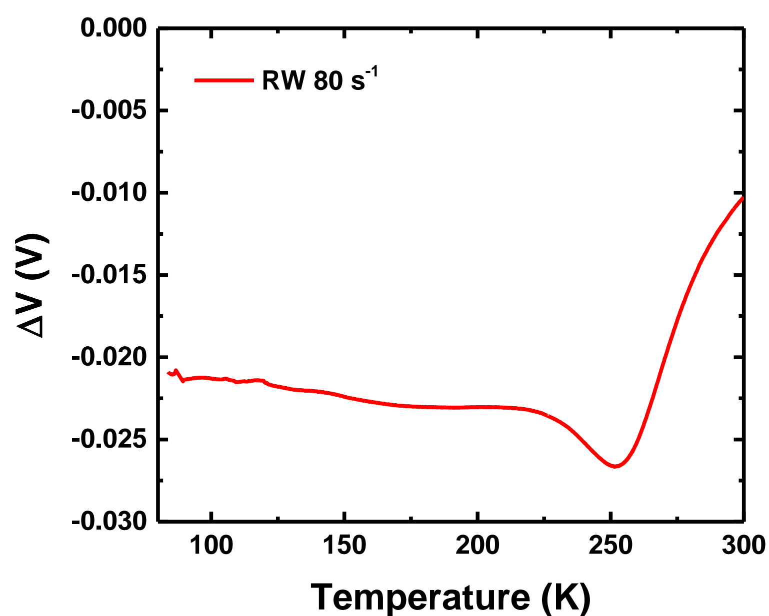
To conclude, experimental and theoretical Dit spectra agrees quite well which indicates the fast C-V measurements can be considered approximate to the calculated ideal C-V curves.

3.4 Constant Capacitance Deep Level Transient Spectroscopy

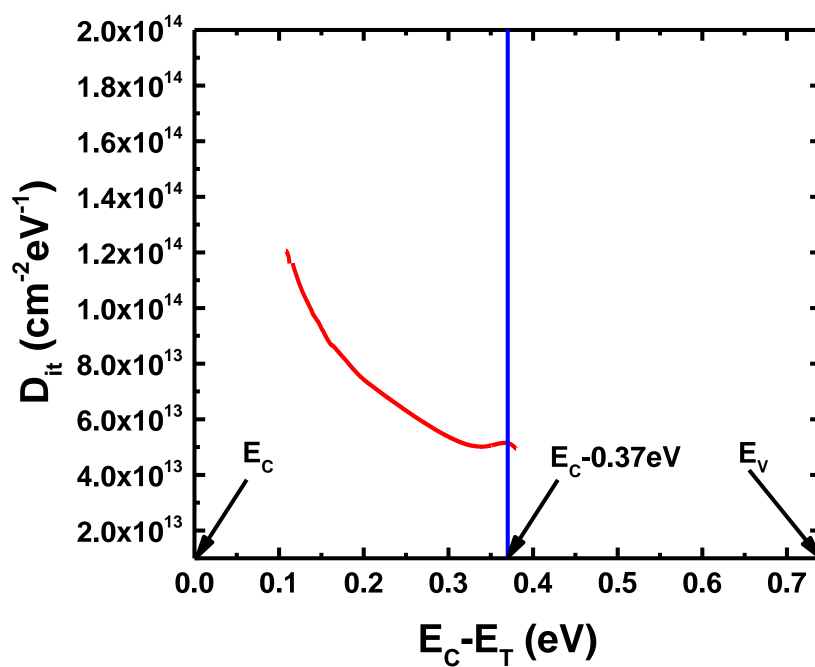
The constant capacitance deep level transient spectroscopy measurements (CC-DLTS) were performed on the HfO_2 /Al_2O_3 /n – $In_{0,53}Ga_{0,47}As$ MOSCap structures to quantify Dit. The CC-DLTS technique is suitable for accurate determination of high concentrations of interface states due to minimum signal distortion. Moreover, CC-DLTS offers high energy resolution, since the large numbers of voltage transients are measured over a wide range of temperature by using small increments in temperature. Another important feature of the CC-DLTS is that the device is pulsed repeatedly into accumulation in a single measurement cycle at constant temperature. This improves the signal-to-noise ratio, since all interface states are in their prime condition. Therefore, CC-DLTS is able to characterize Dit more accurately compared to LT-CV method which essentially depends on single C-V scan.

The distribution of interface states above the mid-gap was characterized by pulsing the MOSCap structures into strong accumulation by applying filling pulse of 1.9V for 10 ms and then measuring the voltage transients maintaining moderate depletion (with Fermi level deep in the bandgap) as interface states emitting captured majority carriers. This procedure is repeated as the temperature increased gradually from 77 to 300K.

Figure 3.8.(a) shows the raw CC-DLTS spectrum for the HfO_2 /Al_2O_3 /n – $In_{0,53}Ga_{0,47}As$ MOSCap structure. Smooth variation of ΔV signal up to 225K and a prominent peak at 250K observed from the CC-DLTS spectrum. The position of the peak in energy corresponds to midgap of the n-$In_{0,53}Ga_{0,47}As$ where the majority carrier emission from interface states no longer dominates the ΔV signal. In the vicinity of midgap energies, minority carrier emission becomes a competitive process and contributes to ΔV signal through surface generation. Such peaks were observed by Johnson et. al in CC-DLTS spectra of MOS capacitors on p-type silicon and it was concluded that these peaks arises from minority carrier contribution, since the peak position and shape showed dependency on the applied depletion bias. Bulk traps may contribute the CC-DLTS signal during the measurement and cause peaks in the spectrum. However, in literature there is no reported bulk state level for MBE grown n-$In_{0,53}Ga_{0,47}As$ in a close proximity to midgap energies. Figure 3.8.(b) presents the Dit distribution above the midgap. The concentration of interface states plotted in the linear scale to emphasize the shape of spectrum. Dit spectrum was obtained by using Eq. 2.44



(a)



(b)

Figure 3. 8: (a) CC-DLTS spectrum for rate window of 80s^{-1} from 77K to 300K (b) Dit distribution above the midgap plotted in linear scale to emphasize the shape of distribution

and Eq. 2.48. A capture cross section value of $1 \times 10^{-16} cm^2$was used in the calculations based on the values from the literature [1]. Dit does not have any dependence on capture cross section, but the calculated energy position of interface states is affected. However, capture cross section dependency of the extracted trap energies is quite minor. Quantitatively, three orders of magnitude change in capture cross section value introduces only ~0.05 eV ambiguity in calculated energy.

As seen in spectra, the Dit increases gradually from concentration of $5 \times 10^{13} cm^{-2} eV^{-1}$ around the midgap to concentration of $1.2 \times 10^{14} cm^{-2} eV^{-1}$ towards edge of the conduction band. The distribution of interface states at high-κ/III-V semiconductor interfaces was proposed to have U shape which means high Dit near the conduction and valance band edges and lower concentrations around the midgap. The shape of Dit distribution at the Al_2O_3/*n*-$In_{0,53}Ga_{0,47}As$ interface have the properties of proposed distribution[14,15]. However, it should be noted that in order to confirm the U shaped distribution throughout the entire bandgap, CC-DLTS measurements need to be performed on Al_2O_3/*p*-$In_{0,53}Ga_{0,47}As$ interface.

3.5 Comparison of Dit Spectra

In this subsection, Dit spectra from CC-DLTS, LTCV and conductance methods were compared and discrepancies among the reported spectra discussed. Figure 3.9 shows the Dit spectra obtained from all three methods. CC-DLTS provided smoothly varying distribution of interface states in the upper half of the bandgap. Dit spectrum from the LTCV has many features within the energy range compared to CC-DLTS, but

provided comparable concentrations of interface state density. Room temperature conductance measurements yielded a Dit spectrum which peaks towards the mid-gap. The Dit profile from conductance measurements decreases from $\sim 1 \times 10^{13}$ to $\sim 2 \times 10^{12} cm^{-2} eV^{-1}$ within the energy range of 0.1eV. Additionally, extracted Dit is almost two orders of magnitude lower compared to results from CC-DLTS and LTCV at E_C-0.27 eV.

The inconsistency between the Dit spectra from each technique can be elucidated by considering strengths and weaknesses of each technique. As indicated in the previous subsection, CC-DLTS method has several advantages over the LT-CV and conductance methods. CC-DLTS measurement is performed by maintaining constant depletion capacitance and so constant depletion width throughout the transient response. Therefore, the position of Fermi level remains constant at the interface during the transient response. This is achieved by using a feedback circuitry which adjusts applied gate bias simultaneously. Therefore, a constant surface potential is conserved during the carrier emission from interface states. This ensures that the measured signal is only the result of carrier emission and makes immune the CC-DLTS to any error which may emerge from band bending fluctuations due to charge non-uniformities at the interface. Such non-uniformities leads to broad and asymmetrical G_P/ω curves calculated from the measured room temperature admittance of the device. The non-equipotential nature of the interface causes fluctuations in band bending which changes the position of the Fermi level at the interface and emission and capture processes occur in a broader energy range [16,17].

This effect should be taken into account during the extraction of Dit by using the appropriate $f_D(\sigma_s)$ coefficient; otherwise conductance method will underestimate Dit.

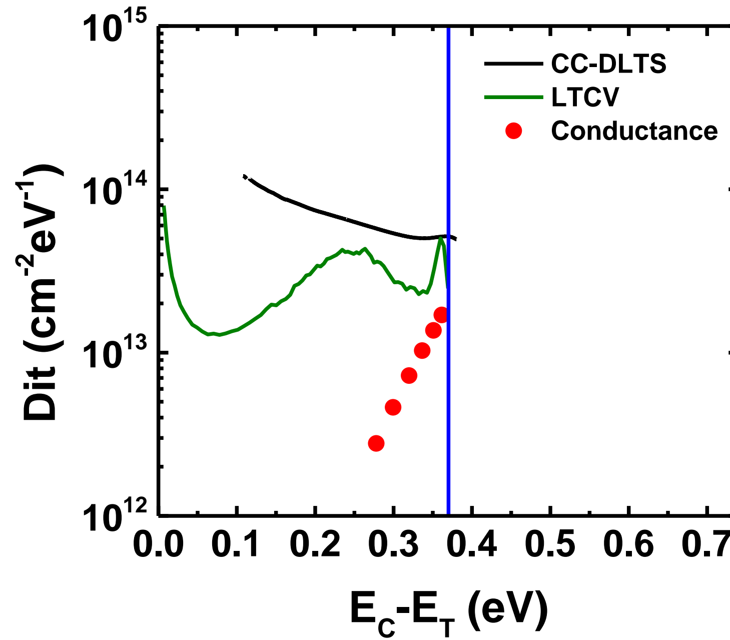


Figure 3. 9: Comparison of Dit spectra from CC-DLTS, LTCV and conductance method

Another advantage of CC-DLTS method arises from the multiple pulsing of the device into accumulation in a single measurement cycle at constant temperature. In a single loop of CC-DLTS measurement, filling pulse is applied repeatedly to obtain transients for specified rate windows. For example, in order to obtain rate window of 80 s^{-1}, the device is pulsed into strong accumulation for 20 times and the transient is measured for a certain time range. This repetitive pulsing process ensures the all interface states are filled before measuring transients. The interface states are always saturated with carriers before each transient measurement and thus, CC-DLTS signal contains the

complete information on the concentration of interface states. The combination of repetitive pulsing process with temperature scanning provides accurate and reliable determination of interface states. The CC-DLTS yielded Dit which varies from low-10^{14} to mid-10^{13} $cm^{-2}eV^{-1}$ within 0.1eV to 0.37eV. In order to obtain concentration of interface states below the 0.1eV, the temperature scan should be started from a point below the 77K.

The LT-CV method was able to provide analogous concentrations of interface states with CC-DLTS towards the mid-gap. However, the difference in Dit is on the order of a magnitude around 0.1eV. Additionally, the distribution profile of interface states shows many features compared to gradual variation in Dit spectrum from CC-DLTS. The LT-CV measurement was performed by using AC signal with 1MHz frequency which was likely insufficient to suppress frequency dependent contribution from the interface states located closely to the conduction band edge. The Dit was underestimated, because the true high frequency capacitance behavior couldn't be achieved even at low temperature. The Dit profile from LT-CV has many features that are considered to be artifacts from the analysis. There is a non-uniform variation in ΔV_G at different surface potentials. In other words, a constant amount of change in surface potential does not result the same amount of variation in ΔV_G. These variations intensified due to differentiation of ΔV_G respect to surface potential which is directly used in the calculation of Dit.

The CC-DLTS is superior to both LT-CV and conductance and able to determine Dit accurately. The conductance method grossly underestimates Dit and the spectrum has

very strong energy dependency. LT-CV measurement suffers from not achieving true high frequency C-V behavior. The distribution profile is also inconsistent with profile from CC-DLTS due to artifacts from analysis.

3.6 References

[1] Y. Hwang, R. Engel-Herbert, N. G. Rudawski, and S. Stemmer, “Analaysis of trap state densities at $HfO_2/In_{0.53}Ga_{0.47}As$ Interfaces”, *Appl. Phys. Lett.*, vol. 96, 102910, 2010

[2] R. Suzuki, N. Taoka, M. Yokoyama, S. Lee, S.H. Kim et al., “1-nm-capacitance-equivalent-thickness HfO_2/Al_2O_3/InGaAs metal-oxidesemiconductor structure with low interface trap density and low gate leakage current density”, *Appl. Phys. Lett.*, vol. 100, 132906, 2012

[3] G. Brammertz, H.C. Lin, K. Martens, A.R. Alian, C. Merckling, J. Peanaud et al., “Electrical properties of III-V interfaces”, *ECS Trans.*, vol. 19, pp. 375-386, 2009

[4] R.D. Long, B. Shin, S. Monaghan, K. Cherkaoui, J. Cagnon, S. Stemmer, P.C. McIntyre, and P.K. Hurley, “Charged defect quantification in $Pt/Al_2O_3/In_{0.53}Ga_{0.47}As/InP$ MOS capacitors”, *J. Electrochem. Soc.*, vol. 158, pp. 103-107, 2011

[5] G. Brammertz, H.C. Lin, M. Caymax, M. Meuris, M. Heyns et al., “On the interface state density at $In_{0.53}Ga_{0.47}As$/oxide interfaces”, *Appl. Phys. Lett.*, vol. 95, 202109, 2009

[6] K.Martens, W.F. Wang, A. Dimoulas, G. Borghs, M. Meuris, G. Groeseneken, and H. E. Maes., “Determining weak Fermi level pinning in MOS devices by conductance and capacitance analysis and application to GaAs MOS devices”, *Solid-State Electron.*, vol. 51, pp. 1101-1108, 2007

[7] K.Martens, W.Wang, K.D. Keersmaecker, G. Borghs, G. Groeseneken, H. Maes, “Impact of weak Fermi-level pinning on the correct interpretation of III-V MOS C-V and G-V characteristics”, *Microelectron. Eng.*, vol. 84, pp. 2146-2149, 2007

[8] E. Lind, Y.M. Niquet, H. Mera, and L.E. Wemersson, “Accumulation capacitance of narrow band gap metal-oxide-semiconductor capacitors”, *Appl. Phys. Lett.*, vol. 96, 233507, 2010

[9] T. P. O’Regan, and P.K. Hurley, “ Calculation of the capacitance-voltage characteristics of GaAs, $In_{0.53}Ga_{0.47}As$, and InAs metal-oxide-semiconductor structures”, *Appl. Phys. Lett.*, vol. 99, 163502, 2011

[10] E.J. Kim, L.Wang, P.M. Asbeck, K.C. Saraswat, and P.C. McIntyre, “Border traps in $Al_2O_3/In_{0.53}Ga_{0.47}As$ (100) gate stacks and their passivation by hydrogen anneals”, *Appl. Phys. Lett.*, vol. 96, 012906, 2010.

[11]Y.Yuan, L. Wang, B. Yu, B. Shin, J. Ahn, P.C. McIntyre, P.M. Asbeck, M. J. W. Rodwell, and Y. Taur, “ A distributed model for border traps Al_2O_3-InGaAs MOS devices” *IEEE Electron Device Lett.*, vol.32, no.4, pp. 485-487, 2011

[12] E.H. Nicollian, and A. Goetzberger, “The Si-SiO_2 interface-electrical properties as determined by the metal-insulator-silicon conductance technique” *Bell Syst. Tech. J.*, vol. 46, no.6, pp.1055-1133, 1967

[13] R. Engel-Herbert, Y. Hwang, and S. Stemmer, “Comparison of methods to quantify interface trap densities at dielectric/III-V semiconductor interfaces” *J. Appl. Phys.*, vol. 50, 121101, December 2010.

[14] H. Hasegawa, and H. Ohno, “Unified disorder induced gap state model for insulator-semiconductor and metal-semiconductor interfaces”, *J. Vac. Sci. Technol.*, vol. B4, 1130, 1986.

[15] W.E. Spicer, I. Lindau, P. Skeath, and C.Y. Su, “Unified defect model and beyond”, *J. Vac. Sci. Technol.*, vol.17, 1019, 1980

[16] H. Deuling, E. Klausmann, and A. Goetzberger, “Interface states in Si-SiO_2 interfaces”, *Solid-State Electron.*, vol. 15, pp. 559-571, 1972.

[17] K. Lehovec, “Frequency dependence of the impedance of distributed surface states in MOS structures”, *Appl. Phys. Lett.*, vol. 8, no. 2, pp. 48-50, Jan 1966.

CHAPTER 4: CONCLUSIONS AND FUTURE CONSIDERATIONS

4.1 Conclusions

This research aimed to compare different interface state characterization techniques by quantifying Dit at the high-κ/$In_{0.53}Ga_{0.47}As$ interface. The obtained Dit profiles were compared and the reasons of inconsistency observed among the results were investigated by considering the physics behind the each technique. In summary:

- The average interface state density was estimated to be $\geq 8 \times 10^{12} cm^{-2} eV^{-1}$ from the false inversion behavior observed in frequency dependent C-V measurements performed at 300K.
- CC-DLTS was proved to be accurate technique that can be used in quantitative characterization of high-κ/III-V interfaces. It is suitable for measuring high concentrations of interface states with high energy resolution. Dit profile from CC-DLTS in upper half of the band gap is in good agreement with the proposed U-shaped interface state distribution for dielectric/III-V interfaces.
- LT-CV was used as independent means of verifying interface spectra obtained from CC-DLTS which relies on measuring temperature

dependent voltage transients at a constant surface potential. Unlike the CC-DLTS, the LT-CV method is the low temperature single scan Terman method which eliminates the necessity using theoretical ideal C-V curve in Dit extraction.

- The CC-DLTS and LT-CV revealed consistent interface state densities with each other in the mid-high 10^{13} $cm^{-2}eV^{-1}$ range. However, Dit profile obtained from LT-CV method was inherently noisier due to the nature of Terman analysis.
- The conductance method severely underestimates Dit and it is proved to be not suitable for accurate characterization of interfaces where the Dit rapidly varies over a few kT/q ranges. The difference in concentration and distribution of interface states compared to CC-DLTS and LTCV suggests that the method is not appropriate to use in the case of moderate to large values of Dit.

4.2 Future Considerations

This work in this thesis provides a critical comparison on interface spectroscopy techniques that depends on distinct carrier modulation mechanisms to quantify Dit. Although this study has laid a foundation for accurate characterization of high-κ/III-V interfaces, there are number of nuances that are required to be investigated in-depth. More focused investigation on these issues can help to refining the techniques and lead to better understanding of the outcomes of experiments.

One important point needs to be explored more thoroughly is the peak that observed in the CC-DLTS measurement around the 250K. The peak may be correlated to bulk trap contribution to CC-DLTS signal, however there is no solid evidence to prove it. Therefore, bulk trap studies must be performed on MBE grown Si doped *n*-$In_{0.53}Ga_{0.47}As$/InP structures to profile the bulk states. This study should help to distinguish contribution from interface and bulk states which leads more accurate Dit profiling. In addition to bulk state studies, the effect of competition between carrier capture-emission processes should be studied, if this can lead to any artificial peaks in CC-DLTS spectra.

Another nuance is the asymmetrical behavior observed in G_P/ω curves which is indicative of rapid variation in Dit. The rapid variation in Dit within the modulation range of AC signal (25mV) is responsible of asymmetrical behavior. The effect of magnitude of AC signal on symmetry of the calculated G_P/ω curves must be studied. This study may provide information on optimum AC signal magnitude that needs to be used for conductance method.

BIBLIOGRAPHY

A. D. Carter, W.J. Mitchell, B.J. Thibeault, J.J.M. Law, and M.J.W. Rodwell, “Al_2O_3 growth on (100) $In_{0.53}Ga_{0.47}As$ initiated by cyclic trimethylaluminum and hydrogen plasma exposures”, *Appl. Phys. Exp.*, vol. 4, 091102, 2011.

C. Adelman, D. Lin, L. Nyns, B. Schepers, A. Delabie, S. Van Elshocht, M. Caymax, “Atomic layer deposited tantalum silicate as gate dielectric for III-V MOS devices”, *Microelectron. Eng.*, vol. 88, pp. 1098-1100, 2011.

C. H. Jan, “CMOS technology scaling for system-on-chip integration-past, present and future”, *ECS Trans.*, vol.44, pp 451-470, 2012.

C. L. Hinkle, A.M. Sonnet, E.M. Vogel, S. McDonnell, G.J. Hughes et al. “GaAs interfacial self-cleaning by atomic layer deposition”, *Appl. Phys. Lett.*, vol. 92, 071901, 2008.

C. N. Berglund, “Surface states at steam-grown silicon-silicon dioxide interfaces”, *IEEE Trans. Electron Devices*, vol.13, no.10, 1966.
carriers and electron states. San Diego:Academic Press, 1992.

D. J. Frank, R.H. Dennard, E. Nowak, P.M. Solomon, Y. Taur, and H.S.P. Wong, “Device scaling limits of Si MOSFETs and their application dependencies”, *Proceedings of the IEEE*, vol. 89, no. 3, pp. 260-288, 2001.

D. K. Schroder, *Semiconductor material and device characterization*. New York: Wiley, 1990.

D. V. Lang, “Deep level transient spectroscopy: a new method to characterize traps in semiconductors,” *J. Appl. Phys.,* vol. 45, pp. 3023-3032, 1974.

D. Zade, K. Kakushima, T. Kanda, Y.C. Lin, P. Ahmet, K. Tsutsui, A. Nishiyama, N. Sugii,

E.Y. Chang, K. Natori, T. Hattori, H. Iwai, “Improving electrical characteristics of $W/HfO_2/In_{0.53}Ga_{0.47}As$ gate stacks by altering deposition techniques” *Microelectron. Eng.*, vol. 88, pp. 1109-1112, 2011.

E. H. Nicollian and J. R. Brews, *MOS (metal oxide semiconductor) physics and technology*. New York: Wiley, 1982.

E. H. Nicollian, A. Goetzberger, and A.D. Lopez "Expedient method of obtaining interface state properties from MIS conductance measurements", *Solid-State Electron.*, vol. 12, pp. 937-944, 1969.

E. H. Nicollian, and A. Goetzberger, "The Si-SiO_2 interface-electrical properties as determined by the metal-insulator-silicon conductance technique" *Bell Syst. Tech. J.*, vol. 46, no.6, pp.1055-1133, 1967

E. J. Kim, E. Chagarov, J. Cagnon, Y. Yuan, A.C. Kummel et al. , "Atomically abrupt and unpinned $Al_2O_3/In_{0.53}Ga_{0.47}As$ interfaces:Experiment and simulation" *J. Appl. Phys.*, vol. 106, 124508, 2009.

E. J. Kim, L.Wang, P.M. Asbeck, K.C. Saraswat, and P.C. McIntyre, "Border traps in $Al_2O_3/In_{0.53}Ga_{0.47}As$ (100) gate stacks and their passivation by hydrogen anneals", *Appl. Phys. Lett.*, vol. 96, 012906, 2010.

E. Lind, Y.M. Niquet, H. Mera, and L.E. Wemersson, "Accumulation capacitance of narrow band gap metal-oxide-semiconductor capacitors", *Appl. Phys. Lett.*, vol. 96, 233507, 2010

E. O'Connor, B. Brennan, V. Djara, K. Cherkaoui, S. Monaghan et al., "A systematic study
of $(NH_4)_2S$ passivation (22%, 10%, 5%, or 1%) on the interface properties of the $Al_2O_3/In_{0.53}Ga_{0.47}As$/InP system for n-type and p-type $In_{0.53}Ga_{0.47}As$ epitaxial layers", *J. Appl. Phys.*, vol. 109, 024101, 2011.

E. O'Connor, S. Monaghan, K. Cherkaoui, I.M. Povey, and P.K. Hurley, "Analysis of the minority carrier response of n-type and p-type Au/Ni/$Al_2O_3/In_{0.53}Ga_{0.47}As$/InP capacitors following an optimized $(NH_4)_2S$ treatment", *Appl. Phys. Lett.*, vol. 99, 212901, 2011

F. Ren, M. Hong, V.S. Hobson, J.M. Kuo, J.R. Lothian, J.P. Mannaerts, J. Kwo, S.G. Chu, Y.K. Chen, and A.Y. Cho, "Demonstration of enhancement-mode p- and n-channel GaAs MOSFETs with $Ga_2O_3(Gd_2O_3)$ as gate oxide" , *Solid-State Electron.*, vol.41, pp. 1751-1753, 1997.

G. Brammertz, H.C. Lin, K. Martens, A.R. Alian, C. Merckling, J. Peanaud et al., "Electrical properties of III-V interfaces", *ECS Trans.*, vol. 19, pp. 375-386, 2009

G. Brammertz, H.C. Lin, M. Caymax, M. Meuris, M. Heyns et al., "On the interface state density at $In_{0.53}Ga_{0.47}As$/oxide interfaces", *Appl. Phys. Lett.*, vol. 95, 202109, 2009

H. Deuling, E. Klausmann, and A. Goetzberger, "Interface states in Si-SiO_2 interfaces", *Solid-State Electron.*, vol. 15, pp. 559-571, 1972.

H. Hasegawa, and H. Ohno, "Unified disorder induced gap state model for insulator-semiconductor and metal-semiconductor interfaces", *J. Vac. Sci. Technol.*, vol. B4, 1130, 1986.

H. Ishii, N. Miyata, Y. Urabe, T. Itatani, T. Yasuda et al., "High electron mobility metal-insulator-semiconductor field-effect transistors fabricated on (111)-oriented InGaAs channels", *Appl. Phys. Exp*., vol. 2, 121101, 2009.

H.C. Lin, G. Brammertz, K. Martens, G. de Valicourt, and L. Negre et al., "The Fermi-level efficiency method and its applications on high interface trap density oxide-semiconductor interfaces", *Appl. Phys. Lett.*, vol. 94, 153508, 2009.

http://www.itrs.net/Links/2011ITRS/Home2011.htm

I.Thayne, X. Li, W. Jansen, I. Povey, E. O'Connor, M. Pemble, P. Hurley, J. Ahn, P. McIntyre, "III-V MOSFETs for sub-15 nm technology generation CMOS: some observations, Issues and Solutions", *CS MANTECH Conference Proceedings*, 2012.

J. A. del Alamo, "Nanometer-scale electronics with III-V compound semiconductors", *Nature*, vol. 479, pp. 317-323, 2011.

K. Lehovec, "Frequency dependence of the impedance of distributed surface states in MOS structures," *Appl. Phys. Lett.*, vol. 8, no. 2, pp. 48-50, Jan 1966.

K. Martens, C.O. Chui, G. Brammertz, B.D. Jaeger, D. Kuzum, M. Meuris, M.M. Heyns, T.

Krshnamohan, K. Saraswat, H.E. Maes, G. Groeseneken, "On the correct extraction of interface trap density of MOS devices with high mobility semiconductor substrates", *IEEE Trans. Electron Devices*, vol. 55, no. 2, pp. 547-556, 2008.

K. Martens, W.F. Wang, A. Dimoulas, G. Borghs, M. Meuris, G. Groeseneken, and H. E. Maes., "Determining weak Fermi level pinning in MOS devices by conductance and capacitance analysis and application to GaAs MOS devices", *Solid-State Electron.*, vol. 51, pp. 1101-1108, 2007

K. Martens, W.Wang, K.D. Keersmaecker, G. Borghs, G. Groeseneken, H. Maes, "Impact of weak Fermi-level pinning on the correct interpretation of III-V MOS C-V and G-V characteristics", *Microelectron. Eng.*, vol. 84, pp. 2146-2149, 2007

L. M. Terman, "An investigation of surface states at a silicon/silicon oxide interface employing metal-oxide-silicon diodes," *Solid-State Electron.*, vol. 5, pp. 285-299, 1962.

M. A. Negara, N. Goel, D. Bauza, G. Ghibaudo, and P.K. Hurley, "Interface state denisities, low frequency noise and electron mobility in surface channel $In_{0.53}Ga_{0.47}As$ n-

MOSFETs with ZrO_2 gate dielectric", *Microelectron. Eng.*, vol. 88, pp. 1095-1097, 2011.

M. L. Huang, Y.C. Chang, C.H. Chang, Y.J. Lee, P.Chang et al., "Surface passivation of III-V compound semiconductors using atomic-layerdeposition-grown Al_2O_3", *Appl. Phys. Lett.*, vol. 87, 252104, 2005.

M. Leskela, and M. Ritala, "Atomic layer deposition chemistry: Recent developments and future challenges", *Angew. Chem. Int. Ed.*, vol. 42, pp. 5548-5554, 2003.

M. Milojevic, C.L. Hinkle, F.S. Aguirre-Tostado, H.C. Kim, E.M. Vogel et al., "Half-cycle atomic layer deposition reaction studies of Al_2O_3 on $(NH_4)_2S$ passivated GaAs(100) surfaces" *Appl. Phys. Lett.*, vol. 93, 252905, 2008.

M. Passlack, M. Hong, and C.P. Mannaerts, "Quasistatic and high frequency capacitance–voltage characterization of Ga_2O_3–GaAs structures fabricated by in situ molecular beam epitaxy", *Appl. Phys. Lett.*, vol. 68, 1099, 1996.

N. M. Johnson and D. J. Bartelink, "Constant-capacitance DLTS measurement of defect-density profiles in semiconductors," *J. Appl. Phys.*, vol. 50, no. 7, pp. 4828-4833, 1979.

N. M. Johnson, "Measurement of semiconductor-insulator interface states by constant-capacitance, deep-level transient spectroscopy," *J. Vac. Sci. Technol.*, vol. 21, no. 2, pp. 303-314, 1982.

P. Blood and J. W. Orton, *The electrical characterization of semiconductors: majority*

P. D. Ye, G. D. Wilk, J. Kwo, B. Yang, H-J. L. Gossman, M. Frei, S. N. G. Chu, J. P. Mannaerts, M. Sergent, M. Hong, K. K. Ng, and J. Bude, "GaAs MOSFET with oxide gate dielectric grown by atomic layer deposition", IEEE Electron Device Lett., vol. 24, no. 4, 2003.

P. D. Ye, Y. Xuan, Y.Q. Wu, and M. Xu, "Inversion-mode $In_xGa_{1-x}As$ MOSFETs (x=0.53, 0.65, 0.75) with atomic-layer-deposited high-κ dielectrics", *ECS Trans.*, vol. 19, no.2, pp. 605-614, 2009.

R. Castagne, and A. Vapaille, "Description of the SiO_2-Si interface properties by means of very low frequency MOS capacitance measurements", *Surf. Sci.*, vol. 28, pp. 157-193, 1971.

R. Engel-Herbert, Y. Hwang, and S. Stemmer, "Comparison of methods to quantify interface trap densities at dielectric/III-V semiconductor interfaces", *J. Appl. Phys.*, vol. 50, 121101, December 2010.

R. L. Puurunen, “Surface chemistry of atomic layer deposition: A case study for the trimethylaluminum/water process”, *J. Appl. Phys.*, vol. 97, 121301, 2005.

R. Suzuki, N. Taoka, M. Yokoyama, S. Lee, S.H. Kim et al., “1-nm-capacitance-equivalent-thickness HfO_2/Al_2O_3/InGaAs metal-oxidesemiconductor structure with low interface trap density and low gate leakage current density”, *Appl. Phys. Lett.*, vol. 100, 132906, 2012.

R.D. Long, B. Shin, S. Monaghan, K. Cherkaoui, J. Cagnon, S. Stemmer, P.C. McIntyre, and P.K. Hurley, “Charged defect quantification in $Pt/Al_2O_3/In_{0.53}Ga_{0.47}As$/InP MOS capacitors”, *J. Electrochem. Soc.*, vol. 158, pp. 103-107, 2011

S. Koveshnikov, N. Goel, P. Majhi, H.Wen, M.B. Santosh, “$In_{0.53}Ga_{0.47}As$ based metal oxide semiconductor capacitors with atomic layer deposition ZrO_2 gate oxide demonstrating low gate leakage current and equivalent oxide thickness less than 1nm” *Appl. Phys. Lett.*, vol. 92, 222904, 2008.

S. Oktyabrsky, P.D. Ye, *Fundamentals of III-V semiconductor MOSFETs.* New York: Springer, 2010.

T. P. O’Regan, and P.K. Hurley, “ Calculation of the capacitance-voltage characteristics of GaAs, $In_{0.53}Ga_{0.47}As$, and InAs metal-oxide-semiconductor structures”, *Appl. Phys. Lett.*, vol. 99, 163502, 2011

W. E. Spicer, I. Lindau, P. Skeath, and C.Y. Su, “Unified defect model and beyond”, *J. Vac. Sci. Technol.*, vol.17, 1019, 1980

X. Wang, L. Dong, J. Zhang, Y. Liu, P. D. Ye, and R. G. Gordon, “Heteroepitaxy of La_2O_3 and $La_{2-x}Y_xO_3$ on GaAs (111) by atomic layer deposition: Achieving low interface trap density”, *Nano Lett.* , vol. 13, pp. 594-599, 2013.

Y. Hwang, R. Engel-Herbert, N. G. Rudawski, and S. Stemmer, “Analaysis of trap state densities at $HfO_2/In_{0.53}Ga_{0.47}As$ Interfaces”, *Appl. Phys. Lett.*, vol. 96, 102910, 2010

Y. Xuan, H.C. Lin, P.D. Ye, and G.D. Wilk, “Capacitance-voltage studies on enhancement-mode InGaAs metal-oxidesemiconductor field-effect transistor using atomic-layer-deposited Al_2O_3 gate dielectric”, *Appl. Phys. Lett.*, vol. 88, 263518, 2006.

Y.C. Wang, M. Hong, J.M.Kuo, J.P. Mannaerts, J. Kwo, H.S. Tsai, J.J. Krajevski, Y.K. Chen, A.Y. Cho, “Demonstration of submicron depletion-mode GaAs MOSFETs with negligible drain current drift and hysteresis”, *IEEE Electron Device Lett.*, vol. 20, 457, 1999.

Y.Yuan, L. Wang, B. Yu, B. Shin, J. Ahn, P.C. McIntyre, P.M. Asbeck, M. J. W. Rodwell, and Y. Taur, " A distributed model for border traps Al_2O_3-InGaAs MOS devices" *IEEE Electron Device Lett.*, vol.32, no.4, pp. 485-487, 2011