Fast-Transient Low-Dropout Regulators in the IBM 0.13μm BiCMOS Process

A Thesis

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By

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* * * * *

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ABSTRACT

This thesis presents work on the design of 1.5V, 100mA low-dropout (LDO) regulators with fast transient responses in the IBM8HP 0.13μm BiCMOS process. A conventional LDO architecture intended for use in an RF system was implemented and measured. The design of a printed circuit board (PCB) that is capable of measuring all pertinent characteristics of the regulator is also presented. Measurements show that the conventional design achieves a recovery time of less than 100ns with output voltage variations of less than 50mV. In addition to the conventional design, a new output capacitor-free architecture is introduced that can be fully integrated onto a chip. Simulations show that the output capacitor-free design achieves a recovery time of less than 50ns with output voltage variations of less than 140mV.

This thesis is dedicated to my parents who encouraged me to pursue my interests and showed me that there is no limit to what hard work and perseverance can achieve.

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CHAPTER 1

INTRODUCTION

Voltage regulators are a critical part of most integrated circuits (ICs). As illustrated in Figure 1.1, these regulators are responsible for providing a stable power supply to the loading circuitry. The choice of the type of regulator depends heavily on the system in which the regulator is operating. While switching regulators can exhibit very good efficiency, they also produce a significant amount of noise that can cause sensitive analog and RF circuits to fail. In these types of applications, linear regulators are typically employed for their low noise performance. However, all linear regulators generate the desired output voltage by directly dissipating the necessary power to account for the difference between input and output voltages. For this reason, low-dropout (LDO) regulators were developed which maximize power efficiency by minimizing the required input voltage.

For analog and RF applications, the transient response of the voltage regulator is critical to ensuring the performance of the loading circuits. The transient response is an indication of how fast the regulator can react to changes in the load current. A faster transient response means less noise at the output, thus reducing the impact of the regulator on the performance of the loading circuitry. For this reason, there is significant interest in the development of fast-transient regulators for analog and RF applications.

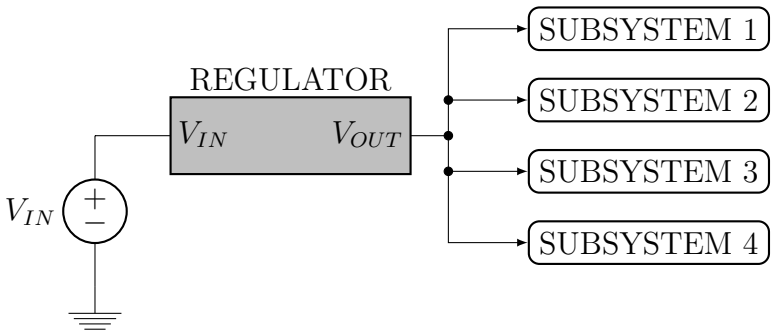


Figure 1.1: Typical Voltage Regulator Application

In addition to a fast transient response, the power supply noise due to crosstalk between critical subsystems can be reduced by powering each subsystem with its own regulator as shown in Figure 1.2. Unfortunately, conventional LDO regulators use a large external capacitance at their output to ensure stability and to provide a low impedance at high frequencies. The inclusion of this external capacitance in the design requires significant area, both on the chip and on the board, making it difficult to use multiple LDOs in a system. As a result of this limitation, interest in output capacitor-free LDO regulators has been growing. These regulators do not require the large output capacitor, and thus can be fully integrated onto the chip, saving a significant amount of area. However, without the capacitor at the output to provide a low impedance at high frequencies, there is a significant challenge in developing output capacitor-free LDO regulators that can achieve a transient response on par with those of the conventional design.

This thesis covers three main contributions. The first is a fast-transient LDO regulator implemented in the IBM8HP 0.13μm process. This regulator is designed using a conventional LDO regulator architecture with a large capacitor at the output to achieve a fast-transient response. Measurements indicate that this design achieves output voltage variations of less

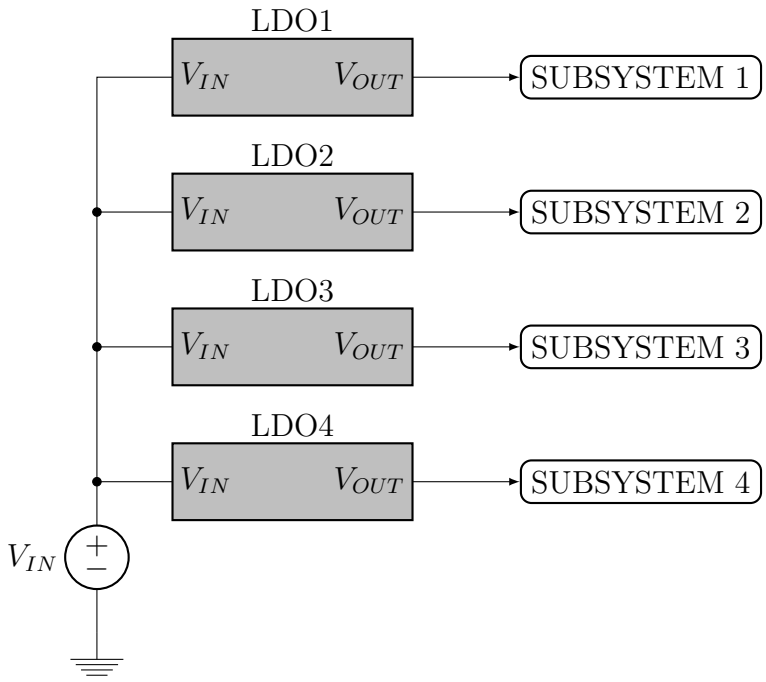


Figure 1.2: Local Power Supplies Using Integrated LDO Regulators

than 50mV with a recovery time of less than 100ns. The second contribution is a printed circuit board (PCB) designed to facilitate the measurement of all pertinent LDO characteristics. This test setup is easily extendable to any regulator that utilizes an off-chip output capacitance, and will facilitate the measurement of future regulator designs. The final contribution of this thesis is the design and simulation of a novel architecture for an output capacitor-free regulator that is capable of achieving a transient response almost as fast as that of the conventional design. Simulations show that the output capacitor-free design can achieve output voltage variations of less than 140mV and a recovery time of less than 50ns. The resulting regulator is suitable for a full-on chip implementation to drive high performance analog or RF circuitry.

The organization of the thesis is as follows. Chapter 2 gives some background on linear regulators, the conventional LDO regulator architecture, and recent advances in output capacitor-free designs. Chapter 3 covers the implementation of the conventional architecture in the IBM8HP 0.13μm BiCMOS process, as well as the test setup used to characterize the design. Chapter 4 introduces a new architecture for a fast-transient output capacitor-free regulator, along with simulation results to demonstrate its capabilities. Finally, Chapter 5 concludes the thesis and provides suggestions for future improvements to this work.

CHAPTER 2

BACKGROUND

Linear regulators are responsible for providing a stable supply voltage to a load circuit, regardless of how much current the load circuitry is consuming. As shown in Figure 2.1, a regulator is comprised of a power transistor and a control feedback loop. The power transistor is responsible for providing the necessary current to the load. The control circuitry that implements $H_{ctl}(s)$ is placed in a feedback loop to drive the power transistor such that the output of the regulator is regulated to the desired voltage. For integrated circuits, the load is typically a current source in parallel with a load capacitance.

2.1 Key Regulator Specifications

As a critical block for almost all integrated circuits, linear regulators have several specifications that must be met in order to ensure the proper operation of the load circuitry. The following sections define each of these specifications as used in this thesis.

2.1.1 Input Voltage and Load Current

The input voltage for integrated regulators is typically specified as the voltage, or range of voltages, at which all the other specifications are met for the regulator. The minimum input voltage is typically determined by the operating characteristics of the power transistor. That

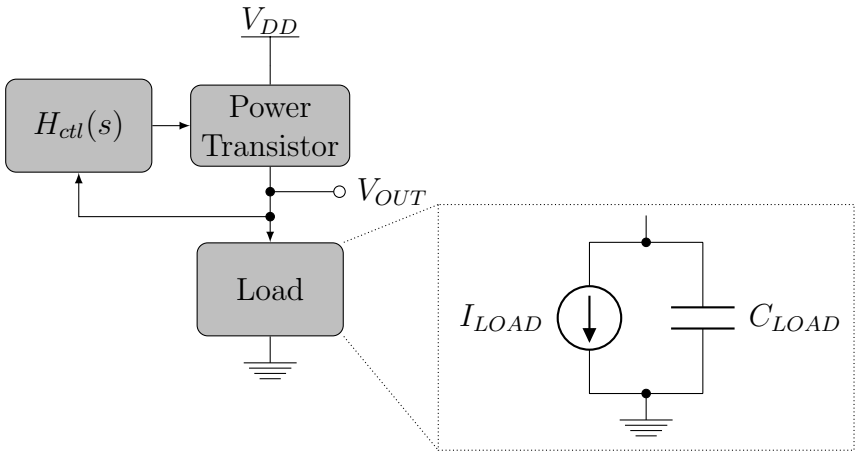


Figure 2.1: Block Diagram of a Linear Regulator

is, the input voltage must provide sufficient drain-source voltage to the power transistor, to ensure that it can supply the maximum load current to the load. The maximum input voltage is dictated by the process and type of transistors used to implement the circuitry of the regulator. For instance, many processes offer thick gate transistors that can sustain larger voltages before breaking down. Implementing the regulator circuitry using these thick gate devices can allow for the regulator to sustain larger input voltages.

The input voltage specification also has a significant impact on the power efficiency of the regulator. The power efficiency can be calculated as

$$\text{Efficiency} = \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT} I_{LOAD}}{V_{DD}(I_{LOAD} + I_Q)}, \tag{2.1}$$

where I_Q is the quiescent current of the regulator as discussed in Section 2.1.5 [8]. As shown, the efficiency is inversely proportional to the input voltage, V_{DD}. Thus, it is desired to minimize the necessary input voltage to improve the efficiency of the regulator.

The load current is typically specified as a minimum and maximum load current, designated I_{min} and I_{max}, respectively. For this range of load currents, it is expected that all

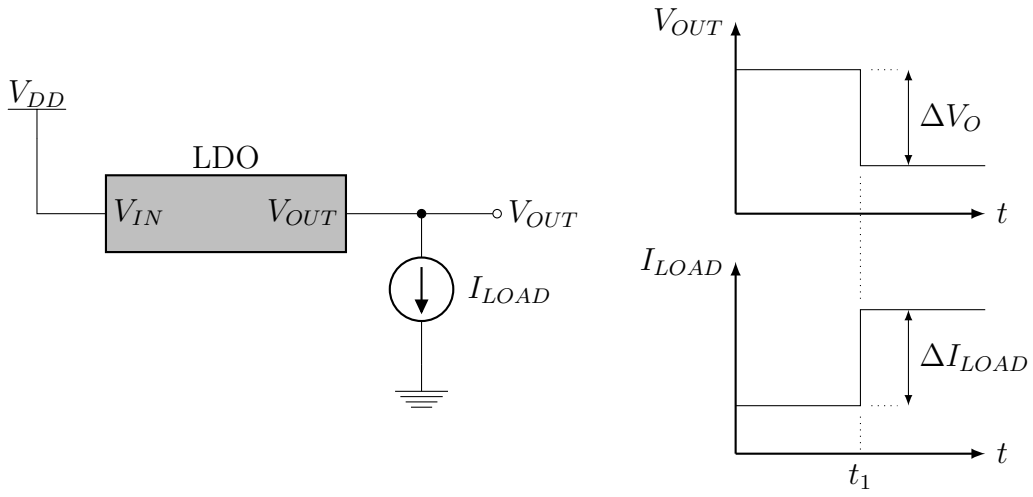


Figure 2.2: Definition of Load Regulation

specifications are met for the regulator. Generally, some properties of the regulator, such as load regulation, discussed in Section 2.1.2, will degrade when the load current is very low and the power transistor is driven into the cutoff region. The maximum load current specification indicates the amount of current that must be sourced through the power transistor, thus dictating its size.

2.1.2 Load Regulation

Load regulation is a measurement of the ability to regulate the output voltage over the entire range of desired load currents. Figure 2.2 shows how load regulation is typically measured for an LDO. The load current starts at the minimum value, I_{MIN}, and the DC output voltage is measured. Next, the load current is increased to the maximum value, I_{MAX} and the DC output voltage is measured again. The load regulation is then given as

$$\text{Load Regulation} = \frac{\Delta V_{OUT}}{\Delta I_{LOAD}}. \tag{2.2}$$

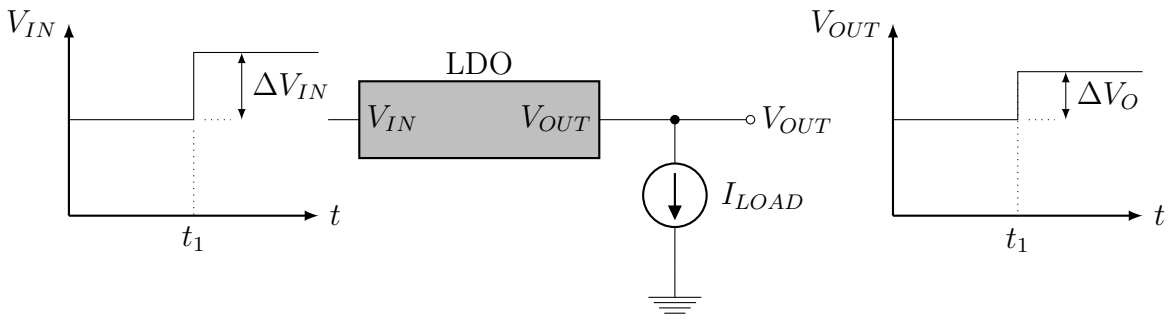


Figure 2.3: Definition of Line Regulation

2.1.3 Line Regulation

Line regulation is a measurement of the ability to regulate the output voltage when the input voltage changes. Figure 2.3 shows how line regulation is typically measured for an LDO. The output voltage is measured for two different input voltages. In this thesis, the change in input voltage is chosen as $\Delta V_{IN} = 0.1\text{V}$. The line regulation is then calculated as

$$\text{Line Regulation} = \frac{\Delta V_{OUT}}{\Delta V_{IN}} \tag{2.3}$$

.

2.1.4 Power Supply Rejection

Power supply rejection (PSR) is a measurement of the ability of the regulator to reject variations in the input voltage. In linear regulators, applying a ripple to the input of the regulator results a ripple out the output of same frequency and smaller amplitude as shown in Figure 2.4. The PSR of a regulator is typically measured in dBs and is given as

$$\text{PSR} = 20\log_{10}\frac{v_{OUT}}{v_{IN}}. \tag{2.4}$$

PSR is similar to line regulation as discussed in Section 2.1.3, however PSR is a small-signal AC measurement, whereas line regulation only measures DC variations.

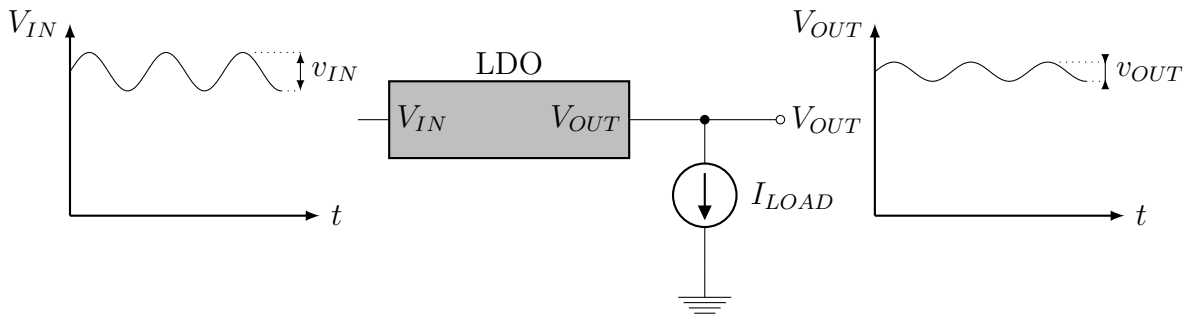


Figure 2.4: Definition of Power Supply Rejection

2.1.5 Quiescent Current

The quiescent current of the LDO is the amount of current consumed by the LDO that is not supplied to the load. It can be used to determine the efficiency of an LDO. In battery-powered applications, the battery life is more readily estimated by using the current efficiency rather than the power efficiency as discussed in Section 2.1.1 [2, 16]. The current efficiency can be calculated as

$$\text{Efficiency}_\text{I} = \frac{I_{OUT}}{I_{IN}} = \frac{I_{LOAD}}{I_{LOAD} + I_Q}. \tag{2.5}$$

Thus, it is desired to minimize the quiescent current of the regulator to increase the current efficiency, allowing for an increase in battery life.

2.1.6 Transient Variations

Transient output variations occur at the output of the regulator when the load current is quickly increased or decreased. This causes undershoots and overshoots in the output voltage, during which the sudden change in load current propagates through the control loop. This is illustrated in Figure 2.5 for the case that the load current suddenly increases. A similar issue occurs when the load current suddenly decreases with the transient variation

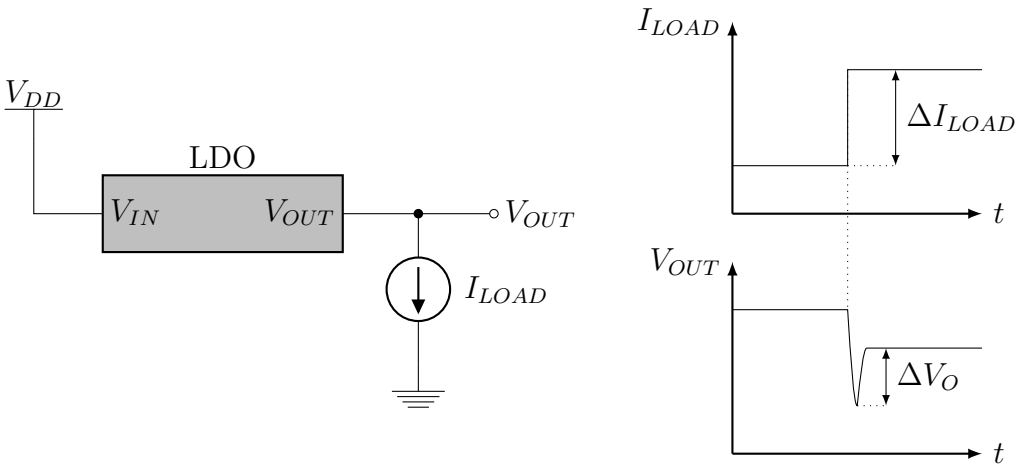


Figure 2.5: Illustration of Transient Supply Variation and Recovery Time

being opposite in magnitude. As shown, the supply variation, ΔV_O, is defined as the peak difference in output voltage when the load current suddenly changes.

Both the recovery time, T_R, and the settling time, T_S, can be used to characterize the transient response of the regulator as shown in Figure 2.6. The recovery time is defined as the time it takes for the output voltage to return to within ΔV_R of the final output voltage. In this thesis, ΔV_R is defined as 1% of the final output voltage. It is important to note that the recovery time does not consider the variation in supply voltage after it recovers to the desired value, making it mostly useful for applications where only the absolute value of the supply voltage matters. Alternatively, the settling time can be used to indicate the time it takes for the output to reach its steady state value after the load current is switched. From Figure 2.6, the settling time is given as

$$T_S = t_{r1} + t_{r2}, \tag{2.6}$$

where t_{r1} is the time it takes for the regulator to respond to the change in load current, and t_{r2} is the time it takes to settle to within $1\% \cdot \Delta V_O$ of the final value after the regulator

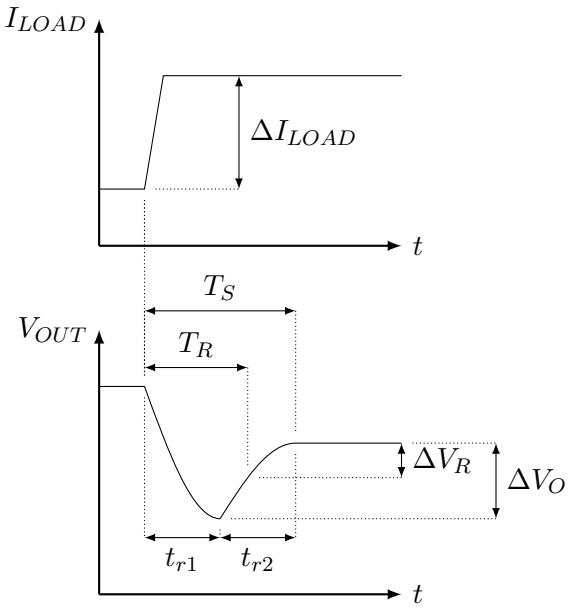


Figure 2.6: Transient Variation Definitions

responds. The settling time is a more suitable metric for sensitive analog or RF applications where any variations in the supply voltage can degrade the performance of the system.

In general, transient variations in LDO regulators have been shown to depend largely on the bandwidth of the regulator, the slew rate of the internal nodes, and any capacitive decoupling at the output [18, 26, 31]. The time for the regulator to react to the change in load current is defined as t_{r1} and can be approximated by

$$t_{r1} \approx \frac{1}{BW_{CL}} + t_{sr}, \tag{2.7}$$

where BW_{CL} is the closed-loop bandwidth of the regulator, and t_{sr} is the delay in the regulator loop due to the finite slew rate of the circuitry. As discussed in Section 2.2, the value of t_{r1} largely determines the magnitude of the transient variation, ΔV_O. The settling

and recovery times are mostly dominated by t_{r2}, which is determined by all of the settling characteristics of the regulator including the bandwidth, slew rate, and phase margin.

2.2 Conventional LDO Regulator Architecture

Conventionally, LDO regulators have been designed using the architecture shown in Figure 2.7. In this architecture, the power transistor, M_P, supplies the necessary current to the load. The use of a PMOS device as the power transistor allows the regulator to operate at input voltages as low as $V_{OUT} + V_{DSATP}$, where V_{DSATP} is the drain-source voltage that is required to maintain the power transistor in the saturation region over the desired load current range. The amplifier, often called the error amplifier in LDO regulators, compares V_{FB} with the output of a bandgap voltage reference, and adjusts the gate voltage of the power transistor such that $V_{FB} = V_{BG}$. Thus, the output voltage can be controlled by choosing R_{FB1} and R_{FB2} such that

$$\frac{R_{FB1} + R_{FB2}}{R_{FB2}} = \frac{V_{OUT}}{V_{BG}}. \tag{2.8}$$

As discussed in Sections 2.2.1 and 2.2.2, a large external capacitor, C_L, is used to stabilize the regulator and improve the transient response. This capacitor will exhibit a nonzero equivalent series resistance (ESR), denoted as R_{ESR} in Figure 2.7. This ESR can significantly impact both the stability and transient response of the regulator, and as such, must be considered when designing a regulator that uses the conventional architecture.

2.2.1 Stability

The conventional LDO regulator architecture, shown in Figure 2.7, can be viewed as a two stage amplifier, with the error amplifier forming the first stage and a power transistor with feedback resistors forming the second stage. This indicates that the uncompensated

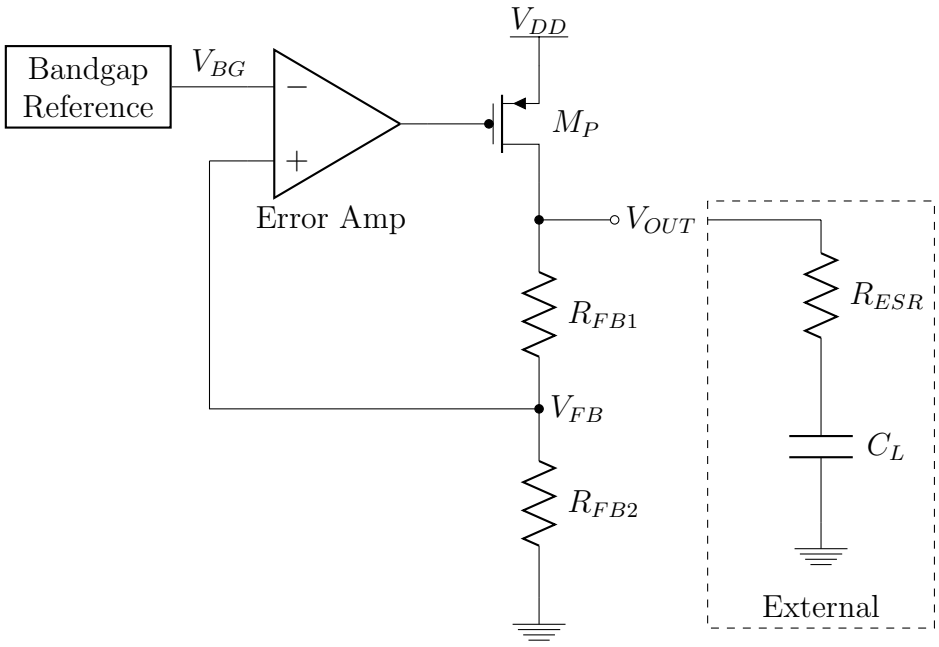
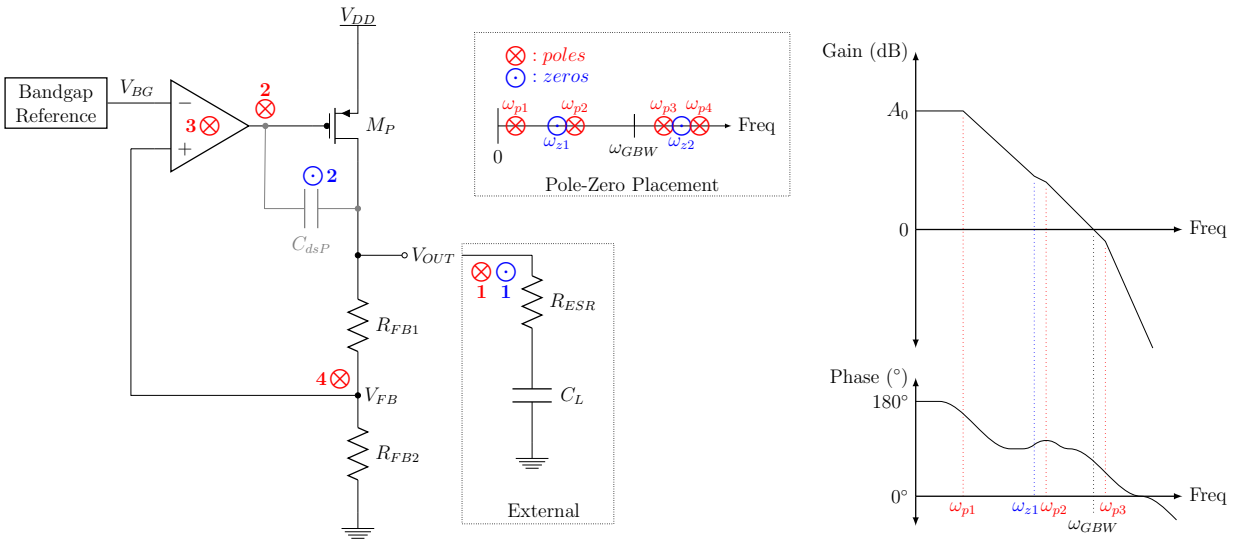


Figure 2.7: Conventional LDO Regulator Architecture

regulator will have at least two significant poles and may be unstable. Thus, the poles and zeroes of the regulator must be carefully designed to ensure its stability [10]. Figure 2.8a shows the poles and zeroes contributed to the loop gain by each node in the regulator. As shown, the regulator exhibits a large amount of poles and zeros that can make stability difficult to achieve.

Figure 2.8b shows the relative placements of the poles and zeros in the conventional design, where the poles and zeros are approximated using the effective resistance and capacitance at each node [30]. The large external capacitor, C_L, creates a dominant low frequency pole at the output of the regulator. This pole can be approximated as

$$\omega_{p1} \approx -\frac{1}{R_{OUT}C_L}, \tag{2.9}$$



(a) Corresponding Nodes for Poles and Zeroes (b) Bode Diagram

Figure 2.8: Pole-Zero Placement of the Conventional Architecture

where $R_{OUT} = (R_{FB1} + R_{FB2}) \parallel r_{dsP}$ is the effective resistance at the output of the regulator, and r_{dsP} is the drain-source resistance of the power transistor. Over the range of valid load currents, r_{dsP} can change by more than an order of magnitude, causing ω_{p1} to be largely dependent upon the load current. Such a large deviation in the location of the dominant pole makes the stabilization of the regulator non-trivial.

Another non-dominant low frequency pole is created at the gate of M_P due the large gate-source and gate-drain capacitances of the transistor. The pole can be approximated by

$$\omega_{p2} \approx -\frac{1}{R_{EA}C_{GP}}, \tag{2.10}$$

where R_{EA} is the output resistance of the error amplifier, and C_{GP} is the effective capacitance at the gate of the power transistor. This pole will create additional phase shift than can render the regulator unstable if it is not carefully designed. If needed, ω_{p2} can be moved to higher frequencies by inserting a voltage buffer to drive the gate of M_P, [2, 7, 31]. Rather

than increasing the current consumption of the regulator to push ω_{p2} to higher frequencies, the effects of ω_{p2} can be canceled by placing a nearby zero as discussed later in this section. Additional poles are formed at V_{FB} as well as at the internal nodes of the error amplifier. To ensure stability, these poles must be placed at frequencies much higher than the unity-gain bandwidth of the regulator.

The conventional architecture contains two zeros that affect the stability. The ESR of the external capacitor will form a left-half-plane (LHP) zero that can be approximated by

$$\omega_{z1} \approx -\frac{1}{R_{ESR}C_L}. \tag{2.11}$$

This zero can be placed near ω_{p2}, such that the pole and zero cancel, as shown in Figure 2.8. However, the designer has little control over R_{ESR}, making pole-zero cancellation a non-trivial task. If $\omega_{z1} < \omega_{p2}$, a bandwidth extension will occur that may move the unity-gain frequency past the other high-frequency poles. On the other hand, if ω_{z1} moves to higher frequencies such that $\omega_{z1} > \omega_{p2}$, excess phase shift will occur for the frequencies between the pole and the zero, resulting in degraded stability. Thus the regulator must be designed such that variations in R_{ESR} can be tolerated without becoming unstable. Alternatively, improvements to the conventional architecture have been proposed that generate an internal low frequency LHP zero that can be used to cancel ω_{p2}, however, this requires that ω_{z1} is moved to high frequencies, which may limit the maximum allowable value for C_L [5].

The second zero is located in the right-half-plane (RHP), and is formed by the gate-drain capacitance of the power transistor, C_{gdP}. Because C_{dgP} appears across the gain stage formed by M_P and the feedback resistors, it exhibits the well-known Miller effect [17, 30]. The Miller effect has three significant effects on the pole-zero frequencies in the regulator. The first of these effects is a significant increase in the effective capacitance at the gate of M_P, moving ω_{p2} to lower frequencies. Second, due to the feedforward path from V_G to V_{OUT},

ω_{p1} will move to higher frequencies. In other words, the separation between the dominant and non-dominant poles will be reduced, degrading the stability of the regulator. The third impact of the Miller effect due to C_{gdP} is an RHP zero, ω_{z2}, that is also caused by the feedforward path from V_G to V_{OUT}. This zero can be approximated as

$$\omega_{z2} \approx \frac{g_{mP}}{C_{gdP}}, \tag{2.12}$$

where g_{mP} is the transconductance of M_P. For large load currents, g_{mP} will be very large, placing ω_{z2} at high frequencies. However, as the load current is decreased, g_{mP} will also decrease, moving ω_{z2} to lower frequencies. If ω_{z2} moves to frequencies close to that of the unity-gain bandwidth of the regulator, the gain margin, and thus the stability, will be degraded. Thus, care should be taken to ensure that the unity-gain bandwidth of the regulator is much less than ω_{z2} for all loading conditions to ensure stability.

2.2.2 Transient Response

As discussed in Section 2.1.6, the transient variations of the regulator are determined largely by the bandwidth of the regulator, the slew rate of its internal nodes, and any capacitive loading decoupling at the output. The instant that the load current switches from I_{MIN} to I_{MAX}, the control circuitry will have yet to react, requiring the difference in load current to come directly from the capacitor. Furthermore, while the capacitor will act as an AC ground at high frequencies, the voltage drop across R_{ESR} will immediately appear at the output, due to the load current begin provided by the C_L. Thus, the transient variation do to a sudden change in load current is approximated as

$$\Delta V_O \approx \frac{\Delta I_{LOAD}}{C_L} t_{r1} + \Delta I_{LOAD} R_{ESR}, \tag{2.13}$$

where t_{r1} is the time it takes for the regulator to respond to the variation and is related to the bandwidth of the regulator as discussed in Section 2.1.6, [27]. As shown in (2.13), C_L

can reduce the transient variations by slowing them down enough for the control circuitry to react to the sudden change. However, the minimum achievable performance will be limited by R_{ESR} which is not easily controlled by the designer. It is important to note that the results of (2.13) do not consider the response of the regulator after the load switch and before t_{r1}, making the equation a somewhat pessimistic approximation, however it still provides fundamental insight into the transient response of the regulator.

Further insight into the transient response of the regulator can be obtained by analyzing the output impedance of the conventional architecture using the simplified diagram in Figure 2.9. For this analysis, the control circuitry, comprised of the error amplifier and feedback network, is simplified into the transfer function $H_{ctl}(s)$. For a fast transient response, the regulator must exhibit a low output impedance at high frequencies to effectively mitigate voltage fluctuations at the output due to sudden changes in the load current. The output impedance of the regulator in Figure 2.9 is derived as

$$Z_{OUT} = \frac{1}{sC_L + H_{ctl}(s)g_{mP}}. \tag{2.14}$$

Again, it is clear that increasing C_L will reduce the output impedance at high frequencies, thus resulting in an improved transient response. The dependence of the transient response on the bandwidth of the control circuity is also shown in (2.14). As discussed previously, the dominant pole created by the large external capacitance requires that the bandwidth of the control circuitry is large to ensure the stability of the regulator. The use of high bandwidth control circuitry is a distinct advantage of the conventional design over the output capacitor-free designs discussed in Section 2.3. The result is that $|H_{ctl}|$ will be larger at high frequencies, yielding a lower output impedance, and thus an improved transient response.

As discussed in Section 2.1.6 the response time of the regulator, t_{r1}, is largely determined by the bandwidth and the slew rate at the internal nodes of the regulator [18, 27]. This

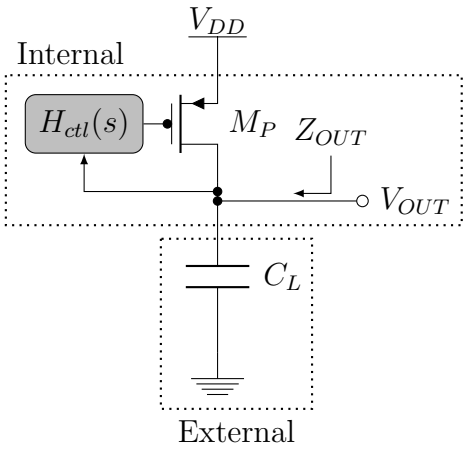


Figure 2.9: Simplified Representation of the Conventional Architecture

problem can be solved by increasing the current of the error amplifier such that the slew rate is not an issue, however this can significantly degrade the efficiency of the regulator, especially when the load current is low. The use of current feedback amplifiers to provide a slew rate improvement [26,32] has also been proposed, however this technique is often limited by voltage headroom and is still limited by the bandwidth of the amplifier during transient voltage swings at the output. Another solution is to dynamically increase the bias current of the amplifier when the load current is high [31]. Such a solution can increase the slew rate of the amplifier, while providing a minimal impact on the efficiency of the regulator, however it will only help when the load current is switched from low to high. When switched from high to low, the bias current of the amplifier will decrease, thus degrading the slew rate.

Slew rate enhancement (SRE) circuits have also been proposed that momentarily increase the amount of current during slewing conditions, without significantly increasing the quiescent current [21, 25]. These slew rate enhancement circuits can ideally sense transient swings in the output voltage, and charge the slow internal node as fast as possible during

such swings without significantly impacting the frequency response, and thus the stability, of the regulator. In the conventional architecture, SRE circuits are typically used to charge and discharge the large gate capacitance of the power transistor.

2.3 Output Capacitor-Free LDO Regulators

Although an output capacitor can be used to achieve fast-transient performance in LDO regulators as discussed in Section 2.2, the use of the output capacitor severely limits the ability to integrate multiple regulators on a single chip, as each regulator would require at least one pin on the chip for the output as well as an external capacitor on the board that is placed close to the pin. To solve these issues, output capacitor-free LDO regulators have been recently developed [3, 6, 13, 14, 16, 18–20, 22–25]. These regulators remove the need for an external capacitor, allowing the entire regulator to be integrated onto the chip.

2.3.1 Stability

To achieve stability in output capacitor-free regulators, a significantly different approach is required than that of the conventional design. This concept is illustrated in Figure 2.10, where the control circuitry for the output capacitor-free design is simplified into the transfer function $H_{slow}(s)$. The pole formed at the output of the regulator is located at a very high frequency due to the low load capacitance, necessitating a dominant pole located at low frequencies in $H_{slow}(s)$. In other words, the output capacitor-free regulator is stabilized by slowing down the control circuitry. This is a significant departure from the strategy of the conventional architecture, shown in Figure 2.9, where the dominant pole is located at the output, and high-bandwidth control circuitry can be used.

Although reducing the bandwidth of the control circuitry stabilizes the output capacitor-free regulators, this can also severely degrade the transient response. Thus, a significant

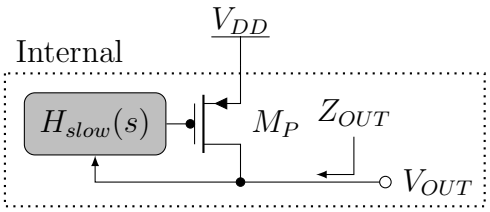


Figure 2.10: Simplified Representation of the Output Capacitor-Free Regulator

challenge in developing output capacitor-free LDO regulators is the creation of an internal dominant pole, while maintaining the largest possible bandwidth. Much of the literature involves compensation strategies similar to the pole-splitting techniques of multistage amplifiers [11, 14, 18, 22, 24, 25]. The movement of many of the poles in LDO regulators over different load conditions makes these types of compensation techniques more difficult than for typical multistage amplifiers. To maintain stability over these conditions, techniques such as damping factor compensation [20], Q-reduction for non-dominant poles [19], and gain reduction [16] have been developed to stabilize output capacitor-free regulators, while minimizing the required internal compensation capacitance. Recently, output capacitor-free LDO regulators based on the flipped voltage follower (FVF) have been proposed [3, 7, 13, 23, 27]. As discussed in detail in Chapter 4, these FVF-based regulators remove the need for a high gain error amplifier, reducing the number of poles that can potentially cause instability. However these FVF-based regulators often suffer from several drawbacks that are discussed in detail in Section 4.1.

2.3.2 Transient Response

While the previously discussed techniques are able to effectively stabilize an output capacitor-free regulator while improving its bandwidth, achieving a transient response comparable to that of conventional designs remains a challenge. The small load capacitance will discharge very quickly after a large increase in current, making the first term in (2.13) rather large. Because the load is integrated on the chip alongside the regulator, the ESR effect in (2.13) can be mitigated, however this is typically insignificant compared to the fast discharging of the small load capacitance. Furthermore, because stability is achieved by placing the dominant pole in the control circuitry, effectively slowing the control loop down, t_{r1} will be large compared to the conventional architecture, resulting in a degraded transient response. This can be seen more clearly by noting the effect of removing the output capacitor on the output impedance of the regulator. Ignoring the small load capacitance, the output impedance in Figure 2.10 is derived as

$$Z_{out} = \frac{1}{H_{slow}(s) g_{mP}}. \tag{2.15}$$

Thus, because the dominant pole is placed in the control circuitry, H_{slow} will exhibit a low bandwidth, resulting in a large output impedance at high frequencies.

As with the conventional architecture, the slew rate of the control circuitry has a significant impact on the transient response of the output capacitor-free regulators. The issue is even more severe in output capacitor-free regulators due to the placement of the dominant pole in the control circuitry. The slew rate is typically the worst at the node at which the internal dominant pole is placed [18]. In [14], the transient response of the regulator was significantly improved by consuming about 6mA of current to overcome these slew rate issues. However, in addition to the large amount of current the regulator in [14] is intended for

microprocessors and exhibits insufficient load regulation capabilities for many other applications. The slew rate enhancement circuits discussed in Section 2.2 are also suitable for use in output capacitor-free regulators [3,13,15,22,24]. Although slew rate enhancement circuits can significantly improve the transient response of an output capacitor-free regulator, they must sense the output voltage to detect when transient swings are occurring, before they can react accordingly. The delay inherent to sensing the output voltage often inhibits their ability to achieve transient performance on par with conventional regulators.

CHAPTER 3

CONVENTIONAL LDO DESIGN

Many applications, especially RF systems, require linear regulators which exhibit a fast transient response. Such regulators reduce the amount cross-talk between critical blocks, improving the performance of the system. This chapter details the design of a fast-transient regulator in the IBM 0.13μm process and a test setup capable of thoroughly characterizing the proposed regulator.

Table 3.1 shows the design goals for the proposed LDO regulator. Because this regulator is designed for a nominal load of 100mA, the quiescent current specification of 3mA is fairly relaxed. With the output capacitor keeping the transient variations at acceptable levels, this current can be used in the error amplifier to obtain a bandwidth that is high enough to ensure that the recovery time specification is met.

The input voltage range of $1.8 - 3$V also poses a challenge. Voltage headroom suffers when the input voltage is 1.8V, however an input voltage of 3V requires the use of thick gate devices for many of the critical transistors which exhibit larger gate capacitance and higher threshold voltage than the standard transistors in the process. This can make it more difficult design the error amplifier and power transistor to achieve the desired performance.

Table 3.1: Design Goals for the LDO Regulator

Parameter	Specification	Units
Input Voltage	$1.8 - 3$	V
Max. Load Current	100	mA
Output Voltage	1.5	V
Transient Variation	± 100	mV
PSR @ 100Hz	< -55	dB
Recovery Time	< 100	ns
Accuracy	3	%
Quiescent Current	3	mA
Load Regulation	20	$^{\mathrm{mV}}/_{\mathrm{A}}$
Line Regulation	1	$^{\mathrm{mV}}/_{\mathrm{V}}$

3.1 Power Transistor and Feedback Network Design

The design of the power transistor and feedback network, as shown in Figure 3.1, are critical to the performance of the regulator. Table 3.2 shows the designed component parameters for the power transistor and feedback network. The power transistor, M_P, was designed to remain in saturation over the entire load current range. As shown in Figure 3.2, this is not trivial to do with the limited headroom of the power transistor. The result is a very large power transistor which makes the design of the error amplifier critical. However the large size of the power transistor is necessary in this design to ensure sufficient loop gain at high load currents. Furthermore, the drain-source resistance is higher in the saturation region than in the triode region. This helps to keep the dominant pole at the output of the regulator from becoming too high which could lead to instability. Increasing the size of the power transistor too much will increase the current in the subthreshold region of the transistor, making it harder to turn off under low load conditions. This can degrade load regulation and power supply rejection depending on the minimum load current that the regulator is required to drive. In this design, a minimum load current of 5mA is used so that the

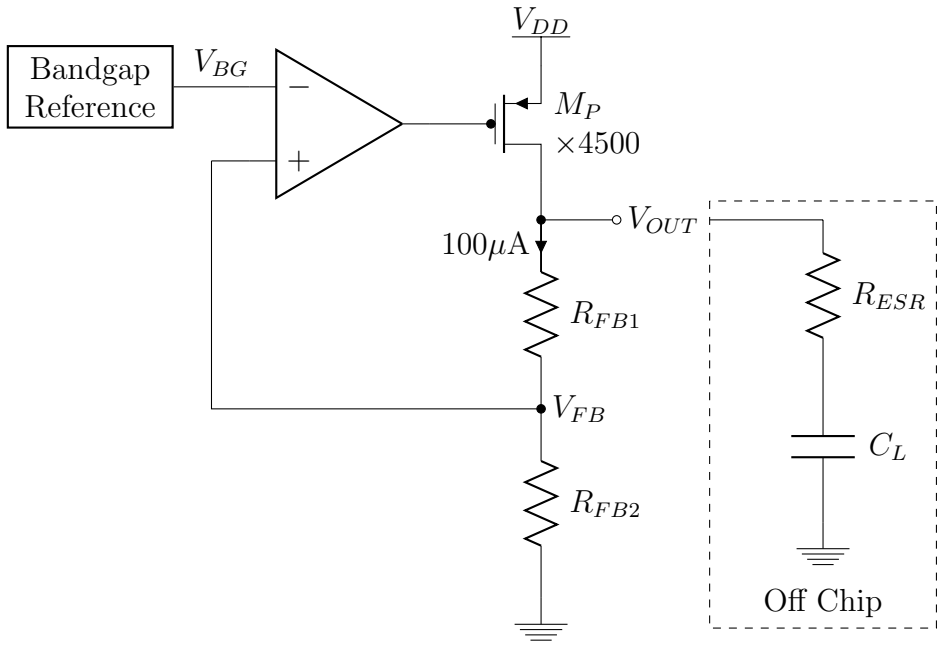


Figure 3.1: Schematic of the Conventional LDO Design

current in the power transistor in the subthreshold region does not significantly impact the performance when the load current is low. Below this minimum load current, the regulator performance will degrade.

The feedback network was designed to ensure that the pole at V_{FB} that is formed by the feedback resistors and the input to the amplifier is well above the unity-gain bandwidth of the regulator. Because the power transistor is so large, its drain-source resistance is typically smaller than R_{FB1} and R_{FB2} and as such, the feedback resistors do not impact the dominant pole at the output of the regulator.

The output capacitor was also selected carefully to ensure the regulator is stable and meets the transient specifications. A large capacitor is required to form the dominant pole with the output resistance of the power transistor, however, larger capacitances often exhibit larger ESRs. While the ESR is necessary to achieve stability, it must be limited to meet the

Table 3.2: Component Parameters for the Power Transistor and Feedback Network

Component	Value	Units
M_P	10/0.24	μm/μm
R_{FB1}	4	kΩ
R_{FB2}	11	kΩ
C_L	1	μF
R_{ESR}	$0.5 - 2$	Ω

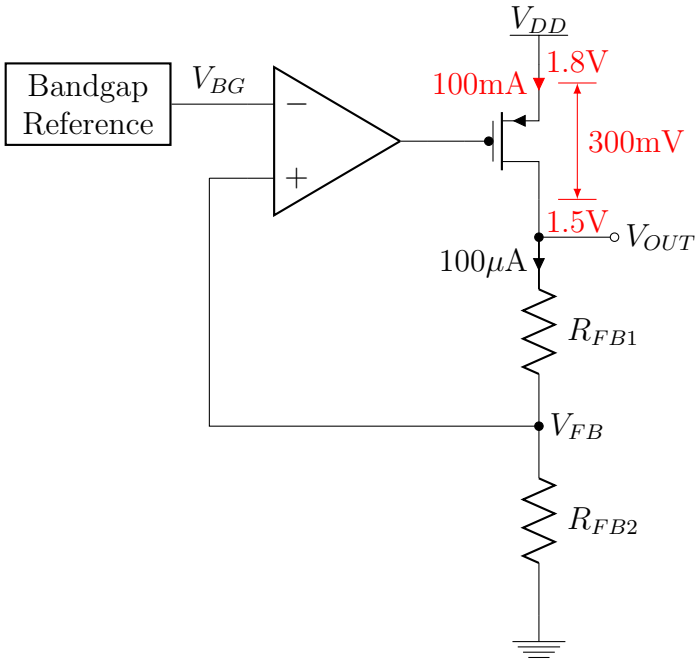


Figure 3.2: Illustration of the Minimum Voltage Headroom in the Regulator

transient variation specifications as discussed in Section 2.2. It is also important to consider other series resistances between the regulator and the output capacitor that add directly with the ESR of the capacitor such as interconnect and bondwire resistance. While these resistances may not have a significant impact on the transient variations, it could have a significant impact on the stability of the regulator by moving the LHP zero that is created by the ESR. Thus, the stability should be confirmed for a range of ESRs. The proposed regulator was designed to ensure stability for ESR values of $0.5 - 2\Omega$ by adjusting the pole at the output of the error amplifier

3.2 Error Amplifier Design

Figure 3.3 shows the schematic of the error amplifier used in the proposed design. The core of the amplifier is the differential pair formed by Q_1 and Q_2. The use of bipolar transistors for the input pair rather than MOSFETs improves the transconductance of the input pair, thus increasing the gain and bandwidth of the amplifier. Transistors $M_1 - M_4$ form two source followers that provide the necessary current to the bases of the input pair. Without these source followers, the input of the amplifier would draw enough current to significantly impact the output of the bandgap voltage reference, thus degrading the accuracy of the regulator. Transistor M_8 creates the bias current with the bias voltage V_{BP}. The bandgap voltage reference generates V_{BP} to create a proportional-to-absolute-temperature (PTAT) current. Biasing the NPN transistors with a PTAT current yields a stable transconductance over the entire operating temperature range so that the bandwidth of the amplifier does not significantly change with temperature [17].

Transistors $M_{12} - M_{14}$ implement dynamic biasing for the amplifier. This technique was first proposed in [31] as a means of improving the current efficiency at low load currents.

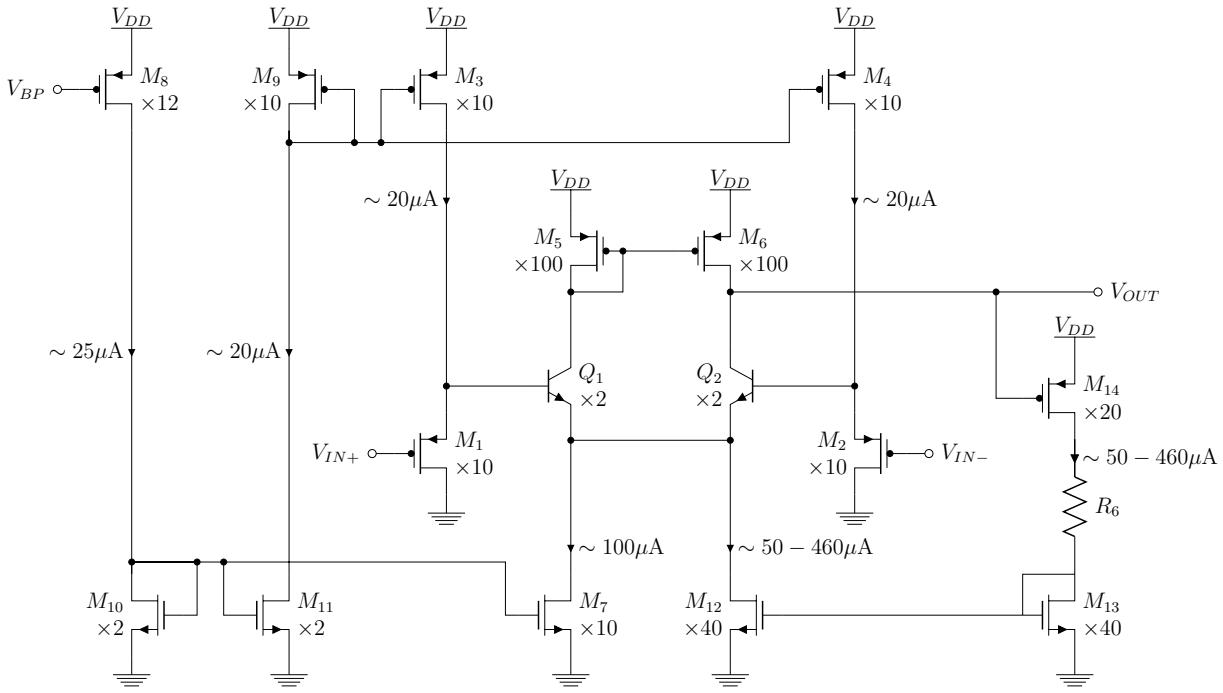


Figure 3.3: Proposed Error Amplifier Schematic

Table 3.3: Component Parameters For the Error Amplifier

Component	Value	Units
$Q_1 - Q_2$	18/0.12	μm/μm
$M_1 - M_2$	9/2	μm/μm
$M_3 - M_4$, M_9	10/1	μm/μm
$M_5 - M_6$	10/1	μm/μm
M_7, $M_{10} - M_{13}$	10/1	μm/μm
M_8	10/5	μm/μm
M_{14}	10/0.24	μm/μm
R_6	3	kΩ

M_{14} mirrors the current in the power transistor to the tail current of the differential pair so that the current consumption of the amplifier is reduced for low load currents where the current consumption of the error amplifier can be a significant portion of the total current consumption of the regulator. Resistor R_6 mitigates current offsets between M_{14} and M_P due to the finite output resistance of M_{14}. Under high load currents, the power consumption of the system is dominated by the load current as well as the dropout voltage, making the increase in current consumption of the error amplifier negligible.

In this design, the dynamic biasing of the error amplifier provides additional benefits to the regulator. The load transistors, $M_5 - M_6$ are designed for the maximum biasing conditions of the amplifier. Thus, at low load currents they are driven into the subthreshold region, resulting in an increase in their drain-to-source resistances. Due to the large size of the power transistor, the output of the error amplifier is very close to V_{DD} such that the power transistor is sufficiently shut off. The high output voltage of the amplifier can degrade the gain if M_6 is driven into the triode region, thus the increase in the drain-to-source resistance improves the gain under these conditions, allowing the regulator to maintain sufficient power supply rejection and load regulation characteristics.

Furthermore, the increase in the bias current of the amplifier during high load current improves the slew rate at the gate of the power transistor. As discussed in Section 2.2, the slew rate at the gate of the power transistor can have a significant impact on the transient performance of the regulator. The increase in current allows for a quicker recovery when the load current swings from low to high currents.

3.3 Bandgap Voltage Reference

The design of the voltage reference used in an LDO regulator is critical to the accuracy and power supply rejection of the regulator. The reference voltage directly sets the output voltage of the regulator, and as such any inaccuracies or power supply ripple in the reference voltage are translated directly to inaccuracies and ripple at the output of the regulator. While a detailed analysis of bandgap voltage references is outside the scope of this paper, this section will cover the most important considerations of the voltage reference design used in the proposed regulator.

Figure 3.4 shows the schematic of a conventional bandgap voltage reference that was used in the proposed LDO regulator design [17,30]. Table 3.4 shows the parameters for each component in the design. The core of voltage reference is formed by $Q_3 - Q_4$, $R_1 - R_5$, and $M_{15} - M_{16}$. The amplifier maintains equal currents in both legs of the core. The feedback loop is stabilized by capacitor C_C. Transistors $M_{17} - M_{18}$ and the resistor R_6 form a startup circuit that ensure that the bandgap enters the correct state when power is applied to the circuit. Assuming $R_1 = R_2 = R_{1,2}$ and $R_3 = R_4 = R_{3,4}$, the output of the voltage reference is given as

$$V_{BG} = V_{BE3} + \frac{R_2 + R_4}{R_5 + (R_3 - R_4)}\Delta V_{BE} \approx V_{BE1} + \frac{R_{1,2} + R_{3,4}}{R_5}\Delta V_{BE}, \tag{3.1}$$

where V_{BE1} is the base-emitter voltage of Q_3, and ΔV_{BE} is the difference in base-emitter voltages between Q_3 and Q_4. The first-order dependence of V_{BG} on temperature can be mitigated by adjusting $R_{1,2}$ and $R_{3,4}$. R_{LP} and C_{LP} form a low pass filter to improve power supply rejection at high frequencies.

Figure 3.5 shows the schematic of the amplifier used in the bandgap voltage reference. This amplifier is a simple differential pair with an active load. Transistors $M_{23} - M_{25}$ form

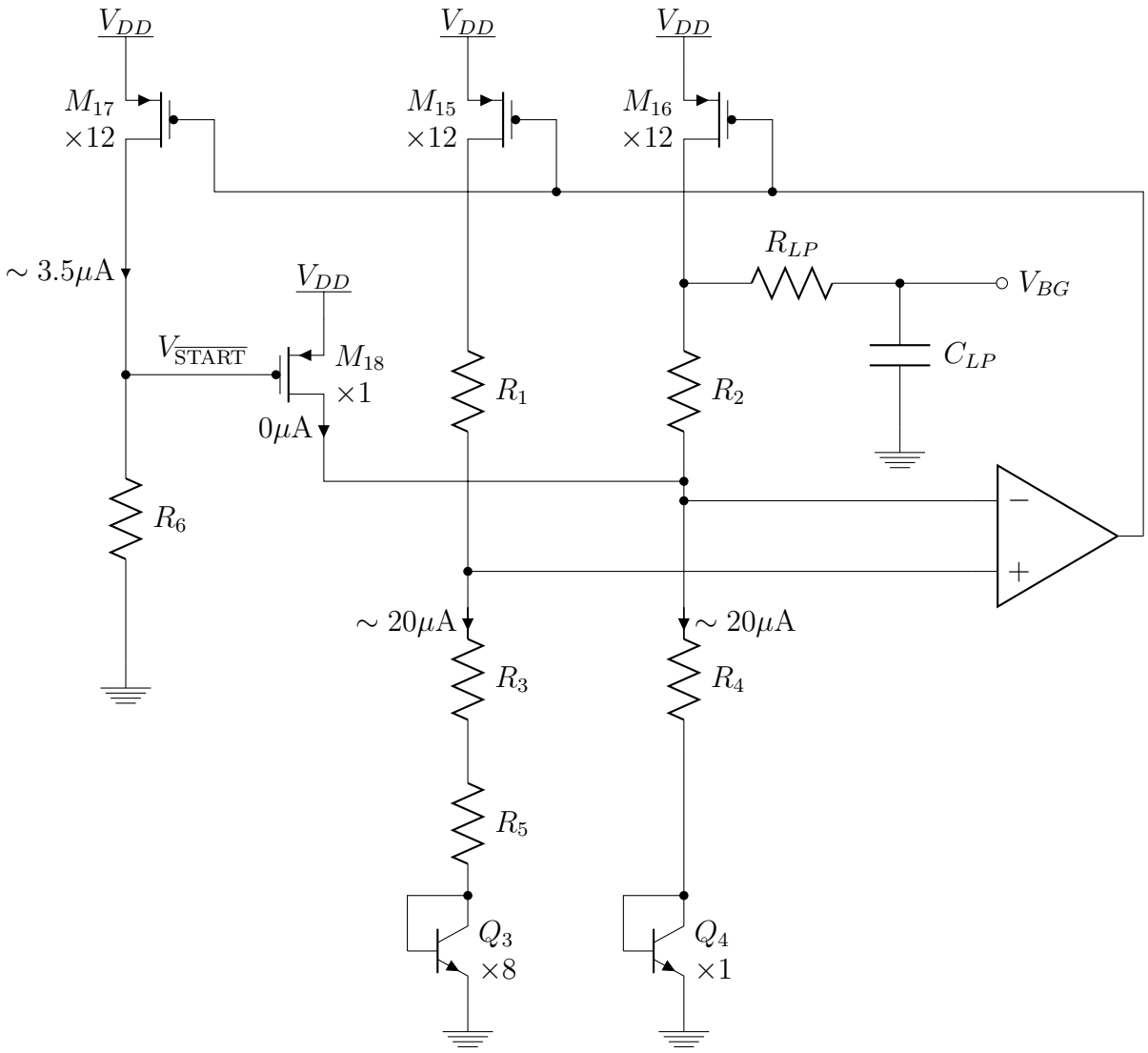


Figure 3.4: Bandgap Voltage Reference Schematic

Table 3.4: Component Parameters for the Voltage Reference

Component	Value	Units
$Q_3 - Q_4$	18/0.12	μm/μm
$M_{15} - M_{17}$	10/5	μm/μm
$M_{21} - M_{22}$, M_{25}	10/5	μm/μm
M_{18}	0.7/0.7	μm/μm
$M_{19} - M_{20}$	10/5	μm/μm
$M_{23} - M_{24}$	10/2	μm/μm
$R_1 - R_2$	11.9	kΩ
$R_3 - R_4$	10	kΩ
R_5	3	kΩ
R_{LP}	10	kΩ
C_{LP}	11.4	pF
$C_{C1} - C_{C2}$	1.7	pF

a self-biasing tail current. This produces a tail current that is proportional to the currents through both legs in the core of the voltage reference. Transistor M_{26} provides a startup current for the self-biasing circuit, with V_{START} generated in the bandgap circuit as shown in Figure 3.4. Transistors $M_{21} - M_{22}$ are sized to have identical gate and drain voltages as $M_{15} - M_{16}$ in the core of the reference generator shown in Figure 3.4. This reduces the input offset of the amplifier that is caused by the finite output resistances of those transistors.

3.4 Layout

Figure 3.6 shows the layout of the proposed design. Table 3.5 shows the area of each block of the regulator. Excluding the pads, the active area of the design requires an area of about 0.34mm^2, with the power transistor consuming the greatest amount of the total area.

The accuracy of the regulator is largely determined by the matching of all differential pairs and current mirrors in the design. All such transistors were carefully placed to optimize matching between corresponding transistors. The layout of the power transistor and traces

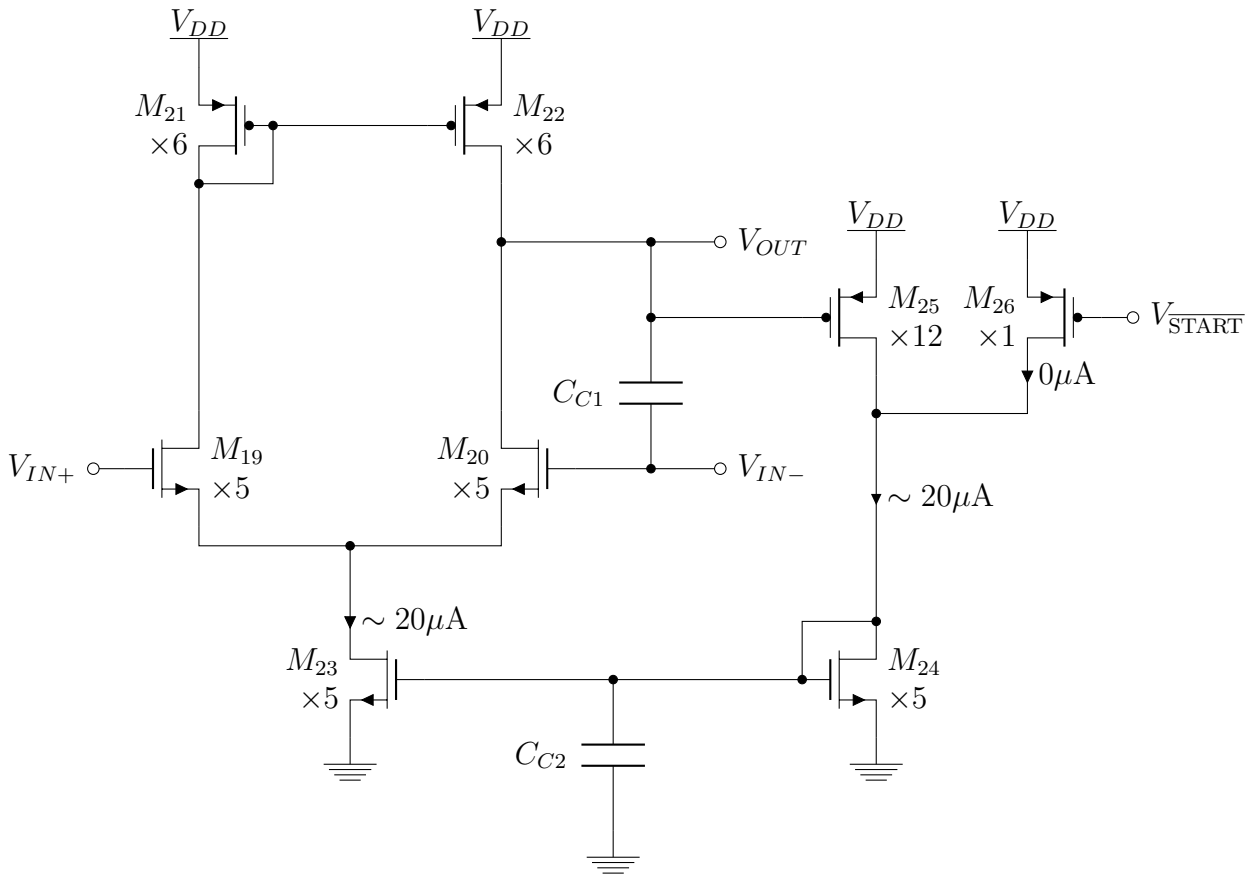


Figure 3.5: Bandgap Amplifier Schematic

Table 3.5: Area Usage in the LDO Regulator

Component	Width (μm)	Height (μm)	Area (mm^2)
Power Transistor	750	200	0.150
Error Amplifier	200	150	0.030
Bandgap Reference	300	150	0.045
Total	750	450	0.340

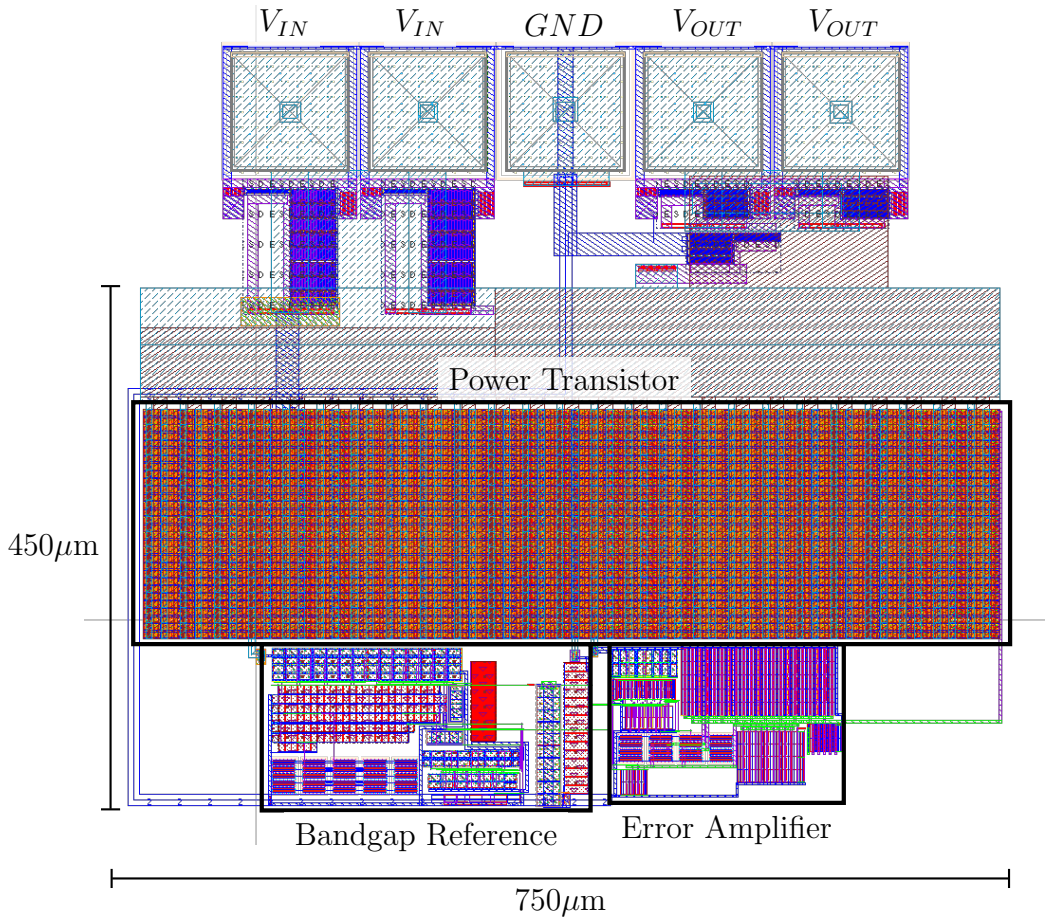


Figure 3.6: The Layout of the LDO Regulator

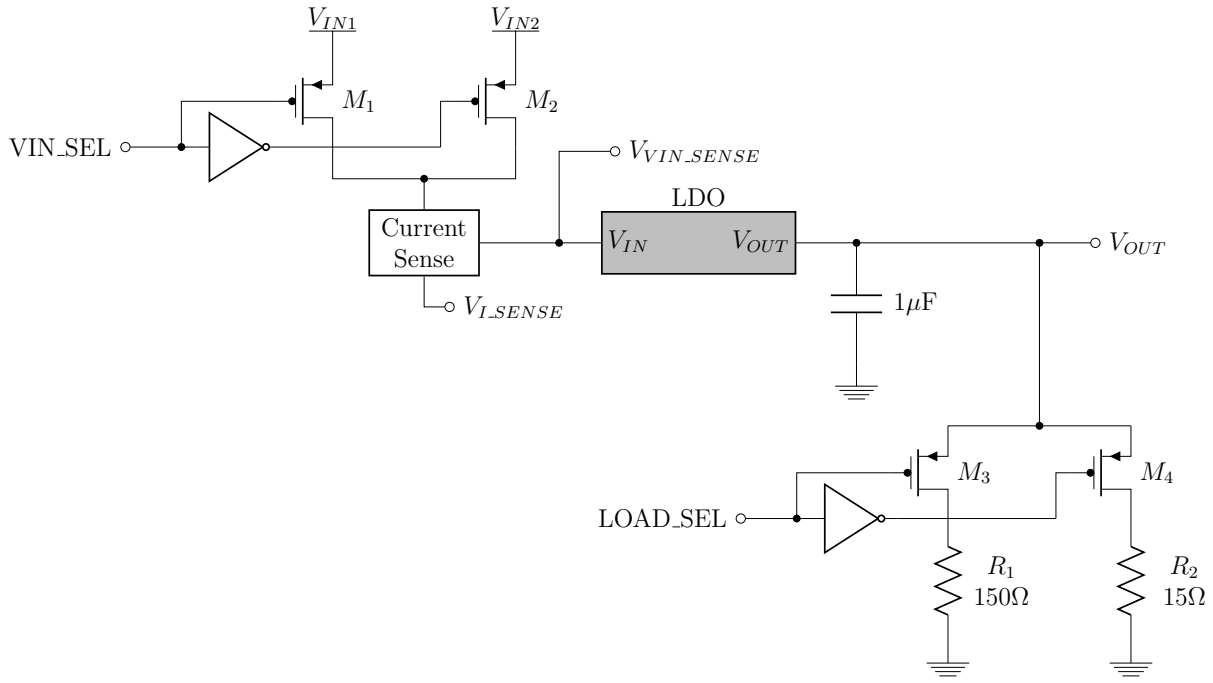


Figure 3.7: Schematic of the LDO Test Setup

that carry the load current is very critical to the performance of the regulator. Any resistance on the V_{IN} trace can reduce the voltage headroom, while resistance on the V_{OUT} trace can add directly to the load regulation measurement. In this layout, all available layers are used to route these traces over the power transistor. Large traces are used in the top two layers to carry the load current to the input and output pads, as these layers exhibit lower resistance than the lower layers.

3.5 Regulator Test Setup

A printed circuit board (PCB) was developed to fully test the capabilities of the proposed LDO. A schematic of the test setup is shown in Figure 3.7. This circuit has been designed to support the testing of all LDO characteristics discussed in Section 2.1.

Transistors $M_1 - M_4$ are power transistors that are used to switch between two input voltages and two loads. These should be power transistors that are capable of passing 100mA with a low on resistance.

The VIN_SEL signal controls the selection of input voltages, allowing for load regulation measurements. The LOAD_SEL signal controls the selection of the load and allows for load regulation and supply variation measurements. The values for R_1 and R_2 have been selected such that the load current will be roughly 10mA and 100mA, respectively. C_1 is used for decoupling with the minimal specifications shown in the figure. This capacitor will also be present in the end-application.

To facilitate quiescent current measurements, the current sense circuit is added before the input of the LDO. This circuitry will be necessary for accurate quiescent current measurements, as the series resistance of the digital multimeter (often listed as the "Burden Voltage" in the user manual) will cause a relatively large voltage drop at 100mA, affecting the performance of the LDO. This particular LDO was designed to have a quiescent current that varies with load current, so it is insufficient to simply measure the current consumption with the load disconnected.

3.5.1 PCB Layout

Appendix A shows the schematic of PCB for the test setup. Figure 3.8 shows the layout of the PCB. The PCB was designed in a single layer with all surface mount components to ease production of the board. As shown in Figure 3.9, the LDO regulator die was wirebonded to the PCB. The five wirebonds in the top left corner of Figure 3.9 connect the input, ground, and output of the regulator to the PCB. The lowest wirebond optionally connects

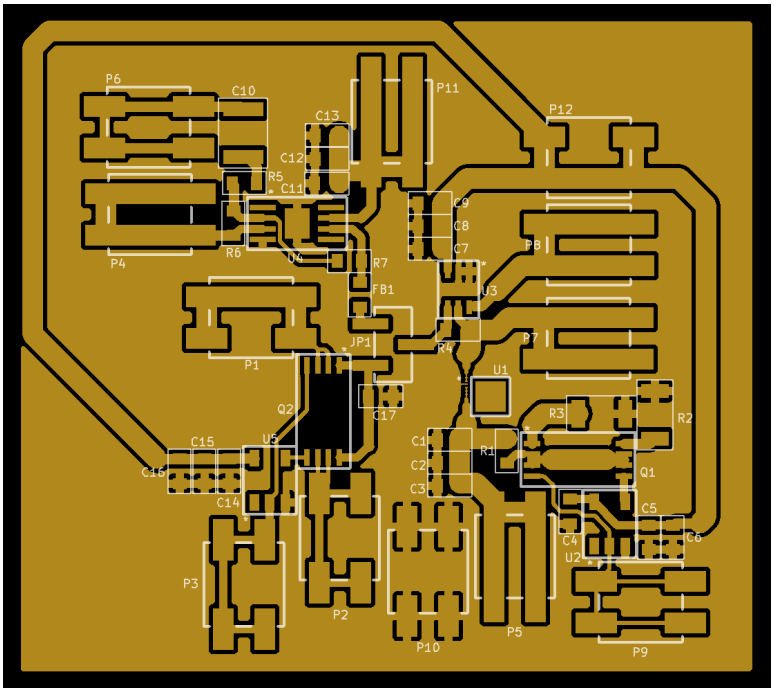


Figure 3.8: PCB Layout for the LDO Test Setup

an RF amplifier that is also present on the die to the output of the regulator to test the operation of the regulator under a more realistic load.

3.5.2 Test Setup Measurements

Using the proposed test setup, the LDO can be fully characterized with the exception of the power supply rejection. The following sections discuss the methodology for each measurement.

Quiescent Current

Figure 3.10 shows how the test setup in Figure 3.7 can be used to measure the quiescent current. Both a constant input voltage and constant load are connected to the LDO while the I_{I_SENSE} output is measured with a multimeter or oscilloscope. The I_{I_SENSE} output

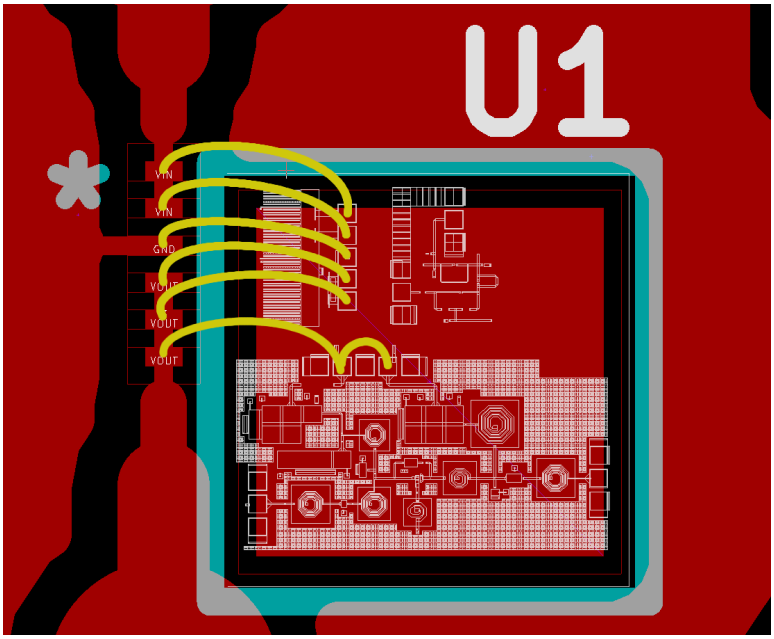


Figure 3.9: Wirebond Diagram for the LDO Test Setup

is provided by current sense circuitry, as shown in Figure 3.7, that measures the current flowing into the LDO and provides a proportional voltage output. The LOAD_SEL input can be used to switch between load currents of 10mA and 100mA to determine the quiescent current at each operating point.

Load Regulation

The proposed test setup can be used to measure the load regulation as shown in Figure 3.11. The LOAD_SEL input is used to switch the load current between 10mA and 100mA, while the output voltage is measured with a DMM or oscilloscope. The change in load current can be calculated as

$$\Delta I_{LOAD} = \frac{V_{OUT2}}{R_2} - \frac{V_{OUT1}}{R_1}, \tag{3.2}$$

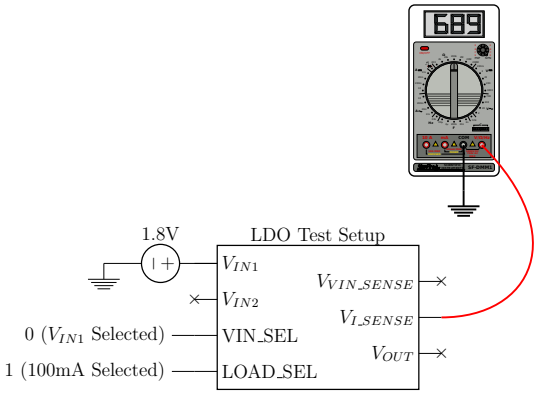


Figure 3.10: Measurement of the Quiescent Current

where R_1 and R_2 are the resistors used to make the load in Figure 3.7 and V_{OUT1} and V_{OUT2} are the output voltage measurements that were taken ($\Delta V_{OUT} = V_{OUT1} - V_{OUT2}$). This allows for the load regulation measurement to account for errors in the resistance values of the load resistors, and removes the need for a current sense circuit in series with the load.

Line Regulation

The proposed test setup can be used to measure the line regulation as shown in Figure 3.12. The LOAD_SEL input is used to switch the input voltage between 1.8V and 1.9V to achieve $\Delta V_{IN} = 0.1V$. The output voltage can then be measured for each of these input voltages to determine ΔV_{OUT}. For improved accuracy, the input voltage is measured at V_{VIN_SENSE} to avoid errors due to the switching transistors and the current sense circuitry. It should be noted that the line regulation measurement is limited by the precision of the voltmeter or oscilloscope used to take the measurement. With ΔV_{OUT} the best measurable line regulation is $1 - 2^{\mathrm{mV}}/\mathrm{V}$ assuming the measurement device has a precision of 1μV.

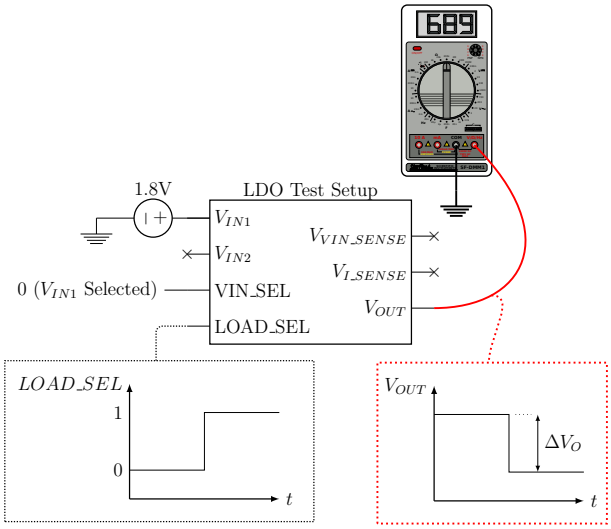


Figure 3.11: Measurement of Load Regulation

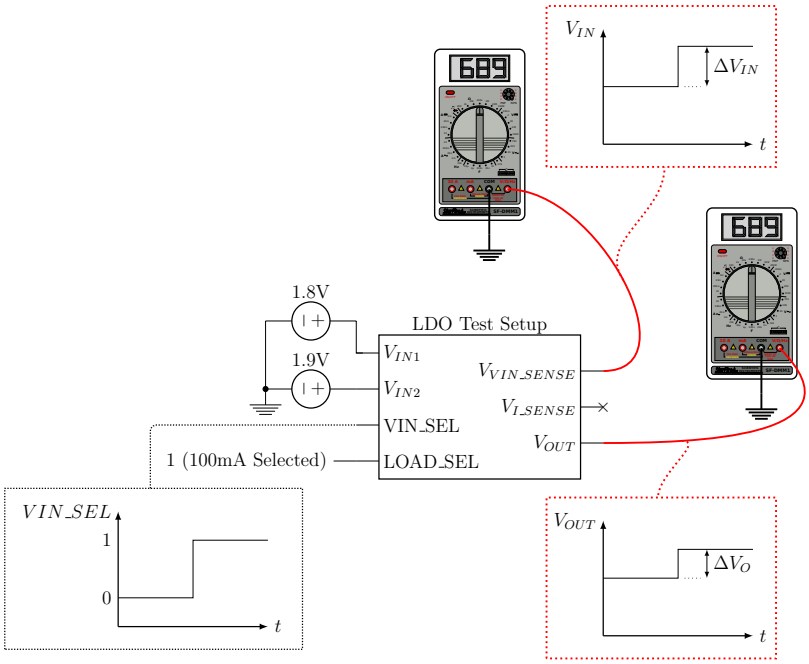


Figure 3.12: Measurement of Line Regulation

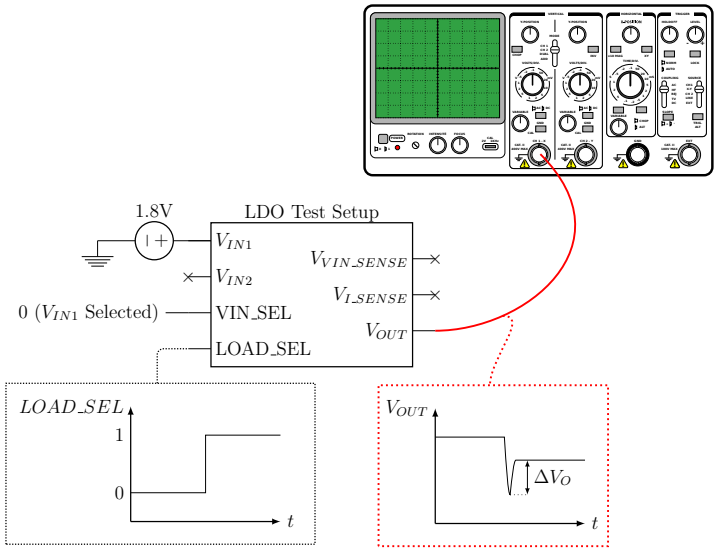


Figure 3.13: Measurement of Supply Variation and Recovery Time

Transient Supply Variation and Recovery Time

The proposed test setup can be used to measure the supply variation and recovery time of the LDO as shown in Figure 3.13. This measurement is very similar to the load regulation test, except that transient data is taken rather than DC measurements. The LOAD_SEL input is used to quickly switch the load between I_{MIN} and I_{MAX}, and the output voltage is measured with an oscilloscope. The supply variation can then be extracted from the output voltage vs. time waveform as the peak change in output voltage. The recovery time can also be extracted from the same waveform as the time difference between the load current pulse edge and the time at which the output has settled to within 1% of the final value. This test can be repeated with a high-to-low transition in LOAD_SEL to determine the transient response to a sudden reduction in load current.

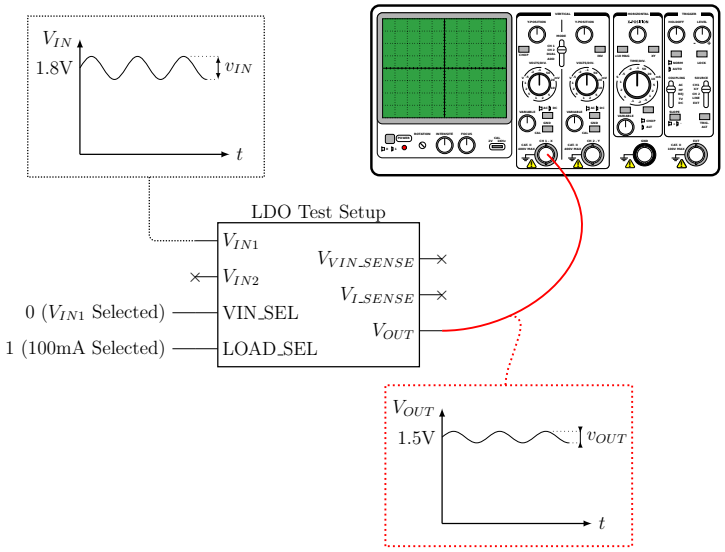


Figure 3.14: Measurement of the Power Supply Rejection

Power Supply Rejection

The proposed test setup can be used to measure the power supply rejection as shown in Figure 3.14. A small ripple is added to the input of the regulator, and the resulting ripple at the output is measured. The power supply rejection can then be calculated as the ratio in the amplitude of the output ripple to the amplitude of the input ripple as discussed in Section 2.1.4. Unfortunately, this method of measuring the power supply rejection is vulnerable to noise while measuring the small ripple at the output, and requires a function generator that can source 100mA of DC current and a sine wave simultaneously. However it is the method which uses the most readily available equipment.

The PCB presented here includes an additional method of measuring power supply rejection that uses a high power operational amplifier to combine the DC and ripple components, allowing for the use of a spectrum analyzer to obtain the full power supply rejection curve and removing the need for a function generator that can source large DC currents [28]. This

requires a spectrum analyzer that has high impedance inputs and is capable of operation at very low frequencies. This circuitry has not been tested due to the unavailability of the required spectrum analyzer and thus will not be discussed further in this paper.

3.6 Results

The proposed LDO regulator was implemented in the IBM 8HP 0.13μm BiCMOS process. Figure 3.15 shows the simulated loop gain of the regulator for the FF corner with $R_{ESR} = 1\Omega$. As shown, the regulator exhibits a loop gain of 83° when $I_L = 100\text{mA}$. For $I_L = 5\text{mA}$, the stability of the regulator degrades due to excess phase shift between 10kHz and 100kHz, however the regulator maintains stability with a minimum phase margin of 50°. The reduction in phase is expected, and is caused when the pole at the output of the error amplifier moves to the left of the LHP zero due to the dynamic biasing of the amplifier.

Figure 3.16 shows the measured output voltage of the regulator. The regulator exhibits load and line regulations of $92^{\text{mV}}/_{\text{A}}$ and $2^{\text{mV}}/_{\text{V}}$, respectively. When the load is placed off-chip, as in the test setup used for these measurements, the resistance of the bondwire degrades the load regulation measurement. It is expected that when the load is integrated with the regulator, the load regulation will improve in the absence of these parasitic resistances. As discussed in Section 3.5.2, the line regulation measurement is limited by the precision of the oscilloscope used to make the measurements.

Interestingly, Figure 3.16 indicates that the output voltage decreases as the input voltage is increased above 2.2V. This is likely caused by the positive feedback created by the dynamic biasing in the error amplifier. The DC power supply rejection can also be estimated from Figure 3.16 as at least -54dB. A similar result was obtained by applying a 100mV_{pp} sine wave of 100Hz to the input of the regulator and measuring the ripple at the output as

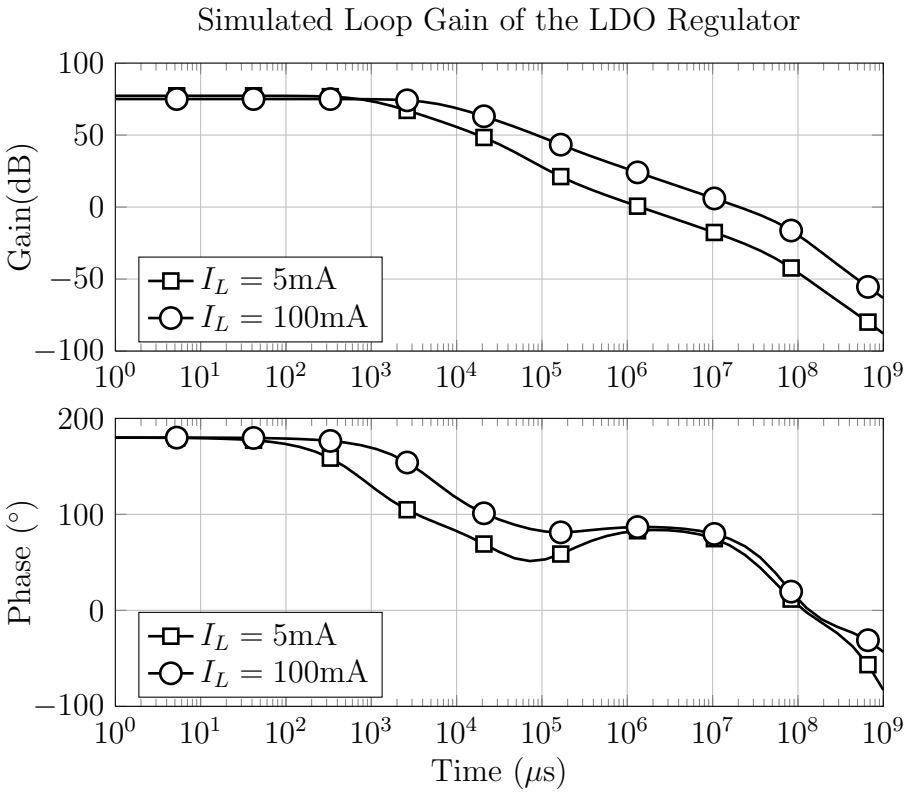


Figure 3.15: Simulated Loop Gain of the Regulator

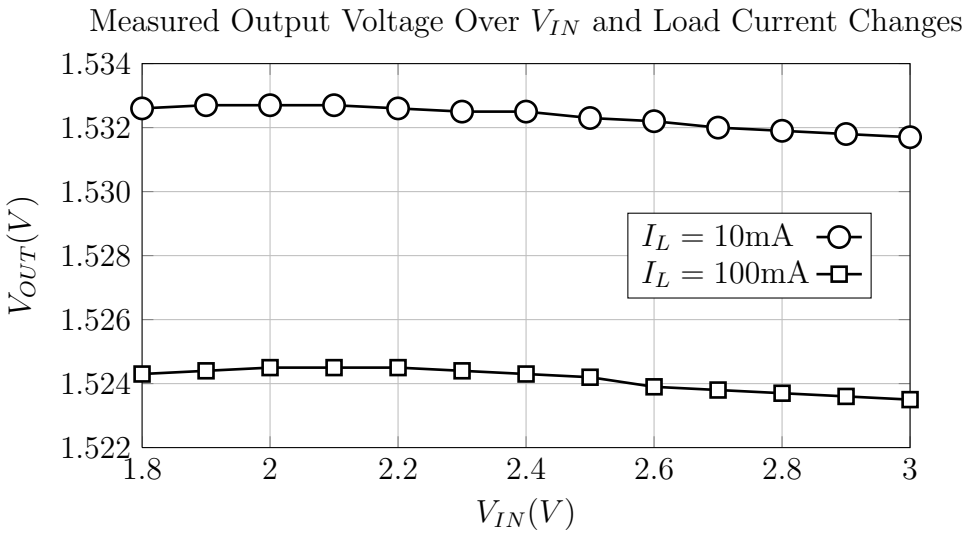


Figure 3.16: Measured Output Voltage of the LDO Regulator

discussed in Section 3.5.2. These methods of measuring PSR are limited by the noise and precision limitations of the measurements taken from the test setup. For a regulator with high PSR, the measured ripple at the output will not be much larger than the noise in the system, significantly impacting the PSR measurement. Making the ripple at the input larger can mitigate this issue by creating a larger ripple at the output, however, such a measurement would include undesired large-signal effects which could further degrade the precision of the measurement. Thus, it is possible that the power supply rejection is better than the measured value, however the current test setup is unable to measure smaller values of ripple.

Figure 3.17 shows the transient response of the regulator when the load current is switched from 10mA to 100mA. Similarly, Figure 3.18 shows the transient response of the regulator when the load current is switched from 100mA to 10mA. The overshoot and undershoot due to the change in load current are limited to 40mV and 48mV, respectively. The output voltage recovers to within 1% of the final value within 96ns.

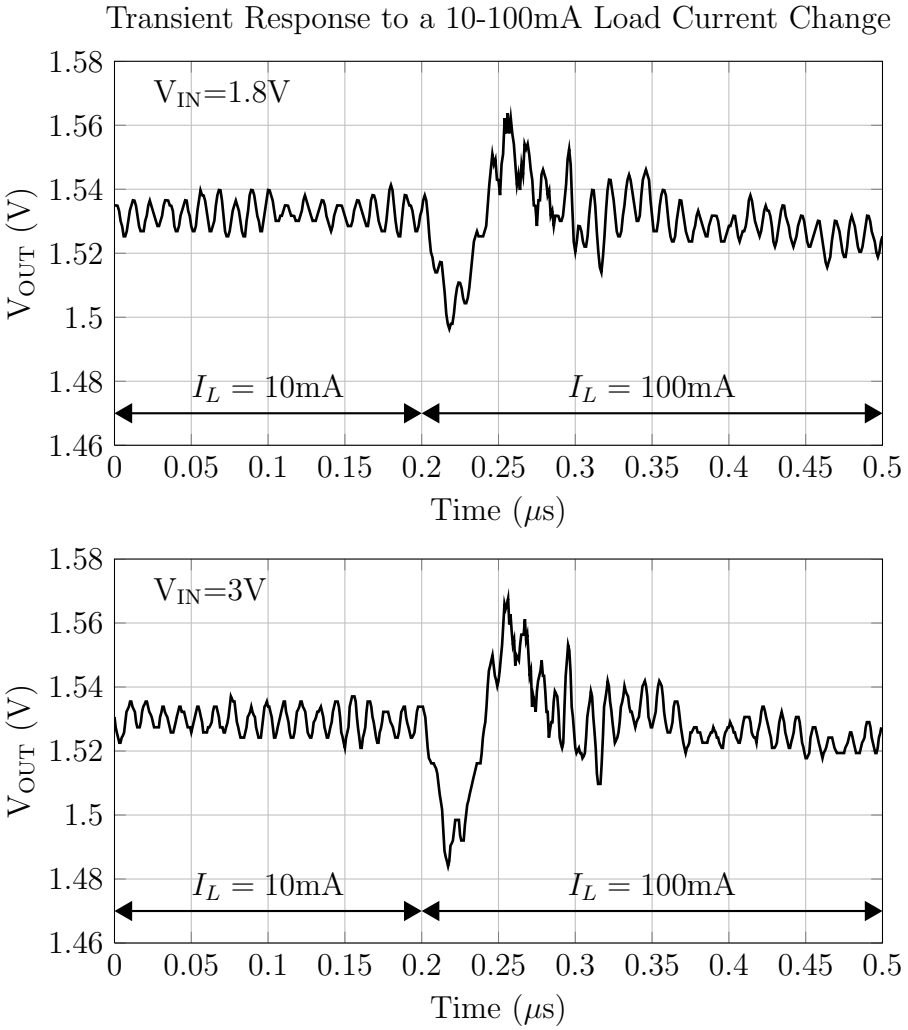


Figure 3.17: Measured Transient Response to $10 - 100$mA Load Change

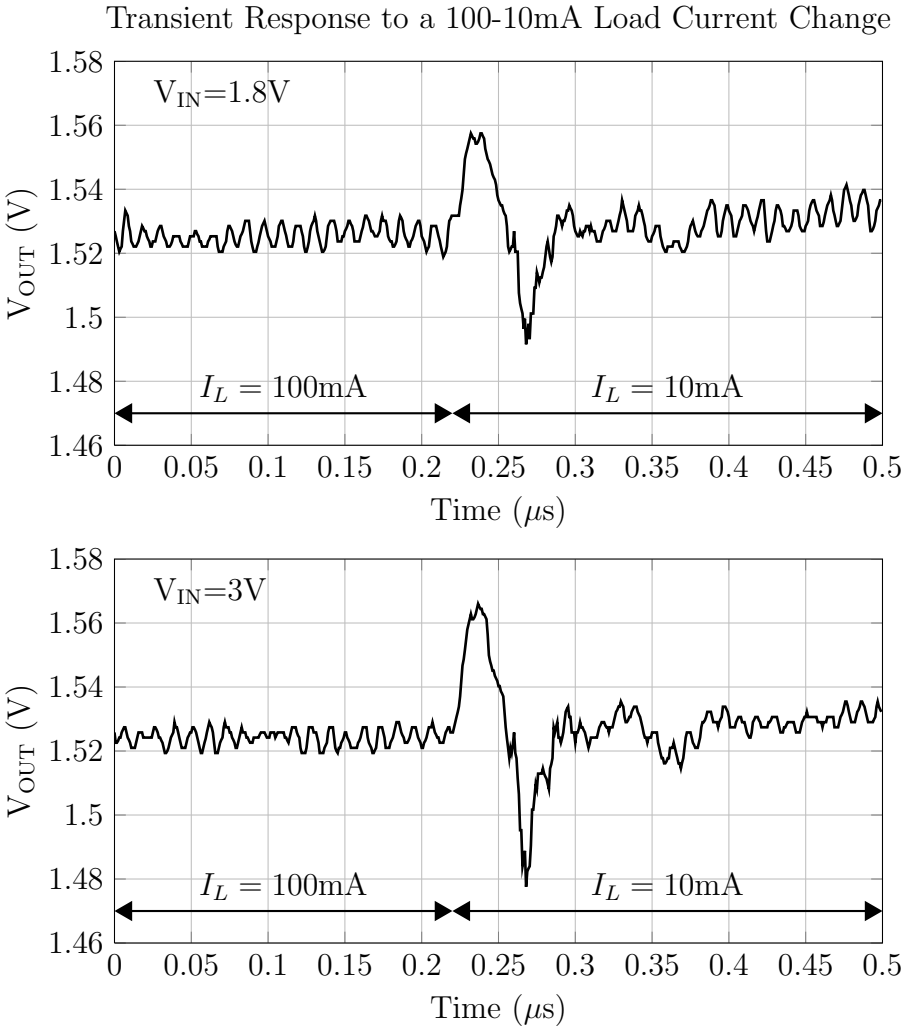


Figure 3.18: Measured Transient Response to $100 - 10$mA Load Change

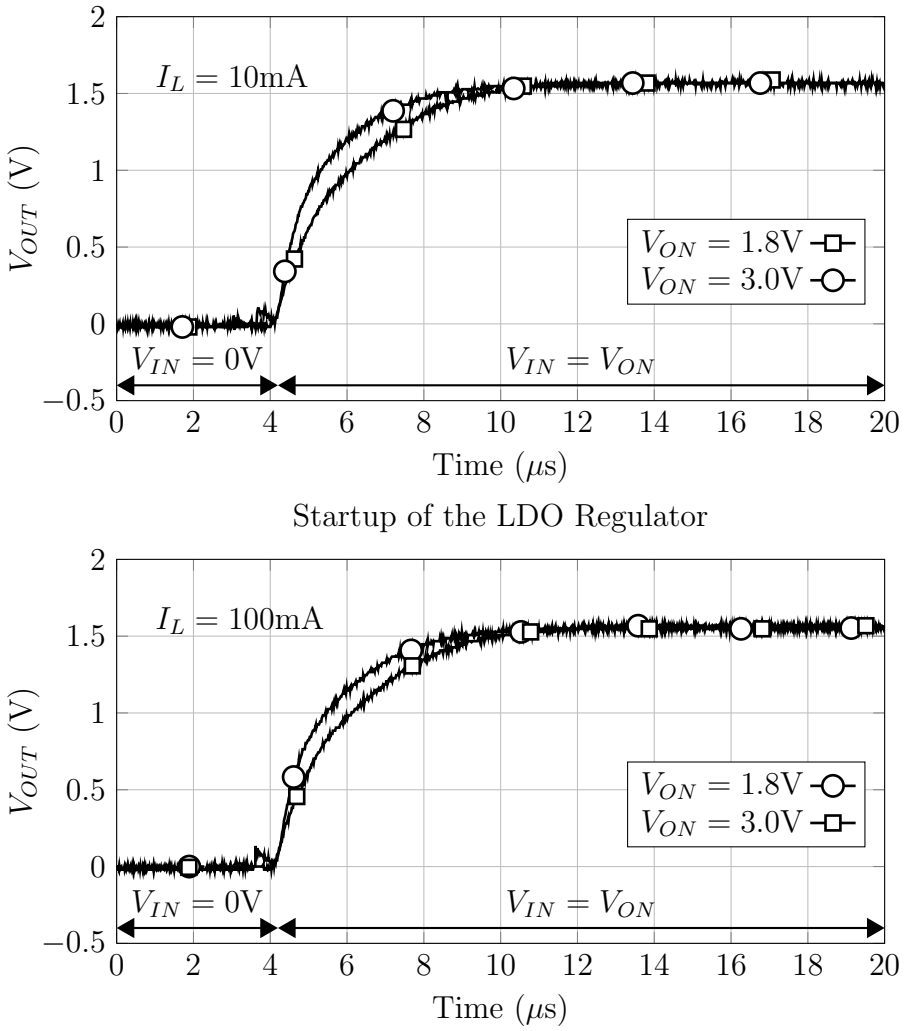


Figure 3.19: Startup Response of the LDO Regulator

Figure 3.19 shows the output of the regulator when the input voltage is switched on. As shown, the turn-on time of the regulator is about 12μs for both low-load and high-load cases. Furthermore, there is no overshoot present at the output, indicating that there are no stability or startup issues in the regulator.

A summary of the results for the regulator design is given in Table 3.6. Except for the line regulation and power supply rejection measurements, which are limited by the

Table 3.6: Summary of Measured Results

Parameter	Specification	Measurement	Units
Input Voltage	$1.8 - 3$	$1.8 - 3$	V
Max. Load Current	100	100	mA
Output Voltage	1.5	1.5	V
Transient Variation	± 100	$+40/-48$	mV
PSR @ 100Hz	> 55	54	dB
Recovery Time	< 100	96	ns
Accuracy	3	2.2	%
Quiescent Current	3	1.04	mA
Load Regulation	100	92	$^{\mathrm{mV}}/_{\mathrm{A}}$
Line Regulation	1.7	2	$^{\mathrm{mV}}/_{\mathrm{V}}$

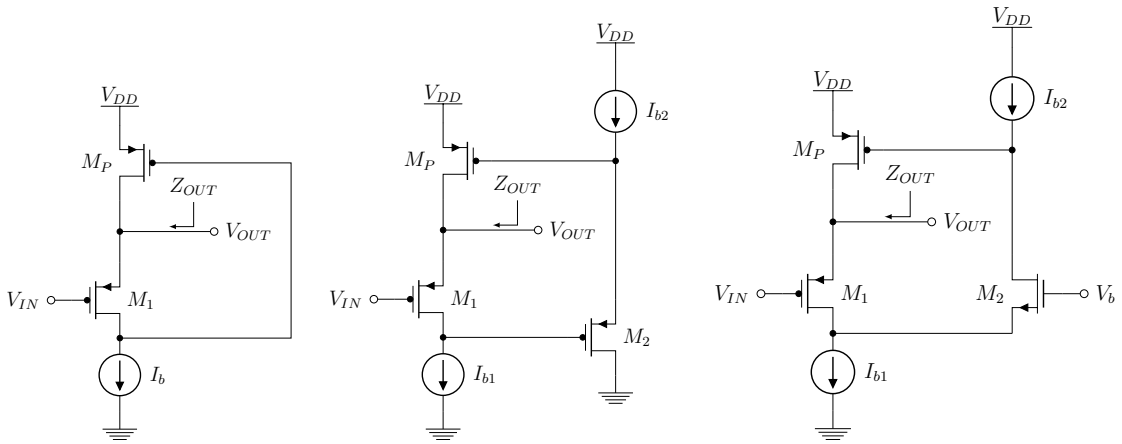
available precision of the test setup, the conventional architecture was able to meet all design specifications for the regulator.

CHAPTER 4

FAST-TRANSIENT OUTPUT CAPACITOR-FREE DESIGN

As semiconductor processing scales to lower process nodes, an increasing amount of circuits are being integrated onto a single chip. Consequently there is a desire to integrate more regulators into such systems. This could allow several power domains that can be chosen to best suit the circuits that each regulator is driving. Furthermore, providing independent power domains to major blocks in sensitive circuits, such as those on an RF chip, can mitigate cross-talk between those blocks, thus improving system performance. For these reasons, it is desired to develop LDO regulators that do not need an output capacitor. Furthermore, to be practical in high-performance applications, such output capacitor-free regulators should exhibit performance on par with those of the conventional design.

The following sections propose an output capacitor-free LDO regulator design based on the flipped voltage follower that is capable of achieving performance on par with conventional LDO regulator designs. Section 4.1 provides a background on FVF-based regulators, while Sections 4.2 and 4.3 improve upon previous FVF-based designs by improving the loop gain, accuracy, and transient variations. Finally, Section 4.5 gives simulation results that verify the performance of the design.



(a) FVF (b) LSFVF (c) CAFVF

Figure 4.1: Schematic of the Flipped Voltage Follower

4.1 Flipped Voltage Follower LDO Regulators

The flipped voltage follower, shown in Figure 4.1a, is an analog buffer designed for reduced output impedance [4]. Transistor M_1 is placed in a cascode configuration with the bias current, I_b, to form a gain stage. That gain stage is then used to regulate M_P to provide the necessary current to V_{OUT} to ensure that the current through M_1 remains constant.

Assuming $g_{m1}r_{ds1} \gg 1$ and $g_{mP}r_{dsP} \gg 1$, the DC gain of the flipped voltage follower is given as $1^{V}/_{V}$. Ignoring parasitic capacitances, the output impedance of the flipped voltage follower is determined as

$$Z_{OUT} = \frac{1}{g_{m1}g_{mP}r_{ds1}}. \tag{4.1}$$

Thus, the flipped voltage follower exhibits a better output impedance than the conventional source follower by a factor of $^{1}/_{g_{mP}r_{ds1}}$. Furthermore, it achieves this improvement without additional quiescent current.

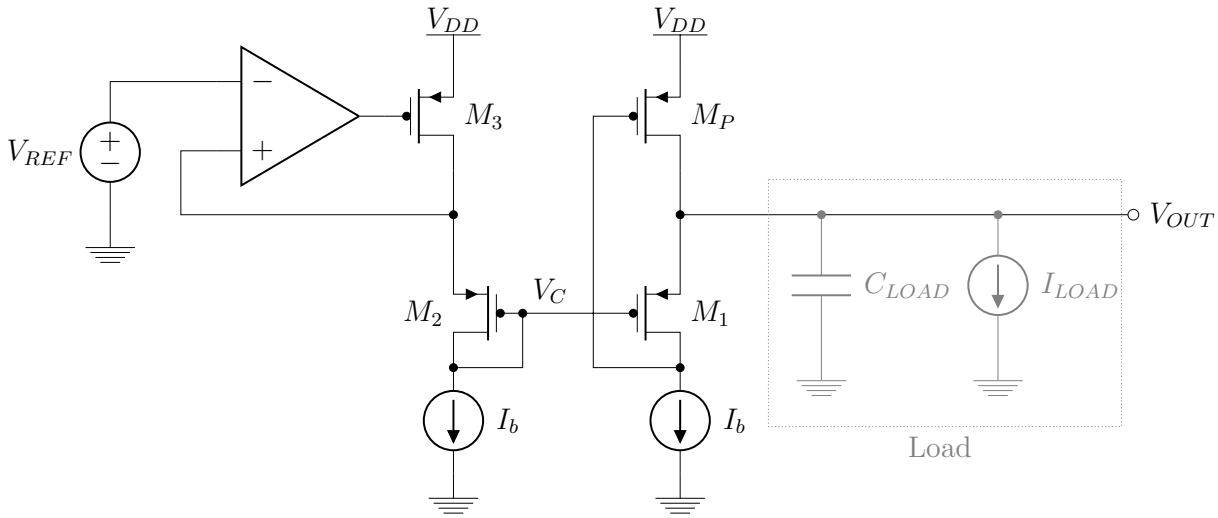


Figure 4.2: Schematic of an FVF-based LDO Regulator

By generating the appropriate input voltage for the FVF, it can be used as an LDO regulator [23]. The generation of this control voltage can be accomplished with the addition of a mirror device and a voltage buffer as shown in Figure 4.2. Assuming M_1 and M_2 are the same size, and ignoring their finite output resistances, the circuit in Figure 4.2 will set V_C such that $V_{OUT} = V_{REF}$. The result is a very compact regulator that can be designed such that it requires no external capacitor, and thus can be fully integrated on to a chip.

The design of the FVF becomes more difficult when used as an LDO regulator than in typical analog systems. Section 4.1.1 analyzes the loop gain and accuracy of the FVF-based regulator, while Sections 4.1.2 and 4.1.3 analyze the stability and transient response of such regulators, respectively.

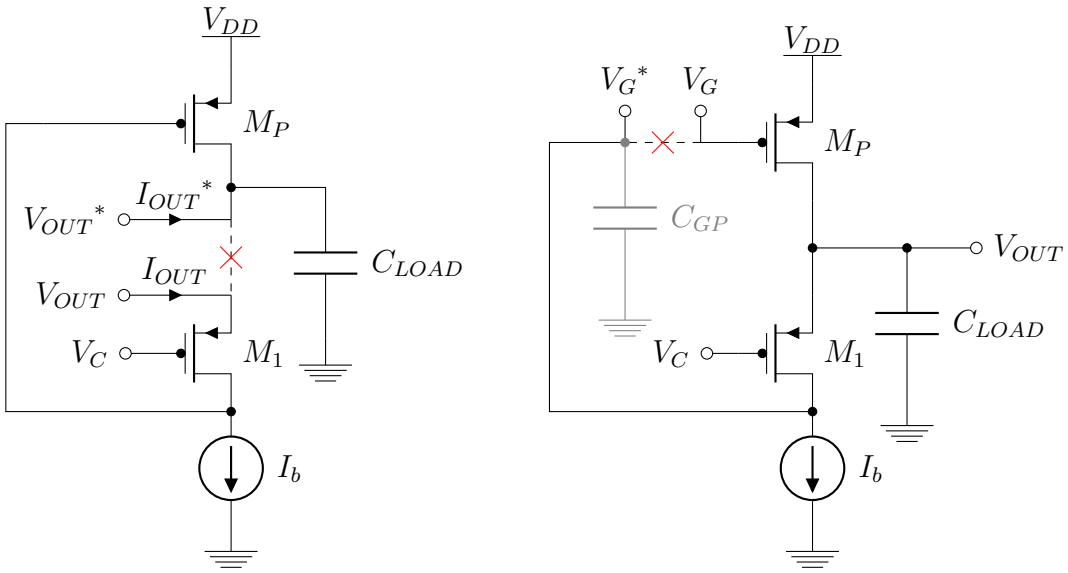
4.1.1 Loop Gain and Accuracy

Although the FVF-based regulator is a simple architecture, calculating an exact loop gain by hand is a difficult task. Such an analysis would need to include the loading effects of the

different parts of the circuit, resulting in complexities significant enough to usually relegate this task to simulation [30]. To gain intuition into the design of the regulator, it is therefore desired to develop an approximate analytical expression for the loop gain. Generally, this is accomplished by breaking the loop at a node, applying a test signal to that node, and determining the returned signal. However, breaking the loop at a node in such a manner will remove the loading effects between the circuits on each side of the broken node. Thus, the node at which to break the loop should be carefully chosen to ensure that the inaccuracies due to the removal of these loading effects is negligible.

The use of a voltage or current as the test signal for measuring the loop gain should be chosen to mimic the loading of the circuits on each side of the broken node. Generally, a voltage source should be used for driving a high impedance node, and a current source should be used to drive a low impedance node. For the FVF-based regulator, this choice is not so simple. Figure 4.3a shows the FVF-based regulator with the loop broken at V_{OUT}. The impedance seen looking into V_{OUT} is the parallel of r_{dsP} and the impedance looking into M_1, which is approximately given as $1/g_{m1}$. At high load currents, $r_{dsP} \ll 1/g_{m1}$, indicating that a voltage source should be used to drive the test signal at V_{OUT} [7]. However at low load currents, r_{dsP} is close to $1/g_{m1}$, making a voltage or current source inadequate approximate the load conditions between V_{OUT} and V_{OUT}^*, thus resulting in excessive inaccuracies in the determined loop gain.

Alternatively, the loop of the FVF-based regulator can be broken at the gate of M_P as shown in Figure 4.3b. Because the gate of M_P presents a very high impedance, only a voltage source should be used to drive the test signal. This configuration would ignore the effect of C_{gsP} as well as the effective Miller capacitance created by C_{gdP}. However, these parasitic capacitances can be lumped together into one capacitance, C_{GP}, at the V_G^* node as shown.



(a) Breaking the Loop at V_{OUT}

(b) Breaking the Loop at Gate of M_P

Figure 4.3: FVF Regulator Loop Gain Analysis

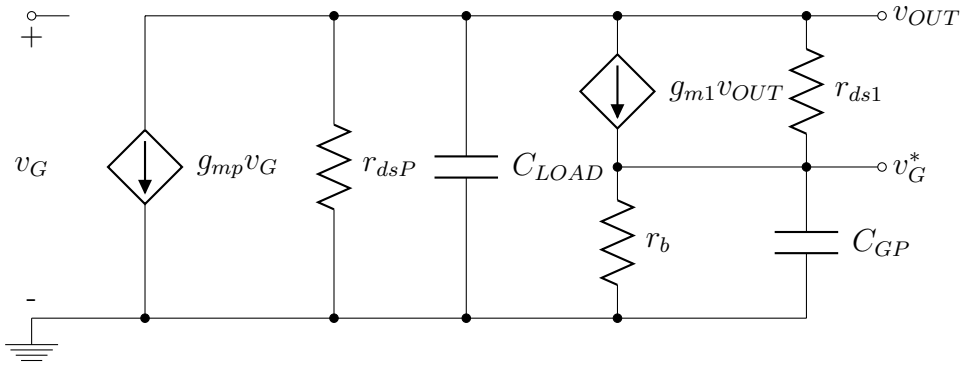


Figure 4.4: Small-signal Model

Thus the poles caused by such capacitances will be included in the loop gain analysis. The Miller capacitance will also create an RHP zero and move the non-dominant pole to higher frequencies [17, 30]. Due to the large transconductance of M_P, the zero will be located at a frequency much higher than the unity-gain bandwidth of the regulator, thus making it negligible. The movement of the non-dominant pole to higher frequencies will only improve the stability of the regulator, making it safe to ignore for the purposes of this analysis.

Figure 4.4 shows the small signal model of the FVF-based regulator with the loop broken at the gate of M_P as shown in Figure 4.3b. The output resistance of the current source is modeled as r_b. Assuming $g_{m1}r_{ds1} \gg 1$, the loop gain of the regulator can be determined from the signal signal model as

$$A_L = \frac{v_G^*}{v_G} = \frac{A_{L,DC}}{a_{p2}s^2 + a_{p1}s + 1}, \tag{4.2}$$

where $A_{L,DC}$, a_{p1}, and a_{p2} are given as

$$\begin{aligned} A_{L,DC} &= -g_{mP}\frac{g_{m1}r_{ds1}r_{dsP}r_b}{r_{ds1}+r_b+g_{m1}r_{ds1}r_{dsP}} \\ &= -g_{mP}\left[g_{m1}(r_b \parallel r_{ds1})r_{dsP} \parallel r_b\right] \end{aligned} \tag{4.3}$$

$$\begin{aligned} a_{p1} = &\left[(r_{ds1} + g_{m1}r_{ds1}r_{dsP}) \parallel r_b\right] C_{GP} \\ &+ \left[\frac{r_{ds1}+r_b}{g_{m1}r_{ds1}} \parallel r_{dsP}\right] C_{LOAD} \end{aligned} \tag{4.4}$$

$$a_{p2} = \frac{r_{ds1}r_b r_{dsP}}{r_{ds1} + r_b + g_{m1}r_{ds1}r_{dsP}} C_{GP}C_{LOAD}. \tag{4.5}$$

The frequency response of the FVF-based regulator will be discussed in detail in Section 4.1.2. Assuming r_b is large compared to r_{ds1}, the loop gain is optimistically determined by the cascaded intrinsic gains of M_P and M_1. This may be inadequate to achieve the desired regulation specifications, especially at lower process nodes where the transconductance and drain-source resistance of the transistors is degraded. As the power transistor is designed to meet the load current requirement, the DC loop gain can only be increased by increasing the

intrinsic gain of M_1. This necessitates the use of high current and a large device to achieve the desired DC loop gain.

The flipped voltage follower also suffers from limited voltage headroom, which can further degrade the loop gain of the regulator. To keep transistor M_1 in saturation, the control voltage is limited to

$$V_{DD} - V_{dsatP} - 2V_T \leq V_C \leq V_{DD} - V_{dsatP} - V_{dsat1} - V_T, \tag{4.6}$$

where V_{dsat} is the drain to source voltage required to keep the corresponding transistor in the saturation region, and V_T is the threshold voltage of the transistors. Equation (4.6) indicates that the flipped voltage follower has a valid input range of just $V_T - V_{dsat,1}$. Furthermore, the load current at any given time will determine the value of V_{dsatP}, causing the upper and lower limits of V_C to significantly change with load current. Because V_C is set to achieve the desired output voltage, transistor M_1 may enter the triode region when the load current is low, resulting in a significantly reduced loop gain. To overcome this limitation, it has been demonstrated that the gate of M_P can be driven with a source follower, as in the LSFVF. Alternatively, an additional common gate stage can be used to drive the gate of M_P to form a cascaded flipped voltage follower (CAFVF) as shown in Figure 4.1c [29]. While the LSFVF and CAFVF solve the voltage headroom issue they also incur higher current consumption and add additional poles that may degrade the stability of the voltage follower.

The accuracy of the control voltage will have a large impact on the accuracy of the FVF-based regulator. As shown in Figure 4.2, an additional voltage buffer and mirroring device must be placed in between the reference voltage and the regulator loop. Any inaccuracies in these circuits will directly translate to errors at the output of the regulator. Furthermore, the FVF regulator will suffer from a systematic offset due to the mirroring device used to generate the control voltage. The drain voltages of M_1 and M_2 will not be equal, resulting

in an offset at the output due to the finite output resistance of those transistors. This will degrade the accuracy of the regulator, even if M_1 and M_2 are perfectly matched.

4.1.2 Stability

As shown in Equation (4.2), the loop gain of the FVF-based regulator exhibits two poles that must be designed to ensure the stability of the regulator. To achieve stability, the two poles should be real and widely separated, allowing the denominator of Equation (4.2) to be approximated as

$$a_{p2}s^2 + a_{p1}s + 1 = \left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right) = \frac{s^2}{\omega_{p1}\omega_{p2}} + \frac{s}{\omega_{p1}} + 1, \tag{4.7}$$

where ω_{p1} and ω_{p2} are the angular frequencies of the dominant, and non-dominant poles, respectively. Solving for ω_{p1} and ω_{p2} yields

$$\omega_{p1} = \frac{1}{a_{p1}} = \frac{1}{\left[(r_{ds1} + g_{m1}r_{ds1}r_{dsP}) \parallel r_b\right] C_{GP} + \left[\frac{r_{ds1}+r_b}{g_{m1}r_{ds1}} \parallel r_{dsP}\right] C_{LOAD}} \tag{4.8}$$

$$\omega_{p2} = \frac{a_{p1}}{a_{p2}} = \frac{1}{\omega_{p1}a_{p2}} = \frac{1}{(r_{ds1} \parallel r_b)\, C_{GP}} + \frac{1}{\left(\frac{1}{g_{m1}} \parallel r_{dsp}\right) C_{LOAD}}. \tag{4.9}$$

To obtain a more intuitive understanding of the poles in (4.8) and (4.9), it helps to consider the nodes at which the poles are created. One of the poles is formed at the output, and is created by C_{LOAD} and the parallel of the resistance seen looking into the drain of M_P (r_{dsP}), and the resistance seen looking into the source of M_1. The other pole is formed at the gate of M_P and is formed by C_{GP} and the parallel of the resistance seen looking into the drain of M_1 and the resistance of the current source r_b. For the FVF-based regulator with a low load capacitance, the dominant pole, ω_{p1} will be formed at the gate of M_P, making the C_{LOAD} term in the denominator of (4.8) negligible. Similarly, the non-dominant pole, ω_{p2} will be formed at the output node, making the $1/C_{GP}$ term in (4.8) negligible. The poles can

then be approximated as

$$\omega_{p1} \approx \frac{1}{\left[\left(r_{ds1} + g_{m1} r_{ds1} r_{dsP}\right) \parallel r_b\right] C_{GP}} \tag{4.10}$$

$$\omega_{p2} \approx \frac{1}{\left(\frac{1}{g_{m1}} \parallel r_{dsp}\right) C_{LOAD}}. \tag{4.11}$$

It is important to note that, assuming r_b is large compared to r_{ds1}, increasing g_{m1} will move ω_{p1} to lower frequencies, while moving ω_{p2} to higher frequencies. Thus, the FVF-based regulator can be stabilized by designing g_{m1} such that there is sufficient separation between the two poles to ensure that ω_{p2} is placed above the unity-gain frequency of the regulator. Alternatively, to further reduce the frequency of the dominant pole, Miller compensation can be added to the FVF-based regulator [13]. The effective Miller capacitance would add directly into C_{GP}, thus decreasing the frequency of the dominant pole. Furthermore, the use of Miller compensation will entails pole splitting, which will cause the non-dominant pole to move to even higher frequencies, improving the stability of the regulator [17, 30].

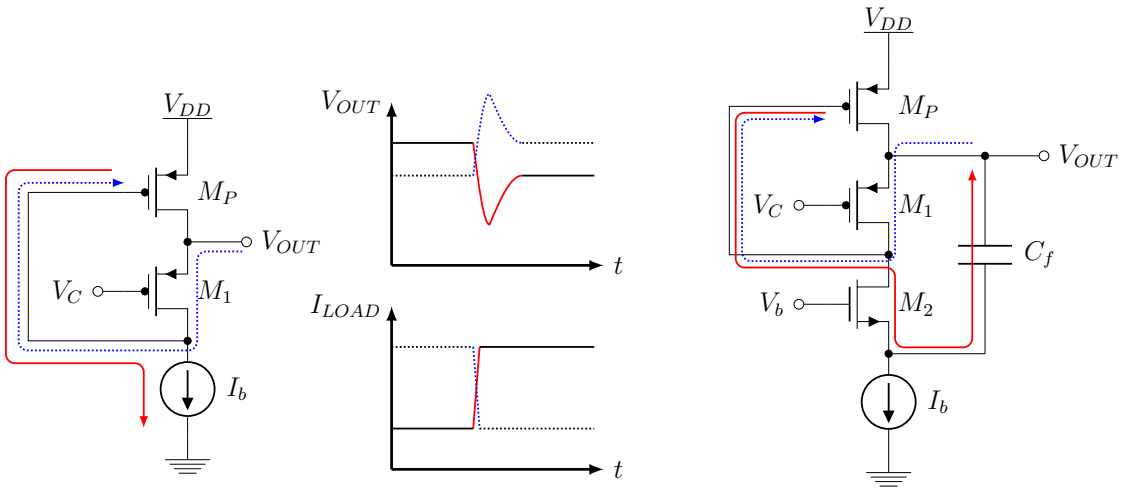
Alternatively, the output node can be chosen to form the dominant pole. In this case, ω_{p2} will be formed at the gate of M_P. However, because the size of power transistor is delegated by the load current requirements, it is difficult to reduce C_{GP}, causing ω_{p2} to also locate to relatively low frequencies. Thus, it is quite difficult to stabilize the basic FVF-based regulator in this configuration. However, ω_{p2} can be moved to sufficiently high frequencies by driving the gate of M_P with a conventional source follower to create a level shifted flipped voltage follower (LSFVF), shown in Figure 4.1b [7,9,29]. The LSFVF architecture effectively reduces the impedance seen at the gate of M_P, thus moving the corresponding pole to much higher frequencies and stabilizing the regulator.

4.1.3 Transient Response

As with most output capacitor-free LDO regulators, the transient response of the FVF-based regulator is severely limited by slewing at the dominant pole. As shown in Figure 4.5a, during positive slewing, current can flow directly from the output node, through transistor M_1 to the gate of M_P, resulting in a large positive slew rate. This indicates that the regulator will have a relatively fast transient response when the load current is switched from high to low. However, when the load current is switched from low to high, negative slewing occurs when transistor M_1 shuts off due to the drop in V_{OUT}, and the maximum current available for discharging the gate capacitance of M_P is I_b. This will result in a very slow transient response when the load current switches from low to high.

The limited slew rate of the FVF-based regulator necessitates the use of slew rate enhancement circuitry as discussed in Section 4. The simplest of such slew rate enhancements is shown in the cascoded FVF regulator of Figure 4.5b [3]. This regulator adds a cascode transistor, M_2, and a capacitor, C_f, to increase or decrease the tail current during large transient swings in V_{OUT}. The capacitor C_f will act like a short when the load current is switched, allowing current to flow from the gate of M_P through M_2 to the output. However, the effectiveness of this approach is limited by the size of C_f and the transconductance of M_2, and this topology still exhibits limited voltage headroom as discussed in Section 4.1.1. This limited voltage headroom will cause M_1 to enter the triode region when there is a sudden rise in V_{OUT}, reducing the transconductance of M_1, and thus reducing the maximum positive slew rate.

While the CAFVF architecture, shown in Figure 4.1c, can improve the voltage headroom for the regulator, the positive slew rate is limited by the current source I_{b2}, resulting in slower transient response compared to the basic FVF architecture. Thus, a more complex



(a) FVF-based Regulator (b) Cascoded FVF Regulator

Figure 4.5: Analysis of slewing in the FVF-based regulator. The solid red and dotted blue lines show the current flow from the gate of M_P when the load current is suddenly increased or decreased, respectively.

slew rate enhancement technique is required. Figure 4.6 shows one such SRE technique [13]. During positive transient swings at the output, current flows through C_1 to increase the current through M_9 which is then mirrored by M_3 to the gate of M_P, resulting in a large positive slew rate. During negative transient swings at the output, the bias current I_b is multiplied by the gain of the common gate stage formed by M_2 and M_7, and mirrored to M_4, resulting in a significant improvement in the negative slew rate. While this technique can significantly improve the slew rate, each current mirror stage has a pole and will that exhibit some propagation delay during fast transient swings. These delays slow down the reaction time of the SRE circuitry, inhibiting this architecture from achieving a transient response performance on par with regulators that use large output capacitors. Furthermore, this SRE technique requires three additional current mirrors that increase the quiescent current of the regulator.

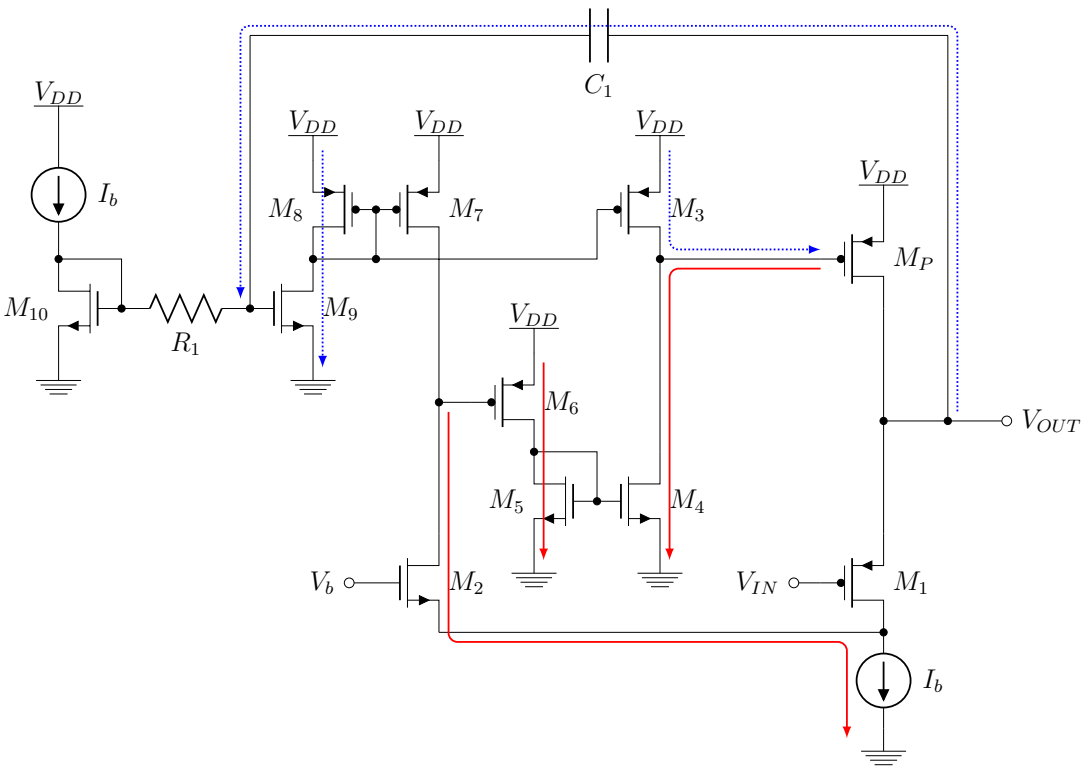


Figure 4.6: The CAFVF regulator with SRE. The solid red and dotted blue lines show the current flow from the gate of M_P when the load current is suddenly increased or decreased, respectively.

4.2 Improving Loop Gain and Accuracy

As discussed in Section 4.1.1, FVF-based regulators typically exhibit low loop gain and poor accuracy due to short-channel effects and limited voltage headroom. Furthermore, the error amplifier used to generate V_C, as shown in Figure 4.2, does not sense the output voltage directly, making it unable to mitigate systematic errors at the output. Placing the amplifier inside the regulation loop as shown in Figure 4.7 can increase the loop gain and accuracy of the regulator by increasing the effective transconductance of M_1. This G_m-boosted FVF (GMB-FVF) regulator also avoids issues caused by the limited voltage headroom by mirroring the current through M_1 to the gate of M_P, thereby allowing a large voltage swing at the gate of M_P while maintaining all devices in the saturation region.

The addition of the amplifier creates a second loop in the regulator as shown in Figure 4.8. Both loops must be analyzed to ensure the stability of the regulator. The main regulation loop is designated by the solid red line in Figure 4.8. It is designated as the main loop because it is analogous to the loop of the FVF-based regulator, and gives the most insight into the regulation characteristics of the circuit. The main loop can be analyzed by breaking the loop at the gate of the power transistor, as done for the FVF-based regulator in Section 4.1.1. The auxiliary loop is shown by the dotted blue line in Figure 4.8, and can be analyzed by breaking the loop at the gate of M_1. If both loops exhibit stable transfer functions, the regulator will be stable [11]. Note that while analyzing one of the loops, it is important to keep the other loop closed, as each loop will have a significant impact on the stability of the other.

Figure 4.9 shows the small signal model of the main loop in the GMB-FVF regulator for loop gain analysis. The current mirrors are assumed to have negligible high-frequency poles and a current gain of K. The resistance seen at the gate of M_P has been simplified to

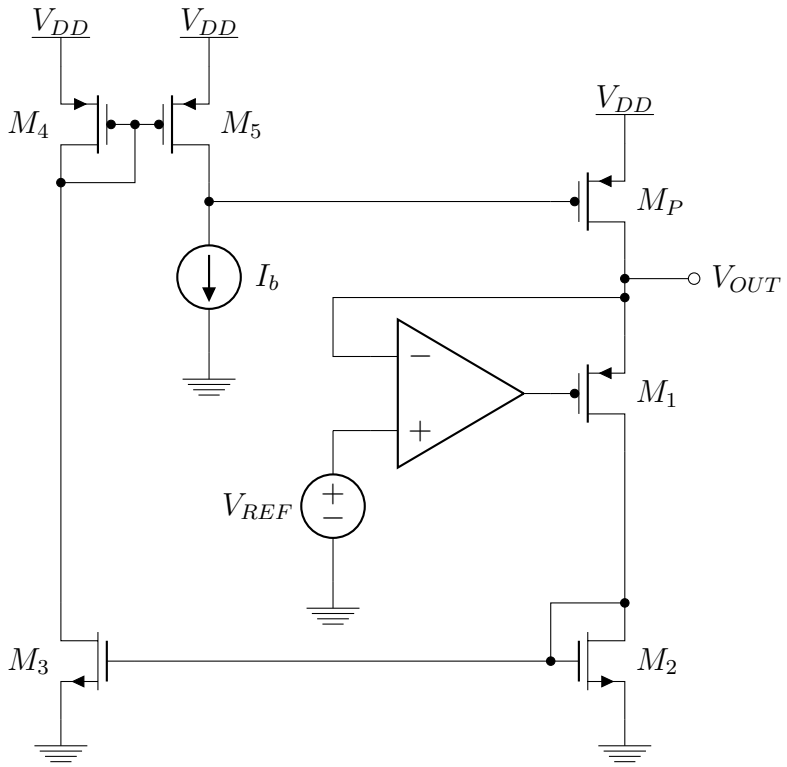


Figure 4.7: Schematic of the FVF-based Regulator with an Amplifier in the Loop

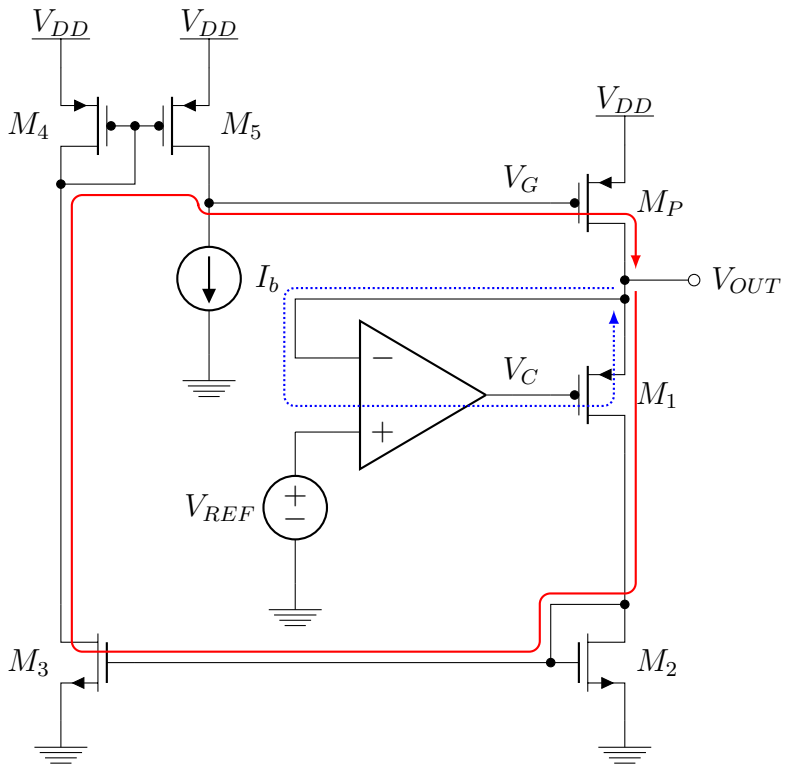


Figure 4.8: Illustration of loops in the GMB-FVF. The solid red line is the main regulation loop, similar to the loop in the FVF-based regulators. The dotted blue line is the auxiliary loop created by the addition of the amplifier.

$r_G = (r_{ds5} \parallel r_b)$, where r_b is the resistance of the current source, I_b. The amplifier is assumed to have a single-pole frequency response, with the gain given as

$$A(s) = -A_0 \frac{1}{1 + \frac{s}{\omega_{pA}}}, \tag{4.12}$$

where A_0 and ω_{pA} are the DC gain and dominant pole of the amplifier, respectively. Assuming $r_{ds1} \gg r_{dsP}$, $g_{m1} \gg 1/r_{ds1}$ and $A_0 \gg 1$, the loop gain of the regulator can be determined from Figure 4.9 as

$$A_L = \frac{v_G^*}{v_G} = A_{L0} \frac{1 + \frac{s}{\omega_{z1}}}{\left(1 + \frac{s}{\omega_{p1}}\right)(s^2 a_{p2} + s a_{p1} + 1)} \tag{4.13}$$

$$A_{L0} = -\frac{A_0 g_{m1}}{A_0 g_{m1} + \frac{1}{r_{dsP}}} K g_{mP} r_G \tag{4.14}$$

$$\omega_{p1} = \frac{1}{r_G C_G} \tag{4.15}$$

$$\omega_{z1} = A_0 \omega_{pA} \tag{4.16}$$

$$a_{p2} = \frac{C_{LOAD}}{\frac{1}{r_{dsP}} + A_0 g_{m1}} \frac{1}{\omega_{pA}} \tag{4.17}$$

$$a_{p1} = \frac{1}{\frac{1}{r_{dsP}} + A_0 g_{m1}} \left[C_{LOAD} + \frac{\frac{1}{r_{dsP}} + g_{m1}}{\omega_{pA}} \right]. \tag{4.18}$$

The DC loop gain in (4.14) is improved by the amplifier when $g_{m1} < 1/r_{dsP}$. Due to the large size, and therefore low output resistance, of M_P, this constraint is easy to meet. As the DC gain of the amplifier, A_0, is increased, the DC loop gain will asymptotically approach a maximum of $A_{L0,max} = K g_{mP} r_G$. Thus, the loop gain can be further adjusted with by adjusting the current mirror gain K. This can be useful for increasing or decreasing the loop gain, as necessary, for stability. Furthermore, because the amplifier is directly sensing V_{OUT}, the GMB-FVF regulator avoids inaccuracies due to short-channel effects. Thus, the GMB-FVF regulator can achieve greater accuracy than the FVF-based regulator.

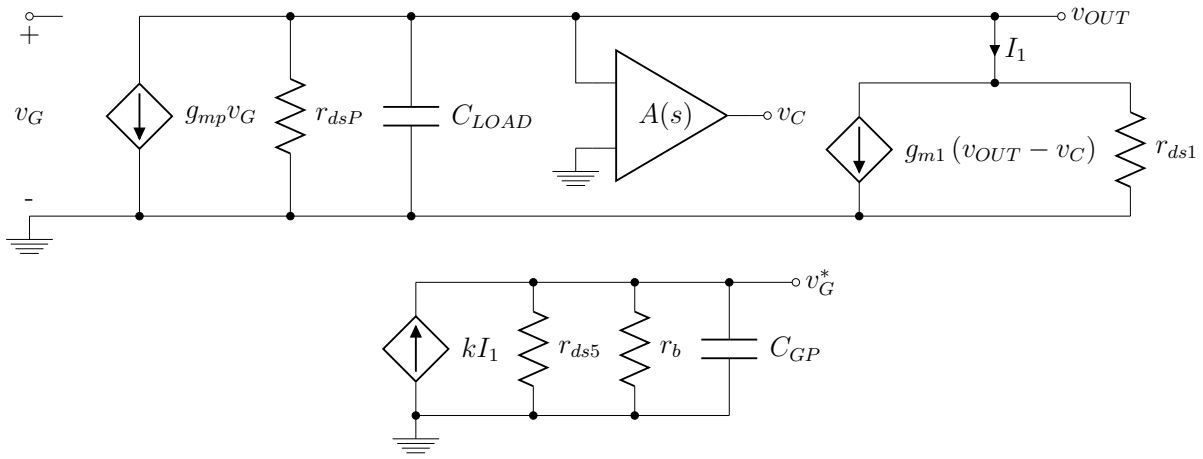


Figure 4.9: Small Signal Model of the FVF-based Regulator with Amplifier in the Loop

As shown in (4.13), moving the amplifier into the regulation loop creates an additional pole and zero compared to the FVF-based regulator loop gain in (4.2). The zero is given by

$$\omega_{z1} = \frac{1}{a_{z1}} = A_0\omega_{pA}. \tag{4.19}$$

This zero is located at the unity-gain frequency of the amplifier, where the amplifier stops boosting the transconductance of M_1. As discussed later, the pole of the amplifier, and thus its unity-gain frequency, will be large. Thus, ω_{z1} will be well above the unity-gain frequency of the regulator, making it negligible.

The additional pole introduced by the amplifier combines with the pole at the output of the regulator to form a complex pole. The second order term in the denominator of (4.13) can then be expressed as [17, 20, 30]

$$s^2a_{p2} + sa_{p1} + 1 = s^2\frac{1}{\omega_{p2,3}^2} + s\left(\frac{2\zeta}{\omega_{p2,3}}\right) + 1, \tag{4.20}$$

where $\omega_{p2,3}$ is the effective frequency, and ζ is the damping ratio of the complex pole pair. From (4.20), $\omega_{p2,3}$ is given as

$$\omega_{p2,3} = \frac{1}{\sqrt{a_{p2}}} = \sqrt{\frac{\frac{1}{r_{dsP}} + A_0 g_{m1}}{C_{LOAD}}} \omega_{pA}. \tag{4.21}$$

The damping ratio can also be derived from (4.20) as

$$\zeta = \frac{1}{2} a_{p1} \omega_{p2,3} = \frac{1}{2} \sqrt{\frac{\omega_{pA}}{\left(\frac{1}{r_{dsP}} + A_0 g_{m1}\right) C_{LOAD}}} \left[C_{LOAD} + \frac{\frac{1}{r_{dsP}} + g_{m1}}{\omega_{pA}} \right]. \tag{4.22}$$

For $\zeta > 1$, the second order term is considered overdamped, resulting in two real poles that can reduce the bandwidth of the system. Similarly, for $\zeta < 1$, the system will be underdamped, and considerable peaking will occur in the frequency response of the regulator due to the resonance of the complex poles [20]. For optimal stability, it is desired that $\omega_{p1,2}$ is located above the unity-gain frequency of the regulator, and that $\zeta \approx 1$ to ensure that the complex poles do not cause peaking that can degrade the gain margin. From (4.22), it is clear that increasing the amplifier gain will reduce the damping ratio which could result in degraded stability. Thus, the gain and bandwidth of the amplifier should be carefully designed to ensure that the complex pole pair that it introduces does not destabilize the regulator.

The stability of the regulator will also depend on the stability of the auxiliary loop. While the analysis of this loop does not give much insight into the performance characteristics of the regulator, it must be carefully analyzed to avoid instability or ringing in the regulator transient response. For loop gain analysis, this loop can be broken at V_C, resulting in the small-signal model shown in Figure 4.10. Assuming $K g_{m1} r_G g_{mP} \gg g_{m1} + \frac{1}{r_{dsP}}$, the loop gain can be derived as

$$A_{L,aux} = \frac{v_C^*}{v_C} = -A_0 \frac{1 + s\frac{1}{\omega_{za1}}}{(s^2 b_{p2} + s b_{p1} + 1)\left(1 + \frac{s}{\omega_{pA}}\right)} \tag{4.23}$$

$$a_{b2} = \frac{C_{LOAD}C_{GP}}{Kg_{m1}g_{mP}} \tag{4.24}$$

$$a_{b1} = \left(1 + \frac{1}{g_{m1}r_{dsP}}\right)\frac{C_G}{Kg_{mP}} + \frac{1}{g_{m1}r_G}\frac{C_{LOAD}}{Kg_{mP}} \tag{4.25}$$

$$\omega_{za1} = \frac{Kg_{mP}}{C_G}. \tag{4.26}$$

The auxiliary loop exhibits a zero, ω_{za1}, and three poles, one of which is created by the pole of the amplifier, ω_{pA}. The other poles can be approximated by assuming $C_G \gg {}^{C_{LOAD}}/_{g_{m1}r_G}$. Using the same method as in Section 4.1.2, the poles can then be approximated as

$$\omega_{pa1} = \frac{1}{a_{b1}} = \frac{g_{m1}r_{dsP}}{1 + g_{m1}r_{dsP}}\frac{Kg_{mP}}{C_G} \tag{4.27}$$

$$\omega_{pa2} = \frac{a_{b1}}{a_{b2}} = \frac{1}{\omega_{pa1}a_{p2}} = \frac{1 + g_{m1}r_{dsP}}{C_{LOAD}r_{dsP}}. \tag{4.28}$$

Both ω_{za1} and ω_{pa2} are located at high frequencies due to the low output resistance and large transconductance of M_P, leaving ω_{pa1} as the dominant pole. It is important to note that ω_{pa1} is not dependent on r_G, and thus is located at frequencies much larger than that of the main loop in (4.15). Therefore, there will not be a lot of separation between the dominant pole, ω_{p1} and the non-dominant poles, ω_{pA} and ω_{p2}. Thus, the DC gain of the amplifier must be limited to ensure that the unity-gain frequency is below these non-dominant poles.

4.3 Improving Transient Variations

As discussed in Section 2.3, output capacitor-free LDO regulators are typically unable to achieve a transient response on par with those of the conventional design. The largest contributor to this issue is the low slew rate at the node where the dominant pole is created. In the proposed GMB-FVF architecture in Section 4.2, the dominant pole is formed at the gate of the power transistor by the large gate capacitance and high output impedance of the current mirror stage.

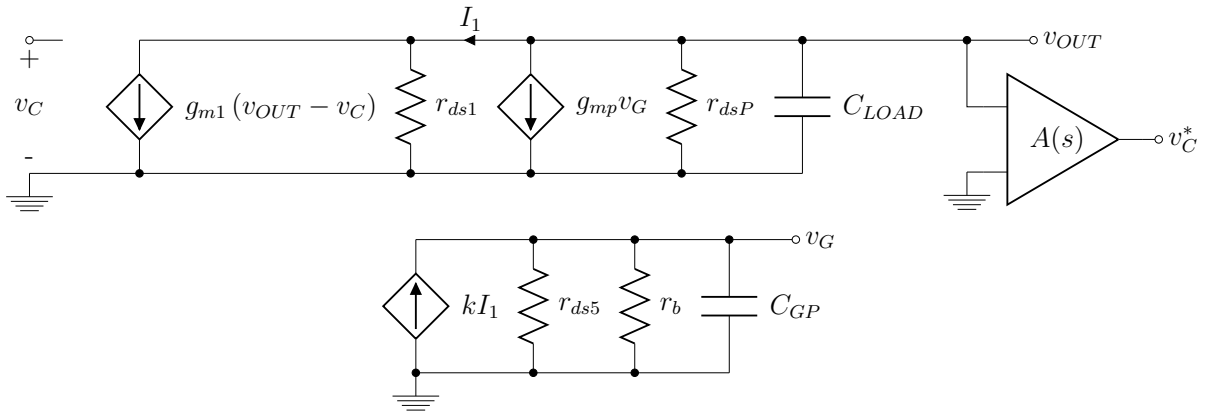


Figure 4.10: Small Signal Model of the GMB-FVF Auxiliary Loop

In the GMB-FVF, the current through M_1 is mirrored by $M_2 - M_5$ to the gate of M_P, thus providing at large positive slew rate at that node. However, no such path is available during negative slewing where only I_b is available for discharging the gate capacitance of the power transistor. As discussed in Section 4.1.3, slew rate enhancement can be applied to improve the negative slew rate at the gate of M_P. Figure 4.11 illustrates the addition of the SRE circuitry to the GMB-FVF regulator. As shown, the SRE circuitry adds an additional path through which to discharge the gate of the power transistor. The SRE is implemented as a dependent current source with a conductance of $G_t(s)$. This current source is responsible for detecting changes in the output voltage due to a change in load current, and quickly discharging the gate of the power transistor.

For the fastest transient response, the number of transistor stages in the SRE circuit must be minimized. Each transistor stage will introduce a pole into the circuit that will increase the delay, and thus the reaction time of the SRE circuit. Thus, it is desired to provide the most direct path for current from the gate of M_P to the output of the regulator as possible. Figure 4.12 shows the proposed SRE circuit. This circuit provides a current

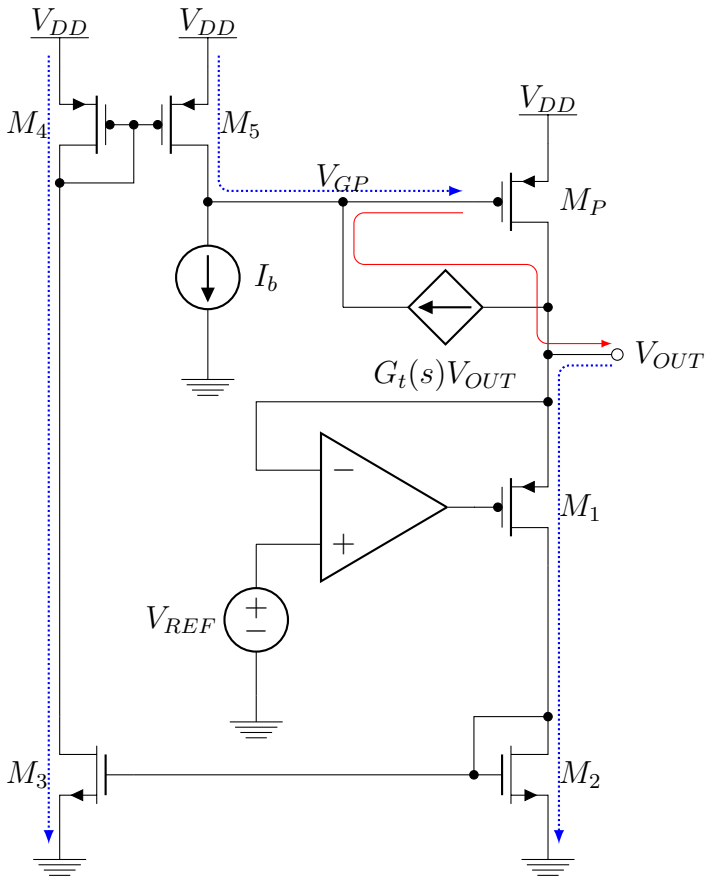


Figure 4.11: Addition of Slew Rate Enhancement to the GMB-FVF Architecture

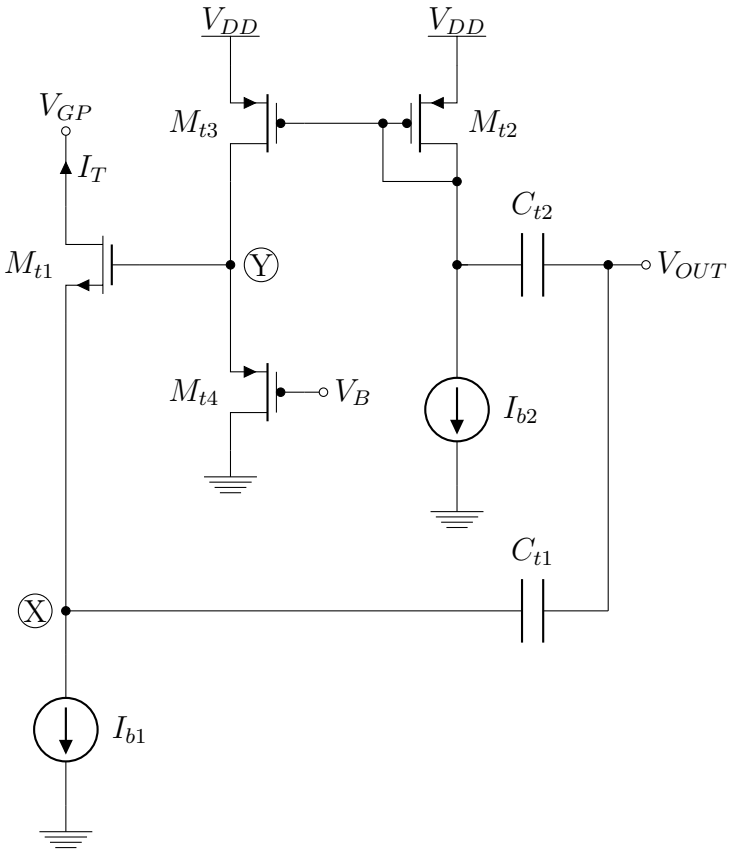


Figure 4.12: Slew Rate Enhancement Circuit

path from the output of the regulator to the gate of M_P through C_{t1} and M_{t1}, resulting in a very low reaction time. A slower secondary path is provided through C_{t2} to drive the gate of M_{t1} such that the effective transconductance of M_{t1} is boosted.

A basic understanding of the SRE circuit in Figure 4.12 can be gained by analyzing the circuit at very high frequencies, where C_{t1} and C_{t2} are effectively short circuits. Ignoring the delay through the current mirror formed by M_{t2} and M_{t3}, the current through the SRE circuit is then given by

$$I_T = (A_T + 1)g_{mt1}V_{OUT}, \tag{4.29}$$

where $A_T = {}^{g_{mt3}}/_{g_{mt4}}$ is the gain of the secondary path. Thus, the SRE circuit is able to provide a large amount of current for discharging the gate of M_P. The principle of the proposed SRE circuit is similar to that of [11, 24], where Ahuja cascode compensation [1] is used to simultaneously reduce the frequency of the dominant pole for stability while increasing the slew rate during transient swings at the output. However, because the Ahuja method reduces the bandwidth of the regulator, the designer has little control over the amount of slew rate improvement that is achieved. The proposed method has no effect on the dominant pole of the regulator, and thus gives the designer more freedom to choose the appropriate trade-off between slew rate enhancement and current consumption.

The addition of the SRE circuity to the GMB-FVF regulator complicates the analysis of the frequency response. A detailed analysis of the loop gain is given in Appendix B. While the SRE circuit adds two poles and two zeros to the loop gain analysis, these poles and zeros effectively cancel, allowing the loop gain to be approximated as

$$A_L \approx A_{L0} \frac{1 + \frac{s}{\omega_{z3}}}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(\frac{s}{\omega_{p4,5}^2} + \left(\frac{2\zeta_p}{\omega_{p4,5}}\right)s + 1\right)} \tag{4.30}$$

$$A_{L0} = -\frac{A_0 g_{m1}}{A_0 g_{m1} + \frac{1}{r_{dsP}}} K g_{mP} r_G \tag{4.31}$$

$$\omega_{z3} = \frac{A_0 g_{m1} + (A_T + 1) g_{mt1}}{g_{m1} + (A_T + 1) g_{mt1}} \omega_{pA} \tag{4.32}$$

$$\omega_{p1} = \frac{1}{r_G C_G} \tag{4.33}$$

$$\omega_{p4,5} = \sqrt{\frac{(1 + A_0 g_{m1} r_{dsP})\,\omega_{pA}}{C_{LOAD}}} \tag{4.34}$$

$$\zeta_p = \frac{1}{2}\sqrt{\frac{\omega_{pA}}{r_{dsP} C_{LOAD}\,(1 + A_0 g_{m1} r_{dsP})}}\left(C_{LOAD} + \frac{1 + (g_{mt1} + g_{mt2}) r_{dsP}}{\omega_{pA}}\right). \tag{4.35}$$

As shown, the locations of the poles are largely unaffected by the addition of the SRE circuit. Interestingly, the SRE circuit shifts the location of the high frequency zero in the GMB-FVF

Table 4.1: Component Parameters for the GMB-FVF Regulator Design

Component	Value	Units
M_P	10/0.24	μm/μm
M_1	8/0.24	μm/μm
$M_4 - M_5$	4/0.30	μm/μm
$Q_1 - Q_2$	10/0.12	μm/μm
$M_{t2} - M_{t4}$	4/0.30	μm/μm
$M_{t5} - M_{t7}$	2/0.30	μm/μm
Q_{t1}	2.5/0.12	μm/μm
M_M	6/0.30	μm/μm
C_m	12	pF
C_{t1}	100	pF
C_{t2}	10	pF

regulator to lower frequencies, allowing it cancel some of the phase shift caused by $\omega_{p4,5}$ and resulting in improved stability.

4.4 G_m-Boosted FVF Regulator Design

The proposed GMB-FVF architecture and SRE circuit have been simulated in the IBM8HP 0.13μm process. Figure 4.13 shows the full GMB-FVF regulator with the slew rate enhancement circuit. Table 4.1 shows the parameters for each component in the circuit. To ensure reliability, high-breakdown devices have been used for all transistors. Transistors Q_{t1} and $Q_1 - Q_2$ have been implemented as the SiGe bipolar transistors available in the process as they exhibit substantially higher transconductances than their MOS counterparts, allowing for a reduction in current consumption. Transistor M_m and capacitor C_m implement the well-known pole-splitting compensation technique [12, 17, 30] to move the dominant pole at the gate of M_P to lower frequencies to achieve stability.

To ensure that the complex poles in the frequency response do not degrade the stability of the regulator, the amplifier was designed for $A_0 = 15$ and $\omega_{pA} = 2\pi \cdot 100$MHz. A schematic

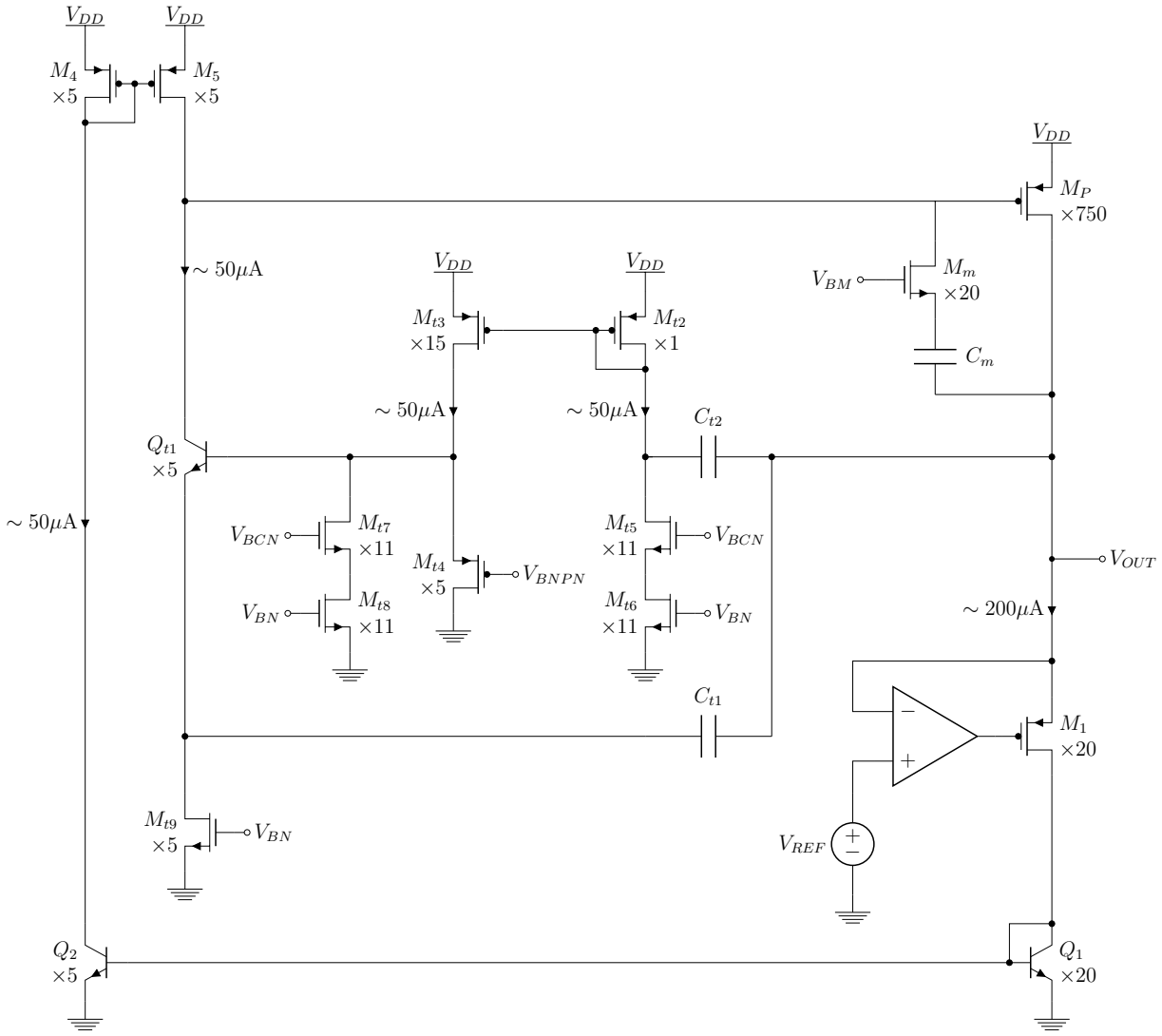


Figure 4.13: Schematic of GMB-FVF Design with Slew Rate Enhancement

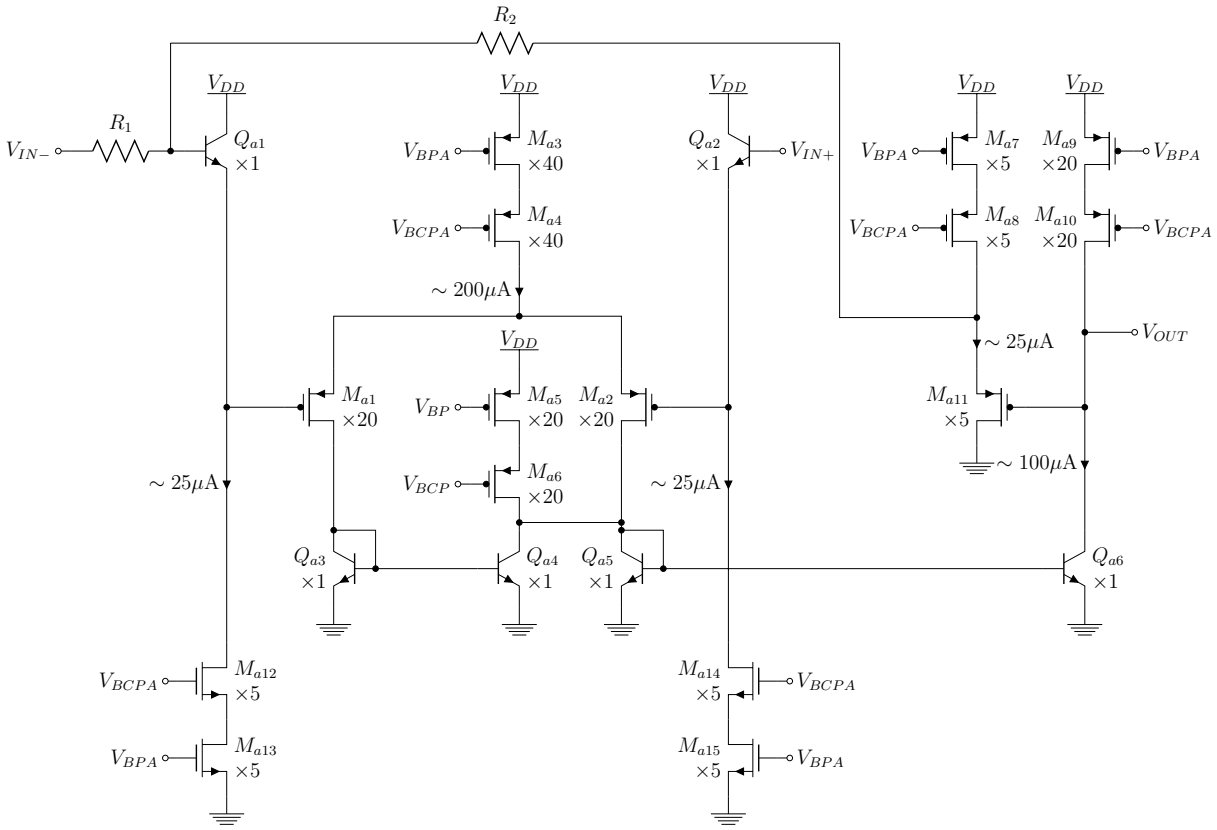


Figure 4.14: Schematics of the GMB-FVF Amplifier Design

of the amplifier is given in Figure 4.14. Table 4.2 gives the parameters for each component in the amplifier. To achieve the high bandwidth, only the SiGe bipolar transistors are used in the signal path with the exception of the differential input pair formed by $M_{a1} - M_{a2}$. The PMOS differential input pair is driven by emitter followers formed by $Q_{a1} - Q_{a2}$. Feedback resistors $R_1 - R_2$ are used in the typical inverting amplifier configuration to set the desired gain and move the dominant pole to higher frequencies. Transistor M_{a1} is proportional in size and drain current to transistor M_1 in the core of the regulator such that $V_{FB} = V_{OUT} = V_{IN-}$ to minimize the loading of the feedback resistors on the amplifier. This reduces the offset of the amplifier, thus improving the accuracy of the regulator.

Table 4.2: Component Parameters for the GMB-FVF Amplifier Design

Component	Value	Units
$Q_{a1} - Q_{a2}$	2.5/0.12	μm/μm
$M_{a1} - M_{a2}$	3/0.3	μm/μm
$M_{a3} - M_{a10}$	20/1.2	μm/μm
M_{a11}	8/0.24	μm/μm
$M_{a12} - M_{15}$	1.5/0.3	μm/μm
$Q_{a3} - Q_{a6}$	10/0.12	μm/μm
R_1	1	kΩ
R_2	15	kΩ

4.5 Simulation Results

Figure 4.15 shows the simulated loop gain of the GMB-FVF regulator with slew rate enhancement in the worst case corner (FF). As shown, the regulator achieves a minimum phase margin of 48° and a gain margin greater than 10dB over the entire load current range. The regulator is also stable when the load current is zero.

Figure 4.16 shows the simulated loop gain of the auxiliary loop created by the amplifier. As expected, the auxiliary loop is easily stable over the load current range due to the low gain of the amplifier. The minimum phase margin in the load current range is 97°. At zero load current, the phase margin degrades significantly to 45°, however the regulator remains stable. This degradation in phase can be attributed to excessive peaking caused when the pole at the output of the regulator moves to lower frequencies due to the increase in r_{dsP} at such low currents.

Figure 4.17 shows a histogram of the DC output voltage of the GMB-FVF regulator over 100 Monte Carlo simulations including both mismatch and process variations at the worst-case temperature (125°C). As shown, the proposed regulator has an accuracy of 1.2%, with a standard deviation of 5mV. It is important to note that these simulations use an

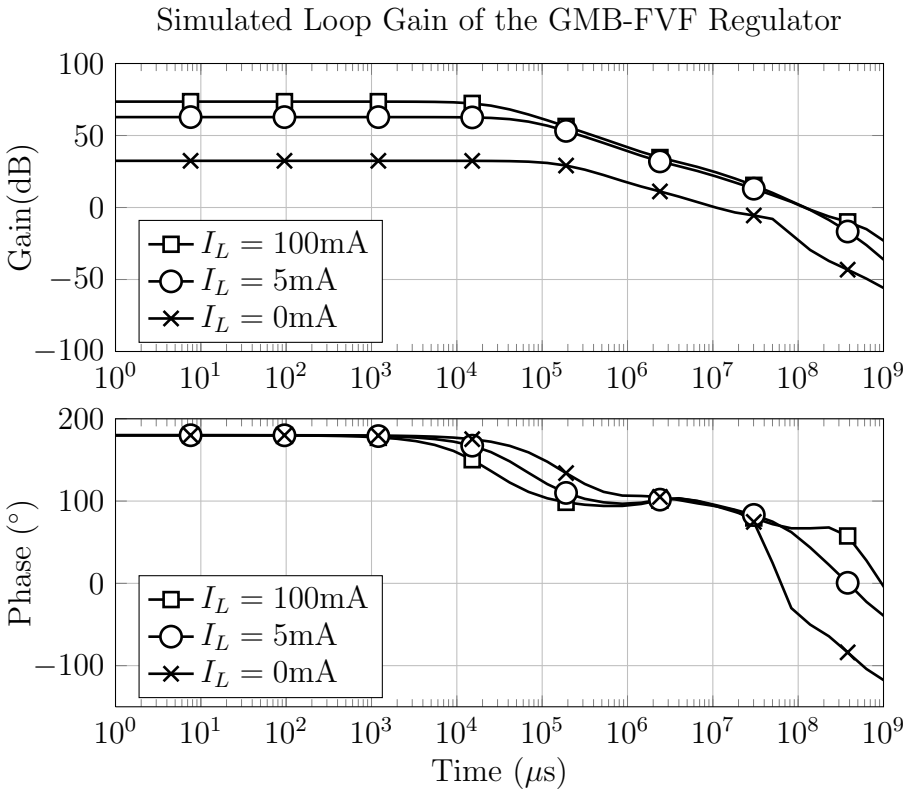


Figure 4.15: Simulated Loop Gain of the GMB-FVF Regulator

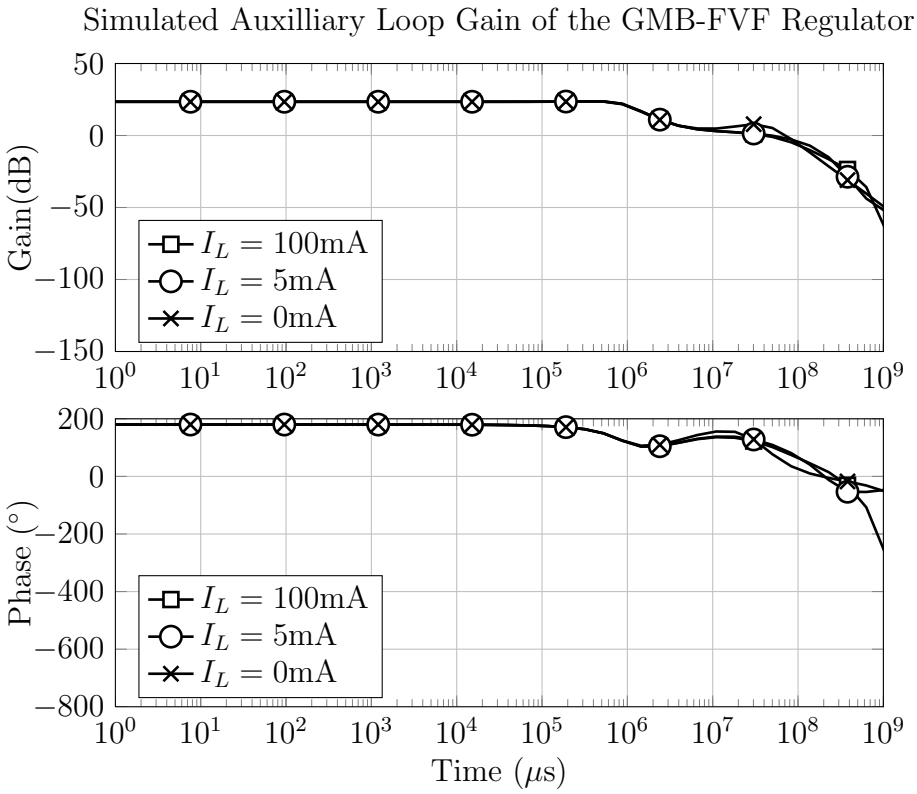


Figure 4.16: Simulated Auxiliary Loop Gain of the GMB-FVF Regulator

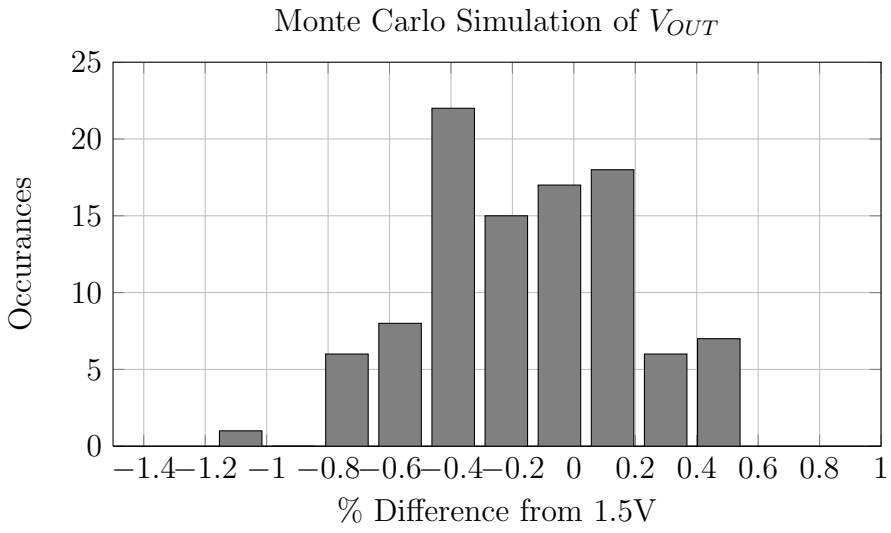


Figure 4.17: Monte Carlo Simulation of the DC Output Voltage

ideal voltage reference. The accuracy of a fully integrated regulator will depend heavily on the accuracy of the voltage reference that is used.

Figures 4.18 and 4.19 show the load and line regulation of the regulator, respectively, for the worst Monte Carlo sample. For load currents between 5mA and 100mA, the regulator exhibits a load regulation of less than $10^{\text{mV}}/_{\text{A}}$ and a line regulation of less than $0.25^{\text{mV}}/_{\text{V}}$. For load currents less than 5mA the load regulation degrades as expected due to the significantly reduced loop gain when M_P is shut off.

Figure 4.20 shows the simulated PSR of the GMB-FVF regulator for the worst Monte Carlo sample. The PSR is better than −58dB up to 10kHz. Thus, the regulator can effectively reject a significant amount of supply ripple from a switching power supply that operates with a switching frequency below 10kHz. As with most output capacitor-free regulators, the lack of a large decoupling capacitor at the output causes the power supply rejection

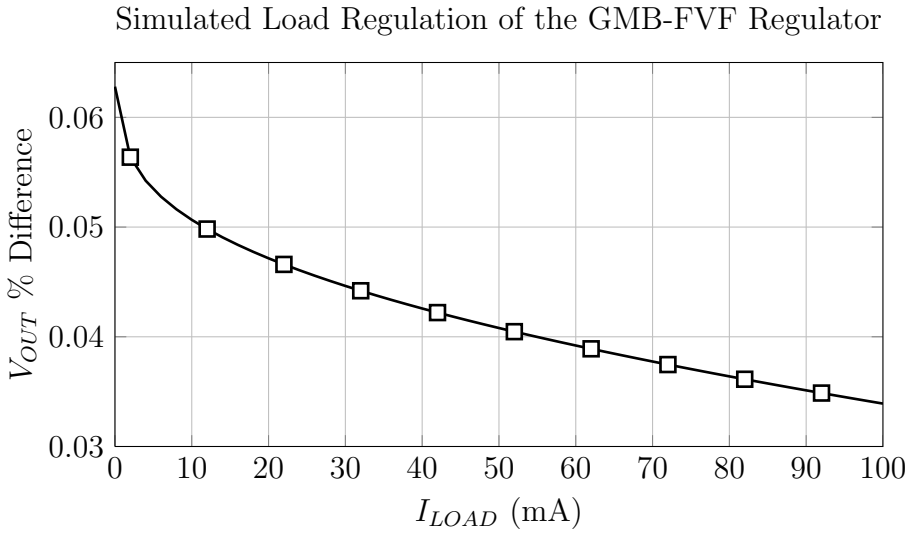


Figure 4.18: Simulated Load Regulation of the GMB-FVF Regulator

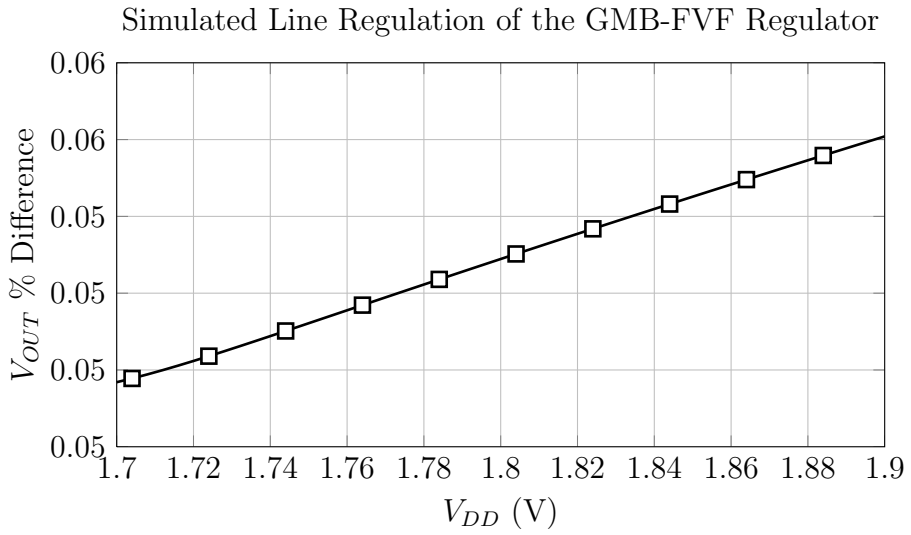


Figure 4.19: Simulated Line Regulation of the GMB-FVF Regulator

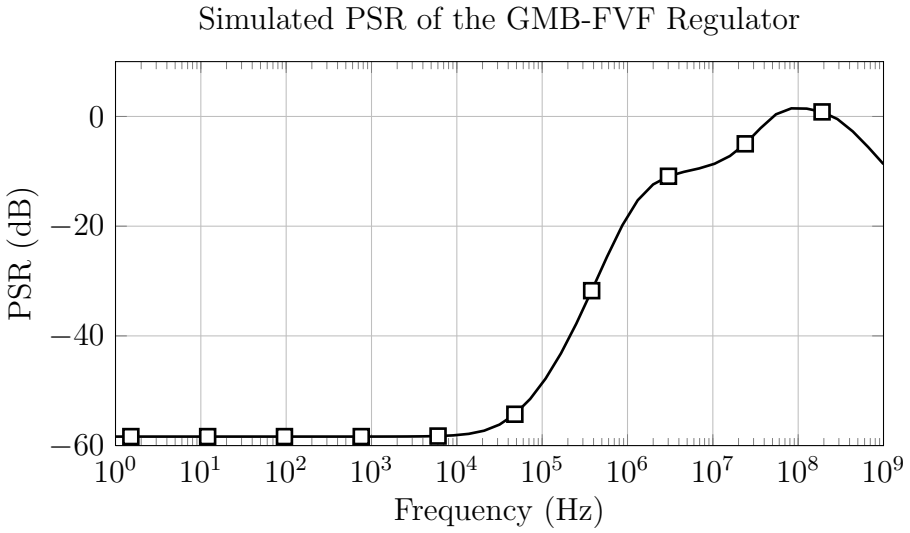


Figure 4.20: Simulated PSR of the GMB-FVF Regulator

to degrade significantly around the unity-gain frequency of the regulator. Thus, applications sensitive to power supply noise in this band may require some additional filtering.

Figure 4.21 shows the transient response of the proposed GMB-FVF regulator for the worst Monte Carlo sample where the full load current is switched in 10ns. The regulator achieves a very fast response time, with an undershoot of 80mV and an overshoot of 140mV. The overshoot is somewhat larger than the undershoot do the the delay of the current mirror stages during positive slewing at the gate of M_P. The output voltage recovers to within 1% of the final value within 50ns. The settling time of the regulator is below 410ns in the worst case.

Table 4.3 compares the results of the GMB-FVF regulator with those of previous publications. The figure of merit is given as [14]

$$FOM = \frac{C_{LOAD}\Delta V_{OUT} I_Q}{I_{MAX}^2}, \tag{4.36}$$

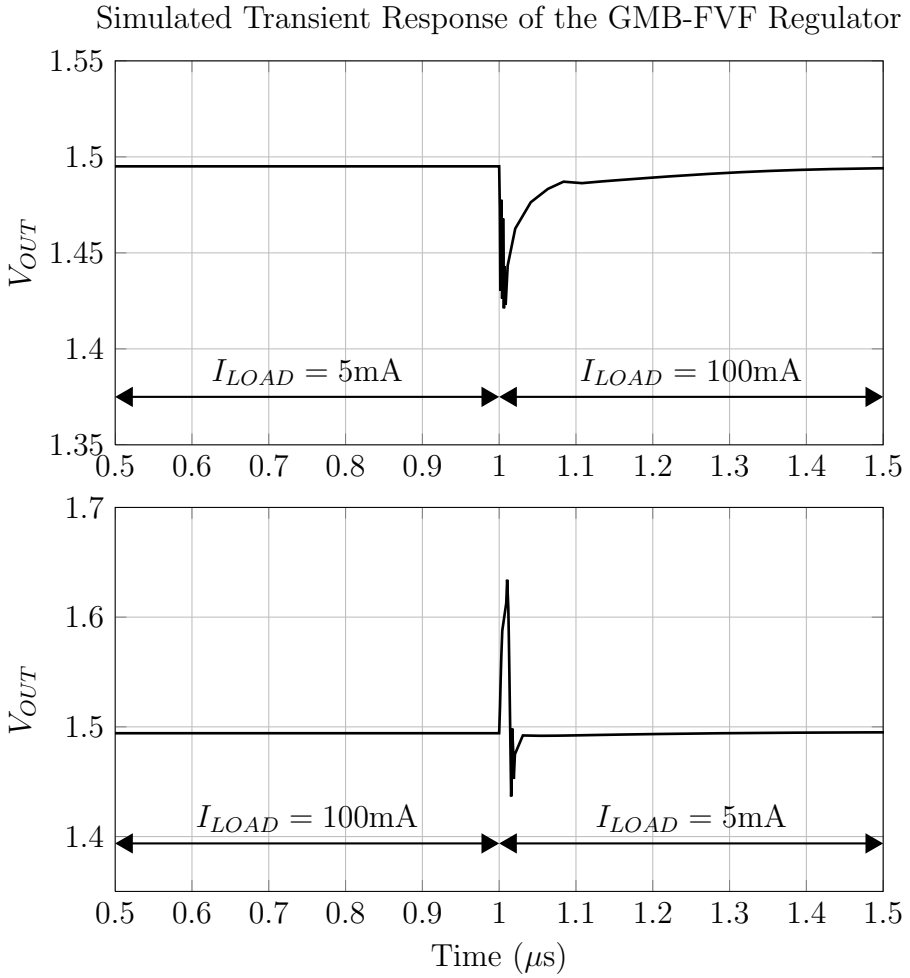


Figure 4.21: Simulated Transient Response of the GMB-FVF Regulator

where ΔV_{OUT} is the output voltage variation, I_Q is the quiescent current and, I_{MAX} is the maximum load current. This figure of merit is useful for comparing the transient response of two regulators, however it should be noted that it does not consider the rise and fall time of the load current used to measure ΔV_{OUT} and as such, can be inconsistent between different publications. As shown, the GMB-FVF regulator is the only regulator that simultaneously achieves low output voltage variation, fast recovery time, low load regulation, and low line regulation.

Table 4.3: Summary of Simulated Results for the GMB-FVF Regulator Regulator

	[14]	[24]	[19]	[13]	[3]	[25]	**This Work**	Units
Year	2004	2007	2007	2010	2011	2012	**2012**	–
Technology	0.09	0.35	0.35	0.09	0.35	0.35	**0.13**	μm
	Si CMOS	Si CMOS	Si CMOS	Si CMOS	Si CMOS	Si CMOS	**SiGe BiCMOS**	–
Input Voltage	1.2	3	1.5	0.75	1.5	2.5	**1.8**	V
Output Voltage	0.9	2.8	1.2	0.5	1.2	2.35	**$1.5 \pm 1.2\%$**	V
Max. Load Current	100	50	50	100	50	100	**100**	mA
V_{OUT} Trans. Variation	± 90	± 90	$+46/-75$	± 114	$+46/-75$	$+227/-236$	**$+140/-80$**	mV
C_{LOAD}	600	100	200	50	200	100	**100**	pF
On-chip Cap.	0	21	6	7	26	6.5	**122**	pF
PSR @ 100Hz	55	57	40	–	40	–	**58.5**	dB
Recovery Time	–	–	150	~ 2000	50	150	**50**	ns
I_{LOAD} Rise/Fall Time	0.2	1000	1000	100	300	500	**10**	ns
Quiescent Current	6	0.065	0.036	0.008	0.035	0.007	**1.2**	mA
Load Regulation	1000	200	338	100	3	80	**10**	$^{mV}/_{A}$
Line Regulation	–	2.5	0.344	3.8	8.8	1	**0.25**	$^{mV}/_{V}$
FOM	32	0.25	0.72	0.005	0.23	0.016	**1.7**	ps

CHAPTER 5

CONCLUSION AND FUTURE WORK

Two fast-transient LDO regulators have been presented in the IBM8HP 0.13μm BiCMOS process. These regulators are able to quickly respond to load current changes, effectively reducing the power supply noise for the system. The conventional design achieves a fast-transient response using a large output capacitor. A thorough test setup has been presented that is capable of fully testing the regulator. The output capacitor-free design implements a novel G_m-boosted Flipped Voltage Follower architecture with a slew rate enhancement circuit. This GMB-FVF design allows for the complete integration of the regulator, while maintaining a transient response close to that of the conventional design. The full on-chip integration of LDO regulators leads to many interesting possibilities, especially in analog and RF systems where many integrated local power supplies can be used to reduce crosstalk between sensitive subsystems.

5.1 Conventional Design and Test Setup

While the conventional design achieved the design goals, the use of the ESR of the output capacitor to stabilize the regulator can be problematic as the ESR is not easily controlled. This issue can be solved by creating an internal zero in the regulator and allowing the zero caused by the ESR to move to high frequencies [5]. Furthermore, there is a desire to design

regulators capable of driving larger load currents for RF circuitry, necessitating a larger power transistor. Placing a buffer between the error amplifier and the power transistor and applying Miller compensation could make the stability of the regulator relatively independent of the size of the power transistor. This could allow the regulator to be easily scaled for larger load currents by only resizing the power transistor and buffer.

The test setup could use three changes to make it more effective at measuring the performance of the regulators. First, the test points should be grouped together in a single location so that it is easier to make all of the necessary connections to the test equipment. Second, the test setup would benefit from a two-layer board design, adding a ground plane to the bottom layer. This will reduce the inductance of all of the traces, which can significantly effect the measurement results when switching large load currents. Finally, more decoupling capacitors should be added to the input supply to reduce ringing caused by parasitic inductances in the traces and wires connecting the power supply to the board. Such an improvement would make it easier to accurately measure the transient response of the regulator.

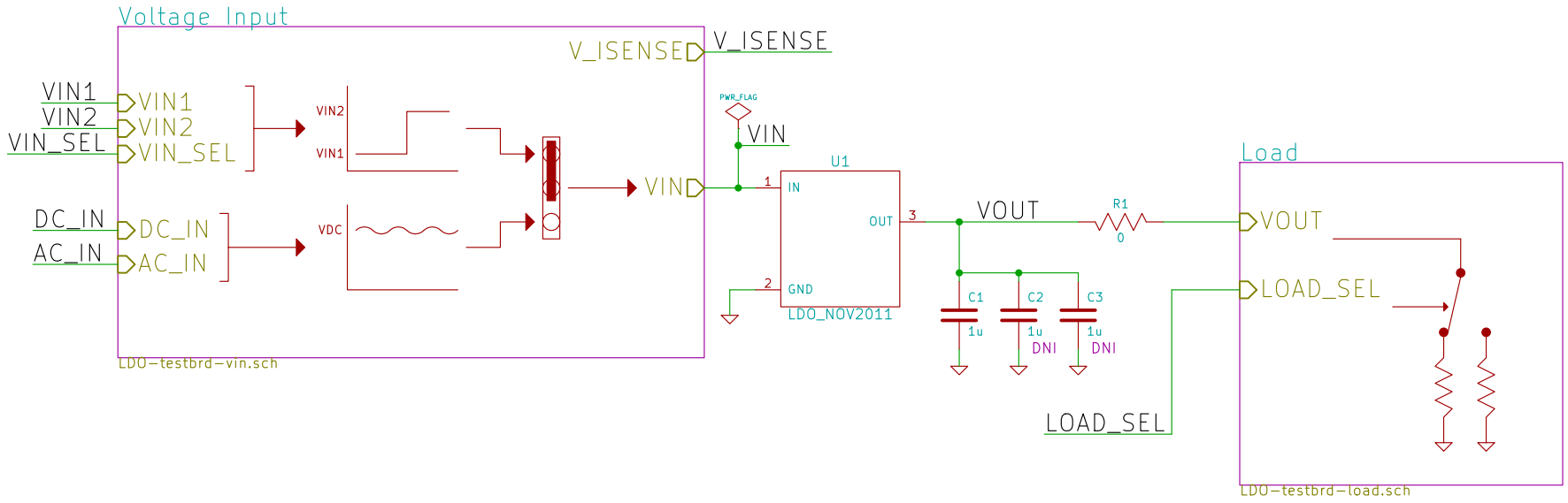
5.2 GMB-FVF Design

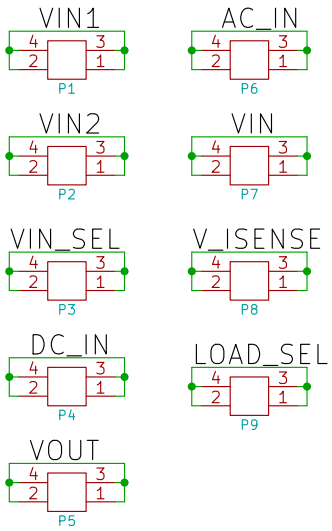
While the GMB-FVF regulator with slew rate enhancement provided a significantly improved transient response, the delay of the current mirrors still limits the ability of the regulator to mitigate overshoots in the output voltage. Thus, it would be beneficial to explore methods of adding slew rate enhancement circuitry capable of quickly charging the gate of the power transistor when an overshoot is detected at the output. The limited voltage headroom between the gate of the power transistor and the input voltage make this a non-trivial task. Furthermore, the proposed design was not optimized for minimum current consumption. Techniques such as dynamic biasing may help improve the current efficiency

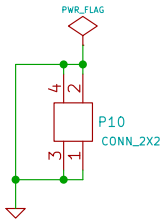
of the regulator, however the impact on the reaction time of the regulator would need to be studied carefully.

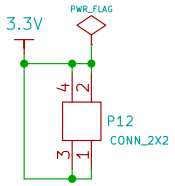
APPENDIX A

SCHEMATIC FOR THE LDO TEST SETUP PCB

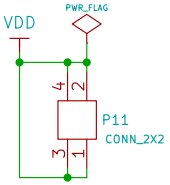








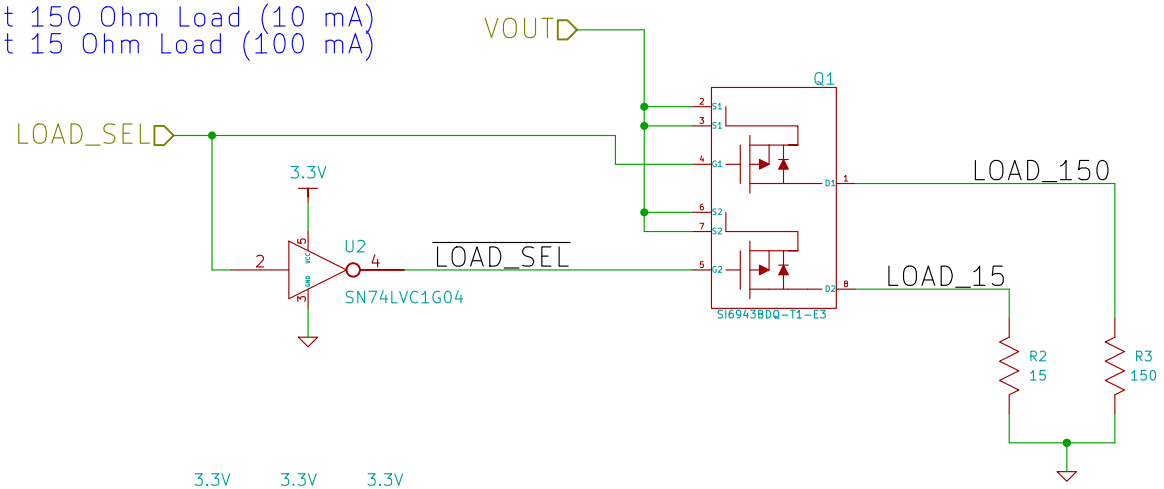
3.3V supply for digital inverters (Only need when using the stepped input)

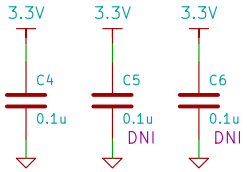


For ripple input:
Set VDD=DC_IN+2.7V
To avoid overheating
U4

Designer: Luke Duncan The Ohio State University / Air Force Research Laboratory		
File: LDO-testbrd.sch Sheet: /		
Title: LDO Test Board		
Size: A	Date: 22 may 2012	Rev: 0.1
KiCad E.D.A.		Id: 1/5

LOAD_SEL=0: Select 150 Ohm Load (10 mA)
LOAD_SEL=1: Select 15 Ohm Load (100 mA)





Designer: Luke Duncan The Ohio State University / Air Force Research Laboratory		
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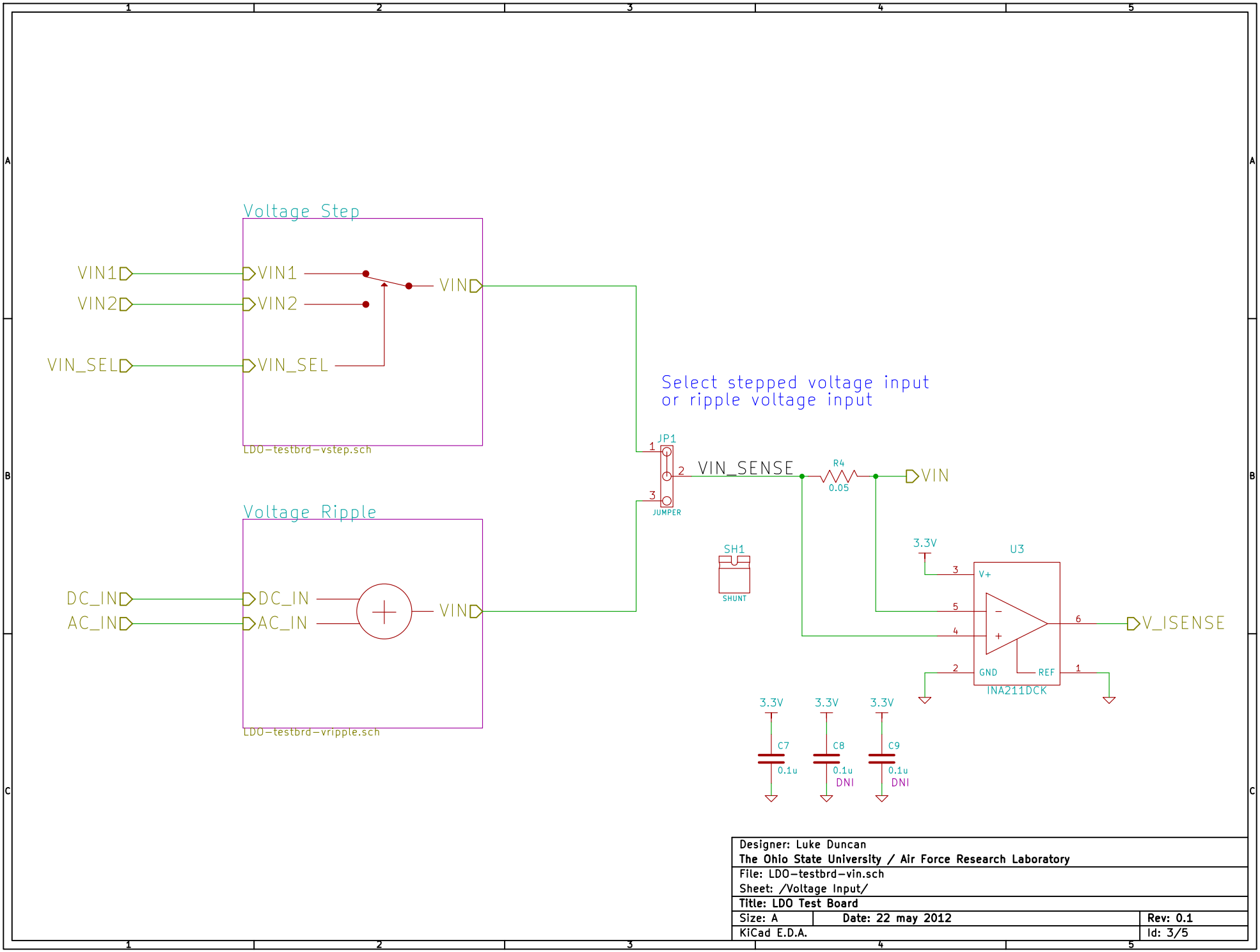
KiCad E.D.A.		Id: 2/5



Designer: Luke Duncan The Ohio State University / Air Force Research Laboratory		
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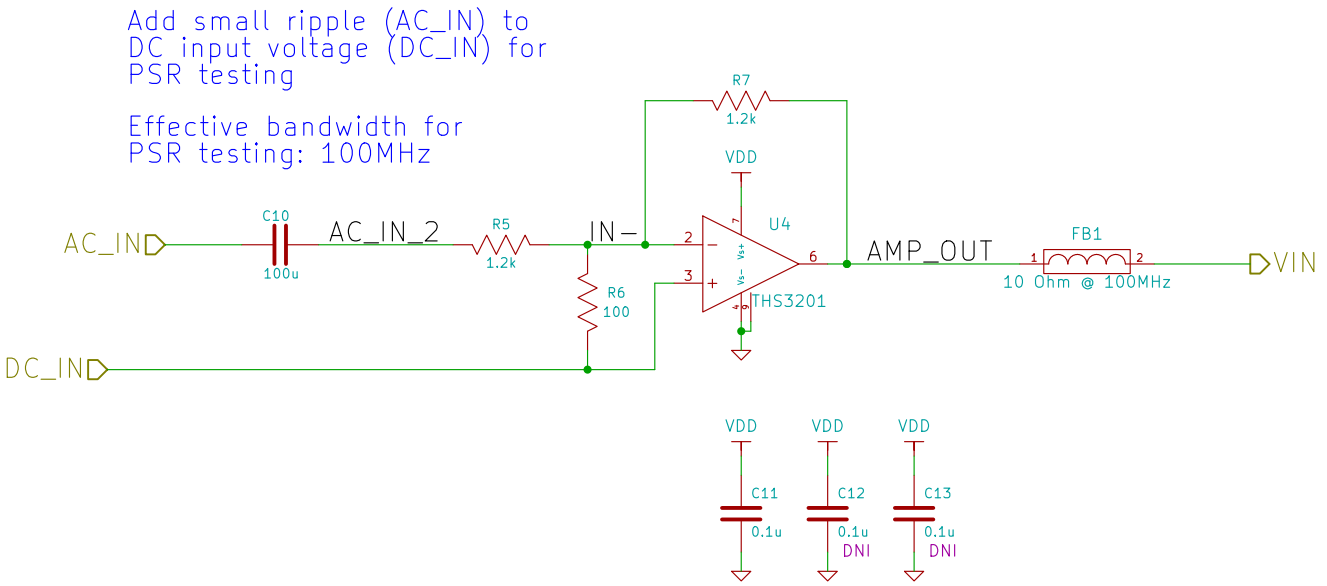
KiCad E.D.A.		Id: 3/5



Designer: Luke Duncan The Ohio State University / Air Force Research Laboratory		
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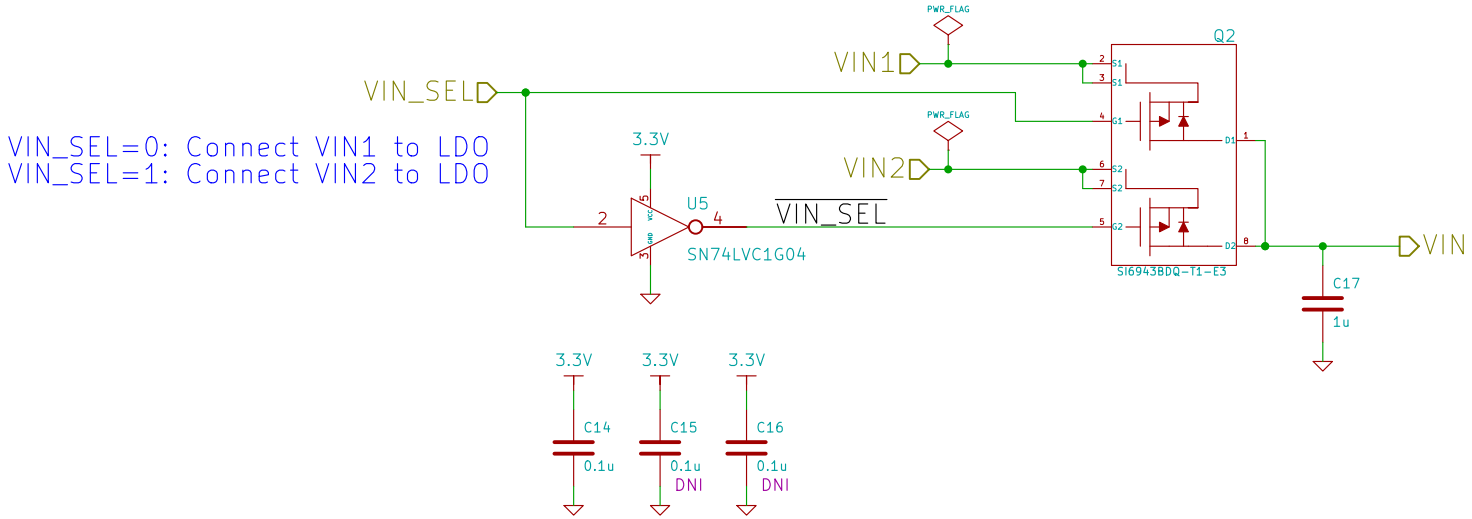
Size: A	Date: 23 may 2012	Rev: 0.1
KiCad E.D.A.		Id: 4/5



Designer: Luke Duncan The Ohio State University / Air Force Research Laboratory		
File: LDO-testbrd-vstep.sch Sheet: /Voltage Input/Voltage Step/		
Title: LDO Test Board		
Size: A	Date: 22 may 2012	Rev: 0.1
KiCad E.D.A.		Id: 5/5

Table A.1: Test Setup PCB Bill of Materials

Reference	Value	Footprint	Qty	Manufacturer	Part Number	Distributor	Description	Note
C1 C17	1u	0603	2	Taiyo Yuden	EMK107B7105KA-T	Digikey	CAP CER 1UF 16V 10% X7R 0603	
C2 C3	1u	0603	2	Taiyo Yuden	EMK107B7105KA-T	Digikey	CAP CER 1UF 16V 10% X7R 0603	DNI
C4 C7 C11 C14	0.1u	0603	4	Taiyo Yuden	EMK107B7104KA-T	Digikey	CAP CER 0.1UF 16V 10% X7R 0603	
C5 C6 C8 C9 C12 C13 C15 C16	0.1u	0603	8	Taiyo Yuden	EMK107B7104KA-T	Digikey	CAP CER 0.1UF 16V 10% X7R 0603	DNI
C10	100u	1210	1	AVX Corporation	JMK325BJ107MY-T	Digikey	CAP TANT 100UF 6.3V 10% 1210	
FB1	10 Ohm @ 100MHz	0603	1	TDK	MPZ1608S101A	Digikey	FERRITE CHIP 100 OHM 3A 0603	
JP1	JUMPER	HEADER_SMD_3_PIN1TOP	1	Sullins	GRPB031VWTC-RC	Digikey	CONN HEADER .050”” 3POS SMD GOLD	
P1 P2 P3 P4 P5 P6 P7 P8 P9 P10 P11 P12	CONN_2X2	HEADER_SMD_2x2	12	FCI	95278-101A04LF	Digikey	CONN HEADER 4POS .100”” DL SMD	
Q1 Q2	SI6943BDQ-T1-E3	TSSOP_8_VISHAY	2	Vishay	SI6943BDQ-T1-E3	Digikey	MOSFET P-CH DUAL 12V 2.3A 8TSSOP	
R1	0	0603	1	Panasonic-ECG	ERJ-3GEY0R00V	Digikey	RES 0.0 OHM 1/10W 0603 SMD	
R2	15	1206	1	Panasonic-ECG	ERJ-8ENF15R0V	Digikey	RES 15.0 OHM 1/4W 1% 1206 SMD	
R3	150	1206	1	Panasonic-ECG	ERJ-8ENF1500V	Digikey	RES 150 OHM 1/4W 1% 1206 SMD	
R4	0.05	0603	1	Panasonic-ECG	ERJ-L03KF50MV	Digikey	RESISTOR .050 OHM 1/10W 1% 0603	
R5 R7	1.2k	0603	2	Panasonic-ECG	ERJ-3EKF1201V	Digikey	RES 1.20K OHM 1/10W 1% 0603 SMD	
R6	100	0603	1	Panasonic-ECG	ERJ-3EKF1000V	Digikey	RES 100 OHM 1/10W 1% 0603 SMD	
SH1	SHUNT	N/A	1	Sullins	NPB02SVFN-RC	Digikey	CONN JUMPER SHORTING 1.27MM GOLD	Install as shown on schematic
U1	LDO_NOV2011	LDO_NOV2011	1	AFRL	LDO_NOV2011	AFRL	1.5V 100mA LDO NOVEMBER 2011	
U2 U5	SN74LVC1G04	SOP_5_DBV	2	Texas Instruments	SN74LVC1G04QDBVRQ1	Digikey	IC SINGLE INVERTER GATE SOT23-5 -40C-125C	
U3	INA211DCK	SOP_6_DCK	1	Texas Instruments	INA211AIDCKT	Digikey	IC CURRENT MONITOR 1% SC70-6 GAIN 200	
U4	THS3201	SOP_8_PowerPad_DGN	1	Texas Instruments	THS3201MDGNREP	Digikey	IC OPAMP CFB 1.8GHZ SGL 8MSOP -55C-125C	

APPENDIX B

FREQUENCY ANALYSIS OF THE GMB-FVF REGULATOR WITH SLEW RATE ENHANCEMENT

The small signal model of the SRE circuit is shown in Figure B.1, where $A_T = {}^{g_{mt3}}/_{g_{mt4}}$ is the gain of the auxiliary loop. The effective conductance of the SRE circuit can be determined from Figure B.1 as

$$G_T(s) = \frac{I_T}{V_{OUT}} = C_{t1}\frac{s\left(1 + s(A_T+1)\frac{C_{t2}}{g_{mt2}}\right)}{\left(1 + s\frac{C_{t1}}{g_{mt1}}\right)\left(1 + s\frac{C_{t2}}{g_{mt2}}\right)}. \tag{B.1}$$

The small signal model of the GMB-FVF regulator with slew rate enhancement is shown in Figure B.2, where r_G is the effective resistance at the gate of M_P. Using (B.1), and assuming that ${}^{1}/_{g_{mi}} >> r_{dsi}$ for all devices, the loop gain of the regulator can be derived from Figure B.2 as

$$A_L = A_{L0}\frac{a_{z3}s^3 + a_{z2}s^2 + a_{z1}s + 1}{\left(a_{p4}s^4 + a_{p3}s^3 + a_{p2}s^2 + a_{pa1}s + 1\right)\left(1 + \frac{s}{\omega_{p1}}\right)} \tag{B.2}$$

$$a_{z3} = \frac{C_{t1}C_{t2}}{A_0 g_{m1} g_{mt2}\omega_{pA}}\left(A_T + \frac{g_{m1}}{g_{mt1}} + 1\right) \tag{B.3}$$

$$a_{z2} = \frac{C_{t1}C_{t2}}{g_{mt2}}\left(\frac{1}{g_{mt1}} + \frac{A_T+1}{A_0 g_{m1}}\right) + \frac{1}{A_0\omega_{pA}}\left(\frac{C_{t1}}{g_{mt1}} + \frac{C_{t2}}{g_{mt2}}\right) + \frac{C_{t1}}{A_0 g_{m1}\omega_{pA}} \tag{B.4}$$

$$a_{z1} = \frac{C_{t1}}{g_{mt1}} + \frac{C_{t2}}{g_{mt2}} + \frac{1}{A_0\omega_{pA}} + \frac{C_{t1}}{A_0 g_{m1}} \tag{B.5}$$

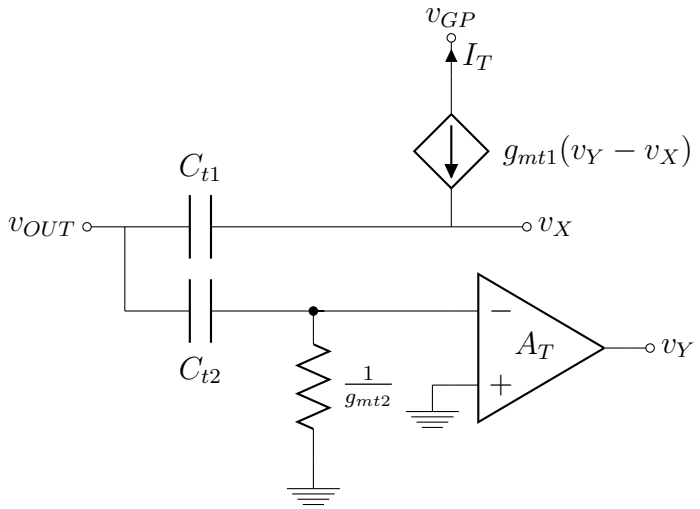


Figure B.1: Small Signal Model of the SRE Circuit

$$a_{p4} = \frac{r_{dsP} C_{LOAD} C_{t1} C_{t2}}{g_{mt1} g_{mt2} \omega_{pA} \left(1 + A_0 g_{m1} r_{dsP}\right)} \tag{B.6}$$

$$\begin{aligned} a_{p3} = \frac{1}{1 + A_0 g_{m1} r_{dsP}} \Bigg[& \frac{C_{t1} C_{t2}}{g_{mt1} g_{mt2}} \left(r_{dsP} C_{LOAD} + \frac{1 + r_{dsP}(g_{mt1} + g_{mt2})}{\omega_{pA}} \right) \\ & + \frac{r_{dsP} C_{LOAD}}{\omega_{pA}} \left(\frac{C_{t1}}{g_{mt1}} + \frac{C_{t2}}{g_{mt2}} \right) \Bigg] \end{aligned} \tag{B.7}$$

$$\begin{aligned} a_{p2} = \frac{1}{1 + A_0 g_{m1} r_{dsP}} \Bigg[& \frac{C_{t1} C_{t2}}{g_{mt1} g_{mt2}} (1 + A_0 g_{m1} r_{dsP}) \\ & + \left(\frac{C_{t1}}{g_{mt1}} + \frac{C_{t2}}{g_{mt2}} \right) \left(r_{dsP} C_{LOAD} + \frac{1}{\omega_{pA}} \right) \\ & + \frac{r_{dsP}(C_{t1} + C_{t2})}{\omega pA} + \frac{C_{t1} C_{t2}}{g_{mt1} g_{mt2}} r_{dsP}(g_{mt1} + g_{mt2}) \Bigg] \end{aligned} \tag{B.8}$$

$$\begin{aligned} a_{p1} = \frac{1}{1 + A_0 g_{m1} r_{dsP}} \Bigg[& \left(\frac{C_{t1}}{g_{mt1}} \right) \left(\frac{1}{r_{dsP}} + A_0 g_{m1} \right) \\ & + \left(r_{dsP} C_{LOAD} + \frac{1}{\omega_{pA}} + r_{dsP}(C_{t1} + C_{t2}) \right) \Bigg]. \end{aligned} \tag{B.9}$$

As shown, the slew rate enhancement circuitry adds two poles and two zeros to the GMB-FVF regulator. The loop gain analysis can be simplified by assuming

$$\frac{C_{t1}}{g_{mt1}}, \frac{C_{t2}}{g_{mt2}} \gg r_{dsP}(C_{LOAD} + C_{t1} + C_{t2}) \tag{B.10}$$

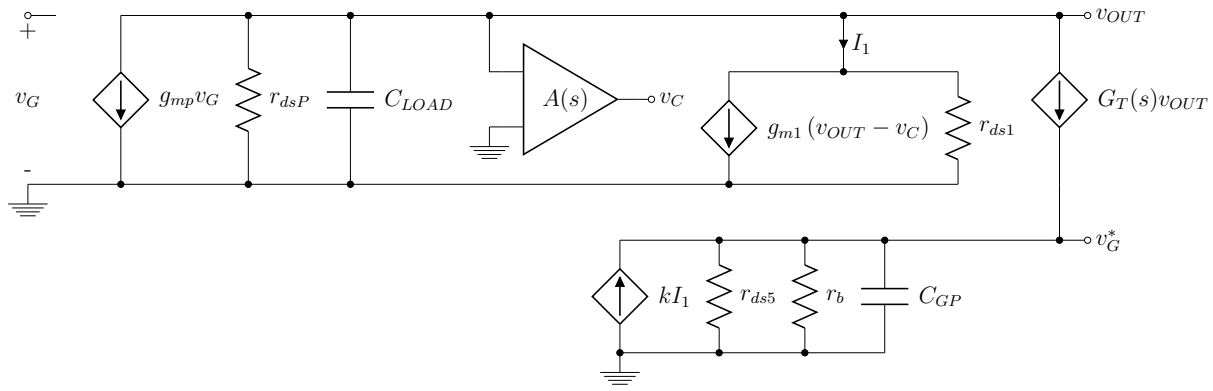


Figure B.2: Small Signal Model of the GMB-FVF regulator with SRE

$$\frac{C_{t1}}{g_{mt1}}, \frac{C_{t2}}{g_{mt2}} \gg \frac{1}{\omega_{pA}}. \tag{B.11}$$

The loop gain can then be approximated as [12]

$$A_L = A_{L0}\frac{\left[\frac{s^2}{\omega_{z1,2}^2}+\left(\frac{2\zeta_z}{\omega_{z1,2}}\right)s+1\right]\left(1+\frac{s}{\omega_{z3}}\right)}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)\left(1+\frac{s}{\omega_{p3}}\right)\left[\frac{s^2}{\omega_{p4,5}^2}+\left(\frac{2\zeta_p}{\omega_{p4,5}}\right)s+1\right]} \tag{B.12}$$

$$\omega_{z1,2} = \sqrt{\frac{1}{1+\frac{(A_T+1)g_{mt1}}{A_0 g_{m1}}}\frac{g_{mt1}g_{mt2}}{C_{t1}C_{t2}}} \tag{B.13}$$

$$\zeta_z = \frac{1}{2}\sqrt{\frac{1}{1+\frac{(A_T+1)g_{mt1}}{A_0 g_{m1}}}}\left(\sqrt{\frac{C_{t1}}{g_{mt1}}\frac{g_{mt2}}{C_{t2}}}+\sqrt{\frac{g_{mt1}}{C_{t1}}\frac{C_{t2}}{g_{mt2}}}\right) \tag{B.14}$$

$$\omega_{z3} = \frac{A_0 g_{m1}+(A_T+1)g_{mt1}}{g_{m1}+(A_T+1)g_{mt1}}\omega_{pA} \tag{B.15}$$

$$\omega_{p2} = \frac{g_{mt1}}{C_{t1}} \tag{B.16}$$

$$\omega_{p2} = \frac{g_{mt2}}{C_{t2}} \tag{B.17}$$

$$\omega_{p4,5} = \sqrt{\frac{\left(1+A_0 g_{m1} r_{dsP}\right)\omega_{pA}}{C_{LOAD}}} \tag{B.18}$$

$$\zeta_p = \frac{1}{2}\sqrt{\frac{\omega_{pA}}{r_{dsP}C_{LOAD}\left(1+A_0 g_{m1} r_{dsP}\right)}}\left(C_{LOAD}+\frac{1+(g_{mt1}+g_{mt2})r_{dsP}}{\omega_{pA}}\right). \tag{B.19}$$

If the SRE circuit is designed such that $(A_T + 1)g_{mt1} <= A_0 g_{m1}$, then $\zeta_z >= {}^1/\sqrt{2}$ and $\omega_{z1,2}$ will be located between ω_{p2} and ω_{p3}. By placing ω_{p2} and ω_{p3} close together, they will cancel with $\omega_{z1,2}$. The loop gain can then be approximated as

$$A_L \approx A_{L0} \frac{1 + \frac{s}{\omega_{z3}}}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(\frac{s}{\omega_{p4,5}^2} + \left(\frac{2\zeta_p}{\omega_{p4,5}}\right)s + 1\right)}. \tag{B.20}$$

Thus, the SRE circuit has a small effect on the poles of the GMB-FVF regulator. The zero, ω_{z3}, is shifted to lower frequencies by the SRE circuit and can improve the stability of the regulator by canceling some of the phase shift caused by $\omega_{p4,5}$.

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