TUNABLE TIME DELAY ELEMENTS IN CMOS 90nm TECHNOLOGY FOR NOVEL VCO IMPLEMENTATION

THESIS

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ABSTRACT

Existing electronic upper frequency is being constantly challenged to cater for new and state-of-the-art wireless applications. The conventional voltage controlled oscillator (VCO) designs are not sufficient to meet the trend. This calls for innovative and novel architectures. Utilizing the concept of distributed-loaded phase shifters we delve on the idea of implementing a tunable wideband VCO in W and V band.

By periodically loading a coplanar waveguide transmission line with varactors, we can vary the phase velocity of the signal travelling through the line and thus creating a true time delay element. Through proper feedback, this system becomes analogous to a ring oscillator which is tunable by an analog control voltage.

Based on these concepts, a distributed-loaded phase shifter was designed in 90nm CMOS technology with center frequency of 100 GHz (W-band) and 60 GHz (V-band). A bandwidth of ~27% and ~30% were achieved respectively. The worst case insertion loss and worst case return loss were kept less than 10dB for both the bands. The performance is limited by the limited tuning range of CMOS varactors and deteriorating quality factor with increasing frequency.

To my family, for their love and support.

ACKNOWLEDGEMENTS

Foremost, I offer my sincere gratitude to my advisor, Dr. Waleed Khalil, for giving me this opportunity to work on this wonderful thesis. It was my privilege to work under him, his vast expertise and wisdom always guided me to push for excellence. Through him, I learned what engineering really meant. One simply could not wish for a better and friendlier mentor.

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Finally, I would like to acknowledge the patience, care, love and support of my parents and my sister throughout my life. They mean everything to me. Any success I have today, could not been possible without them.

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CHAPTER 1

INTRODUCTION

This thesis focus on a novel idea of VCO implementation using distributed analog phase shifter. The frequency of interest is in W-band with 20% bandwidth.

1.1 Motivation

Since the birth of electrical telegraphy in the 1830's, the transmission rates and the broadcast frequencies have increased tremendously. Communication links have progressed from few symbols to tens of gigabits per second. Operating frequencies have gone from KHz to MHz to GHz. Yet wireless applications are being explored to even higher frequencies testing the upper frequency limit of contemporary electronic technology, between 110 and 170 GHz. Few examples include 71-76/81-86 GHz for satellite services, 77 GHz used for automotive cruise control radar, 94GHz military radar targeting and tracking applications, and 94GHz atmospheric radio window for imaging mm-wave radar in astronomy. Inexpensive availability of technology and demand would further up the frequency scale. Thus the W-band (75-110 GHz) remains a hot research

topic. Voltage controlled oscillators are one of the fundamental blocks of any wireless transceiver system. Challenges at these frequencies call for exploration of novel ideas for stable and fully integrated chip implementation.

1.2 Thesis Contribution

This thesis attempts to address the challenges of a W-band VCO implementation through distributed phase shifter and an out-of-phase feedback amplifier based on "Barkhausen Criteria". However, the scope of this thesis is limited only to provide low-loss and high tun-ability using coplanar waveguide line periodically loaded with varactors. However, the idea of stable generation of sinusoidal signal is verified through a successful system-level simulation.

To take advantage of high-yield and low-cost CMOS technology, the distributed-line phase shifters topologies in 90nm CMOS process are researched. CMOS also allows for full system integration on a single chip. Distributed phase shifters are the ideal choice due to their high-frequency feasibility. With specification of achieving 20% bandwidth with less than 10dB insertion loss and return loss, successful simulations were performed at center frequency of 100 GHz (W-band) and 60 GHz (V-band). The varactor performance at these frequencies is the distinguished limiting factor because of its limited $C_{\max} / C_{\min}$ and quality factor.

1.3 Thesis Outline

After a brief introduction and motivation behind this thesis as described in Chapter 1, Chapter 2 describes the theory and basic design equations of distributed

analog phase shifters. Latter part of the chapter discusses the most recent and relevant publications to date.

Chapter 3 delves into the design and optimization aspects of achieving variable capacitance via the varactor models available in the IBM CMOS 90nm design kit in cadence.

Proposed phase shifter transient and S-parameter simulation results are presented in Chapter 4.

Finally, Chapter 5 summarizes and concludes the results obtained in this thesis and includes future work of the ideas presented herein.

CHAPTER 2

DISTRIBUTED TRANSMISSION LINE PHASE SHIFTERS: THEORY AND LITERATURE REVIEW

Analog phase shifting can be realized by using loaded transmission-line phase shifter acting as a tunable time delay element having low loss, high-frequency and wideband implementation. Multiple distributed sections are required to get desired phase range. This theoretical chapter describes the basic principle and design theory of distributed phase shifters loaded with varactors. It further discusses relevant research work published to date.

2.1 Basic Principles and Theory

A tunable time delay phase shifter is created by adding tunable reactance to a transmission line, thus loading the otherwise unloaded transmission line. The reactance alters the electrical length of the transmission line, altering the phase velocity of the signal propagating along the line and thus creating the phase shift. It is essential to optimize the transmission line structure to get desired phase delay with minimal insertion loss. Figure 2.1 shows the distributed model of shunt loaded transmission line. In general, it is possible to add both shunt and series tunable reactance to the transmission line;

however the technology for adding tunable series reactance (inductance) is yet to be fully developed. Thus a shunt variable capacitance is periodically added to the line as discrete element. This loading makes the distributed structure a periodic structure with a pass band and a stop band response. Care must be taken to ensure the frequencies of interest fall into the pass band while maintaining a high performing, efficient structure.

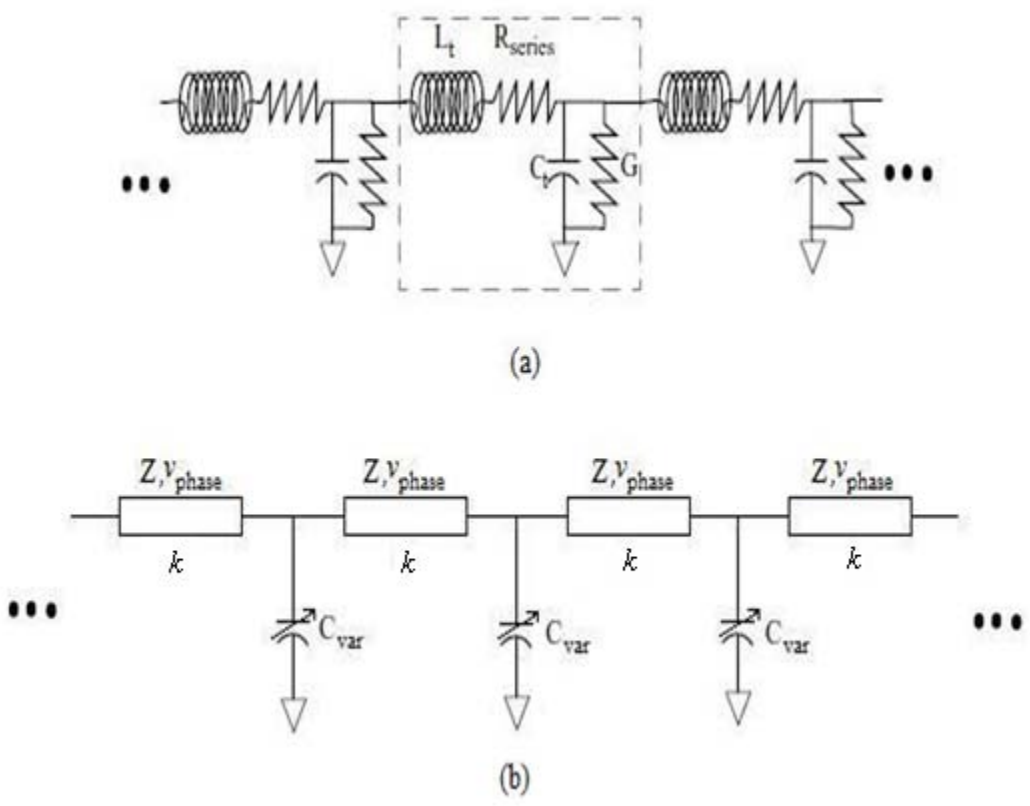


Figure 2.1(a) Distributed transmission line model (b) Loaded transmission line

The distributed inductance and capacitance per unit length of the transmission line are presented as L_t and C_t respectively; k is the length of each section. Changing the

capcitance alters impedance and phase velocity as given by Equation (2.1) and (2.2), respectively.

$$Z = \sqrt{\frac{kL_t}{kC_t + C_{\text{var}}}} \tag{2.1}$$

$$v_{phase} = \frac{k}{\sqrt{kL_t\left(kC_t + C_{\text{var}}\right)}} \tag{2.2}$$

However previous equations fail to cover the periodic nature of the circuit. The discontinuities created by the addition of tunable capacitors result in small reflections from each capacitor as the signal propagates along the length of the circuit. As the frequency of the signal increases and approaches a certain value, the phase of the incident and reflected signal interfere destructively, preventing forward propagation. The frequency beyond which there is no power transfer as the impedance of the line goes to zero is known as Bragg frequency. In other words, the signal is fully reflected back to the source at Bragg frequency. Careful design should ensure that we operate well above the Bragg frequency. Thus above equations are not valid in the vicinity of the Bragg frequency and a more exact analysis must recognize the discrete nature of the loading [1]. Equation for characteristic impedance is modified as given by Equation (2.3)

$$Z = \sqrt{\frac{kL_t}{kC_t + C_{\text{var}}}}\sqrt{1 - \frac{\omega^2}{4}kL_t\left(kC_t + C_{\text{var}}\right)} = \sqrt{\frac{kL_t}{kC_t + C_{\text{var}}}}\sqrt{1 - \left(\frac{\omega}{\omega_b}\right)^2} \tag{2.3}$$

Where f_b is the Bragg frequency, given by Equation (2.4).

$$f_b = \frac{1}{\pi\sqrt{kL_t(kC_t + C_{\text{var}})}} \tag{2.4}$$

It sets the upper limit of the frequency of operation as shown in Figure 2.2.

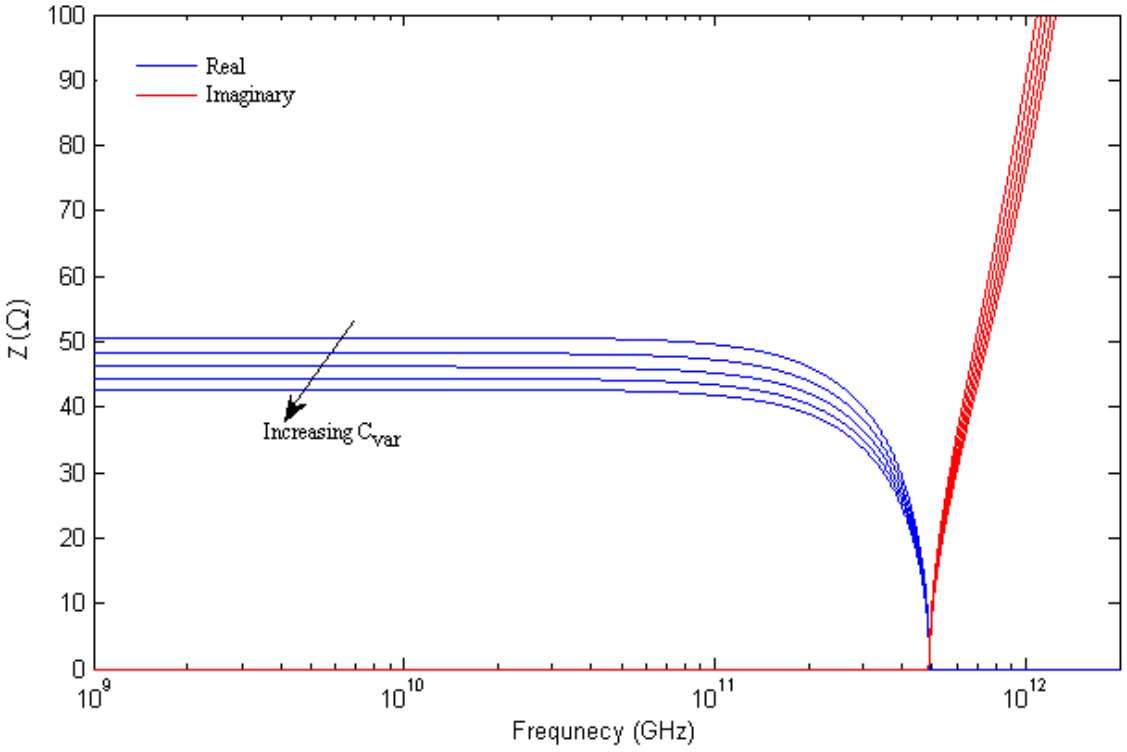


Figure 2.2 Effect of Bragg frequency on line characteristic impedance

Assuming lossless line, the time delay per section of the line is thus given by Equation (2.5)

$$\tau = \sqrt{L_t(C_t + C_{\text{var}})}\left(1 + \frac{\omega^2}{6\omega_b^2} + \cdots\right) \tag{2.5}$$

It is evident that changing the shunt capacitance values results in different time delays, thus creating a true time delay (TTD) phase shifter.

2.2 Literature Review

In literature analog phase shifting has been realized using loaded transmission line, reflection type and vector modulator based techniques. The objective of this section was not to be comparative and exhaustive in referencing all publications (arguably not possible and useful). Thus we limit our discussion to publications limited to implementation of distributed transmission line phase shifters.

N. **S.** Barker and G. M. Rebeiz [2] were the first to present a wide-band true time delay (TTD) phase shifter. Their design consisted of a finite-ground coplanar waveguide (CPW) transmission line fabricated on a quartz substrate with fixed-fixed beam MEMS bridge capacitor. The TTD performance was limited by Bragg frequency. By pulling down on the MEMS bridges, the capacitive loading of the CPW line increases and hence change in phase velocity of the signal, which in turn yields a TTD phase shift. Through measurement, they demonstrated a 0-60GHz TTD with 2-dB loss/118° phase shift at 60GHz and 1.8 dB loss/84° phase shift at 40GHz. Furthermore, they present a transmission line model (Figure 2.3) which fits very well with the measured results. However, the model suffers from limitations, e.g. the skin loss at low-frequencies is not taken into account. Also the attenuation used is the unloaded transmission line, which is different from the loaded transmission line.

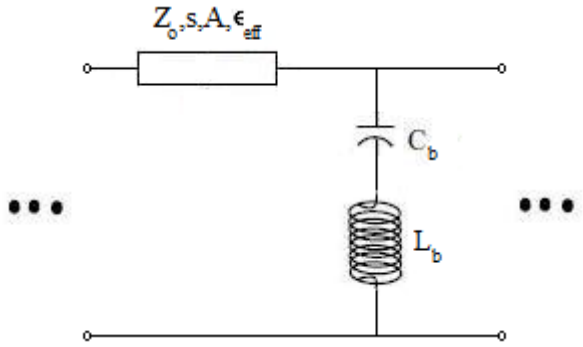


Figure 2.3 Line cell model, where Z_o is unloaded line impedance, s is the periodic spacing of bridge, A is unloaded line attenuation, $\in_{eff}$ is effective dielectric constant, C_b is bridge capacitance and L_b is bridge inductance [2]

They improved on their model in [3] by modeling the line loss by inclusion of a series resistance with line inductance. Also, the effect of series resistance of bridge is accounted by including R_b in series with C_b. The analytic model gives accurate prediction for given set of specifications. They further extend the design to U-band and W-band. The design is optimized for maximum phase shift for minimum insertion loss. The U-band design obtains a $70°$/dB at 40GHz and $90°$/dB at 60GHz. The W-band design gives $70°$/dB for wideband range of 75-110GHz. It is shown that the series bridge resistance (scaled as $\sqrt{f}$) severely impacts the performance of phase shifter in W-band. The phase shift per decibel at 110GHz drops from $115°$/dB for no bridge resistance to $38°$/dB for 0.4Ω bridge resistance. Also, they demonstrate that a 15% and 30% increase in bridge capacitance tuning greatly improves the performance by $50°$/dB and $155°$/dB respectively at 100GHz. Further scaling of frequency is shown to be limited by Bragg

frequency of the periodically loaded line. Figure 2.4 compares the measured and modeled S-parameters and phase shift in W-band for worst case, i.e. maximum bias (26V).

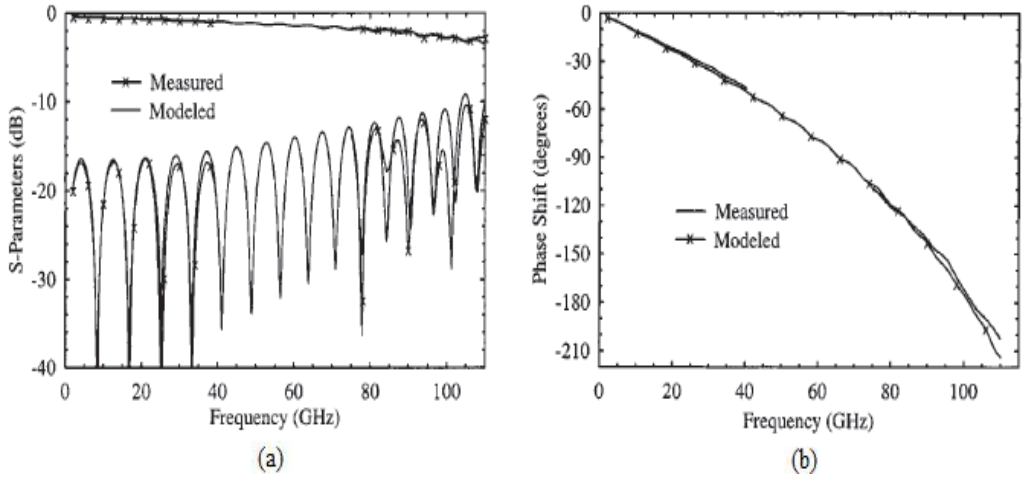


Figure 2.4 (a) S-parameter at maximum bias of 26V (b) Phase shift at maximum bias (26V) [3]

Nagra *et al.* [1] investigated distributed phase shifter using GaAs Schottky diodes. Varactor diodes are used instead of MEMS bridges for variable capacitance. Their optimized design circuits provides a $0-360°$ phase shift at 20GHz with maximum insertion loss of 4.2dB or a $86°$/dB loss at 20GHz. By defining a loading factor ($C_{\text{var}}^{mar} / sC_t$), they analyze the circuit for optimum value of loading factor to minimize the total insertion loss. They also present a propagation matrix model to accurately predict the circuit behavior and valid up till the Bragg frequency. However, scaling of frequency is limited by the diode series resistance on the upper side and large chip size on the lower side. Reducing Schottky contact width and doubling diode perimeter to decrease diode resistance are discussed as potential future work for even high frequency applications.

An ultra-compact varactor loaded transmission line phase shifter at C-band using lumped elements in $0.6\mu m$ GaAs MESFET process is presented by F. Ellinger *et al* [4]. Using single DAC and hence single control voltage, an insertion loss of $4\text{dB} \pm 1.7\text{dB}$ at 5-6GHz range is measured.

D. Kang *et al.* [5] presented a novel digital phase shifter in $0.18\mu m$ RF CMOS technology. Their distributed phase shifter is implemented using distributed active switches that consist of a ladder network of series inductors and shunt capacitances (provided by gate capacitance of common source MOSFETs). The input signal is sampled by the gate circuits at different phases and combined at the output through every activated cascode unit. Figure 2.5 shows the circuit topology and measured phase shift. However, this design is highly susceptible to process and temperature variations. Also, the scaling is limited by f_T of the transistors. It also has a high DC power consumption (~mW).

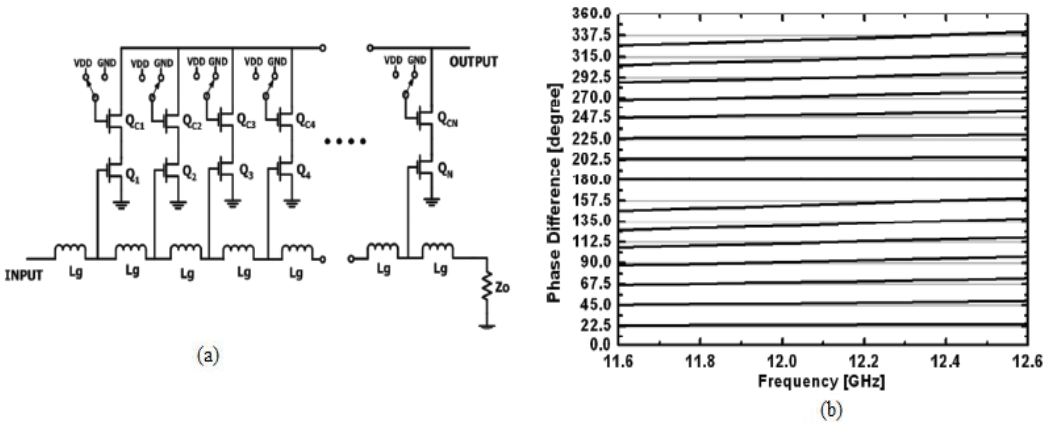


Figure 2.5 (a) Proposed topology (b) Measured 4-bit phase shift in steps of $22.5°$ [5]

Y. Yu *et al.* [6] presented a 60GHz digitally controlled phase shifter in 65nm CMOS technology using a differential varactor-loaded differential transmission line architecture, as shown in Figure 2.6.

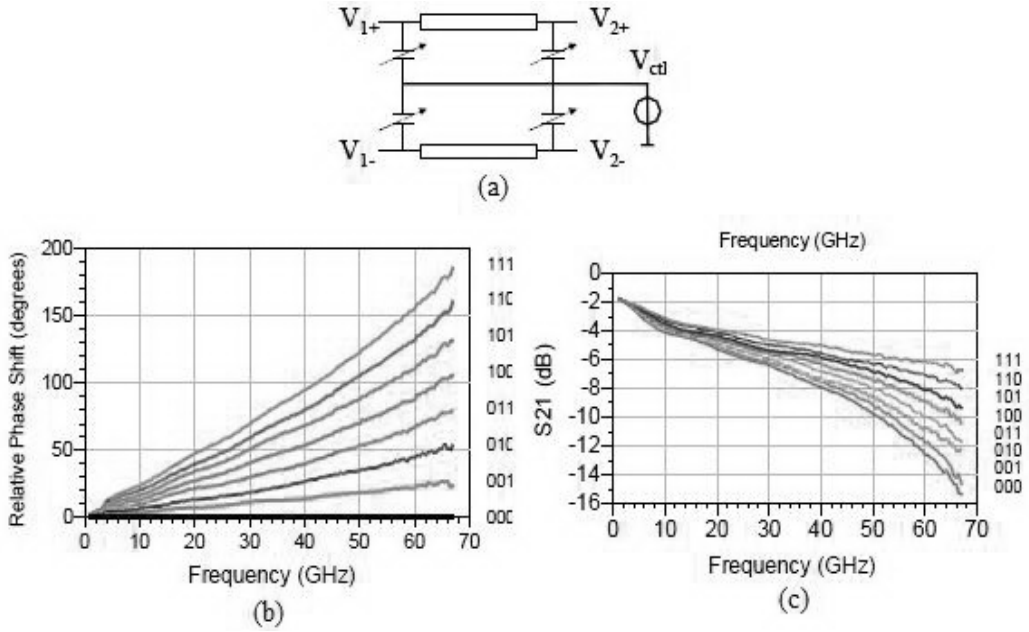


Figure 2.6 (a) Proposed differential phase shifter loaded with differential varactors (b) Relative phase shift for 8 different states (c) Corresponding insertion loss [6]

The differential gates of MOS varactors are connected to the differential terminals of the transmission line and the n-well to the DC control voltage. The differential phase shifters only required to achieve a $180°$, as the differential path can be swapped to provide a full $0-360°$ phase shift. Another advantage is elimination of low-impedance AC ground for n-well. With a phase resolution of $22.5°$ an average insertion loss of 8.5-10.3dB is achieved from 55-65GHz.

Liang-Hung Lu *et al.* [7] employed active inductors in synthetic transmission line architecture to implement a continuous phase shifter with measured insertion loss than 1.1dB for full $0-360°$ phase change from 3.5GHz to 4.5GHz in $0.18\mu m$ CMOS process. The phase tuning is controlled by the transistor bias currents, since the input impedance of an active inductor is dependent on the bias currents. Figure 2.7 shows the proposed synthetic unit of transmission line with active inductor and schematic of cascode active inductor along with measured 4GHz S-parameter results.

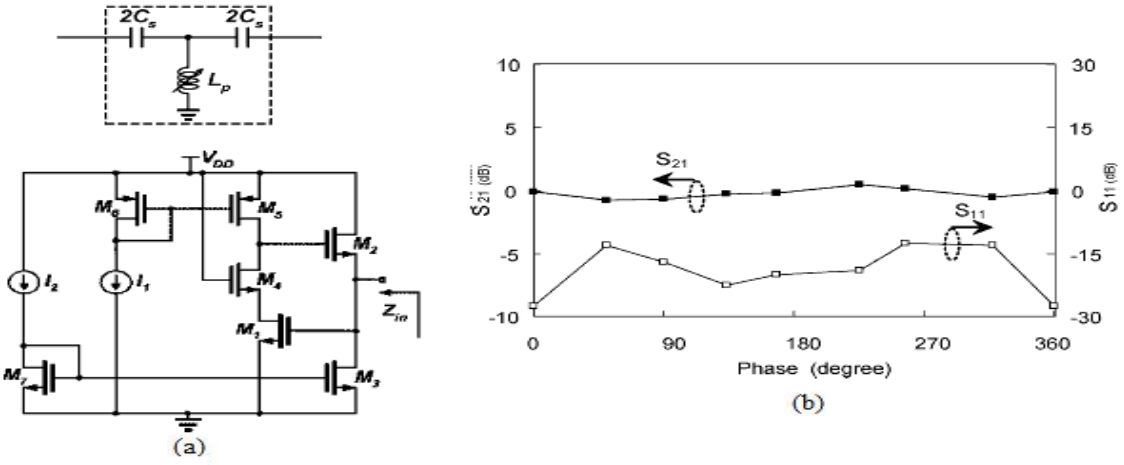


Figure 2.7 (a) Proposed line with tunable inductance with schematic (b) Measured S-parameters at 4GHz [7]

CHAPTER 3

VARACTORS

3.1 Introduction

Varactor is a tunable passive device used as a variable capacitor. Varactors exhibit low losses, i.e. a high quality factor (Q), sufficient tuning range $(\Delta C / \Delta V)$, low parasitic capacitance and high linearity at radio frequencies. In today's low supply voltage trend, varactors have a high capacitive tuning ratio with a low voltage tuning range.

3.2 Varactor Structures

3.2.1 MOS Varactor

Available in IBM CMS9FLP library are the thin and thick oxide NFET in n-well models (HSPICE and SPECTRE models *ncap* and *dgncap* respectively). Figure 3.1 shows the cross section of MOS varactor. The MOS varactor n+ drain and source diffusions are in n-well.

MOS varactor variable capacitance is achieved by controlling the gate-to-diffusion/n-well voltage V_{gd}, which forces electrons to accumulate in the silicon surface

beneath the gate. With a positive V_{gd}, the MOS varactor behaves like a parallel-plate capacitor with an accumulation layer below the silicon layer. The device capacitance equals the gate-oxide capacitance. When reverse-biased, a depletion layer is formed in the n-well directly under the gate. Due to the depletion capacitance in series with the gate-oxide capacitance the device capacitance decreases, reaching a minimum when the applied reverse bias voltage is equal to the threshold value.

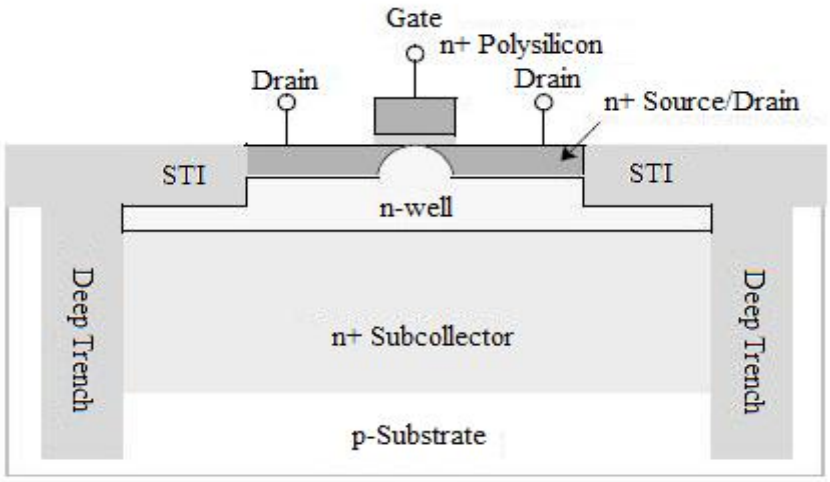


Figure 3.1 MOS varactor

3.2.2 pn-junction Varactor

Available is a hyper-abrupt (HA) junction varactor (HSPICE and SPECTRE model *havar*). HA varactors are derived from p-n-junctions where it's doping profile changes in a controlled non-linear way with density of the dopants increasing toward the junction and abruptly dropping to zero at the junction. Figure 3.2 shows the cross section of a HA diode varactor. The varactor p-n junction is always reverse biased and it

functions as a capacitor because the reverse bias voltage causes charge carriers to move away from the p-n junction. The opposite edges of the p and n regions collect the charge and act as the conductive plates of a cathode and an anode. As the carriers move away from the p-n junction, a depletion region near the junction is formed which is the equivalent to the dielectric of a conventional capacitor. As the reverse voltage is increased, the charge carriers move further away from the p-n junction, which causes the varactor capacitance to decrease. The varactor capacitance is therefore tunable by the reverse bias voltage, and the value of the capacitance depends on the junction area and the doping profile in the junction.

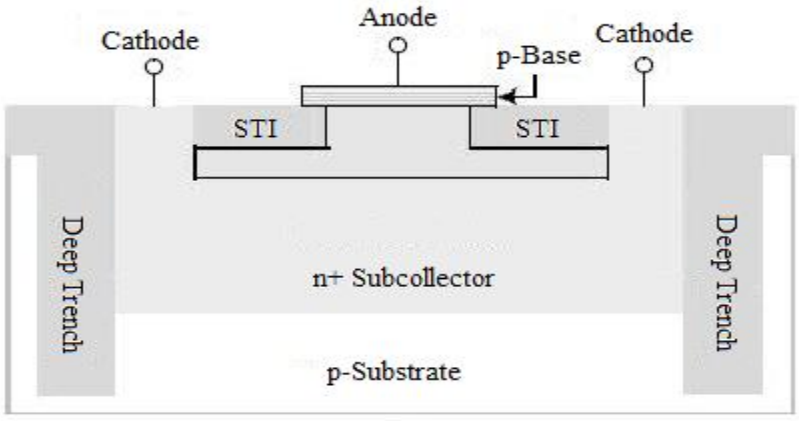


Figure 3.2 pn-junction varactor

3.3 Varactor Simulations

The tuning range and quality factor value are the two most key parameters of

varactor performance. This section describes the simulation methodology and issues related to understand key varactor characteristics.

Figure 3.3 shows the one-port schematic. Large capacitor (10μF) and inductor (10H) are used to isolate dc and RF signal paths. However, the series resistance (R_{wire}) and inductance (L_{wire}) to represent the wiring parasitic are not taken into account. All the varactor substrate connection passes through the spreading resistance of the lightly doped substrate, which affects the high-frequency varactor performance. A value of 50 Ω is used for the simulation purpose. A substrate contact model representing the connection from the metal layers to the substrate is used $(subc)$. They are important because they minimize local potential variations to prevent latch-up, maintain substrate potential at desired level and aid in noise isolation.

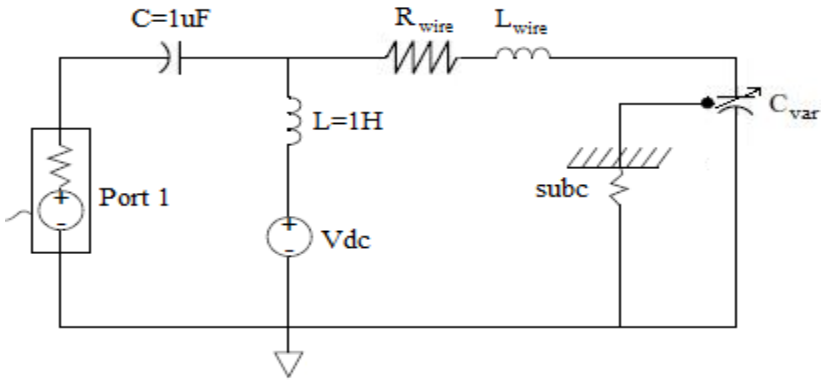


Figure 3.3 One-port simulation circuit

The varactor capacitance and quality factor can be calculated from the Y parameters using the Equations 3.1 and 3.2, respectively.

$$C = \frac{imag(Y_{11})}{2\pi f} \tag{3.1}$$

$$Q = \frac{imag(Y_{11})}{real(Y_{11})} \tag{3.2}$$

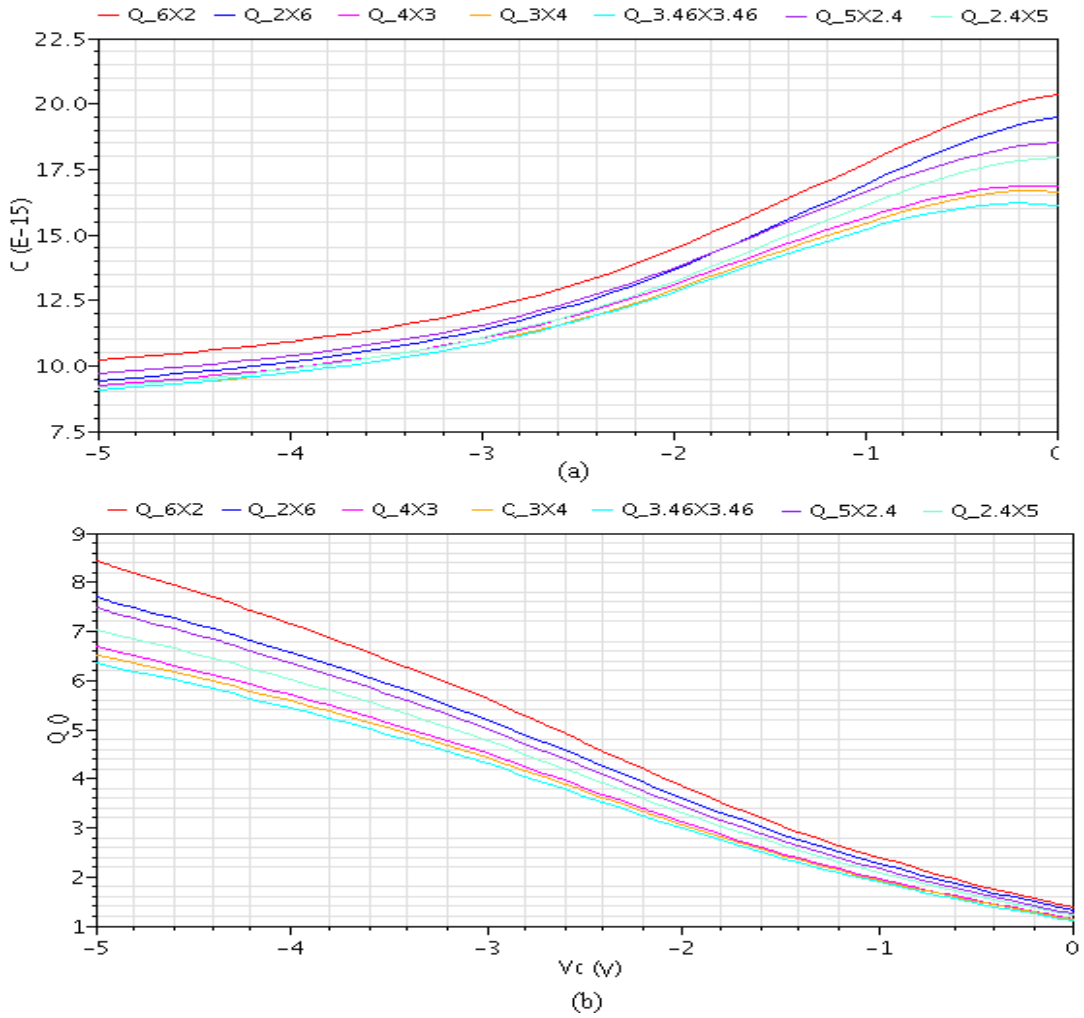


Figure 3.4 (a) capacitance (b) quality factor vs. junction area at 100 GHz

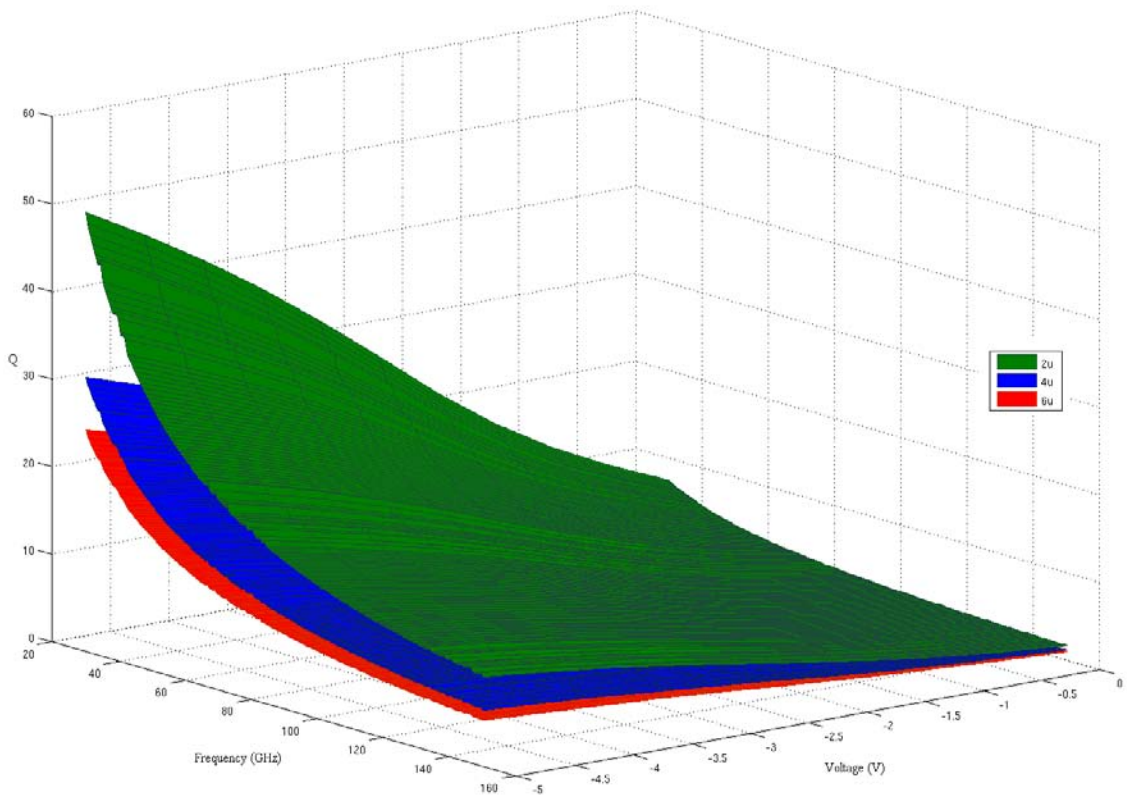


Figure 3.5 Quality factor performance vs. frequency and reverse bias voltage for varying anode length

For same junction area, the capacitance is the same, as shown in Figure 3.4. However, narrower devices exhibit higher quality factor than the squarer ones. As expected, the quality factor decreases with increasing frequency and decreasing reverse bias voltage. With increase in frequency, the parasitic resistance increases and with decreasing reverse bias, the capacitance decreases and hence the quality factor performance trend (Figure 3.5). Also, smaller length gives better quality factor, because the anode length drives the diode series resistance. Similarly, increase in width decrease the quality factor.

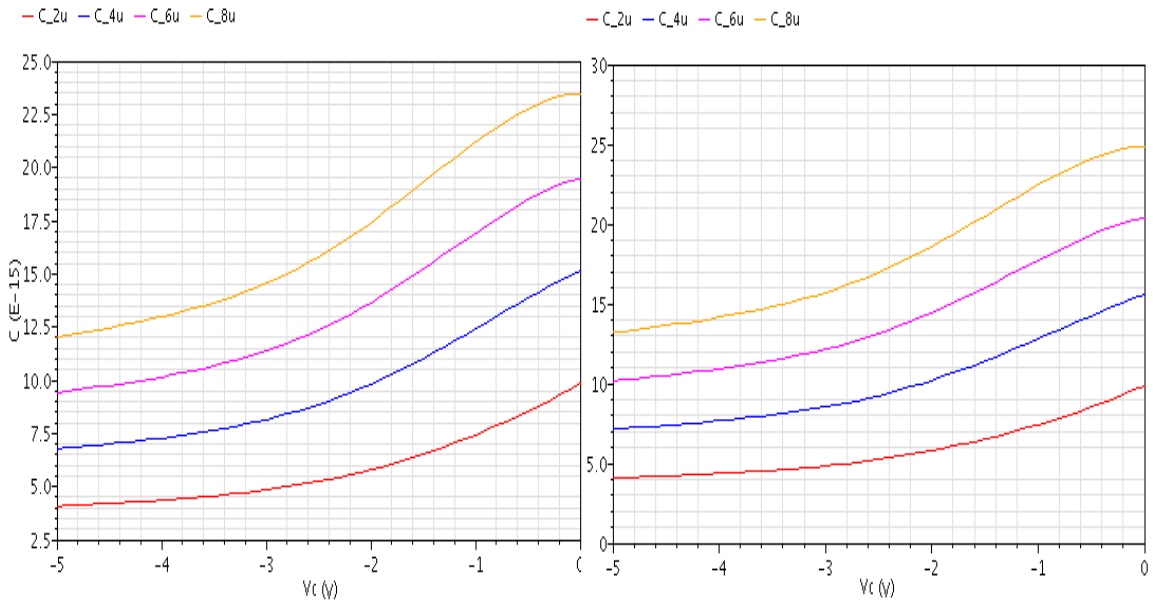


Figure 3.6 capacitance vs. (a) anode length (b) anode width at 100 GHz

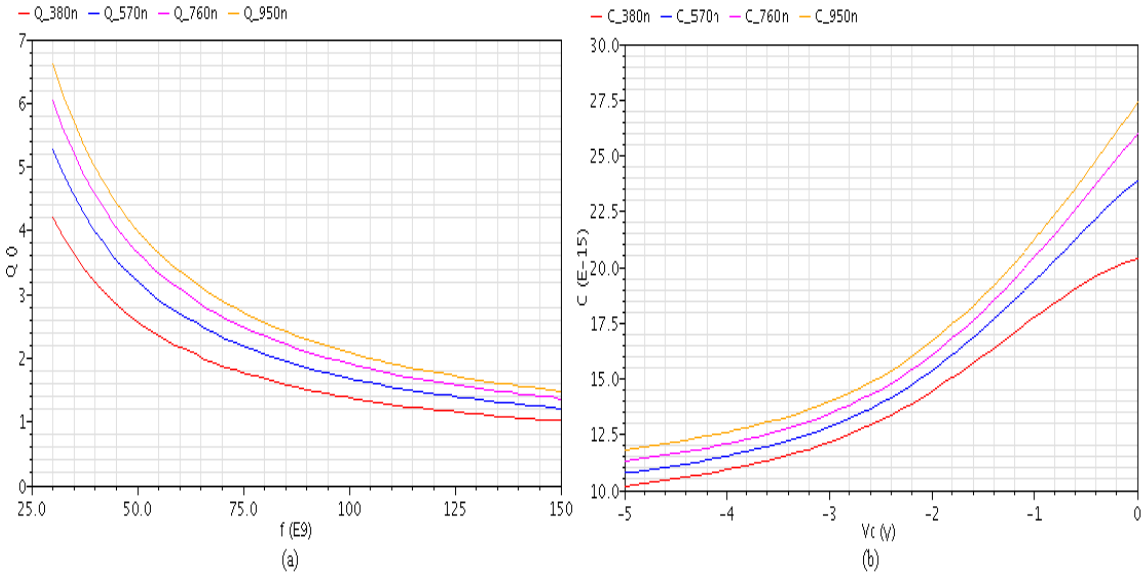


Figure 3.7 (a) quality factor vs. frequency (b) capacitance vs. reverse bias voltage, for different cathode widths

Increase in width/length increases the capacitance but the tuning ratio remains close to 2.1 (Figure 3.6). The effect of cathode width on the quality factor and capacitance value is shown in Figure 3.7. Note that the capacitance can be scaled by multiplicity. Number of channels and Rx repetition do not affect the quality factor.

Figure 3.8 and Figure 3.9 shows the quality factor performance for thin-oxide MOS varactor. Increasing frequency and decreasing capacitance decreases the quality factor. Wider varactor device exhibits lower quality factor. Variation of capacitance with widths and lengths is shown in Figure 3.10. The tuning range remains constant, close to 4. However, a large value of length decreases the tuning range with a bump in the C-V characteristic. Again, the quality factor is unaffected by the number of channels and Rx repetition. Similar performance trend is observed with the thick-oxide MOS varactor. However, the thick-oxide has a larger voltage range (-0.5 to $1.25V_{DD}$) but has a lower tuning range (~2.2) in compression with the thin-oxide device.

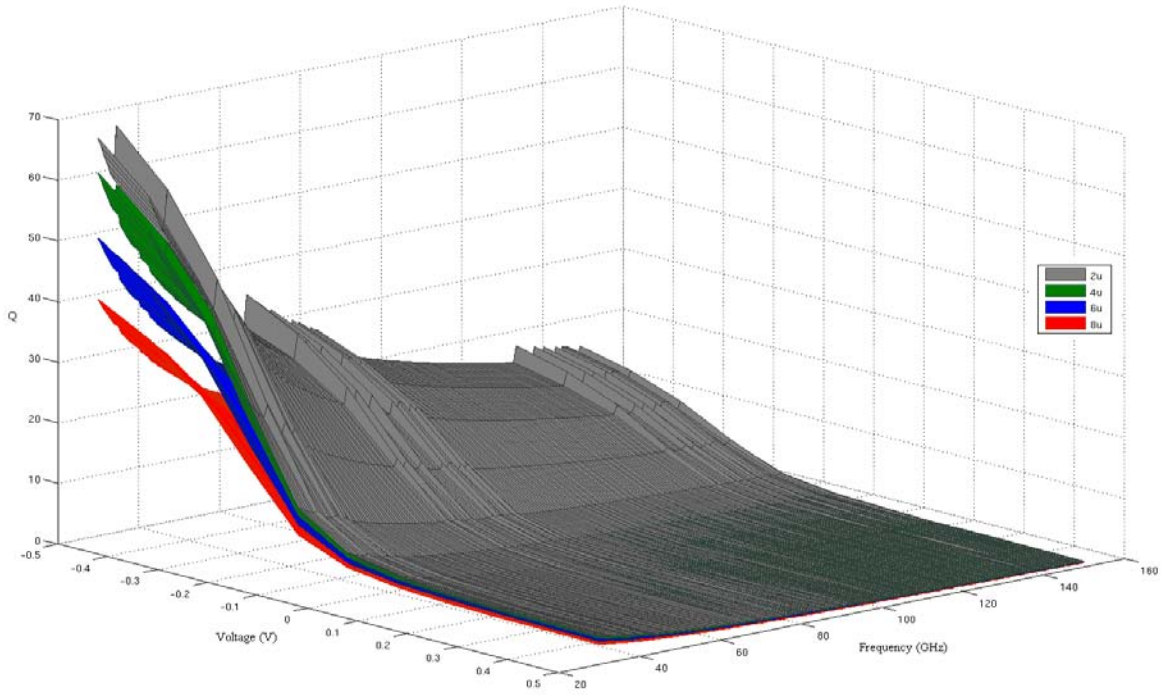


Figure 3.8 Quality factor performance vs. frequency and voltage for varying width

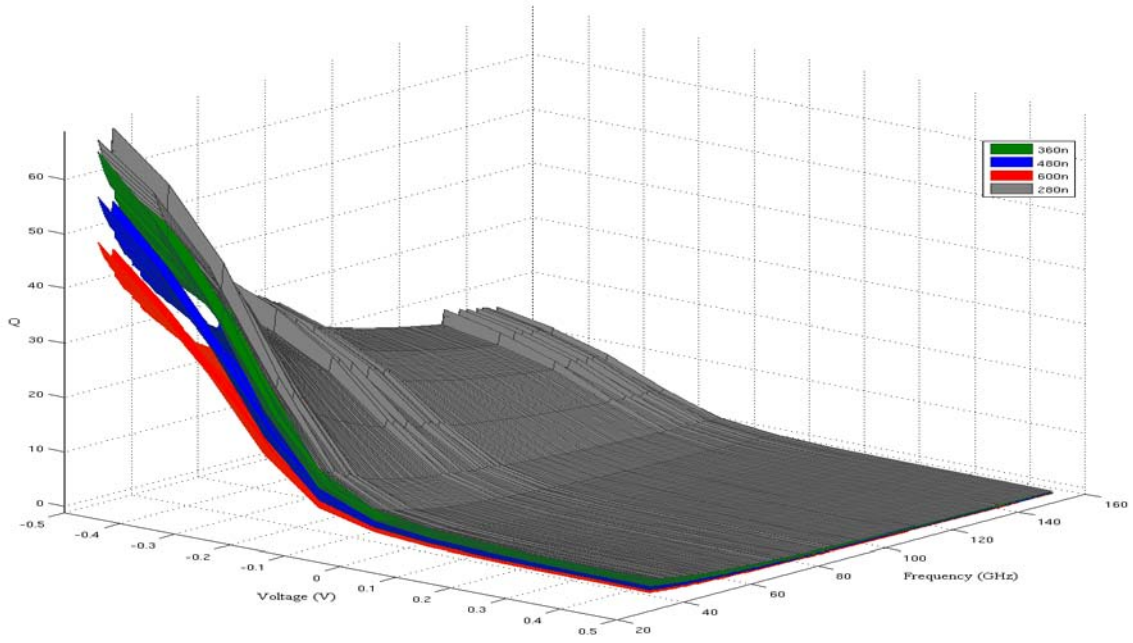


Figure 3.9 Quality factor performance vs. frequency and voltage for varying length

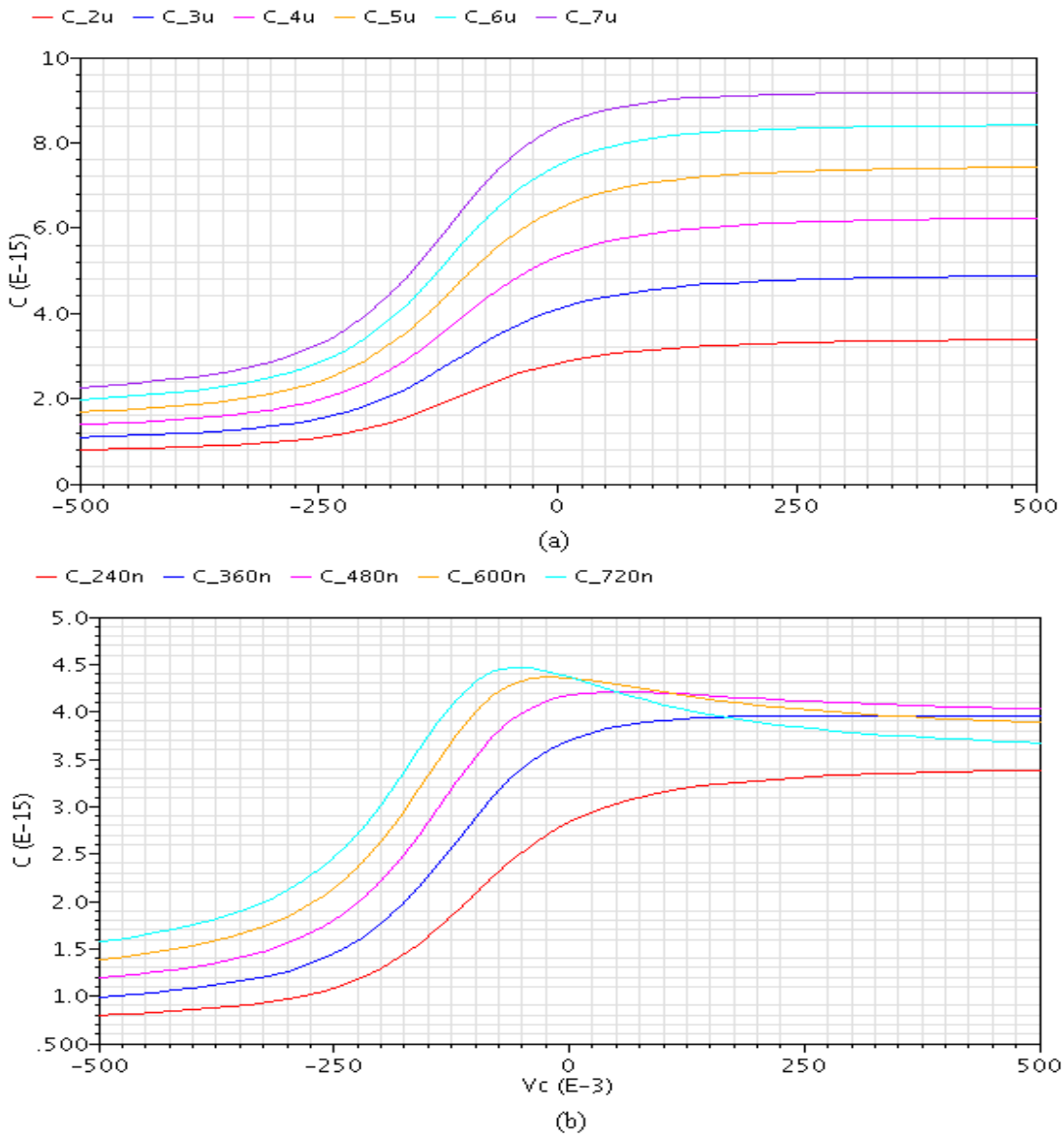


Figure 3.10 Capacitance vs. (a) width (b) length at 100 GHz

CHAPTER 4

DESIGN AND SIMULATION RESULTS

4.1 System Modeling

The hypothesis of combining loaded transmission line phase shifter with out-of-phase amplifier in a feedback loop to implement a voltage controlled oscillator was verified by doing a simulation level simulation in ADS. Figure 4.1 shows the system level schematic.

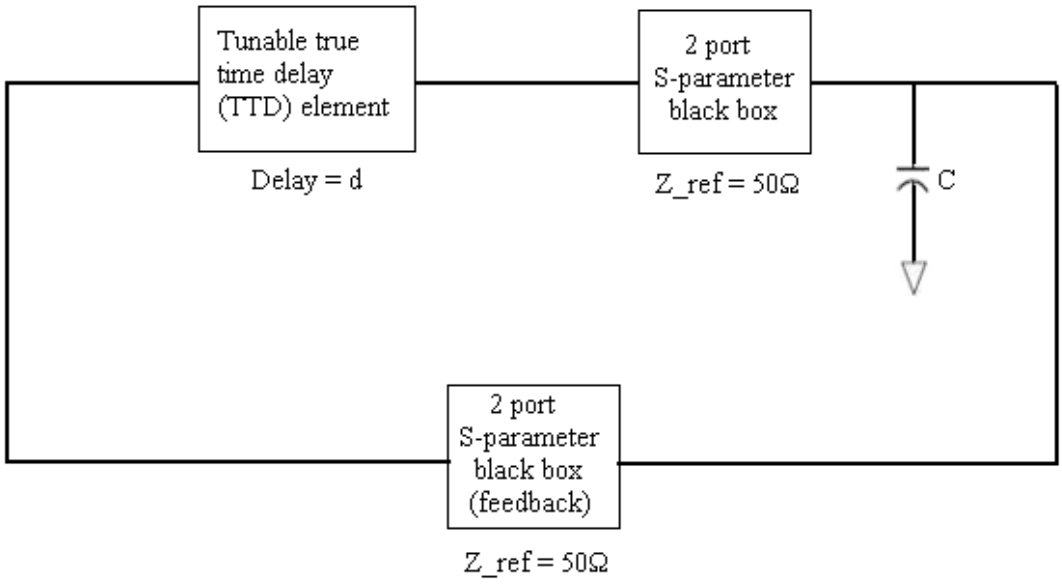


Figure 4.1 System level schematic

Figure 4.2 shows the simulation result. The time period of the system is double than that of the time delay path. This is because the amplifier provides a $-ve$ feedback, thus the signal has to travel twice around the loop to regain its original polarity. Amplifier also compensates for the losses incurred from the time delay path, thus leading to the non-decaying building of oscillations. As shown, for a delay of $5ns$ the time period is $10ns$. Same results were obtained for different values of delay. The capacitor C mimics the capacitive nature of the transmission line and produces a sinusoidal waveform instead of a square wave at output.

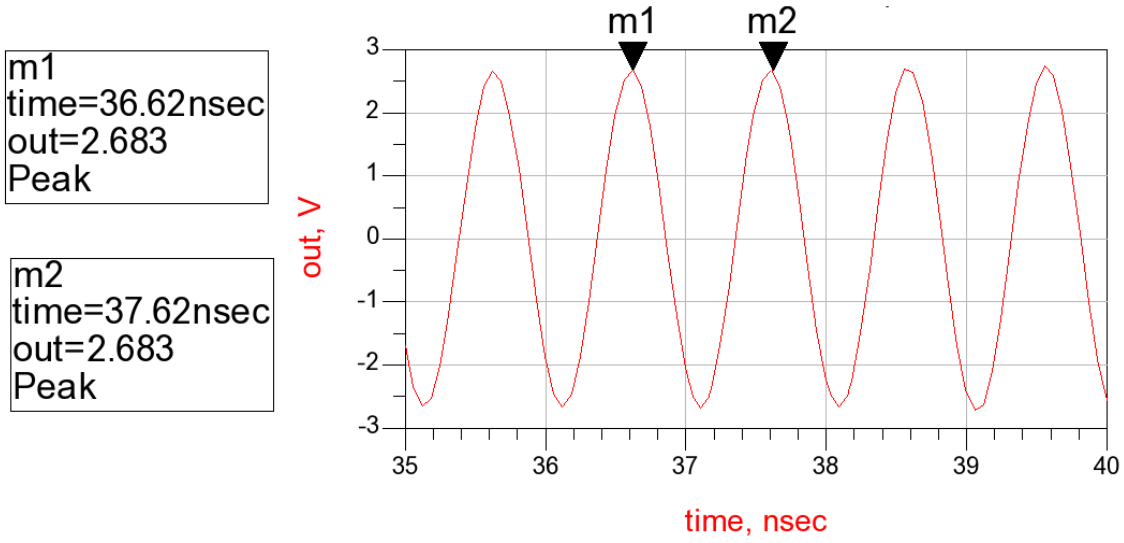


Figure 4.2 System level simulation results

4.2 System Topology

Tunable time delay is achieved by varying the reactance of the line. Thus by

coupling/de-coupling transmissions lines in or out of the signal path or by coupling/de-coupling capacitors in or out at periodic intervals of the transmission lines or simply loading the line periodically, control over the reactance of the line can be obtained.

4.2.1 Switch Topology

As shown in Figure 4.3 (a) switch is used to couple capacitors to the transmission line. More control on tuning can be achieved by inserting switches in the capacitor grid, analogous to programmable array logic. This topology can take advantages of using mim (metal-insulate-metal) caps owing to their excellent Q performance and low parasitics at higher frequencies. Another advantage is absence of control voltage present all the time. This eliminates static power dissipation. However, mim-caps take large area and this topology can only provide discrete step size of variation in shunt reactance. Another approach is to vary the length of the transmission line by coupling or decoupling lines in the signal path (Figure 4.3 (b)). If the switch is ON, then the line is shorted and thus the line is switched OFF. The line adds no delay to the signal. However, if the switch is OFF, the line is switched ON into the circuit. Depending upon the length of the line, the signal suffers specific amount of true time delay. However, this method is crude and inefficient way of tuning.

The critical aspect of switch topology is the proper working of the switch. Thus we investigate the feasibility of using a switch at such high frequencies. A switch is a simple MOS structure with control voltage applied at the gate. When ON, it presents a resistance value of R_{ON}, while R_{OFF} when OFF. The ratio R_{OFF}/R_{ON} should be at least

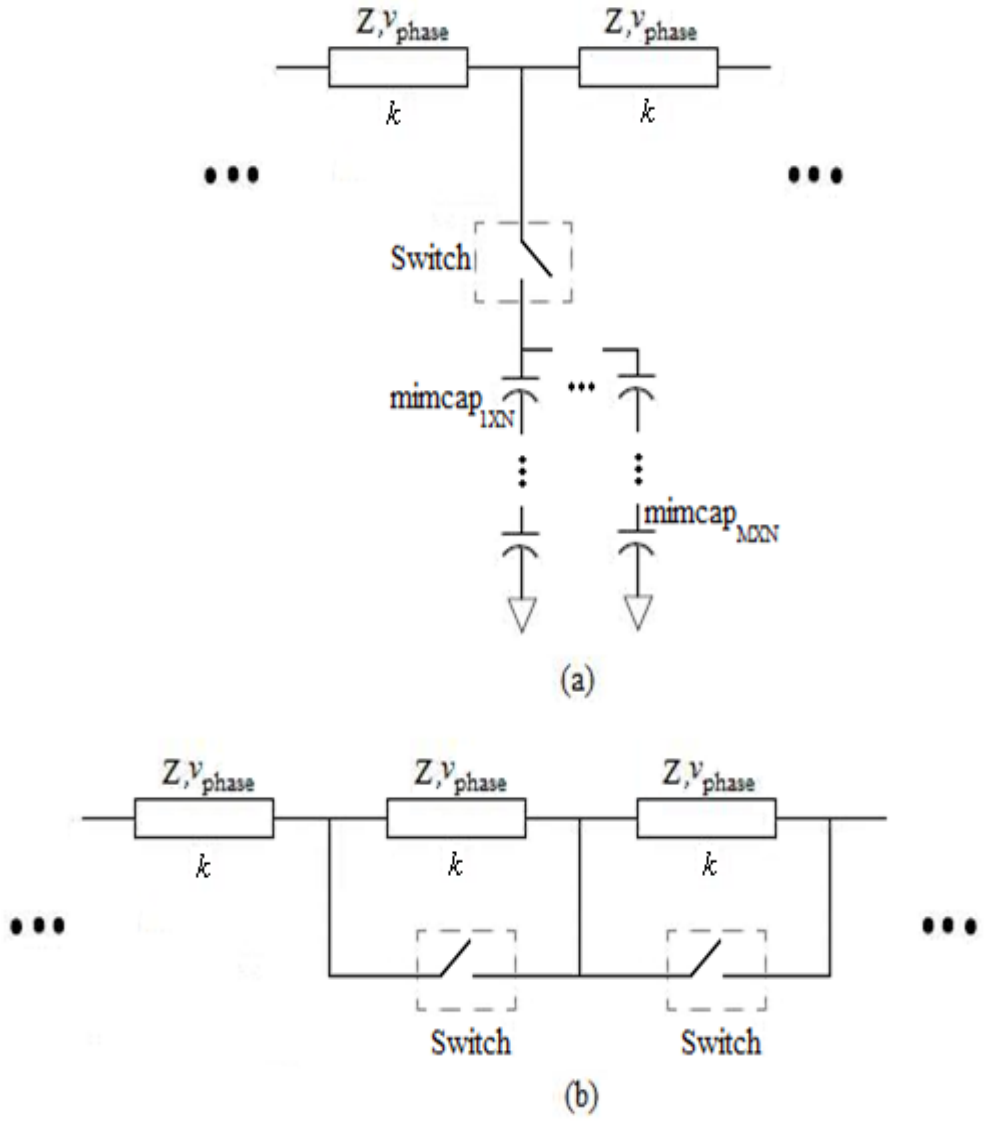


Figure 4.3 (a) Switch-cap structure (b) Switch-line structure

of order of 1000 for proper switch operation. However as the frequency increases, the channel resistance is shunted by the low substrate contact resistance. Figure 4.4 shows the cross-sectional view of a NMOS switch and its equivalent model.

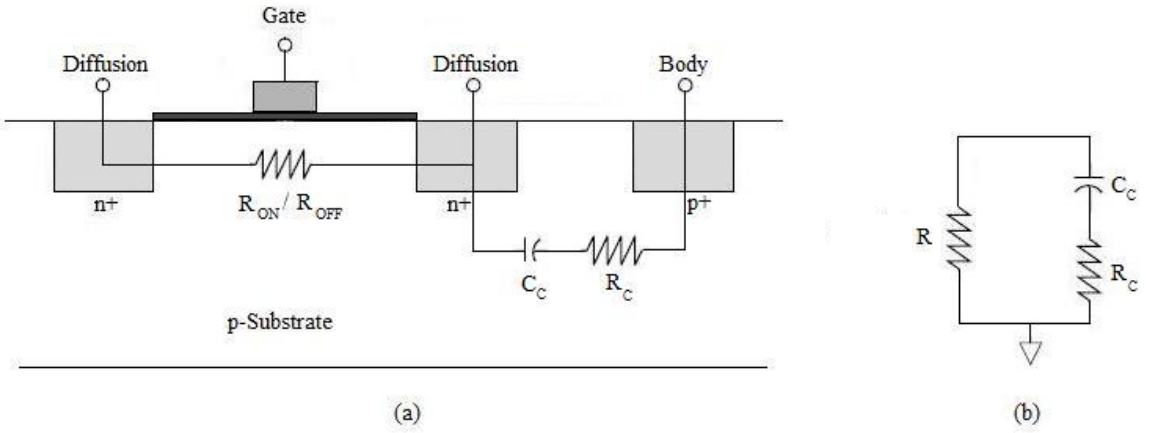


Figure 4.4 (a) NMOS switch cross section (b) Equivalent switch resistance model

The substrate contact capacitance C_C isolates the substrate contact resistance R_C if the frequency of operation is fairly low. However as the frequency increases, X_C decreases and as a result R_C comes into parallel to the channel resistance and dominates over it. As a result, the ratio R_{OFF}/R_{ON} and hence switch operation suffers. Through DC analysis, R_{OFF} was found to be 218.9 GΩ and R_{ON} equal to 638.2 Ω for a minimum dimension NMOS switch. The ratio R_{OFF}/R_{ON} was only 2 at 100 GHz. S-parameter simulations were done to obtain Y-parameters. Using Equation (4.1) and Equation (4.2) and assuming, $\frac{1}{R} \approx 0$ for switch OFF case, R_C and C_C values were found to be 128.325 Ω and 14.6 *fF* respectively.

$$real(Y) = \frac{1}{R} + \frac{w^2 C_C^2 R_C}{1 + w^2 C_C^2 R_C^2} \tag{4.1}$$

$$imag(Y) = \frac{wC_C}{1 + w^2 C_C^2 R_C^2} \tag{4.2}$$

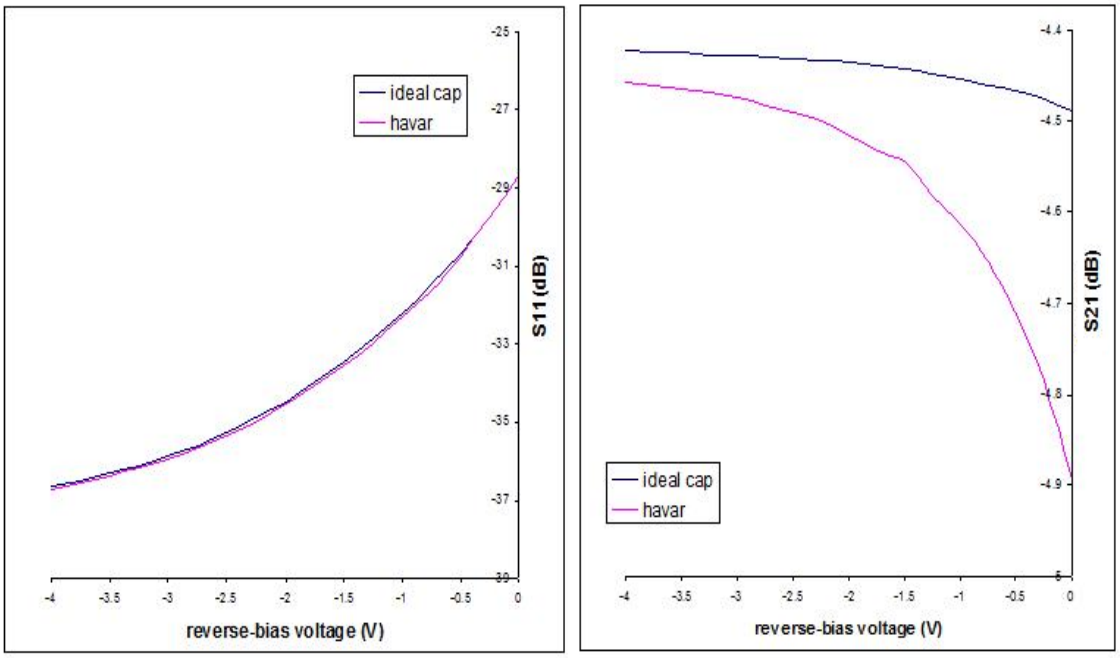
4.2.2 Periodic Loading Topology

Eliminating the choice of using a switch in W/V-band, we explore the other topology of adding varactors periodically to the transmission line. A single supply voltage is used to tune the varactors. Also, this analog type of tuning enables us to tune to any value of desired time delay. This topology however suffers from relatively heavy insertion loss due to poor varactor quality factor at high frequencies. To further the analysis, the total insertion loss by loading a CPW line with varactor diodes is given by Equation (4.3) [1]

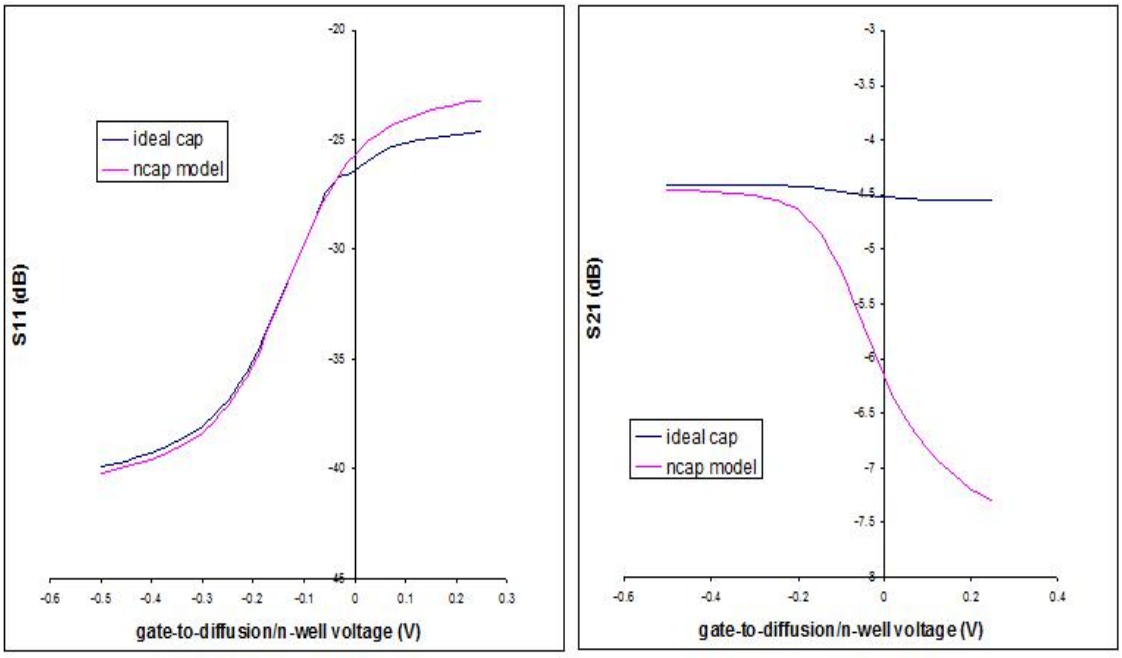
$$IL = n\pi \frac{f^2}{f_s} C_{\text{var}}^{\max} Z_L + nk\alpha(Z_i)\frac{Z_i}{Z_L} \tag{4.3}$$

Where n is the number of sections of length s, f_s is the diode cutoff frequency, $\alpha(Z_i)$ is attenuation per unit length and $\frac{Z_i}{Z_L}$ is the loading factor. The first term describes the diode loss, while the second term reflects the skin losses in the CPW line.

The diode loss limits the tuning range and the frequency of operation. Figure 4.5 compares the performance of ideal varactor versus varactor junction (*havar*) and MOS (*ncap*) varactor models in IBM $90nm$ CMOS process at 100GHz. Clearly $S11$ is unaffected as quality factor has insignificant impact on mismatching along the line.



(a)



(b)

Figure 4.5 (a) Hyper abrupt pn junction varactor (b) Thin-oxide NMOS varactor

4.3 Transmission Line Design

We analyze in detail a CPW (coplanar waveguide) line. CPW lines provide extremely high frequency response (100 GHz or more) since connecting to CPW does not entail any parasitic discontinuities in the ground plane. Other advantages of using CPW include low ground inductance for shunt elements, elimination of backside processing (thinning, via etch, backside plating), minimal cross-talk between lines and low radiation losses. However disadvantages include potentially higher heat dissipation and lower dielectric constant (half of the fields are in air) than microstrip lines [8]. Figure 4.6 shows a conventional CPW line.

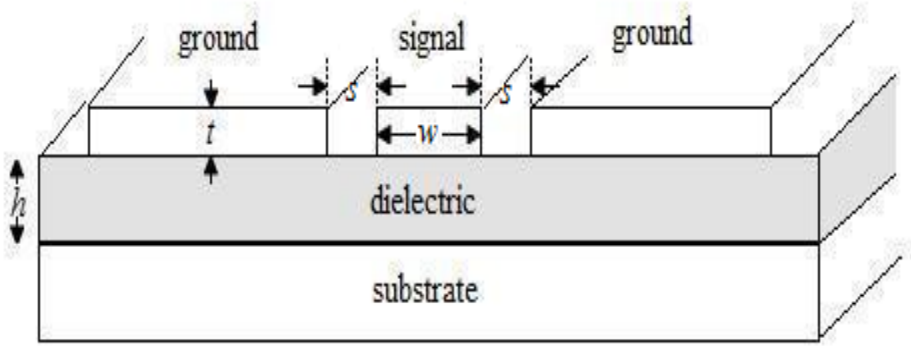


Figure 4.6 Conventional CPW

For years, the substrate losses and inferior Q values of passive components had starnged the realization of MMIC phase shifters in CMOS. However with recent advancement in fabrication technology CMOS MMIC applications have begun to pickup.

Thus CPW in CMOS 90nm technology was researched. Table 4.1 lists the substrate parameters.

Relative dielectric constant ε_r	Relative permeability	Substrate thickness h	Conductor thickness t	Conductor conductivity	Dielectric loss tangent	Conductor surface roughness
3.9	1.00	25 μm	0.90 μm	2.5e7 Sm^{-1}	0.20	0.00 m

Table 4.1 Substrate parameters

Adding shunt capacitance leads to mismatch along the line and hence insertion loss at the output. To minimize this mismatching, either the unit cell capcaitance of the line should be made much larger than the variable capacitance or vice-versa. Former is attempted in this research because later would suffer from large losses due to higher parasitic resistance. Simulations were carried to increase the per unit length capacitance of the line keeping the characteristic impedance of the line to be 50Ω. The LineCalc ulitity in ADS synthesizes the physical dimenions of the CPW line for given substrate, frequency of operation, impedance of the line and desired differential phase shift. These were used in S-parameter simulations to extract the lumped element values, using Equations (4.4) - (4.6).

Note here $S_{11} = S_{22}$ and $S_{12} = S_{21}$ as CPW is a symmetrical structure.

$$Z = Z_0 \sqrt{\frac{(1+S_{11})^2 - S_{12}^2}{(1-S_{11})^2 - S_{12}^2}} \tag{4.4}$$

$$e^{-\gamma L} = \frac{1 - S_{11}^2 + S_{12}^2}{2S_{12}} + K$$

$$where, \quad K = \sqrt{\frac{\left(1 - S_{12}^2 + S_{12}^2\right)^2 - 4S_{12}^2}{4S_{12}^2}}$$

(4.5)

$$R = real(Z * \gamma L)$$

$$L = img(Z * \gamma L) / w$$

$$G = real(\gamma L / Z)$$

$$C = img(\gamma L / Z) / w$$

(4.6)

Where R is the resistance in series with the inductance per unit cell (L) of the line. It represents the losses due to skin effect at higher frequencies. G is the conductance in parallel with the capacitance per unit cell (C) of the line. It represents the losses through the substrate. L is the length of each section.

Simulations were carried out at 100 GHz. The length of the line was chosen to get 180° phase shift at the output. The calculated length was 1.044mm. Dimensions of the line were varied for a constant line characteristic impedance of 50Ω. Results are tabulated as seen in Table 4.2. Clearly at the conductor width of 20.628μm and spacing of 3μm, the capacitance per unit cell is the maximum with a value of ~100*f*F. Bringing the conductors too close increases the loss through them substantially, evident by the increase in value of R.

$S(\mu m)$	$W(\mu m)$	$C_t\left(pF/m\right)$	$L_t\left(nH/m\right)$	Z	$R(130.5\mu m)\Omega$	$G(130.5\mu m)\Omega^{-1}$
0.3	0.0182	80.8	17.2	138.3-123i	227.19	3.6e-04
0.4	0.117	79.4	19.86	70.78-44.8i	42.87	5.1e-4
0.6	0.804	86.91	21.73	52.94–251i	11.52	7.8e-04
0.8	1.8873	90.95	22.74	51.1–5.995i	6.92	9.2e-04
1.0	2.965	93.46	23.36	50.53-3.26i	5.09	0.001
1.3	5.00	95.36	24.05	50.38-1.08i	3.6	0.0011
1.5	6.6659	96.83	24.2	50.03-0.2i	2.97	0.0011
1.8	9.147	97.79	24.47	49.91-0.7i	2.38	0.0012
2.0	10.896	98.39	24.59	49.86+1.1i	2.1	0.0012
2.2	12.711	98.75	24.69	49.82+1.3i	1.87	0.0012
2.5	15.55	99.1	24.78	49.78+1.3i	1.61	0.0012
2.7	17.533	99.2	24.81	49.76+1.84i	1.476	0.0012
3.0	20.628	99.35	24.83	49.73+2.0i	1.3	0.0012
3.5	26.155	99.2	24.81	49.71+2.3i	1.08	0.0012
4.0	32.191	98.9	24.73	49.09+2.4i	0.92	0.0012
4.5	38.797	98.4	24.6	49.69+2.6i	0.801	0.0012
5.0	46.022	97.7	24.46	49.68+2.6i	0.702	0.0012
6.0	62.404	96.3	24.08	49.68+2.6i	0.55	0.0011
7.0	81.274	94.8	23.7	49.69+2.7i	0.45	0.0011
8.0	102.347	93.4	23.3	49.7+0.7i	0.38	0.001
9.0	125.426	92.1	23.0	49.71+2.7i	0.33	9.6e-04
10.0	150.445	90.9	22.7	49.72+2.7i	0.29	9.2e-04
11.0	177.131	89.9	22.4	49.73+2.6i	0.262	8.9e-04
12.0	205.4	89.0	22.2	49.74+2.65i	0.234	8.62e-04
13.0	235.196	88.2	22.0	49.74+2.6i	0.21	8.33e-04
14.0	266.4	87.4	21.8	49.77+2.6i	0.193	8.06e-04
15.0	299.131	86.7	21.6	49.78+2.5i	0.177	7.82e-04
17.5	386.716	85.2	21.3	49.78+2.4i	0.146	7.2 e-04
20.0	482.219	83.9	20.9	49.82+2.28i	0.123	6.81e-04

Table 4.2 Variation of line unit cell element values with CPW physical dimensions

As supported by the Equation (2.4), increasing the number of sections increases the Bragg frequency. However, for same differential phase shift at output, the value of shunt capacitance decreases beyond minimum attainable with increasing sectioning $(<1fF)$. Also, more sections implies more shunt capacitances, thus more mismatch along the line and thus increase in S_{11}, as evident from Table 4.3. However for 2 section line,

the Bragg frequency is very close to operating center frequency of 100 GHz. Thus, the anomaly with Z and S11 value, supported by Equation (2.3).

# of sections	2	4	6	8	10	12	14	16
$S(\mu m)$	522	261	174	130.5	104.4	87	74.57	65.25
$C_{\text{var}}(fF)$	5	2.5	1.67	1.25	1	0.833	0.714	0.625
$f_b(GHz)$	122	244.63	366.9	489.26	611.5	733.9	856.23	1021.9
Z	33.72	47.60	47.68	47.69	47.69	47.69	47.69	47.69
$S_{21}(dB)$ @100GHz	-4.53	-4.42	-4.42	-4.41	-4.41	-4.41	-4.41	-4.41
$S_{11}(dB)$ @100GHz	-21.09	-38.81	-38.45	-37.64	-37.39	-37.14	-37.01	-36.98
$\Delta\angle S_{21}(\text{deg})$ @100GHz	9.02	8.943	8.944	8.914	8.91	8.904	8.907	8.91

Table 4.3 Effect of sectioning on Bragg frequency

4.4 Phase Shifter Simulations

The critical performance metrics for true time delay phase shifters are insertion loss and return loss (typically $< -10dB$) for achieving given delay in desired frequency range. Circuit was optimized and simulated to achieve 20% bandwidth with center frequency of 100 GHz. Table 4.3 allows the selection of an 8-section CPW line to be an appropriate choice as Bragg frequency (~489 GHz) is much larger than maximum frequency of operation (110 GHz). The varactor has some finite capacitance value at 0.0V, thus the length of each section was tailored to achieve 100 GHz center frequency.

Figure 4.7 shows the 100 GHz transient response. Thin-oxide NMOS was used with width and length of 3µm and 240n respectively with multiplicity of 5. The length of

each section was 115µm. A -0.5V leads to a delay of 4.24ps, while 0.5V a delay of 5.51ps. The oscillating frequency is calculated using Equation (4.7) and summarized in Table 4.4. The S-parameters simulations results are shown in Figure 4.9. The worst case insertion loss is kept at 8.03dB while return loss is always less than 15dB. The bandwidth obtained is 27.18%.

To operate at different frequency band, the circuit requires scaling of the line and varactor dimensions to meet the specifications. To demonstrate the robustness of the concept, another set of simulations were performed in V-band, with center frequency of 60 GHz. Table 4.5 summarizes the simulation result. The bandwidth is 29.87%. Figure 4.8 shows the transient analysis simulation result. The S-parameter results are shown in Figure 4.9. In this case, thick-oxide NMOS varactor was used with width and length of 1µm and 240n respectively with multiplicity of 10. Length of each section was 185µm.

$$Frequency = \frac{1}{2 * Delay} \tag{4.7}$$

Voltage (V)	Delay (ps)	Frequency (GHz)	S11 (dB)	S21 (dB)
-0.5	4.24	117.924	-30.10	-5.17
0	5.00	100	-19.02	-6.74
0.5	5.51	90.744	-16.18	-8.03

Table 4.4 Result summary (W-band)

Voltage (V)	Delay (ps)	Frequency (GHz)	S11 (dB)	S21 (dB)
-0.5	6.89	72.568	-19.20	-5.29
0	8.33	60	-13.95	-7.22
0.5	9.15	54.644	-12.81	-8.26

Table 4.5 Result summary (V-band)

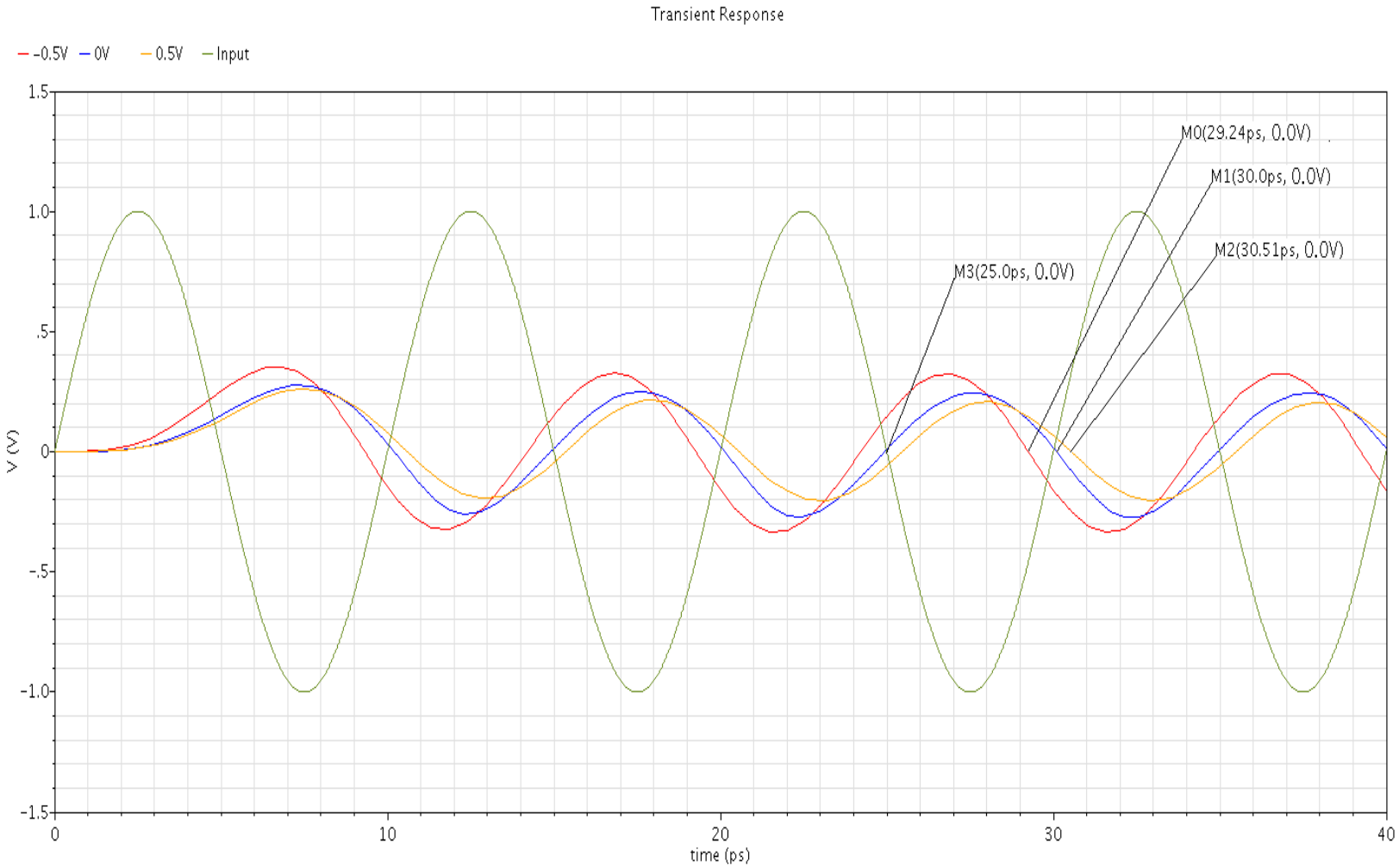


Figure 4.7 Transient response (W-band)

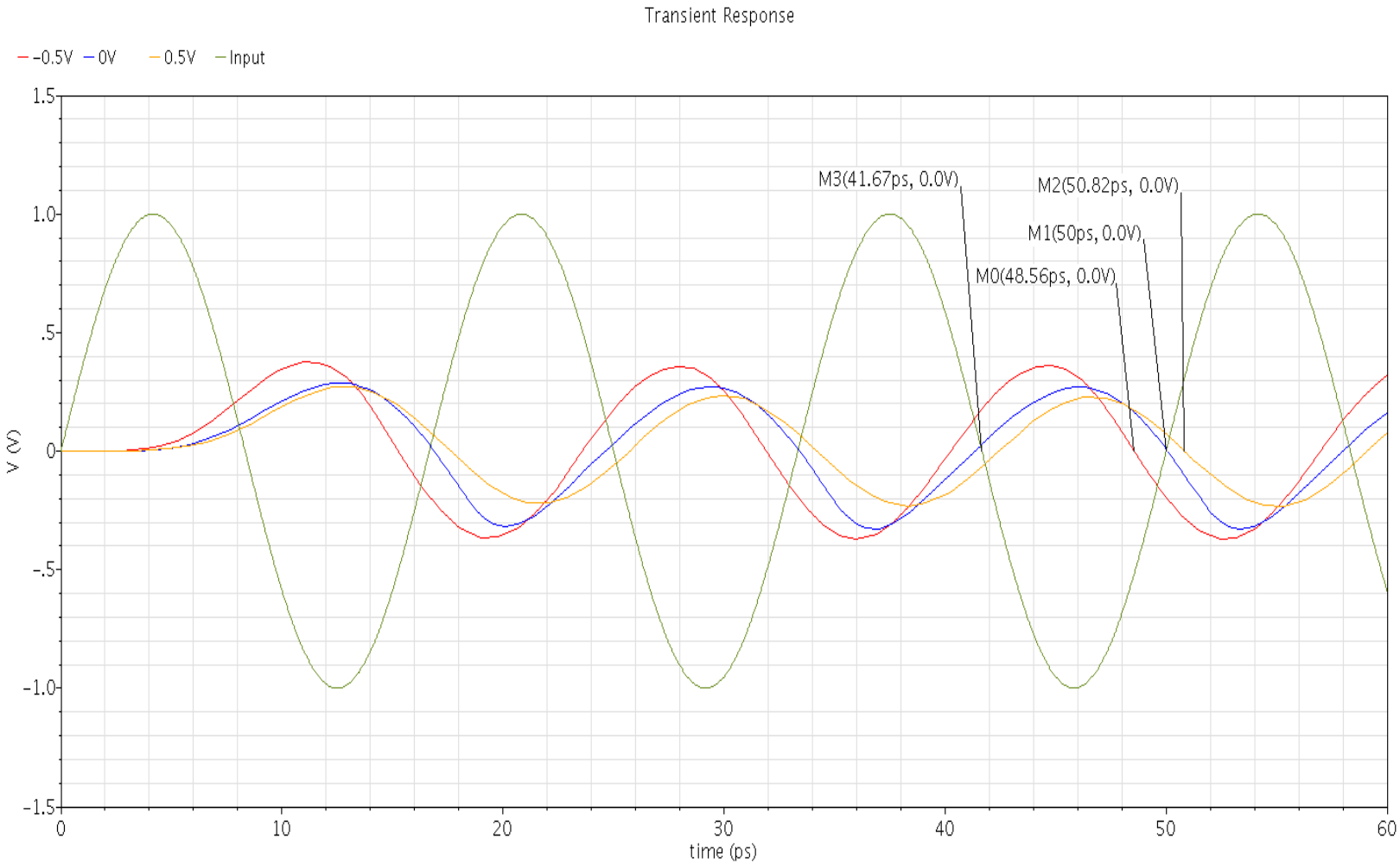


Figure 4.8 Transient response (V-band)

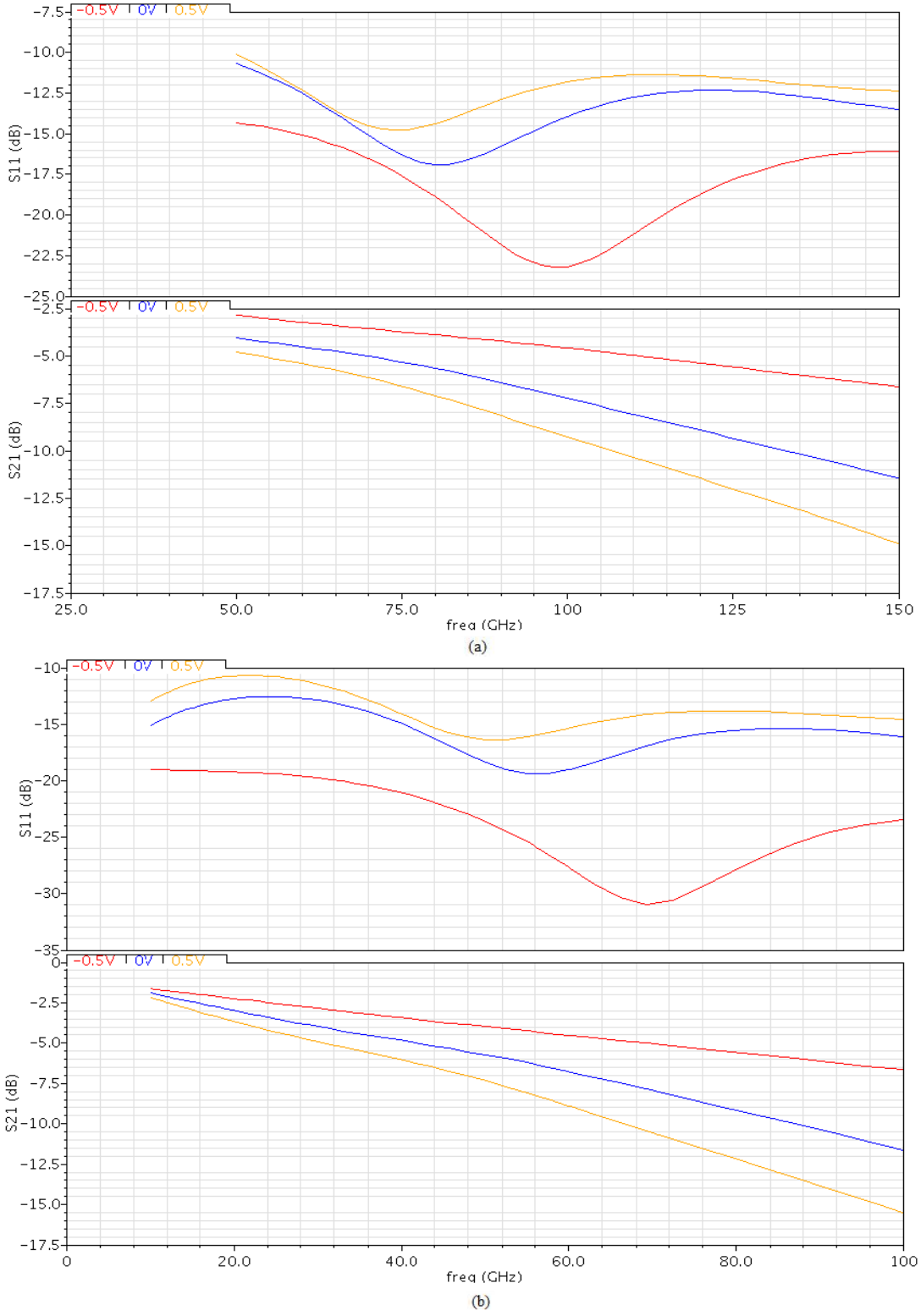


Figure 4.9 S-parameter simulation result (a) W-band (b) V-band

CHAPTER 5

CONCLUSION AND FUTURE WORK

This chapter summarizes the design and results of the distributed phase shifter for novel VCO implementation discussed. It then presents some future extensions using the ideas presented in this thesis.

5.1 Conclusion

The work of this thesis used IBM 90nm CMOS technology for all varactor and phase shifter simulations. This work presents the first attempt of CMOS distributed phase shifter design by periodically loading CPW line with varactors in W-band and V-band, taking advantages of well-established CMOS technology. The specifications were met and exceeded, evident by the simulation results.

5.2 Future Work

To fully implement the VCO architecture, an out-of-phase feedback amplifier is to be designed. The challenge lies in providing exact 180° out-of-phase at the amplifier output over a wide range of frequency of order of ten gigahertz. This might limit the bandwidth of the full VCO architecture. Also, the amplifier is needed to compensate for

the total loss the signal suffers going through the line so as to provide a unity gain loop for stable oscillations. The design of the amplifier is further complicated due to stability issues at these frequencies. Further challenge lies in design of appropriate matching networks while maintaining constant phase at the output.

The current design is based on an analog control voltage to vary the phase of the line. Hence, any electrical noise on the control line will transfer into the phase noise at the output oscillations. This can be addressed though digital control input.

Another interesting aspect not issued in this thesis is the modeling of the phase shifter with varactors. The model would accurately predict the insertion and return loss at certain operating frequency for given physical dimensions of the CPW line and varactors tuning range and series resistance.

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