III-V SEMICONDUCTORS ON SIGE SUBSTRATES FOR MULTI-JUNCTION PHOTOVOLTAICS

DISSERTATION

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by

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ABSTRACT

The epitaxial integration of high quality III-V semiconductors with Si is of fundamental interest for photovoltaic devices since Si substrates offer a lighter, stronger, and cost effective platform for device production. However, the lattice-mismatch between conventional III-V photovoltaic materials and Si generates threading dislocations in the epitaxial device layers, which can limit solar cell performance, depending of the density of such defects, the particular III-V material, and the device design. By using compositionally step-graded SiGe interlayers up to 100% Ge, which is lattice-matched to GaAs, the ~ 4% lattice-mismatch between Si and GaAs and $In_{0.49}Ga_{0.51}P$ is accommodated in the Group IV alloy system; this has produced defect densities less than $1x10^6$ cm^{-2} in fully relaxed the Ge/SiGe/Si (SiGe) virtual substrates. This unique approach to III-V/Si integration is employed in this dissertation for the development of GaAs and $In_{0.49}Ga_{0.51}P$ single junction (SJ) solar cells and ultimately $In_{0.49}Ga_{0.51}P$/GaAs dual junction (DJ) solar cells, integrated on a Si platform.

The residual threading dislocation density (TDD) present in the SiGe substrates transfers to the epitaxially grown III-V layers and thus can influence III-V solar cell performance. In this dissertation we report, for the first time, on the impact of TDD on the minority carrier electron lifetime in GaAs grown on SiGe. The electron lifetime in metamorphic p-type GaAs was found to be lower than that of holes in n-type GaAs at a

given TDD. This resulted from the higher mobility of electrons compared to holes and thus enhanced interactions with the TD array. Incorporating a TDD dependent lifetime into metamorphic GaAs solar cell device models, higher reverse saturation current densities and lower open-circuit voltages for n^+/p compared to p^+/n were predicted. This result was experimentally confirmed in this dissertation by diode and solar cell device measurements of both n^+/p and p^+/n GaAs cells grown on GaAs and SiGe substrates. The higher performance of the p^+/n GaAs-on-SiGe solar cell, by virtue of its higher open-circuit voltage, offers great potential for both space and terrestrial photovoltaic applications. The extension of this technology to space applications has lead to the development of large area GaAs-on-SiGe solar cells (up to 4 cm^2) with no degradation in cell performance. These large area cells will be flown on the International Space Station to test their actual space performance, which indicates their technological importance. Meanwhile, record terrestrial performance was measured and suggests efficiencies higher than 20% are realizable with current SiGe substrate technologies.

The production of $In_{0.49}Ga_{0.51}P$/GaAs DJ solar cells on Si, first required the investigation of homoepitaxial $In_{0.49}Ga_{0.51}P$ solar cell growth by solid source molecular beam epitaxy to determine the proper $In_{0.49}Ga_{0.51}P$ growth parameters and device designs. The significant performance improvements were obtained for p^+/n and n^+/p $In_{0.49}Ga_{0.51}P$ single junction solar cells through annealing; however, further optimization is still required to obtain performance comparable with commercial devices. Regardless, $In_{0.49}Ga_{0.51}P$ cell structures were integrated on SiGe substrates and the depletion region recombination component of the reverse saturation current density increased with increasing TDD, suggesting a decrease in minority carrier lifetime. However, the lower

mobility of carriers in $In_{0.49}Ga_{0.51}P$, compared to GaAs, predicts a greater TDD tolerance for $In_{0.49}Ga_{0.51}P$ solar cell open-circuit voltages when compared to GaAs solar cells. Like GaAs cells, $In_{0.49}Ga_{0.51}P$-on-SiGe cells also exhibit a polarity preference and thus only p^+/n DJ devices on SiGe were investigated.

The development of SJ GaAs and $In_{0.49}Ga_{0.51}P$ cells on SiGe has allowed the first realization of an $In_{0.49}Ga_{0.51}P$/GaAs DJ solar cell on Si with an output voltage of greater than 2 V. Although the DJ solar cell efficiency was limited by the quality of the $In_{0.49}Ga_{0.51}P$ top cell, comparison with an identical DJ cell grown on GaAs found that the DJ cell on Si retained 92% of open-circuit voltage and 99% of short-circuit current. Moreover, the p^+/n dual junction $In_{0.49}Ga_{0.51}P$/GaAs solar cell grown on SiGe demonstrated an open-circuit voltage that was consistent with the value predicted by the developed metamorphic dual junction device model. Therefore, this model can be used to guide the development of multi-junction cells on SiGe or other lattice-mismatched cell/ substrate combinations. Based on these results, p^+/n DJ efficiencies on SiGe in excess of 22% for space and 25% for terrestrial applications are expected with current SiGe substrate technologies.

Dedicated to my grandparents,

Olen and Ada Genter

and

Norris and Esther Andre

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FIELDS OF STUDY

Major Field: Electrical Engineering

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CHAPTER 1

INTRODUCTION AND MOTIVATION

1.1 Introduction

Semiconductor materials in the form of both homoepitaxial and heteroepitaxial layers offer a wide range of energy bandstructures that can be used in electronics (FETs, HBTs), optoelectronics (LEDs, lasers, solar cells, detectors), sensors, as well as many other applications. In general, material defects should be minimized in order to produce the highest quality semiconductor layers and thus the highest performance devices. To achieve this, epitaxial device layers should be grown on substrates with the same lattice constant. However, it is neither economical nor physically possible to create high quality crystalline substrates for every semiconductor alloy of interest; the four most readily available are Si, Ge, GaAs, and InP. (These lattice constants are denoted in Figure 1.1.) The constraint placed on bandstructure engineering and device design by these conventional substrate choices is evidenced by the fact that very few semiconductor heterostructures are integrated into technology. Of the heterostructures in commercial use, virtually all consist of lattice-matched material systems such as $In_{0.53}Ga_{0.47}As/InP$, $In_{0.49}Ga_{0.51}P/GaAs$, and $In_{0.47}Al_{0.53}P/GaAs$, with $Al_xGa_{1-x}As/GaAs$ as the overwhelmingly

dominant system. The implementation of lattice-mismatched systems offers a fuller utilization of the available semiconductor properties by expanding the vertical lines in Figure 1.1 in the horizontal direction by working at lattice constants other than those of Si, GaAs, Ge, and InP, but still utilizing these substrates as platforms for epitaxial growth.

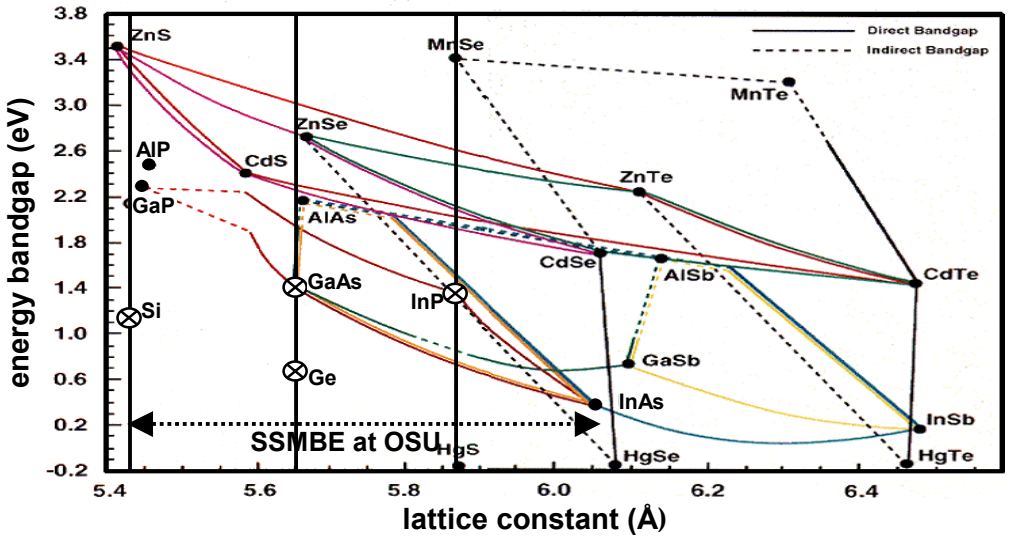

Figure 1.1 Semiconductor energy bandgap versus crystalline lattice constant. Vertical solid lines denote conventional crystalline semiconductor substrate lattice constants. The arrow indicates the lattice constant range that can be obtained at OSU using SSMBE.

The problems with lattice-mismatched epitaxy are the defects induced by the integration of structurally dissimilar crystalline materials such as misfit and threading dislocations as well as anti-phase domains and boundaries. Even low concentrations of these mismatched induced defects can wreak havoc on electronic and optoelectronic

device performance due to their great sensitivity to crystalline disorder. Threading dislocations (TDs) and anti-phase domains (APDs) in particular can "kill" device performance by introducing conductive shunt paths, increasing carrier recombination rates, introducing traps within the bandgap, and even by complicating device processing techniques. An excellent example of the issues generated by lattice-mismatched integration is the nascent field of GaN electronics. Here, GaN device layers are typically grown on sapphire substrates due to the lack of a compatible lattice-matched substrate. The resulting mismatch in lattice constant, crystalline structure, interface valency, and thermal expansion coefficient, leads to high leakage currents, low frequency noise, carrier compensation, and layer cracking. Fortunately for the GaN research community, the unique properties on GaN make GaN devices less sensitive to electrically active defects than their III-As and III-P counterparts. Even so, GaN devices are now close to or at the point of development where lattice-mismatched defects now play dominant roles; a worldwide search for solutions that minimize the impact of lattice-mismatched defects is ongoing.

The epitaxial integration of device-quality III-V materials on Si substrates has been considered the "holy grail" of the electronics industry for several decades. Monolithically integrating III-V compounds onto Si substrates provides a large area and low cost substrate for III-V epitaxy, while providing Si VLSI circuitry access to the excellent optical properties and ultra-fast switching speeds provided by III-V compound semiconductor materials. To date, of the many approaches used in III-V/Si integration, only the implementation of Ge/SiGe/Si (SiGe) substrates has demonstrated material quality suitable for minority carrier devices over large areas. In the proposed work, III-V

epitaxy on SiGe substrates will be performed. Various experimental techniques will be used to identify electrically active defects, their sources, and their relation to material properties. Several variations of solar cell designs consisting of single junction GaAs and $In_{0.49}Ga_{0.51}P$ cells and dual junction $In_{0.49}Ga_{0.51}P$/GaAs cells will be grown, tested, and analyzed in order to provide a sensitive vehicle by which the direct impact of specific lattice-mismatched defects on devices can be gauged. The goal is to achieve a vertically integrated picture, starting from growth, interface properties, bulk structural and electronics properties, and leading to device performance characteristics for an extremely promising solution to the III-V/Si integration question.

1.2 III-V Si integration

The integration of III-V semiconductor compounds onto Si substrates has been of great interest for a variety of applications. These include optical interconnects for chip-to-chip and board-to-board communications; ultra-high bandwidth VLSI systems which utilize III-V compounds for high-frequency subsystems without sacrificing established cost-effective Si VLSI for basic circuitry; optoelectronic integrated circuits (OEICs) which combine the optimum optical properties of III-V materials for photonic devices (e.g. lasers, optical modulators, LED's) with conventional Si driving circuitry and signal processing, and high efficiency III-V solar cells on lightweight Si substrates. Since significant material incompatibilities exist between III-V materials and Si, namely polar on non-polar epitaxy, a 4% lattice-mismatch (GaAs:Si), and a thermal expansion coefficient mismatch, methods to mitigate resulting defects and models to assess the tolerance of each application to such defects are necessary before such applications become part of main stream technology.

Various methods have been used in order to achieve III-V/Si integration; these methods are summarized in Table 1.1.[1] Although most methods avoid III-V/Si heteroepitaxy entirely, there are other fundamental issues to overcome. For example, flip-chip and fluidic assembly requires full production lines for Si and III-V technologies as well as a special assembly line to integrate devices. In these procedures, III-V devices are vulnerable since they exist as freestanding layers prior to placement. Epitaxial lateral overgrowth (ELO) can reduce lattice-mismatch defects, but has to remedy the presence of growth front coalescence defects as well as area limitations. Wafer bonding requires extremely (almost atomically) flat surfaces as well as precise placement with respect to position and orientation, which is in reality extremely difficult to achieve. Moreover, it does not escape the effect of thermal expansion coefficient mismatch, which can lead to fracturing of the bonded layers. From Table 1.1 it is clear that the direct epitaxial integration method has the fewest handling steps since it does not require substrate removal or the bonding of surfaces. Another feature of epitaxial integration is that III-V material can be selectively deposited after Si fabrication, but prior to metal deposition, and thus high temperature Si processing steps will not degrade III-V material layers. Furthermore, with the exception of successful wafer bonding, direct epitaxy is the only methods applicable to large area devices such as solar cells.

Comparison of Integration Methods

Integration Method	III-V Fabrication	Substrate Removal	Epilayer Transfer	Bonding to Si
Flip-Chip	Before Transfer	After Transfer	GaAs substrate	Bump Bonding
ELO	Before & After Transfer	Before Transfer	Free Standing	Van der Waal's
Applique	Before Transfer	Before Transfer	Free Standing	Metallic Bonding
Fluidic Assembly	Before Transfer	Before Transfer	Fluidic Suspended	Van der Waal's
Wafer Bonding	After Transfer	After Transfer	N/A	various methods
Epitaxial	After Integration	N/A	N/A	N/A

Table 1.1 Comparison of various III-V/Si integration methods.[after Ref. 1]

1.3 Epitaxial III-V Si integration and photovoltaics

The ability to achieve device-quality III-V heterostructures epitaxially integrated onto Group IV substrates is a vital goal for communication satellites, which need light-weight high-efficiency radiation-hard space solar cells in order to increase the specific power (watts/kg) of solar array power supplies. Currently, commercial III-V solar cells for space applications are grown on Ge substrates since the enhanced mechanical strength compared to GaAs allows the use of substrates that are thinner and thus lighter. Moreover, since Ge represents only a 0.07 % lattice-mismatch with respect to GaAs, device performance is not significantly affected. The replacement of Ge substrates with Si substrates for photovoltaics, is advantageous not only because it is stronger and lighter but also more thermally conductive, cheaper, and available in larger areas.

Unfortunately, III-V epitaxial layers grown on Si often exhibit lattice-mismatched induced defect densities that limit solar cell performance.

In view of the enormous technological value of integrating GaAs with Si epitaxially for photovoltaics applications, it is not surprising that GaAs growth on Si has been the subject of extensive research efforts. A number of epitaxial techniques have been employed to reduce the threading dislocation density (TDD) in GaAs epitaxial layers, including use of mis-oriented substrates, strained layer superlattice (SLS) buffers, and thermal cycle annealing (TCA).[2,3,4,5,6,7] However, in spite of these approaches the TDDs have not been reduced below the mid-10^6 cm^{-2} level. It is believed that dislocation tangling blocks dislocation glide and prevents efficient removal of dislocations by SLS buffers and other strain-induced dislocation glide-based suppression mechanisms.[8] Based on these efforts, p+/n GaAs solar cells with efficiencies of 15.2% for AM0 and 16.5% for AM1.5 have been achieved.[9] The low open-circuit voltage values were identified as the major impediment to high performance devices and require lower TDDs for further improvement.

These results have motivated an alternative approach to monolithic integration in which the surface lattice constant of the Si substrate is engineered prior to III-V epitaxy by growing compositionally step-graded $Si_{1-x}Ge_x$ layers up to 100% Ge. Thus, the reduction of lattice-mismatch induced defects is addressed in a material system and under growth conditions that are independent from the III-V epitaxial device layers. Hence, a wider range of growth conditions (temperature, growth rate, etc.) may be accessible to achieve more optimal lattice relaxation than is possible with III-V growth parameters. Using this technology, in a joint research effort between The Ohio State University and

the Massachusetts Institute of Technology, a TDD of ~$1x10^6$ cm^{-2} for GaAs on Si has been reported.[10,11] Compositionally step-graded $Si_{1-x}Ge_x$ layers up to 100% Ge have achieved low TDDs by the gradual introduction of strain (lattice-mismatch). This eliminates the need for the entire system mismatch to be accommodated at a single heterointerface, thus resulting in films with fewer threading dislocations.[8] A representative TEM image for an epitaxial GaAs layer on a SiGe substrate is shown in Figure 1.2b; an example of direct epitaxy of GaAs on Si is shown in Figure 1.2a. By preparing a "virtual Ge substrate" for III-V epitaxy, similar techniques used in III-V growth on a true Ge substrate can be employed to mitigate effects of polar on non-polar growth, leaving the mismatch in thermal expansion a remaining issue.

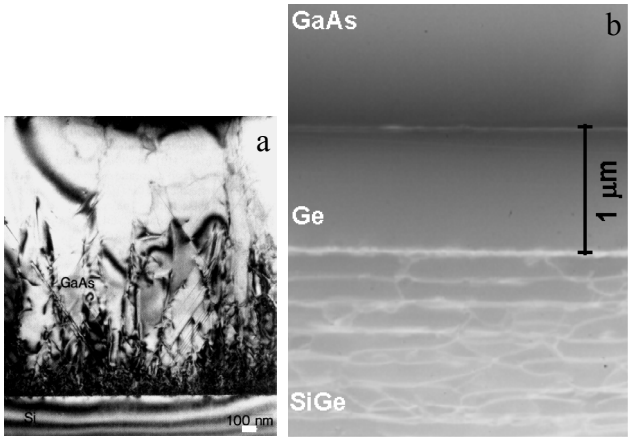

Figure 1.2 a) TEM micrograph of direct epitaxy of GaAs on Si.[after Ref. 12] b) TEM micrograph of GaAs on Si using SiGe graded buffer layers.[after Ref. 13]

1.4 Research objective

The objective for the proposed research is motivated by the fundamental issues related to the control of a wide range of defects in lattice-mismatched, heterovalent III-V/Si heterostructures and the enormous technological interest in achieving viable epitaxial integration of III-V devices on Si. It is clear from the previous sections and prior work in the field that to achieve the latter requires mastering of the former. Hence, the objective consists of two main thrusts. The first is to develop a fundamental framework to achieve device-quality III-V (GaAs and $In_{0.49}Ga_{0.51}P$) epitaxy on a Si platform using Ge/SiGe/Si (SiGe) substrates, exploiting growth techniques that produce controlled GaAs/Ge interfaces [14] and extending beyond the growth and measurement of record-quality n-type GaAs/SiGe [10], which have been demonstrated in previous research at The Ohio State University. The second is to apply the knowledge obtained from the first thrust toward achieving optimum single junction (SJ) GaAs and $In_{0.49}Ga_{0.51}P$ and dual junction (DJ) $In_{0.49}Ga_{0.51}P$/GaAs solar cells grown on SiGe. Previous work at The Ohio State University has demonstrated high performance p+/n GaAs-on-SiGe solar cells, 15.5% for AM0 [13], but n+/p GaAs and n+/p and p+/n In0.49Ga0.51P cells on GaAs and on SiGe had not been investigated. This effort will require a wide array of basic materials and device studies that will lead to correlations between growth conditions, structural properties, electronic properties, and device optimization. By focusing on III-V heterostructures that are lattice-matched to Ge, this work will provide guidelines for transitioning a wide range of conventional III-V heterostructure devices, including solar cells, LEDs, and transistors that are currently grown on GaAs or Ge substrates, to Si-based substrates. It is worth noting that from the

viewpoint of basic materials research, developing III-V solar cells on SiGe enables the evaluation the III-V/SiGe integration method since they cannot be connected to external power sources that can aid in carrier collection and their large device areas provide a good vehicle to test lateral uniformity of material quality.

1.5 Organization of this thesis

The remainder of this dissertation is organized as follows. Chapter 2 will review the hurdles to the epitaxial integration presented by the GaAs/Si material system. Since photovoltaics cells are the main test device used in this research, Chapter 3 describes the performance characteristics and device design of solar cells for space and terrestrial applications as well as design consideration for high efficiency III-V solar cells and the use of alternative substrate for photovoltaics, while, Chapter 4 describes the solar cell device models used to correlate device performance and material properties. Chapter 5 briefly describes the experimental tools used in this research along with their application in this research. In Chapter 6 the minority carrier lifetime of GaAs is discussed along with experimental evidence showing impact of TDD on the lifetime of holes and electrons in GaAs. These materials parameters are then employed in device models in Chapter 7 to describe expected diode performance as a function of TDD, followed by n+/p and p+/n GaAs solar cell data that supports such models.

In Chapter 8, the growth methods developed for $In_{0.49}Ga_{0.51}P$ by solid source molecular beam epitaxy are discussed along the device performance characteristics for $In_{0.49}Ga_{0.51}P$ solar cells grown on GaAs substrates. Although improvement in $In_{0.49}Ga_{0.51}P$ growth are still needed, Chapter 9 presents $In_{0.49}Ga_{0.51}P$ device models as a

function of TDD as well as metamorphic n+/p and p+/n device performance for $In_{0.49}Ga_{0.51}P$-on-SiGe solar cells. The culmination of the GaAs and $In_{0.49}Ga_{0.51}P$ cell development resulted in the development of a p+/n DJ $In_{0.49}Ga_{0.51}P$ /GaAs solar cell grown on SiGe, which are described in Chapter 10 along with DJ device models for n+/p and p+/n cells as a function of TDD. Finally, the PV application of GaAs/SiGe solar cells are presented in Chapter 11, including reports of the highest independently confirmed efficiencies and the first reports of thermal testing and testing under high concentration for GaAs-on-SiGe solar cells. Chapter 12 concludes this thesis by summarizing the results and indicating areas of on going and future work.

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CHAPTER 2

EPITAXIAL HURDLES: III-V / SI INTEGRATION

In the previous chapter the technological benefits of III-V/Si integration were summarized; however, the technological hurdles to such integration were not fully addressed. The challenges to III-V/Si epitaxial integration, including inter-diffusion, polar/non-polar interfaces, lattice mismatch, and thermal expansion mismatch, will be discussed in this chapter along with methods to overcome some of these challenges. Previous research at The Ohio State University has determined methods for controlling the formation of anti-phase domains and inter-diffusion which can lead to undesirable active junctions at the GaAs/Group IV interface. Then, by using Ge/$Si_{1-x}Ge_x$/Si (SiGe) substrates, researchers at The Ohio State University have achieved low threading dislocation densities in relaxed GaAs on a Si; however, the control of thermal expansion generated microcracks are still under investigation.

2.1 Anti-phase domain nucleation at III-V/Group IV interface

The formation anti-phase domains (APDs) in the zinc-blende crystal structure of III-V materials deposited on the diamond crystal structure of Group IV substrates results from the polar-nonpolar nature of this heteroepitaxial interface and the atomically

stepped nature of crystal surfaces. Figure 2.1a shows a pictorial representation of an APD resulting from uniform As growth initiation on a single stepped Ge surface. The APD is bound by anti-phase boundaries (APBs) that consist of metallic As-As or Ga-Ga bonds. These bonds are expected to be electronically charged, introducing recombination centers in the bandgap and therefore degrading the GaAs electrical quality and p-n junction performance.[1,2] Therefore, the elimination of extended APD formation was a critical step in attaining high quality III-V material on Ge, Si, and SiGe substrates and has been studied extensively by research groups using solid source molecular beam epitaxy (SSMBE) and metal-organic vapor deposition (MOCVD) over the last 30 years.

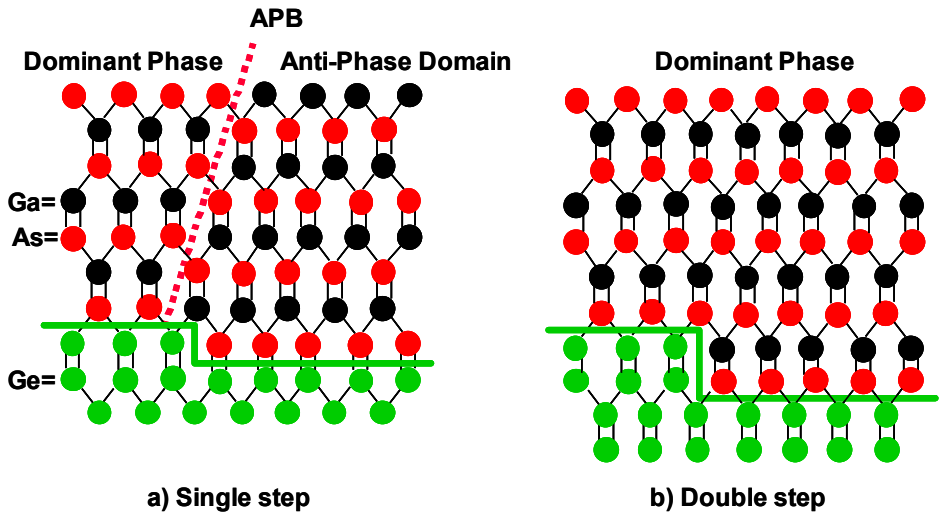

Figure 2.1 Schematic of a) a single-stepped Ge surface demonstrating the formation of APB's during GaAs growth and b) a double-stepped Ge surface demonstrating growth of a single domain of GaAs.

As shown pictorially in Figure 2.1b, "APD-free" GaAs can be obtained on a double stepped Ge surface with a uniform As initiation layer.[1] Other research has shown that GaAs layers that exhibit a single domain at the termination of GaAs growth can also be obtained by the annihilation of APBs as the layer is grown.[3, 4] This phenomena is described in Figure 2.2 and is enhanced by the use of (100) Ge or Si substrates with an off-cut in the <110> direction. It should be noted that APD suppression has been studied for both the GaAs/Si and GaAs/Ge material systems; however, the GaAs/Si material system has added complications such high lattice mismatch and a higher oxide desorption temperature.[3] Regardless of the means used to achieve "APD-free" GaAs, whether complete suppression APD formation or the elimination of extended APDs by APB annihilation, this material incompatibility has not limited the realization of high quality GaAs/Ge integration, as is evident by the commercial production of high efficiency GaAs/Ge solar cells as well as high minority carrier lifetimes for GaAs layers grown on Ge.[5, 6, 7]

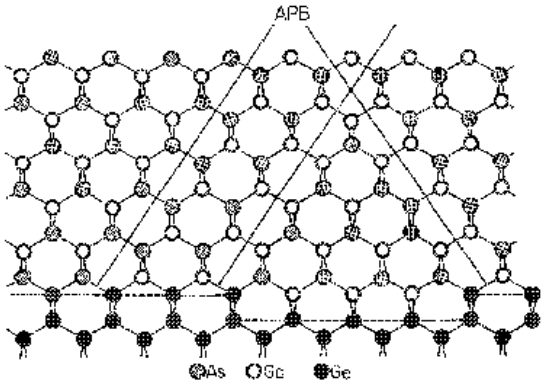

Figure 2.2 A schematic showing the annihilation of APBs and the coalescence of two GaAs domains. [after Ref. 3]

2.2 Atomic inter-diffusion at III-V/Group IV interface

The growth of III-V compounds on Group IV substrates such as Si and Ge can result in significant atomic inter-diffusion. Group III and Group V atoms that diffuse into the Group IV substrate can act as substitutional p-type and n-type dopants, respectively. Where as, the Group IV atoms which out-diffuse into the III-V epitaxial layers are amphoteric substitutional dopants in the III-V lattice, but are most commonly n-type in nature, indicating placement on a Group III lattice site. This intermixing at the III-V/Group IV heterointerface can type convert doped layers and therefore reduce material quality of the epitaxial film as well as significantly alter device performance.

This problem is significant for III-V photovoltaic applications where Ge substrates have become the substrate of choice. In solar cell growth, a n+/p GaAs solar cells grown on a p-type Ge substrate will typically show higher open-circuit voltages than the same n+/p GaAs cell grown on a p-type GaAs substrate.[8] In this case, the As diffusion into the p-type Ge substrate type converts the p-type Ge substrate and forms a n/p Ge junction in series with the n+/p GaAs junction. This series connection produces a GaAs/Ge dual junction solar cell, as shown in Figure 2.3a. By "controlling" the As diffusion into the substrate and growing an intentional GaAs tunnel junction to connect the two cells, the efficiency and stability of the "inadvertent Ge junction" has been improved over the last 10 year such that it is commonly used in commercial devices. In order to obtain a n+/p GaAs solar cell on Ge without an "active Ge junction" manufacturers have resorted to growth on an n-type Ge substrate with a GaAs tunnel junction to ohmically connect the p-GaAs base and the n-type Ge substrate.[8]

For a p+/n GaAs solar cell on an n-type Ge substrate, the Ge out-diffusion into the GaAs layer will further dope the layer n-type, while the As diffusion in the Ge substrate will further dope the substrate n-type. However, Ga diffusion into the substrate will act as a p-type dopant and can type-convert the Ge substrate if the concentration of Ga diffused is greater than the n-type Ge doping, as described in Figure 2.3b. This can result in a GaAs/Ge dual junction cell with a p+/n polarity which are also capable of high open-circuit voltages.[9, 10]

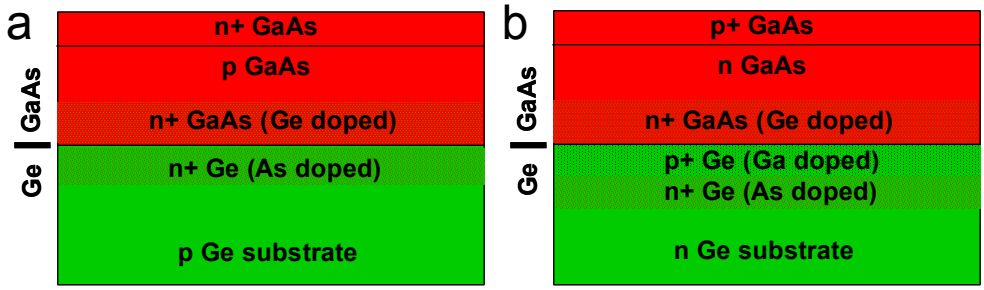

Figure 2.3 This figure describes inter-diffusion for GaAs solar cells grown on a) a p-type Ge substrate and b) an n-type Ge substrate.

2.3 GaAs/Ge interface nucleation via SSMBE

Previous work at The Ohio State University developed solid source molecular beam epitaxy (SSMBE) GaAs initiation conditions that produced "APD-free" GaAs films, with low inter-diffusion and high minority carrier lifetimes.[11, 12, 6, 7] Figure 2.4 shows cross-sectional (X) and plan-view (PV) TEM images of a GaAs layers grown on Ge with non-optimum and optimum growth conditions; non-optimum conditions

produced GaAs films with APB's nucleated at a GaAs/Ge interface and extended through the GaAs layers. The APB's are generated due to a stacking mismatch created by the single stepped Group IV surface. Using a double-stepped surface and optimum initiation conditions eliminates the GaAs-Group IV stacking mismatch and eliminates the nucleation of APB's.

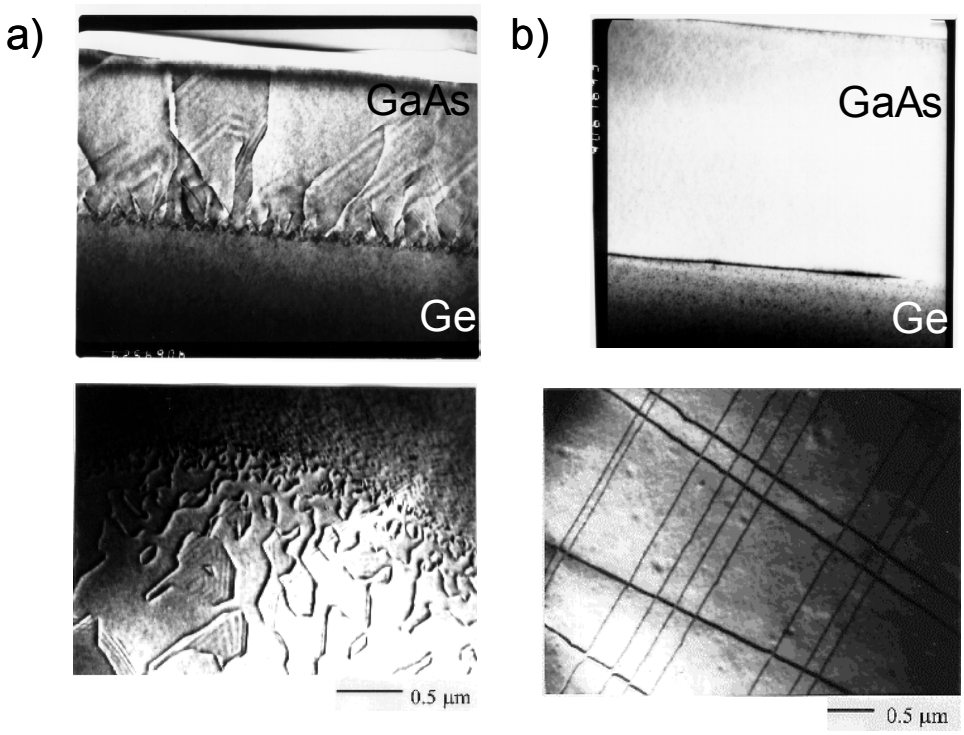

Figure 2.4 Cross-sectional TEM and plan-view TEM images of GaAs growth on Ge where a) a non-optimal interface nucleation procedure resulted in the incorporation of large APBs and b) an optimal nucleation procedure resulted in suppression of APB formation. [after Ref. 11]

An investigation of the GaAs/Ge nucleation process via SSMBE was performed to determine the optimum nucleation procedures.[13] The key growth processes for "APD-free" GaAs/Ge with effective blocking of inter-diffusion are included below.

1) Use of (001) Ge wafers offcut 6^{o} toward the [110] to promote the formation of a "double-stepped" Ge surface and encourage the annihilation of APDs, if any form.
2) Deposition of epitaxial Ge at ~350^{o}C (300-1000Å) to reduce carbon contamination.
3) A 20 minute anneal of the Ge susbtrate at 640^{o}C to achieve a double-stepped Ge surface.
4) Deposition of ~30 Å GaAs growth via migration enhanced epitaxy (MEE) at 350^{o}C starting with an As pre-layer to ensure uniform nucleation.
5) Deposition of ~1000 Å GaAs growth at 500^{o}C at a growth rate of ~0.1μm/hr to act as a diffusion barrier.

Although the culmination of all of these steps form the robust recipe for GaAs/Ge growth by SSMBE, it was found that GaAs initiation at 350^{o}C via migration enhanced epitaxy (MEE) was critical to obtaining complete APD suppression as shown in Figure 2.5. The MEE process involves the deposition of a single atomic layer of either the Ga or As, and allows full coverage of the Ge surface with a single, complete layer of either Ga or As instead of a "mixed" interface nucleation layer. If MEE is not employed and after an initial As pre-layer both Ga and As are co-evaporated at 500°C, a high density of APD are formed at the interface which annihilate within ~50 nm of the GaAs/Ge interface, as shown in Figure 2.6. This procedure (no MEE) also results in "APD-free" GaAs epilayers; however, the presence of small short-range APD disorder at the interface can influence inter-diffusion or conduction at the GaAs/Ge interface.

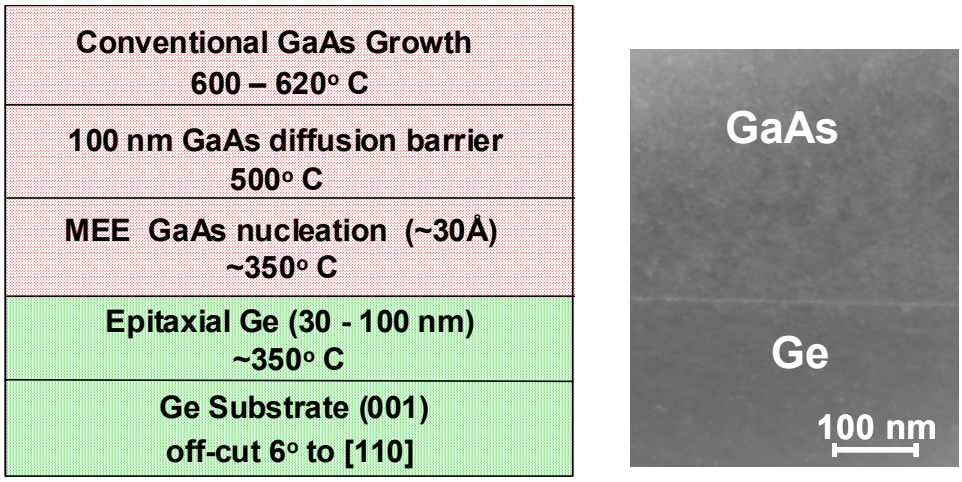

Figure 2.5 Schematic of the "optimum" SSMBE growth conditions for complete suppression of APD disorder at the GaAs/Ge interface.

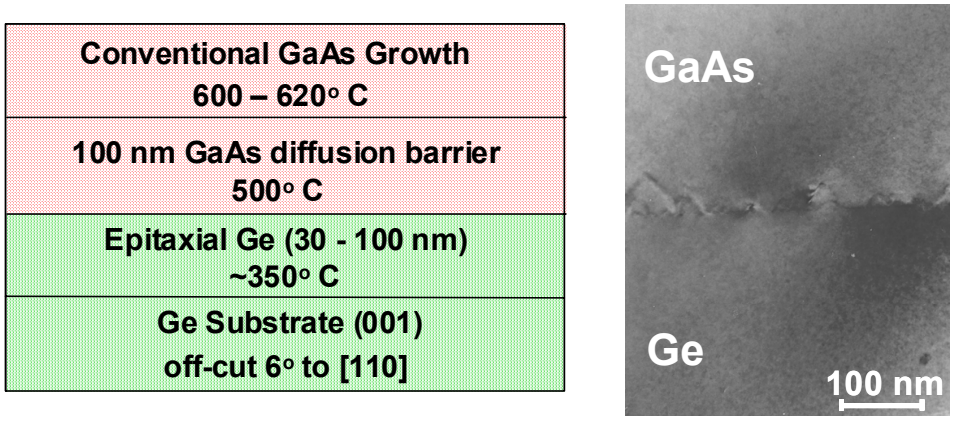

Figure 2.6 Schematic of the "no MEE" SSMBE growth conditions eliminate extended APDs in GaAs by the annihilation of short range APD disorder at the GaAs/Ge interface.

A unique feature of this growth process was the inclusion of the epitaxial Ge layer which produced GaAs/Ge films which were free of stacking faults, APD, and TDs. The presence of these defects in GaAs/Ge without epitaxial Ge was attributed to carbon contamination of the Ge surface and thus an epitaxial Ge layer was implemented in order to bury the carbon contamination and prevent defect nucleation at the GaAs/Ge interface.[13] The amount of carbon contamination was also reduced using a UV-ozone treatment, which grows an oxide on the Ge substrate prior to growth. This allowed high quality GaAs layers to be grown on Ge without an epitaxial Ge layer, since it was not necessary for APD suppression in the absence of carbon contamination.[13] Another important parameter in this growth process were the growth temperatures selected. The low temperature, 350^{o}C, "freezes-in" the double-stepped Ge surface obtained during the Ge substrate anneal at 640°C. While the complete mono-layer coverage obtained using MEE combined with the low thermal energy due to the low growth temperature, suppresses diffusion of atoms across the interface. The final initiation step, the co-evaporation of GaAs at 500^{o}C at a low growth rate (0.1μm/hr), further suppresses diffusion by lowering the thermal energy during the initial 1000Å of growth. After completion of this nucleation procedure the GaAs coated Ge wafer can be treated as an epitaxially-ready GaAs wafer for additional III-V epitaxy by SSMBE or MOCVD. While this procedure is not necessarily a unique solution to APB-free GaAs/Ge interfaces and APB free GaAs/Ge films, Li et al, also using SSMBE, have confirmed the reproducibility of this method.[14] This is significant since it demonstrates that the methods developed are transportable to other MBE systems.

A comparison of the inter-diffusion for both growth procedures (MEE and no MEE) are shown in Figure 2.7. Note that the secondary ion mass spectroscopy (SIMS) data indicates that the elimination of the MEE nucleation step increases the diffusion of As while still resulting in Ge out-diffusion below the SIMS detection limit. Using capacitance-voltage (C-V) measurements, which measure the conductivity of the GaAs layers, we found that the GaAs doping profiles were modified by Ge out-diffusion more than 2μm from the GaAs/Ge interface as shown Figure 2.8. These results conclude that the MEE nucleation step is vital in controlling interface diffusion in addition to promoting an APB-free interface.

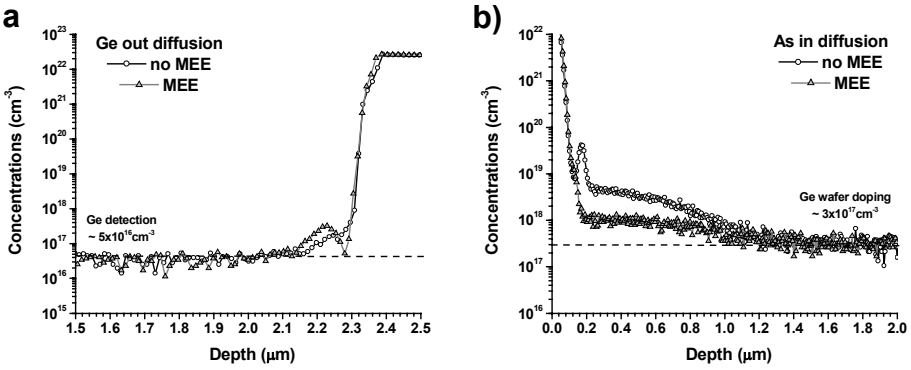

Figure 2.7 SIMS data showing the minimization of atomic inter-diffusion at the GaAs/Ge interface for a) Ge and b) As. Note the increased As diffusion when eliminating the MEE nucleation step.[after Ref. 11]

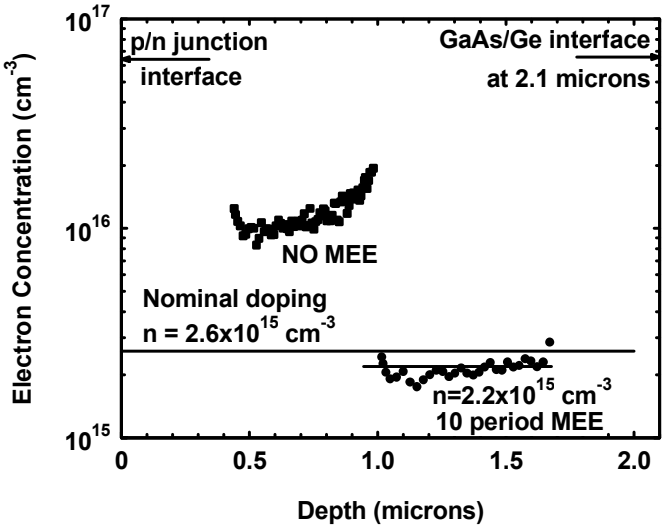

Figure 2.8 Capacitance-voltage dopant profiles for GaAs grown on a Ge substrate. The GaAs growth nucleated using MEE at 350°C showed lower n-type conductivity than the GaAs growth nucleated at 500°C without MEE. [after Ref. 11]

2.4 Lattice mismatch

The lattice mismatch between GaAs and Si (~ 4%) is largely responsible for the inability to achieve high performance devices and high material quality through epitaxial integration. Lattice mismatched heteroepitaxy involves the epitaxial growth of a layer with a lattice constant different than that of the underlying substrate. The amount of lattice mismatch, or misfit (*f*), is defined in Equation 2.1,

$$f = \frac{a_f - a_s}{a_s} \qquad \text{Equation 2.1}$$

where a_f and a_s are the lattice constant of the epitaxial layer and the substrate, respectively.[15] Figure 2.9 shows a schematic representation of epitaxial growth of an epitaxial layer material with both a larger and a smaller relaxed lattice parameter when compared to the substrate material. This results in a tetragonally distorted lattice in which the in-plane lattice constant of the layer material conforms to the atomic spacing of the substrate material.

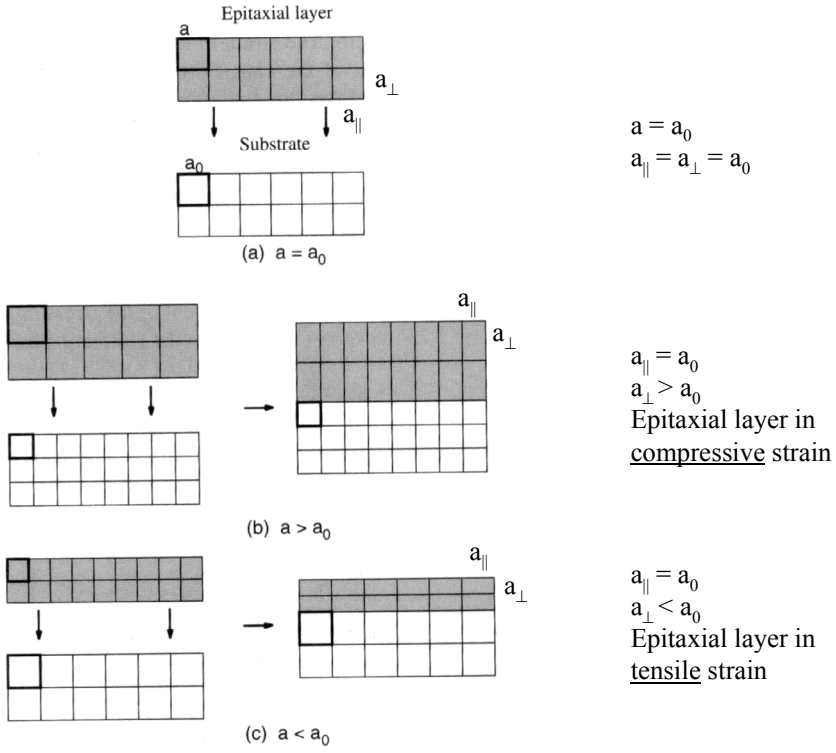

Figure 2.9 This figure demonstrates the growth of an epitaxial layer of lattice constant, a, on a substrate of lattice constant, a_0 where a) $a = a_0$, b) $a > a_0$ and c)$a < a_0$. If a lattice mismatch exists, either tensile or compressive strain can be incorporated into the epitaxial layer.[after Ref. 16]

The epitaxial layers will continue to grow in this "tetragonally distorted" or pseudomorphic form until the layer thickness reaches the critical thickness, h_c. Beyond the critical thickness, it becomes energetically favorable to relieve the strain by other methods, such as the generation of a dislocation. The critical thickness is typically described by the Mathews Blakeslee criteria [15], shown in Figure 2.10, and depends on the amount of mismatch, the lattice constant, and the Poisson ratio of the layer material. As indicated in this figure, the GaAs/Si material system has a critical thickness of ~1 nm while the GaAs/Ge material system has a critical thickness of ~220 nm.

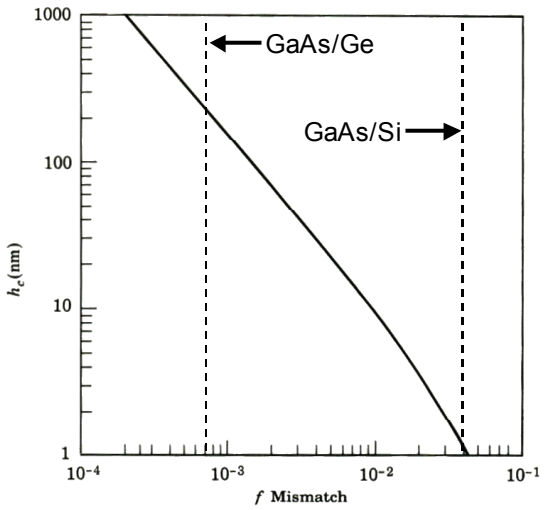

Figure 2.10 Matthews-Blakeslee criteria for critical thickness, h_c, versus misfit, f. [after Ref. 15].

Direct epitaxy of large mismatched systems, such as GaAs/Si in which the critical thickness is less than 4 mono-layers of GaAs, results in uncontrolled lattice relaxation, such as three-dimensional growth and the introduction of a large number of immobile edge and threading dislocations. The result is a near completely relaxed film containing threading dislocation densities, TDDs, of greater than 10^9 cm^{-2}.[17] However, for lower mismatch systems (< 1-1.5%), the incorporation of strain is more controlled and predominately results in the formation of 60^o misfit dislocations at the herterointerface and the associated threading dislocations.[18, 19] Figure 2.11 shows a schematic of the misfit dislocation (MD) segment and the corresponding threading dislocations (TDs) terminating at a free surface. The orientation of the burgers vector for TDs indicate that while the TD itself does not relieve strain, TD glide and the lengthening of the MD segment at the interface does provide strain relaxation. Unfortunately, for the highly mismatched GaAs/Si material system the uncontrolled nucleation of dislocations results in small, sessile misfit segments that require a high density of TDs and MD segments for adequate strain relief. The more controlled nucleation of glissile 60^o misfits for lower mismatch systems can produce long misfit segments that relieve strain and thus require fewer TDs. Moreover, since it is the TDs that penetrate the epitaxially grown device layers, the TDs can act as a site of localized recombination, which can decrease minority carrier diffusion lengths and increase depletion region recombination in junctions. In this manner the TDD plays a large role on photovoltaic solar cell performance by influencing carrier collection and the open-circuit voltage.

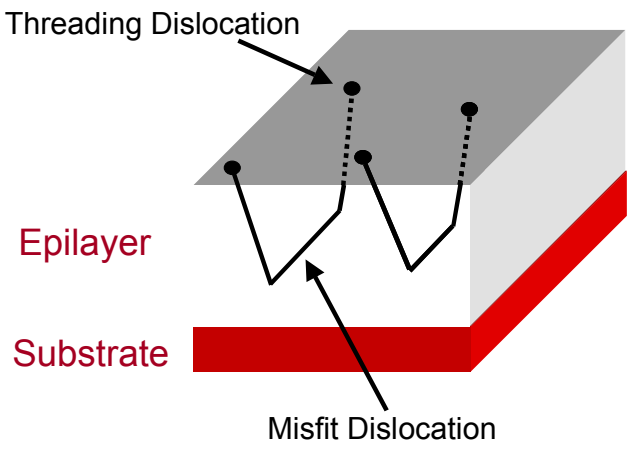

Figure 2.11 Schematic representation of misfit and threading dislocation segments typical for growth of lattice mismatched systems. The misfit segment is contained at the interface and the thread segment propagates through the epilayer and terminates at the growth surface.

2.5 Thermal expansion mismatch

Unlike the GaAs/Ge material system which have a thermal expansion coefficient mismatch of ~ 0% at 300 K, the GaAs/Si material system has a mismatch of ~125% at 300 K. The thermal expansion coefficient (α) of a semiconductor represents the change in lattice constant for a change in temperature. For heteroepitaxy, a thermal expansion coefficient mismatch indicates that the lattice constant of the epilayer (i.e. GaAs) changes at a different rate than that of the substrate (i.e. Si) as the temperature of the integrated material system is changed. For example, $\alpha(Si) = 2.6 \times 10^{-6}\ K^{-1}$ and $\alpha(GaAs) = 5.8 \times 10^{-6}\ K^{-1}$ at 300 K [20], this suggests that the Si lattice will expand less when heated and

contract less when cooled when compared to the GaAs lattice. Assuming GaAs grown on Si is fully relaxed at growth temperature, the GaAs film will be in tension as the system is cooled to room temperature, which is opposite of the compressive strain induced by the lattice mismatch. For the GaAs/Si system the thermal strain was estimated to be ~$2x10^{-3}$, less than 10 percent of the lattice mismatch strain for the GaAs/Si system, ~$3.9x10^{-2}$.[21]

While the thermal mismatch strain is significantly smaller than the lattice mismatch strain incorporated for the GaAs/Si material system, the thermal strain can become significant at large epitaxial layer thicknesses. Although some of the thermal strain may be relaxed by defect nucleation and glide, as the temperature decreases there is no longer enough thermal energy to relieve strain by these mechanisms. The result, as seen in the GaAs/Si system, is that the tensile strain is relieved by the incorporation of concave wafer bowing and cracking of the epilayer.[22,23,24] Similar to the critical thickness for defect nucleation during growth, the extent of the epilayer cracking also depends on the thickness of the epilayer, which determines the magnitude of the tensile strain energy introduced during cooling. Therefore, there is a "critical thickness", t_c, below which cracking will not occur. For the GaAs/Si system, reports indicate that this thickness is approximately 3-5 μm, after which epilayer cracking can result in a crack spacing of less than 200 μm along the <110> directions.[25, 26] Unfortunately, for direct GaAs/Si growth 3-5 μm is not sufficient for growth of a GaAs solar cell structure while still incorporating TDD reduction layers sufficient to reduce the TDD below ~$5x10^6$ cm^{-2}. The formation of cracks and wafer bow combined with the high TDDs has limited the success of GaAs/Si monolithic integration.

2.6 GaAs/Si integration via $Si_{1-x}Ge_x$ graded buffer layers

The $Si_{1-x}Ge_x$ alloy system has been used to obtain a low dislocation density Ge epilayer on a Si substrate. This allows $Ge/Si_{1-x}Ge_x/Si$ (SiGe) substrates to be treated as a "virtual Ge" substrates using the GaAs growth initiation methods discussed above. In this manner "APD-free" GaAs with low inter-diffusion for GaAs grown on SiGe has been confirmed as well as TDDs consistent with that of the SiGe substrates.[7] Figure 2.12 shows a representative X-TEM image of a GaAs layer grown on a SiGe substrate which exhibits no APD formation at the interface. The low TDD of the SiGe substrates is obtained by using compositionally step-graded $Si_{1-x}Ge_x$ buffer layers at an average grading rate of 10% Ge/μm. In this manner, the strain (lattice mismatch) is gradually introduced by increasing the Ge content, eliminating the need for the total system lattice-mismatch to be accommodated at a single heterointerface. This results in films with fewer TDs and MD segments than that achieved by direct growth (only 1 heterointerface).[27] For graded layers, TDs nucleated in the initial layers for strain relaxation are also capable of gliding and thus introducing a misfit segment at the new heterointerfaces as grading continues. The growth schematic for the SiGe substrates is shown in Figure 2.13.

Unfortunately, while the compositionally graded buffer layer technique effectively reduces TD nucleation, the MDs cause a "cross-hatch" surface morphology which can restrict TD dislocation glide such that the TDs may become "pinned" by the surface morphology and generate TD "pile-ups".[28] Once glide is impeded, the existing TDs and MD segments can no longer contribute to relaxation and additional TDs and MD segments must nucleated for continued relaxation as the grading continues and additional

strain is incorporated. This process effectively negates the benefits of compositionally step-graded buffer layers. Researchers at the Massachusetts Institute of Technology found that by incorporating a chemical mechanical polishing (CMP) at $Si_{0.5}Ge_{0.5}$ results in a "freeing" of the TDs in "pile-ups" so that the existing TDs can continue to glide and efficiently generate longer MD segments in order to relieve strain.[29,28] By eliminating the deep surface morphology that impeded TD glide, the additional nucleation of TDs was successfully suppressed, resulting in a 100% Ge layers on Si with TDDs of ~$1x10^6$ cm^{-2}. Further TDD reduction is predicted after process optimization (temperature, grading rate, placement of CMP, etc.).

Since GaAs and Ge have similar thermal expansion coefficients, the SiGe alloy system suffers from the same thermal mismatch issues discussed in Section 2.5 for the GaAs/Si material system. In the development of SiGe substrates, the tensile strain induced upon cooling is balanced by the intentional compressive strain generation in the final Ge layer, such that upon return to room temperature the final 100% Ge layer is cubic and relaxed.[29] However, while this method produces strain free and crack free Ge layers ~ 1 μm in thickness, the process of heating the SiGe substrates to growth temperature and the subsequent growth of thick GaAs layers will again induce tensile strain upon cooling and thus the GaAs and Ge epilayers are susceptible to cracking. Recently Yang et. al have studied GaAs grown on SiGe substrates and have found that the cracking threshold was ~ 3 μm and crack spacing along the off-cut directions , <110>, of ~ 170 μm for GaAs films grown at ~ 725-750 °C as indicated in Figure 2.14.[20] Figure 2.15 shows X-TEM images indicating that cracks in GaAs/SiGe extend into the Ge epilayers while GaAs/Si terminate at the Si surface, as expected. Conventional III-V

epitaxy of the as designed SiGe substrates poses similar thermal expansion coefficient mismatch problems experienced by conventional GaAs/Si epitaxy, such as wafer bow and epilayer cracking. While this work will not specifically consider solutions to epilayer cracking and wafer bow due to thermal mismatch, the impact on photovoltaic cell performance is discussed.

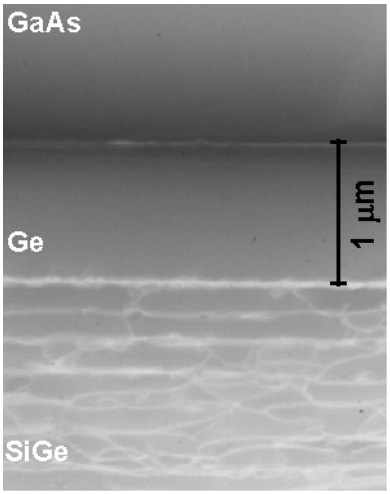

Figure 2.12 X-TEM of GaAs/SiGe showing APD suppression and low TDDs.

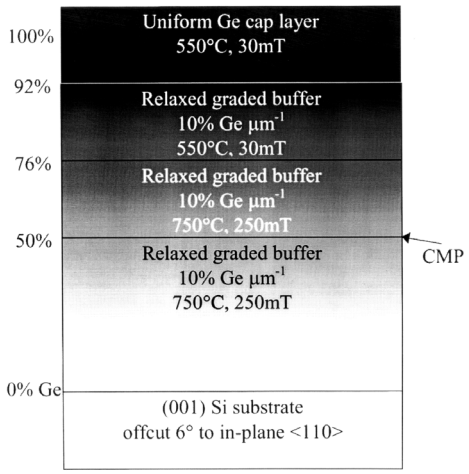

Figure 2.13 Ge_xSi_{1-x} grading scheme utilizing a CMP process during the grade in order "free" pinned threading dislocations. [after Ref. 29]

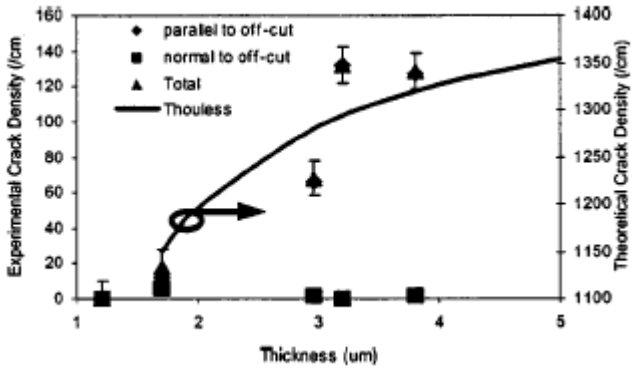

Figure 2.14 Crack density in GaAs on SiGe as a function of GaAs film thickness. The GaAs films were grown on SiGe substrates at 750 °C. The graph shows that cracks in the <110> direction which are parallel to the off-cut direction are dominate for GaAs films with thicknesses less than 4 μm. [after Ref. 20]

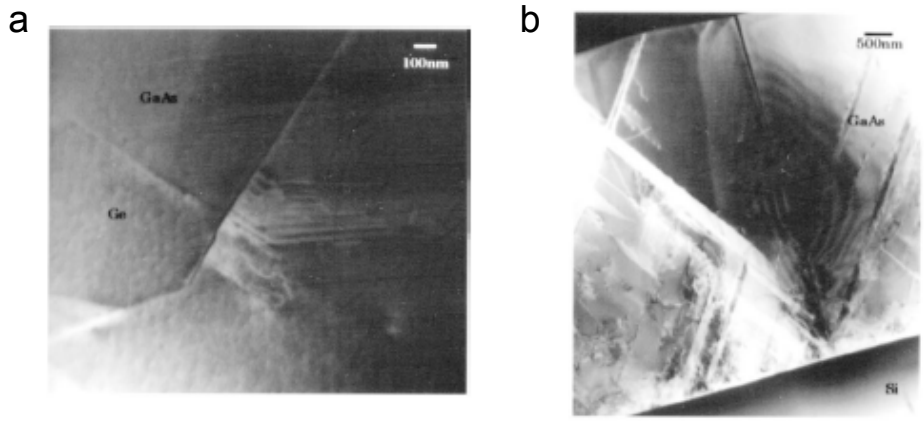

Figure 2.15 X-TEM micrographs of cracks in the epilayers, a) shows a GaAs thin film grown on a SiGe substrate, where the crack propagates beyond the GaAs/Ge interface. And b) shows GaAs/Si where the crack terminates at the Si substrate.[after Ref. 20]

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CHAPTER 3

PHOTOVOLTAICS

In this chapter we present an overview of photovoltaics (PV) to familiarize the reader with solar cell operation and the terminology used in this field. The need for both high efficiency and low cost solar cells is addressed as well as the development of high efficiencies solar cells on low weight, mechanically strong substrates for space application. The device structures for high efficiency III-V PV applications are presented. Moreover, the potential advantages of using Si as an alternative substrate for III-V photovoltaics are discussed and the state-of the-art GaAs/Si PV technology is presented. The use of Si substrates for III-V PV and the evolution of advanced high efficiency solar cells toward lattice-mismatch materials have motivated the study of conventional III-V materials grown on Si-based substrates presented in this thesis.

3.1 Solar cell device structures and operation

Figure 3.1 shows a cross-sectional view of the band diagram for a typical p+/n homojunction solar cell in the dark and under illumination. The p+/n configuration implies a p-type emitter and an n-type base where the emitter is illuminated first and is usually more highly doped and thinner compared to the base. The window and back

surface field (BSF) are heterostructures that serve to reduce recombination at these interfaces by the passivation of dangling bonds and the "reflection" of minority carriers back toward the junction due to a band-offset or band-bending. The materials used in these heterostructures have a higher bandgaps than the junction material to minimize parasitic photon absorption and should have band-offsets in the appropriate bands (conduction (E_c) or valence band (E_v)) in order to adequately "reflect" the minority carriers. Also, these heterostructures are usually lattice-matched to the active solar cell material to avoid the formation of defects at these interfaces that might increase recombination or reduce solar cell material quality.

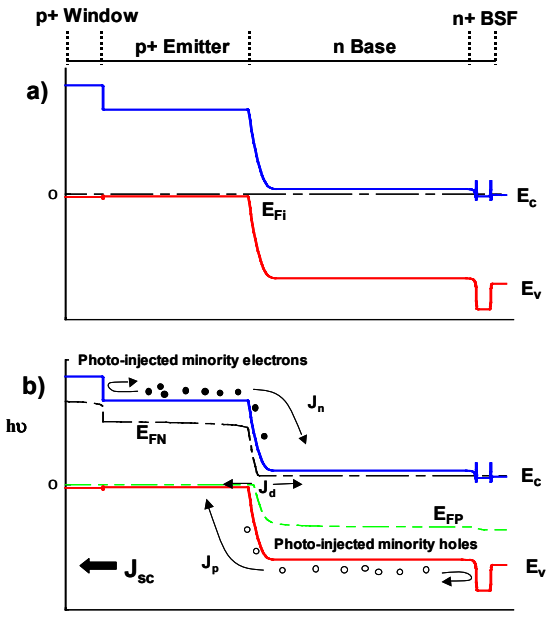

Figure 3.1: Cross-sectional view of the bands diagram for a p+/n homojunction solar cell a) in the dark and b) under illumination.

Device operation depends upon the solar cell's ability to absorb photons and provide the generated minority carriers to the external circuit. The illumination of the

device generates electron/hole pairs through the absorption of photons with energies greater than the bandgap of the material. These electrons and holes then diffuse in the layer either toward or away from the junction. The carriers that diffuse toward the junction are swept across the depletion region due to the built-in potential and thus become majority carriers on the opposing side of the junction. The carriers that diffuse away from the junction hopefully diffuse back toward the junction aided by presence of the heterojunction interface. The light current (J_L) generated is composed of the holes from the base (J_p), the electrons from the emitter (J_n), and the carriers generated in the depletion region (J_d). This light current flows in the direction opposing the conventional forward biased diode current. The basic form of the current density-voltage relationship, assuming the solar cell is a linear device, is shown in Equation 3.1. For convenience, this equation explicitly shows the opposing direction of J_L.

$$J = J_{dark}(V) - J_L \qquad \text{Equation 3.1}$$

By connecting the solar cell to a load, current will flow and a voltage will be measured across the load that equals the voltage across the junction. The voltage across the diode acts to forward bias the diode, and thus the current flowing is the forward bias current minus J_L. The maximum power from the solar cell is obtained when the resistance of load is such that both the J and V are maximized; this point is the maximum power point or P_m. Figure 3.2 shows an illuminated current density-voltage (LIV) curve in which P_m is denoted, also denoted are other solar cell performance characteristic namely, the short circuit current density (J_{sc}) and the open-circuit voltage (V_{oc}).

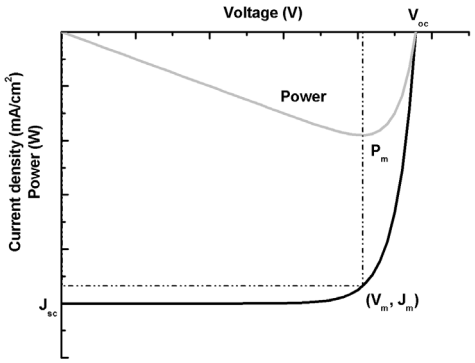

Figure 3.2: An illuminated current-voltage (LIV) characteristic for a solar cell is shown.

The short-circuit current density, J_{sc}, is measured with the solar cell biased at 0V; generally J_{sc} is equal to J_L, if there is negligible series resistance. The open-circuit voltage, V_{oc}, is measured at zero current flow; from Equation 3.1, it is clear that this condition occurs when $|J_{dark}|=|J_L|$. Typically, a higher J_L will produce a higher V_{oc} since the forward biased dark diode will generate a higher voltage in order to satisfy $|J_{dark}|=|J_L|$. The fill factor, *FF*, describes the "squareness" of the LIV curve and is defined by Equation 3.2. A higher *FF* indicates a higher P_m and better energy conversion.

$$FF = \frac{P_m}{I_{sc} \times V_{oc}} \qquad \text{Equation 3.2}$$

The solar cell efficiency (η) describes its ability to convert photons into electrical power, it is quantified as the ratio of the maximum power generated divided by the input power provided from the illumination source (P_{in}). It can also be described the by the performance parameters just discussed, as shown in Equation 3.3.

Equation 3.3

$$\eta = \frac{P_m}{P_{in}} = \frac{FF \times I_{sc} \times V_{oc}}{P_{in}}$$

3.2 Space and terrestrial photovoltaic applications

The solar spectrum incident on a solar cell depends on its locations. In space, the AM0 spectrum is considered the input spectrum and has an integrated power density, P_{in}, of 135.3mW/cm^2. However, the solar spectrum on earth is greatly influence by the Earth's atmosphere and the optical path length light must travel in the atmosphere. The standard spectrum used for terrestrial measurement is the AM1.5 spectrum with an integrated power density of 100.0 mW/cm^2. These spectra are shown in Figure 3.3. In the "AMn" nomenclature, AM stands for "air mass" and n=1/cos(θ) where θ is the angle of the sun from a position on earth. The shortest path length through the atmosphere is therefore described by the AM1 (θ = 0°). There is no "air mass" in space (AM0) since there is no atmosphere, thus the spectra in space does not follow this nomenclature.

The differences in the AM1.5 spectrum compared to the AM0 spectrum are a lower input power density, a large reduction in photons at short wavelengths (large energies > 2.5 eV), and a decrease in photons at long wavelengths (low energies < 0.9 eV). For these reasons the AM1.5 efficiencies are higher compared to AM0 efficiencies despite lower output powers. The theoretically calculated efficiencies for these spectra as a function semiconductor bandgap are shown in Figure 3.4. The optimum bandgaps are 1.4 eV to 1.6 eV for AM0 and AM1.5, respectively. In each case, GaAs represents an efficient solar cell material. The highest efficiencies achieved for single junction (SJ) GaAs homoepitaxial devices are 23% (AM0) and 25.1% (AM1.5).[1]

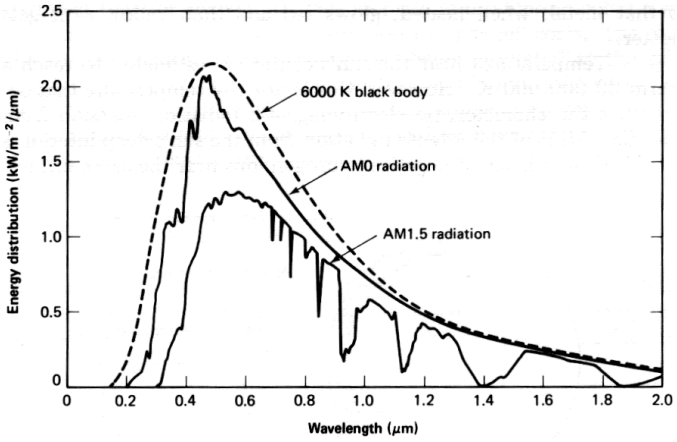

Figure 3.3 The AM0 and AM1.5 spectrum. [after Ref. 2]

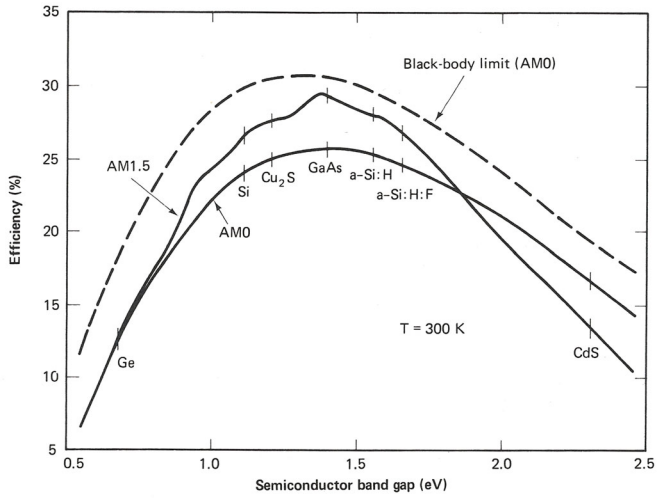

Figure 3.4 Efficiency versus bandgap for AM0 and AM1.5 spectrums. [after Ref. 2]

There are many factors that contribute to the reduced efficiencies in physically realized solar cells. The maximum efficiency models used in Figure 3.4 ignore losses due to surface recombination velocities (SRV), limited cell thickness, material absorption

coefficients, and the influence of material properties on the reverse saturation current (J_o); all of these factors will tend to decrease cell efficiencies. Variations amongst published models for $J_o(E_g)$ can change the maximum theoretical efficiency values as well as the ideal bandgaps for cell design.[3, 4, 5]. This should always be considered when comparing theoretical maximum efficiencies, practically achievable efficiencies (using measured material parameters and full device models), and physically realized efficiencies.

Besides the differences in space and terrestrial solar spectra, the needs for space and terrestrial PV application vary greatly. Terrestrial applications such as solar powered calculators do not require high efficiencies since it is a low power application; this is a high volume consumer device so low cost is the most important factor. Power generation for domestic electricity, usually requires low cost solar cells at the expense of solar cell efficiency since large area panels can be mounted to roofs or in un-populated land in order to obtain the desired power output. One terrestrial application that requires high efficiency cells are mobile powered devices for military applications, such as troops on foot. In this case, large solar panels are not easily transported or desired due to their high visibility. In space, high efficiency has always been important because higher efficiencies means fewer solar cells, a smaller footprint, and thus a lower launch weight for the solar array. The launching cost of the satellite in space is a are an appreciable percentage of the total cost, and thus cost of the actual solar cells is often less critical than their weight. The other major concern for space (and even terrestrial applications) is the mechanical strength of the solar cells; this issue will be addressed further in later sections.

3.3 High efficiency multi-junction solar cells

As mentioned above, high efficiency solar cells are of critical importance for space applications such as satellite power systems; this has lead to the development of high-efficiency multi-junction solar cells. To conserve area, solar cells with varying bandgaps are grown on top of each other. In this way, the solar cells can be connected in *series* epitaxially by using tunnel junction device layers as "low resistance contacts" between the cells. The method by which a multi-junction series stack takes advantage of the whole solar spectrum as illustrated in Figure 3.5. A schematic diagram of two, three and four-junction solar cell device structures are shown in Figure 3.6.

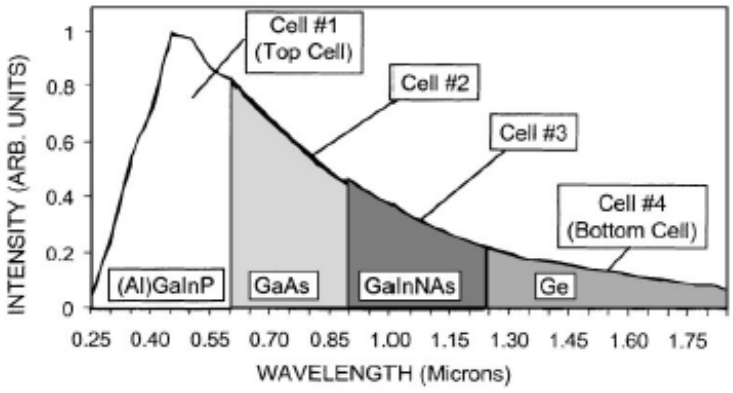

Figure 3.5 Schematic illustration of spectrum utilization for a series-connected four-junction solar. [after Ref. 6]

Since the individual junctions are connected in series (optically as well as electrically) the light current is reduced; this reduction is offset by the addition of the V_{oc} values of the individual cells and thus higher power and higher efficiencies are produced. Due to current continuity, the current through the stack will be limited by the worst-performing cell; each individual cell should be current-matched to all of the others in the

stack in order to maintain optimum performance. Current matching can be achieved by optimizing the thickness of each cell so that the proper numbers of photons are absorbed and collected in each sub-cell.

In the development of high efficiency multi-junction solar cells, lattice-matched materials were used to avoid the formation of dislocations. This imposes a limitation on the materials and thus bandgaps that can be used; in turn, this reduces the theoretically predicted efficiencies since the ideal bandgap values are not employed. The most common dual-junction (DJ) solar cell is the $In_{0.49}Ga_{0.51}P$/GaAs configuration. The $In_{0.49}Ga_{0.51}P$ cell is grown on top since its bandgap (1.9-1.85 eV) is larger than that of GaAs (1.42 eV), thus allowing lower-energy photons, which are not absorbed by the top junction, to pass through to the bottom junction. $In_{0.49}Ga_{0.51}P$/GaAs configuration DJ cells grown on GaAs substrates and have achieved maximum efficiencies of 29.5% for AM1.5 and 25.7% for AM0 illumination.[7] As mentioned above, the current in this cell (~16 mA/cm^2) is lower that of a GaAs SJ cell (~ 32 mA/cm^2) due to the spectral splitting; however, the V_{oc} of the DJ is ~ 2.4 V compared with ~ 1.05 V for a GaAs SJ cell, for AM0 illumination.

A further improvement in collection efficiency can be achieved by inserting a third junction, composed of 0.67 eV bandgap Ge, below the GaAs junction. This is achieved by growing the conventional DJ structure on a Ge substrate under such conditions that a diffused n/p junction is formed in the Ge substrate. This results in a triple-junction (TJ) solar cell with the same J_{sc} as the DJ cell since the DJ structure wastes all photons with energies less than 1.42 eV (0.87 μm). An external quantum efficiency measurement for such a TJ solar cell is shown in Figure 3.7. Efficiencies for TJ cells

have evolved with use of optically transparent tunnel-junctions and with improvements in the diffused Ge junctions; currently the maximum efficiencies measured for this structure are 32.3% for AM1.5 and 29.3% for AM0 illumination.[8] Again, this structure does not necessarily represent the theoretically optimum bandgap profile for a triple-junction cell; however, it does maintain the lattice-matched condition since there is only a 0.07% lattice mismatch between GaAs and Ge.

For a quadruple-junction solar cell, a 1.0 eV sub-cell in between the GaAs and Ge junctions of the existing Ge-GaAs-InGaP TJ device structures would boost the efficiency of the resulting four-junction cell to 41% (AM1.5).[9] Due to the bowing parameter in the lattice constant of the InGaAsN alloy, $In_{0.08}Ga_{0.92}As_{0.97}N_{0.03}$ can be grown lattice-matched to GaAs while obtaining a bandgap of ~1.0 eV. To date single-junction InGaAsN solar cells have been inefficient and no high efficiency 4-junction solar cells have been produced; InGaAsN material quality has been the limiting factor.

Conventional $In_{0.48}Ga_{0.52}P$/GaAs based commercial cells on Ge substrates have average lot efficiencies of ~19.0%, ~21.8% and ~28.3% for SJ, DJ and TJ cells respectively for AM0 illumination.[10] In recent years, there has been little advancement in the SJ and DJ technologies since the TJ technology has shown so much promise. Another reason the SJ and DJ are lower than those reported above is that these are grown on an in-active Ge substrate which can introduce some cell degradation. The reason for the use of this alternative substrate is discussed in Section 3.5.

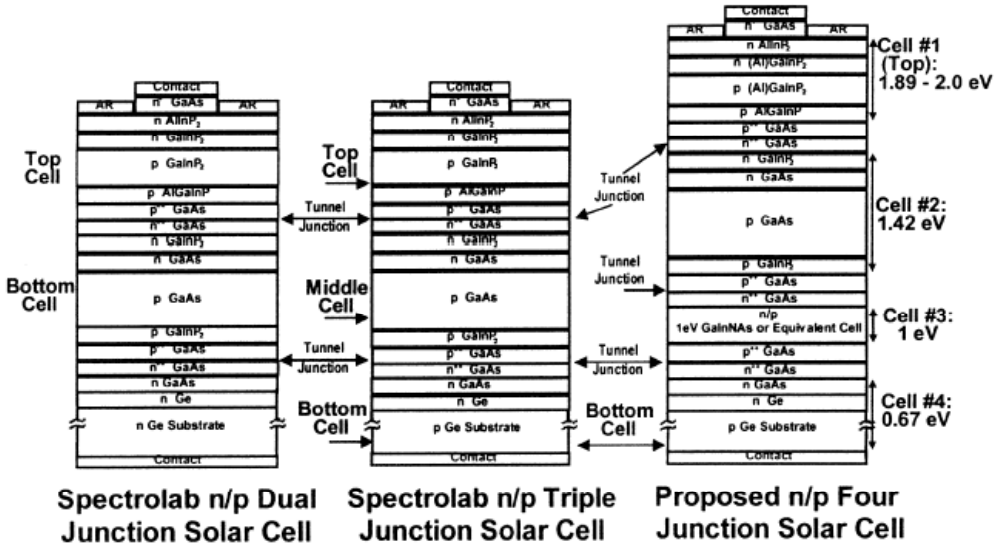

Figure 3.6 Spectrolab's dual, triple, and quadruple junction solar cell structures. [after Ref. 6]

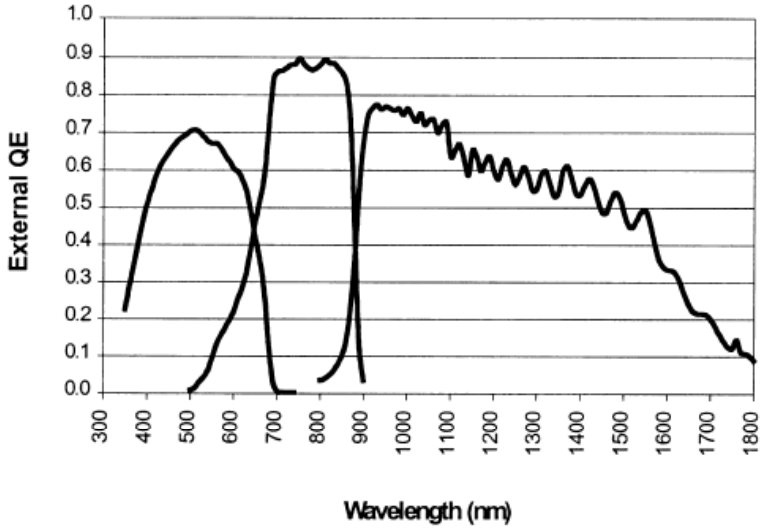

Figure 3.7 Quantum efficiency for a triple junction solar cells showing collection from the InGaP, GaAs, and Ge sub-cells. [after Ref. 6]

3.4 PV system costs

Although there have been drastic reductions in manufacturing costs for multi-junction solar, high efficiency III-V cells are still more expensive per watt than Si based photovoltaics. However, for space applications, the weight, the efficiency, and the radiation resistance of the solar array are also important parameters and were analyzed by Fatemi et. al. [11]. The beginning of life (BOL) and end of life (EOL) efficiencies for crystalline Si, InGaP/GaAs DJ and InGaP/GaAs/Ge TJ solar cells are compared in Table 3.1, along with the power density (W/m^2), the specific power (W/ kg), and the normalized cost /W. Note, the information provided uses the EOL for low earth orbit (LEO) conditions (80°C), which takes into account the degradation of the cell due to exposure to cosmic radiation (1 MeV electrons at a dose of $1x10^{15}$ electrons/cm^2). It is clear that the Si cells are the cheapest per watt. However, when we consider the specific power for the cells after they are CICed (Cells are Interconnected and Covered) and attached to the solar panel, as shown in Table 3.2, we find that the multi-junction solar panels have a higher specific power than the Si solar panels. Considering the normalized cost for the assembled panels, we find that the multi-junction solar cells are in fact cheaper per watt as well. Moreover, since the weight saving will also reduce the launch costs, which are typically $10,000-20,000/ kg for LEO orbit [12]. The weight savings for a 10,000 W array are ~56 kg which translate to a cost saving of $1,120,000 for a TJ solar panel compared with Si solar panel. Table 3.3 shows the launch cost saving when high-efficiency cells are used.

Cell Technology	Cell Efficiency BOL/EOL	W/kg (EOL)	W/m^2 (EOL)	Cell Cost (EOL) ($/Watt)
Single Crystal Silicon	17% / 13.4%	574	143	1.00
DJ InGaP/GaAs/Ge	23.5% / 19.8%	288	245	1.29
TJ InGaP/GaAs/Ge	26% / 22.6%	323	275	1.15

Table 3.1 Comparison of cell efficiency, specific power (W/kg), power density (W/m^2), and normalized cost for various solar cell technologies. [after Ref. 11]

Cell Technology	CIC W/kg	Panel W/kg	Panel Cost ($/Watt)
Single Crystal Silicon	221	63	1.00
DJ InGaP/GaAs/Ge	199	86	0.84
TJ InGaP/GaAs/Ge	223	97	0.75

Table 3.2 Specific power (W/kg) for packaged (CIC) and assembled (panel) solar cells and the normalized panel cost for various solar cell technologies [after Ref. 11]

Cell Technology	TJ GaInP/GaAs/Ge	DJ GaInP/GaAs/Ge	Conventional Si
EOL array (Watts/kg)	97	86	63
EOL Watts needed	***10,000***	***10,000***	***10,000***
Est. weight of array	103 kg	116 kg	159kg
Weight savings	56 kg	43 kg	-
Launch cost savings	$1,120,000	$860,000	-

Table 3.3 Launch cost comparison between TJ InGaP/GaAs/Ge, DJ InGaP/GaAs/Ge, and conventional Si solar arrays assuming launch costs of $20,000/kg. [after Ref. 11 and 13]

3.5 Alternative substrates for III-V PV

From the discussions above, it is clear that Ge substrates are used in space PV applications, not GaAs substrates. This may be surprising considering the lattice-mismatch and the polar/non-polar interface of the GaAs/Ge material system; however, Ge substrates are used for very practical reasons. First, (100) substrates are used III-V PV materials and the cleavage planes ({110}) are perpendicular to the to the substrate's surface; any pressure applied to the surface can easily fracture the III-V substrates.[14] This is especially true for space PV applications where, due to weight considerations, the substrate should be thin (<140 μm). Production solar cells on GaAs had very poor yields for this reason and thus were not practical from a manufacturing perspective.[15] The cleavage planes for Ge (and Si) are {111} type planes which lie at an angle with respect to the substrate (100) surface and therefore can with stand more force with out fracture. This fact, coupled with the extra mechanical strength of Ge over GaAs makes Ge a better substrate candidate for PV applications. Moreover, the GaAs/Ge incompatibilities were resolved and high efficiency III-V/Ge solar cells were produced, thus Ge substrates have become the industry standard. Of course, using a Ge substrate has another advantage since it can be used as the bottom cell in high efficiency triple-junction (TJ) solar cells.

PV manufacturers have found that Ge substrates can be thinned to ~140 μm for use in PV arrays where as a GaAs substrate would need a thickness of greater than 500 μm; the weight of a cell on Ge would be ~ 30% of that on GaAs. Since Si is less dense (see Table 3.4) and similar substrate thicknesses can be obtained, a high efficiency III-V cell on Si could weigh ~ 12% of that on GaAs, thus increasing the specific power if high efficiencies can be achieved. Another advantage of Si over Ge is the high availability,

large area, and low cost of Si substrates which can help to further decrease costs and increase manufacturing capacity. This would allow the transfer of such technologies to terrestrial applications. Of course for III-V/Si applications, the impact of a 4% lattice mismatch and other mismatched properties discussed in Chapter 2 need to be addressed.

Comparison of Substrate Materials

Properties	GaAs	Ge	Si
Mass density (g cm^{-3})	5.318	5.323	2.329
Hardness (mohs)	4-5	6.3	7
Thermal conductivity (W/(cm K))	0.06	0.8	1.3
Thermal expansion mismatch	0%	3%	125%
Lattice mismatch	0%	0.07%	4%
Substrate Diameters (in)	3-6	3-8	8-12
Relative Substrate Cost	high	mid	low

Table 3.4 Comparison of substrate properties, all mismatch values are relative to GaAs.[16]

3.6 SJ GaAs on Si

Many groups have recognized the potential benefits of epitaxial III-V/Si solar cells, which has lead to investigations of methods to control and reduce threading dislocation densities (TDDs) in this lattice-mismatched heterostructure. These groups have been successful in reducing threading dislocation densities in the III-V over-layers from ~ 10^{9}-10^{10} cm^{-2} for direct GaAs on Si epitaxy to ~$7x10^{6}$-$1x10^{7}$ cm^{-2} range using strained-layer super-lattices, thermal cycle annealing, or intermediate lattice constant III-V layers. In these works, the minority carrier lifetimes measured to asses the material quality in GaAs epitaxial layers are 1-3.5 ns, while the V_{oc} values for p+/n SJ GaAs cells

typically on the order of 940 mV and lower, under AM0 conditions. The TDD reduction methods mentioned above all utilize III-V materials to obtain the GaAs lattice parameter.

Another approach that has been investigated is the accommodation of lattice mismatch prior to III-V epitaxy. By the growth of step-graded $Si_{1-x}Ge_x$ layers, up to 100% Ge, on Si substrates the lattice mismatch is addressed in a non-polar material system and under growth conditions that are independent from the III-V solar cell growth conditions. This "virtual Ge substrate" approach has resulted in threading dislocation densities less than $1x10^6$ cm^{-2} within relaxed GaAs overlayers.[17, 18] The impact of this lower TDD and a controlled GaAs/Ge interface has yielded the highest minority carrier lifetimes reported to date for GaAs grown on Si, with values in excess of 10 ns being demonstrated in n-type GaAs at a doping concentration of $1x10^{17}$ cm^{-3}.[18] Also, a record high AM0 V_{oc} for verified single junction GaAs cells, greater than 980 mV, have been achieved for p+/n cells on SiGe substrates.[19] This work, by our research group at The Ohio State University, has shown the III-V/SiGe is a viable option for high efficiency III-V solar cells on a Si-based substrate and serves as the starting point for future III-V solar cell development. Specifically, the impact of device polarity is explored by studying the impact of TDD on electron lifetime p-type GaAs and comparing the performance of n+/p GaAs SJ solar cells on SiGe with p+/n device performance.

3.7 Other lattice-mismatched photovoltaic devices

As alluded to in Section 3.3, physically realized solar cell efficiencies have been limited by both lattice constant as well as epitaxial layer material quality. Dual junction theoretical iso-efficiency contours are shown in Figure 3.8. The conventional dual junction cell design uses a top cell of $In_{0.49}Ga_{0.51}P$ that is lattice-matched to the GaAs bottom cell and lattice-matched to a GaAs (Ge) substrate. This design is indicated by I in Figure 3.8; DJ efficiencies of ~26% have been achieved for this structure; although, this is lower than the 32% theoretical limit shown in the figure. The iso-efficiency curves in Figure 3.8 show that by moving to a lattice-mismatched compound such as $In_xGa_{1-x}As$, in place of the GaAs bottom cell, DJ cell efficiencies could significantly improve.

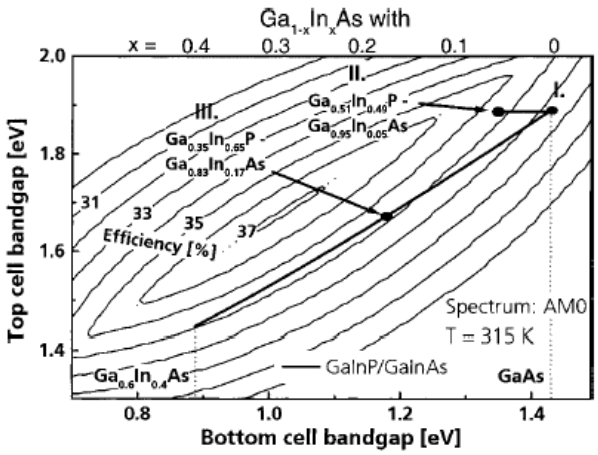

Figure 3.8: Projected maximum iso-efficiencies contours versus bandgap of the top and bottom cell for an AM0 spectrum for a dual junction solar cell. [after Ref. 5]

Great interest in lattice-mismatched high efficiency DJ and TJ solar cells has been shown in recent years.[5,20, 21, 22] However, as described in Section 3.6, the introduction of thick lattice-mismatch layers will introduce lattice-mismatch defects such as TDs. The impact of TDD for n-type GaAs has been quantified, but there is relatively little information on other material systems or polarity materials. To better design such lattice-mismatched solar cells requires the understanding the impact of TDD on different materials such as $In_xGa_{1-x}As$ and $In_xGa_{1-x}P$. To this end, SJ $In_{0.49}Ga_{0.51}P$ and $In_{0.49}Ga_{0.51}P$/GaAs DJ solar cell performance are modeled in this thesis as a function of TDD. Experimental demonstration n+/p and p+/n SJ $In_{0.49}Ga_{0.51}P$ and p+/n $In_{0.49}Ga_{0.51}P$/GaAs DJ solar cells on SiGe substrate are then compared with modeling results.

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CHAPTER 4

SOLAR CELL MODELING

Various device models will be discussed in this thesis, this chapter houses the basic equations, variable names, and analysis methods employed. These equations help identify the important materials parameters and their influence on solar cell performance. For example, the impact of a diodes' reverse saturation current (J_o) and a diodes' effective ideality factor (n) on a solar cells' open circuit voltage (V_{oc}) and fill factor (FF). The impact of threading dislocations on material properties and device performance are not discussed in this chapter explicitly, but are covered in detail in later chapters.

4.1 Dark current

Two contributions to the dark diode current density will be considered in this thesis, one is the ideal diode current (n_1=1) which accounts for the finite dimensions of an n/p junction and carrier recombination at material interfaces, while the other accounts for carrier recombination in the depletion region (n_2~2).

$$J_{dark} = J_{o1}\left(\exp\left(\frac{qV}{n_1 kT}\right)-1\right)+J_{o2}\left(\exp\left(\frac{qV}{n_2 kT}\right)-1\right) \qquad \text{Equation 4.1}$$

The J_{o1} term in Equation 4.1 is the diffusion component of the reverse saturation current. An analytic expression for J_{o1} was derived using the current density and continuity equations and assuming no generation in the diode, no recombination in the depletion region, the Boltzman approximation is valid, low-level injection is valid, steady state, and that the quasi-fermi levels are constant across the depletion region. With these assumptions the minority carrier concentrations at the edges of the depletion regions are determined, resulting in the following expression for J_{o1}.[1]

$$J_{o1} = J_p + J_n$$
$$= qn_i^2\left(\frac{F_p}{N_A}\left(\frac{D_n}{\tau_n}\right)^{1/2} + \frac{F_n}{N_D}\left(\frac{D_p}{\tau_p}\right)^{1/2}\right) \qquad \text{Equation 4.2}$$

where:

$$F_p = \frac{S_n \cosh(W_p/L_n) + (D_n/L_n)\sinh(W_p/L_n)}{S_n \sinh(W_p/L_n) + (D_n/L_n)\cosh(W_p/L_n)}$$

$$F_n = \frac{S_p \cosh(W_n/L_p) + (D_p/L_p)\sinh(W_n/L_p)}{S_p \sinh(W_n/L_p) + (D_p/L_p)\cosh(W_n/L_p)}$$

N_A = acceptor concetration in p - type layer
N_D = donor concetration in n - type layer
W_n = n – type layer width (excluding depleted region)
W_p = p – type layer width (excluding depleted region)
W_d = depletion layer width
L_p = minority carrier hole diffusion length
L_n = minority carrier electron diffusion length
D_p = minority carrier hole diffusion coefficient
D_n = minority carrier electron diffusion coefficient
τ_p = minority carrier hole lifetime
τ_n = minority carrier electron lifetime
S_n = minority carrier electron surface recombination velocity
S_p = minority carrier electron surface recombination velocity
n_i = intrinsic carrier concetration

The width of the depletion layer (W_D) is described by Equation 4.3 and Equation 4.4 using the "depletion approximation".[2]

$$W_D = x_n + x_p$$

Equation 4.3

$$= \left[\frac{2k_s\varepsilon_o}{q}(V_{bi} - V)\left(\frac{N_A}{N_D(N_A + N_D)} \right) \right]^{1/2} + \left[\frac{2k_s\varepsilon_o}{q}(V_{bi} - V)\left(\frac{N_D}{N_A(N_A + N_D)} \right) \right]^{1/2}$$

$$= \left[\frac{2k_s\varepsilon_o}{q}(V_{bi} - V)\left(\frac{(N_A + N_D)}{N_A N_D} \right) \right]^{1/2}$$

$$V_{bi} = \frac{kT}{q} \ln\left[\frac{N_D N_A}{n_i^2} \right]$$

Equation 4.4

The portion of the depletion region located in the n-type layer (x_n) and p-type layer (x_p) of the junction are written here explicitly since this thickness is accounted for in the emitter and base layer thicknesses, x_p and x_n. From this equation it is clear that the depletion layer width is a function of applied voltage (V); it decreases in forward bias (V>0) and increases in reverse bias (V<0). This has little impact on J_{o1} since these widths are usually small perturbations to the total layer thickness. Therefore, most analysis methods do not account for the voltage dependence of the base and emitter layer thickness and use the unbiased values (V=0).

Equation 4.2 can also be written entirely in terms the minority carrier mobility instead of the minority carrier diffusion coefficient using Equation 4.5 and the minority carrier diffusion length instead of the minority carrier lifetime using equation Equation 4.6. Thus, J_{o1} tends to increase with decreasing minority carrier lifetime and decreasing

diffusion length. Since τ and L as well as D depend on the dopant concentration, it is not obvious from this equation how the J_{o1} responds to doping changes.

$$\frac{D}{\mu} = \frac{kT}{q} \qquad \text{Equation 4.5}$$

$$L = (D\tau)^{1/2} \qquad \text{Equation 4.6}$$

Other forms of Equation 4.2 are often presented in textbooks; these include the infinite diode approximation, where F_n and F_p converge to 1, and the one-side abrupt infinite diode where the minority carrier current from the low-doped base is the only contribution to J_{o1}.[2] The full expression for J_{o1} will be used in this thesis; however, in Chapter 7 the infinite diode expression is compared to the full expression to examine the impact of such an approximation on J_{o1}.

The depletion region recombination current (J_{o2}) was determined from Shockley-Read-Hall recombination statistics for a single trap level, E_T. Equation 4.7 represents the steady state carrier recombination rate, R ($s^{-1}cm^{-3}$).

$$R = \frac{np - n_i^2}{\tau_{po}(n + n_{T1}) + \tau_{no}(p + p_{T1})} \qquad \text{Equation 4.7}$$

where:

$$n_{T1} = N_C \exp\left(-\frac{E_C - E_T}{kT}\right)$$

$$p_{T1} = N_V \exp\left(\frac{E_V - E_T}{kT}\right)$$

(In this equation N_C an N_V are the effective densities of the conduction and valence bands respectively.) It is reasonable to assume that the quasi-Fermi levels are flat in the depletion region [3]; thus the *np* product in the depletion region can be can be described by $np = n_i^2 \exp(qV / kT)$ where V is the voltage applied across the junction. Moreover, the carrier concentrations, *n* and *p*, must cross at some point within the depletion region; thus $n = p = n_i \exp(qV / 2kT)$. Consequently, assuming that the recombination-generation center is at mid-gap ($n_{TI} \approx n_i \approx p_{TI}$) and equal capture cross-sections for both holes and electrons ($\tau_o = \tau_{no} = \tau_{po}$) the recombination rate at this point ($n=p$) can be described by $R = (n_i / 2\tau_o)\exp(qV / 2kT)$, the recombination current density can then be calculated as shown in Equation 4.8. It should be noted that Sah-Noyce-Shockley [3] investigated this for a symmetric junction as a function of E_T, while Choo [4] examined this for an asymmetric junction. One result of Choo's analysis was lower recombination values for an n+/p than a p+/n diode for donor-like trap levels; however, the reverse was true for acceptor-like trap levels. The impact on trap energy is not modeled in this thesis and only the mid-gap trap approximation just described is used to calculate the depletion region recombination component, J_{o2}.

$$J_r \approx qW_D R = qW_D \frac{n_i}{2\tau_o}\left(\exp\left(\frac{qV}{2kT}\right)-1\right) = J_{o2}\left(\exp\left(\frac{qV}{n_2 kT}\right)-1\right) \qquad \text{Equation 4.8}$$

$$J_{o2} = qW_D \frac{n_i}{2\tau_o}$$

Using W_D as the width of the depletion region assumes uniform R-G in the entire depletion region; however, this is an over estimate since $n \approx p$ exists over a much smaller region. There will be recombination-generation in the rest of the depletion region but it will not be described by n=2; this is one of the reasons why physically realized diodes can exhibit n_2 values less than 2. Also, Equation 4.8 shows a direct correlation of W_D on J_{o2}. This implies that lower base doping values will increase in the depletion region width and thus will increase J_{o2}. Moreover, since J_{o2} decreases with decreasing W_D and thus increasing applied voltage (V), the effective ideality factor can in fact be greater 2. Most models do not account for the voltage dependence of W_D when calculating I-V characteristic or solar cell parameters [1, 5]; however, such effects are considered in Ref. 3 and 4. In this thesis, the voltage dependent and voltage independent depletion widths will be used in Chapter 7 and the impact on device modeling results are discussed. It is stated explicitly in the text when the voltage dependent models are employed.

Another term, which is implemented in various ways in the literature, is τ_o in Equation 4.8. Ref. 3 and 4 use $\tau_o = \sqrt{\tau_{po}\tau_{no}}$, Ref. 2 uses $\tau_o = 0.5\left(\tau_{po} + \tau_{no}\right)$; in this thesis, the minority carrier lifetime used will be that associated with the diode's base, τ_{base}; since the base is the layer in which the majority of the depletion region is formed. This is consistent with Ref. 5 where the impact of TDs on τ and J_o are also discussed. Note, the minority carrier lifetime is inversely related to J_{o2} and thus reductions in lifetime will increase the reverse saturation current of the diode

4.2 Light current

The generated light current (J_L) was derived in the same manner as the reverse saturation current component J_{o1}; however, this time the generation term is non-zero. Carrier generation is characterized by the absorption of photons in the material as given by Equation 4.9.

$$G(x,\lambda) \approx \alpha(\lambda)\Gamma_o(\lambda)\exp(-\alpha(\lambda)x) \qquad \text{Equation 4.9}$$

where:
$\alpha(\lambda)$ = absorption coefficent
$\Gamma_o(\lambda)$ = incident flux of photons

For an n/p cell, the hole current from the n-type emitter at the edge of the depletion region (J_p) and the electron current from the p-type base at the edge of the depletion region (J_n) are evaluated since it is assumed that all carriers entering the depletion region are collected. Then, assuming that all photons absorbed in the depletion region create an electron/hole pair, which cross the junction, the depletion region contribution (J_d) to the light current is calculated. The equations used for each current component are given below.[1] The total light current (J_L) is the sum of all three components integrated over all wavelengths. Parasitic absorption in window layers, back surface fields, and tunnel junctions as well as surface reflectance can be accounted for by adjusting the incident photon flux ($\Gamma_o(\lambda)$).

$$J_p = q\Gamma_o\left(\frac{\alpha L_p}{(\alpha L_p)^2 - 1}\right)\left(F_{p1} - F_{p2}\exp(-\alpha W_n)\right) \qquad \text{Equation 4.10}$$

where:

$$F_{p1} = \frac{S_p + \alpha D_p}{S_p \sinh(W_n / L_p) + (D_p / L_p)\cosh(W_n / L_p)}$$

$$F_{p2} = \alpha L_p + \frac{S_p \cosh(W_n / L_p) + (D_p / L_p)\sinh(W_n / L_p)}{S_p \sinh(W_n / L_p) + (D_p / L_p)\cosh(W_n / L_p)}$$

$$J_n = q\Gamma_o\left(\exp(-\alpha(W_n + W_d))\right)\left(\frac{\alpha L_n}{(\alpha L_n)^2 - 1}\right)\left(F_{n1} - F_{n2}\exp(-\alpha W_p)\right) \qquad \text{Equation 4.11}$$

where:

$$F_{n1} = \alpha L_n - \frac{S_n \cosh(W_p / L_n) + (D_n / L_n)\sinh(W_p / L_n)}{S_n \sinh(W_p / L_n) + (D_n / L_n)\cosh(W_p / L_n)}$$

$$F_{n2} = \frac{-S_n + \alpha D_n}{S_n \sinh(W_p / L_n) + (D_n / L_n)\cosh(W_p / L_n)}$$

$$J_d = q\Gamma_o\left(\exp(-\alpha(W_n))\right)\left(1 - \exp(-\alpha W_d)\right) \qquad \text{Equation 4.12}$$

$$J_L = \int_{\lambda}\left(J_n + J_p + J_d\right)d\lambda \qquad \text{Equation 4.13}$$

Although this is a complicated equation, longer diffusion lengths typically lead to higher light currents since the carriers have a higher probably of being collected at the junction before they recombine. If the device layers are significantly longer than the diffusion length than the benefit of back-surface fields are lost. If the diffusion lengths are comparable to the layer thickness or longer, than high surface recombination velocities have a significant impact on J_L through the loss of carriers at these interfaces. For a dual junction cell, the spectral splitting is obtained by varying the width of the top cell such that adequate photons arrive at the bottom cell to obtain a current-matched light current in each cell. The value of J_L calculated depends greatly on the absorption coefficient and the incident photon flux spectrum used which makes the comparison of theoretically calculated and experimental values difficult; thus spectral splitting in multi-junction solar cells is usually optimized experimentally.

TDs reduce both the minority carrier lifetime and the diffusion length and thus at certain TDD values ($> 1x10^7$ cm^{-2}), significant reductions in J_L are predicted.[5] However, in this thesis we have chosen to use a constant value of J_L as a function of TDD. A constant value of J_L is used so that the influence of device performance from changes in J_o alone can be determined. This may result in overestimated V_{oc} values compared with models that account for changes in J_L with TDD.

4.3 Current density - voltage curves

The current voltage curves for solar cells presented in this thesis will use the form shown in Equation 4.14.

$$J = J_{o1}\left(\exp\left(\frac{qV}{kT}\right)-1\right)+J_{o2}\left(\exp\left(\frac{qV}{2kT}\right)-1\right)-J_L \qquad \text{Equation 4.14}$$

For a single junction solar cell a vector of voltage values is used in Equation 4.14 to calculate the expected current density, *J*. The dark current density – voltage curve (DIV) is determined for J_L=0, while the illuminated current density – voltage curve (LIV) includes the desired light current. However, in order to determine the V_{oc} value from the LIV curve, Equation 4.14 was solved numerically for the *J*=0 condition. For a series-connected dual junction solar cell, the voltage across each junction differs for a given value of *J*. In this case, a vector of current values is defined and the voltage across each junction is numerically solved at each current density value. The voltages from each cell are then summed to generate the total voltage across the dual-junction solar cell for a given current density. The resulting voltage and current density vectors represent the DJ current-voltage relationship. The effective ideality factor, *n*, as function of voltage is determined by calculating the derivative the natural logarithm of the *J* with respect to the *V,* dividing by *q/kT*, and inverting the result. This n-V relationship helps identify the transition between J_{o2} and J_{o1} dominance. The *FF* for the LIV curve is calculated numerically, by multiplying the current vector by the voltage vector, which results in the power vector. From this the maximum power point can be found directly and P_{max} is divided by the product of J_{sc} and V_{oc} determined by the end point of the current vector *J*= J_{sc} and *J*=0 and thus the *FF* is determined. As mentioned above the J_L (or J_{sc} if series resistance is negligible) is taken to be a constant for a particular cell configuration; the values typically used in this thesis for a SJ GaAs cells is 30 mA/cm^2 and for SJ $In_{0.49}Ga_{0.51}P$ or DJ $In_{0.49}Ga_{0.51}P$ /GaAs cells is16 mA/cm^2 for an AM0 spectrum.

Series resistance (R_s) and shunt resistance (R_{sh}) are not accounted for in the theoretical device models used in this thesis since we are concerned with impact of cell performance due to changes in depletion region recombination, not the influence of resistance. However, it is important to understand the impact of R_s and R_{sh} on the solar cell LIV curves and solar cell parameters. The resistance values are incorporated in the IV relationship as shown in Equation 4.15. The sources of R_s in a solar cell are the bulk resistance of the semiconductor and the resistance of the contacts and interconnects. One issue of importance is the emitter sheet resistance since this layer is typically thin and current needs to be transported horizontally in order to be collected at the grid fingers. Conduction through heterojunction interfaces can also lead to increased series resistance values. The sources of R_{sh} are more difficult it quantify since they depend on lattice defects in the depletion region or leakage currents at the mesa sidewalls. Figure 4.1 shows the impact of both R_s and R_{sh} on LIV and solar cell performance characteristics. It is clear that R_s impacts the FF and I_{sc} but has little impact on the measured V_{oc} value. Where as, R_{sh}, impacts the FF and V_{oc} but has little impact on I_{sc}.

Equation 4.15

$$I = I_{o1}\left(\exp\left(\frac{q(V - IR_s)}{kT}\right) - 1\right) + I_{o2}\left(\exp\left(\frac{q(V - IR_s)}{2kT}\right) - 1\right) - \frac{V - IR_s}{R_{sh}} - I_L$$

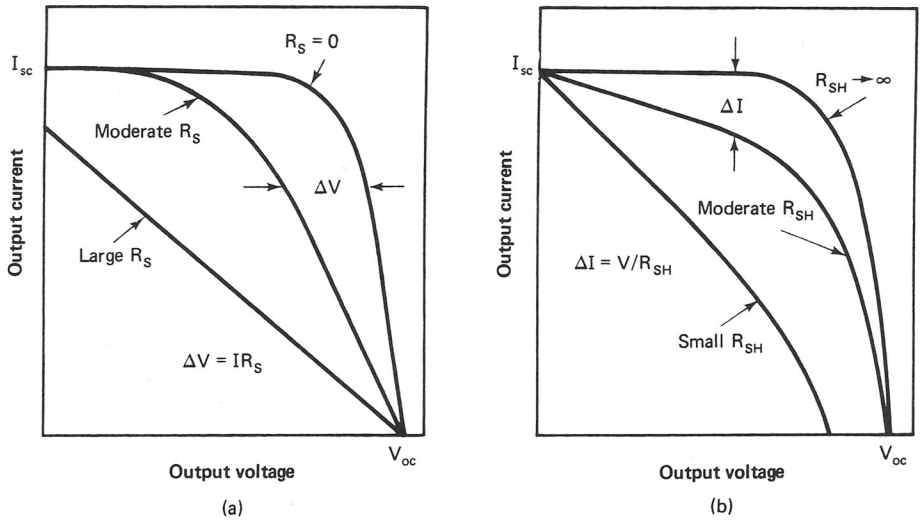

Figure 4.1 The effect of a) series resistance (R_s) and b) shunt resistance (R_{sh}) on the performance characteristics of a solar cell. [after Ref. 1]

In Figure 4.2 the dark current density – voltage (DIV) curve for a GaAs p+/n diode with no TDs is plotted. Four different models are used; the solid lines represent the use of both J_{o1} and J_{o2} in Equation 4.14 with both voltage independent and dependant depletion widths and the dashed lines represent the use of only the J_{o2} term in Equation 4.14 with voltage independent and dependant depletion widths. Examining these curves we find that the J_{o1} term starts to dominate at ~ 1V as shown by an increase in the slope of the solid lines. It is clear that a decrease in W_D with increasing voltage causes a decrease J_{o2} and the slope of the DIV; the effective ideality factor for a voltage dependant W_D is ~2.1 compared with 2 for the voltage independent W_D.

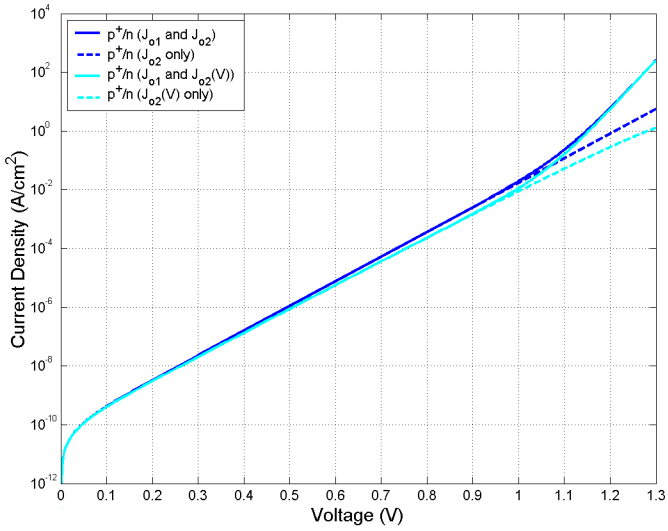

Figure 4.2 The dark current density – voltage (DIV) curve for a GaAs p+/n diode with no TDs using 4 different diode models.

In Figure 4.3 the illuminated current density - votlage (LIV) curve for a GaAs p+/n diode with no TDs is plotted using a J_{sc} value of 30 mA/cm^2. It is evident that lower V_{oc} values result from the voltage independent W_D due to higher J_o values. The FF values are lower for the dashed line since they only incorporate J_{o2} and thus have higher effective ideality factors, although, they have higher V_{oc} values. Using the J_{o2} diode model, the dependence of the V_{oc} on J_{sc} and J_{o2} is shown in Equation 4.16. It is clear that higher J_o values decrease V_{oc} where as higher J_{sc} values increase V_{oc}.

$$V_{oc} \approx \left(\frac{2kT}{q}\right)\ln\left(\frac{J_{sc}}{J_{o2}}\right) = \left(\frac{2kT}{q}\right)\left(\ln\left(J_{sc}\right) - \ln\left(J_{o2}\right)\right) \qquad \text{Equation 4.16}$$

The dominance of the J_{o2} component exhibited in the DIV and LIV curves for SJ GaAs solar cells indicates the importance of the minority carrier lifetime on V_{oc} as shown in Equation 4.8. This relationship will be studied in detail in subsequent chapters as the minority carrier lifetimes are reduced by the presence of TDs.

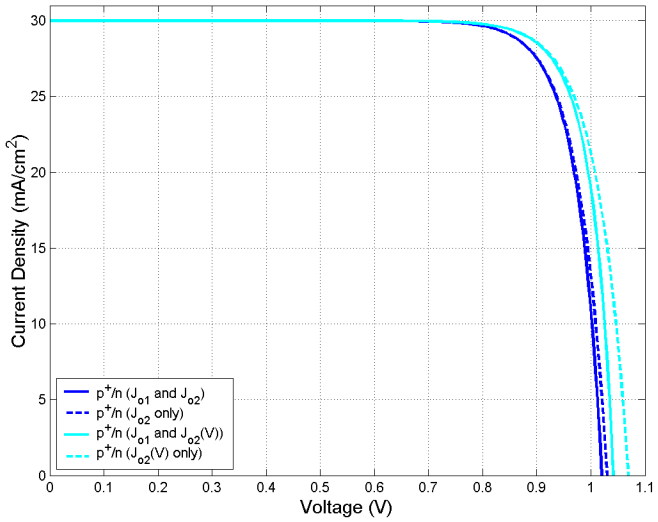

Figure 4.3 The light current density – voltage (LIV) curve for a GaAs n+/p diode with no TDs using 4 different diode models.

4.4 Conclusions

The basic material parameters and equations governing both dark and light current components were presented. The influences of the lifetimes and depletion widths on current voltage curves were specifically addressed. Although, the calculation for the light current was presented, the light current will be considered a constant for the remainder of this thesis in order to isolate the impact of depletion region recombination

on the open-circuit voltage. Some particulars concerning the manner in which these I-V curves were numerically generated are included here for reference.

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CHAPTER 5

APPLICATIONS OF EXPERIMENTAL TECHNIQUES

A variety of experimental tools and techniques are used to investigate the material quality and minority carrier properties of lattice-mismatched materials systems and to correlate material characteristics with device performance. The major growth tool used is solid source molecular beam epitaxy (SSMBE); films are grown for material quality optimization, dopant incorporation calibrations, compositional calibrations, as well as test structures utilized in particular measurements and device structures such as diodes and photovoltaic cells. However, for some applications and studies a metal-organic vapor deposition (MOCVD) growth tool was used as well. A variety of experimental techniques that provide information on both structural and optical quality as well as dopant concentration and transport characteristics are used, these include X-ray diffraction, photo-luminescence, Hall effect, capacitance-voltage profiling, and secondary ion mass spectroscopy (SIMS). Transmission electron microscopy and scanning electron microscopy, and wet etching techniques are used to extract the threading dislocation density in materials layers; these results are then correlated with the minority carrier lifetimes measured by time-resolved photoluminescence as well as with device

performance characteristics. Some of the primary experimental techniques utilized are described below as well as a brief description of their application to this research project.

5.1 Growth by solid source molecular beam epitaxy

A modified Varian Gen II solid source molecular beam epitaxy (SSMBE) system at The Ohio State University is used for III-V semiconductor growth. MBE is a growth technique that uses an ultra high vacuum (UHV) environment and high purity elemental source material to produce high quality layers with low impurity concentrations and atomic precision.[1, 2, 3] This particular system is equipped with Group III sources: Ga, In, and Al, Group V sources: As and P, and dopant sources: Si and Be. Major growth parameters that influence epitaxial film material quality are the flux of the individual elemental sources, the growth rate, and the substrate temperature. These optimized growth parameters may differ for each compound; for example, GaAs is nominally grown at ~600°C where as $In_{0.53}Ga_{0.47}As$ is nominally grown at ~500°C. Since the P source has only been used at Ohio State University (OSU) for 3 years, the basic growth parameter space for the phosphide compounds of interest are still under development and require further optimization. Currently, the InGaP and AlGaInP alloys used in this thesis are grown at 490°C. At these growth temperatures, it is assumed that all Group III atoms incident on the surface will stick and thus the Group III alloy composition can be determined by knowing the flux of atoms from each Group III source. More information on SSMBE and the exact methods used to control Group III alloy compositions and growth rates are presented in Appendix A. It should be noted that a unique feature of the SSMBE used in these experiments is the ability to deposit epitaxial Ge; the Ge source is

used during growth initiation of GaAs on Ge or SiGe substrates. The use of the epitaxial Ge source is described in more detail in Appendix B.

5.2 Growth by metal-organic chemical vapor deposition

Unlike SSMBE, which uses elemental sources, metal-organic chemical vapor deposition (MOCVD) uses alkalis of Group III elements and Group V hydrides.[4,5] These gases are carried by an H_2 carrier gas to the substrate surface where the reactants are adsorbed on the surface and react to form the III-V compounds while the by-products are desorbed. All MOCVD samples were grown through a collaboration with NASA Glenn Research Center; the horizontal geometry low-pressure MOCVD reactor used for growth accommodates a single 2" wafer, maintains a pressure of 190 torr, and uses RF heating with a thermocouple placed below the susceptor. This particular system is equipped with high-purtiy precursor materials trimethylindium (TMIn), trimethylgallium (TMGa), diethylzinc (DEZn), arsine (100% AsH_3), phosphine (100% PH_3) and silane (100 ppm in H_2). Major growth parameters that influence epitaxial film material quality are the flow of the individual gases and the substrate temperature. The GaAs and InGaP layers (the only MOCVD grown III-V compounds used in this work) were grown at a substrate temperature of 620°C, a growth rate ~ 2μm/hr, and a V/III ratio of 100. Like SSMBE the doping concentrations were calibrated by electrochemical capacitance voltage measurements as well as Hall effect measurements and the InGaP composition calibrations used X-ray diffraction measurements.

5.3 Alloy composition and material quality

X-ray diffraction (XRD) techniques are used to measure the spacing between crystalline planes. Using the single crystal substrate with a known lattice constant and orientation (nominally {100}) as a reference, the interplanar spacing of an epitaxial layer's crystalline planes can be determined and the perpendicular and in-plane lattice parameters can be extracted. Typical XRD analysis uses the measured interplanar spacing of {004} planes and either {224} planes or {115} planes.[6,7] The composition of a ternary alloy film can be determined from these extracted lattice parameters since there is a unique relaxed lattice parameter for each alloy composition. Since this project is focused on lattice-mismatched material systems, it is important to examine both the perpendicular and in-plane lattice parameters since epitaxial layers will be relaxed to some degree; without assessing the degree of relaxation the alloy composition cannot be determined. Note that the composition of a quaternary alloy cannot be determined from X-ray alone since another independent variable is required. A complete description on the use of x-ray diffraction to determine ternary alloy compositions is provided in Appendix C. X-ray diffraction also gives a quantitative measure of material quality by measuring the full width at half maximum (FWHM) of diffraction peaks; this analysis is used in growth parameter optimization by comparing the FWHM of films grown under varying conditions.

Room temperature photoluminescence (PL) can also be used to determine the composition of a ternary alloy by measuring the bandgap of the epitaxial material. By continuously generating electron/hole pairs using a laser with photon energies greater than the material bandgap of interest, photons produced during radiative recombination of

these carriers can be measured as a function of photon wavelength/energy. The resulting spectrum indicates the characteristic energies associated with the radiative recombination processes, from which the material bandgap and optical defects can be identified.[8] The relative quality of a material versus growth conditions can also be analyzed using PL by considering the peak intensity and the peak FWHM of the band-band recombination peak as well as by considering the intensity of any peaks associated with defects. The determination of epitaxial layer bandgap by PL is essential when determining the composition of a quaternary alloy such as $In_{1-x-y}Ga_xAl_yP$ since it provides the extra independent variable needed for analysis.

5.4 Carrier concentration

Carrier concentrations for III-V epitaxial films are determined by van der Pauw Hall effect and capacitance-voltage (CV) measurements.[9,10] Using this data, the carrier concentration versus dopant source temperature or dopant gas flow are determined for a given material growth rate. The carrier concentration calibration curves are determined for each compound and can be appropriately scaled for other growth rates, thus allowing accurate doping concentrations in the growth of device structures. Hall effect measurements require growth on a semi-insulating substrate so that current conduction in other layers is minimized. Ohmic contacts to the layer of interest allow currents to be passed and voltages to be measured. By passing current through and measuring voltages across the appropriate contacts (with and with out a magnetic field present) the carrier type, the carrier concentration, and the carrier Hall mobility of the

conductive layer can be determined. Thus, Hall effect is also used in growth optimization to correlate mobility and dopant concentration with growth conditions.

CV curves measure the carrier concentration by correlating the change in capacitance with the change in depletion layer thickness and thus the carrier concentration of the material being depleted. CV measurements require a one side abrupt p-n junction or an Schottky junction for extraction of carrier concentration. Since this usually requires a processed device and does not measure carrier mobility, this technique is mostly used to confirm the carrier concentration in devices that have already been grown and processed, such as solar cells and diodes. A CV measurement can also be made by forming a Schottky contact with an electrolyte to the surface of an unprocessed material and quasi-ohmic contacts using indium-gallium eutectic and a metal probe. Electrochemical capacitance voltage (ECV) profiling can also be used to determine the carrier concentration as a function of layer depth; this is achieved by using an electrolyte that etches the semiconductor layer with applied bias or with applied bias and illumination. The advantages of this technique are that multiple doping concentration levels can be determined from a single sample by using a stepped doping profile, no device processing is required, and it can be performed on samples with conducting or non-conducting substrates. For this reason it is often used to generate doping calibration curves.

Secondary ion mass spectroscopy (SIMS) can be used to determine the total concentration of dopant atoms incorporated into the film. Since this is a physical sputtering technique it can be used on any sample; however, the proper standards are needed to determine accurate concentrations. Moreover, the ionization yields of the

sputtered atoms from different ion sources (typically Cs^+ and O_2^+) vary and so the appropriate sputtering ion must be selected to measure the particular secondary ion of interest.[11] For example, to measure Si concentrations an O_2^+ ion should be used, where as, a Cs^+ ion should be used when measuring Be concentrations. Since SIMS has a physical sputtering component, it too can be used to profile impurity concentration through a sample. By comparing these results with Hall or CV measurements, one can determine whether the dopant atoms have been incorporated at inactive interstitial locations with the crystal. SIMS is also used to identify impurities such as oxygen that might be compensating dopant atoms or to characterize the diffusion of elements in device structures or at hetero-junction interfaces. The SIMS data presented in this thesis were performed by Evans Analytic Group, Applied Microanalysis Labs, Inc., and the National Renewable Energy Laboratory.

5.5 Threading dislocation density

The evaluation of the TDD is essential to the project goals; it allows the correlation between material properties and cell performance characteristics with theoretical models. Currently three methods of measuring the TDD of a substrate or epitaxial layer are employed in this project; they are an electron induced beam current (EBIC) measurement performed with a scanning electron microscope (SEM) [12], cross-sectional transmission electron microscopy (XTEM), and etch pit density (EPD) measurements [13]. There are limitations in each of these methods that make them complementary techniques. The use of XTEM for dislocation assessment is a destructive and time-consuming process. Statistically, this method can be used to determine TDD

greater than $1x10^7$ cm^{-2}; thus, it provides an upper bound for samples with lower TDDs. Measurement of TDD via EPD is a destructive technique in which preferential etching at threading dislocations leaves pits where TD are present; this etching creates features that can be imaged using an optical microscope or an SEM. Overlapping etch pits, that may occur at dislocation pile-ups or in samples with uniform high TDDs, can reduce the measured TDD since the TDs cannot be counted individually. Therefore, EPD results are usually considered a lower bound. EBIC measurements use the electron beam of a SEM to generate electron-hole (e-h) pairs in a p-n junction or Schottky junction device. The carriers diffuse to the depletion region where the built in voltage of the depletion region separates the e-h pairs; carriers that reach the depletion region and cross the junction are collected by the external circuit thus creating a current. A decrease in the collected current indicates spatially localized recombination that might occur at a dislocation. Although EBIC is often the preferred measurement technique since it is non-destructive and indicates the electrical activity of defects, it is also a lower estimate of TDD when dislocation pile-ups cannot be resolved or when threading dislocations are rendered electrically inactive due to passivation or other phenomena.

5.6 Minority carrier lifetime

The minority carrier lifetime is an important material parameter that is used to characterize the material quality of epitaxial films. Low lifetimes can result from impurities as well as material defects such as anti-phase domains or threading dislocations. Time resolved photoluminescence (TRPL) is considered the most accurate method for measuring minority carrier lifetimes.[14,15] Unlike conventional PL

experiments, only the wavelength corresponding to the band-band transition of the material is typically monitored. By monitoring the emitted photon intensity as a function of time after the exciting laser pulse is terminated, the time constant associated with the return of the semiconductor material to equilibrium can be quantified. The particular system used in this research, courtesy of the National Renewable Energy Laboratory, uses a single photon counting technique where the incident light signal is pulsed and the time to the first emitted photon detection is recorded.[16] The decay curve generated is formed by multiple measurements and the statics of recombination. A double heterostructure is used in these measurements to confine the carriers to the material of interest as well as to define uniform boundary conditions at both the front and back interfaces. Since the well layer is typically doped with a distinct polarity, for example n $\sim 2x10^{17}$ cm^{-3}, the recombination rate measured will reflect that of the rate limiting carrier concentration, which in this example, corresponds to the minority carrier holes. With a few assumptions, the decay time constant, τ_{TRPL} can be related to the bulk minority carrier lifetime, τ_{bulk}, and the surface recombination velocity, S. By growing samples of varying layer thickness under the same growth conditions, both τ_{bulk} and S can be determined.

5.7 Device processing

The basic steps involved in processing a III-V based solar cell are described below; however, a detailed description is found in Appendix D. First, an e-beam evaporator is used to deposit the large area back contact. Photolithography is used to remove photo-resist (PR) from cell finger and front contact pad areas. The front contact is then initiated with an e-beam evaporator after which a thick gold layer is deposited in a

thermal evaporator. Since this is a relatively thick contact, the PR thickness must be in excess of the metal deposition thickness so that the metal that has been deposited on areas with PR can "lift-off" when the PR is removed. Next, photolithography is used to define the solar cell device area so that the junction can be isolated via a mesa etch. Finally, since the MgF_2/ZnS anti-reflection coating deposited in a thermal evaporator is insulating, photolithography is used to pattern PR so that the front contact pad is covered with PR; the ARC deposited on this pad can then be lifted off by PR removal. Just before deposition of the ARC, the entire sample is etched to remove the thin highly doped contact layer. After this, solar cells are ready for measurements and characterization. Optimization of ohmic contacts, surface passivation, and ARC design are processing parameters that can have a significant effect on device performance; therefore, careful analysis of device performance at various points in processing is completed in order to diagnose any non-idealities that may have occurred in processing.

5.8 Solar cell performance

Both dark and light current-voltage measurements, DIV and LIV respectively, are performed on processed solar cells. By considering the DIV performance, the reverse saturation current density, J_o, and the diode ideality factor, n, can be determined. This allows the comparison of J_o values with those predicted by models for substrates with varying TDD. LIV measurements are performed with an AM0 calibrated solar simulator (courtesy of NASA Glenn Research Center (GRC)) and an AM1.5 calibrated solar simulator (courtesy of the National Renewable Energy Lab (NREL)), thus V_{oc}, J_{sc}, FF, P_m, and η of a cell for space and terrestrial applications are determined. Solar

concentrator measurements, up to 100 suns, under AM1.5 illumination were also performed (courtesy of NREL). Using a Xenon ARC bulb, LIV measurements are performed at OSU to obtain a qualitative measure of AM0 or AM1.5 performance; this is done by calibrating the light intensity of the bulb to achieve the J_{sc} value of a reference cells measured with a calibrated sources. In this manner, individual cell quality can be checked prior to further characterization.

The external quantum efficiency for a solar cell describes the incident photon to collected electron conversion efficiency as a function of photon wavelength. Using a known incident photon flux at a given wavelength, the short circuit current measures the number of collected electrons. EQE measurements are an effective diagnostic tool since they can indicate problems in material quality and cell design. In order to achieve accurate quantitative results, the entire cell should be uniformly illuminated and the photon flux should be accurately known. There are two basics types of EQE measurement configurations; in one case, a white light source is filtered with notch filters where as another method uses a monochromator to achieve monochromatic light. The EQE measurements performed at NASA GRC and NREL use the filter wheel design. The EQE measurement at OSU uses a monochromator and thus does not have a uniform beam; therefore, a focused spot measurement is used where the area of the spot and the incident power are known from which the photon flux is calculated. In this configuration, the beam illuminates areas with varying front contact metal coverage and thus the extracted EQE values must be normalized. Recently, a more diffuse beam was used with a small area reference and test cells (< 0.36 cm^2). It was found that by maintaining the same cell positioning for reference and test cells, variations in the beam

non-uniformities were minimized and EQE measurements consistent with filter wheel results were produced.

Since unintentional Ge junctions can be formed during III-V epitaxy on Ge and SiGe, a photo-voltage measurement technique was developed to test for Ge activity. By appropriately filtering the light from the quartz lamp used in solar simulator such that there is photon absorption in a potential Ge cell but no photon absorption in a III-V cell, any potential voltage that forms across the device in an open-circuit measurement results from an active Ge cell. This technique essentially measures the open-circuit voltage of the Ge cell. This is very significant since EQE measurements of Ge junctions in series with other cells requires advanced light-biased EQE measurement tool that are not currently available at OSU. Moreover, for non-optimized Ge junctions, the Ge sub-cell may breakdown when reverse voltages are applied in an attempt to zero bias the Ge junction. A zero bias across the Ge junction is required since the EQE is a short circuit measurement.

5.9 References

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CHAPTER 6

MINORITY CARRIER PROPERTIES OF GaAs GROWN ON SiGe

The ability to produce high quality GaAs on Si substrates is desirable for many reasons including the low cost, high mechanical strength, and large area of Si substrates as well as the possibility of integrating III-V opto-electronics with Si VLSI circuitry. To this end, the minority carrier hole lifetime in GaAs grown on Si-based substrates has been studied over the last 15 years to assess the quality of these metamorphic un-doped or n-type GaAs layers. A large variation in lifetime has been measured stemming from the epitaxial hurdles present in the GaAs/Si material system, namely a 4% lattice-mismatch and a polar/non-polar interface. However, before this thesis, the minority carrier electron lifetime for p-type GaAs grown on a Si-based substrate had not been measured.[1]

Understanding the impact of TDs on both electron and hole minority carrier lifetime is critical to device modeling and device design and therefore is the subject of this chapter. In Section 6.1 a detailed description concerning the use of time-resolved photoluminescence (TRPL) for measuring the lifetime in homoepitaxial GaAs double heterostructures (DHs) is described. Also the minority carrier mobility and diffusion coefficients are discussed since they play an important role in modeling the impact of

TDs on minority carrier lifetime. This review provides a baseline for GaAs material quality in the absence of large densities of TDs. In Section 6.2, the proposed model for minority carrier lifetime (τ) as a function of threading dislocation density (TDD) is presented. Previous work concerning the hole lifetime (τ_p) in metamorphic GaAs DHs grown on Si-based substrates is reviewed to show the application of this model; this data will then be compared to electron lifetime (τ_n) data presented in the next section. Finally, Section 6.3 describes the experimental study that was completed to measure the electron lifetimes for GaAs DHs on SiGe substrates. Since this represents original work provided by this thesis, the growth, measurement, and analysis details are provided. The measured lifetimes for GaAs/GaAs and GaAs/SiGe for p-type GaAs double heterostructures (DHs) and the expected dependence of these lifetimes on TDD are presented. Collectively, the data presented in this chapter shows the validity of the described models for both n-type and p-type GaAs with a dopant concentration of approximately 1 - 2x10^{17} cm^{-3}.

6.1 GaAs minority carrier lifetime and mobility

The minority carrier lifetime of holes and electrons in GaAs has been extensively studied. In some cases TRPL measurements have been completed on DHs of various thicknesses (d) in order to examine the surface recombination velocity (S) of the hetero-junction interfaces and extract bulk lifetimes (τ) based on Equation 6.1.[2] With advances in the quality of epitaxial GaAs layers, the measured minority carrier lifetimes have reached the theoretical limits for band-band/radiative recombination given by Equation 6.2, where N is the dopant concentration (cm^{-3}) and B is the band-band radiative

recombination coefficient (cm^3s^{-1}). Theoretical calculations based on the GaAs band structure suggest a *B* value of 1-2 $x10^{-10}$ $cm^{-3}s^{-1}$.[3, 4]

$$\frac{1}{\tau_{PL}} = \frac{1}{\tau} + \frac{2S}{d} \qquad \text{Equation 6.1}$$

$$\tau_R = (BN)^{-1} \qquad \text{Equation 6.2}$$

Figure 6.1 a and b show the dependence of lifetime (the measured TRPL decay constant, τ_{PL}) on dopant concentration for n-type and p-type GaAs, respectively. [5, 6] In each case, the values equal and more often exceed the theoretically expected values based on B = $2x10^{-10}$ $cm^{-3}s^{-1}$. In Figure 6.1a, the data points at each doping concentration represent τ_{PL} for n-type GaAs DHs with *d* values from 0.25 μm to 10 μm; the largest measured τ_{PL} corresponds to the thickest active layer, in this case *d*=10 μm. Figure 6.1b, shows compiled data for p-type GaAs DHs from various sources, the variation in lifetime is indicative of variations in material quality, DH active layer thickness, doping calibration methods, and TRPL measurement technique. In this figure, the two lines indicate *B* values of $1x10^{-10}$ $cm^{-3}s^{-1}$ and $2x10^{-10}$ $cm^{-3}s^{-1}$. Based on these values, a doping concentration of $2x10^{17}$ cm^{-3} is should have a theoretically expected lifetime is 25-50 ns.

The lifetime values in Figure 6.1a are in excess of the expected values, a phenomena which results from photon recycling. Photon recycling is described by the self-absorption and the subsequent reemission of the photons. When photon recycling

occurs, the decay time measured by TRPL is indicative of the time for multiple carrier recombination events and thus an apparently higher lifetime is measured. Since this phenomenon is non-linear with *d*, a linear fit to Equation 6.1 is not obtained. Figure 6.2a shows this effect; note, curve I assumes no photon recycling while curve II shows the experimentally measured results which include photon recycling. Work by Ahrenkiel et. al. found that for high quality GaAs the photon recycling could be accounted for using Equation 6.3. In this equation, τ_{nR} represents all contribution to lifetime that are non-radiative. With the photon recycling factor, ϕ, given in Figure 6.2b.[2] However, it was found that ϕ depends on active layer doping, the index of refraction of the DHs barrier layers, and the substrate thickness, doping, and bandgap. Therefore the values of ϕ shown in Figure 6.2b cannot be generally applied.

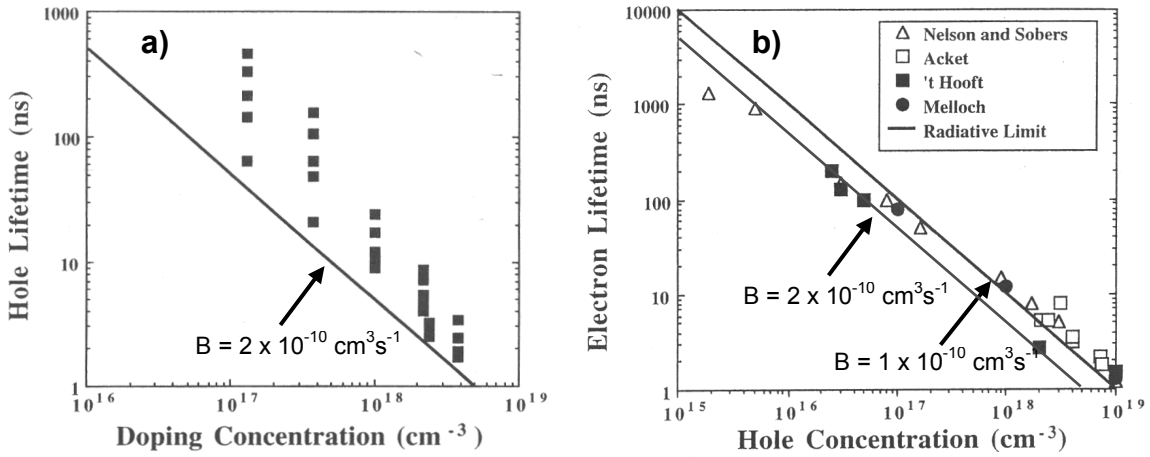

Figure 6.1: a) The TRPL decay time constant (τ_{PL}) for n-type GaAs DHs grown by MOCVD for active layers thicknesses from 0.25 μm to 10 μm. [after Ref. 5] b) The TRPL decay time constant (τ_{PL}) for p-type GaAs DHs grown by various techniques. [after Ref. 6]

$$\frac{1}{\tau_{PL}} = \frac{1}{\tau_{nR}} + \frac{1}{\phi(d)\tau_R} + \frac{2S}{d} \qquad \text{Equation 6.3}$$

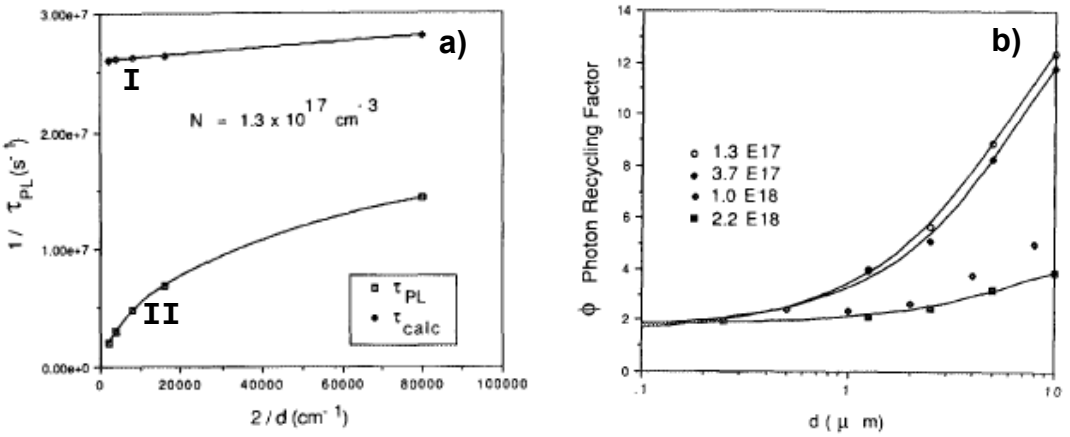

Figure 6.2: a) Curve II shows the PL decay times with photon recycling present; this curve is not linear. Curve I shows the decay times calculated by Equation 6.1 given the same bulk lifetime and surface recombination velocity extracted from Curve II, but with no photon recycling. [after Ref. 2] b) The measured values of ϕ for various n-type GaAs dopant concentrations. [after Ref. 2]

The general result of these TRPL and photon recycling studies indicated that a B value of $2\text{x}10^{-10}$ $\text{cm}^{-3}\text{s}^{-1}$ can be used both p-type and n-type GaAs. The value of $\phi \sim 1.95$ for active layer thicknesses (d) below ~ 1.0 μm may be employed in most cases. Therefore, by using thinner DHs this non-linearity due to changes in ϕ with d can be minimized and S and τ can be more easily extracted. Finally, the need to account for photon recycling depends on each sample set and this discussion clearly demonstrates the

apparent ambiguity in B values between 1-2x10^{-10} $cm^{-3}s^{-1}$ and experimental data presented.

The minority carrier lifetime, τ, and the minority carrier diffusion length, L, are related by the minority carrier diffusivity or diffusion coefficient, D, as shown in Equation 6.4. The minority carrier diffusion coefficient, D, which is indicative of the rate of carrier motion resulting from a carrier concentration gradient can be related to the minority carrier mobility, μ, using the Einstein Relation shown in Equation 6.5.

$$L = (D\tau)^{1/2} \qquad \text{Equation 6.4}$$

$$\frac{D}{\mu} = \frac{kT}{q} \qquad \text{Equation 6.5}$$

Knowing the minority carrier mobility or diffusion coefficient for a material is important since it is a principal factor in understanding the impact of TDD on lifetime as well as device performance. This is a difficult measurement and very little data is available; however, there have been some measurements on n-type and p-type GaAs, as shown in Figure 6.3. For electrons it has been found that the minority carrier mobility is lower than the majority carrier mobility for the same carrier concentrations, this was theoretically expected due to heavy hole scattering in the p-type GaAs. At a doping of 2x10^{17} cm^{-3}, the majority carrier mobility is 4000-3500 $cm^2V^{-1}s^{-1}$ depending on the carrier compensation ratios, where as, the minority carrier mobility is ~ 3000 $cm^2V^{-1}s^{-1}$. For holes, the theory is not consistent with measured values, and in fact the values at

dopant concentrations less than $1x10^{18}$ cm^{-3} do not deviate significantly from majority carrier mobilities. As noted above, the mobility is related by the Einstein relation, and a fit to the minority carrier diffusion coefficient is shown in Figure 6.3c. It should be noted that there is approximately a factor ten difference in the electron and hole mobilities and thus in the electron and hole diffusion coefficients.

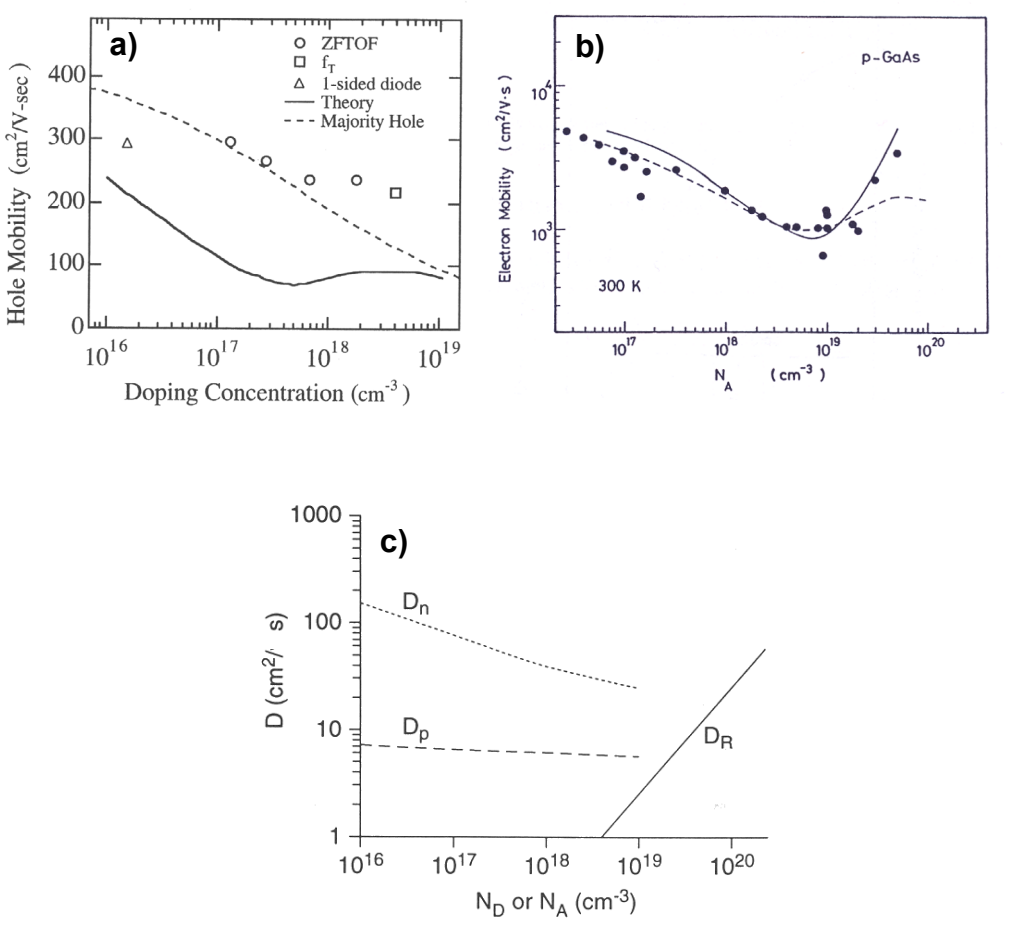

Figure 6.3 a) The mobility of majority and minority carrier holes in GaAs as a function of doping concentration. [after Ref. 7] b) The mobility of minority carrier electrons as a function of doping concentration. [after Ref. 8] c) The expected minority carrier diffusion coefficients for electron and holes in GaAs as a function of doping concentration as suggested by Ref. 9.

6.2 Threading dislocation density and minority carrier properties

As discussed, threading dislocations (TDs) are introduced in lattice-mismatched epitaxy. Since these defects can extend throughout the epitaxial layer, they can have a significant impact on the bulk material properties, specifically minority carrier properties such as minority carrier diffusion length and minority carrier lifetime. There is limited data concerning minority carrier properties of III-V semiconductor compounds as a function of TDD since they are highly dependent on the growth technique, the overall material quality, as well as the doping concentration. A fairly well characterized material is metamorphic n-type GaAs grown on Si substrates.

The work by Yamaguchi et al. calculated a dislocation-limited diffusion length [10], and the basic premise behind this model is outlined here. In order for minority carriers to recombine at a dislocation they must first diffuse to a dislocation. The diffusion of minority carrier is described by the diffusion equation, Equation 6.6. We assume that a single dislocation has an occupation volume given by Equation 6.7.

$$\frac{\delta n}{\delta t} = D\frac{\delta^2 n}{\delta^2 x} \qquad \text{Equation 6.6}$$

$$\pi x_c^2 = \frac{1}{[TDD]} \qquad \text{Equation 6.7}$$

Then by assuming that the carrier concentration is zero at the dislocation core, that there is no spatial concentration gradient a distance x_c away from the dislocation core, and that the excess carrier concentration, n_o, exists at x_c for all time, the differential equation can

be solved using separation of variable. We find that the excess minority carrier concentration is described by Equation 6.8, with a characteristic dislocation mediated diffusion length of L_{TDD} and a dislocation mediated recombination lifetime of τ_{TDD}. Note that L_{TDD} is independent of material specific parameters, where as, τ_{TDD} is a material and doping dependent parameter through D.

$$n(x,t) = n_o \sin(x / L_{TDD}) e^{-t/\tau_{TDD}} \qquad \text{Equation 6.8}$$

$$L_{TDD} = \frac{2x_c}{\pi} = \frac{2}{\pi^{3/2}[TDD]^{1/2}} \qquad \text{Equation 6.9}$$

$$\tau_{TDD} = \frac{L_{TDD}^2}{D} = \frac{4}{\pi^3 D[TDD]} \qquad \text{Equation 6.10}$$

Since these are characteristic values, we can express the total diffusion length and lifetime as shown in Equation 6.11 and Equation 6.12. In these equations, L_{max} and τ_{max} represent the maximum lifetime in a particular semiconductor material at a given doping concentration from all other contribution (Shockley-Read-Hall, Auger, band-band, etc.) in the absence of TDs.

$$\frac{1}{L^2} = \frac{1}{L_{\max}^2} + \frac{1}{L_{TDD}^2} \qquad \text{Equation 6.11}$$

$$\frac{1}{\tau} = \frac{1}{\tau_{\max}} + \frac{1}{\tau_{\mathrm{TDD}}} \qquad \text{Equation 6.12}$$

Based on this model, a decrease in τ is expected with increasing TDD. The minority carrier lifetimes achieved for GaAs double heterostructures (DHs) grown on Si substrates via direct epitaxy using III-V strained-layer superlattices as interlayers have been reported to be up to 2 ns in n-type GaAs.[11, 12, 13, 14, 15] These lifetimes are believed to be defect-limited due to the high residual TDDs (> $7x10^6$ cm^{-2}) and the fact that these lifetimes are much lower than homoepitaxial lifetimes (τ_{max}) achieved at the same dopant concentrations (~ 20-100 ns).[11,12,13,14,15] Other attempts to reduce the TDD and thus increase τ_p have utilized thick Ge layers [16] or $Si_{0.04}Ge_{0.96}$ layers [17] resulting in reported lifetimes of 3 ns and 2.5 ns, respectively. More recent work done in our research group at The Ohio State University, has shown that an interlayer consisting of compositionally graded $Si_{1-x}Ge_x$ up to 100% Ge results in TDDs in GaAs on Si of ~$1x10^6$ cm^2, which translates to minority carrier hole lifetimes of up to 10 ns.[18, 19] Figure 6.4 shows a plot of minority carrier hole lifetimes versus TDD for n-type GaAs. In this figure, the modeled data assuming D = 7.1 cm^2s^{-1} (for $2x10^{17}$ cm^{-3} from Ref. 2) and a τ_{max} of 20 ns (from Ref. 12) is plotted with experimental results from three different research groups. The doping densities for these DHs are ~$1x10^{17}$ cm^{-3} for Ref. 12, 18, and 19 and ~ 0.6 $x10^{17}$ cm^{-3} for Ref.11. It should be noted that all earlier reports were for a single DH decay times (τ_{PL}) where as data from Ref. 18 and 19 and τ are values extracted from the linear relationship in Equation 6.1 using the values of τ_{PL} measured for three DHs with varying active layer thicknesses (d). Also, none of this data accounts for

photon recycling. This is because the TDD dominated lifetimes do not support photon recycling and the use of lower bandgap substrates such as Ge and Si which do not reemit photons capable of exciting carriers in the GaAs DH were used. Radiative recombination must be the dominant mechanism to see appreciable photon recycling, as shown by Equation 6.3.

From this figure we see that the trend suggested by this model fits the data for a particular DHs doping. Also plotted in this figure is the modeled result for a D value 2 cm^2s^{-1}, which implies a hole mobility of only 77 $cm^2V^{-1}s^{-1}$. This was the suggested fit to the data from Ref. 11, who indicted that the mobility could be impacted by the TDD in this TDD regime. There have been a few reports suggesting that the majority carrier electron mobility was impacted little by TDs until a TDD of $1x10^8$ cm^{-2}.[20] There have been no reports concerning the impact of TDD on minority carrier mobility in GaAs. This analysis brings to point another ramification of this model, the independence of the lifetime on τ_{max} once dominated by τ_{TDD} and the suggestion that an increase in D (by a decrease in doping) will decrease τ in the TDD dominated regime. From Section 6.1 we find that there is little change in D_p with doping concentration so this effect may not be appreciable. However, it is interesting to note that the data from Ref. 11 shows higher lifetimes for lower dopant concentrations ($0.6x10^{17}$ cm^{-2}) which is counter to the expected result. This may be an indication of a change in defect-carrier interactions that may depend on the Fermi level, and thus a break down in the assumption used in this simple model or defect passivation.

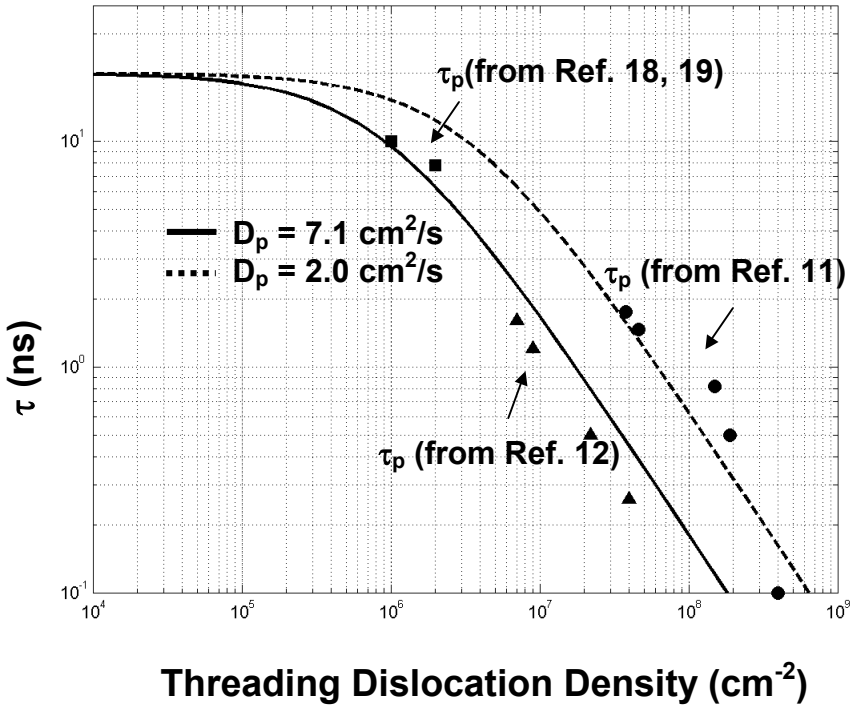

Figure 6.4: Theoretical dependence of minority carrier lifetime on threading dislocation density. Experimental values represent data from Ref. 11, 12, 18, and 19 for n-type GaAs DHs grown on Si.

6.3 P-type GaAs DHs grown on SiGe

6.3.1 DH growth

In order to understand the impact of TDD on electron lifetimes, p-type GaAs DHs were grown on a GaAs substrate, and two SiGe substrates with varying TDDs. Three thicknesses were grown so that *S* could be determined and τ_{max} extracted. The growth structure and growth process are described in this section.

Compositionally graded, p-type, relaxed SiGe layers grown on Si substrates were grown by both ultra-high vacuum [21] and low-pressure chemical vapor deposition [22]. In each case the Si substrates used were (100) oriented with a 6° off-cut toward the [110] direction and the compositional step grading has been completed at an average rate of 10% Ge / μm, terminating with a 100% Ge cap layer. By using (SiGe) substrates with and without a chemical mechanical polish (CMP), a set of SiGe substrates with different threading dislocation densities (TDDs) in the fully relaxed Ge cap layer were obtained for the purpose of this study. The TDDs were measured by counting etch pits in the Ge termination layer prior to III-V growth and the etch pit densities (EPDs) were determined to be ~ $1x10^6$ cm^{-2} with a CMP and ~ $4x10^6$ cm^{-2} without a CMP. These two substrates, as well as a GaAs substrate ((100) oriented with a 6° off-cut toward the [110]) with an EPD < $1x10^3$ cm^{-2} were used for DH growth.

GaAs growth on the Ge terminated surface of the SiGe substrates was initiated by using solid source molecular beam epitaxy (SSMBE) prior to DH growth by low pressure metal-organic chemical vapor deposition (LP-MOCVD). The GaAs growth initiation procedure followed the method described in Ref. 23, but without the application of a

time-consuming migration enhanced epitaxy (MEE) step that would eliminate all anti-phase domain (APD) disorder. However, we have shown that this modified nucleation process yields very high quality material, with all APD disorder confined to within ~ 50 nm of the GaAs/Ge interface, well beneath the DH structure, and minority carrier hole lifetimes for GaAs/SiGe in excess of 10 ns for n-type DH structures that is limited only by residual TDs.[19,23] In this manner, 0.1 μm GaAs initiation layers were grown on SiGe substrates, prior to transfer to an LP-MOCVD reactor for DH growth.

A series of $In_{0.49}Ga_{0.51}P$/GaAs/$In_{0.49}Ga_{0.51}P$ DH structures were then grown at 620°C; DHs of a given thickness were grown on the two GaAs-coated SiGe substrates with different dislocation densities and the GaAs control substrate, simultaneously. The DHs consisted of GaAs wells of varying thickness (0.5 μm, 1.0 μm, and 1.5 μm) with 50 nm $In_{0.49}Ga_{0.51}P$ barrier layers. The GaAs wells had a Zn dopant concentration of ~ $2x10^{17}$ cm^{-3} and the $In_{0.49}Ga_{0.51}P$ barrier layers had a Zn dopant concentration of ~ $5x10^{18}$ cm^{-3}, which were confirmed by secondary ion mass spectroscopy (SIMS) and electrochemical capacitance voltage profiling. The doping values were selected to be consistent with solar cells structures to be discussed in the next chapter. A 0.1 μm GaAs buffer was grown by MOCVD prior to DH growth, resulting in a total GaAs buffer layer thickness of 0.2 μm on the SiGe substrates. A representative cross-sectional transmission electron microscopy (XTEM) image of an $In_{0.49}Ga_{0.51}P$/GaAs/$In_{0.49}Ga_{0.51}P$ DH structure grown on a SiGe substrate having a TDD of ~ $4x10^{6}$ cm^{-2} is shown in Figure 6.5. No long-range APDs penetrating the DH structure are evident, which is consistent with our earlier n-type DH studies; therefore, only residual TDs are present in the DHs, as designed.

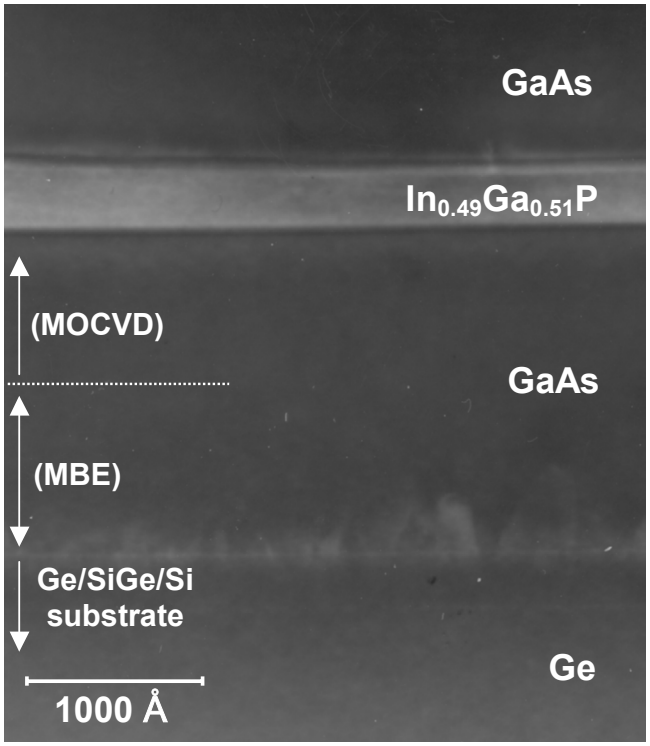

Figure 6.5 Cross-sectional transmission electron microscope images of 0.5 μm well $In_{0.49}Ga_{0.51}P/GaAs/In_{0.49}Ga_{0.51}P$ double heterostructures grown on a SiGe substrate with a TDD of $\sim 4x10^6$ cm^{-2}. A two-beam bright field condition using the (220) reflection was used to produce the XTEM image. Short-range, self-annihilating APDs are seen at the GaAs/Ge interface and are confined to within 50 nm of this interface; APDs do not extend into the DH. There is no evidence of defect formation at the regrowth interface.

6.3.2 DH lifetimes

Room temperature time-resolved photoluminescence (TRPL) using the time-correlated single-photon counting technique was used to measure the minority carrier electron lifetime, τ_n, in these DHs. A cavity-dumped dye laser synchronously pumped by a mode-locked Nd:YAG was used to create electron-hole pairs with in the well of the DHS. The resulting photoluminescence was focused onto the slits of a scanning monochromator set to ~870 nm (GaAs band-to-band transition peak) and detected with a micro-channel plate (MCP) detector. The injection level of photo-excited carriers within the sample was maintained below the equilibrium carrier concentration by attenuating the average incident laser power thus low-level injection conditions were maintained. This system can resolve decay rates as short as 0.020 ns.

Again, a double heterostructure is used in these measurements to confine the minority carrier to the active region as well as to define uniform boundary conditions at both the front and back interfaces. With a few assumptions, the decay time constant, τ_{PL} can be related to the bulk minority carrier lifetime, τ, and the surface recombination velocity, S, as shown in Equation 6.1. Figure 6.6 shows the TRPL decays, the measured τ_{PL} values, and the linear fit used to extract τ and S. Attempts to use the $\phi(d)$ values presented in Figure 6.2b produced non-physical results, therefore, a single phi value ($\phi \sim 1.95$) was used to correct this data for photon recycle as suggested in Ref. 2. This approximation is reasonable since the d values are small and the fit is fairly linear. If photon recycling were neglected the electron lifetime would be 38 ns which is greater than theoretically expected given a B value of 2×10^{-10} $cm^{-3}s^{-1}$. The relatively large surface recombination velocity, ~3500 cm^2/s, may result from the high doping in the

window layers. Other reports for low SRV values for the $In_{0.49}Ga_{0.51}P$/GaAs hetero-interface were for un-doped layers (~ 2 cm/s) or n-type layers (~ 196 cm^2/s).[24] In fact, n-type GaAs DHs used in this studying and grown in the manner had SRV values of ~500 cm^2/s; this difference in *S* may also result from lower conduction band offsets compared with valence band offsets or different interfacial defects due to the dopant species used.

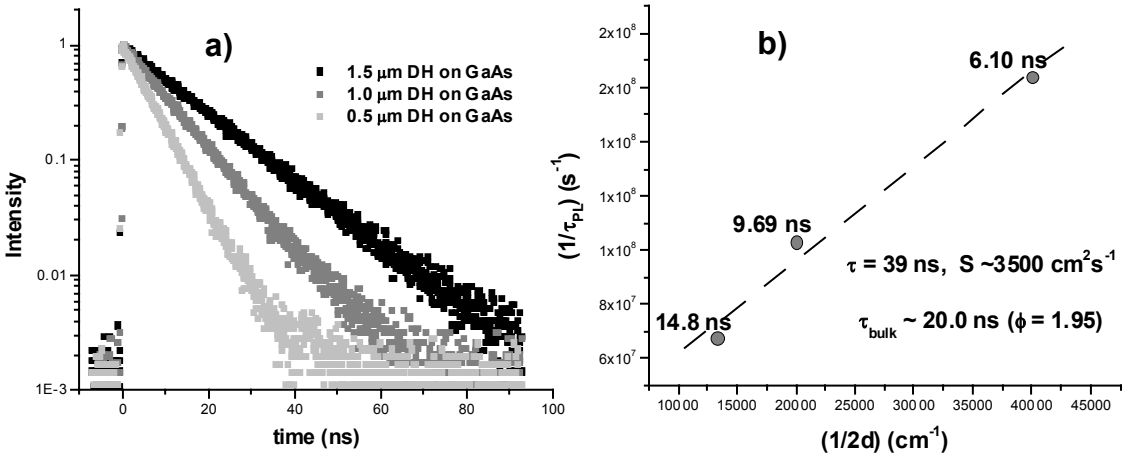

Figure 6.6 a) Decay for GaAs DHS of varying thickness. b) Extracted lifetime and surface recombination velocity for homoepitaxial DHs. Due to the linearity of the curve a uniform photon recycling factor was used.

The TRPL decays shown in Figure 6.7 were measured on the 0.5 μm DHs grown on all three substrates. Well-defined single-exponential transients were observed for all three samples. The influence of higher TDDs is evidenced by the faster decay for DHs on SiGe substrates (higher TDDs).

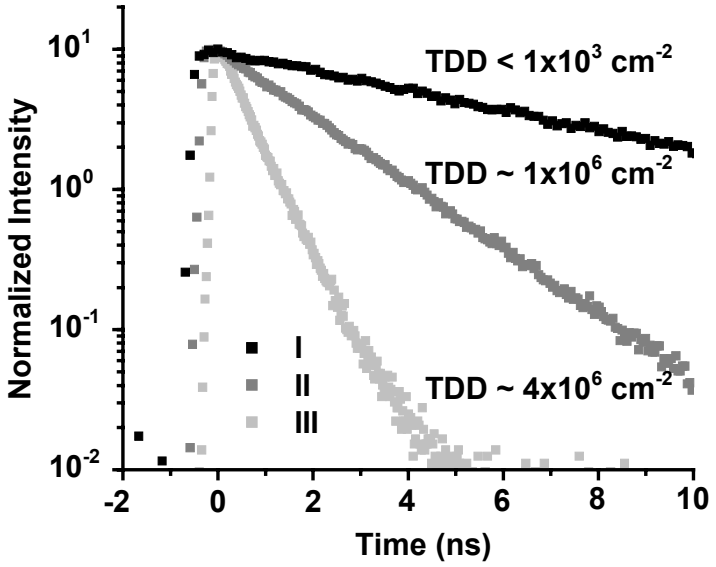

Figure 6.7 Room temperature time-resolved photoluminescence measurements for p-type $In_{0.49}Ga_{0.51}P$/GaAs/ $In_{0.49}Ga_{0.51}P$ double heterostructures (DHs) grown on I) GaAs II) SiGe with a CMP and III) SiGe without a CMP. This data was measured for DHs with a GaAs well thickness of 0.5 μm and a Zn dopant concentration of ~ $2x10^{17}$ cm^{-3}.

Photon recycling effects were not present in DHs grown on SiGe since the lifetimes were dominated by recombination at TDs. Moreover, there was little variation in decay times for different well thicknesses and no systematic trend, thus a SRV could not be extracted for DHs grown on SiGe. (For example, DHs with d = 1.0 μm had a shorter lifetime than that for d = 0.5μm.) This phenomenon results from the fact that the lifetimes were significantly shorter than those on GaAs substrates while good SRVs were maintained.[18] Figure 6.8 illustrates this effect. Plotted in the figure are the expected τ_{PL} values as a function of S from Equation 6.1 for given values of τ and d. One can see that a bulk lifetime of 0.6 ns are only sensitive to values of S in excess of ~10,000 where as for a bulk lifetime of 20 ns, changes are apparent at ~ 500 ns.

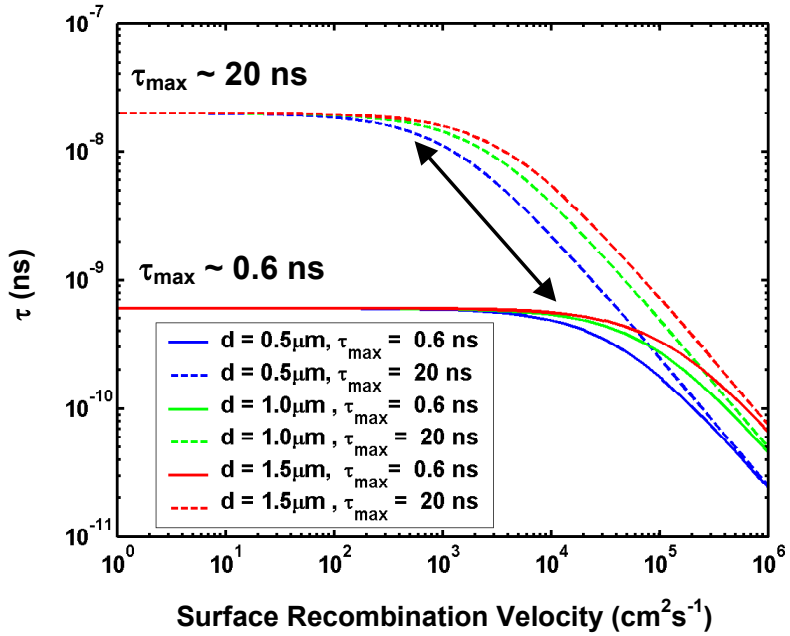

Figure 6.8 Measured lifetimes as a function of surface recombination velocity, *S*, for various well thicknesses (*d*) and initial bulk lifetimes.

The variation in the TRPL electron lifetimes extracted for each well thickness (0.5 μm, 1.0 μm, and 1.5 μm) for DHs grown on a given SiGe substrate were less than 20% and can be a consequence of minor variations in material quality resulting from localized inhomogeneities in TDD. The average of the TRPL electron lifetimes for these DHs are ~ 1.54 ns and ~ 0.53 ns for the SiGe substrates with a TDD of ~ $1x10^6$ cm^{-2} and TDD of ~ $4x10^6$ cm^{-2}, respectively. The average τ_n for p-type GaAs DHs grown on SiGe are plotted in Figure 6.9 along with values of τ_p in n-type GaAs DHs grown on SiGe substrates from Ref. 18 and Si substrates from Ref. 12. While the measured lifetimes for n-type and p-type homoepitaxial GaAs DHs have comparable values (22 ns and 20 ns,

respectively), GaAs DHs on Si demonstrate a substantial disparity between electron and hole minority carrier lifetimes. Theoretical calculations of τ_n and τ_p based on Equation 6.11, represented in Figure 6.9 by solid lines, support and generalize these differences. In the modeled results, the value of τ_{max} was chosen to be 20 ns for both electrons and holes in order to be consistent with other publications; this value is comparable with homoepitaxial GaAs results measured in this study and with the theoretically expected value for band-band recombination (25 ns) using a band-band coefficient of $2x10^{-10}$ cm^3/s and a dopant concentration of $2x10^{17}$ cm^{-3}. The minority carrier diffusion coefficients used in these calculations were $D_n \sim 78$ cm^2/s for electrons and $D_p \sim 7.1$ cm^2/s for holes, as measured for homoepitaxial GaAs at a doping concentration of $2x10^{17}$ cm^{-3}, and were kept constant as a function of TDD since TDDs in GaAs in excess of $1x10^8$ cm^{-2} are required to significantly impact the carrier mobility.

The lower lifetime of electrons, which has been revealed by both the experimental data and the modeled results, is understood by noting the difference in minority carrier diffusion coefficients (D) or equivalently the minority carrier mobilities (μ) for electrons and holes in GaAs. Since the τ_n and τ_p in the low TDD regime (less than $1x10^3$ cm^{-2}) are comparable, the higher mobility of electrons reduces the average time for carrier-dislocation interaction; i.e. τ_n is more sensitive to TDD than τ_p for GaAs, resulting in the observed shorter electron recombination lifetimes. In the context of the Equation 6.9, a factor of 11 increase in D_n compared to D_p results in an earlier dominance of the threading dislocation lifetime component (τ_{TDD}) for electrons compared to holes. Based on the modeled result, a TDD of $\sim 1x10^5$ cm^{-2} would be necessary to achieve a 10 ns electron lifetime in p-type GaAs compared with a TDD of $\sim 1x10^6$ cm^{-2} for holes in n-

type GaAs for a dopant concentration of $2x10^{17}$ cm^{-3}. This result is significant for GaAs devices grown on Si-based substrates since differences in minority carrier lifetimes can significantly impact device design and performance. Recent work on p^+/n and n^+/p GaAs solar cells grown on Si-based substrates have shown that n^+/p solar cells have lower open-circuit voltages at a given TDD due to the enhanced recombination of electrons compared to holes.[25] This subject is explored in the next Chapter.

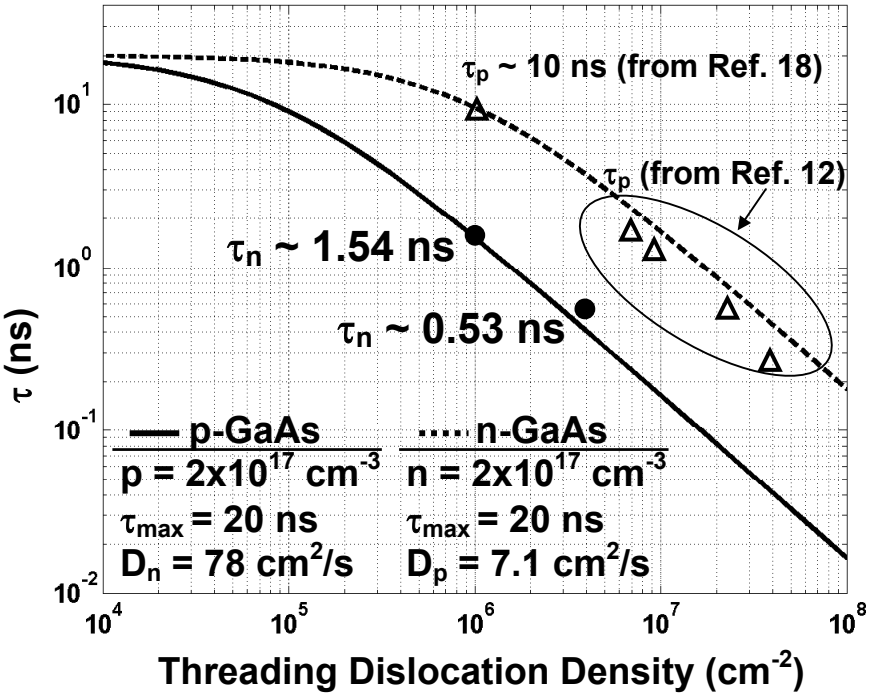

Figure 6.9 The minority carrier electron and hole lifetime as a function of threading dislocation density in GaAs. The solid lines represents the expected values based on Equation 6.12 and the parameters shown in the figure. The experimental data points for τ_n are those presented in this thesis and the experimental data points for τ_p are taken from Ref. 18 and Ref. 12.

Although not discussed in detail in this thesis, the minority carrier diffusion length is an important material parameter in GaAs/Si solar cell development, since it impacts the minority carrier collection and thus the J_{sc} achieved. Using Equation 6.11, the expected diffusion lengths, L_n and L_p, as a function of TDD were calculated use the same material parameters employed in Figure 6.9. Note that the diffusion lengths of holes, L_p, at a TDD of $1x10^6$ cm^{-2} is expected to be 2.5 μm where as the diffusion length of electrons, L_n, is 3.4 μm. Moreover, L_p and L_n converge in the limit of TDD dominated diffusion length, L_{TDD}.

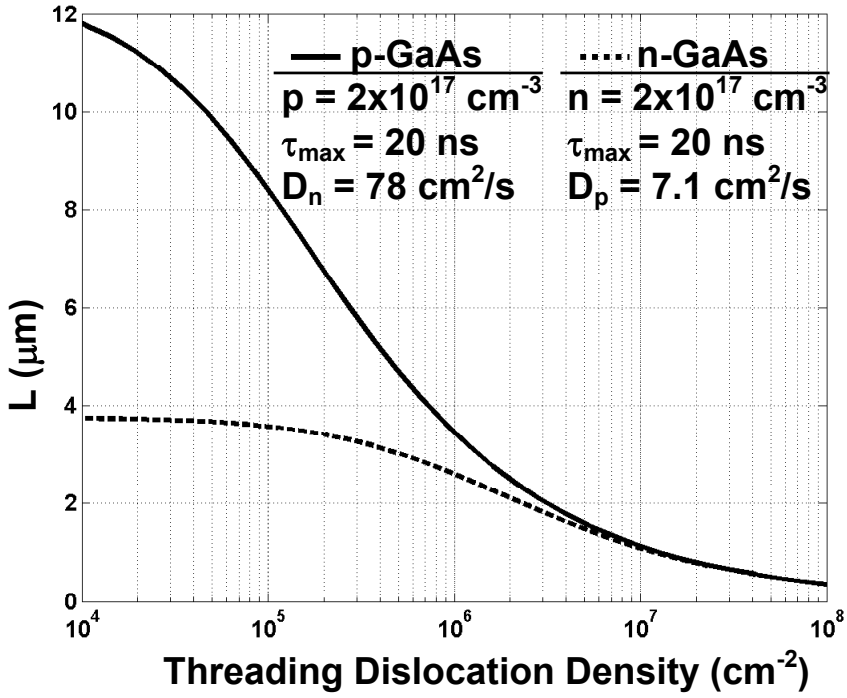

Figure 6.10 The minority carrier electron and hole diffusion lengths as a function of threading dislocation density in GaAs. The solid lines represents the expected values based on Equation 6.11 and the parameters shown in the figure.

6.4 Conclusions

The minority carrier lifetime of electrons, τ_n, in p-type GaAs double heterostructures (DHs) grown on GaAs substrates and compositionally graded $Ge/Si_{1-x}Ge_x/Si$ (SiGe) substrates with a varying threading dislocation density (TDD) were measured at room temperature using time-resolved photoluminescence. The electron lifetime for homoepitaxial GaAs and GaAs grown on SiGe (TDD ~ $1x10^6$ cm^{-2}) with a dopant concentration of $2x10^{17}$ cm^{-3} were ~ 20 ns and ~ 1.5 ns, respectively. The electron lifetime measured on SiGe was substantially lower than the previously measured minority carrier hole lifetime, τ_p, of ~ 10 ns, for n-type GaAs grown on SiGe substrates with a similar residual TDD and dopant concentration. The reduced lifetime for electrons is a consequence of their higher minority carrier mobility, which yields an increased sensitivity to the presence of dislocations in GaAs grown on metamorphic buffers. The disparity in dislocation sensitivity for minority carrier electron and hole recombination has significant implications for metamorphic GaAs devices that are described in the next Chapter.

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CHAPTER 7

GaAs SOLAR CELLS GROWN ON SiGe

Obtaining high minority carrier lifetimes is a critical step toward high performance GaAs devices on Si-based substrates. As shown in the previous chapter, there is a fundamental difference in the minority carrier lifetime of electrons and holes in GaAs with TDDs greater than $1x10^5$ cm^{-2}. The impact of this result on a diodes' reverse saturation current (J_o), a diodes' effective ideality factor (n), and on a solar cells' open circuit voltage (V_{oc}) and fill factor (FF) are explored in this chapter. In Section 7.1, the "standard" solar cell device structures for both n+/p and p+/n solar cells are presented. The TDD dependent lifetime/diffusion length model is incorporated into the "standard" diode/solar cell device models for dark and light current density versus voltage characteristic (DIV and LIV). Thus, the theoretical impact of TDD on the reverse saturation current components, J_{o1} and J_{o2}, V_{oc}, and FF is quantified. The experimental DIV curves for both n+/p and p+/n GaAs solar cells grown on GaAs and SiGe are examined in Section 7.2. These cells were grown, processed, and measured for the purposes of this thesis, in order to examine the validity of the proposed models for both n+/p and p+/n devices. Finally, in Section 7.3, experimental solar cell data is compared

to the modeled V_{oc}(TDD) curves. It is demonstrated that for a given TDD, a p+/n GaAs solar cell has a higher V_{oc} value than an n+/p GaAs solar cell; this is a direct result of the lower electron minority carrier lifetimes reported in Chapter 6.

7.1 Threading dislocation density and GaAs device models

In Chapter 4 the "standard" solar cell IV models were discussed in detail. These models depend on the thickness and dopant concentration of device layers as well as other material parameters. As shown in Chapter 6, the behavior of both the minority carrier lifetime and diffusion length as a function of TDD can be modeled with all other material parameters fixed. Thus, both τ(TDD) and L(TDD) are incorporated into the IV models. The GaAs single junction solar cell structures and the modeling input parameters used in this chapter are shown in Figure 7.1. Other GaAs material parameters used in this modeling are an intrinsic carrier concentration, n_i, of 2.1x10^6 cm^{-3}, a bandgap of 1.42 eV, and a relative dielectric constant of 12.9.

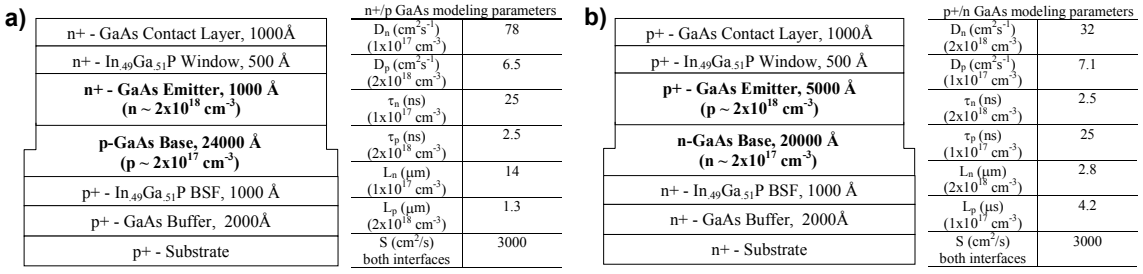


Figure 7.1 The solar cell device structures and material parameters for a) n+/p and b) p+/n GaAs solar cells used in this chapter.

To account for impact of TDs on a diodes' IV curve (described by Equation 7.1), the influence of TDs on both J_{o1} and J_{o2} must be determined. We will examine each component individually before modeling the entire DIV (J_{sc}=0) curve for various TDDs.

$$J = J_{o1}\left(\exp\left(\frac{qV}{kT}\right)-1\right)+J_{o2}\left(\exp\left(\frac{qV}{2kT}\right)-1\right)-J_{sc} \qquad \text{Equation 7.1}$$

First we examine the diffusion current, J_{o1}(TDD), for n+/p and p+/n solar cells using Equation 7.2; the results are shown in Figure 7.3. We find that in the TDD dominant regime, J_{o1} for an n+/p diode is higher than that of a p+/n diode. Since both L_p and L_n converge to the same value at high TDDs (they are material independent values) and since the term associated with the lower doped base typically dominates J_{o1} in one-side abrupt junctions, we can see that differences in electron and hole mobility/diffusion coefficients generates higher recombination rates and thus higher reverse saturation currents in n+/p diodes. In this figure, we have plotted both the finite and infinite diode case; in the infinite diode F_p=F_n=1. Note that the infinite diode models shows a difference in J_{o1} for n+/p and p+/n diodes at low TDD, where as the finite diode shows J_{o1} for p+/n and n+/p converge at low TDD.

$$J_{o1} = qn_i^2\left(\frac{F_p}{N_A}\left(\frac{D_n}{L_n}\right)+\frac{F_n}{N_D}\left(\frac{D_p}{L_p}\right)\right) \qquad \text{Equation 7.2}$$

$$\text{with} \quad \frac{1}{L^2} = \frac{1}{L_{\max}^2}+\frac{\pi^3[TDD]}{4}$$

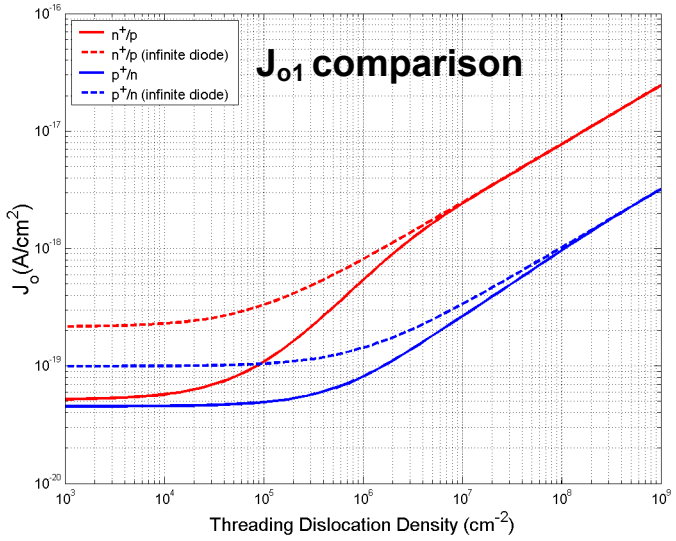


Figure 7.2 This shows the reverse saturation current from diffusion (J_{o1}), using Equation 7.2, and L(TDD) for n+/p and p+/n diodes.

Now in wide-bandgap materials, which have low n_i values, depletion region recombination often dominates the total J_o. This recombination current component, J_{o2}, is described by Equation 7.3. From this, we find an inverse relationship between J_{o2} and τ_{base}. Thus, lower τ_n values compared with τ_p values contribute to higher J_{o2} values for n+/p diodes. In Figure 7.3, we plot J_{o2}(TDD) for both n+/p and p+/n diodes.

$$J_{o2} = \frac{qn_i W_D}{2}\left(\frac{1}{\tau_{base}}\right) \qquad \text{Equation 7.3}$$

$$\text{with} \quad \frac{1}{\tau} = \frac{1}{\tau_{\max}} + \frac{\pi^3 D[TDD]}{4}$$

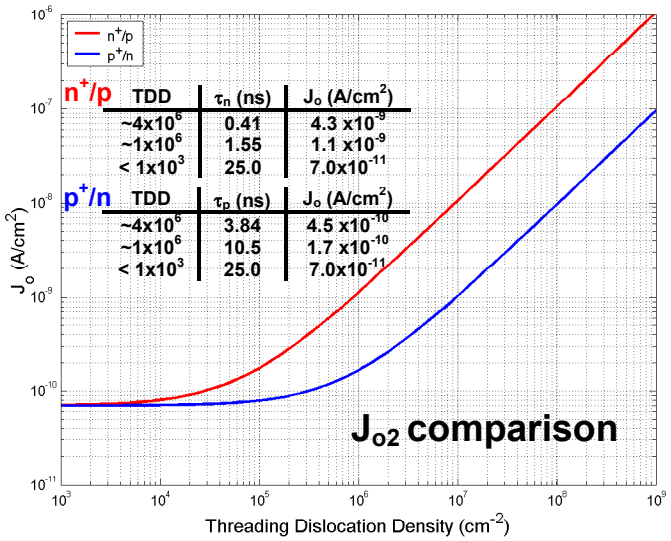


Figure 7.3 This shows the reverse saturation current from depletion region recombination (J_{o2}), using Equation 7.3, with τ(TDD) for n+/p and p+/n diodes. The embedded table compares the calculated τ and J_{o2} values for a couple of TDDs.

Comparing these two figures it is clear that at lower voltages J_{o2} will dominate the DIV curve since it is on the order of 10^{-10} A/cm^2 compared with J_{o1} which is on the order of 10^{-19} A/cm^2. To determine the voltage regions of dominance for each current component, the DIV curve is calculated using both J_{o1} and J_{o2} components in Equation 7.1 (J_{sc}=0). We plot the DIV curve for three TDD values in Figure 7.4 for n+/p diodes and in Figure 7.5 for p+/n diodes. An increase in J_o with TDD is seen in each figure by a shift in the DIV curve to higher current density values. The shift exhibited in Figure 7.4 for n+/p diodes is greater than that exhibited in Figure 7.5 for p+/n diodes for the same

changes in TDD values. This is a direct result of the fact that J_{o2} values for n+/p diodes begin to increase at lower TDD values compared to p+/n diodes, as shown in Figure 7.3.

In these DIV curves, we have chosen to include a voltage dependent depletion width. This is not done in other TDD dependent modeling completed to date [1]; however, it is employed in the Sah-Noyce-Shockley model [2] from which the expression for J_{o2} was derived (with various approximations). It is clear that a decrease in W_D with voltage causes a decrease J_{o2} and thus the effective ideality factor is higher than the n=2 value shown in Equation 7.1. In the case where W_D is fixed at its unbiased value, the effective ideality factor is 2 (instead of ~ 2.1), until J_{o1} becomes dominant at higher voltages where n decreases to a value of 1.

In each figure, a line representing a typical AM0 GaAs solar cell J_{sc} value (~30 mA/cm^2) is also plotted. The intersection of this line with the DIV curve describes the expected V_{oc} value for a solar cell with that TDD. It is evident that lower open-circuit voltages are expected for n+/p diodes at a given TDD due to increased J_o values. The arrows in these figures represent the range in V_{oc} values expected for a change in TDD from 1x10^3 to 4x10^6 cm^{-2}; clearly, a larger variation in the V_{oc} predicted for n+/p solar cells. Moreover, another result of higher J_{o2} values is that the J_{o1} (n=1) region starts to contribute at a higher voltage, and thus the effective ideality factor for solar cells in the vicinity of V_{oc} are higher and the FF lower.

Figure 7.6 shows V_{oc}(TDD) and FF(TDD) for various device models are calculated assuming a J_{sc} of 30 mA/cm^2. The main result, irrespective of the model used, is that n+/p V_{oc} values are lower then p+/n solar cells as are the FFs. The V_{oc} values begin to decrease significantly at ~ 1x10^5 cm^{-2}, the same TDD where τ_n began to decrease

(see Chapter 6). The impact of TDD on FF is often overlooked, since the FF depends on many other factors; however, this analysis provides an upper bound for GaAs device with TDs present. Looking at the various models implemented, the solid lines represent the use of both J_{o1} and J_{o2} in Equation 7.1 with both voltage independent and dependent depletion widths. The dashed lines represent the use of only the J_{o2} term in Equation 7.1 and again voltage independent and dependent depletion widths are used. The general results from the comparison of these models are that the curves for n+/p and p+/n, for a given model, converge at low TDDs, using only the J_{o2} component leads to higher V_{oc} values at lower TDDs, but converge with the full model (J_{o1} and J_{o2}) at higher TDDs due to the dominance of the J_{o2} component, and that using the voltage dependent depletion width produces higher V_{oc} values due to the reduction in J_o through the reduction in W_D with increasing voltage. Figure 7.6b shows the *FF*(TDD) for these same models. It is clear that the n+/p solar cells have lower *FF*s due to the earlier dominance of the J_{o2} component and thus higher effective ideality factors. The models that only use the J_{o2} component have the lowest *FF*s since the effective ideality factor does not decrease at low TDDs. For the full models, the voltage dependent depletion width model produces lower FFs at high TDD since the effective ideality factor is higher (n~2.1). However, in the low TDD regime, the lower value of J_{o2} causes the J_{o1} component to dominate at earlier voltages and thus higher FF values are obtained. Because the cell efficiency depends both on V_{oc} and *FF*, the dominance of J_{o2} in metamorphic cells causes reductions in efficiency from both terms.

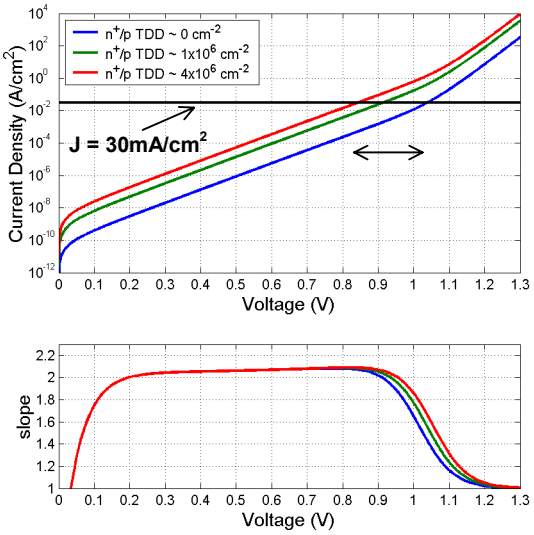


Figure 7.4 The DIV for n+/p GaAs solar cells with varying TDD. Also shown is the effective "ideality factor" as a function of voltage for these three device.

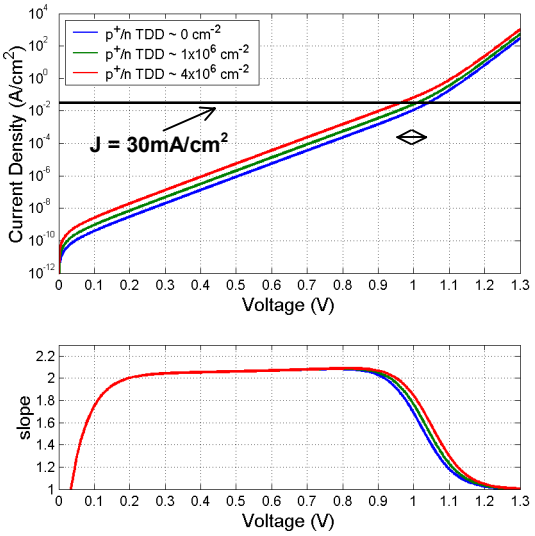


Figure 7.5 The DIV for p+/n GaAs solar cells with varying TDD. Also shown is the effective "ideality factor" as a function of voltage for these three device.

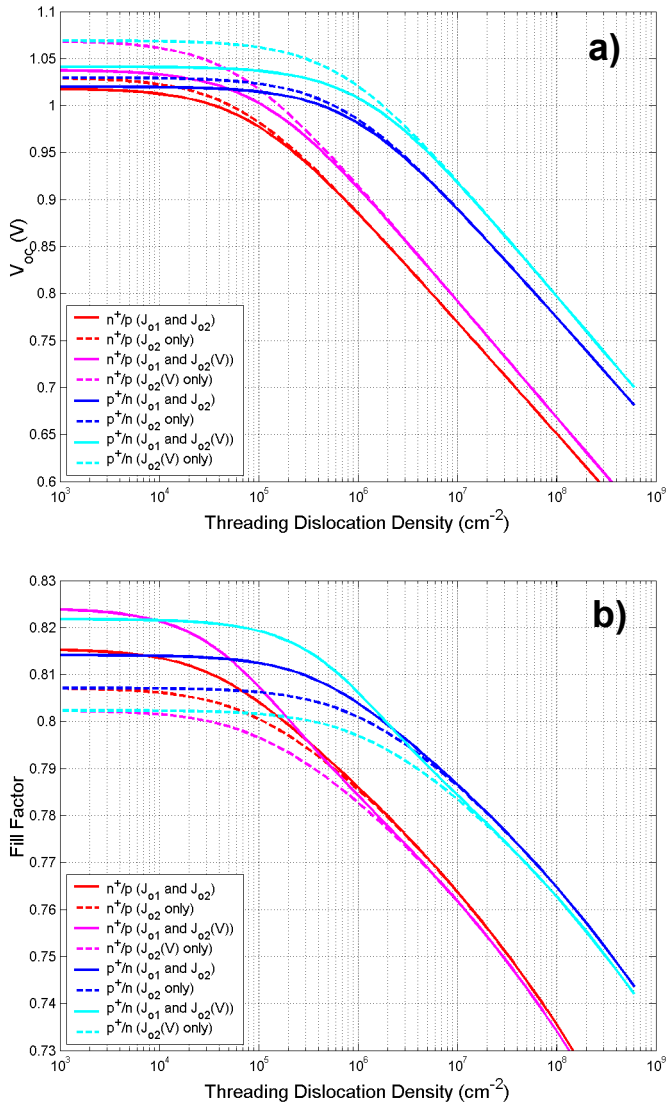


Figure 7.6 a) Open-circuit voltage (V_{oc}) as a function of TDD for n+/p and p+/n solar cells, assuming J_{sc} of 30 mA/cm^2. b) Fill Factor (FF) as a function of TDD for n+/p and p+/n solar cells, assuming J_{sc} of 30 mA/cm^2.

7.2 GaAs on SiGe diode performance

In order to measure the impact of TDD on GaAs diode/solar cell performance the p+/n and n+/p device structures shown in Figure 7.1 were grown on a GaAs substrate and SiGe substrates with varying TDDs. In some cases these devices were grown by solid source molecular beam epitaxy (SSMBE) and in others low pressure metal-organic chemical vapor deposition (LP-MOCVD). Measurement of homoepitaxial solar cells grown by both methods produced similar results, thus a comparison of devices is valid.

For this study, both n-type and p-type SiGe substrates were needed in order to make back contacts to the solar cells. Compositionally graded, relaxed n-type SiGe layers grown on n-type Si substrates were grown by ultra-high vacuum chemical vapor deposition (UHV-CVD)[3], where as compositionally graded, relaxed p-type SiGe layers grown on p-type Si substrates were grown by low-pressure chemical vapor deposition (LP-CVD)[4], in each case a chemical mechanical polish (CMP) step was employed at $Si_{0.5}Ge_{0.5}$ which produced a final TDD of $\sim 1x10^6$ cm^{-2}. Also used in this study was a p-type SiGe grown by LP-CVD that did not use a CMP step, therefore, this substrate had a higher residual TDD of $\sim 4x10^6$ cm^{-2}. The TDDs were measured by counting the etch pit densities (EPDs) in the Ge termination layer prior to III-V growth.

GaAs growth on the Ge terminated surface of the SiGe substrates was initiated by using solid source molecular beam epitaxy (SSMBE) prior to device growth by LP-MOCVD or SSMBE. The GaAs growth initiation procedure followed the method described in Ref. 5; however, not all devices utilized migration enhanced epitaxy (MEE) step that would eliminate all anti-phase domain (APD) disorder. As described in Chapter

6, good material quality (high lifetimes) has been obtained for both initiation conditions. The III-V growth conditions for solar cell device layers are outlined here. For LP-MOCVD growth, the GaAs growth rate was ~ 2μm/hr and the $In_{0.49}Ga_{0.51}P$ growth rate was ~ 2.2 μm/hr, Si and Zn were used for n-type and p-type dopants respectively. For SSMBE growth, the GaAs growth rate was ~ 1μm/hr and the $In_{0.49}Ga_{0.51}P$ growth rate was ~1.12 μm/hr, Si and Be were used for n-type and p-type dopants respectively. Unlike the DHs from Chapter 6, these growths were performed individually, not simultaneously, due to the larger substrate size needed for solar cell devices. Therefore, there may be fluctuation in exact growth conditions from growth to growth.

To confirm the electrical activity of the dislocations, electron beam induced current (EBIC) measurements were performed on these devices after processing. From Figure 7.7 we see that there are clearly more localized recombination centers in Figure 7.7b compared with Figure 7.7a. Dark-spots densities of ~$1.3x10^6$ cm^{-2} and ~$1.2x10^6$ cm^{-2} and ~$4.2x10^6$ cm^{-2} were measured for the cells grown on SiGe, which are close to the EPD values measured in the substrates. Thus, the residual TDDs are maintained in the III-V epitaxial layers. This also shows that there is a correlation between the defects measured by EPD and those that are electrically active in EBIC. It should be noted that in some material systems, such as $In_{0.69}Ga_{0.31}As$, where diodes with relatively high TDDs do not show a clear J_o(TDD), dark spots are not seen in EBIC images.[6] In others materials, where defects are passivated by hydrogen the recombination, the intensity of the "dark-spots" are reduced.[7] These results suggestions that this model may not be applicable to all materials. However, looking with EBIC may be a good way to test a material system to determine if this model can be applied.

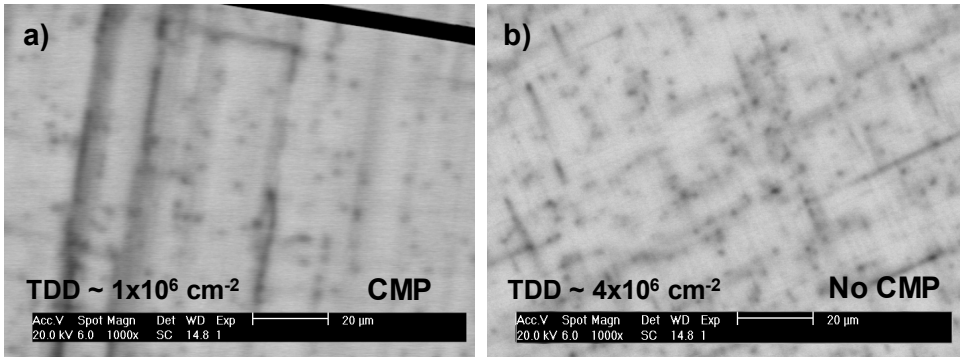
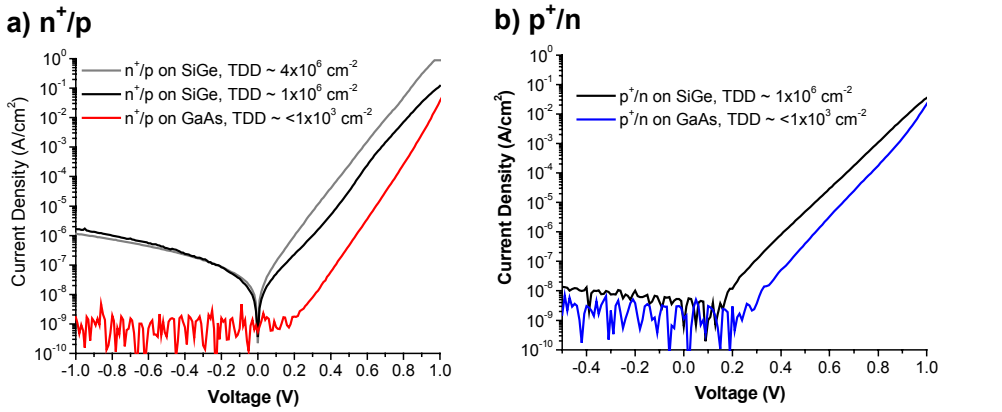


Figure 7.7 Plan-view EBIC images for GaAs solar cells grown on SiGe substrates with two different TDDs.

The X-TEM images from Chapter 6 shows that no structural defects are seen at the SSMBE/LP-MOCVD re-growth interface and thus re-growth is not expected to significantly impact the device performance. The devices were processed in the manner outlined in Appendix D, all processing was completed at Ohio State except for the deposition on the antireflective coating. The base doping levels were confirmed by measuring the capacitance-voltage profile using a Boonton 7200 C-V meter. The base doping level measured for all of the diodes in this study were in the range of 1.5×10^{17} to 2.5×10^{17} cm^{-3}. The diode dark current density versus voltage curves (DIVs) were measured in a Signatone dark box with a Keithley 2400 digital source meter with a current detection limit of 0.1 nA. Diode areas were 1.0 mm^2. The extracted reverse saturation current (J_o) and an "ideality factor" (n) for each diode were determined from these DIV curves using a linear fitting algorithm on the logarithm of current density versus voltage for the voltage range of 0.4 V to 0.8 V.

The DIV measurements from five GaAs diodes/solar cells are shown in Figure 7.8. In Figure 7.8a, the performance for n+/p diodes with three different TDD are compared. The extracted J_o values and the effective ideality factor, n, from linear fits are shown in the corresponding table along with the measured electron lifetime at these TDDs from Chapter 6. In the same manner, Figure 7.8b shows the performance for p+/n diodes with two different TDD. It is clear that and increase in TDD produced an increase in J_o and n values as expected. For a given polarity device, the form of Equation 7.3 suggests that the ratio the J_{o2} values should be similar to the inverse ratios of their lifetimes and thus the ratio of their TDDs when in the TDD dominated regime. Since the homoepitaxial cells are clearly in the transition period between J_{o2} and J_{o1} dominance and not in the TDD dominated regime, the measured J_o values cannot be directly compared to those with higher TDDs. If we compare the J_o values for n+/p diodes at two different TDD we find that the ratio of J_o is ~ 5, where as the ratio of their TDDs is ~ 4 and the inverse ratio of their measured lifetimes is ~ 3.

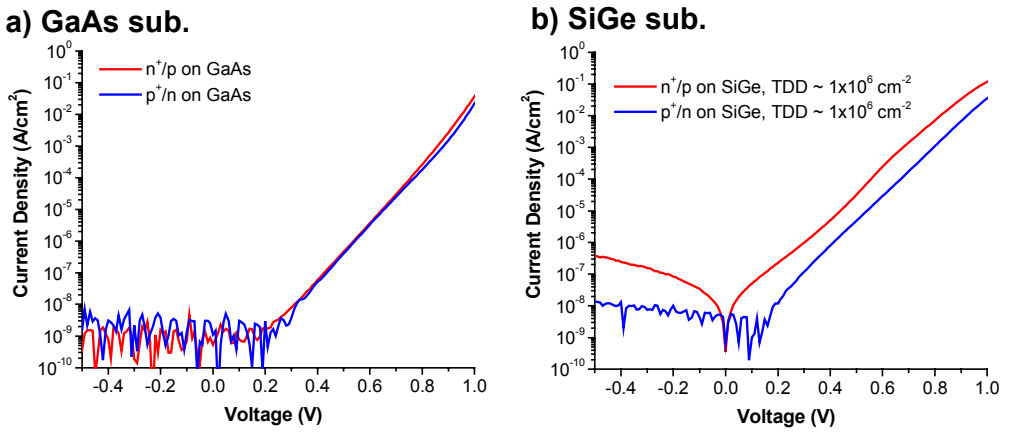
The DIV curves for n+/p and p+/n diodes with the same TDD are compared in Figure 7.9. In the cases of growth on GaAs substrates with TDDs less than $1x10^3$ cm^{-2} there is no difference in cell performance; however, this in clearly not the case for a TDD of ~$1x10^6$ cm^{-2}, shown in Figure 7.9b. From the models, we expect that the ratio of J_{o2} values should reflect the ratio of τ_p / τ_n and thus of D_n/D_p values in the TDD dominated regimes. At a TDD of $1x10^6$ cm^{-2} we find that the ratio of J_o(n+/p)/ J_o(p+/n) is 12, ratio of τ_p/τ_n is 7, and the ratio of D_n/D_p values is 11. These ratios are consistent with the trend suggested by the proposed device models, although, there is not an exact match between experimental and theoretical J_o values.



sub.	TDD	τ_n (ns)	J_o (A/cm^2)	n
SiGe	~4x10^6	0.53	3 x10^{-8}	2.1
SiGe	~1x10^6	1.5	6x10^{-9}	2.1
GaAs	< 1x10^3	20.0	1.3x10^{-11}	1.8

sub.	TDD	τ_p (ns)	J_o (A/cm^2)	n
SiGe	1x10^6	10	5x10^{-10}	2.1
GaAs	< 1x10^3	22.4	1.3x10^{-11}	1.8

Figure 7.8 DIV curves for a) n+/p and b) p+/n GaAs diodes grown on GaAs and SiGe substrates.



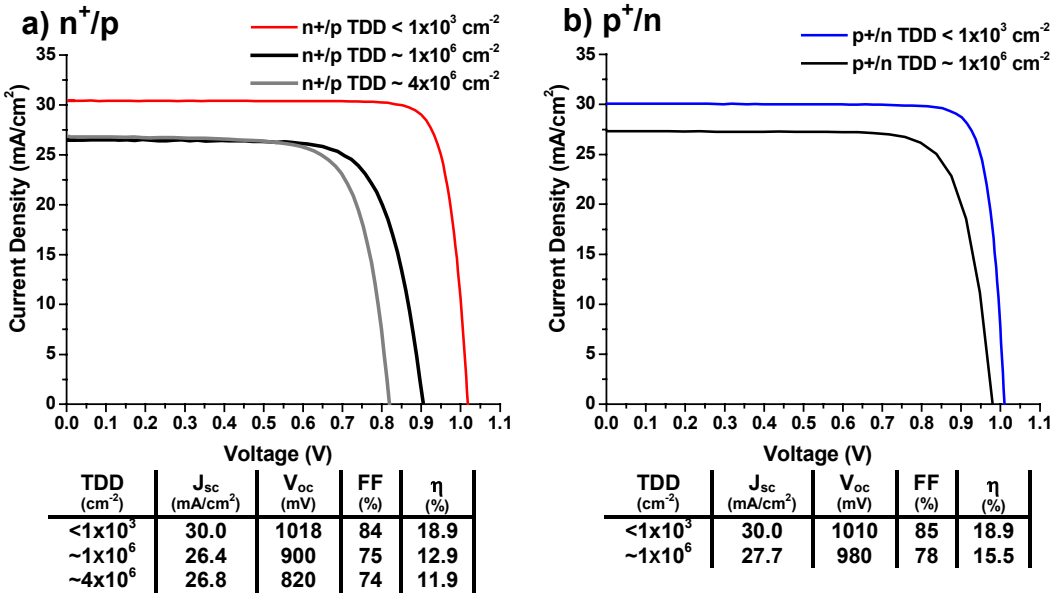
	TDD	τ (ns)	J_o (A/cm^2)	n
n$^+$/p	< 1x10^3	20	1.3x10^{-11}	1.8
p$^+$/n	< 1x10^3	22	1.3x10^{-11}	1.8

	TDD	τ (ns)	J_o (A/cm^2)	n
n$^+$/p	~ 1x10^6	1.5	6x10^{-9}	2.1
p$^+$/n	~ 1x10^6	10	5x10^{-10}	2.1

Figure 7.9 a) Diodes grown on GaAs substrates with TDDs less than 1x10^3 cm^{-2} have matching device performance. b)Devices on SiGe with the same TDD, ~ 1x10^6 cm^{-2}, have differing device performance. The n+/p diode has a higher J_o value compared to the p+/n diode.

7.3 GaAs on SiGe solar cell performance

The solar cell performance for these GaAs devices were measured at NASA Glenn Research Center with an X-25 Spectrolab Solar Simulator calibrated for the AM0 spectrum. Figure 7.10 shows the LIV and the solar cell performance parameters for each device. As indicated by the experimental DIV data presented, increased TDDs reduce V_{oc} and lower V_{oc} values for n+/p solar cells compared to p+/n solar cells are measured. It is clear that the J_{sc} values for solar cells on SiGe are lower than those on GaAs substrates; however, the parameter of interest in this discussion is V_{oc} since J_{sc} at this TDD can be improved by cells design, metal coverage, improvements in ARC, etc.



TDD (cm^{-2})	J_{sc} (mA/cm^2)	V_{oc} (mV)	FF (%)	η (%)
$<1x10^3$	30.0	1018	84	18.9
$\sim1x10^6$	26.4	900	75	12.9
$\sim4x10^6$	26.8	820	74	11.9

TDD (cm^{-2})	J_{sc} (mA/cm^2)	V_{oc} (mV)	FF (%)	η (%)
$<1x10^3$	30.0	1010	85	18.9
$\sim1x10^6$	27.7	980	78	15.5

Figure 7.10 LIV curves for a) n+/p and b) p+/n GaAs solar cells measured under AM0 illumination.

The device models discussed earlier are substantiated by experimental V_{oc} values measured at 30 mA/cm^2 for the solar cells grown on GaAs and SiGe described in this thesis and in Ref. 8, 9, and10. These V_{oc} values are compared with modeled results as shown in Figure 7.11. In order to show the general nature of this TDD dependence, representative V_{oc} data obtained from the literature for GaAs solar cells having appreciable TDDs are also plotted in Figure 7.11.[11,12,13,14] This data includes GaAs solar cells grown on Si substrates using other interlayer approaches that yield higher TDD values than using SiGe, as well as data for GaAs cells grown on dislocated GaAs substrates with a range of TDD values. While the measured V_{oc} values for n^+/p and p^+/n homoepitaxial samples have comparable values as expected (1.05 V and 1.03 V, respectively), the two device polarities demonstrate a substantial disparity in V_{oc} with increasing TDD.

Although some scatter in V_{oc} data is be expected, it is clear that the trend suggested by the device models is reflected in experimental data. These sources of deviations include the accuracy of TDD values, the device layer doping values, and the J_{sc} for which these V_{oc} values were measured. For example, a good AM1.5 J_{sc} value is 25 mA/cm^2 compared with 32 mA/cm^2 for the AM0 spectrum. A change in J_{sc} from 22 mA/cm^2 to 32 mA/cm^2 is expected to change the V_{oc} for a given cell, assuming a voltage independent n=2 diode model, by a voltage of 0.02 V regardless of J_o. This is seen in Equation 7.4.

$$V_{oc} \approx \left(\frac{2kT}{q}\right)\ln\left(\frac{J_{sc}}{J_{o2}}\right) = \left(\frac{2kT}{q}\right)\left(\ln\left(J_{sc}\right) - \ln\left(J_{o2}\right)\right) \qquad \text{Equation 7.4}$$

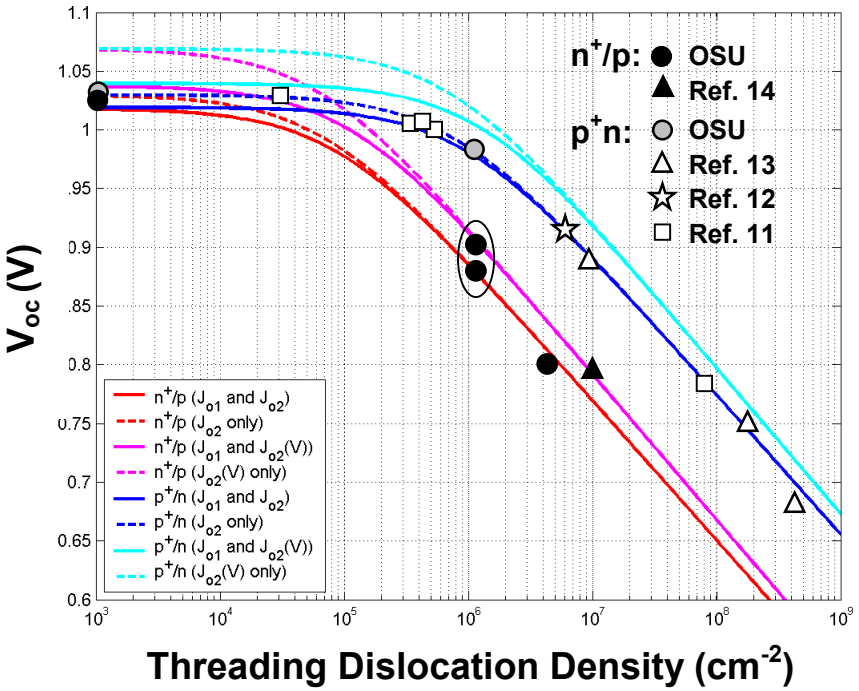


Figure 7.11 The open circuit voltage for n^+/p and p^+/n GaAs solar cells as a function of threading dislocation density. The lines represent the theoretically calculated values presented in Section 7.1. The V_{oc} data from Ref. 12, 13, 14 are for GaAs solar cells grown on Si substrates and the data from Ref. 11 are for GaAs solar cells grown on intentionally dislocated GaAs substrates using $GaAs_{1-x}P_x$ layers. This data demonstrates the completeness of this model beyond GaAs integration on SiGe substrates.

There are clearly more data points for p+/n solar cells shown in Figure 7.11 than for n+/p, since prior work in this field concentrated only on p+/n GaAs solar cells. Most direct epitaxial methods have not been able to obtain TDD lower than ~$7x10^6$ cm^{-2}, where as the use of SiGe has demonstrated TDD of ~$1x10^6$ cm^{-2}; the significance of this

TDD reduction results in a improvement in V_{oc}. The V_{oc} data for p+/n cells with TDD < $1x10^6$ cm^{-2} were taken from GaAs cells grown on a dislocated template using GaAsP, not a Si substrate. This data shows the consistency of the V_{oc} trend as it approaches the homo-epitaxial V_{oc} values plotted at a TDD of $1x10^3$ cm^{-2}.

As mentioned above, there has been significantly less research by other groups concerning n+/p GaAs/Si solar cell device performance. In fact, only one other published report exists.[14] Since this represents only one data point and was published in 1981, it was important to experimentally verify the behavior of V_{oc}(TDD) for n+/p GaAs solar cells. The two circled data points for n+/p solar cells at a TDD of $1x10^6$ cm^{-2} were measured for two solar cells grown on a single SiGe substrate. This cell had an active junction that resulted from Arsenic diffusion into the p-type Ge layer of the SiGe substrate; this type conversion created a Ge n/p junction whose built-in voltage added to the GaAs built-in voltage and produced a higher V_{oc} value. In some cases, the active Ge junction produced V_{oc} values of ~0.90 V where as the in-active Ge junction produced V_{oc} values of ~0.86 V. The non-active junction showed high series resistance due to conduction through the compensated/inter-diffused layers, although its V_{oc} value matches the modeled results. The development of active Ge or Si junctions was the main reason n+/p cells were avoided in early work GaAs/Si solar cell development, despite the fact n+/p solar cells were the dominate cell polarity used commercially. From this research, it is clear that another reason n+/p GaAs/Si devices should be avoided for high efficiency applications is the reduced performance at TDD of $1x10^6$ cm^{-2} compared to p+/n devices.

The measured *FF* values for these solar cells are not directly compared to the *FF* values calculated in Figure 7.6b because the *FF* is greatly influenced by series resistance

(R_s) and J_{sc}. Series resistance in these cells varies greatly due to the conduction through GaAs/Ge or GaAs/Si interfaces where inter-diffusion or hetero-junction barriers can exist. The V_{oc} values were easily compared because they are independent of R_s since V_{oc} is measured with no current flow; moreover, the effect of J_{sc} on V_{oc} is easily quantified. *FF*s for p+/n GaAs/Si solar cells up to 79% have been achieved for 1-sun measurements. These values are lower than values measured for homo-epitaxial GaAs cells, which are typically in the range of 83-86%. The *FF* for n+/p solar cells at various TDD have been ~ 74-75%, except for the higher series resistance cells discussed earlier which had *FF* values of ~ 60%. This data suggests that device polarity may also play a role in metamorphic GaAs cell efficiency through reduced *FF*s as well as V_{oc} values.

7.4 Conclusions

The presence of TDs lead to increased reverse saturation currents in GaAs diodes. A significant difference in the reverse saturation current values for n+/p and p+/n diodes was observed, due to the fundamental difference in lifetime for electron and holes in GaAs with TDs. We found that both the diffusion (J_{o1}) and the depletion region recombination (J_{o2}) terms are impacted by these changes in lifetime (τ(TDD)), although, J_{o2} typically dictated the solar cell device performance due to the dominance of depletion region recombination in the vicinity of V_{oc}. Given the experimental data for V_{oc} shown in Figure 7.11, we find that solar cell modeling closely predicts V_{oc} values as a function of TDD. The application of these modeling techniques to other III-V metamorphic diodes will be explored in Chapter 9; where the impact of TDD on $In_{0.49}Ga_{0.51}P$ is investigated.

7.5 References

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CHAPTER 8

$In_{0.49}Ga_{0.51}P$ SOLAR CELLS GROWN BY SSMBE

Before considering the impact of threading dislocations on $In_{0.49}Ga_{0.51}P$ (InGaP) material properties or solar cell performance, the properties of this material were first studied on a lattice-matched GaAs substrate. Unlike GaAs, this material is relatively new to SSMBE since a valved phosphorus source has only been available for ~ 15 years. Therefore, Section 8.1 will detail the growth procedures and calibrations used in SSMBE InGaP growth at the Ohio State University. Based on these growth parameters, the development of InGaP single junction solar cells are reported in Section 8.2. A comparison of as-grown and annealed n+/p and p+/n InGaP solar cells indicated improved device performance with annealing. Changes in the n+/p and p+/n cell design were also investigated in order to improve InGaP solar cell performance in the as-grown condition. Although improvements in performance have been demonstrated, further optimization is required for InGaP solar cell performance that is consistent with commercial devices.

8.1 SSMBE of $In_{0.49}Ga_{0.51}P$

A literature survey was completed pertaining to the growth of InGaP by SSMBE as reported by other research groups before attempting to grow this alloy for the first time in our SSMBE system at the Ohio State University. In particular, there were four research groups from 1991-2000 who published studies concerning SSMBE of III-P materials and the electrical and optical properties of $In_{0.49}(Al_xGa_{1-x})_{0.51}P$ (InAlGaP) alloys grown with valved solid phosphorus (P) sources.[1, 2, 3, 4] Based on these references and testing at OSU, growth conditions for InGaP were selected. Some of the growth parameters considered were the growth temperature, the Phosphorus:Group III "flux" ratio, and the P cracker temperature. Also considered was the ability to reproducibly achieve lattice-matched InGaP and to achieve carrier concentration calibration curves for InGaP and InAlGaP alloys. The information presented in this chapter was used as a starting point for InGaP solar cell development and for studies concerning the impact of threading dislocations on InGaP material properties and solar cell performance.

8.1.1 Phosphorus source

Before discussing the use of the solid phosphorus source for InGaP growth by SSMBE, a basic description of the solid P source is provided along with a description of the sources ability to control the particular phosphorus molecule used for growth, P_2 or P_4. In the case of the three-zone EPI valved source shown in Figure 8.1[5], the P atoms are first sublimed from the red P source material in the "red zone" at a temperature between 350°C and 400°C and are condensed as white P in the "white zone" at a temperature of ~ 50°C. After a designated length of time, the sublimation of red P from

the “red zone” is terminated and the white P collected in the “white zone” is the “source” of P molecules for III-P semiconductor growths. One difference in these solid forms of P is that white P auto ignites in the presence of oxygen (like a grenade), where as, red P requires both oxygen and a spark for ignition (like a match). (This is the reason why red P is used as the P source material and is only converted to white P in vacuum.) The advantage of using white P compared to red P for SSMBE growth is that the higher vapor pressure of white P results in a more stable flux of P molecules. The “white zone” temperature is typically set to ~ 68-72°C for reasonable P fluxes, at this temperature the white P sublimes as P_4 molecules which then pass through the open valve into the “cracking zone” where they are subjected to an elevated temperature. The elevated temperature can dissociate the P_4 molecules to produce P_2 molecules and also heats the valve assembly to prevent the condensation of P molecules that could inhibit the valve from opening and closing. The decision to use P_2 or P_4 molecules, and thus the selection of the P cracker temperature, has safety/system considerations as well as InGaP material quality considerations.

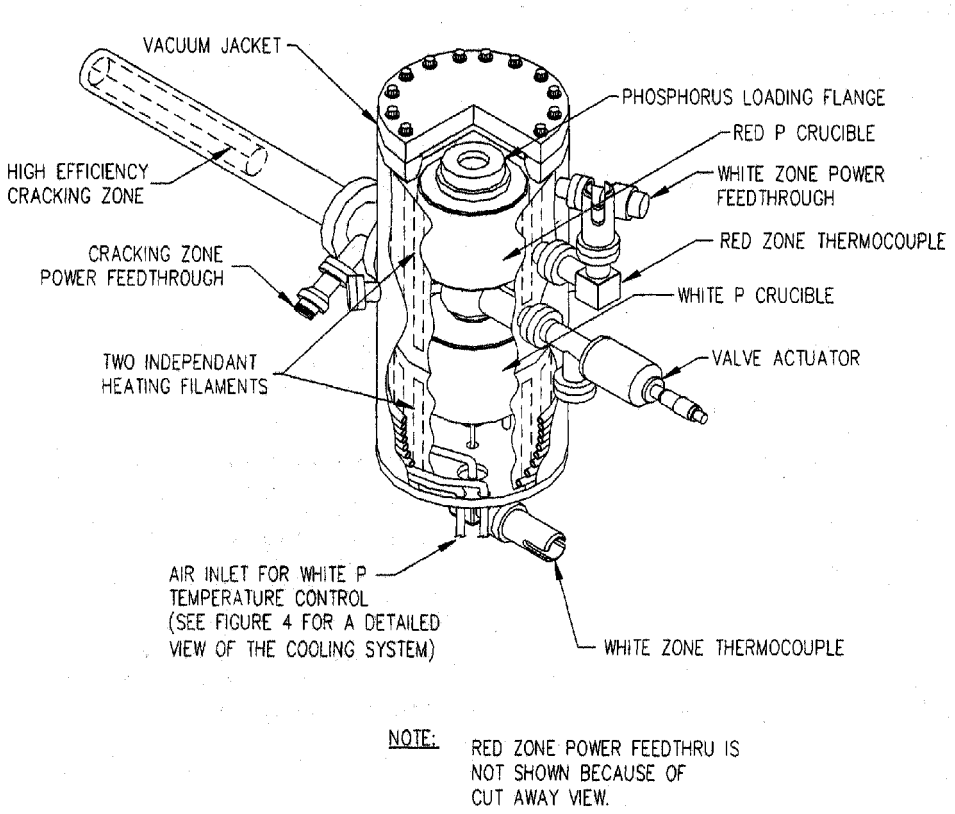


Figure 8.1 EPI Mark IV valved P source with cracker. This figure shows the "red zone", the "white zone", and the "cracking zone" of the solid P source. [after 5]

When considering the impact of P usage on the SSMBE system, it is important to account for the P that is not incorporated into the epitaxial films. Essentially, P_4 molecules condense on surfaces colder than ~ 100°C as white P and P_2 molecules condense as red P. The presence of white P on the walls of the SSMBE chamber poses a fire hazard if the MBE chamber is accidentally vented to room air since room air would provide an ignition source (oxygen). To prevent such fires during controlled chamber openings, the MBE system is "baked" at a temperature of ~ 200°C prior to venting the

chamber in order to remove any white P from the walls of the chamber. The P that sublimes from the walls of the chamber during this baking procedure is collected on a specially designed liquid nitrogen chilled cryo panel for proper disposal. (This process if often called P recovery.) One problem with this procedure is that the white P can become physically trapped under metallic evaporations and thus may still be present after baking the chamber, which represents a significant fire risk.

Unlike the majority of white P, red P remains on the walls of the chamber after baking since it has a higher sublimation temperature. When red P is exposed to room air it can react and produce phosphine gas, which is a health risk. However, monitoring of phosphine levels during chamber openings at OSU has not detected measurable amounts phosphine. Red P on the chamber walls can also absorb H_2O and form P_4O_6, which can serve as a source of oxygen contamination in material layers grown later in the SSMBE chamber. Finally, since red P remains in the chamber any excess accumulation has to be neutralized with chemical cleaning which requires dismantling the vacuum system. Normal chamber openings do not require system cleaning and thus exposure to air can be minimized by the continuous flow of nitrogen gas through the chamber. There are risks associated with the use of both P_2 and P_4 and so the safe use of P in SSMBE has been something that each research group has had to develop on there own. Over the last 4 years, OSU has developed a safe and reliable method for cataloging P conversion process and the total P usage, an efficient P recovery process, and safe system venting and opening procedures that minimize fire hazards.

The impact of the P species used in InGaP growths has less to due with the actual P_2 or P_4 molecules and more to due with the impact of the higher cracker temperature on

impurities that may be present in the P source. Reports in the literature suggested that increases in the cracker temperature from 700 °C to 1000°C significantly impact the material quality of InGaP through increased incorporation of oxygen [2] or increased incorporation of unintentional acceptors levels [6]. Ref. 2 showed that the higher cracker temperatures "cracked" P_4O_6 molecules that were present, which made the incorporation of oxygen into the epitaxial films more efficient. It was for this reason that 800°C was initially selected as the P cracker temperature at OSU and the fact that some references stated that such cracker temperatures produced "P_2" dominated fluxes [3]. Based on large deposits of white P on the chamber walls and the examination of the mass spectra on the newly acquired quadrupole mass analyzer, it was later determined that a significant portion of the P molecules were actually P_4, not P_2. As such, a "P_4" dominated P flux was initially used for InGaP growths at OSU. During the P recovery process, where the white P sublimes from the chamber walls and is collected for safe disposal, the chamber pressures, which are typically below $1x10^{-10}$ torr, rose to pressures in excess of $1x10^{-2}$ torr, creating undesirable system condition. By increasing the cracker temperature to 950°C a P flux dominated by "P_2" molecules was achieved. This was confirmed by the fact that during P recovery significantly lower amounts of white P were collected in the liquid nitrogen cryo panel and pressure during P recovery are consistently below $1x10^{-4}$ torr.

8.1.2 Growth rate and growth temperature

As discussed above, there are many variables to consider when optimizing the growth parameters for SSMBE InGaP. Based on the literature survey, the typical growth temperatures were between 450°C and 490°C. Above this temperature range, the In composition was found to decrease due to In desorption and thus the assumption of Ga and In sticking coefficients of ~1 would no longer be valid.[3] The ability to grow at lower temperatures was limited by the optical infrared pyrometer used in the SSMBE system at OSU, which did not give consistent temperature readings below ~ 475°C, depending the mounting configurations and the temperatures of the other sources in the SSMBE system. Since, higher growth temperatures were also shown to incorporate less oxygen [7], a "standard" growth temperature of ~ 490°C was selected for InGaP growths and growth studies. InGaP growths at 490°C with sufficient P flux were capable of producing smooth films and good RHEED reconstructions.

Using a sticking coefficients of 1 for both Ga and In, calculations similar to those shown in Appendix A were completed to obtain the proper fluxes or beam equivalent pressures (BEPs) for 48.5% In and 51.5% Ga and a growth rate of ~ 1.123 mono-layers/sec or ~3.175 Å/s or ~1.14 μm/hour. This growth rate was selected as our standard growth rate since it used the same In rate (or BEP) that was being used in our $In_{0.53}Ga_{0.47}As$ research [8] and it was consistent with the growth rates found in the literature that were typically ~1μm/hr.[1, 2, 3] Other groups have reported growth rates of ~2 μm/hr by SSMBE and have achieved reasonable device performance.[9, 10] . As a note, it was more difficult to obtain smooth InAlP or InAlGaP layers with thickness in

excess of 1 μm. Since only thin layers were employed in the InGaP solar cell structures, the RHEED pattern maintained a streaky appearance and so no change in growth characteristics were performed at such device layers. It should also be mentioned that the use of InAlGaP in early research was impeded by the source configuration that included 1 Ga source and 2 Al sources. The Ga source could not be changed at these interfaces to accommodate the quaternary InAlGaP layers adjacent to InGaP layers. To remedy this situation, an Al source was replaced with a Ga source; thus such structures are now readily grown.

8.1.3 Phosphorus:Group III flux ratio

As mentioned above, a substrate growth temperature of ~490°C and a growth rate of ~ 1.14 um/hr were used for all growths while the P cracker temperatures of both 800°C (P_4) and 950°C (P_2) were used. A series of InGaP samples were grown using various P/III beam equivalent pressure (BEP) ratios in order to optimize the optical quality of the materials. The BEP is used instead of actual flux ratios since the BEP is easily measured with an ionization gauge in the MBE chamber. This gauge has different ionization efficiency for each type of atoms, so the P:III BEP ratio reflects the BEP of P molecules compared with the total Group III BEP with reference to the ionization efficiency of In. (See Appendix A for more details.) Since other groups have reported an increase in deep level concentration with an increase in the P:III ratio above 30:1[11, 12], we studied flux ratios from 3:1 to 20:1. We found that P_2:III ~ 12 and P_4:III ~ 7 showed the best luminescence characteristics of InGaP samples grown on semi-insulating GaAs substrates, in the sense of narrow spectral width and high luminescent intensity for room

temperature PL spectra. The measured PL curves for the InGaP samples grown using P_2 are shown in Figure 8.2a for room temperature PL and Figure 8.2b for low temperature PL. Since the InGaP layers grown with P:III ratios 12:1 and 6:1 have comparable low-temperature PL performance, it is not conclusive that one growth condition is superior to the other. Growths completed that were phosphorus deficient (ie. 3:1 for P_2:III) had rough surfaces and poor surface reconstruction as shown by a RHEED patterns with ill-defined streaks and the appearance spots. It should be noted that changes in cracker temperature from 950°C to 800°C for the same white zone temperature increases the measured BEP. This fact makes comparisons of BEP ratios with those in the literature difficult since the cracking efficiency of the cells being used cannot be known.

X-ray diffraction for the InGaP layers grown in the P_2 study showed that the InGaP layers were lattice-matched to the GaAs substrate. This is consistent with Equation 8.1 which expresses the InGaP bandgap as a function of In composition from Ref. 13 and the RT PL peak energy of 1.891 eV shown in Figure 8.2. However, RT E_g values of lattice-matched InGaP up to 1.91eV have been reported.[14]

$$E_g(In_{1-x}Ga_xP) = 1.35 + 0.649x + 0.78x^2 \qquad \text{Equation 8.1}$$

From the LT PL we find that the high intensity peak energy is 1.970 eV. The secondary peak energy is 1.924eV, ~46 meV below the primary peak. Similar secondary peaks (located ~ 30-60 meV below the main transition) have been identified in other InGaP studies and have been attributed to a D-A transition [15] or an indirect transition induced by spatially separated partially ordered InGaP regions [16]. The InGaP ordering

mentioned above refers to the ordering of In and Ga atoms on the Group III sub-lattice and results in a decreased InGaP bandgap for the same InGaP chemical composition and lattice constant. Although, this was not considered a significant issue for SSMBE compared with MOCVD, some reports have concluded that some ordering (23% to 40%) is present for SSMBE films grown at elevated temperatures or low P:III ratios.[3] Yoon et al. found that the degree of ordering may decrease with decreasing substrate since the LT (10K) peak energy increased from 1.94 to 1.97 eV with an decrease in growth temperature from 500°C to 440°C. Yoon et al. also reported that increasing P:III ratios from 10:1 to 50:1 resulted in increase in LT PL peak energy from 1.94 to 1.97 eV.[17] However, since the 19K PL peak energy in Figure 8.2b is ~1.970 eV, a low degree of ordering is expected in SSMBE films grown for this thesis.

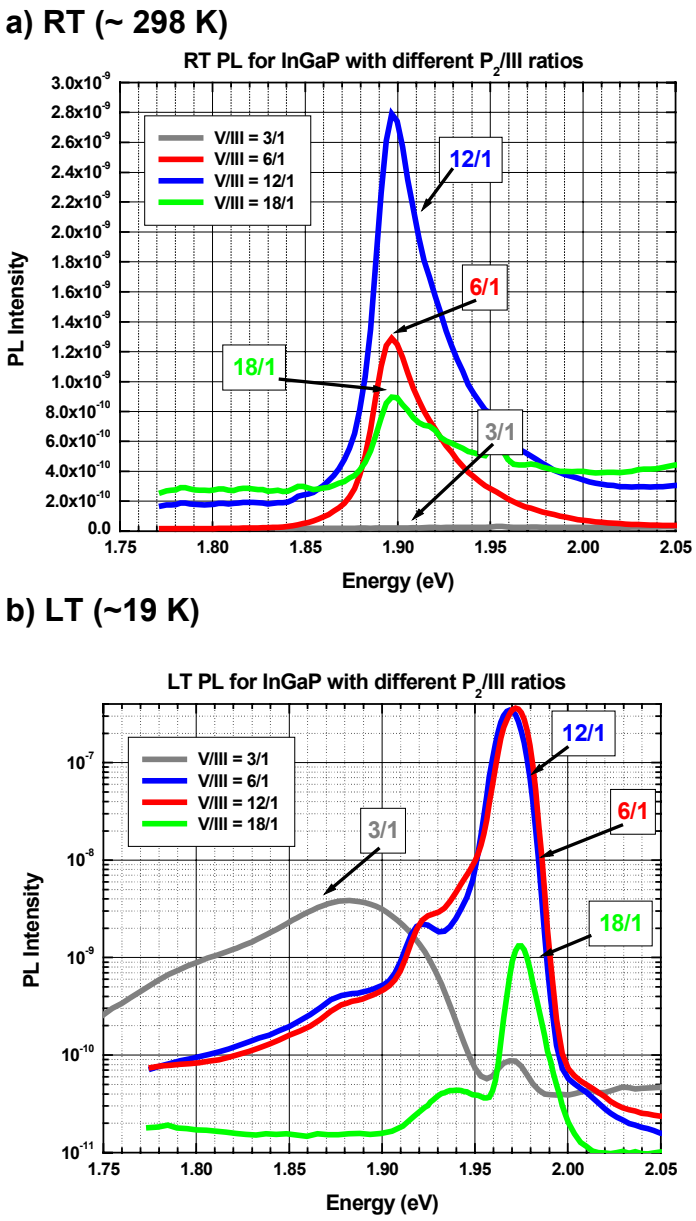


Figure 8.2: a) Room temperature (RT) photoluminescence (PL) and b) low temperature (LT) PL measured at 19K for unintentionally doped InGaP layers grown with varying P_2:III BEP ratios.

8.1.4 Alloy Composition

Unlike GaAs where only the growth rate, not the chemical composition, can drift due to changes in the Ga flux, achieving the proper InGaP composition requires that both the Ga flux and In flux have the proper ratio. Figure 8.3 shows double crystal x-ray diffractions (DCXRD) scans measured for ~ 1.7 μm thick InGaP layers grown on GaAs substrates. These scan were performed perpendicular to the wafer off-cut so that the peak splitting is representative of the lattice mismatch. Sample I was the first sample grown in a series of 4 samples (I, II, III, VI) grown consecutively with the same Ga and In source temperatures. The XRD data indicates that sample I was Ga rich (51.8%) since it had a smaller lattice constant when compared with GaAs. As consecutive samples were grown and Ga and In are consumed from the sources, the flux from the cells changes such that sample IV is Ga poor (51.2%). The amount of mismatch associated with these samples would cause the PL peak energy at RT to shift from 1.895 eV to 1.886 eV, a change of ~ 9 meV. Based on this data, the InGaP fluxes are ideally measured before each growth in order to avoid drifts in InGaP composition. We were also able to obtain InAlGaP compositions using the methods described in Appendix A, validating the assumption that In, Al, and Ga, atoms have a unity sticking coefficient under these growth conditions.

8.1.5 Dopant concentrations

The carrier concentration measured in InGaP layers grown by SSMBE generally followed the same dopant calibration curves measured for GaAs layers grown by SSMBE. The dopant calibrations curves were generated by plotting the carrier concentration measured by electro-chemical capacitance voltage (ECV) versus dopant

source temperature. However, the p-type carrier concentration in InGaP deviated from that measured in GaAs at doping levels lower than ~$1x10^{17}$ cm^{-3}. As shown in Figure 8.4a, a target doping of ~$6x10^{16}$ cm^{-3} from the GaAs calibration curve resulted in an InGaP layer that was fully depleted and based on the layer thickness the doping was less than $1x10^{16}$ cm^{-3}. It is suspected that either an oxygen related defect, a point defect, or other another impurity related defect is causing compensation p-type InGaP layers. Therefore, the GaAs calibration can be used above ~ $1x10^{17}$ cm^{-3}; however, below this level it is difficult to attain a reproducible InGaP carrier concentration. Such problems were not found in n-type InGaP where predictable doping levels as low as $6x10^{16}$ cm^{-3} have been measured. To date, highly doped InGaP (~ $1x10^{19}$ cm^{-3}), capable of producing a wide bang gap tunnel junction have not been achieved. Early investigations were limited by the lack of source material in the Be dopant source and such investigation are just now being restarted. The investigations of InAlGaP and AlInP doping calibration curves have been limited by reliable methods for measuring carrier concentrations by ECV or Hall effect. Instead, calibration growths at the doping levels needed for the solar cell structures are measured by Schottky barrier (Hg-probe) capacitance-voltage (CV) measurement. These calibration indicate that carrier concentrations of 1-$2x10^{18}$ cm^{-3} have been achieved for both p-type and n-type material.

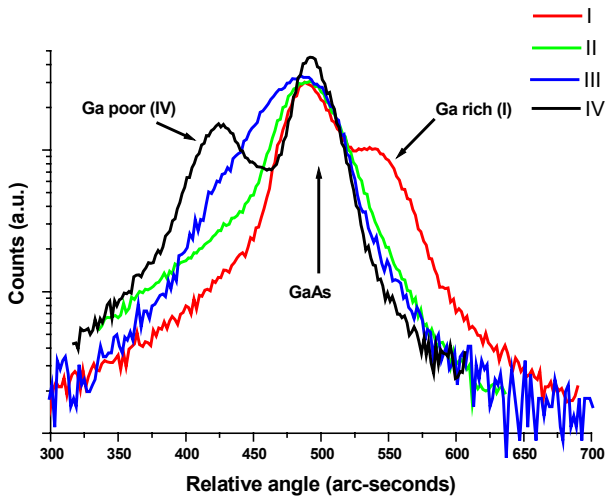


Figure 8.3: Variation in InGaP composition with growth time due to increased depletion of the Ga source compared with the In source. The range of $In_{1-x}Ga_xP$ shown are x = 51.8% to 51.2%.

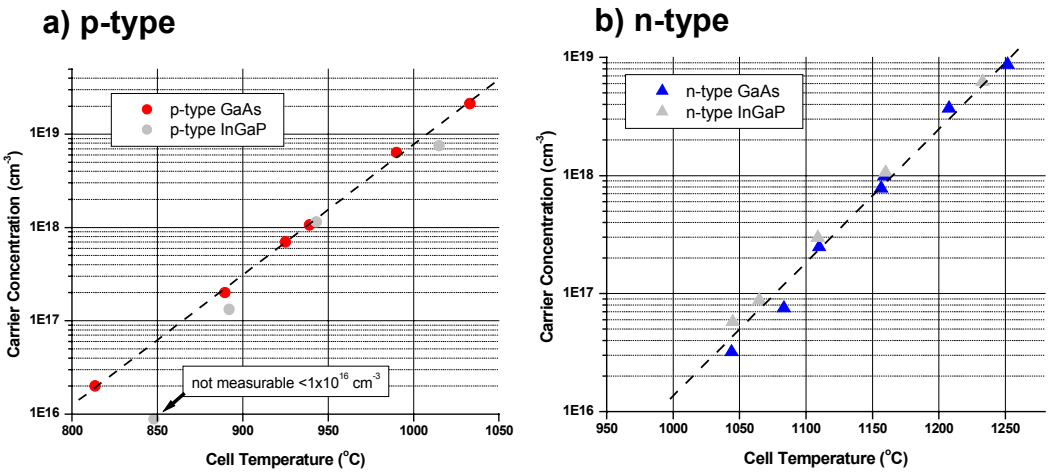


Figure 8.4: InGaP and GaAs a) p-type and b) n-type doping calibration curves.

8.2 $In_{0.49}Ga_{0.51}P$ solar cells

8.2.1 Literature survey

In order to investigate the device polarity dependence of InGaP single junction (SJ) and InGaP/GaAs dual junction (DJ) solar cells as a function of TDD in Chapter 9 and Chapter 10, respectively, high quality homoepitaxial n+/p and p+/n InGaP SJ solar cells are required. Researchers at the National Renewable Energy Laboratory (NREL), using metal organic chemical vapor deposition (MOCVD), published the first SJ InGaP and InGaP/GaAs DJ solar cell devices in 1985 [18] and published the first high efficiency result in 1990 [19]. With further improvements in InGaP material quality, device design, and solar cell grid design, researchers at NREL achieved a record efficiency (29.5% for AM1.5-G) for a dual junction cell in 1994 [20], overtaking the record held by an AlGaAs/GaAs DJ solar cell (27.6% for AM1.5-G) [21]. This established InGaP/GaAs as the material system of choice for high efficiency multi-junction III-V solar cell devices. The majority of research performed at NREL was focused on the n+/p device polarity; their major findings include the use of disordered InGaP as a BSF layer for high V_{oc} values, the use of a high purity phosphine source and the use of a phosphine purifier was critical to good current carrier collection, and that the InGaP top cell thicknesses for use in InGaP/GaAs DJ cell structures should be ~ 0.6 μm for AM0 illumination and ~0.7 μm for AM1.5-G illumination.[20] It took NREL over 10 years to develop high performance devices, and as such, it was expected that the InGaP top cell could pose a significant challenge to the realization of high performance InGaP /GaAs DJ on GaAs and SiGe substrates grown by SSMBE.

NREL's success, prompted development of MOCVD grown InGaP/GaAs DJ solar cells of both polarity devices by commercial vendors, such as Tecstar (p+/n) and Spectrolab (n+/p), in the early 1990's; since this work was part of commercial solar cell development, there were no published details pertaining to the exact dopant concentrations or the thickness of device layers.[22, 23, 24, 25] Other academia based research groups focusing on high performance PV devices studied the InGaP top cells and wide bandgap tunnel junctions in the mid to late 1990's; Takamoto et al. studied the InGaP top cell as grown by MOCVD [26] and Pessa et al. studied GSMBE and SSMBE of the InGaP top cell [27]. Both of these research groups used $In_{0.47}Al_{0.53}P$ (InAlP) BSF and window layers and focused device optimization on the n+/p device polarity, exclusively. Only three reports have been published which show p+/n device structure details, and all efforts have low device performance and use emitter layers with thicknesses of 0.2μm, 0.3μm, and 0.17 μm for Ref. 28, Ref. 29, and Ref. 30, respectively. The main limitation in p+/n InGaP cell development was the production of high quality, highly doped p-type InAlGaP or InAlP material for use as a window layer. Even commercial DJ and triple junction (TJ) solar cells solar cells grown by Tecstar employ a p-type AlGaAs window layer for the InGaP top cell, in order to achieve high performance p+/n devices.[24] It should also be noted that most recent advancements in InGaP cell performance are reported for triple junction solar cells. This is because the TJ solar cell technology (InGaP/GaAs/Ge) has gained prominence in the market place by virtue of the fact that higher efficiencies are obtained with no added processing costs.

8.2.2 Annealing comparison

Based on this literature survey, an n+/p and a p+/n InGaP solar cell device structure was designed. The n+/p device mimicked the structure and doping concentrations presented by Takamoto et al. [26] and is shown in Figure 8.5a; although, $In_{0.47}(Al_{0.7}Ga_{0.3})_{0.53}P$ layers were used for the windows and BSF layers. The p+/n design was based on the total InGaP cell thickness of 0.6 μm, consistent with the n+/p design, and the emitter thickness used by Rafat et al. [28]; this structure is shown in Figure 8.5b. Note that the n-type emitter of the n+/p device is 0.05μm where as the p-type emitter in the p+/n device is 0.2μm. Also note that a highly doped InGaP BSF layer was used after the base but before the InAlGaP BSF layer; this bi-layer BSF scheme was used by Takamoto et al. who found that improved minority carrier reflection is obtained compared with a single layer BSF design.[26] The $In_{0.49}Ga_{0.51}P$ and $In_{0.47}(Al_{0.7}Ga_{0.3})_{0.53}P$ layers were grown at a rate of ~ 1.15 μm/hr, a growth temperature of 490°C, and a P_2:III BEP ratio of 6:1 with reference to the In BEP.

After growth, the substrates were cleaved into pieces, so that one of the pieces could be annealed. The annealing of the solar cell structure was motivated by recent studies by Dekker et al., who found that ex-situ annealing of InGaP quantum wells grown by SSMBE increased PL intensities and the TRPL decay constants.[31] The optimum annealing conditions reported by Ref. 31 were rapid thermal annealing (RTA) at a temperature of 875 °C for 1 s. Before annealing, the solar cell device structures were protected with ~ 2000A of SiN_4 to prevent desorption of As or P from the surface of the samples during the anneal. The samples were ramped up to 875°C ramp in 20 s with N_2

ambient and then ramp down to 500°C in 20 s at which point the furnace power was terminated and the sample was allowed to cool to room temperature. Both the as-grown and annealed samples from the same SSMBE growth were then fabricated into solar cells in the manner outlined in Appendix D and the solar cell device performances were compared.

n++ GaAs contact layer (1000Å)	~1 x10^{19}
n+ $In_{0.49}(Al_{0.7}Ga_{0.3})_{0.51}P$ window (300 Å)	~4 x10^{18}
n+ $In_{0.49}Ga_{0.51}P$ emitter (500 Å)	~2 x10^{18}
p $In_{0.49}Ga_{0.51}P$ base (5500 Å)	~5 x10^{16}
p+ $In_{0.49}Ga_{0.51}P$ back surface field (300 Å)	~2 x10^{18}
p+ $In_{0.49}(Al_{0.7}Ga_{0.3})_{0.51}P$ BSF (300 Å)	<2 x10^{18}
p+ GaAs buffer (3000 Å)	~2 x10^{18}
p+ GaAs substrate	-

a) n^+/p InGaP solar cell device structure

p++ GaAs contact layer (1000 Å)	~1x10^{19}
p+ $In_{0.49}(Al_{0.7}Ga_{0.3})_{0.51}P$ window (300 Å)	<4 x10^{18}
p+ $In_{0.49}Ga_{0.51}P$ emitter (2000 Å)	~2 x10^{18}
n $In_{0.49}Ga_{0.51}P$ base (4000 Å)	~1.5 x10^{17}
n+ $In_{0.49}Ga_{0.51}P$ back surface field (300 Å)	~2 x10^{18}
n+ $In_{0.49}(Al_{0.7}Ga_{0.3})_{0.51}P$ BSF (300 Å)	~2 x10^{18}
n+ GaAs buffer (3000 Å)	~2 x10^{18}
n+ GaAs substrate	-

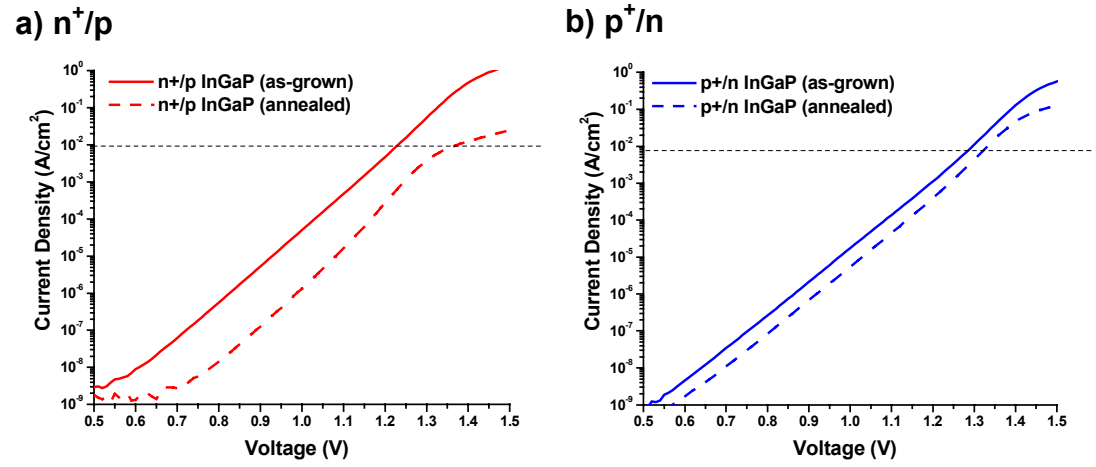
b) p^+/n InGaP solar cell device structure (thick emitter)

Figure 8.5 InGaP SJ solar cell structures used in the as-grown and annealed device performance comparison for a) n+/p and b) p+/n polarity devices.

The base doping for these diode/solar cell structures were estimated by measuring the capacitance-voltage profile using a Boonton 7200 C-V meter. The base doping level measured by CV were ~5x10^{16} cm^{-3} for n+/p diodes and ~1.5x10^{17} cm^{-3} for p+/n diodes. The low doping of the p-type base layer resulted from dopant compensation at low doping levels in p-type InGaP that was discussed in Section 8.1.5. CV measurements were also performed on the annealed diodes to see if the annealing changed the carrier concentration in the base layer. These measurements showed that there was no change in carrier concentration in either the n+/p or p+/n devices. (It may be necessary to perform

ECV measurements on as-grown and annealed structures to profile the carrier concentrations a function of depth, to determine if there was a significant redistribution or activation of dopant atoms in other device layers.)

Figure 8.6 shows the DIV curves and diode performance parameters for as-grown and annealed n+/p and p+/n InGaP diodes. The DIV curves were measured in a Signatone dark box with a Keithley 2400 digital source meter with a current detection limit of 0.1 nA. Because the reverse saturation current density is lower than the detection limit of the current meter used, only the DIV data from 0.5 V to 1.5 V is presented. The series resistance causes the DIV curve to roll off at high voltages and appears to be more significant in the annealed device compared with as-grown device. In both cases the reverse saturation current density for the annealed devices are lower than the as-grown devices. Based on the device models presented in previous chapters, an increase in minority carrier lifetime should result in a decrease in J_{o2} values. This is consistent with Ref. 31, which showed an increase in InGaP lifetime with annealing and with PL measurements performed on the as-grown and annealed samples which showed and increase in luminescence intensity. The lower J_o values also indicate that higher open-circuit voltages (V_{oc}) are expected for annealed devices.



n+/p	J_{o1} (A/cm^2)	n	J_{o2} (A/cm^2)	n
as-grown	-	-	~1x10^{-14}	1.7
annealed	~2x10^{-19}	1.3	~1x10^{-16}	1.7

p+/n	J_o (A/cm^2)	n
as-grown	~1.5x10^{-14}	1.85
annealed	~4x10^{-15}	1.85

Figure 8.6 DIV curves for a) n+/p and b) p+/n InGaP diodes in the as-grown and annealed condition. The embedded tables show the extracted diode performance characteristics.

The solar cell performance for these InGaP solar cells were measured at OSU using a Xenon ARC lamp with a calibrated intensity based on the short circuit current density (J_{sc}) of a InGaP reference solar cell measured at NASA Glenn Research Center for the AM0 spectrum. Figure 8.7 shows the LIV curves for each device. Note that these devices have not been coated with an anti-reflective coating (ARC) and thus the measured J_{sc} values cannot be compared to directly to the values of high performance devices presented in other references. A typical J_{sc} value for a high performance InGaP/GaAs DJ solar cell with an ARC and metal coverage of ~2% is ~16 mA/cm^2 (AM0) [19, 23, 25]; thus if we account for the lack of an ARC and a metal coverage of ~10% for the cell data presented in this chapter, a measured J_{sc} of ~ 11 mA/cm^2 is expected to correspond to "high performance" carrier collection. The LIV curves show

that for both polarity device, annealing the InGaP cell structures increased the carrier collection (J_{sc}), specifically J_{sc} increased by a factor of 1.15 for n+/p cells and by a factor of 1.26 for p+/n cells. The increase in J_{sc} coupled with the lower J_o values, shown by the DIV curves of Figure 8.6, serve to increase the open circuit voltages (V_{oc}) in the annealed solar cells compared with the as-grown solar cells. The improved carrier collection suggests longer minority carrier diffusion lengths / lifetimes and perhaps passivated interfaces. A comparison of the external quantum efficiencies (EQE) curves for as-grown and annealed n+/p solar cells is shown in Figure 8.8a, and describes the carrier collection efficiency as a function of photon wavelength for each device. The carrier collection in the base of the n+/p device is enhanced by annealing, which is indicated by increased EQE values at long wavelengths. Moreover, the p+/n solar cell EQE data, shown in Figure 8.8b, shows increased collection across the entire spectrum indicating improvement in material quality in both the p-type emitter and the n-type base material. When comparing these cells with high performance devices, we find that the J_{sc} values are lower than expected, as are the V_{oc} values. The V_{oc} of the n+/p devices are much lower, 1.21-1.30 V compared with ~1.35 V indicative of the low base doping concentrations and poor back surface field (BSF) performance.

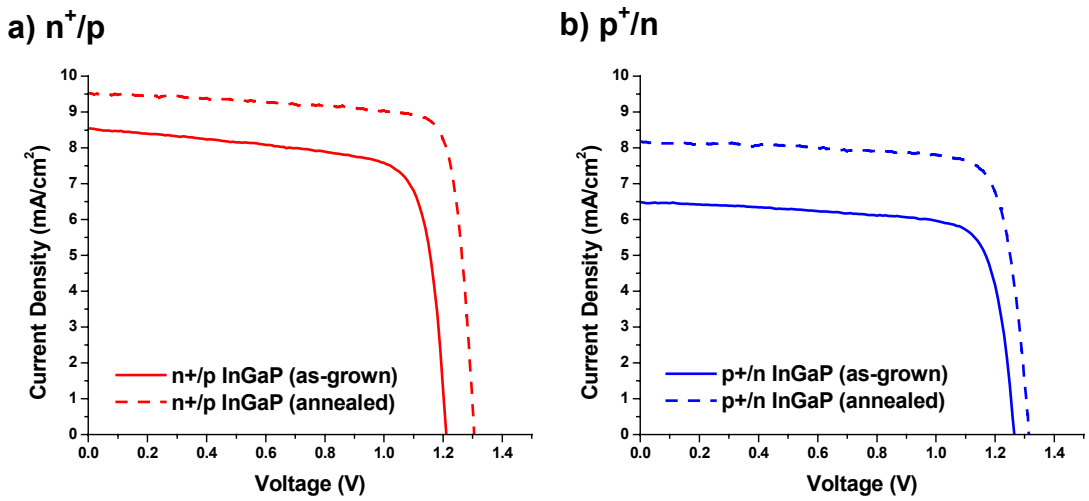


Figure 8.7 LIV curves for as-grown and annealed a) n+/p and b) p+/n InGaP solar cells grown on GaAs substrates.

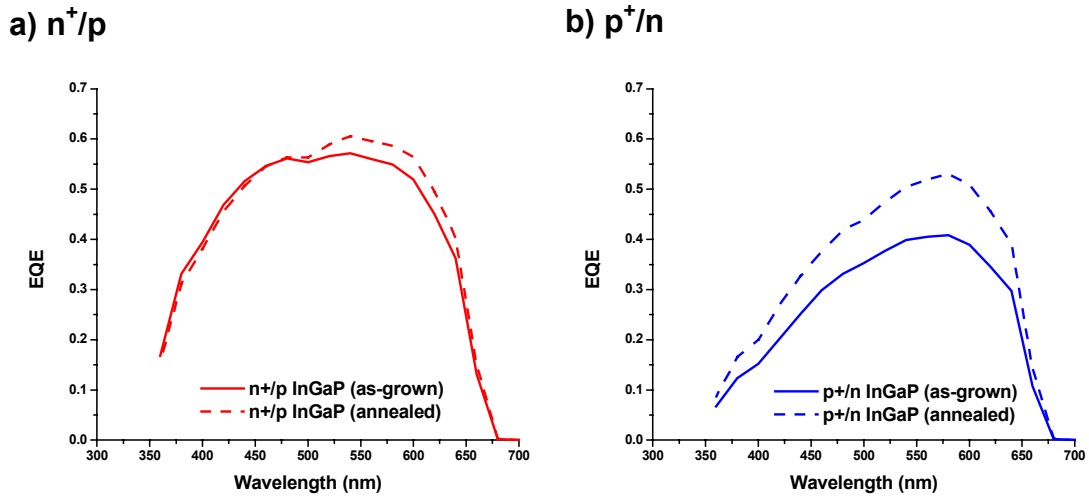


Figure 8.8 EQE curves for as-grown and annealed a) n+/p and b) p+/n InGaP solar cells grown on GaAs substrates.

8.2.3 Cell design comparison

Based on the results from the previous section, a solar cell design change was investigated for both the n+/p and p+/n device structures. The new device structures are shown in Figure 8.9 with the changed device parameters denoted in bold text. The n+/p design was modified by an increase in the base doping value, in an attempt to increase V_{oc} values. In an attempt to improve J_{sc} values, the p+/n device was modified by decreasing the emitter thickness to 500Å, consistent with the n+/p design, while keeping the total cell thickness of 0.6 μm. SSMBE growth conditions for these structures are consistent with those presented in Section 8.2.2, except for the fact that a P_2:III flux ratio of 9:1 was used in these growths; however, based on recent results this change is not expected to have a significant impact on carrier collection [32]. These devices were processed in the as-grown condition in order to examine the InGaP cell performance attained without ex-situ annealing.

n++ GaAs contact layer (1000Å)	~1 x10^{19}
n+ $In_{0.49}(Al_{0.7}Ga_{0.3})_{0.51}P$ window (300 Å)	~4 x10^{18}
n+ $In_{0.49}Ga_{0.51}P$ emitter (500 Å)	~2 x10^{18}
p $In_{0.49}Ga_{0.51}P$ base (5500 Å)	**~2 x10^{17}**
p+ $In_{0.49}Ga_{0.51}P$ back surface field (300 Å)	~2 x10^{18}
p+ $In_{0.49}(Al_{0.7}Ga_{0.3})_{0.51}P$ BSF (300 Å)	<2 x10^{18}
p+ GaAs buffer (3000 Å)	~2 x10^{18}
p+ GaAs substrate	-

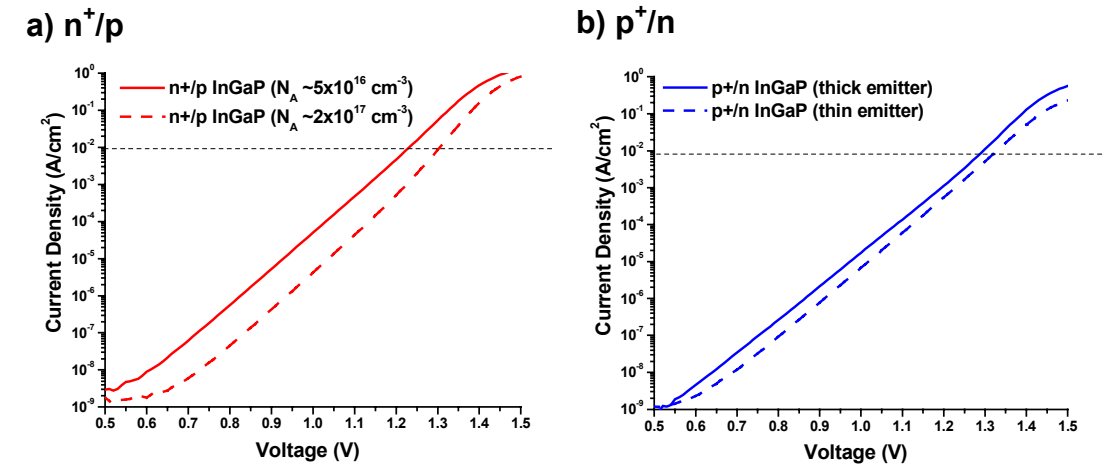
a) n^+/p InGaP solar cell with higher base doping

p++ GaAs contact layer (1000 Å)	~1x10^{19}
p+ $In_{0.49}(Al_{0.7}Ga_{0.3})_{0.51}P$ window (300 Å)	<4 x10^{18}
p+ $In_{0.49}Ga_{0.51}P$ emitter **(500 Å)**	~2 x10^{18}
n $In_{0.49}Ga_{0.51}P$ base **(5500 Å)**	~1.5 x10^{17}
n+ $In_{0.49}Ga_{0.51}P$ back surface field (300 Å)	~2 x10^{18}
n+ $In_{0.49}(Al_{0.7}Ga_{0.3})_{0.51}P$ BSF (300 Å)	~2 x10^{18}
n+ GaAs buffer (3000 Å)	~2 x10^{18}
n+ GaAs substrate	-

b) p^+/n InGaP solar cell with a thin emitter

Figure 8.9 InGaP single junction solar cell structures used in the device design performance comparison for a) n+/p and b) p+/n polarity devices.

The DIV curves for these new structures are compared with DIV curves for the as-grown device structures shown in Figure 8.5. It is clearly evident that an increase in the base doping for the n+/p diode significantly reduced the reverse saturation current density. This results from reductions in both J_{o2} and J_{o1} with increasing base doping. A decrease in J_o for the p+/n device is also shown, although, this was not necessarily expected. This reduction in J_o may result from an increase in the bandgap of InGaP (increased Ga), general improvements in material quality, or changes in the emitter doping that are not detectable by CV measurements.



n+/p	J_{o1} (A/cm^2)	n	J_{o2} (A/cm^2)	n
lower	~2x10^{-19}	1.3	~1x10^{-14}	1.7
higher	~1x10^{-19}	1.3	~5x10^{-16}	1.7

p+/n	J_o (A/cm^2)	n
thick	~1.5x10^{-14}	1.85
thin	~2.5x10^{-15}	1.80

Figure 8.10 DIV curves for a) n+/p and b) p+/n InGaP diodes in the as-grown condition for two different device designs. The embedded tables show the extracted diode performance characteristics.

The LIV curve comparison for these device structures are shown in Figure 8.11. Since the n+/p InGaP solar cell with a higher base doping showed a significant reduction in J_o, substantially higher V_{oc} values were obtained (1.275 V compared with 1.210 V). While an increase V_{oc} was obtained, the increased p-type base doping significantly reduced the number of carriers collected as seen from the measured J_{sc} values (6.56 compared to 8.55 mA/cm^2) and the reduction in EQE values shown in Figure 8.12a. The reduction in J_{sc} also reduces the measured V_{oc}, so that when a J_{sc} of 16 mA/cm^2 is obtained by increased photon flux, the highly doped n+/p device has a V_{oc} of 1.301 V. The n+/p device still exhibits lower V_{oc} values than expected for high quality InGaP solar cells (~1.350 V). Again, this indicates that the BSF in the n+/p device may be limiting the V_{oc} performance as suggested in Ref. 33, which found V_{oc} values of ~1.28 V for an $In_{0.5}(Al_{0.1}Ga_{0.9})_{0.5}P$ BSF layers compared with ~1.35 V for disordered InGaP BSF layers. (Remember high quality p-type InAlGaP is difficult to achieve by both SSMBE and MOCVD.) The reduced emitter thickness for the p+/n device improved the J_{sc} by a factor of 1.26 as intended; this is reflected in the EQE curve shown in Figure 8.12b by an increase in collection efficiency across the entire spectrum. The V_{oc} value was also increased as a result of a lower J_o and a higher J_{sc}. The V_{oc} value for this cell, measured at 16 mA/cm^2 was 1.331 V, which is in reasonable agreement with high performance devices when considering the state of InGaP cell development and that lower J_o values and higher J_{sc} values may be achieved with the annealing of this device structure.

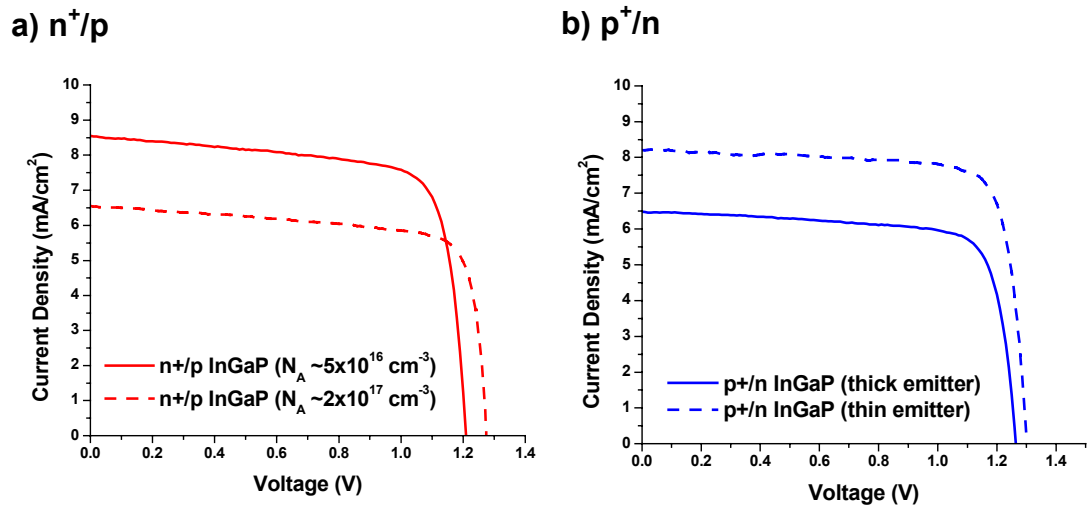


Figure 8.11 LIV curves for a) n+/p and b) p+/n InGaP solar cells in the as-grown condition for two different device designs.

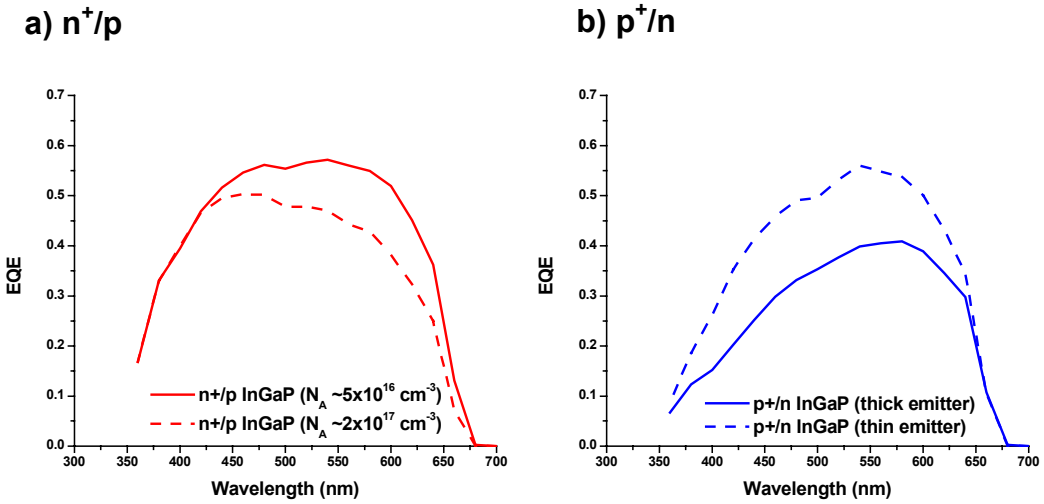


Figure 8.12 EQE curves for a) n+/p and b) p+/n InGaP solar cells in the as-grown condition for two different device designs.

8.2.4 On going investigations

For p+/n solar cell development, it is clear that both annealing of device layers and the thin emitter design significantly improved device performance by decreasing the reverse saturation current and increasing carrier collection. Since J_{sc} values of ~ 11 mA/cm^2 have not yet been reached, efforts to further optimize the p+/n device are still on going. Recent results (to be reported by Lueck et al.) showed that in-situ annealing at 700°C for duration of 5 minutes increased J_{sc} from 8.5 to 9.3 mA/cm^2 in p+/n solar cells with a thin emitter design.[32] While this value is still lower than the desired value, it is higher than any of the p+/n devices reported in this thesis. In-situ annealing of this structure also reduced J_o and thus a V_{oc} of 1.340 V was measured for AM0 illumination, while a V_{oc} of 1.360 mV was measured for a J_{sc} of 16 mA/cm^2. Most importantly, the in-situ annealing technique is applicable to the thermal expansion coefficient mismatched III-V/SiGe material system since it is performed immediately after growth of the GaAs cap layer at ~575°C. In this case the added strain due to thermal expansion occurs only as the substrate is reduced in temperature from ~700°C to room temperature. This is unlike ex-situ annealing by RTA for which the sample is reduced from growth temperature to room temperature which strains the epitaxial film and then subsequent RTA treatment rapidly increases the temperature up to 875°C before returning to room temperature, which adds additional thermal expansion strain. III-V growths on SiGe that have received annealing by RTA have exhibited catastrophic cracking in the III-V epi-layers rendering them unsuitable for device processing. As for n+/p cell development, the p-type material quality of InGaP and the quality of the BSF has inhibited carrier collection and V_{oc} values. Since future work at OSU is focused on high performance p+/n

devices on SiGe that are more robust to elevated TDDs, the n+/p device has not been further optimized to date.

Although improvements in InGaP material quality by optimized growth conditions and in-situ annealing are still needed in order to obtain high performance devices, there are other factors that may also impact the J_{sc} values of these SSMBE InGaP solar cells as well. One such factor is the bandgap (E_g) of the InGaP top cell; other high performance cells grown by MOCVD typically use an InGaP active junction with an E_g of ~1.86 eV compared with InGaP grown by SSMBE which typically has an E_g of ~1.89 eV. The wider bandgap can decrease the number of photons absorbed and thereby reduce J_{sc} values in SSMBE grown InGaP top cells. Although Pessa et al. have shown fully processed devices with J_{sc} values of ~15.2mA/cm^2 for InGaP grown by SSMBE [27], the exact bandgap of this material is not reported.

Another source of carrier loss may result from the use an $In_{0.47}(Al_{0.7}Ga_{0.3})_{0.53}P$ window layer with a E_g of ~2.2 eV for the solar cells presented in this chapter. Other high efficiency reports have used AlInP (~ 2.35 eV) and thus there is lower parasitic absorption in the window layer. In these studies $In_{0.47}(Al_{0.7}Ga_{0.3})_{0.53}P$ layers were used because early studies at OSU suggested that reliable carrier concentrations p-type AlInP could not be obtained. Since these studies were completed, higher purity phosphorus source material has been obtained and the background oxygen levels in the UHV chamber have been lowered such that new studies are needed. The use of the quaternary alloy was not suspected to have a large impact in the SSMBE solar cells discussed in the chapter because $In_{0.49}(Al_xGa_{1-x})_{0.51}P$ is supposed to be indirect at x = 0.7 [34], but may have some impact on carrier collection once the InGaP material quality issues are

resolved. Finally, and optimized BSF layer for a p+/n InGaP solar cell may also increase carrier collection in these SSMBE devices. Friedman et al. found that the BSF of the n+/p InGaP cell was very important for both high performance J_{sc} and V_{oc} values [33]; however, there have been no published studies or studies performed at OSU pertaining to optimization of BSF layers for p+/n InGaP devices.

8.3 Conclusions

The growth parameters used for SSMBE while producing smooth films have not achieved the InGaP material quality or InGaP solar cell performance produced by optimized MOCVD growth. The use of ex-situ rapid thermal annealing produced decreased reverse saturation currents in n+/p and p+/n InGaP diodes with no change in the base-layer carrier concentrations, suggesting improvements in material quality and minority carrier lifetimes. This translated to improved solar cell device performance by increases in both J_{sc} and V_{oc}. Further improvements in carrier collection and V_{oc} were achieved by use of a thin emitter device structure in p+/n InGaP solar cells. However, an increase in base doping for the p+/n device significantly reduced J_{sc} while increasing V_{oc}. As such, the optimization of SSMBE grown InGaP for solar application is the subject of future work at OSU so that high performance dual junction solar cell son SiGe can be developed. Although fully optimized InGaP material and devices have not yet been obtained, the discussion of metamorphic InGaP devices grown on SiGe substrates are described in the next Chapter.

8.4 References

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CHAPTER 9

$In_{0.49}Ga_{0.51}P$ SOLAR CELLS GROWN ON SiGe

Unlike GaAs solar cells, $In_{0.49}Ga_{0.51}P$ (InGaP) solar cells grown by SSMBE at OSU are still at an early stage of development. As such, the short-circuit current density, J_{sc}, values are ~85% of the value obtained for high performance commercially manufactured cells, while the V_{oc} values are only slightly lower (~ 95%) than high performance cell values. This lower InGaP material quality for homoepitaxial devices complicates the study of InGaP material parameters and solar cell performance as a function of threading dislocation density (TDD) and makes the extraction and comparison of bulk lifetimes impractical. Instead, InGaP solar cells were grown on SiGe substrates and compared with cells grown on GaAs in order to determine the impact of higher TDDs on InGaP device performance. These device results may then provide information concerning the affects of TDs on InGaP material parameters.

In Section 9.1, the solar cell device structures for both n+/p and p+/n InGaP solar cells are presented. The TDD dependant lifetime/diffusion length model is incorporated into the "standard" diode/solar cell device models for dark and light current density versus voltage characteristics (DIV and LIV). Thus, the theoretical impact of TDD on

the reverse saturation current components, J_{o1} and J_{o2}, and V_{oc} is quantified. The experimental DIV curves for both n+/p and p+/n InGaP solar cells grown on GaAs and SiGe are examined in Section 9.2. These cells were grown, processed, and measured in order to examine the validity of the proposed models for both n+/p and p+/n InGaP devices. Finally, the LIV curves for InGaP solar cells are presented in Section 9.3. AM0 performance indicates that the TDD does not hinder carrier collection at this state of material development and that InGaP solar cells appear more TDD tolerant than GaAs solar cells.

9.1 Threading dislocation density and $In_{0.49}Ga_{0.51}P$ device models

In Chapter 4 the "standard" solar cell IV models were discussed in detail. These models depend on the thickness and dopant concentration of device layers as well as other material parameters. As shown in Chapter 6, the behavior of both the minority carrier lifetime and diffusion length as a function of threading dislocation densities (TDDs) can be modeled with all other material parameters fixed. Thus, both L(TDD) in Equation 9.1 and τ(TDD) Equation 9.2 are incorporated into the IV models for InGaP single junction solar cells with an n+/p and a p+/n device polarity. In this chapter we will consider the full diode expression including diffusion and recombination components to the reverse saturation current, but a voltage independent depletion width. Moreover, since references for all the needed InGaP material parameters are not available in published literature, the parameters selected for use in this model are discussed below.

$$\frac{1}{L^2} = \frac{1}{L_{\max}^2} + \frac{\pi^3 [TDD]}{4} \qquad \text{Equation 9.1}$$

$$\frac{1}{\tau} = \frac{1}{\tau_{\max}} + \frac{\pi^3 D[TDD]}{4} \qquad \text{Equation 9.2}$$

The device structures and the modeling input parameters used in this chapter are shown in Figure 9.1 and Table 9.1. From the GaAs model developed in Chapters 6 and 7, it is clear that the minority carrier diffusion coefficients and the minority carrier lifetimes for electron and holes are important parameters when considering the impact of elevated TDDs. Since there are no published values for minority carrier diffusion coefficients in InGaP, the majority carrier mobilities as a function of dopant concentration reported in Ikeda et al. were used to approximate these values.[1] The values extracted from this reference were similar to the GaAs material parameters, in that D_n decreased by a factor of ~3 from a doping concentration of $1.5\text{x}10^{17}$ cm^{-3} to a doping concentration of $2\text{x}10^{18}$ cm^{-3} and D_p did not change significantly for this doping range. Unlike GaAs, the InGaP diffusion coefficients are significantly lower (~23.5 cm^2/s compared to ~78 cm^2/s for electrons) which will have an impact on modeling results. The minority carrier lifetime for n-type and p-type InGaP are not well established, although references suggest that the band-band radiative coefficient, B, for InGaP is consistent with GaAs (~ $2\text{x}10^{-10}$ cm^3/s)[2]. However, the measured InGaP lifetimes are lower than the values suggested by B, and it is not clear whether, in the state of the art InGaP material, electron and hole lifetimes are equivalent. For electrons in p-type InGaP with a doping concentration of ~ $0.7\text{-}1.5\text{x}10^{17}$ cm^{-3}, device analysis by Yang et al. [3] suggested τ_n values of 5-10 ns were obtained, while King et al. [4] measured a τ_n of >2 ns. Based on these values and the fact that τ = 7.5 ns resulted in modeled V_{oc} values consistent with InGaP solar cell performance, 7.5 ns was used in the device model for

both the minority carrier electron and hole lifetimes. The fact that these material parameters (D and τ) are not well established may impact how successfully this model describes the experimental results.

The surface recombination velocities (S) measured by King et al. for an n+/p InGaP cell design were ~$8x10^4$ cm^2s^{-1} and ~$1.3x10^5$ cm^2s^{-1} for the emitter and base, respectively. These S vlaues are also consistent with results extracted from IV analysis by Yang et al. for n+/p InGaP solar cells; therefore, a value of $1x10^5$ cm^2s^{-1} was used in the device models for both S_n and S_p in n+/p and p+/n InGaP solar cells. A discrepancy in the intrinsic carrier concentration values (n_i) for InGaP found in the literature arises from the variability of the InGaP bandgap depending on the degree of ordering in the material. Since MBE grown material generally has little ordering, an InGaP bandgap of 1.9 eV and the corresponding n_i value of 705 cm^{-3} (based on Ref. 5) will be used in this chapter. A relative dielectric constant of 11.8 was also used based on Vegard's Law and Ref. 6. The solar cell structures used in the model are consistent with the devices discussed in Chapter 8, with a thin emitter design used for both polarity devices, and with high performance n+/p dual junction solar cells, with InGaP top cells.[7, 8]

n++ GaAs contact layer (1000 Å)	~1 $x10^{19}$
n+ $In_{0.49}(Al_{0.7}Ga_{0.3})_{0.51}P$ window (300 Å)	~4 $x10^{18}$
n+ $In_{0.49}Ga_{0.51}P$ emitter (500 Å)	~2 $x10^{18}$
p $In_{0.49}Ga_{0.51}P$ base (5500 Å)	~1.5 $x10^{17}$
p+ $In_{0.49}Ga_{0.51}P$ BSF (300 Å)	<2 $x10^{18}$
p+ $In_{0.49}(Al_{0.7}Ga_{0.3})_{0.51}P$ BSF (300 Å)	<2 $x10^{18}$
p+ GaAs buffer (3000 Å)	~2 $x10^{18}$
substrate	-

a) n^+/p InGaP solar cell device structure

p++ GaAs contact layer (1000 Å)	~1x10^{19}
p+ $In_{0.49}(Al_{0.7}Ga_{0.3})_{0.51}P$ window (300 Å)	<4 $x10^{18}$
p+ $In_{0.49}Ga_{0.51}P$ emitter (500 Å)	~2 $x10^{18}$
n $In_{0.49}Ga_{0.51}P$ base (5500 Å)	~1.5x10^{17}
n+ $In_{0.49}Ga_{0.51}P$ BSF (300 Å)	~2 $x10^{18}$
n+ $In_{0.49}(Al_{0.7}Ga_{0.3})_{0.51}P$ BSF (300 Å)	~2 $x10^{18}$
n+ GaAs buffer (3000 Å)	~2 $x10^{18}$
substrate	-

b) p^+/n InGaP solar cell device structure

Figure 9.1 Device structures for a) n+/p and b) p+/n InGaP solar cells.

a) InGaP n+/p modeling parameters

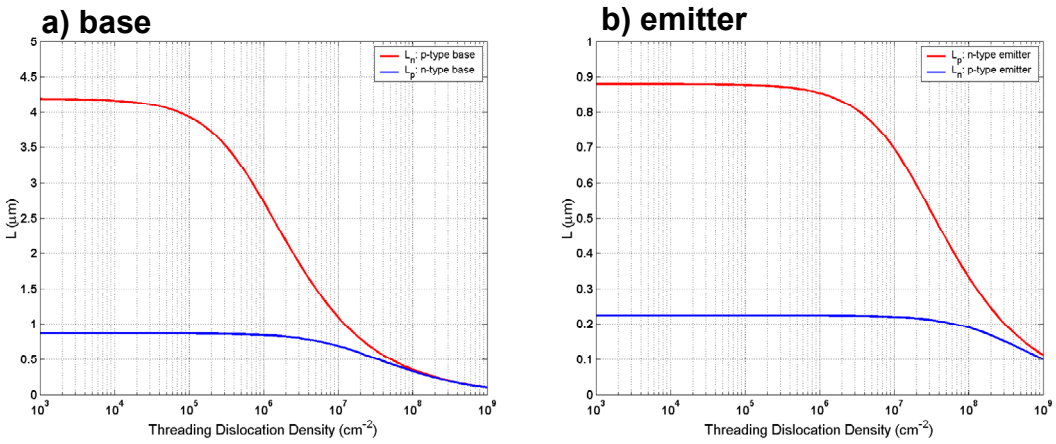
Parameters	Model
D_n (cm^2s^{-1}) ($1.5x10^{17}$ cm^{-3})	23.5
D_p (cm^2s^{-1}) ($2x10^{18}$ cm^{-3})	1
τ_n (ns) ($1.5x10^{17}$ cm^{-3})	7.5
τ_p (ns) ($2x10^{18}$ cm^{-3})	0.5
L_n (μm) ($1.5x10^{17}$ cm^{-3})	4.20
L_p (μm) ($2x10^{18}$ cm^{-3})	0.22

b) InGaP p+/n modeling parameters

Parameters	Model
D_n (cm^2s^{-1}) ($2x10^{18}$ cm^{-3})	15.5
D_p (cm^2s^{-1}) ($1.5x10^{17}$ cm^{-3})	1
τ_n (ns) ($2x10^{18}$ cm^{-3})	0.5
τ_p (ns) ($1.5x10^{17}$ cm^{-3})	7.5
L_n (μm) ($2x10^{18}$ cm^{-3})	0.88
L_p (μm) ($1.5x10^{17}$ cm^{-3})	0.87

Table 9.1: InGaP minority carrier properties for a) n+/p and b) p+/n InGaP diode structures used in the InGaP device model.

Because the InGaP solar cell will be used as the top cell in a dual junction solar cell, the total cell thickness is only ~0.6 μm. As such the minority carriers generated in the base need only to diffuse less than ~ 0.55 μm in order to be collected. Figure 9.2 shows the expected diffusion lengths based on the assumed D and τ values presented in Table 9.1 and Equation 9.1. Although this figure suggests that both carriers in the emitter and base of both polarity devices should easily be collected, InGaP cell results, presented in Chapter 8, show that carrier collection in the p-type base of the n+/p cells with low TDD were reduced with an increase in base doping from $4x10^{16}$ cm^{-3} to $2x10^{17}$ cm^{-3}, suggesting a reduction in diffusion length. In any case, based the diffusion lengths dependence on TDD, we do not expect to see a difference in J_{sc} for cells grown on GaAs substrates compared with those grown on SiGe substrates.



TDD (cm^{-2})	L_n (μm)	L_p (μm)
0	4.20	0.866
$5x10^5$	3.24	0.854
$1x10^6$	2.73	0.842
$4x10^6$	1.65	0.780

TDD (cm^{-2})	L_n (μm)	L_p (μm)
0	0.880	0.2236
$5x10^5$	0.867	0.2234
$1x10^6$	0.855	0.2232
$4x10^6$	0.790	0.2220

Figure 9.2 Minority carrier diffusion lengths as a function of TDD in the a) base and b) emitter of n+/p and p+/n InGaP solar cells based on the material parameters in Table 9.1.

To account for the impact of TDs on a diodes' IV curve (described by Equation 9.3), the influence of TDs on both J_{o1} and J_{o2} must be determined. We will examine each component individually before modeling the entire DIV (J_{sc}=0) curve for various TDDs.

$$J = J_{o1}\left(\exp\left(\frac{qV}{kT}\right)-1\right)+J_{o2}\left(\exp\left(\frac{qV}{2kT}\right)-1\right)-J_{sc} \qquad \text{Equation 9.3}$$

First we examine the diffusion current, J_{o1}(TDD), for n+/p and p+/n solar cells using Equation 9.4; the results are shown in Figure 9.3a. We find that J_{o1} for an n+/p diode is higher than that of a p+/n diode at low TDD values. This results from the fact that the

base layer of the InGaP diode is relatively thin (0.55 μm), the p-type base of the n+/p diode has a higher diffusion coefficient and a longer minority carrier diffusion length when compared with the n-type base of the p+/n diode, and the surface recombination velocities in the InGaP/InAlGaP material system are relatively high (~ 100,000 cm^2/s). These factors cause an increase in recombination at the back surface filed (BSF) for the n+/p diode compared with the p+/n diode. (This is unlike GaAs solar cell modeling in Chapter 7 where the GaAs had a ~2.5 um base thickness and low surface recombination velocities ~ 1000-3000 cm^2/s produced similar J_{o1} values for n+/p and p+/n devices at low TDD values.) With increasing TDD, the reverse saturation current increases at a faster rate for the n+/p device compared with the p+/n device due to the differences in electron and hole mobility/diffusion coefficients as the diffusion lengths in each device reach the TDD dominated limit, L_{TDD}.

$$J_{o1} = qn_i^2\left(\frac{F_p}{N_A}\left(\frac{D_n}{L_n}\right)+\frac{F_n}{N_D}\left(\frac{D_p}{L_p}\right)\right) \qquad \text{Equation 9.4}$$

Now in wide-bandgap materials, which have low n_i values, depletion region recombination often dominates the total J_o. The depletion region recombination current density component, J_{o2}, is described by Equation 9.5. From this, we find an inverse relationship between J_{o2} and τ_{base}. In Figure 9.3b we plot J_{o2}(TDD) for both n+/p and p+/n InGaP diodes. Because the cells have an identical design and equivalent τ_n and τ_p values were assumed in the absence of TDs, the only difference in J_{o2}(TDD) is the earlier reduction in τ_n of an n+/p diode compared with τ_p of a p+/n diode based on the higher mobility of electrons compared to holes.

$$J_{o2} = \frac{qn_i W_D}{2}\left(\frac{1}{\tau_{base}}\right)$$ Equation 9.5

Comparing these two figures it is clear that at lower voltages, J_{o2} will dominate since it is on the order of 10^{-13} A/cm^2 compared with J_{o1}, which is on the order of 10^{-25} A/cm^2. Because of the higher bandgap (smaller n_i) of InGaP compared with GaAs, InGaP J_o values are generally lower. To determine the voltage regions of dominance for each reverse saturation current component, the DIV curve is calculated using both J_{o1} and J_{o2} components in Equation 9.3 (J_{sc}=0). We plot the DIV curve for five TDD values in Figure 9.4a for n+/p InGaP diodes and in Figure 9.4b for p+/n InGaP diodes. An increase in J_o with TDD is seen in each figure by a shift in the DIV curve to higher current density values. The shift exhibited for an n+/p diode is greater than that exhibited for a p+/n diode for the same change in TDD value. This is a direct result of the fact that J_{o2} values for n+/p diodes begin to increase at lower TDD values compared to p+/n diodes, as shown in Figure 9.3. Also included in this figure, is line representing a typical AM0 InGaP solar cell J_{sc} value (16-17 mA/cm^2) for use in a dual junction solar cell. The intersection of this line with the DIV curve describes the expected V_{oc} value for a solar cell with the corresponding TDD. It is evident that lower open-circuit voltages are expected for n+/p diodes at a given TDD due to increased J_o values. This modeling also shows that the InGaP diode performance is expected to be dominated by J_{o2} at voltages near V_{oc}; however, reports have shown that n=1 region in the vicinity of ~ 1.3 V have been observed in n+/p InGaP solar cell structures.[9] These reports indicate that J_{o1} may be more significant than suggested by this model.

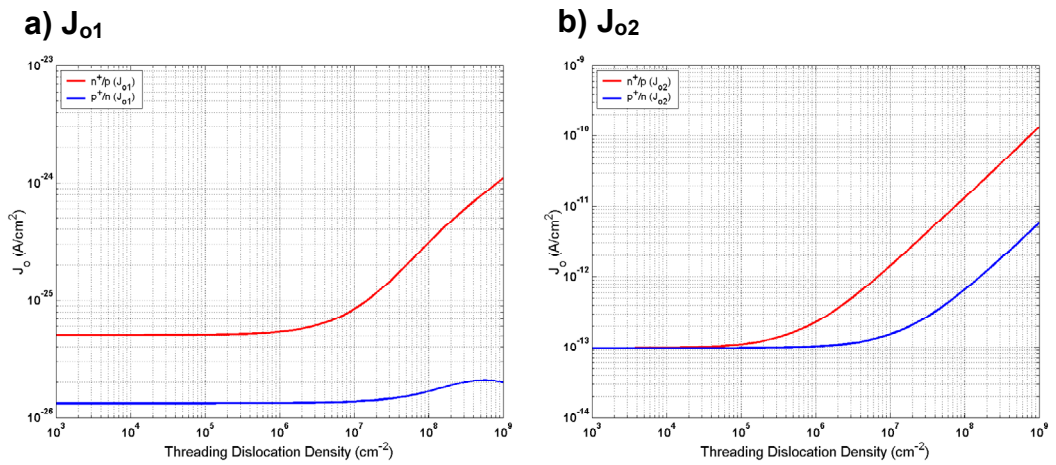


Figure 9.3 The reverse saturation current density as a function of TDD for the a) diffusion component (J_{o1}) and b) depletion region recombination component (J_{o2}) for both n+/p and p+/n InGaP diodes.

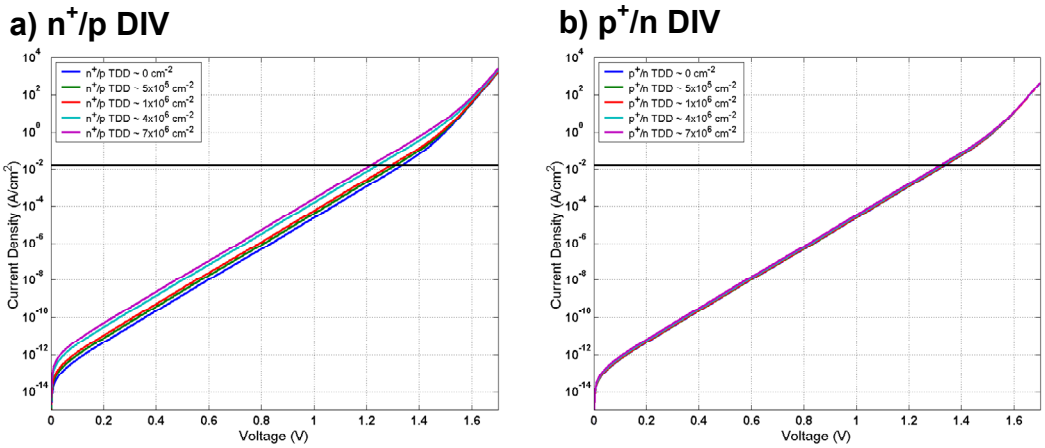


Figure 9.4 Modeled DIV curves for a) n+/p InGaP diodes and b) p+/n InGaP diodes with varying TDDs. The horizontal line in each figure represents a current density of 16 mA/cm^2 indicating the dominance of J_{o2} near V_{oc}.

Figure 9.5 compares V_{oc} values as a function of TDD for n+/p and p+/n InGaP solar cells based on the complete diode model shown in Equation 9.3. The main result is that the V_{oc} values for n+/p devices are expected to be lower than V_{oc} values for p+/n devices for a given TDD. As in the case of GaAs solar cells, this results from the higher recombination rate of electrons compared with holes. By plotting the complete diode model along with the V_{oc}(TDD) calculated using the diffusion component (J_{o1}) and the recombination component (J_{o2}) alone, we find that J_{o2} dominates at V_{oc} when assuming a short circuit current density of 16 mA/cm^2. Since some reports have shown that J_{o1} (n~1) may be dominant near V_{oc}, at least for n+/p InGaP solar cells, these curves represent a range of possible V_{oc} values from ~1.33 V (based on J_{o2}) to 1.43 V (based on J_{o1}) for lower TDD values. However, if the dominance of J_{o1} resulted from an increase in the value of the diffusion component by carrier loss at the BSF, then lower V_{oc} values may also be obtained despite the dominance of J_{o1}. These results are consistent with GaAs solar cell models, where a clear TDD dependence on solar cell performance is predicted and p+/n cells are expected to be more tolerant of high TDDs compared with n+/p cells. Unlike GaAs, the onset of degradation in V_{oc} values for InGaP solar cells occurs at higher TDDs. Figure 9.7 compares remaining fraction of V_{oc} as function of TDD for InGaP and GaAs n+/p solar cells and InGaP and GaAs p+/n solar cells for a J_{sc} value of 16 mA/cm^2. The difference in the onset of V_{oc} degradation results from the lower minority carrier diffusion coefficients for homoepitaxial InGaP (D_n~ 23.5 cm^2/s and D_p~1 cm^2/s) compared with GaAs (D_n~ 78.1 cm^2/s and D_p~7.1 cm^2/s), indicating that InGaP solar cells are more tolerant to TDs compared with GaAs solar cells.

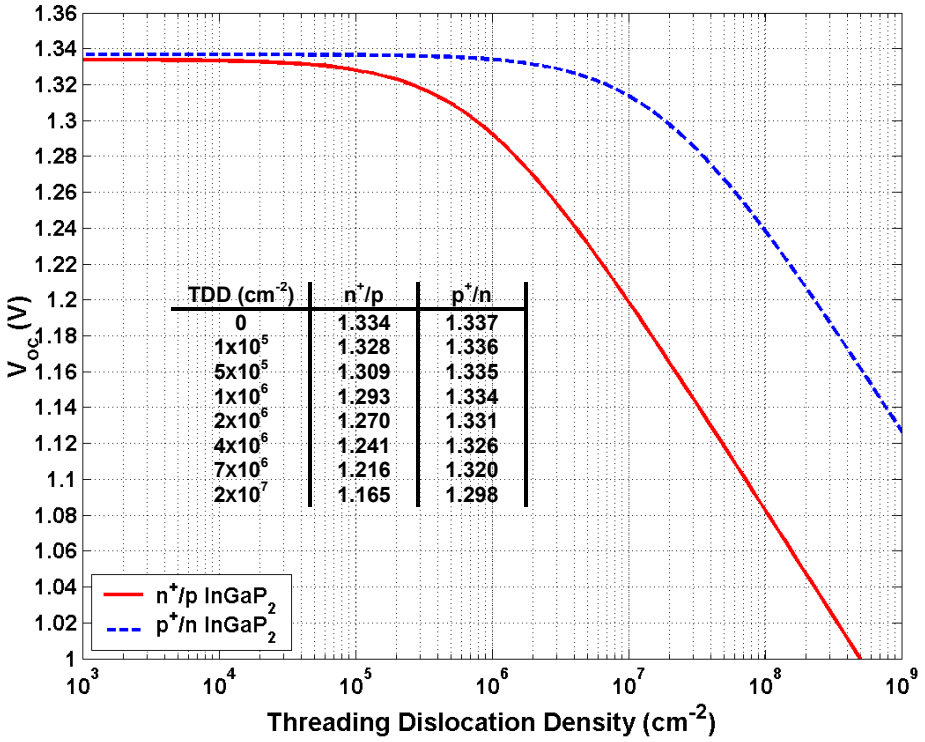


Figure 9.5 Open-circuit voltage (V_{oc}) as a function of TDD for n+/p and p+/n InGaP solar cells, assuming a J_{sc} of 16 mA/cm^2. The embedded table shows V_{oc} values extracted from this plot.

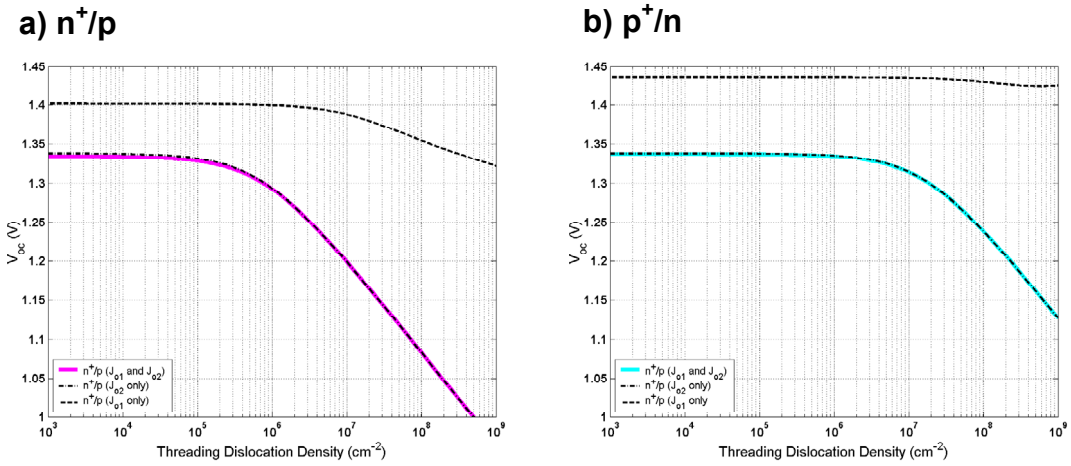


Figure 9.6 Open-circuit voltage (V_{oc}) as a function of TDD for a) n+/p and b) p+/n InGaP solar cells, assuming a J_{sc} of 16 mA/cm^2. Also plotted are V_{oc} (TDD) calculated using the J_{o1} and J_{o2} components individually.

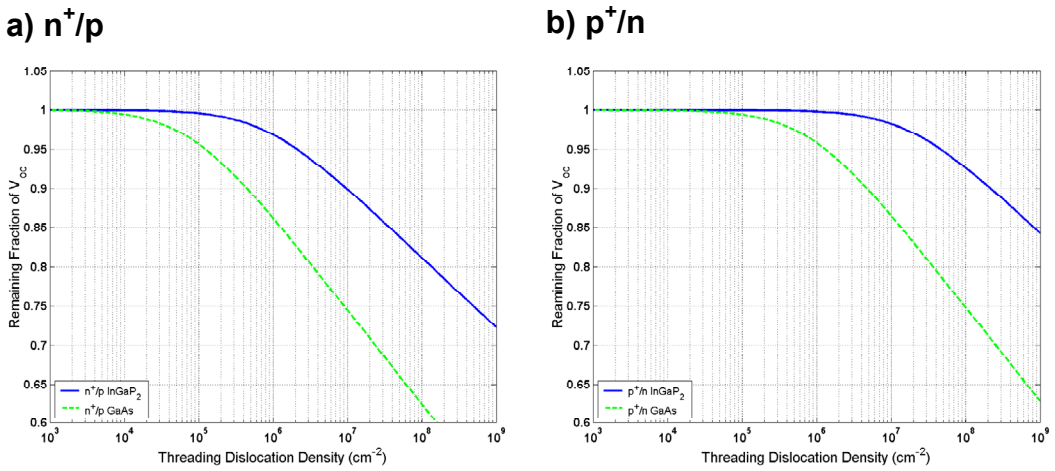


Figure 9.7 Remaining fraction of V_{oc} as function of TDD for GaAs compared to InGaP single junction solar cells with a) n+/p and b) p+/n polarity devices.

9.2 $In_{0.49}Ga_{0.51}P$ on SiGe diode performance

In order to measure the impact of TDD on InGaP diode/solar cell performance, p+/n and n+/p InGaP device structures (shown in Figure 9.1) were grown by solid source molecular beam epitaxy (SSMBE) on a GaAs and SiGe substrates with an (100) orientation and a 6° off-cut toward a {111} plane. GaAs growth initiation on the Ge terminated surface of the SiGe substrate followed the method described in Chapter 2. This process incorporated an epitaxial Ge layer by SSMBE, a GaAs migration-enhanced epitaxy (MEE) layer, and a low-temperature low growth rate GaAs layer, which should produce a GaAs/Ge interface with no anti-phase disorder. The $In_{0.49}Ga_{0.51}P$ and $In_{0.47}(Al_{0.7}Ga_{0.3})_{0.53}P$ layers were grown at a rate of ~ 1.15 μm/hr, a growth temperature of 490°C, and a P_2:III BEP ratio of 12:1 with reference to the In BEP.

For this study, both n-type and p-type SiGe substrates were needed in order to make back contacts to the solar cells. Compositionally graded, relaxed n-type SiGe layers grown on n-type Si substrates were grown by ultra-high vacuum chemical vapor deposition (UHV-CVD)[10], where as compositionally graded, relaxed p-type SiGe layers grown on p-type Si substrates were grown by low-pressure chemical vapor deposition (LP-CVD)[11], in each case a chemical mechanical polish (CMP) step was employed at a composition of $Si_{0.5}Ge_{0.5}$. The TDDs were measured by counting the etch pit densities (EPDs) in the Ge termination layer prior to III-V growth and were measured to be ~$1.0x10^6$ cm^{-2} for the p-type substrate and ~$1.8x10^6$ cm^{-2} for the n-type substrate. The devices were processed in the manner outlined in Appendix D; however, the devices discussed in this chapter do not have an anti-reflective coating (ARC). The base doping for these diode/solar cell structures were estimated by measuring the

capacitance-voltage profile using a Boonton 7200 C-V meter. The base doping level measured by CV were ~$2x10^{17}$ cm^{-3} for n+/p diodes and ~$9.5x10^{17}$ cm^{-3} for p+/n diodes; these doping values vary slightly from the target doping concentration and the values used in device models.

To confirm the electrical activity of the dislocations, electron beam induced current (EBIC) measurements were performed on these devices after processing. Figure 9.8a shows an EBIC image of the n+/p InGaP solar cell; it showed a dark spot density (DSD) of ~$1x10^{6}$ cm^{-2} which is consistent with the EPD measurements on the SiGe substrate. Figure 9.8b shows the EBIC image for the p+/n InGaP solar cell grown on SiGe. As evident in the figure, the p+/n cell has a higher DSD than the n+/p cell and was measured to be ~ $7x10^{6}$ cm^{-2} compared with ~$2x10^{6}$ cm^{-2} measured by EPD for this SiGe substrate. It is not clear whether this difference resulted from the activity of TDs in InGaP, a problem with the particular n-type substrate used (they are grown in batches so the quality may vary from wafer to wafer), or a problem generated in the InGaP growth by SSMBE. In any case, the n-type substrate TDD will be referred to as ~$7 x10^{6}$ cm^{-2} until further analysis can be performed. The fact that the TDs are evident in EBIC indicates that recombination is occurring at the TDs, however, whether this is the dominant recombination mechanism has yet to be determined.

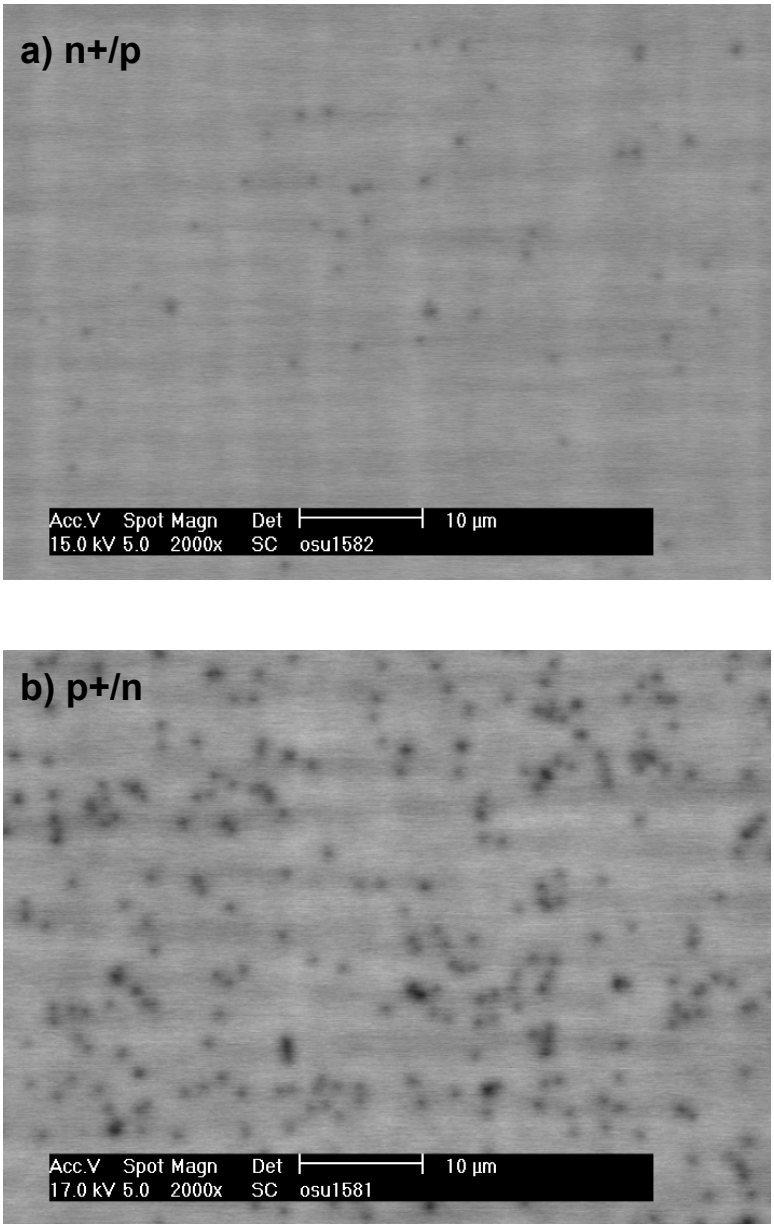
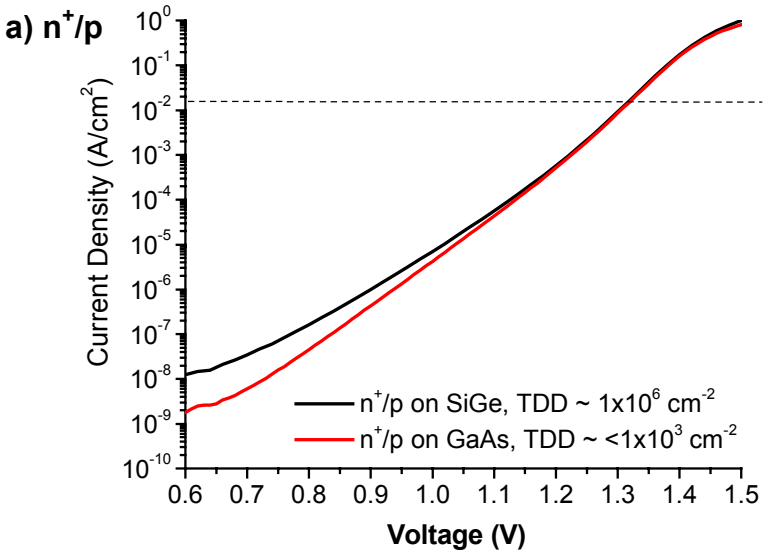


Figure 9.8 Plan-view EBIC images for a) n+/p InGaP solar cells grown on SiGe with DSD of ~ $1x10^6$ cm^{-2} and b) p+/n InGaP solar cell grown on SiGe with a DSD of ~ $7x10^6$ cm^{-2}.

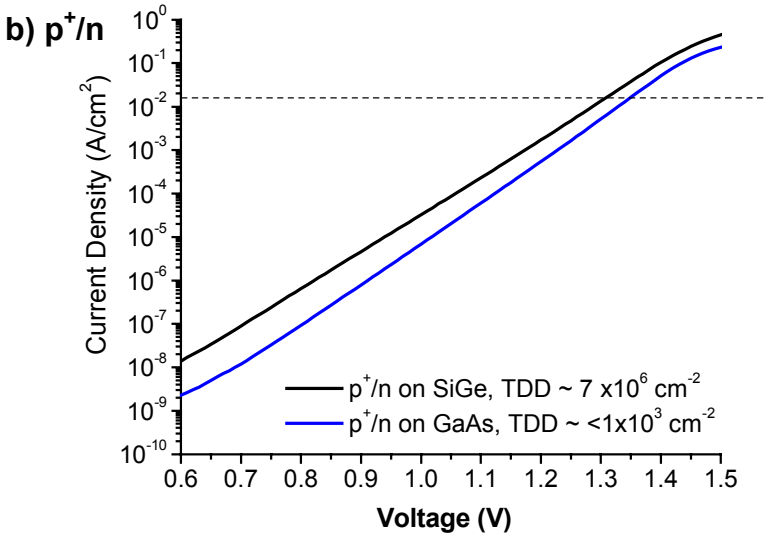
In Figure 9.9a, shows the DIV curves and performance parameters n+/p InGaP diodes grown on p-type GaAs and SiGe substrates. The DIV curves were measured in a Signatone dark box with a Keithley 2400 digital source meter with a current detection limit of 0.1 nA. Because the reverse saturation current density is lower than the detection limit of the current meter used, the DIV data presented was only measured from 0.5 V to 1.5 V. Above ~1.4 V, the series resistance causes the DIV curve to roll off. In analysis of these n+/p DIV curves, two slopes were identified which corresponds to the J_{o2} and J_{o1} components of the reverse saturation current. The extracted J_o values and effective ideality factors are included in the embedded tables. Due to the high series resistance (R_s), the IV curves were corrected for R_s before J_o and n values were extracted (the raw DIV data is shown in the figure). The onset of J_{o1} dominance occurs before the expected V_{oc} which indicates that J_{o1}, not J_{o2}, will determine the V_{oc} of the n+/p solar cell.[9] Moreover, the convergence of the J_{o1} components for n+/p InGaP diodes grown on GaAs and SiGe suggests that the mechanism controlling J_{o1} in these devices does not depend strongly on the density of TDs. The differences in the J_{o2} components for these devices cannot be compared directly due to the different ideality factors; however, there is a clear increase in J_{o2} and n for the n+/p InGaP diode grown on SiGe compared with the homoepitaxial diode.

In the same manner, Figure 9.9b shows the performance for p+/n diodes grown on n-type GaAs and SiGe substrates. The homoepitaxial ideality factor is not described by n=2, but by n= 1.7, which is similar to the homoepitaxial n+/p InGaP diode. Where as, the heteroepitaxial diode is described by n=2 which is indicative of depletion region recombination. Although, the J_o values cannot be directly compared with the model due

to variation in ideality factor, there is a clear increase in the reverse saturation current through recombination at TDs. Moreover, J_{o2} is expected to dominate at V_{oc}, which is consistent with the model. Comparing the DIV performance parameters of for n+/p and p+/n heteroepitaxial InGaP diodes we find that the p+/n InGaP diode shows a higher J_{o2}; however, it also has a higher TDD. Based on the modeled results for n+/p at $1x10^6$ cm^{-2} and p+/n at $7x10^6$ cm^{-2}, the n+/p J_{o2} is expected to be higher than the p+/n J_{o2} by ~ a factor of 2. This is not evident in the experimental data. This may result from differences in the minority carrier parameters used in the model compared with the actual material parameters for SSMBE InGaP material used in these diodes. More advanced diode models for SSMBE InGaP are currently being developed using the trap energies and capture cross-sections measured in by deep level transient spectroscopy (DLTS) on InGaP diodes. This information may help determine the sources of recombination in both n+/p and p+/n diodes, apart from recombination at TDDs. This information may help determine the fundamental source of these recombination mechanisms and thus suggest possible alteration in SSMBE growth procedures to reduce such recombination mechanisms.



sub.	TDD	J_{o1} (A/cm^2)	n	J_{o2} (A/cm^2)	n
SiGe	~1x10^6	~5x10^{-21}	1.2	4.5x10^{-14}	2.0
GaAs	< 1x10^3	~5x10^{-21}	1.2	5.5x10^{-15}	1.7



sub.	TDD	J_o (A/cm^2)	n
SiGe	~7x10^6	8x10^{-14}	2.0
GaAs	< 1x10^3	2x10^{-15}	1.7

Figure 9.9 DIV curves for a) n+/p and b) p+/n InGaP diodes grown on GaAs and SiGe substrates. The embedded tables show the extracted diode performance characteristics.

9.3 $In_{0.49}Ga_{0.51}P$ on SiGe solar cell performance

The solar cell performance for these InGaP solar cells were measured at NASA Glenn Research Center with an X-25 Spectrolab Solar Simulator calibrated for the AM0 spectrum and at OSU using a Xenon ARC lamp with uniform illumination in order to obtain LIV curves at a J_{sc} value of 16 mA/cm^2. Figure 9.10 shows the AM0 LIV curves and the solar cell performance parameters for each device. (Note that these devices have not been coated with an anti-reflective coating (ARC).) The V_{oc} value achieved for the p+/n configuration solar cell is close to that of high performance commercial cells, and will increase with an ARC and improved InGaP material quality with annealing as discussed in Chapter 8. While the lower V_{oc} values for the homoepitaxial n+/p solar cell compared to p+/n solar cell stems from a high diffusion based recombination mechanism present in n+/p cells. The J_{sc} values for n+/p cells are lower as well, based on the high base doping concentration that reduced minority carrier collection, as reported in Chapter 8. Based on prior ARC coating results on InGaP cells, an increase in J_{sc} by a factor of ~1.37 is expected for both polarity devices, suggesting that J_{sc} is expected to be ~ 12.5 mA/cm^2 for p+/n cells. By accounting for the higher metal coverage for this solar cell grid design (10%) compared with that of other dual junction cells (~2%) [7,8], the expected J_{sc} at the current state of SSMBE InGaP material quality and device design is ~13.6 mA/cm^2, which still shy of high performance AM0 J_{sc} values of 16-17 mA/cm^2. Surprisingly, the J_{sc} values for InGaP solar cells grown on GaAs are ~2% lower than those on SiGe. This J_{sc} reduction resulted from the oxidation of the $In_{0.47}(Al_{0.7}Ga_{0.3})_{0.53}P$ window layers for the homoepitaxial devices since they were processed ~5 months before the solar cells grown on SiGe. This reduction in J_{sc} is exhibited in the external quantum

efficiency (EQE) measurements by lower collection efficiencies across the entire spectrum. Thus, at this point in InGaP material development, growth on SiGe substrates has not limited minority carrier collection in InGaP solar cells.

In order to compare the InGaP open-circuit voltage values with the device model, the V_{oc} values were measured for a short circuit current density of 16 mA/cm^2 for all devices. In this way the impact of J_o on V_{oc} can be isolated from variations in J_{sc}. The measured V_{oc} values are compared with modeled results as shown in Figure 9.11. Now examining the V_{oc} values, we see that the V_{oc} of n+/p cells are limited by a mechanism that causes J_{o1} dominance near V_{oc}, not recombination at TDs. This limits the ability of the model to describe V_{oc} performance; however, the limited data collected thus far is consistent with the model. More data at TDDs greater than 1x10^6 cm^{-2} are needed since V_{oc} values at higher TDDs are expected to be lower than ~ 1.300V and thus the TDD dependent degradation might be appreciable. When considering the p+/n design, the device model suggests a V_{oc} value of 1.320V at a TDD of 7x10^6 cm^{-2} where experimental results showed a V_{oc} value of 1.301 V. The model's prediction is based on a D_p of 1 cm^2/s, where as, a D_p of 2.5 cm^2/s (also shown in Figure 9.12) would be consistent with the experimental V_{oc} obtained for this p+/n InGaP cell on SiGe. In fact, a D_p of 2 cm^2/s was suggested by Ref. 4, for n-type InGaP with a doping of 2x10^{18} cm^{-3}. This indicates that the "actual" D_p is likely to be higher than the value used in the device modeling of Section 9.1 and more importantly that p+/n InGaP/SiGe solar cells seem to follow the basic device model. Clearly, more data as a function of TDD is needed to confirm or dispute the application of this model to the InGaP material system, as well as independent measurements of minority carrier diffusion coefficients for n-type and p-type InGaP.

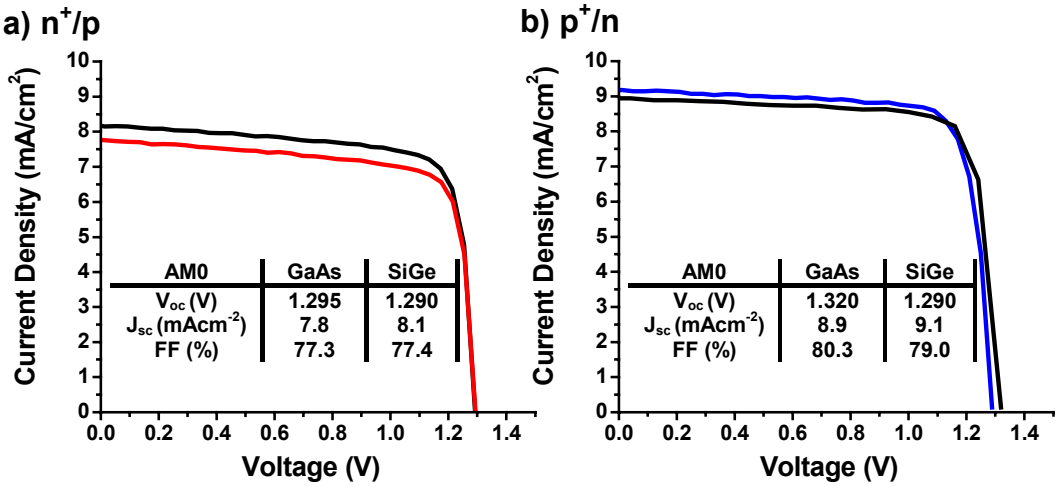


Figure 9.10 AM0 LIV curves and solar cell performance parameters for a) n+/p and b) p+/n InGaP solar cells grown on GaAs and SiGe substrates.

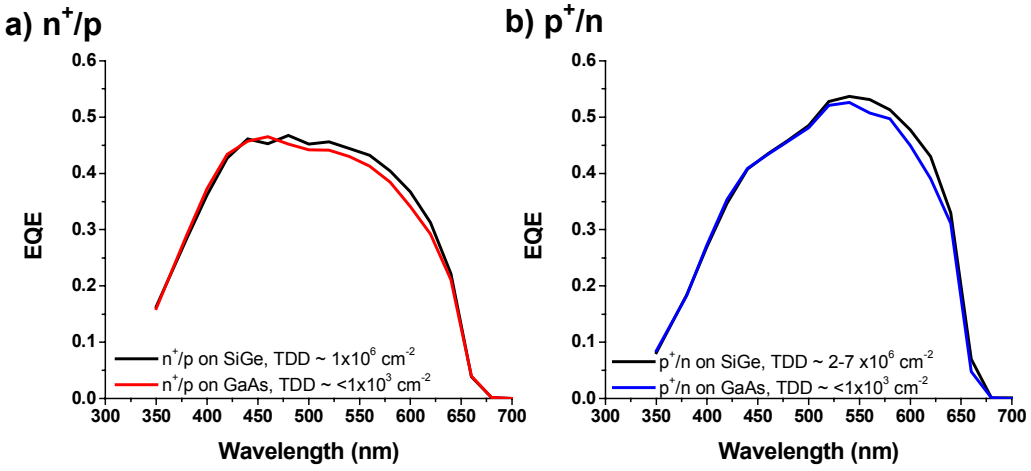


Figure 9.11 External quantum efficiency (EQE) curves for a) n+/p and b) p+/n InGaP solar cells grown on GaAs and SiGe substrates.

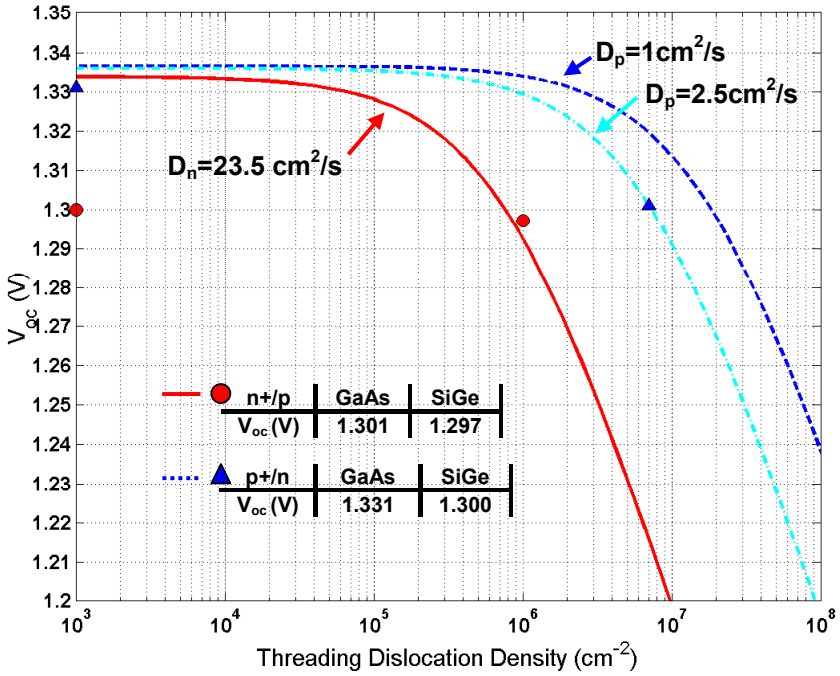


Figure 9.12 Modeled V_{oc} values as a function of TDD for n+/p and p+/n InGaP solar cells, assuming a J_{sc} of 16 mA/cm^2 compared with experimental V_{oc} values for InGaP solar cells grown on GaAs and SiGe measured at J_{sc} of 16 mA/cm^2.

9.4 Conclusions

The presence of TDs produced an increase in the J_{o2} reverse saturation current components for both n+/p and p+/n InGaP diodes grown on SiGe compared with InGaP diodes grown on GaAs. However, the overall low material quality of the homoepitaxial n+/p InGaP device limited the ability to observe the impact of TDD on V_{oc} for an InGaP solar cell grown on SiGe with a TDD of ~ $1x10^6$ cm^{-2}. The reverse saturation current component that was dominant near V_{oc} was a diffusion based J_{o1} component that was not TDD dependent. A clear TDD dependence was seen in p+/n cells; however, due to the lack of information on minority carrier properties in InGaP it is not definite whether InGaP recombination statistics follow the suggested model. Regardless, the fact that relatively high V_{oc} values were achieved is encouraging for the development of high performance p+/n InGaP/GaAs dual junction solar cells grown on SiGe since the p+/n InGaP top cell design is expected to be resistant to degradations in J_{sc} and V_{oc} at TDDs of ~ $1x10^6$ cm^{-2}, which can be achieved with current SiGe substrate growth technologies.

9.5 References

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CHAPTER 10

DUAL JUNCTION $In_{0.49}Ga_{0.51}P$/GaAs SOLAR CELLS GROWN ON SiGe

The development of $In_{0.49}Ga_{0.51}P$ (InGaP) solar cells grown by SSMBE at OSU not only provided information concerning the impact of TDs on InGaP device performance and material parameters, but also allowed the development of dual junction (DJ) solar cells devices that employ an InGaP top cell and a GaAs bottom cell. Based on the modeling presented in Chapter 7 concerning GaAs solar cell performance as a function of TDD and in Chapter 9 concerning InGaP solar cell performance as function of TDD, Section 10.1 describes the expected impact of TDs on DJ solar cell performance for p+/n and n+/p polarity devices. Based on this analysis, the development of p+/n DJ solar cells grown on GaAs and SiGe are examined in Section 10.2. These cells were grown, processed, and measured, in order to examine the validity of the proposed model for p+/n DJ solar cell devices. Finally, the solar cell performance characteristics for both AM0 and AM1.5-G illumination are presented in Section 10.3. Although the DJ cells grown on GaAs and SiGe suffer from low J_{sc} values, the cell performance indicates that ~92% of the V_{oc} value is retained and that the increased TDD did not hinder minority carrier collection at the current state of DJ solar cell development at OSU. Based on this result,

conversion efficiencies for a p+/n $In_{0.49}Ga_{0.51}P$/GaAs DJ cell on SiGe with a TDD of ~$1x10^6$ cm^{-2} in excess of 22.2% for AM0 illumination and 25.4% for AM1.5-G illumination are practically achievable.

10.1 Threading dislocation density and DJ device models

In this chapter we will consider the full diode expression, shown in Equation 10.1, including the diffusion and recombination components to the reverse saturation current, but a voltage independent depletion width. The DJ device structures follow the same cell designs presented in earlier chapters with a total GaAs cell thickness of ~ 3 μm and an InGaP cell thickness of 0.6 μm; however, the GaAs tunnel junction (TJ), which is typically grown between the two component cells as an "ohmic interconnect", was not incorporated into the DJ device model. The modeling input parameters are reviewed in Table 10.1 and are similar to those used in previous chapters. One change is the value of D_p for n-type InGaP. In this chapter, both the n-type InGaP base and emitter use a D_p of 2.5 cm^2/s based on the device results presented in Chapter 9 and data from Ref. 1. The DJ current-voltage model for series connected cells was developed based on the fact that the current through each sub-cell must be equal (current continuity); therefore, by calculating the voltage drop across each sub-cell for a given current, the voltages across each sub-cell are summed giving the total voltage drop across the DJ device for that particular current. Based on the modeled results for the individual sub-cells we expect that the J_{o2} component will dictate the V_{oc} obtained for each component cell; however, the full diode equation will still be used for the purposes of this analysis.

$$J = J_{o1}\left(\exp\left(\frac{qV}{kT}\right)-1\right)+J_{o2}\left(\exp\left(\frac{qV}{2kT}\right)-1\right)-J_{sc} \qquad \text{Equation 10.1}$$

a) n+/p modeling parameters

Parameters	InGaP
D_n (cm^2s^{-1}) ($1.5x10^{17}$ cm^{-3})	23.5
D_p (cm^2s^{-1}) ($2x10^{18}$ cm^{-3})	2.5
τ_n (ns) ($1.5x10^{17}$ cm^{-3})	7.5
τ_p (ns) ($2x10^{18}$ cm^{-3})	0.5
S_n, S_p (cm^2/s)	100,000
Bandgap (eV)	1.90
n_i (cm^{-3})	705
k_s	11.8

Parameters	GaAs
D_n (cm^2s^{-1}) ($2x10^{17}$ cm^{-3})	78.1
D_p (cm^2s^{-1}) ($2x10^{18}$ cm^{-3})	6.5
τ_n (ns) ($2x10^{17}$ cm^{-3}))	2.5
τ_p (ns) ($2x10^{18}$ cm^{-3})	25
S_n, S_p (cm^2/s)	3,000
Bandgap (eV)	1.42
n_i (cm^{-3})	$2.3x10^6$
k_s	13.2

b) p+/n modeling parameters

Parameters	Model
D_n (cm^2s^{-1}) ($2x10^{18}$ cm^{-3})	15.5
D_p (cm^2s^{-1}) ($1.5x10^{17}$ cm^{-3})	2.5
τ_n (ns) ($2x10^{18}$ cm^{-3})	0.5
τ_p (ns) ($1.5x10^{17}$ cm^{-3})	7.5
S_n, S_p (cm^2/s)	100,000
Bandgap (eV)	1.90
n_i (cm^{-3})	705
k_s	11.8

Parameters	GaAs
D_n (cm^2s^{-1}) ($2x10^{18}$ cm^{-3})	32
D_p (cm^2s^{-1}) ($2x10^{17}$ cm^{-3})	7.1
τ_n (ns) ($2x10^{18}$ cm^{-3})	2.5
τ_p (ns) ($2x10^{17}$ cm^{-3})	25
S_n, S_p (cm^2/s)	3,000
Bandgap (eV)	1.42
n_i (cm^{-3})	$2.3x10^6$
k_s	13.2

Table 10.1: Modeling parameters for the InGaP/GaAs DJ solar cell model with a) n+/p and b) p+/n device polarities.

The DIV curve for the DJ cell is calculated using both J_{o1} and J_{o2} components in Equation 10.1 with J_{sc}=0. Figure 10.1 shows the DIV curves for the GaAs and InGaP sub-cells along with the combined InGaP/GaAs DJ DIV curve. From this figure, it is clear that the "n=2" region has become an "n~4" region due the fact that for the same current the voltage approximately doubles. In the same manner, the "n=1" region exhibits and effective ideality factor of "n~2". No attempt will be made to extract "effective J_o" since it results from a combination of the GaAs cell and InGaP cell performance; it should be noted that if one of the sub-cell shows significant shunt resistance at low voltages, the distribution of current and voltage across the two cells can be severely distorted. This can results in DIV with regions with uncharacteristic ideality factors. The DIV curves for n+/p DJ diodes and p+/n DJ diodes with various TDDs are plotted in Figure 10.2a and Figure 10.2b, respectively. As expected, the n+/p DJ solar cells exhibit a larger increase in the "effective J_o" than the p+/n polarity devices. This stems from the fact that higher recombination currents were exhibited for both the individual n+/p GaAs and n+/p InGaP sub-cells when compared with their p+/n counterparts, thus the resulting n+/p DJ device exhibits the same behavior. Also included in these figures, is a line representing a typical AM0 DJ solar cell J_{sc} value (16 mA/cm^2); the intersection of this line with the DIV curve describes the expected V_{oc} value for a solar cell with the corresponding TDD. Again, this line intersects the DIV curve in the "n~4" region suggesting dominance of "J_{o2}" reverse saturation current components of the individual sub-cells near V_{oc}. It is also evident that lower open-circuit voltages are expected for n+/p diodes at a given TDD due to increased "J_o".

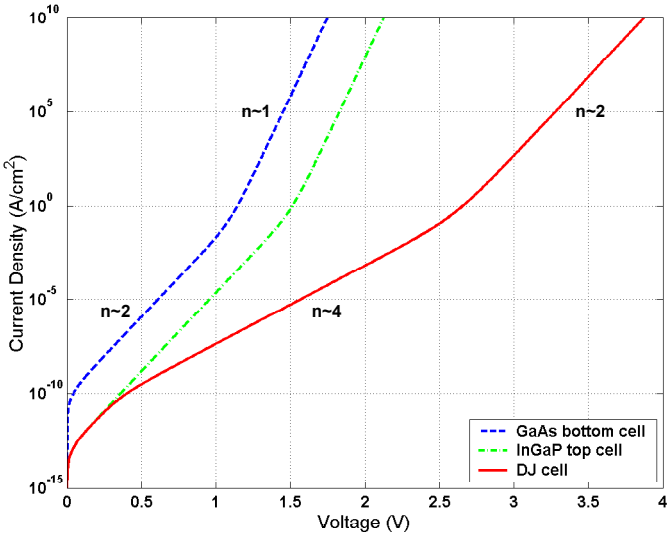

Figure 10.1 Modeled DIV curves for the p+/n GaAs and InGaP sub-cells and the resulting series connected DJ solar cell with no TDs.

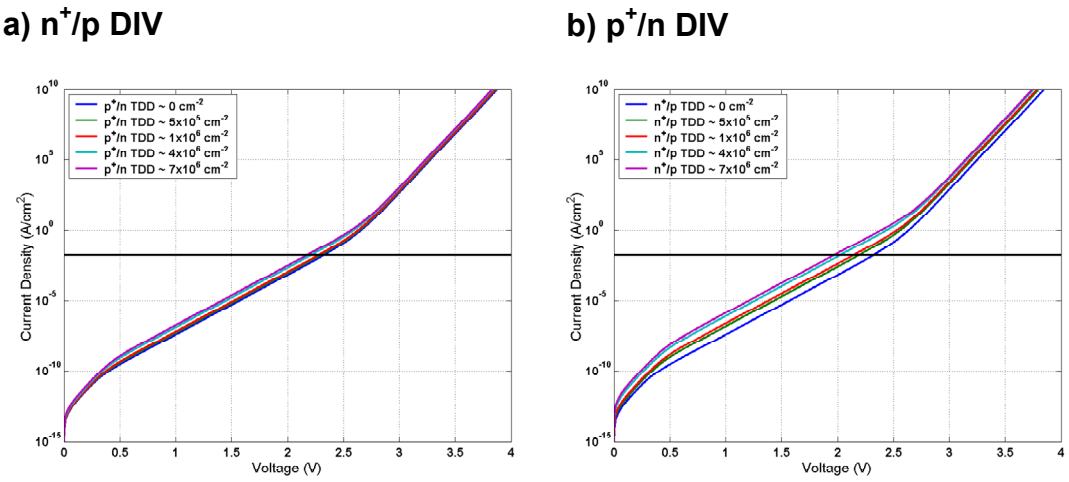

Figure 10.2 Modeled DIV curves for a) n+/p and b) p+/n DJ solar cells with varying TDDs. The horizontal line in each figure represents a current density of 16 mA/cm^2 indicating the dominance of "*n*~4" near V_{oc}.

Figure 10.3 compares V_{oc} as a function of TDD for n+/p and p+/n DJ solar cells based on complete diode model shown in Equation 10.1 and a J_{sc} value of 16 mA/cm^2. The main result is that the V_{oc} values for n+/p devices are expected to be lower than V_{oc} values for p+/n devices for a given TDD. The calculated fill factor (FF) (Figure 10.4a) and AM0 efficiency values (Figure 10.4b) are plotted for both n+/p and p+/n DJ cells as a function of TDD. It is important to point out that the FF values measured for most high performance DJ solar cells exhibit FF values of 84-88%.[2,3,4] This is attributed to the fact that as the current density decreases as V_{oc} is approached, one of the cells may "shut off" before the other cell, which in turn shuts off the DJ device. This enhances the FF by a rapid decrease in current density with voltage that does not reflect of the ideality factors of the diodes. As such, the efficiency predicted by the model (~ 23%) will increase to ~24.5% if a FF 88% is used in Equation 10.1. This efficiency is consistent with DJ devices with AM0 J_{sc} values of ~ 16 mA/ cm^2.[3] Recent advancements in DJ solar cells have been able to increase J_{sc} values up to ~17.4 mA/cm^2 based on improved InGaP material quality and the use of wideband gap tunnel junctions.[4] This has resulted in AM0 efficiencies of ~ 27% and V_{oc} values of 2.500V which are higher than the values presented in this model.[4] Regardless of the homoepitaxial J_{sc} or V_{oc} values achieved by DJ solar cells, the basic result presented in Figure 10.3 is still valid; p+/n DJ cells are expected to exhibit a greater TD tolerance compared with n+/p DJ cells.

$$\eta = \frac{P_m}{P_{in}} = \frac{FF \times I_{sc} \times V_{oc}}{P_{in}} \qquad \text{Equation 10.2}$$

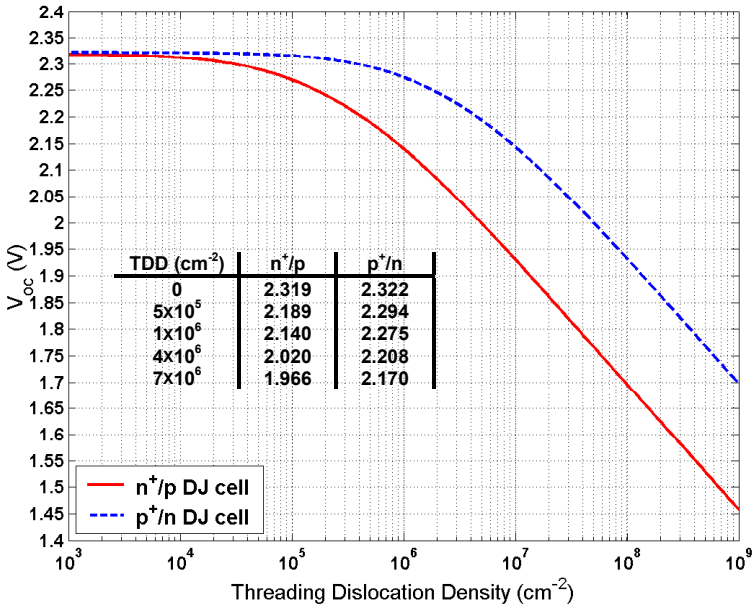

Figure 10.3 Open-circuit voltage (V_{oc}) as a function of TDD for n+/p and p+/n DJ solar cells, assuming a J_{sc} of 16 mA/cm^2. The embedded table shows V_{oc} values extracted from this plot.

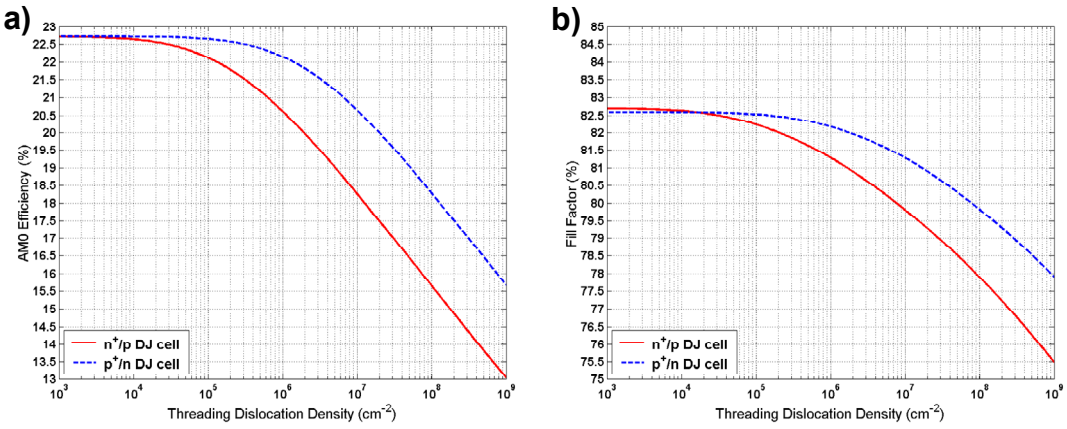

Figure 10.4 a) AM0 efficiency and b) fill factor (FF) as a function of TDD for n+/p and p+/n DJ solar cells, assuming a J_{sc} of 16 mA/cm^2.

As discussed in Chapter 9, the InGaP top cell is expected to be more TD tolerant than the GaAs bottom cell stemming from the overall lower diffusion coefficients of minority carriers in InGaP compared with GaAs (as seen in Table 10.1). Figure 10.5 compares the remaining fraction of V_{oc} as function of TDD for DJ InGaP/GaAs solar cells to the remaining fraction of V_{oc} in the InGaP and GaAs sub-cells assuming a J_{sc} value of 16 mA/cm^2 for both n+/p and p+/n polarity devices. The minority carrier diffusion coefficient impacts the onset of V_{oc} degradation and the rate of degradation in the TDD dominated regime. By defining 95% as the "onset of degradation", degradation occurs at a TDD of 4x10^5 cm^{-2} for a n+/p DJ cell the, while the p+/n cell maintains a fraction of V_{oc} greater than 95% until a TDD of 4x10^6 cm^{-2}. This suggests that SiGe with TDD of 1x10^6 cm^{-2} are suitable for high performance p+/n DJ devices and are expected to maintain 98% of the homoepitaxial V_{oc} value.

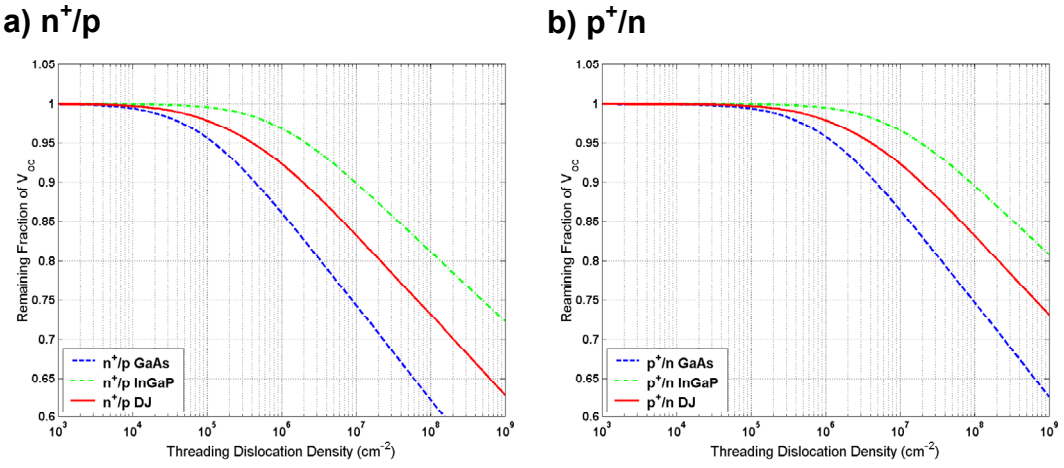

Figure 10.5 Remaining fraction of V_{oc} as function of TDD for the individual GaAs and InGaP sub-cells and the combined DJ solar cell for a) n+/p and b) p+/n polarity devices.

10.2 DJ solar cell growth, processing, and measurements

Based on these modeling results, it is clear that p+/n InGaP/GaAs DJ solar cells should perform better at elevated TDDs than n+/p DJ cells. Therefore, p+/n InGaP/GaAs DJ solar cells were grown by solid source molecular beam epitaxy (SSMBE) on GaAs and SiGe substrates. Compositionally graded, n-type, relaxed SiGe layers grown on Si substrates were grown by ultra-high vacuum chemical vapor deposition.[5] The particular substrates used in this work had an etch pit densities (EPD) of ~ 1.8×10^6 cm^{-2}, as measured in the Ge termination layer prior to III-V growth. The GaAs substrate used for device performance comparison, had the same orientation and off-cut as the SiGe substrate, (100) oriented with a 6° off-cut toward a {111} plane, but an EPD of less than 1×10^3 cm^{-2}. The InGaP/GaAs DJ solar cell structure is shown in Figure 10.6. Note that a thicker emitter design (0.2 μm compared with 0.05 μm) was used in the InGaP top cell since these devices were grown prior to InGaP top cell device optimization. The GaAs growth initiation on the Ge terminated surface of the SiGe substrate followed the method described in Chapter 2 and Ref. 6. This process incorporated an epitaxial Ge layer by SSMBE, a GaAs migration-enhanced epitaxy layer, and a low-temperature low growth rate GaAs layer. Cross-sectional transmission microscopy (X-TEM) images of the entire cell are shown in Figure 10.7a, with a close-up of the InGaP top cell with the GaAs tunnel junction (TJ) and the GaAs contact layer in Figure 10.7b. Figure 10.7c shows the GaAs/Ge interface, which exhibits no anti-phase domain disorder, as expected. Unfortunately electron beam induced current (EBIC) could not be used to confirm the TDD in the DJ cell structure since a biased EBIC technique similar to that used for DJ EQE measurements is required. The substrate used for the DJ on SiGe was also used in

Chapter 9 for a InGaP/SiGe single junction solar cell which reported a dark spot density (DSD) of 7 x10^6 cm^{-2} as measured by EBIC; this suggests that the DJ cell may have a TDD in the range of 2 to 7 x10^6 cm^{-2}.

p++ GaAs contact layer (1000 Å)	~1x10^{19} cm^{-3}
p+ $In_{0.47}(Al_{0.7}Ga_{0.3})_{0.53}P$ window (300 Å)	~2 x10^{18} cm^{-3}
p+ $In_{0.49}Ga_{0.51}P$ emitter (2000 Å)	~2 x10^{18} cm^{-3}
n $In_{0.49}Ga_{0.51}P$ base (4000 Å)	~1.5 x10^{17} cm^{-3}
n+ $In_{0.49}Ga_{0.51}P$ back surface field (300 Å)	~2 x10^{18} cm^{-3}
n+ $In_{0.47}(Al_{0.7}Ga_{0.3})_{0.53}P$ back surface field (300 Å)	~2 x10^{18} cm^{-3}
n++ GaAs TJ (250 Å)	~2 x10^{19} cm^{-3}
p++ GaAs TJ (300 Å)	~2 x10^{19} cm^{-3}
p+ $Al_{0.7}Ga_{0.3}As$ window (400 Å)	~3 x10^{18} cm^{-3}
p+ GaAs emitter (5000 Å)	~2 x10^{18} cm^{-3}
n GaAs base (20,500 Å)	~2 x10^{17} cm^{-3}
n+ $Al_{0.7}Ga_{0.3}As$ back surface field (1000 Å)	~2 x10^{18} cm^{-3}
n+ GaAs buffer (2000 Å)	~2 x10^{18} cm^{-3}
Ge (300Å)	uid
n+ SiGe substrate	~1 x10^{18} cm^{-3}

Figure 10.6 p+/n InGaP/GaAs DJ solar cell structure grown on a SiGe substrate with the layer description, layer thickness, and the target dopant concentration.

The growth rates used for the GaAs bottom cell were 1.0 μm/hr and 0.6μm/hr, for the GaAs and $Al_{0.7}Ga_{0.3}As$ layers, respectively. N-type GaAs and $Al_{0.7}Ga_{0.3}As$ layers were grown at 610°C with an As_2:III beam equivalent pressure (BEP) ratio of 14:1 with reference to the Ga BEP, while the p-type GaAs and $Al_{0.7}Ga_{0.3}As$ layers were grown at 575°C with an As_2:III ratio of 24:1. The GaAs tunnel junction layers were grown at 550°C with an As_2:III ratio of 24:1. After the tunnel junction was grown, there was a growth stop so that the In and Ga source temperatures could be changed and the BEP

values measured in order to achieve the proper $In_{0.49}Ga_{0.51}P$ composition. Subsequently, the $In_{0.49}Ga_{0.51}P$ and $In_{0.47}(Al_{0.7}Ga_{0.3})_{0.53}P$ layers were grown at a rate of ~ 1.15 μm/hr, a growth temperature of 490°C, and a P_2:III BEP ratio of 9:1 with reference to the In BEP. By using two Ga sources, there was no growth stop at the heterostructure interfaces for either the GaAs or $In_{0.49}Ga_{0.51}P$ sub-cells. Following the $In_{0.49}Ga_{0.51}P$ sub-cell growth, the substrate temperature was increased with P_2 overpressure until 550°C at which point the As_2 flux was initiated and the P_2 flux was terminated. After 60 seconds of As_2 exposure, the growth of the p-type GaAs contact layer commenced a rate of 0.6 μm/hr.

The fabricated solar cells had a device area of 0.044 cm^{-2} and 10 % metal coverage, which is higher than the 2% used for most DJ solar cells. The devices were processed using photolithography and wet chemical etching as outlined in Appendix D. Ohmic contacts were made to the p-type GaAs contact layer using Cr-Au (100Å/2 μm) metallization and to the Ge coated back of the SiGe substrate and the n-type GaAs substrate using Ni-Ge-Au (50Å/328Å/1000Å) metallization with a 4 min anneal at 400°C. The anti-reflection coating (ARC) consisted of MgF_2-ZnS-MgF_2 (70Å/500Å/1000Å) and was deposited in a thermal evaporator. After ARC, the J_{sc} values increased by a factor of ~1.34. The illuminated current density versus voltage (LIV) measurements under an AM0 spectrum (NASA Glenn Research Center) and under an AM1.5-G spectrum (the National Renewable Energy Laboratory) were performed in order to determine the short-circuit current density (J_{sc}), the open-circuit voltage (V_{oc}), the fill-factor (FF), and the efficiency (η) of the solar cells for space and terrestrial applications. The external quantum efficiency (EQE) measurements were performed, courtesy of the National Renewable Energy Laboratory, on the DJ solar cells by biasing

the cells such that the top cell and then the bottom cell were limiting current collection; in this manner, the individual photo-response of each cell was ascertained.

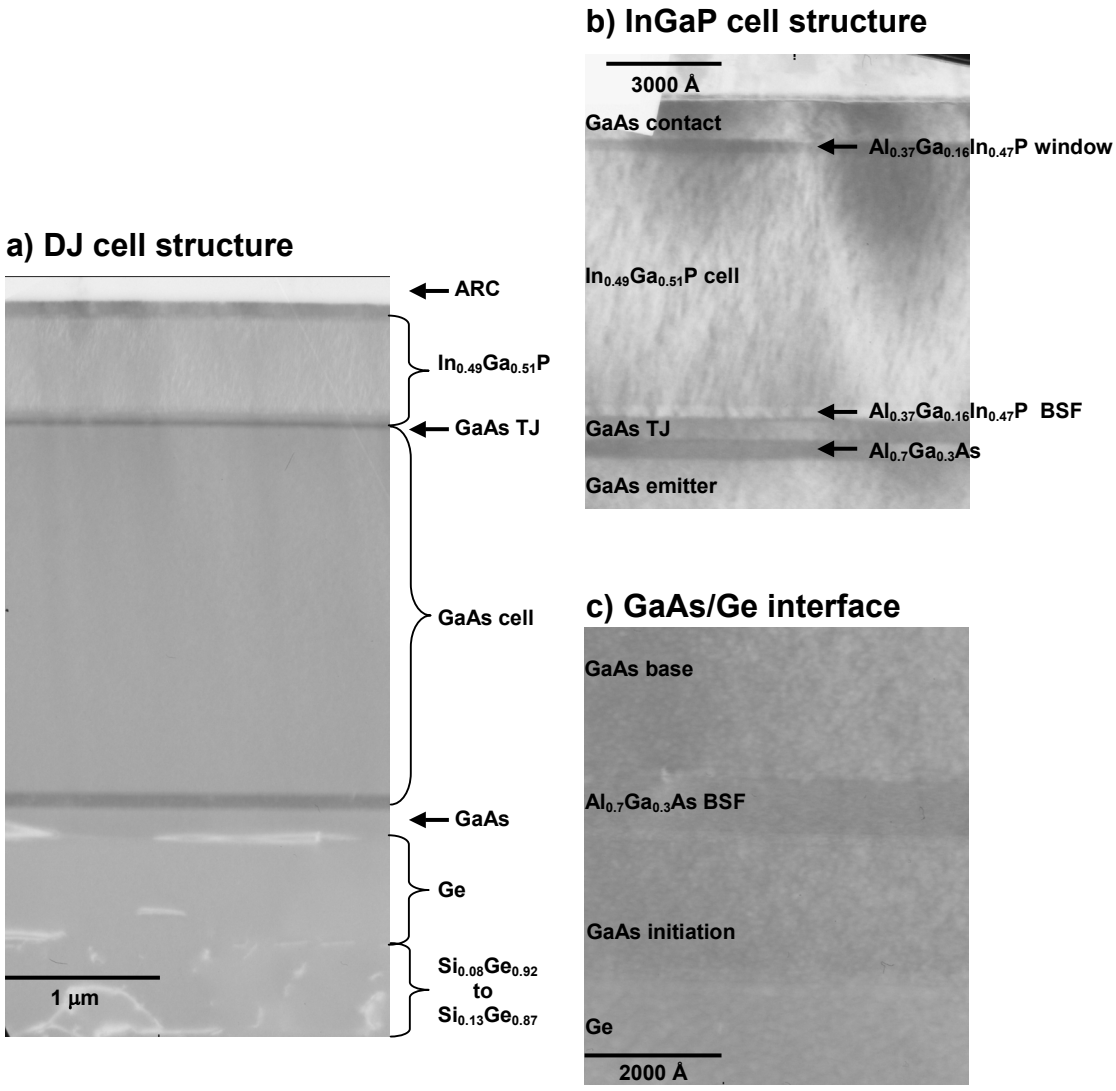

Figure 10.7 Cross-sectional transmission electron (X-TEM) micrograph of the p+/n InGaP/GaAs DJ solar cell structure grown on a SiGe substrate. The a) compete cell structure is shown as well as a close up of the b) InGaP top cell and the c) GaAs/Ge interface of the GaAs bottom cell for the DJ grown on SiGe.

Figure 10.8a shows the DIV curves for a p+/n DJ solar cell grown on GaAs and SiGe substrates. The DIV curves were measured in a Signatone dark box with a Keithley 2400 digital source meter with a current detection limit of 0.1 nA. Two slopes were identified in the DIV curve of the homoepitaxial DJ, which corresponds to the "J_{o2}" and "J_{o1}" components of the reverse saturation current for each sub-cell. Based on a J_{sc} of 16 mA/cm^2, the DIV indicates that the "J_{o1}" components start to dominate near V_{oc}. This results from the fact that homoepitaxial p+/n GaAs diodes exhibit an ideality factor of n~1 at V_{oc} and that the InGaP diode with a "thick emitter" had an increased J_{o1} component compared to "thin emitter" device as described in Chapter 8. The DJ solar cell grown on SiGe does not follow the expected DJ DIV characteristic and the cause of the deviations in the DIV is currently under investigation. As mentioned earlier, unequal distribution of voltages or a difference in tunnel junction performance for homoepitaxial and heteroepitaxial cell may be possible causes. The GaAs tunnel junction performance shown in Figure 10.8b was only tested for homoepitaxial growth. It showed a peak current density of 250 mA/cm^2 and a specific resistance of ~ 0.1 Ω/cm^2 similar to other reports.[7] Since 1-sun AM0 and AM1.5 J_{sc} values will not exceed 18 mA/cm^2, the tunnel junctions's peak current density is adequate; however, a better tunnel junction must be developed for concentrator application where J_{sc} values in excess of 5,000 mA/cm^2 may be obtained. Moreover, to maximize the J_{sc} for an optimized DJ cell, a wide-bandgap tunnel junction made of InGaP or AlGaAs needs to be developed in order to eliminate the parasitic absorption that occurs in a GaAs tunnel junction.

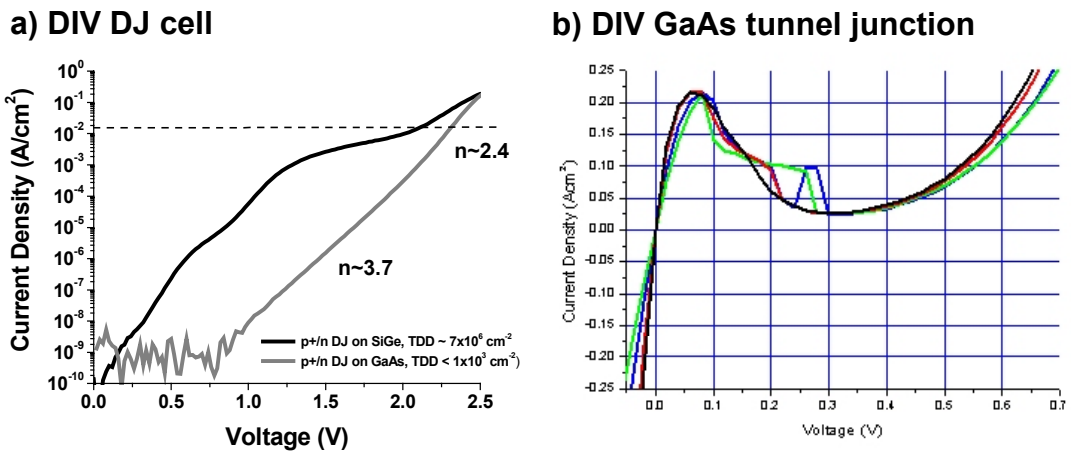

Figure 10.8 a) DIV curves for p+/n DJ solar cells grown on GaAs and SiGe substrates. b) DIV curve for a GaAs tunnel junction grown on a GaAs substrate.

10.3 DJ solar cell performance

AM0 and AM1.5-G LIV curves and solar cell performance parameters for InGaP/GaAs p+/n DJ soalr cells grown on SiGe and GaAs are shown in Figure 10.9. The AM0 J_{sc} values for both the homoepitaxial and heteroepitaxial DJ solar cells are ~ 6.9 mA/cm^2 which are significantly lower than typical AM0 DJ values (~16-17 mA/cm^2 [8, 9]). As noted earlier, this DJ cell structure had an InGaP top cell with a "thick emitter" that inhibited current collection in the InGaP cell and thus the total DJ device. With improvements in the InGaP top cell design and lower metal coverage AM0 J_{sc} values of 13.6 mA/cm^2 should be obtainable with the current SSMBE InGaP growth conditions. This increase in J_{sc} will increase the cell V_{oc} and efficiency values as well. The external quantum efficiency curves (EQE) for the InGaP top cell on GaAs and SiGe, shown in Figure 10.10a, indicate no variation in carrier collection which is consistent with the fact

that there is no significant difference in the measured J_{sc} values. Moreover, the integrated current density based on the EQE and AM0 spectrum is ~ 7 mA/cm^2 which is consistent with the measured AM0 J_{sc} values for the DJ devices. This confirms the fact that the InGaP top cell is the current limiting junction in the DJ device. Figure 10.10b shows the EQE for the DJ grown on GaAs, showing both the InGaP top cell and GaAs bottom cell response. Unfortunately the GaAs bottom cell grown on SiGe could not be biased properly to obtain an EQE curve, this may result from the high shunt resistance seen in the DIV curve as shown in Figure 10.8a. We can conclude that at this point in InGaP material development, growth on SiGe substrates has not limited minority carrier collection in the developed DJ solar cells.

As mentioned above, the other performance parameters such as V_{oc} and efficiency will improve with increases J_{sc}. The fill factor (FF) of these devices, ~ 70% on SiGe and ~ 77% on GaAs, are limited by other factors as well. One source of the reduced FF is the high oval defects density present in these devices (~ 500 cm^{-2}). Oval defects result form oxygen contamination in the Ga sources [10] and under current SSMBE growth conditions at OSU only produce defect densities of ~ 50 cm^{-2} in DJ devices. These defects are not particular to DJ solar cells and merely reflect SSMBE system quality. Therefore, DJ cell efficiencies will improve by reduction in the oval defects and other sources of shunt resistance present in DJ devices. Despite the low performance parameters, we find that when compared with homoepitaxial DJ performance parameters the DJ on SiGe retains 99% of J_{sc}, 91% of V_{oc}, 91% of FF, and 81% of the energy conversion efficiency. These results also represent the highest V_{oc} for an InGaP/GaAs DJ solar epitaxially integrated on a Si-based substrate reported to date. The only other report

for an n+/p configured device, resulted in a total V_{oc} of 1700mV under AM0 illumination.[11] The use of SiGe to obtain low TDD and the use of a p+/n DJ device for metamorphic dual junctions represents a significant technological advancement.

In order to compare this device performance with the developed DJ device model, the LIV curves were measured with a J_{sc} of 16 mA/cm^2. The V_{oc} values for the DJ on GaAs increased to 2262 mV while the V_{oc} for the DJ device on SiGe increased to 2120 mV. The measured V_{oc} values are compared with the model in Figure 10.10. The V_{oc} value for the homoepitaxial DJ device is lower than the modeled result due to the higher shunt resistance and higher reverse current densities in the InGaP top cell. As such, the V_{oc} for the DJ on SiGe is also lower than predicted by the model for a TDD of 7x10^6 cm^{-2}; however, the basic trend is reflected in this experimental data. The ability to compare the DJ device model with experimental results will improve as the DJ device performance is optimized and lower TDDs are obtained. Based on the measured V_{oc} and expected improvements in FF up to at least 78% with the elimination of shunt resistance, we conservatively predict that DJ cells on SiGe with a TDD of ~7x10^6 cm^{-2} to produce AM0 efficiencies of at least 19.6%.

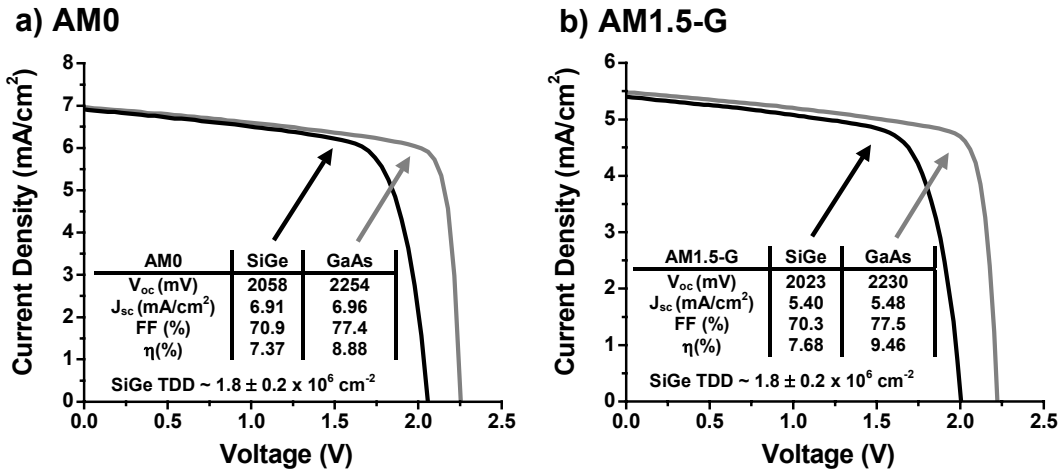

Figure 10.9 LIV curves and solar cell performance parameters for DJ solar cells grown on GaAs and SiGe substrates measured under a) AM0 and b) AM1.5-G illumination.

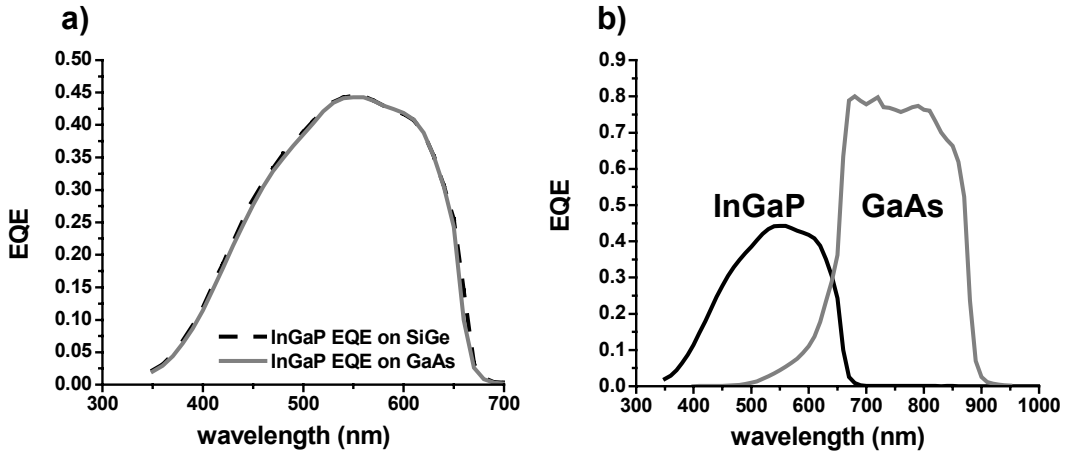

Figure 10.10 External quantum efficiency (EQE) curves for a) the p+/n InGaP top cell of the DJ solar cells grown on GaAs and SiGe and b) the p+/n InGaP top cell and GaAs bottom cell of the DJ solar cell grown on a GaAs substrate.

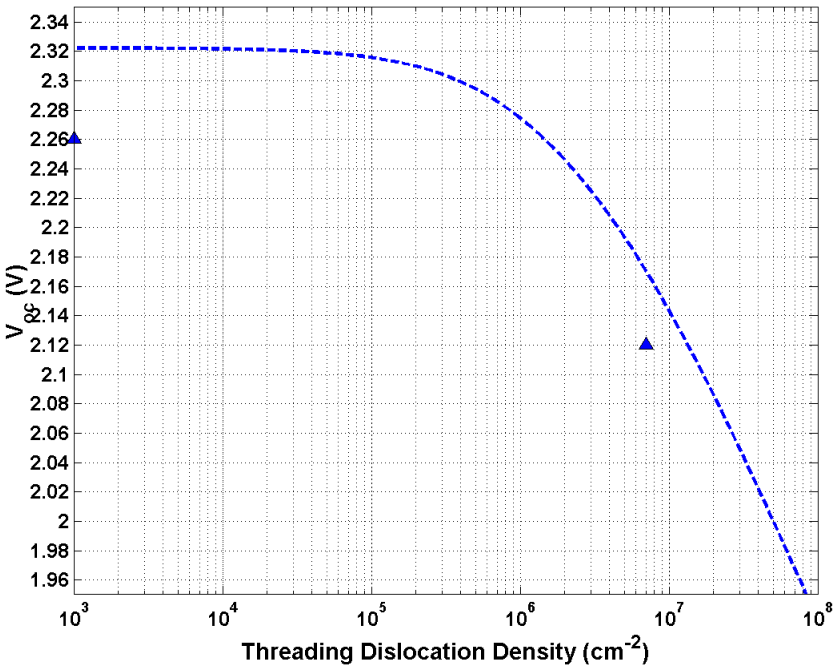

Figure 10.11 Modeled V_{oc} values as a function of TDD for p+/n InGaP/GaAs DJ solar cell, assuming a J_{sc} of 16 mA/cm^2 compared with experimental V_{oc} values for InGaP/GaAs DJ solar cells grown on GaAs and SiGe measured at J_{sc} of 16 mA/cm^2.

10.4 Conclusions

The performances of InGaP/GaAs n+/p and p+/n DJ solar cells as function of TDD were modeled. Due to the polarity preference of the individual sub-cells the DJ cells are also expected to demonstrate a p+/n polarity preference. As such, p+/n InGaP/GaAs DJ solar cells were grown on GaAs and SiGe and the device performances are compared. The presence of TDs for the DJ grown on SiGe decreased V_{oc} in a manner that is consistent with the modeled results; however, the DIV curve indicates that improvements in device structure are needed. Although the J_{sc} was limited by the InGaP top cell design; V_{oc} values in excess of 2V on a Si substrate were achieved for the first time, which is encouraging for the development of high performance p+/n DJ solar cells grown on SiGe substrates. Based on the modeled results and the fact that TDDs of ~ $1x10^6$ cm^{-2} can be achieved with current SiGe growth technologies, p+/n DJ solar cells grown SiGe should achieve an efficiency of greater than 22% for AM0 and 25% for AM1.5.

10.5 References

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CHAPTER 11

GaAs-ON-SiGe PHOTOVOLTAIC APPLICATIONS

Besides the fundamental studies concerning the influence of lattice-mismatch induced defects on GaAs, InGaP and DJ solar cells grown on SiGe substrates, studies were also completed to help this method of integration advance to commercial applications. To this end, high performance single junction GaAs solar devices were measured under both AM0 and AM1.5 illumination. Large area solar cells up to 4 cm^2, consistent with commercial solar cell areas, were produced and characterized. These large area cells were packaged for space flight and are schedule for the next shuttle launch to the International Space Station in order to characterize the impact of thermal cycling and the space environment on these devices. Moreover, preliminary measurements under solar concentration were performed on a high performance GaAs/SiGe solar cell since this technology is of great interest for terrestrial concentrator solar cell applications.

11.1 Growth and processing of p+/n GaAs solar cells grown on SiGe substrates

Compositionally graded, n-type, relaxed SiGe layers were grown (100) oriented Si substrates with a 6° off-cut toward the nearest {111} by ultra-high vacuum chemical

vapor deposition. A chemical mechanical polish was employed at $Si_{0.5}Ge_{0.5}$ followed by growth of the remainder of the $Si_{1-x}Ge_x$ layers up to 100% Ge, in order to achieve a lower residual TDD [1]. Two separate sets of SiGe substrates were used in these studies, and although the same SiGe buffer designs were used, variations in UHV-CVD reactor conditions produced SiGe substrates with varying properties. The fist set of SiGe substrates were grown on 0.03 Ω-cm 4" Si substrates with a doping concentration in the epitaxial SiGe layers of ~ 1 x 10^{18} cm^{-3} and resulted in a TDD of ~ 0.9 ± 0.2 x 10^6 cm^{-2}; these substrates have produced the highest efficiency GaAs-on-Si solar cells measured to date. The second set of SiGe substrates were grown on 0.01 Ω-cm 6" Si substrates and the dopant concentration in the SiGe layers were again doped ~ 1 x 10^{18} cm^{-3}, but the final TDD was 1.8 ± 0.2 x 10^6 cm^{-2}. These substrates were used in the large area device studies. The TDD in the Ge termination layer for the substrates used in this work was determined by counting the etch pit density (EPD). The impact of this change in TDD on device performance will be discussed later.

The solar cell device structures were grown by low-pressure metal-organic chemical vapor deposition (MOCVD), after deposition of a 0.1 μm GaAs nucleation layer by solid source molecular beam epitaxy (SSMBE) on the Ge termination layer of the SiGe substrates. The SSMBE GaAs initiation conditions include the deposition of an epitaxial Ge layer (~30 nm), a substrate anneal at 640°C, 10 periods of migration-enhanced epitaxy of GaAs at 350°C beginning with an As pre-layer, and concludes with a 0.1 μm layer of GaAs grown at a rate of 0.1μm/hr and a substrate temperature of 500°C. This initiation procedure suppresses anti-phase domain (APD) formation and minimizes

cross-diffusion, which allows the use of thin GaAs buffer layers of less than 200 nm [2]. Further details concerning the SSMBE GaAs initiation can be found in Ref. 2 and 3 and in Chapter 2, while the influence of MOCVD over growth on these SSMBE initiation layers can be found in Ref. 4 and Ref. 5. MOCVD was used for solar cell growth since surface defects in the SiGe substrate caused catastrophic failure in solar cells grown my SSMBE. These defects are discussed in Appendix E and do not represent a fundamental limitation of SiGe substrates in general.

The horizontal geometry low-pressure MOCVD reactor used for growth of solar cell device layers accommodates a single 2" wafer, maintains a pressure of 190 torr, and uses RF heating with a thermocouple placed below the susceptor [6]. The GaAs and $In_{0.49}Ga0_{.51}P$ (InGaP)layers were grown at a substrate temperature of 620°C, a growth rate ~ 2μm/hr, and a V/III ratio of 100. Silane and diethylsinc were used as n-type and p-type dopant sources, respectively, and the doping concentrations were calibrated by electrochemical capacitance voltage measurements. The substrates reached growth temperature in ~ 5 min and after growth of the cell structure the substrates were allowed to cool radiatively with arsine flow until the substrate temperature reached ~ 300°C. There was no growth hold between the InGaP and GaAs layers. Figure 11.1 shows the standard GaAs heteroface solar cell structure that was used for all devices. Figure 11.2 shows a cross-sectional transmission electron microscopy (X-TEM) image of the cell structure grown on a SiGe substrate; this image shows the III-V device layers after the removal of the contact layer, the Ge termination layer of the SiGe substrate, and some of the SiGe step-graded buffer layers. No impact from the transfer from MBE growth to

MOCVD growth is seen from TEM; moreover, higher magnification images confirm the suppression of APD disorder at the GaAs/Ge interface.

The devices were processed using photolithography and wet chemical etching similar to the methods presented in Appendix D. Ohmic contacts were made to the p-type GaAs contact layer using either un-annealed Cr:Au or annealed Zn:Au and to the Ge coated back of the SiGe substrates using Al with a 15 min anneal at 400°C or Au with a 5 min anneal at 400°C. Before depositing the back contact, the front surface was protected and the back surface was etched with a combination of the NH_4OH-based and HCL-based etches to ensure the removal of III-V layers. The variation in contact metallization resulted from the fact devices were processed both at Ohio State University and at NASA Glenn. The anti-reflection coating (ARC) consisted of MgF_2 / ZnS / MgF_2 and was deposited in a thermal evaporator. Due to variations in the thickness of ARC layers, the increase in short-circuit current density for solar cells with different ARC depositions varies between 30 – 37% and thus the changes in measured short-circuit densities for the cells presented in this chapter do not necessarily indicate changes in material quality.

Illuminated current density versus voltage (J-V) measurements under an AM0 spectrum were measured at the NASA Glenn Research Center (GRC) and under an AM1.5-G and AM1.5-D spectrum at the National Renewable Energy Laboratory (NREL) were performed in order to determine the short-circuit current density (J_{sc}), the open-circuit voltage (V_{oc}), the fill-factor (FF), and the efficiency (η) of the solar cells for space and terrestrial applications. The solar cells produced had various areas and grid designs; the devices ranged in size from 0.0444, 0.36, 1.0, to 4.0 cm^2 with metal coverage of 10, 8, 4, and 7 percent, respectively.

p++ GaAs contact layer (1000Å)	~1x10^{19} cm^{-3}
p+ $In_{0.49}Ga_{0.51}P$ window (500 Å)	~1x10^{18} cm^{-3}
p+ GaAs emitter (5000 Å)	~2x10^{18} cm^{-3}
n GaAs base (2.0 μm)	~1x10^{17} cm^{-3}
n+ $In_{0.49}Ga_{0.51}P$ back surface field (1000 Å)	~1x10^{18} cm^{-3}
n+ GaAs buffer (1000 Å)	~1x10^{18} cm^{-3}
n+ GaAs buffer by MBE (1000 Å)	~2x10^{18} cm^{-3}
Ge layer (300 Å)	-
n SiGe substrate	-

Figure 11.1 The p^+/n GaAs solar cell device structure on Ge/ SiGe /Si substrates.

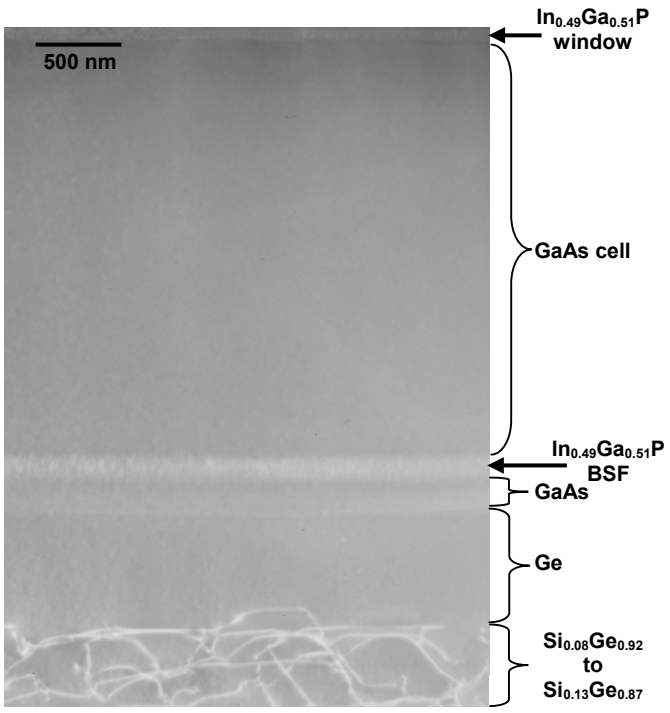

Figure 11.2 X-TEM image of a p^+/n GaAs solar cell grown by MOCVD on a Ge/ $Si_{1-x}Ge_x$ /Si substrate.

11.2 High performance p+/n GaAs/SiGe solar cells

By the reduction in TDD to ~ 1x10^6 cm^{-2} we have achieved V_{oc} values of 980 mV for AM0 illumination, the highest reported values for open-circuit voltage, V_{oc}, of any GaAs cell epitaxially integrated on a Si substrate reported to date [7,8]. Figure 11.3 shows the illuminated J-V for AM0 and AM1.5-G spectra. For AM1.5-G an efficiency of 18.1% was measured while the AM0 efficiency was measured to be 15.5 %, both of which exceed the highest independently confirmed efficiency for GaAs-on Si solar cells produced elsewhere [9,10]. Given that the grid shadowing for the GaAs/SiGe cell in Figure 11.3 is 10%, a more accurate comparison is obtained by scaling these results for 4.5% metal coverage, commensurate with the GaAs/Si cell from Ref. 9 and 10. This yields efficiencies for GaAs/SiGe of 18.8 % and 16.5 %, more than 1 % absolute higher than other verified reports.

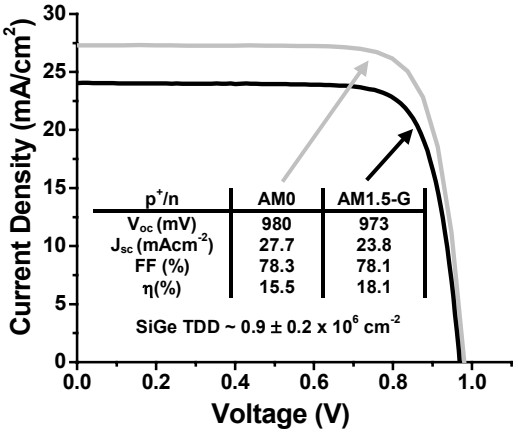

Figure 11.3 Illuminated J-V curves under AM0 and AM1.5-G spectrum for a single junction GaAs solar cell (area = 0.0444 cm^2) grown on Ge/ $Si_{1-x}Ge_x$ /Si substrates.

The high V_{oc} values obtained in this work are responsible for the increased cell efficiency. V_{oc} had been the primary impediment to achieving high efficiency GaAs on Si solar cells due to the sensitivity of V_{oc} on dislocation-mediated recombination current losses for metamorphic GaAs junctions. Modeling of this recombination process has predicted V_{oc} values for metamorphic GaAs cells that match the experimental performance for TDD values in various GaAs/Si and GaAs/SiGe cell structures as shown in Chapter 7. Due to increased recombination for GaAs solar cells grown on SiGe we find the measured ideality factor, n, is typically between 2 to 2.2 where as for homoepitaxial GaAs solar cells, with the same cell design and similar processing, we find that n is typically ~ 1.8. The changes in ideality factor can be attributed to the dominance of depletion region recombination contribution to the total reverse saturation current density which is often modeled by $n = 2$ [11]. Lower ideality factors can indicate that the diffusion term ($n = 1$) begins to contribute significantly and when the specific trap levels and capture cross-sections in the material of interest deviate from the assumptions in Ref 11. (For a more complete discussion see Chapter 7 of this thesis.) To demonstrate the impact of the ideality factor on cell performance we calculate the *FF* for two cases, $n = 2$ and $n = 2.1$, given a V_{oc} of 973 mV and a J_{sc} of 23.6 mA/cm^2. This results in predicted values for the *FF* of 79.9 and 79.1% for $n = 2$ and $n = 2.1$, respectively. Therefore, it is fair to conclude that the device performance shown in Figure 11.3 agrees with the suggested models and that the V_{oc} and *FF* is close to the expected limit for this TDD.

As a result, the total cell efficiencies presented in Figure 11.3 for a GaAs on SiGe solar cell is primarily limited by a reduced J_{sc} which resulted from a large grid obscuration (10%), a non-optimum anti-reflection coating and poor back surface field as

well as surface defects in UHV SiGe substrates. For GaAs/SiGe solar cells with a more optimum ARC and lower grid coverage we have obtained J_{sc} values of 29.6 mA/cm^2 and 24.5mA/cm^2 for AM0 and AM1.5, respectively. Since the diffusion length of holes in the n-type base are expected to be 2.7 μm at this TDD and other GaAs/Si device with higher TDD have achieved higher J_{sc} values [10,12] improvements in J_{sc} for GaAs/SiGe are expected. Therefore, at a TDD of ~ 1 x 10^6 cm^{-2} GaAs/SiGe should result in practically achievable AM1.5-G efficiencies of greater than 20% and AM0 efficiencies of greater than 17.5%. Any further reduction in TDD due to the evolution of SiGe substrate technology will serve to decrease minority carrier recombination that will increase J_{sc} and decrease depletion region recombination, which translates directly to increased V_{oc} and *FF*, all of which increase the overall cell efficiency.

11.3 Large area p+/n GaAs/SiGe cells for space applications

There has been concern whether the thermal expansion coefficient (TEC) mismatch between GaAs and Si, which can cause microcracks in the GaAs epilayer, will limit solar cell device areas and increase performance variations. To demonstrate the robust nature of the GaAs/SiGe integration method, the variation in the average performance characteristics for six 1.0 cm^2 single junction GaAs cells grown on SiGe and eight 1.0 cm^2 single junction GaAs cells grown on GaAs with the same device structure and processing are compared in Table 11.1. The variations in mean values of the individual cell performance characteristics (J_{sc}, V_{oc}, *FF*, and η) for cells grown on GaAs and on SiGe are comparable and thus the use of a SiGe substrate instead of a GaAs

substrate does not lead to added device variation, even though micro-crack densities in these GaAs/SiGe cells range from 3 - 72 cm^{-2}.

substrate	GaAs	SiGe
V_{oc}	1.7%	1.1%
J_{sc}	0.4%	0.7%
FF	4.6%	3.6%
η	3.8%	3.8%

Table 11.1 Percent deviation of the mean for solar cell performance characteristics measured on 1.0 cm^2 solar cells grown on GaAs and SiGe substrates under AM0 illumination. Statistics based on the measurement of eight solar cells grown on GaAs and six solar cells grown on SiGe.

Figure 11.4 shows representative AM0 illuminated J-V curves for 1.0 cm^2 solar cells grown on GaAs and SiGe; the average performance characteristics for both homoepitaxial (8 cells) and heteroepitaxial (6 cells) are shown in the embedded table. Comparing these average performance characteristics we see that there is a 3% change in J_{sc}, a 7% change in V_{oc}, and a 15% change in FF between the average performances on a GaAs substrate versus a SiGe substrate. The difference in FF, dominates the differences in total cell efficiency and is larger than expected based on the device models discussed earlier and thus must result from a source other than increased depletion region recombination. The highest performance large area (1.0 cm^2) GaAs on SiGe solar cells achieved to date for AM0 illumination had a V_{oc} of 972 mV, J_{sc} of 29.6 mA/cm^2, FF of 71.4 % and η of 15.0%.

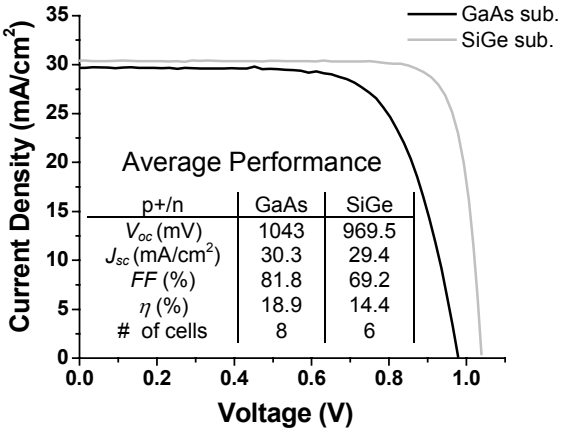

Figure 11.4 Average performance characteristics measured on 1.0 cm ^{2} cells on GaAs and SiGe substrates under AM0 illumination.

Figure 11.5 shows the AM0 illuminated J-V performance for GaAs solar cells with areas of 0.36, 1.0, and 4.0 cm^2 grown on a single SiGe substrate; this represents a factor of ten increase in cell area. These cells were subject to the same substrate, growth, and processing conditions and had an average micro-crack density of ~ 10 cm^{-2}. Therefore, the total number of cracks per cell has not introduced a significant degradation mechanism for large area devices. Note that, the cells presented in Figure 11.5 were grown on SiGe with a TDD of 1.8 ± 0.2 x10^6 cm^{-2}, approximately two times higher than the TDD in the small area cells presented earlier in Section 11.2. This reduces the V_{oc} from ~980 mV shown in Figure 11.3 to ~950 mV shown in Figure 11.5, consistent with theoretical expectations for these TDDs shown in Chapter 7. There is also a series resistance limitation on the measured *FF* values for these cells; although, the variation in *FF* does not scale with increasing device area. The cause of this low average *FF* (~73%)

is under investigation. High *FF* values up to 78% have been achieved for GaAs/SiGe for cell area up to 0.36 cm^2; thus, this reduction in *FF* is not a fundamental limitation of the GaAs/SiGe integration method and high efficiencies for large area solar cells are expected.

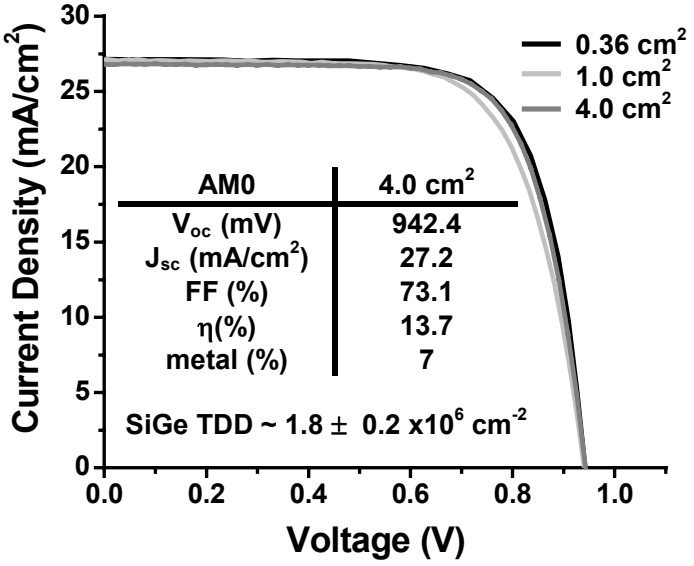

Figure 11.5 AM0 illuminated J-V curves for single junction GaAs solar cells grown on Ge/ $Si_{1-x}Ge_x$ /Si substrates. The performance characteristics for the 4.0 cm^2 solar cell are included in the figure. There is no systematic variation in cell performance with a ten-fold increase in cell area.

Figure 11.6 shows a photograph of a 1.0 cm^2 GaAs/SiGe solar cells with cracks perpendicular to the grid fingers. Typically, microcracks form in the GaAs cleave planes, which are {011} type for a (001) substrate. To investigate the cause of *FF* reduction for GaAs cells on Si-based substrates we looked at the *FF* as a function of crack density and direction with respect to the grid fingers; the results are shown in Figure 11.7. The

formation of microcracks results from the reliving of stresses in the epitaxial layers generated by the thermal expansion coefficient (TEC) mismatch between Si and GaAs. It was suggested by Tobin et. al that the redirection of current due to microcracks may increase series resistance and thus reduce the *FF* [13]. Figure 11.7 does not show a clear dependence on crack direction or density and thus is not suspected to cause the *FF* reduction in these cells. A reduced *FF* was also noted by O'hare et al. for GaAs/Ge/Si compared with GaAs/Si after a thermal cycled growth, although the exact source of the *FF* reduction was not determined, they suggested that there were complication at the GaAs/Ge interface during high temperature processes [14]. However, since the GaAs/Ge interface is well know, and GaAs/Ge solar cells do not show the same impact on *FF*, it may result from SiGe interfaces which was also present in Ref. 14. The exact cause of the reduced *FF* in GaAs/SiGe is still under investigation; however, recent data suggests that the adherence of grid fingers on GaAs/SiGe solar cells may be the culprit. As noted earlier, high *FF*s of 78% were achieved for GaAs/SiGe for cell area of 0.044 cm^2 and therefore low *FF*s should not be a fundamental limitation of GaAs/SiGe solar cells.

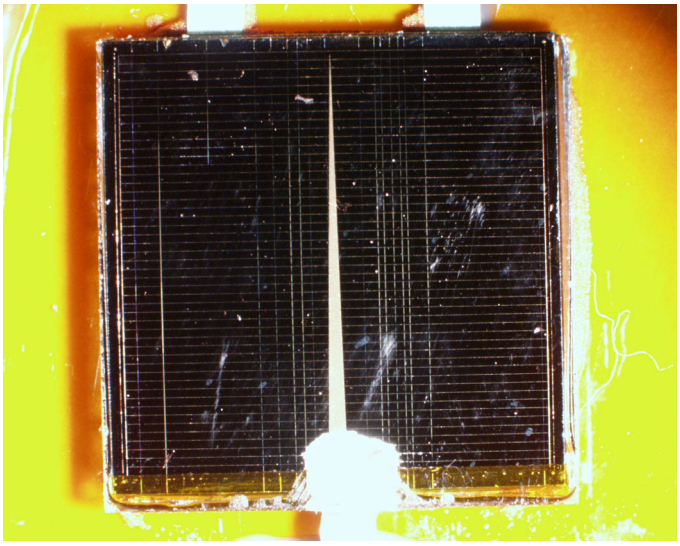

Figure 11.6 This is a fully processed 1.0 cm^2 solar cell on SiGe used for MISSE5 (See Section 11.4). Cracks are seen perpendicular to the grid fingers.

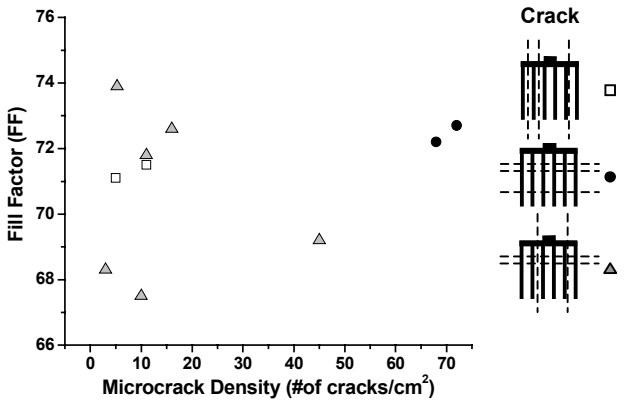

Figure 11.7 The variation with *FF* measured under AM0 illumination for single junction GaAs solar cells grown on SiGe substrates. No correlation between the measured *FF* and the mircocrack density and direction with respect to the grid fingers was found.

11.4 MISSE5 space testing of p+/n GaAs/SiGe cells

Another motivation for the development of these large area GaAs/SiGe solar cells was for use on the MISSE5 payload (Materials International Space Station Experiment, number 5) where a 5.5" by 3" area was earmarked for GaAs/SiGe solar cells. The point of contact for this experiment was NASA GRC who was also in charge of the hardware for electrical measurements for the entire experiment; therefore, many of the details in this section were provided by our NASA GRC collaborators. MISSE5 was constructed inside a PEC (passive experiment container), which is basically an aluminum suitcase. The PEC will be launched aboard a NASA Space Shuttle for transport to the International Space Station (ISS). Once at the ISS, astronauts will attach the PEC to a handrail on the outer surface of the ISS and open the PEC suitcase. Typically, the PEC is left in this position for approximately one year at which point astronauts close the PEC and it is returned to Earth. Since no shuttles have been launched since the Shuttle Columbia was lost on February 1, 2003, there is no experimental space data on these cells to present in this thesis. MISSE5 is schedule for the first flight once NASA Space Shuttle launches resume (no earlier than March of 2005). A description of the MISSE5 experiment and the GaAs/SiGe cells used will be provided since the manufacturing and characterization of these cells represented a large body of this thesis work.

In the past, the PECs of the MISSE missions have primarily contained passive experiments, designed to characterize the durability of materials subjected to the UV and atomic oxygen present at the ISS orbit. The MISSE5 experiment differs from previous experiments since it has an active payload. MISSE5 includes a 25W solar array, Li ion

batteries, on-board data acquisition electronics (including long term data storage) and a telemetry system. The telemetry system will transmit the data collected during the previous orbit to Earth approximately once every 4 minutes, thus ground stations will be able to autonomously collect the data. There are 39 solar cell experiments aboard MISSE5 as shown in Figure 11.8. This includes 36 cells characterized by J-V measurements and 3 cells characterized by measurements of J_{sc}. There are temperature sensors distributed around the experiment that are recorded every 10 minutes to provide a record of the thermal cycle environment and sun sensors to record the solar angle of incidence in two axes during a J-V measurements.

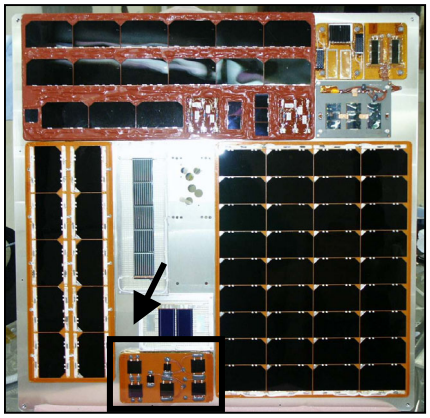

Figure 11.8 Layout of the entire MISSE5 testbed. The arrow and box indicate the GaAs/SiGe test area.

The goal of the GaAs/SiGe experiment is to examine the effects of the low earth orbit (LEO) space environment on the GaAs/SiGe solar cells. One of the primary interests is the effect of the thermal cycling on these TEC mismatched materials. As previously discussed, the GaAs device layers have a larger TEC than the Si substrate,

which places the GaAs epi-layers in a tension upon cool down from the solar cell growth temperature. A portion of this strain energy is relieved by the formation of cracks in the GaAs epi-layers as shown in Figure 11.6. In the ISS orbit, the temperatures of the GaAs/Si devices are expected to vary from +80 °C to -60 °C during each 90-minute orbit; thus, the GaAs epi-layers will be subjected to a sinusoidal variation in tensile strain 16 times per day. This thermal cycling of the solar cells may induce damage to the cells due to the TEC mismatch and thus the performance of the solar cells will be monitored. Two GaAs/SiGe devices will be actively monitored during flight by J-V characterization labeled IV1 and IV2 in Figure 11.9. The J_{sc} will be monitored for a cell on a SiGe and a GaAs substrate labeled Jsc1 and Jsc2, respectively. The others cells, P1, P2, and P3, are passive and will be measured upon return to Earth; the post flight and pre-flight performance will be compared. Degradation in these cells may come from two sources, one is the isolation of area of the cells by cracks such that current cannot be collected from these areas. Another source is the increase in series resistance by the redirection of current due to cracks. An increase in series resistance should be observable through measurement of the fill factor (*FF*) of the J-V characterized devices, which would be not measurable by changes in J_{sc} alone. Due to the ISS orbit and the short duration of the expected mission, degradation due to the radiation environment is expected to be minimal.

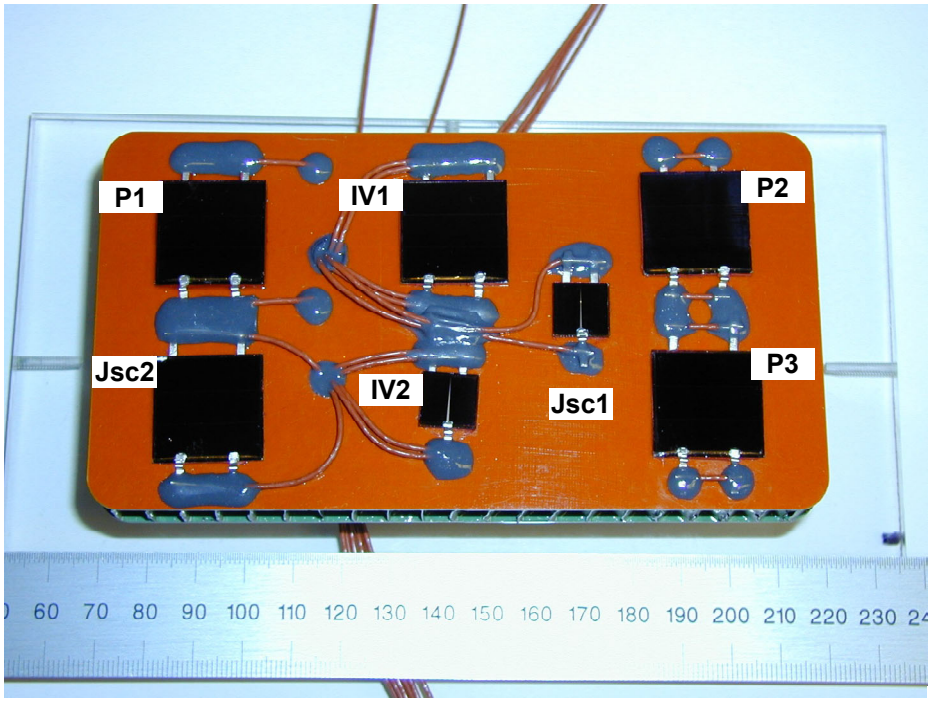

Figure 11.9 The schematic and a photograph of the GaAs/SiGe experimental test bed for MISSE5.

Although the space testing has not been completed to date, simulated thermal cycling experiments have been performed at NASA GRC on both GaAs/SiGe and GaAs/GaAs solar cells. The thermal cycle parameters for ground tests were a temperature range of +/- 80°C and an 8-minute cycle time. After 100, 250, 500, 1000, 3000, 6000 cycles, the AM0 illuminated J-V performance was characterized. Figure 11.10 shows the normalized value of the solar cell performance parameters from a GaAs/SiGe 1.0 cm^2 solar cell and a GaAs/GaAs 1.0 cm^2 solar cell. The percent change in all of the solar cell performance parameters was less than 3%, which was consistent with the variation in the GaAs/GaAs reference solar cell. Photographs were taken to evaluate the number of cracks after each set of thermal cycling; the photographs showed

no change in the crack density after 6000 thermal cycles. Since a year at LEO represents ~ 6,000 thermal cycles, once the MISSE5 experiment is completed the result of earth simulations and space testing can be compared.

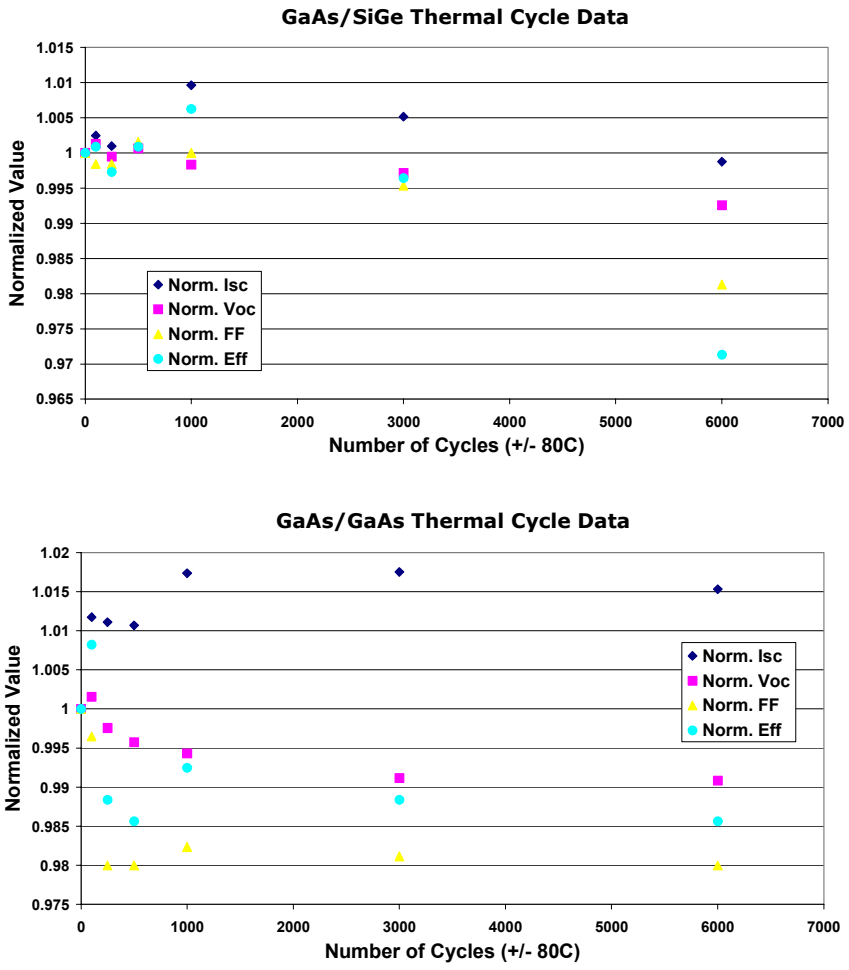

Figure 11.10 Normalized performance parameters for GaAs/SiGe and GaAs/GaAs p+/n solar cells as a function of the number of thermal cycles.

11.5 p+/n GaAs/SiGe cells for terrestrial applications

The one-sun AM1.5-G measurements were included in Section 11.2. For solar cell concentrator applications the standard is AM1.5-D where "D" stands for direct illumination compared with "G" for global. The direct spectrum is used for concentrator measurements since diffusely scattered light will not enter the concentrator lenses at the proper angle to be focused on the solar cell device. In practice, concentrator cells use lenses to collect the light and focus it to a smaller area solar cell, in this manner more power can be achieved with fewer solar cells. Although commercial devices will operate at a particular concentration, devices for testing measure the illuminated J-V at varying light fluxes to simulate varying solar concentrations. For a linear device, a solar concentration of 100 would produce a short circuit current density of 100 times the one-sun J_{sc} value. As described in earlier chapters, an increase in J_{sc} should increase V_{oc} and therefore, there is a potential increase in efficiency with increasing concentration. Another factor that may lead to increased efficiencies with increasing concentration is an increased *FF*. The *FF* can actually increase due to the operation of the solar cell at higher voltages where n=1 current component can dominate over the n=2 component. Again, the reduced ideality factor will increase the *FF* and can minimize the differences in GaAs/Ge or GaAs/GaAs and GaAs/SiGe cell performance that resulted from differences in ideality factor at one-sun illumination levels. Moreover, since these cells operate at higher currents and higher temperatures due to the higher photon flux the larger thermal conductivity of Si with respect to Ge and GaAs may help concentrator performance.

This increase in *FF* was demonstrated by Tobin et al. [15] who produced a GaAs/Si concentrator solar cell with 21.3% efficiency at 273 suns. Figure 11.11a shows J_{sc} versus V_{oc} which demonstrates the change in ideality factor from n=2 to n=1 for both GaAs cells on GaAs and Si substrates. The efficiency versus concentration is shown in Figure 11.11b; the efficiency increases from ~ 16 % to 21% from 1 to 273 suns. One of the most important factors for concentrator cells is the grid design; a typical concentrator grid design is show in Figure 11.12. The grid is circular based on the ability of the lenses to focus light; the fingers are thin and close together and the metal coverage in the designated area ~ 4.2% [16]. Since high currents are generated, the distribution of the current to the grids is extremely important [16]. Un-illuminated area under the grid fingers and that shadowed by grid fingers significantly influence the diode performance [17]. For these reasons concentrator measurements performed on one-sun grid designs solar cells suffer from high series resistance and do not typically show significant improvements in efficiency.

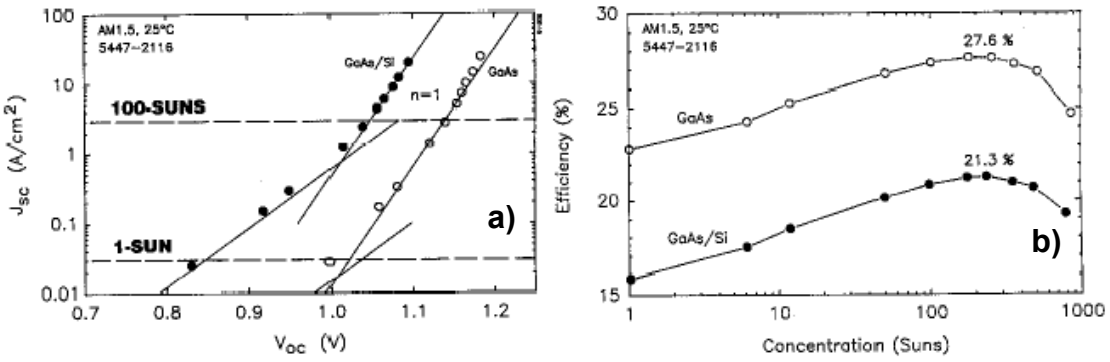

Figure 11.11 GaAs/GaAs and GaAs/Si concentrator performance from Ref. 15.

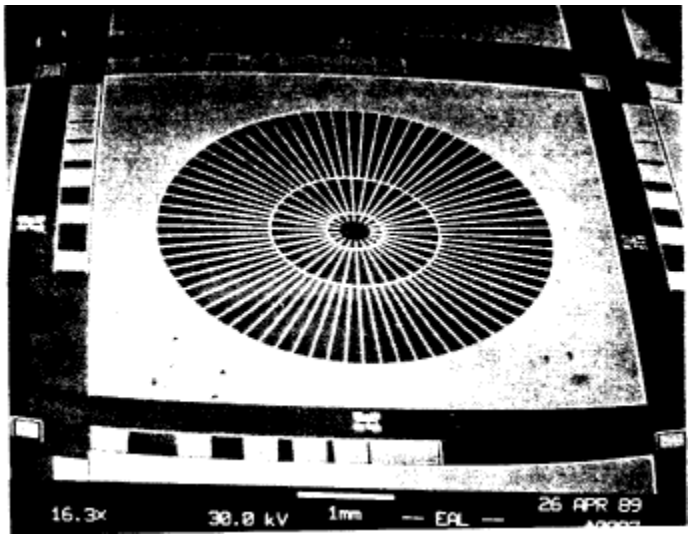

Figure 11.12 Concentrator cell design from Ref. 16. The designated illumination area is 0.126 cm^2 and the metal coverage is 4.2%.

The manner in which concentrator performance is measured is also an important consideration. The High Intensity Pulsed Solar Simulator (HIPSS) at NREL has two low-pressure xenon arc lamps that deliver 1 ms pulses of light. The beam is adjustable to provide concentrations of 1 to 2000 suns. The HIPSS has a temperature-controlled vacuum plate that has an electrically isolated voltage contact. The HIPSS system uses a calibrated linear cell to determine the concentration based on the measured J_{sc}. To minimize the heating of the cell, a pulsed light source is used and only part of the J-V is recorded during the 1ms pulse. Once the total J-V is recorded, the flux/concentration is changed by opening the aperture to a larger setting. Another method of measurement is the continuous illumination concentrator (CIC); it uses a 1-kW short-arc xenon lamp. The light from the xenon source is reflected off a mirror onto a concentrator lens mounted on a translation stage. The flux/concentration is changed by adjusting the

position of the lens. The system can be adjusted to achieve concentration ratios of 0.1 to 200 suns. Since there is no reference cell the test cell is assumed to be linear. Special biasing is required to obtain the proper V_{oc} since the continuous illumination elevates the cell temperature and thus reduces the V_{oc} obtained. For these two reasons the HIPSS measurement is considered more accurate; however, as will be seen in the next paragraph the HIPSS has limitations at low concentrations.

Concentration measurements on a single junction GaAs cell grown on SiGe for a conventional 1-sun grid design measurements were performed at NREL using the HIPSS system instead of the CIC system since it was not known if the GaAs/SiGe solar cells would be linear. Figure 11.13 shows the efficiency versus concentration for such a cell. The HIPSS data (red squares) collected did not make physical sense because the 1-sun HIPSS data did not match the 1-sun efficiency measured with the X-25 solar simulator (green circles); the difference in efficiency was 15.8% compared to 19.5%. First, it should be noted that the high performance GaAs/SiGe cell efficiency for AM1.5-D was 19.5%. This increase in efficiency compared with AM1.5-G illumination (18.1%) resulted from the fact that concentrator cell measurements use the designated illumination area, thus the bus bar metal area was subtracted from the cell area making the designated illumination area 0.0405 cm^2. Moreover, the metal coverage in this region of the GaAs/SiGe cell was only 2.6% compared with ~ 4.2% from a typical concentrator design; this also resulted in an extremely high AM1.5-D 1-sun efficiency for the GaAs/SiGe cell.

After further investigation by NREL staff, a custom HIPSS measurement (blue triangles) was performed which was intended to produce a better spectrum at lower

concentrations. There were still spectrum deficiencies at the concentrations less than ten but this data was more representative of the low concentration performance. The lack of a peak in efficiency at higher concentration resulted from reduction in *FF* with increasing concentration.

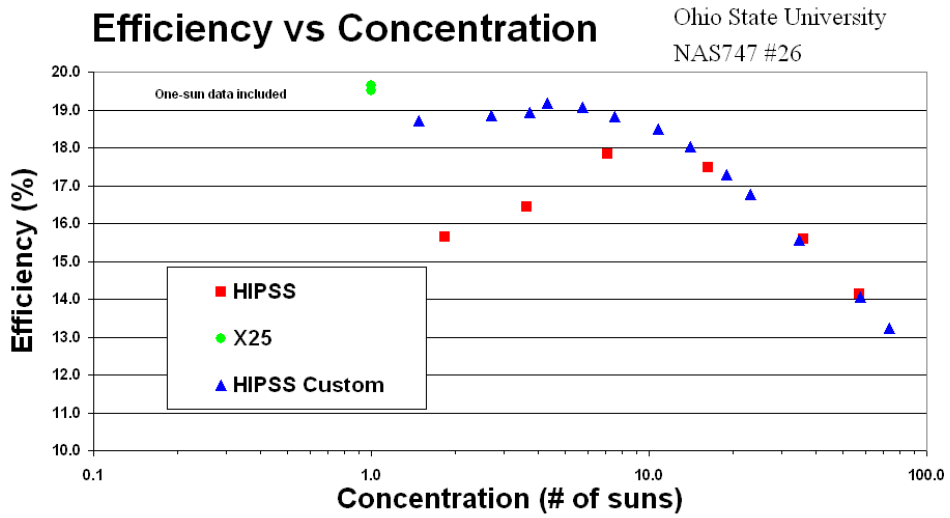

Figure 11.13 Efficiency versus concentration for AM1.5-D spectrum for a single junction GaAs solar cell (designated area = 0.0405 cm^2) grown on SiGe substrate. There is no peak in efficiency with concentration due to conventional 1-sun grid design.

Figure 11.14 shows (I_{sc}/ I_{sc}(one-sun))divided by the concentration plotted against the concentration for AM1.5-D spectrum for a single junction GaAs solar cell grown on SiGe substrate. The fact that the slope is close to zero shows that the J_{sc} increases with concentration with a ratio of ~ 1:1 for the custom HIPPS measurement; thus, the solar cell was linear up to at least 75 sun. Based on this data it is clear that in order to evaluate any meaningful concentrator performance we will need to use a proper concentrator grid design. Also, small area cells must employ the custom HIPSS method which still may

have spectrum problems at concentrations lower than ~ 10 suns. Although, since these devices showed linearity up to 100 suns, it maybe possible to use other measurement techniques such as the CIC which performs better at low concentrations.

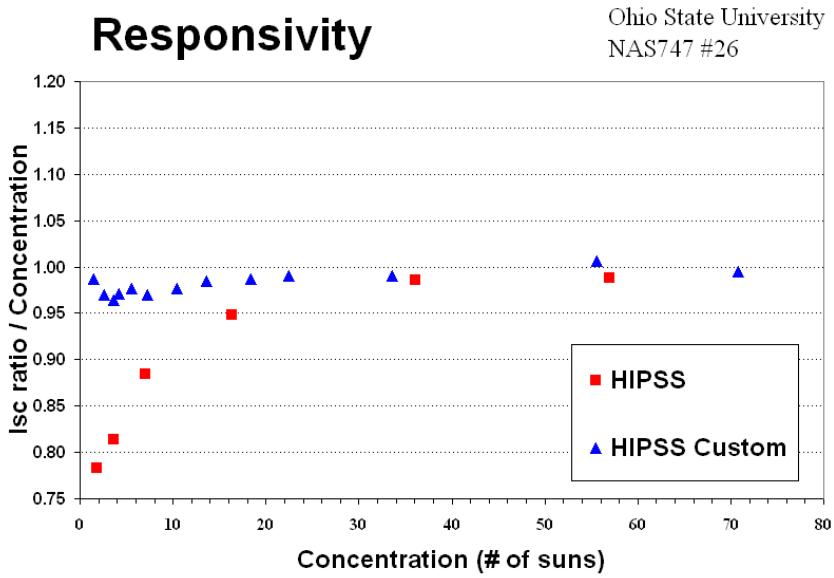

Figure 11.14 (I_{sc}/ I_{sc}(one-sun))divided by the concentration versus the concentration for AM1.5-D spectrum for a single junction GaAs solar cell (designated area = 0.0405 cm^2) grown on SiGe substrate. This figure indicates that this cell was linear in the concentration range measured (up to 75 suns).

11.6 Conclusions

High performance single junction GaAs solar cells on SiGe for space and terrestrial one-sun applications have been demonstrated. Moreover, SiGe substrates have proved to be a robust template for large area solar cell devices. Although the results of MISSE5 have not been obtained to date, simulated experiments have shown that the degradation of the solar cells with thermal cycling produced negligible changes in

efficiency and crack density; therefore, thermal cycling at LEO does introduce a significant failure mechanism for GaAs/SiGe solar cells. Moreover, it is clear that more understanding of concentrator application is needed; however, the GaAs/SiGe solar cells have linear behavior with concentration. Before further testing is completed a proper concentrator grid design needs to be used in order to demonstrate the potential increase in efficiency with concentration for GaAs/SiGe terrestrial applications.

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CHAPTER 12

CONCLUSION AND FUTURE WORK

12.1 Summary of results

The body of work presented in this thesis spans the study of the minority carrier lifetime in GaAs as a function of threading dislocation density (TDD) to the development of an InGaP/GaAs dual junction (DJ) solar cell model that accounts for the presence of elevated TDD to the physical realization of such a DJ solar cell on a metamorphic SiGe substrate. The common thread throughout this thesis is the basic understanding of how TDs influence III-V materials properties and photovoltaic device performance. Based on the results presented in this thesis, we can conclude that SiGe substrates are a viable platform for the commercial realization of high performance p+/n III-V multi-junction solar cells epitaxially integrated on a Si-based substrate.

Specifically, the minority carrier lifetime of electrons, τ_n, in p-type GaAs double heterostructures (DHs) grown on GaAs substrates and compositionally graded Ge/$Si_{1-x}Ge_x$/Si (SiGe) substrates with a varying threading dislocation density (TDD) were measured at room temperature using time-resolved photoluminescence. The electron lifetime for homoepitaxial GaAs and GaAs grown on SiGe (TDD ~ $1x10^6$ cm^{-2}) with a

dopant concentration of $2x10^{17}$ cm^{-3} were ~ 20 ns and ~ 1.5 ns, respectively. The electron lifetime measured on SiGe was substantially lower than the previously measured minority carrier hole lifetime, τ_p, of ~ 10 ns, for n-type GaAs grown on SiGe substrates with a similar residual TDD and dopant concentration. The reduced lifetime for electrons is a consequence of their higher minority carrier mobility, which yields an increased sensitivity to the presence of dislocations in GaAs grown on metamorphic buffers. These experimental results were consistent with a TDD dependent minority carrier lifetime model, and thus this lifetime model was incorporated into the GaAs solar cell device model to investigate the impact of TDs on n+/p and p+/n solar cell performance.

The resulting GaAs device models suggested that the decrease in lifetime as a function of TDD increases the depletion region recombination (J_{o2}) current density, which dominates the junction's total reverse saturation current density (J_o). The higher reverse saturation currents translated into an expected decrease in open circuit voltage (V_{oc}) for GaAs solar cells with elevated TDDs; however, the onset of this performance degradation occurred at a TDD of $1x10^5$ cm^{-2} for n+/p devices compared with a TDD of $1x10^6$ cm^{-2} for p+/n devices. In order to confirm the polarity preference suggested by the modeled results, both p+/n and, for the first time at OSU, n+/p GaAs solar cells were grown on GaAs and SiGe substrates. A significant difference in the reverse saturation current values for n+/p and p+/n diodes were observed, and were consistent with the expected difference in electron and hole lifetimes in GaAs with a TDD of $1x10^6$ cm^{-2}. Given the experimental V_{oc} values provided in this thesis and those available in the literature, we find that solar cell modeling closely predicts GaAs solar cell V_{oc} values as a

function of TDD and thus the p+/n polarity preference for GaAs solar cells integrated on Si-based substrates is confirmed.

Based on these findings, high performance single junction p+/n GaAs solar cells on SiGe for space and terrestrial one-sun applications were demonstrated. Total area efficiencies of 18.1% under the AM1.5-G spectrum were measured; this is the highest independently confirmed AM1.5 efficiency for a GaAs solar cell grown on a Si-based substrate to date. Analysis showed that efficiencies of greater than 20% are practically achievable at the current state of SiGe substrate development. Moreover, large area solar cells were also studied in order to examine the impact of device area on GaAs-on-SiGe solar cell performance. An increase in device area from 0.36 cm^2 to 4.0 cm^2 did not degrade the measured performance characteristics. Moreover, the device performance uniformity for these large area heteroepitaxial cells is consistent with that of homoepitaxial cells; thus, device growth and processing on SiGe substrates did not introduce added performance variations. The success of this integration method has lead to the scheduled flight testing of GaAs/SiGe solar cells aboard the International Space Station. Thus far, physically simulated experiments showed that the degradation of the solar cells with thermal cycling produced negligible changes in efficiency and crack density; therefore, thermal cycling at low earth orbits should not introduce a significant failure mechanism for GaAs/SiGe solar cells.

Growth of $In_{0.49}Ga_{0.51}P$ by solid source molecular beam epitaxy (SSMBE) was also investigated in this thesis in order to develop n+/p and p+/n $In_{0.49}Ga_{0.51}P$-based solar cell structures at OSU. Although improvement in the homoepitaxial quality of $In_{0.49}Ga_{0.51}P$ solar cells are still needed to achieve high performance devices, the impact

of TDDs on $In_{0.49}Ga_{0.51}P$ diode and solar cell performance were modeled and measured. The presence of TDs produced an increase in the J_{o2} reverse saturation current components for both n+/p and p+/n $In_{0.49}Ga_{0.51}P$ diodes grown on SiGe compared with $In_{0.49}Ga_{0.51}P$ diodes grown on GaAs. However, the overall low material quality of the homoepitaxial n+/p $In_{0.49}Ga_{0.51}P$ device limited the ability to observe an impact of TDD on V_{oc} for an $In_{0.49}Ga_{0.51}P$ solar cell grown on SiGe with a TDD of ~ $1x10^6$ cm^{-2}. A clear TDD dependence was seen in p+/n $In_{0.49}Ga_{0.51}P$ solar cells; however, due to the lack of information on minority carrier properties in $In_{0.49}Ga_{0.51}P$ it is not definite whether the recombination statistics exactly follow the suggested model. That being said, the current results are not inconsistent with modeling results, which suggest that a p+/n polarity preference is expected for $In_{0.49}Ga_{0.51}P$ solar cells with elevated TDDs and that $In_{0.49}Ga_{0.51}P$ solar cells are more tolerant to elevated TDDs than GaAs solar cells by virtue of the lower mobility of electron and holes in $In_{0.49}Ga_{0.51}P$ compared with GaAs.

The performance of n+/p and p+/n $In_{0.49}Ga_{0.51}P$/GaAs DJ solar cells as function of TDD were calculated based on the GaAs and $In_{0.49}Ga_{0.51}P$ single junction device models presented in this thesis. Due to the polarity preference of the individual sub-cells the DJ solar cell is also expected to demonstrate a p+/n polarity preference. As such, p+/n $In_{0.49}Ga_{0.51}P$ /GaAs DJ solar cells were grown on GaAs and SiGe and the device performances were compared. The presence of TDs for the DJ grown on SiGe decreased V_{oc} in a manner that is consistent with the modeled results; however, the dark current density versus voltage characteristic indicated that improvements in device structure are needed. Although the J_{sc} in these devices were limited by the $In_{0.49}Ga_{0.51}P$ top cell design; high V_{oc} values (>2.05 V for AM0 illumination) were achieved, which is

encouraging for the development of high performance p+/n DJ solar cells grown on SiGe substrates. Based on the modeled results and the fact that TDDs of ~ $1x10^6$ cm^{-2} can be achieved with current SiGe growth technologies, p+/n DJ solar cells grown SiGe should achieve an efficiency of greater than 22% for AM0 and 25% for AM1.5-G.

12.2 Extensions of this research and future directions

Besides the studies concerning the minority carrier lifetimes and diode and solar cell performance parameters considered in this thesis, other investigations are being and have been performed on devices and materials discussed in this thesis. One example is the proton irradiation of n+/p and p+/n GaAs solar cells grown on GaAs and SiGe substrates. The degradation in solar cell performance characteristics are being measured as a function of proton fluence, which is important information for space qualification of III-V solar cells. A set of companion samples were also grown by SSMBE which correspond to n+/p and p+/n diodes with a base doping of ~ $5x10^{16}$ cm^{-3} grown on GaAs, Ge and SiGe substrates. The lower base doping in these diodes enhances the detection of deep level induced by radiation as measured by deep level transient spectroscopy (DLTS). Results thus far have not shown a significantly different rate of defect introduction for GaAs diodes grown on SiGe substrates compared with those grown on GaAs substrates. Moreover, GaAs-on-SiGe solar cells are more robust to radiation-induced degradation in solar cell performance when compared with homoepitaxial GaAs devices. This study is being executed by Maria Gonzalez and initial result were reported at the 31st IEEE Photovoltaic Specialists Conference in June 2004.[1] Such radiation

studies will be extended to $In_{0.49}Ga_{0.51}P$ solar cells and diodes, for which low doped $In_{0.49}Ga_{0.51}P$ diode structures grown on GaAs and SiGe have already been grown.

Solar cell structures, double heterostructures with varying thickness, and thick single layers have been characterized by AFM, EBIC, TEM, and SIMS to compare the quality of GaAs grown on various SiGe substrates by SSMBE and MOCVD. The majority of this characterization was performed John Boeckl and a full analysis will be presented in his PhD dissertation. To briefly summarize, we have found low inter-diffusion and reproducible microstructure at the GaAs/Ge interface for GaAs initiation by SSMBE and subsequent regrowth by SSMBE or by MOCVD. In both cases, the TDDs in the GaAs layers grown by SSMBE and MOCVD are representative of the values measured in the SiGe substrates. Current voltage characteristics were also measured on GaAs diodes that contained the performance degrading "bat defect" discussed in Appendix E. Differences in the growth mechanisms within the defects for GaAs overgrowth by SSMBE and MOCVD were identified by X-TEM. These results explain the device performance degradation for SSMBE grown solar cells with "bat defects" and the defect tolerance of solar cells grown by MOCVD with "bat defects" present.

Although $In_{0.49}Ga_{0.51}P$ growth conditions and solar cell structures have been intensively studied, further research is still required to achieve $In_{0.49}Ga_{0.51}P$ device performance consistent with commercial solar cells To this end, $In_{0.49}Ga_{0.51}P$ double heterostructures (DHs) were grown and were measured by TRPL in the as-grown and annealed condition for $In_{0.49}Ga_{0.51}P$ at doping levels consistent with those used in the base of $In_{0.49}Ga_{0.51}P$ solar cells. The TRPL decays measured on 0.5 μm $In_{0.49}Ga_{0.51}P$ DHs showed that the hole lifetime increased from 1.3 ns to 3.0 ns while the electron lifetime

increased from 0.35 ns to 1.35 ns with annealing, although further growths and measurements are need to extract S and τ_{bulk} values. In-situ annealing of p+/n $In_{0.49}Ga_{0.51}P$ solar cells are also being studied in order to develop a device optimization processes that is compatible with III-V integration on SiGe substrates, and it is being studied as part of Matthew Lueck's master's thesis. These lifetime and cell performance comparisons coupled with DLTS studies on these $In_{0.49}Ga_{0.51}P$ diodes should help identify the source of the performance limiting defects in SSMBE $In_{0.49}Ga_{0.51}P$ material and is the subject of paper that will be presented at the 32nd IEEE Photovoltaic Specialist Conference in January 2005.[2] The majority of future $In_{0.49}Ga_{0.51}P$ solar cell growth and solar cell performance analysis will be studied by Mathew Lueck, while the DLTS studies in $In_{0.49}Ga_{0.51}P$ in the as-grown and annealed conditions are part of on going research by Maria Gonzalez concerning deep levels in SSMBE grown $In_{0.49}Ga_{0.51}P$.

$In_xGa_{1-x}P/In_xGa_{1-x}As$ DJ solar cells that are lattice-mismatched with respect to a Ge substrate have been vigorously studied over the past 5 years.[3,4,5] To date efficiency projections have not accounted for the degradation of performance parameters with increasing TDDs and needs to be considered when selecting an optimum bandgap profile and device polarity. Since these lattice-mismatched devices will have higher TDDs than the underlying conventional Ge substrate, this device technology represents a unique opportunity for metamorphic SiGe substrate since the residual TD network may provide sufficient dislocations for the relieving of strain in subsequent layers. Such work has been started to OSU and with our collaborators at NASA Glenn Research Center (GRC). NASA GRC have grown $In_{0.71}Ga_{0.29}P/In0._{23}Ga_{0.77}As$ DJ solar cells on GaAs and SiGe substrates which represent a total system mismatch of 1.7% and 5.8%, respectively.

To date, V_{oc} values of 1.417 V on SiGe compared with 1.782V on GaAs have been achieved with AM0 illumination and no ARC coating; however, it is believed that the n+/p device configuration used in this device has limited V_{oc} and device performance.[6] Device modeling which incorporates the impact of TDs on such lattice-mismatched DJ device structures is an area of future research. Another interesting feature of these lattice-mismatched solar cells is that they show no epilayer cracking which is unlike lattice-matched DJ cells, thus, ongoing work is being completed to asses the impact of the added compressive lattice-mismatch strain on the thermal expansion tensile strain.

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APPENDIX A

RHEED INTENSITY OSCILLATIONS AND BEAM FLUXES FOR THE DETERMINATION OF COMPOSITION AND GROWTH RATE IN SSMBE

In any semiconductor growth process the ability to control a compound's growth rate and elemental compositions are of particular importance, solid source molecular beam epitaxy (SSMBE) is no exception. In general, the primary factors in SSMBE that affect a compound's growth rate are the flux of elemental constituents impinging the substrate surface and the substrate's temperature. By using a combination of beam equivalent pressures (BEPs) and reflection high energy electron diffraction (RHEED) intensity oscillation frequencies the composition and growth rate of III-As or III-P alloys can be estimated with a high degree of accuracy. A brief overview of SSMBE and RHEED is included here, along with a fundamental description of RHEED intensity oscillations. The application of these concepts to the growth of III-As or III-P alloys is presented along with an explicit method for calculating the composition and growth rate of ternary alloys.

A.1 Solid source molecular beam epitaxy (SSMBE)

In order to understand the determination of growth rate in a SSMBE system a basic understanding of the system's sources, geometry, and growth mechanisms are important. MBE is an atomic layer film growth technique that utilizes an ultra high vacuum (UHV) environment to produce high quality layers with mono-layer precision. Figure A.1 shows a simplified arrangement of the material sources and the substrate in a MBE system. The material sources, or cells, contain high purity elements such as Al, As, Ga, In, P, etc.; combinations of these are then used in semiconductor film growth. Upon heating a cell, a molecular beam escapes from the cell orifice as the source material either evaporates or sublimes. For a given cell design, the cell flux, the number of molecules/(cm^2-s) that impinge the substrate at a given point, depends on the cell temperature, cell design, source material, and amount of source material in the cell. However, the cell flux alone is does not determine the growth rate since not all of the atoms that hit the substrate necessarily stick. Thus, the sticking coefficient of each type of molecule must also be considered. During early MBE investigations it was found that for particular substrate temperature ranges Group III atoms have approximately unity sticking coefficients to the substrate surface and that Group V molecules do not stick (and accumulate) on the substrate surface in the absence of Group III atoms. Therefore, when grown with an over-flux of Group V molecules, the compound growth rate is determined by the rate of arrival of Group III atoms. [1]

As seen in Figure A.1, each cell has a shutter located directly in front of it capable of blocking the molecular beam from the growth surface when closed. This gettering process is enhanced by liquid nitrogen cooled panels that line the cells and chamber

walls; these panels can be seen clearly in Figure A.2. As mentioned above Group V molecules do not have high sticking coefficients and therefore the shutter does not act as an adequate impediment to molecular flow toward the substrate. Therefore, most Group V sources are now designed with valves as well as shutters. Another benefit of the valved Group V sources is that the molecular flux can be altered by changing valve position instead of the cell temperature. Therefore, since the shutters close in less than 0.1 seconds and growth rates are on the order of ~1 mono-layer/second, the Group III fluxes and thus film growth can be terminated in a fraction of a mono-layer. It is this fact that allows MBE systems to grow semiconductor films with atomic precision and extremely abrupt interfaces.

From this brief description, it seems that the only measurement needed to determine the growth rate of a compound is the flux from each of the Group III sources being used, assuming that the substrate is at an appropriate temperature. In typical MBE systems, cell fluxes are measured using a beam equivalent pressure (BEP) gauge that mounts on the backside of the substrate holder. (See Figure A.2.) This gauge can be rotated into a position similar to the position of the substrate during growth. This gauge operates just like an ion gauge, as electrons from the filament pass to the grid they ionize molecules at a rate proportional to the local molecule density. The positive ions produced are then accelerated toward the collector thus generating a current proportional to the pressure. Due to many factors, the BEP reading is not the flux needed to calculate an exact growth rate; in fact, the ionization efficiency for each type of molecule is not the same. As a result, the Ga BEP for a GaAs growth rate of 1 mono-layer/second is different than the Al BEP for an AlAs growth rate of 1 mono-layer/second. Even if ex-

situ measurements, such as X-ray diffraction, are done to correlate a particular BEP with a particular growth rate, this is extremely labor intensive since it requires at least three growths per cell and a reliable means of ex-situ determination of growth rate. It is more convenient to have a non-destructive in-situ method for determining the growth rate and then correlating it to the measured BEP values. This is achieved with the use of RHEED intensity oscillations (RIO).

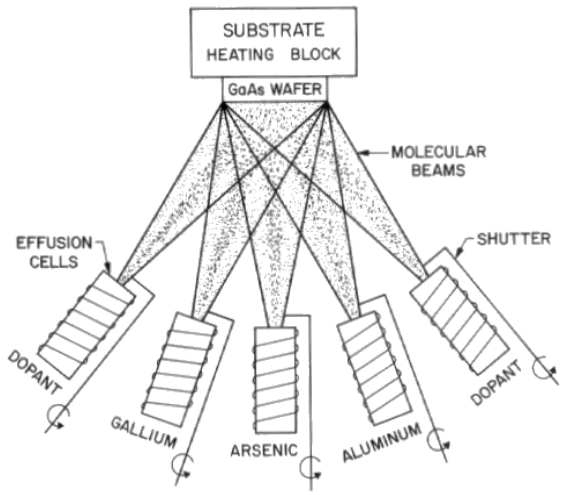

Figure A.1: A schematic of the material sources and the substrate in a SSMBE. [after 1]

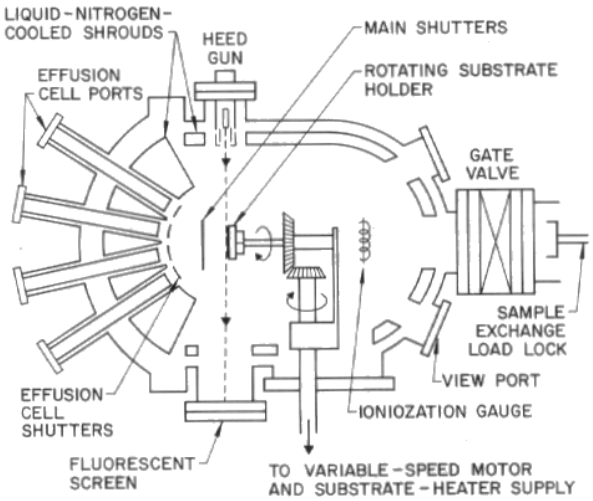

Figure A.2: A schematic of a MBE system with the main components labeled. Note the location of LN2 cooled shrouds, cell shutters, and the position of the substrate. Also note the geometry of the RHEED system. [after 1]

A.2 Reflection high energy electron diffraction (RHEED)

Before discussing the details of RIO a brief introduction to reflection high energy electron diffraction (RHEED) is presented. RHEED is a highly surface sensitive technique in which the pattern generated reflects the surface periodicity of the substrate. In RHEED, a collimated mono-energetic electron beam is directed toward the wafer surface at a glancing angle of typically one degree. [1] The MBE schematic in Figure A.2 shows the position of the two components of the RHEED system, the electron gun and the viewing screen. Typically, a phosphor screen is placed opposite the electron gun to record the electrons diffracted from a substrate's surface when it is in growth position. As shown, the RHEED setup does not interfere with the cells' molecular beam paths, thus, the technique can be used for in-situ analysis of the substrate surface during epitaxy. Figure A.3 shows a typical RHEED pattern for a [001] GaAs substrate along the [110] and $[1\bar{1}0]$ crystallographic directions. Because RHEED is sensitive to the arrangement of atoms on the surface of the substrate, the intensity of the RHEED streaks seen in Figure A.3 depend on the degree of order of the substrate surface.[2] Therefore, as mono-layer of material is deposited by SSMBE the intensity of the RHEED pattern changes and thus the growth process can be directly monitored. By determining the frequency of the RHEED intensity oscillations (RIO) the growth rate of the material is directly measured; this process is described in the next section.

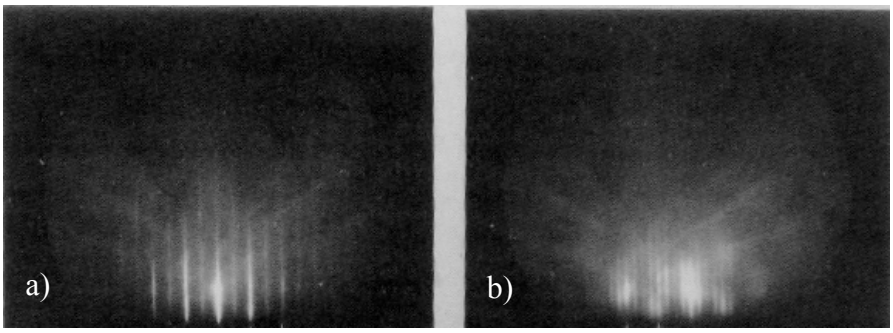

Figure A.3: Typical GaAs (001) RHEED patterns along the a) [110] and b) $[1\bar{1}0]$ crystalline directions. This particular reconstruction is known as a (2x4) reconstruction. [after 3].

A.3 RHEED intensity oscillations (RIO)

Before beginning RIO analysis a well ordered surface, like the As terminated GaAs(001)-(2 x 4) reconstruction, is needed. A detector is then positioned on the specular spot of the 00 rod of the diffraction pattern. Although all of the streaks undergo intensity oscillations, the specular spot is usually the brightest point of the diffraction pattern and yields the best signal to noise ratio. (The generation of the specular spot is a result of kinematical diffraction that occurs and will not be discussed here.[2]) The intensity of this spot can be obtained from the pattern on the phosphor screen in a number of ways, one of the simplest being collection through a lens/fiber optic focused on the spot. The collected light is then fed into a photo-multiplier tube, which generates a voltage proportional to the intensity of the signal. The intensity from the reconstructed surface should remain constant before growth, the value of which depends on many factors. [2] Once the growth is initiated, there is an initial transient and then the intensity of the

pattern begins to oscillate. The voltage produced can then be fed into a spectrum analyzer that determines the frequency components of the signal and thus the frequency of the RIO. Figure A.4 shows a typical RHEED oscillation for the growth of GaAs at approximately 1.2 μm/hr.

As alluded to earlier, the frequency of the oscillations is related to the rate of epitaxy and therefore the ordering of the substrate surface. Figure A.5 shows a possible sequence of surface conditions during the growth of a single mono-layer of material which explains the origin of these intensity oscillations. The surface is shown to initially grow in "islands" as the atoms diffuse and randomly nucleate on the wafer surface. As long as the terrace or step widths are large compared to the diffusion length of the adatoms on the surface, the atoms cannot diffuse to step edges for nucleation and this 2-D growth nucleation model is accurate.[4] With continued deposition, the island formations increase in size until a complete mono-layer of coverage is achieved. After completion of a mono-layer ($\bar{\theta} = 1$), as shown in Figure A.5, the surface is again atomically smooth and well ordered as it was prior to the start of deposition.

Also shown in Figure A.5, an atomically smooth surface corresponds to maximum surface order and therefore maximum RHEED intensity. Similarly, a condition of maximum disorder exists under the condition of half mono-layer surface coverage and thus correspond to a minimum in the RHEED intensity. Since the surface achieves a complete mono-layer of coverage prior to the nucleation of the next mono-layer, each additional layer produces a full cycle of a RIO. It should be noted that in the case of growth on an As terminated GaAs(001)-(2 x 4) surface reconstruction the completion of a mono-layer corresponds to the regaining of an As terminated GaAs(001)-

(2 x 4) reconstruction. Since there are four "layers" of atoms present in the zinc-blende cubic lattice the thickness of a mono-layer is half of the GaAs lattice parameter.

Now that the frequency of the RHEED intensity oscillations are understood as well as the growth rate extraction, other signal features need to be addressed. From Figure A.4 it is easily seen that the amplitude of the oscillations damp out as growth proceeds and in fact oscillate about a lower intensity when compared to the intensity before growth. As mentioned above, this lower intensity is attributed to a lack of order on the substrate surface. It has been reported that as growth proceeds, the step edge density changes and thus the surface is no longer ideal for the 2-D growth model. The equilibrium step edge density is governed by surface diffusion length for the particular growth conditions; therefore in general, a higher substrate temperature causes the step edge density to reach equilibrium more quickly and thus the RIO damp out more quickly.[2] This can become a problem when attempting to extract the growth rate from the signal. Again as seen in Figure A.4, once growth has terminated, the intensity of the specular spot recovers back to it pre-growth value. This results from the return of the step edge density to its pre-growth value. Thus when measuring growth rates via RIO, the surface must be given adequate recovery time after growth before data can again be taken.

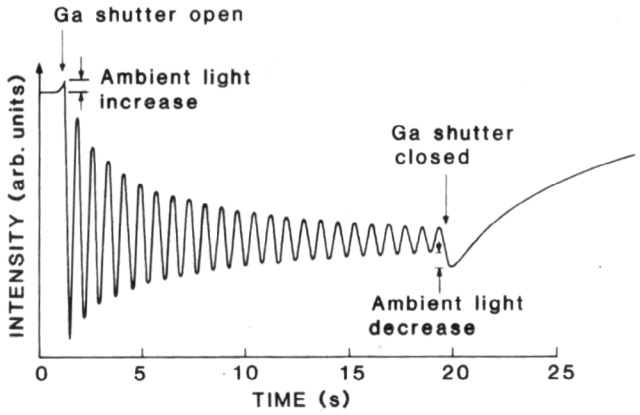

Figure A.4: Plot of RHEED intensity versus time during growth showing the variation in RHEED intensity. These oscillations correspond to a GaAs growth rate of approximately 1.2 μm/hr. [after 4]

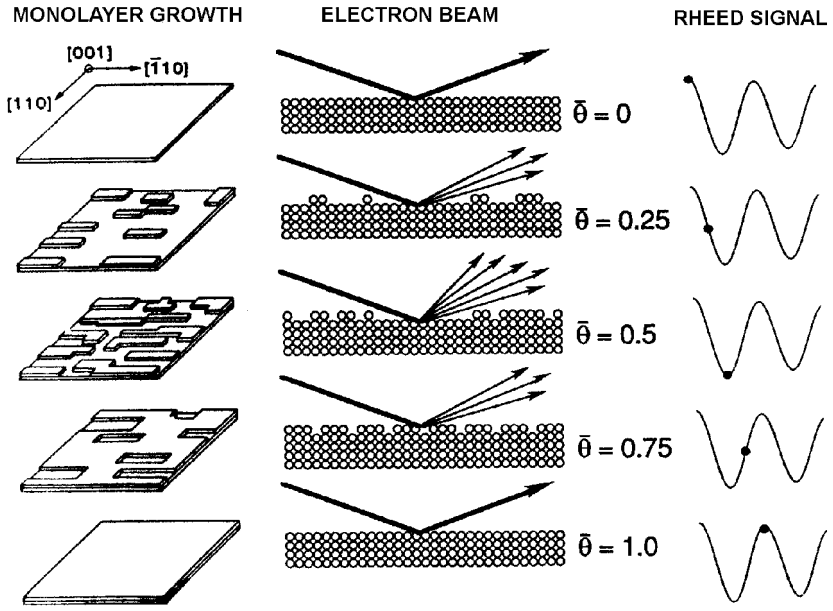

Figure A.5: Model demonstrating the correlation between the order of a growing surface and the intensity of the RHEED diffracted beam. This model predicts that the completion of one mono-layer corresponds to the completion of one oscillation. [after 5]

A.4 Compositional control and growth rate of III-V binary and ternary compounds

Although the manner in which RIO is used to extract semiconductor growth rates is straightforward, the way in which they are implemented vary from material system to material system as well as from laboratory to laboratory. In fact, over the last six years, the methods for determining growth rates and compositions at EMDL have evolved and changed. One thing that has remained unchanged, is that in EMDL, a designated piece of substrate (a "RHEED piece") remains in vacuum for use during RIO, in this way, only a small piece of substrate material is needed and it can be used indefinitely. We use RIO rates and BEP values to correlate the growth rate of Group III elements to the composition of ternary and quaternary alloys, but only for mixed Group III alloys. With the recent addition of a P source, we have found that the same methods apply to both III-As and III-P alloys and that RIO analysis performed on III-As can be applied to III-P without further RIO analysis. Since Group V elements do not have unity sticking coefficient, the composition of mixed V alloys must be determined by ex-situ calibrations, while, the growth rate is still determined by the RIO of the Group III constituents. The application of RIOs and BEPs to the determination of material growth rate and composition are described in the subsequent sections.

A.4.1 GaAs and $Al_xGa_{1-x}As$:

Determining the GaAs growth rate in a MBE system with Ga and As sources is very standard because GaAs substrates are readily available and commonly used. When the RIO are recorded and analyzed, the resulting a growth rate or frequency (f) that corresponds to the number of mono-layers/second (ML/s). The physical growth rate, *R,*

in Å/s, can be determined by accounting for the lattice constant, *a*, of the material being grown. (See Equation A.1.)

$$R\left[\frac{\text{Å}}{\text{second}}\right] = f\left[\frac{\text{mono - layer}}{\text{second}}\right] \times (a/2)\left[\frac{\text{Å}}{\text{mono - layer}}\right] \qquad \text{Equation A.1}$$

Another popular semiconductor compound is AlAs. Unfortunately, Al reacts easily with oxygen and so AlAs substrates are not commonly found or used. However, since the lattice-mismatch between AlAs and GaAs is ~0.1% there is little impediment to using GaAs substrates for AlAs epitaxial film growth or for growth rate determination. Therefore, the RIO analysis of AlAs on GaAs is performed to directly measure f_{Al}; the physical growth rate.

If the desired material is an $Al_xGa_{1-x}As$ alloy, then there are two possible methods of analysis for obtaining the alloy's composition and growth rate. In the first approach the independent AlAs and GaAs growth rates are measured via RIO analysis and are consequently used in Equation A.2 to determine the composition and in Equation A.3 to determine the growth rate. Since both Ga and Al rates are determined on a GaAs substrate, the *f* values in ML/s can be compared directly.

$$x = \frac{f_{AlAs}}{f_{AlAs} + f_{GaAs}} \qquad \text{Equation A.2}$$

$$f_{Al_xGa_{1-x}As} = f_{GaAs} + f_{AlAs} \qquad \text{Equation A.3}$$

In the second approach, the $Al_xGa_{1-x}As$ rate, f_{AlGaAs}, is determined directly from RIO analysis by opening both Al and Ga shutters. This rate is used with either the AlAs or the GaAs rates as in Equation A.4 and Equation A.5 to determine the Al composition, x.

$$x = \frac{f_{AlAs}}{f_{Al_xGa_{1-x}As}} \qquad \text{Equation A.4}$$

$$1 - x = \frac{f_{GaAs}}{f_{Al_xGa_{1-x}As}} \qquad \text{Equation A.5}$$

Calculating the physical growth rate in Å/s, R, of the ternary alloy and a mismatched binary is a more complicated process because it requires knowledge of the perpendicular lattice parameter as well as the in-plane lattice parameter. In general, Vegard's Law or other experimental fits used to approximate the relaxed lattice parameter of the ternary. If the films are strained, then the perpendicular an in-plane lattice parameters may be altered from the calculated relaxed value. Since the lattice mismatch between $Al_xGa_{1-x}As$ and GaAs is so small, R_{AlGaAs}, can be extracted by using the $Al_xGa_{1-x}As$ lattice parameter calculated using Vegard's Law in Equation A.1 without significant error.

A.4.2 $In_xGa_{1-x}As$ and $In_xAl_{1-x}As$:

Although the manner in which growth rates and compositions are determined does not change, the manner in which they are experimentally obtained becomes more complicated when dealing with highly mismatched systems as well as epitaxy on different substrates. In this case, the lattice mismatch between InAs and GaAs is ~ 7% so

direct growth is not an option. Direct growth would generate many defects and thus would destroy the surface order needed for RIO. Moreover, the "RHEED piece" would consequently not be available for GaAs rate determination either. If the In mole fraction were low enough, it might be possible to obtain an $In_xGa_{1-x}As$ or $In_xAl_{1-x}As$ rate via the approach described by Equation A.5. From this an InAs rate could be extracted. Unfortunately, the compositions of $In_xGa_{1-x}As$ and $In_xAl_{1-x}As$ typically used are lattice matched to InP substrates, which represents a ~3.5% lattice mismatch to GaAs; consequently, direct ternary growth on GaAs at typical compositions is not an option either. (Since $In_xGa_{1-x}As$ and $In_xAl_{1-x}As$ at a given In composition are fairly lattice matched the case of $In_xGa_{1-x}As$ will be presented here as representative for both ternary compounds.)

One solution to this problem would be to increase the Ga rate (f^a_{GaAs}) in order to decrease the In mole fraction and thus the degree of lattice-mismatch; however, this requires obtaining an extra Ga rate that would otherwise not be necessary. The rate, f^a_{InGaAs} represents the number of mono-layers/second of $In_xGa_{1-x}As$ when grown on GaAs and it is not the desired $In_xGa_{1-x}As$ rate, f^b_{InGaAs}. From this, the InAs rate (f_{In}) must be extracted and then, by adding it to the desired GaAs rate, f^b_{GaAs}, the final $In_xGa_{1-x}As$ rate and composition are obtained. This is demonstrated in Equation A.6 - Equation A.8.

$$\left(f_{In}\right)_{onGaAs} = \left(f^{a}{}_{In_xGa_{1-x}As}\right)_{onGaAs} - \left(f^{a}{}_{GaAs}\right)_{onGaAs} \qquad \text{Equation A.6}$$

$$\left(f^{b}{}_{In_xGa_{1-x}As}\right)_{onGaAs} = \left(f^{b}{}_{GaAs}\right)_{onGaAs} + \left(f_{In}\right)_{onGaAs} \qquad \text{Equation A.7}$$

$$1 - x = \frac{f^{b}_{GaAs}}{f^{b}_{In_xGa_{1-x}As}}$$ Equation A.8

This method is very impractical if many $In_xGa_{1-x}As$ are desired since it requires two Ga rates for every $In_xGa_{1-x}As$ composition. Moreover, the oscillations are poor due to the high growth rates and the lattice-mismatch which can introduce more uncertainties. [2]

A more ideal solution for calculating the composition from RIO requires a second "RHEED piece" which uses a substrate other than GaAs. An obvious solution would be to use an InAs substrate to directly measure the InAs rate. Since this substrate is uncommon EMDL initially used a metamorphic InAs buffer grown on an InP substrate for InAs RIO; however, since the surface morphology of lattice-mismatched layers is often rough the oscillation were not very strong. Recently, EMDL procured an InAs substrate for InAs RIO analysis and strong oscillation are now obtained. Since the InAs rates are determined on an InAs substrate, the rates must be scaled for a GaAs substrate in order to compare the InAs and GaAs rates, as in Equation A.9. Consequently, the composition and growth rate with respect to a GaAs substrate can be found using Equation A.10 and Equation A.11.

$$\left(f_{InAs}\right)_{onGaAs} = \left(\frac{a_{GaAs}}{a_{InAs}}\right)^2 \left(f_{InAs}\right)_{onInAs}$$ Equation A.9

$$x = \frac{\left(f_{InAs}\right)_{onGaAs}}{\left(f_{InAs}\right)_{onGaAs} + \left(f_{GaAs}\right)_{onGaAs}}$$ Equation A.10

$$\left(f_{In_xGa_{1-x}As}\right)_{onGaAs} = \left(f_{GaAs}\right)_{onGaAs} + \left(f_{InAs}\right)_{onGaAs}$$ Equation A.11

Once the Ga and In rates and the composition are determined the relaxed lattice parameter can be estimated. If the $In_xGa_{1-x}As$ is grown on an InP and it is fully strained, then Equation A.12 and Equation A.13 are used to calculate the growth rate in ML/s and Å/s, respectively. If the layers are relaxed, then Equation A.14 and Equation A.15 should be used. Again, these are estimates of growth rate in lattice-mismatch cases since the degree of relaxation and the perpendicular lattice parameter cannot be known a priori.

$$\left(f_{In_xGa_{1-x}As}\right)_{onInP} = \left(\frac{a_{InP}}{a_{GaAs}}\right)^2 \left(f_{In_xGa_{1-x}As}\right)_{onGaAs} \qquad \text{Equation A.12}$$

$$\left(R_{In_xGa_{1-x}As}\right)_{onInP} = \left(\frac{a_{InP}}{a_{GaAs}}\right)^2 \left(f_{In_xGa_{1-x}As}\right)_{onGaAs} \left(\frac{1}{2}\left(\frac{\left(a_{In_xGa_{1-x}As}\right)^3}{a_{InP}}\right)^{1/2}\right) \qquad \text{Equation A.13}$$

$$\left(f_{In_xGa_{1-x}As}\right)_{onIn_xGa_{1-x}As} = \left(\frac{a_{In_xGa_{1-x}As}}{a_{GaAs}}\right)^2 \left(f_{In_xGa_{1-x}As}\right)_{onGaAs} \qquad \text{Equation A.14}$$

$$\left(R_{In_xGa_{1-x}As}\right)_{onIn_xGa_{1-x}As} = \left(\frac{a_{In_xGa_{1-x}As}}{a_{GaAs}}\right)^2 \left(f_{In_xGa_{1-x}As}\right)_{onGaAs} \left(\frac{a_{In_xGa_{1-x}As}}{2}\right) \qquad \text{Equation A.15}$$

A.4.3 Using BEP values for compositional analysis

As mentioned above the BEP sensitivity factors can be determined for ternary alloys from ex-situ X-ray analysis of grown compounds. For example, if the BEP values for In and Ga are known, and the composition, *x*, is determined from x-ray diffraction

from an $In_xGa_{1-x}As$ layer, the sensitivity factor of In with respect to Ga can be determined by solving for S_{In} in Equation A.16.

$$x = \frac{S_{In}(BEP_{In})}{S_{In}(BEP_{In}) + BEP_{Ga}} \qquad \text{Equation A.16}$$

Moreover, if S_{In} is known than the composition, x, can be estimated from the BEP values alone using Equation A.16. If the sensitivity factor, S_{In}, is consistent for all BEP values then S_{In} can be used with In and Ga BEP values to calculate compositions for all $In_xGa_{1-x}As$ alloys.

Now, if a relationship between BEP values and RIO rates, f, can be defined, then alloy growth rates can also be inferred from the measured BEP values used. Fortunately, for a given system condition, f can be correlated with the measured BEP from a Group III cell. By measuring RIO at various Ga rates a Ga BEP versus f plot can be generated. This plot is linear and so it can be used to interpolate the Ga BEP values for other Ga rates as well. Since RIO for InAs, AlAs, and GaAs can be independently measured, we can plot BEP versus f for each. If we adjust f for each, such that they are all referenced to a GaAs substrate, as in Equation A.9, then we can determine the sensitivity factors for In and Al BEP values by determining the multiplicative factor that causes all three curves to converge to one slope. The experimental data, shown in Figure A.6, was measured in EMDL; the BEP sensitivity factors were found to be $S_{In} = 0.664$ and $S_{Al} = 2.03$ for a Ga BEP reference. It should also be noted that these sensitivity factors are similar to those determined from x-ray analysis of near lattice-matched alloys and variations are only due to the accuracy in which BEP values, X-ray composition, and rates are measured for a

given growth. This method of comparing RIO rates is more accurate since it allows a best match over several data points and BEP measurement conditions and does not require growth of a layer or ex-situ analysis.

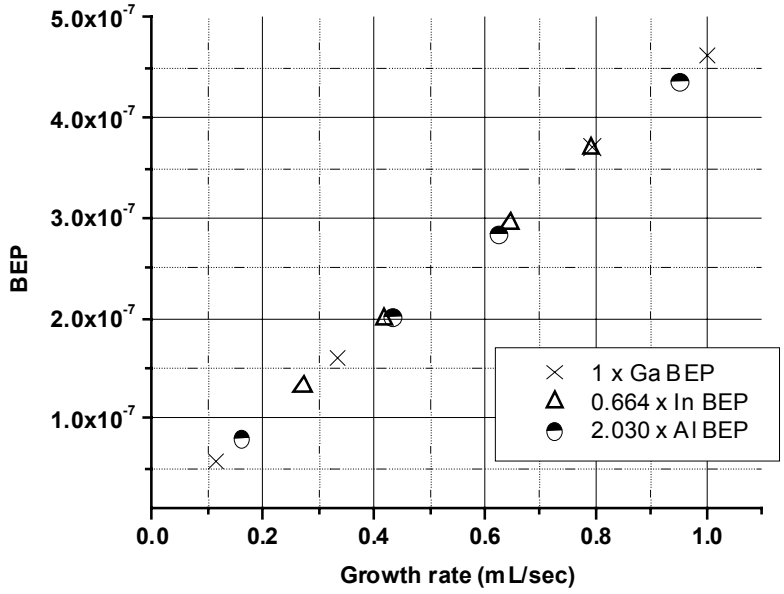

Figure A.6: The measured BEP values multiplied by the determined sensitivity factor versus the growth rate relative to a GaAs substrate for Ga, Al and In Group III cells.

From a linear fit to this curve the growth rate at a particular BEP value can be determined with reference to a GaAs substrate; by using a combination of these values and Equation A.12 - Equation A.15 the growth rate for any ternary alloy can be determined. These equations can be easily extended to quaternary alloys, and we have found that consistent quaternary compositions and growth rates are also obtained using this method. Moreover, if the same Ga and In BEP values used in an $In_xGa_{1-x}As$ alloy are

used in an $In_xGa_{1-x}P$ alloy, the composition remains fixed but the growth rate is altered by the substrate choice and the difference lattice parameter.

Using BEP for composition control and growth rate evaluation is more practical than measuring the RIO rates prior to each growth since it requires much less time. Consistent technique when measuring the BEP values improves the accuracy of this method; such as measuring the Group III BEP values prior to exposing the chamber to As or P fluxes since this can change the back ground pressure measured by the ion gauge. This method does require that a few RIO values be periodically checked to ensure that the BEP versus *f* curves have not shifted. Shifts in this curve can occur and are usually attributed to excessive coating of the ion gauge filaments.

A.5 References

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APPENDIX B

CHARACTERIZATION OF EPITAXIAL GE BY SSMBE AND IMPLICATIONS FOR III-V /GE AND III-V/SIGE DEVICES

As mentioned earlier, the use of epitaxial Ge was and important factor in reducing the carbon contamination from the Ge substrate. Although, carbon contamination is reduced, the purity of the epitaxial Ge layer is impacted by the presence of Group III and Group V elements in the SSMBE chamber. In this appendix we investigate the properties of SSMBE grown Ge with two different cell positions and three different sources. We found that the lateral uniformity was impacted by the aperture present in the cryo-shroud and the length of the Ge effusion cell used. Moreover, the concentration of trace elements was a function of both the effusion cell and the position in the chamber. We were able to achieve n-type Ge conductivity through the use of a newly designed integral cooling effusion cell.

B.1 SSMBE of Ge

The growth of epitaxial Ge using effusion cells in SSMBE has not conventionally been performed. The first limitation is that Ge has a very high melting point (937°C) and

low vapor pressures, such that typical evaporation rate are less than 0.1μm/hour [1]. Secondly, epitaxial Ge for SiGe growth by effusion cells are even more complicated since Si has an even higher melting point (1412°C) and corrodes conventional crucible material (pyrolitic boron nitride, PBN). Most epitaxial SiGe is grown by chemical vapor deposition or deposited by e-beam; however, recent advancements in effusion cell technology has made epitaxial Ge a reality; however, it is still plagued by slow growth rates and contamination from the degradation of various crucible/liner materials. The use of Ge in this research does not require thick layers or fast growth rates so epitaxy using effusion cells was attempted.

The effusion cells used for Ge epitaxy are described in Table B.1. It shows a large range of thermocouple temperatures and background chamber pressures. At high temperatures the PBN crucible begins to decompose and thus there are increased levels of nitrogen in the UHV chamber. The thickness of the Ge layer as function of position was determined by growing a thin layer of Ge on a GaAs wafer. Due to the difference in the index of refraction of Ge and GaAs, and x-ray rocking curve of the 004 planes shows thickness fringes [2]. Using a fitting program called RADS Mercury written by Bede Scientific, we were able to determine the thickness of the Ge layer as shown in Figure B.1. Since the D1 x-ray diffractometer at The Ohio State University is equipped with an X-Y stage, translation of the sample allowed a layer thickness profile across the wafer to be determined. Figure B.2 shows this profile for cell B and Cell C; the profile from Cell B is more uniform than from Cell C. This results from the difference in length of the cell; cell B is ~ 1 inch shorter. It should be noted that the orifice in the cryo shroud through which the molecular beam passes is 2 inches in diameter. Since the machine was

originally design for 2” wafers this would not have presented a significant problem with uniformity from these ports; however, a 3” wafer used here has 30% reduction with in 0.5 inches from the edge of the wafer if grown using either cell B or cell C.

Cell Description	Growth Rate	Operating Temperature	Background pressure
A: HT cell	~0.1 μm/hr	1460 °C	~ 1e-8 torr
B: LT cell	~0.1 μm/he	1050°C	~ 4e-10 torr
C: Cooled Cell	~ 0.09 μm/hr	1250°	~ 3e-10 torr

Table B.1 Description of performance characteristics for the three Ge effusion cells used in this thesis

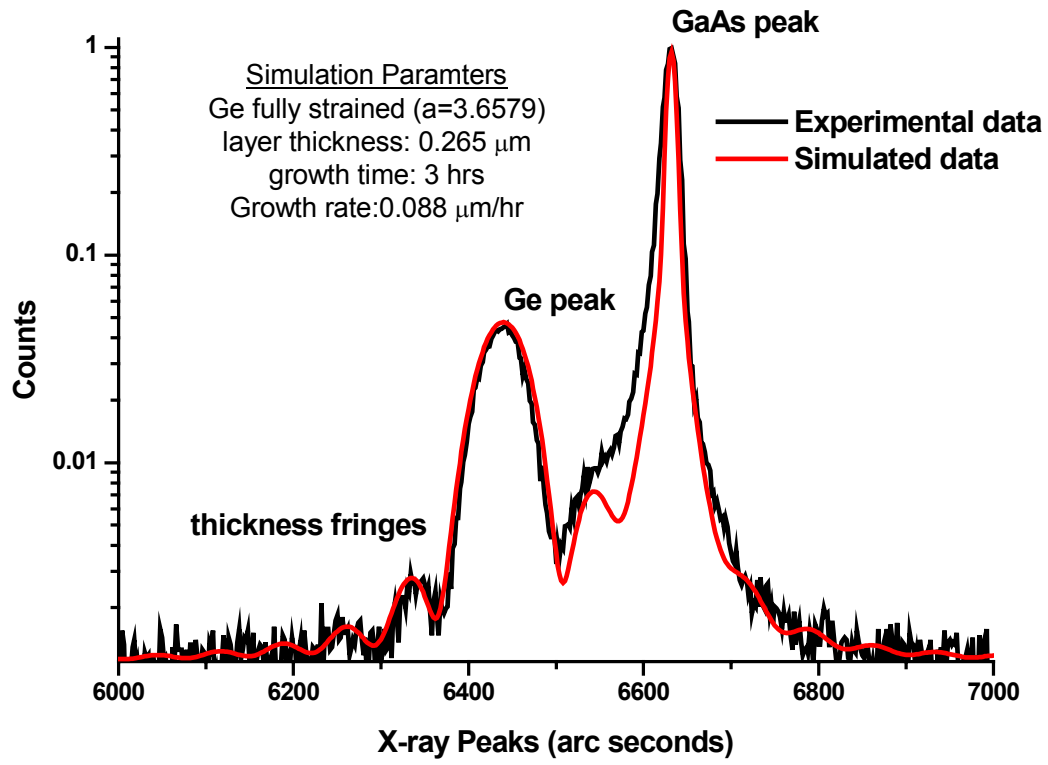

Figure B.1 X-ray rocking curve from an epitaxial Ge layer on a GaAs susbtrate. The plot shows the experimental data and the simulated rocking curve data using RADS Mercury.

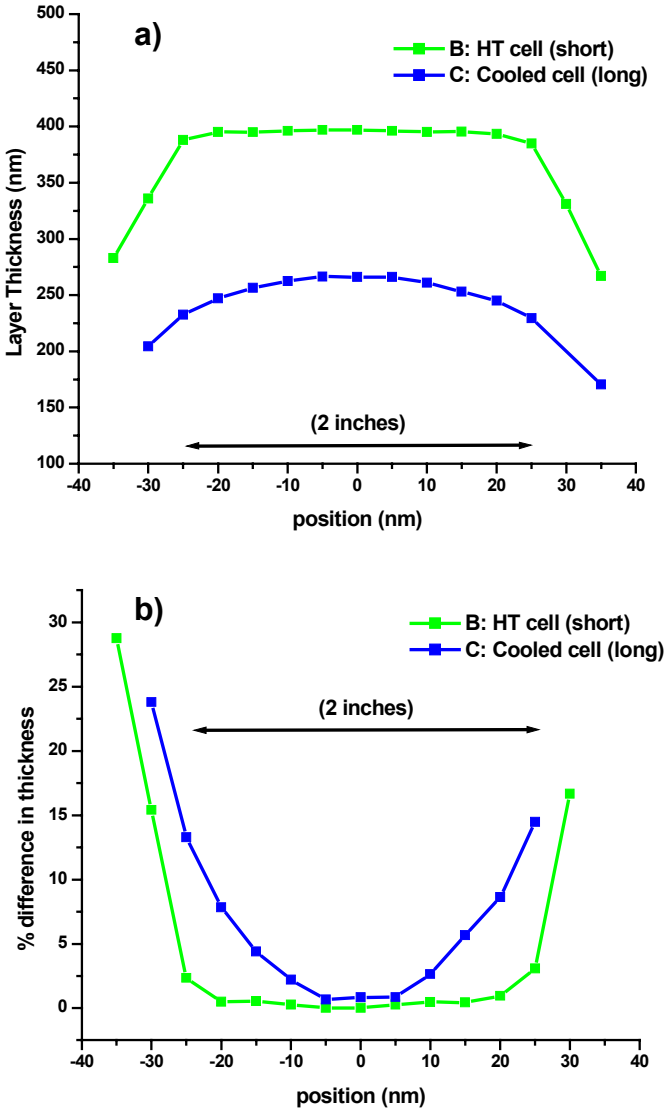

Figure B.2 The Ge layer uniformity from the LT cell (B) and Cooled cell (C). a) Shows the layer thicknesses a function of position where "0 nm" represents the center of the wafer. b) Shows the percent difference in thickness as a function of position.

The conductivity of these epitaxial Ge layers varies for the different cells which is associated with the effusion cell temperature as well as the effusion cells' ability to radiatively heat the surrounding area (i.e. chamber walls and cyro shrouds). The main impurities of interest were aluminum (Al), arsenic, (As), and phosphorus (P) whose concentrations were measured by secondary ion mass spectroscopy (SIMS). Since the level of both III and VI elements are of interest the samples needed to be grown on a Ge substrate to insure that Ga and As did not out diffuse from the substrate. The HT cell (A) had the highest levels of Al and As contamination, 4×10^{18} cm^{-3} and 4×10^{18} cm^{-3} respectively. Although these concentrations are similar, the Al impurities compensated the As impurity concentration and the Ge layer had p-type conductivity. Subsequent growths with this cell produced Al concentration up to 2×10^{19} cm^{-3} which resulted from significant the evaporation of Al in the chamber in attempt to remove oxygen contamination form the Al effusion cell.

The LT cell (B) had lower Al concentration and lower As concentration; however, the Al doping, 1×10^{18} cm^{-3}, was able to compensate the n-type As doping, 4×10^{17} cm^{-3}, thus the Ge layer again had p-type conductivity. The lower effusion cell temperature reduced the amount of radiative heating to the wall of the chamber thus reducing the concentrations of Al and As. Using the cooled effusion cell (C) the level of Al was less than $< 1 \times 10^{17}$ cm^{-3}, while still higher than desired, the As concentration, $\sim 1.5 \times 10^{18}$ cm^{-3}, was sufficient to compensate the Al concentration and thus the Ge layer had n-type conductivity. Although Cell C operated at a higher cell temperature than Cell B, the ability to transmit heat to the walls of the chamber was significantly reduced by the integral cooling of the cell. Moreover, the increase in As is attributed to the large amount

of As deposited in the chamber after the use of cell B and immediately before the use of cell C and the increased heating of the cryo shroud opening due to the closer proximity of the cell to the cryo shroud sue to the longer cell length.

The increase is As concentration as the Ge was grown with Cell C is real and is attributed to the gradual heating of the cryo shroud wile the layer was being grown. This doping profile was confirmed by electrochemical capacitance voltage (ECV) profiling as shown in Figure B.4. ECV data for the p-type Ge layers is not presented because the CV and IV are very poor due to the poor quality of the material. The ECV measurements did show p-type conductivity, however, they did not profile well. This was not the case for Cell C, which gave both nice IV and CV curves. To confirm that the p-type Ge layers were indeed p-type, diodes were processed on these samples since each Ge layer was grown on a n-type Ge substrate. These IV curves are shown in Figure B.5.

There is no SIMS data concerning the P incorporation using Cell A since this cell was used prior to adding a Phosphorus source to the SSMBE chamber. Comparing cell B and cell C, we find that the level of P is much higher in the Cooled cell. The P concentration of $7x10^{17}$ cm^{-3} may also contribute the n-type conductivity of this layer. Again this is due to the accumulation of P in the chamber as well as the increased heat load since the cell is hotter and closer to the cryo shroud.

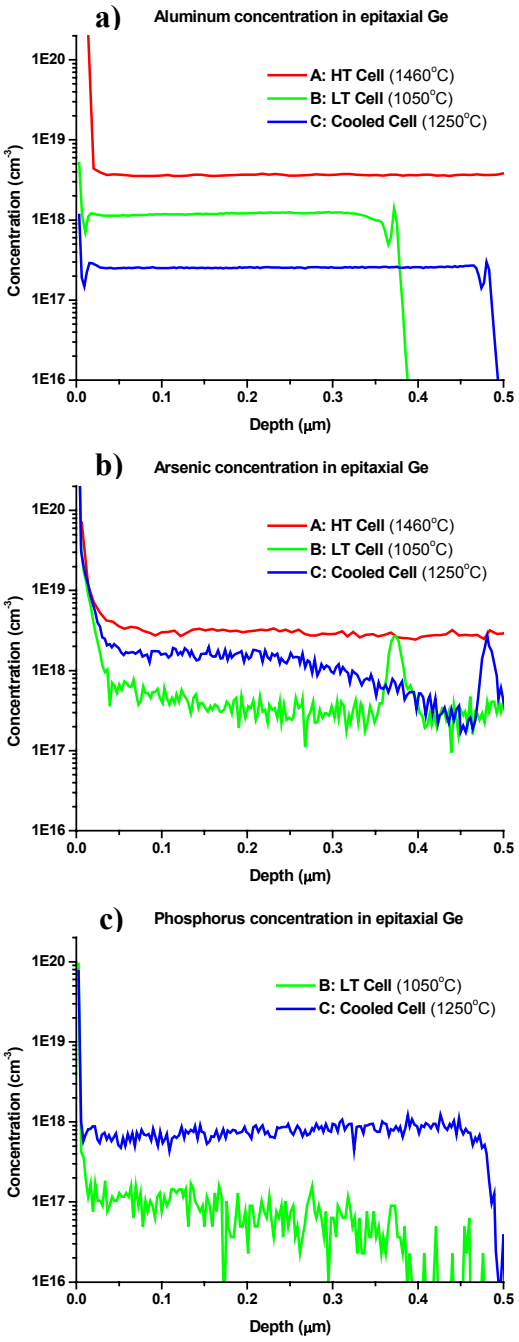

Figure B.3 SIMS profiles for a) aluminum, b) arsenic, and c) phosphorus for all three Ge effusion cells.

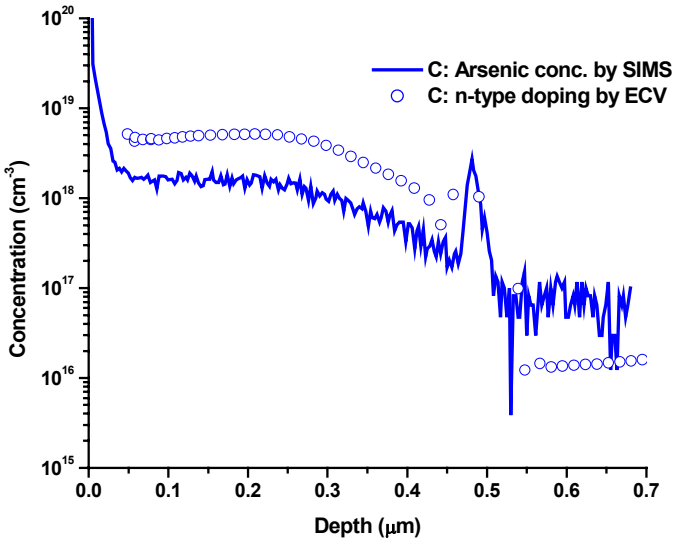

Figure B.4 Doping concentration profile for the n-type Ge layer grown with the Cooled effusion cell (C). This plot shows both the SIMS and ECV data.

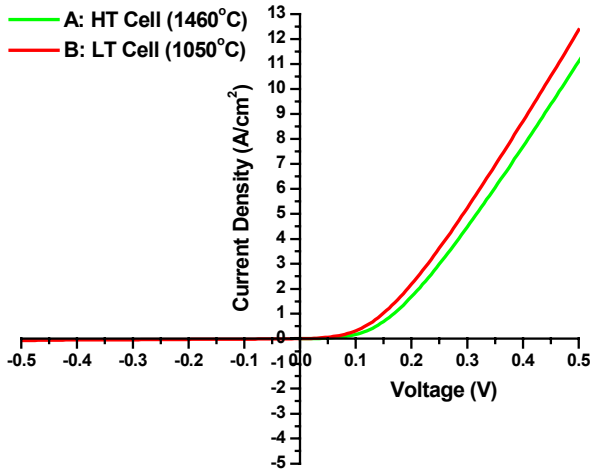

Figure B.5 These I-V curve confirms the presence of a p-n junction formed by a p-type epitaxial Ge layer and a n-type Ge substrate.

B.2 References

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APPENDIX C

XRAY DIFFRACTION

The use of X-ray diffraction in this Ph.D. research has focused on the determination of alloy compositions, the determination of relaxation in lattice-mismatched epitaxial layers, and the determination of epitaxial layer tilt. Before describing how such information is ascertained from X-ray diffraction, a review of the geometry of diffraction, the geometry of the zinc-blend crystalline lattice as well as the geometry of the corresponding reciprocal lattice are provided. Moreover, the orientation of a nominally (001) substrate and the accessibility of diffraction from various sets of planes (or reciprocal lattice points) from such a substrate is described. From this foundation basic analysis procedure for determining the structural properties of lattice-mismatched epitaxial layers is presented.

C.1 Bragg's Law

The most basic description of diffraction is given by Bragg's law, which describes the diffraction of a wave (in this case an X-ray photon) from parallel planes of a perfect infinite crystal.

$$\sin\theta_{hkl} = \frac{\lambda}{2d_{hkl}}$$ Equation C.1

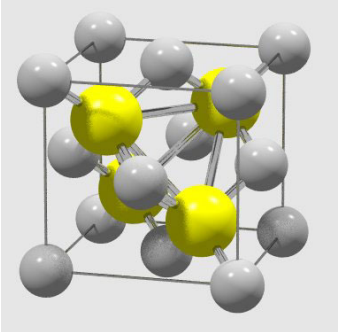
In this equation, d_{hkl} is the spacing between the *(hkl)* diffraction planes, λ is the wavelength of incident wave, and θ_{hkl} is the angle of incidence measured from the planes of diffraction to the direction of the incident wave as well as angle between the diffracted wave and the planes of diffraction. For this discussion we will consider only first order diffraction, where higher order diffractions (*n*) results from "planes" spaced *1/n* from the first order lattice spacing. We will assume a monochromatic X-ray source; thus, a unique Bragg angle (θ_{hkl}) exists for a given set of planes in a given crystal lattice. The spacing between the diffraction planes, d_{hkl}, can be found using Equation C.2 for a cubic crystalline lattice (*a*=*b*=*c*) with a lattice parameters of *a*.

$$\frac{1}{d_{hkl}^2} = \frac{h^2}{a^2} + \frac{k^2}{a^2} + \frac{l^2}{a^2}$$ Equation C.2

C.2 Zinc-Blend Lattice

The arrangement of atoms in a zinc-blend lattice is show in Figure C.1; it can be considered two face-centered cubic (FCC) lattices with an offset of <¼ ¼ ¼>. In general, a zinc-blend lattice consists of two different atoms, each occupying a given FCC sub-lattice. In the case of III-V semiconductors, one FCC lattice houses the Group III atoms while the other houses the Group V atoms. It should be noted that certain ternary and quaternary III-V compounds have varying degrees of order on the Group III FCC sub-lattice, which can affect diffraction conditions. The lattice vectors for a III-V zinc-

blend binary alloy are given in Figure C.1. A diamond lattice has the same lattice vectors as the zinc-blend lattice, but normally consist of a single type of atom; both Si and Ge have a diamond lattice.



4 - Group III atoms: a<0,0,0>, a<0, ½, ½>, a<½, 0, ½>, a<½, 0, ½>
4 - Group V atoms: a<¼, ¼, ¼>, a<¼, ¾,¾>, a<¾, ¼,¾>, a<¾,¾,¼>

Figure C.1: Zinc-blend unit cell and the respective lattice vectors for the 8 atoms of the unit cell.

C.3 Structure Factor

In order to properly consider diffraction from a crystalline lattice, the diffracted waves from each atom of the lattice need to be considered and the resultant amplitude of the diffracted wave determined. The structure factor, F_{hkl}, describes the amplitude of a diffracted wave from a particular set of atomic plane for which the Bragg condition is satisfied. The equation for calculating the structure factor is given in Equation C.3. This amplitude also depends on the ability of a particular atom (element) to scatter the incident

wave and is represented by the atomic scattering factor, f_n. The intensity of the diffracted wave is therefore determined by $I^2=F_{hkl}\,F_{hkl}^*=|F_{hkl}|^2$.

$$F_{hkl} = \sum_{1}^{N} f_n e^{2\pi i(hu_n+kv_n+lw_n)} \qquad \text{Equation C.3}$$

where:
(hkl) = plane
f_n = atomic scattering factor for atom n
$< u_n v_n w_n >$ = lattice vector for atom n
N = number of atoms in unit cell

Solving this equation for a zinc-blend alloy we find that the amplitude of diffraction from certain planes are zero while others are almost zero, and are in fact zero in the case of a diamond lattice were $f_1=f_2$. Specifically, the diffraction from (001) planes is forbidden, diffraction from (002) planes is extremely weak (almost zero), while diffraction from (004) planes is maximum. The rules for diffraction from a zinc-blend lattice based on Equation C.3 are given below.

Diffraction conditions for an (*hkl*) plane in a zinc-blend lattice:

- *hkl* mixed (even and odd) : $|F|^2=0$
- *hkl* all even: ($h+k+l$) = even multiple of 2 : $|F|^2=16|f_1^2+f_2^2|$
- *hkl* all even: ($h+k+l$) = odd multiple of 2 : $|F|^2=16|f_1^2-f_2^2|$
- *hkl* all odd: $|F|^2=16|f_1^2+f_2^2|$

C.4 Reciprocal Lattice

While a complete derivation of the reciprocal lattice and the uses of reciprocal lattice vectors are beyond the scope of this appendix, a brief introduction of the relevant diffraction issues are presented. In the reciprocal lattice, sets of parallel (*hkl*) atomic

planes are represented by a single point located a distance $1/d_{hkl}$ from the reciprocal lattice origin. A vector from the reciprocal lattice origin to the reciprocal lattice point (RLP) is the reciprocal lattice vector, $\mathbf{G_{hkl}}$, and its direction is perpendicular to the real space planes of the same indices. For cubic crystalline systems, real lattice vectors and the reciprocal lattice vectors with the same indices are parallel. An example of the reciprocal lattice for a FCC crystal is shown in Figure C.2. Note that $\mathbf{G_{004}}$ is twice the length of the $\mathbf{G_{002}}$, where as, the interplanar spacing of {004} planes is half that of {002} planes. Moreover, there is no (100) reciprocal lattice point in Figure C.2; this fact results from the structure factor for FCC crystals in which mixed indices planes (even and odd) do not diffract constructively.

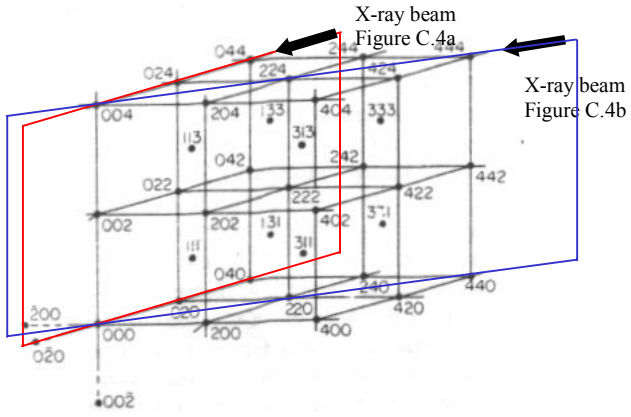
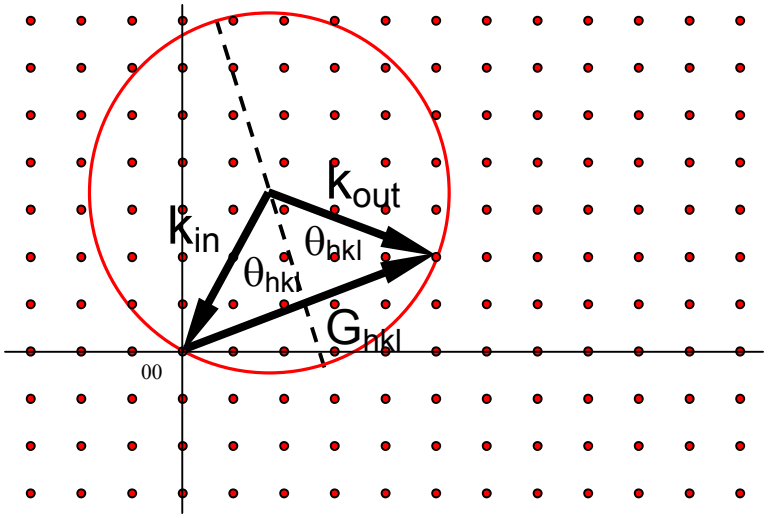


Figure C.2: A 3-D representation of a reciprocal lattice for an FCC crystal with 2-D slices. [after 1]

In reciprocal space, Bragg's law can be translated into a condition of conservation of momentum. Here, $\mathbf{k_{in}}$ represents an incident beam and $\mathbf{k_{out}}$ the corresponding diffracted beam, we are assuming elastic scattering so these vectors have equal magnitudes. Since we are in reciprocal space, the magnitude of $\mathbf{k_{in}}$ and $\mathbf{k_{out}}$ are equal to

$1/\lambda_{xray}$. Moreover, since we are using the same λ for all diffractions, we can represent the conservation of momentum condition by a sphere of radius $1/\lambda_{xray}$; this is known as the Ewald's sphere. The condition for diffraction is only met for a reciprocal lattice vector, $\mathbf{G_{hkl}}$, which connects two RLPs intersected by the Ewald's sphere. Figure C.3 shows an example of an Ewald's sphere drawn over a 2-D reciprocal lattice with $\mathbf{G_{hkl}}$ satisfying the diffraction condition as marked.



Law of sines:

$$\frac{1/\lambda}{\sin(90^\circ)} = \frac{0.5|G_{hkl}|}{\sin(\theta_{hkl})}$$

$$\sin(\theta_{hkl}) = \frac{\lambda}{2}|G_{hkl}| = \frac{\lambda}{2d_{hkl}}$$

Bragg's Law!

Figure C.3: 2-D representation of the Ewald's Sphere and diffraction condition in a reciprocal lattice.

C.5 Substrate Orientation: Real Space and Reciprocal Space

For the purposes of this exam, we will only consider diffraction from material grown on a nominally (001) substrate, thus the surface normal is ~ [001]. Therefore, as

we rotate the substrate about the [001] azimuth (we will call this Phi), we also are rotating the reciprocal lattice about the [001] axis. Since the detector has a finite aperture, the detector and the X-ray beam are coplanar. Thus, the direction of the X-ray beam needs to be 2-D plane of reciprocal space that contains the desired RLP in order to satisfy the diffraction condition and in order to detect the diffracted beam. As we rotate about the RL in Figure C.2 about the [001] azimuth, we find that the (004) RLP will always be accessible where as the {224} and {044} RLPs are only accessible at four directions of the incident beam. Two representative 2-D slices from a diamond RL are shown in the figure below; these figures represent the accessible RLPs in a diamond lattice for a given X-ray beam direction.

To get a better idea what this means in real space we will look at Figure C.5, which depicts an (001) oriented substrate. The best way to think about the necessary geometry to achieve diffraction is to ask: Given that the omega axis is always parallel to the X-ray beam, what angle of rotation (Phi) is necessary such that only omega will be moved to bring the desired diffraction plane parallel to the X-ray beam? For the (224) plane, which is in the same 2-D RL slice as the (111) plane (see Figure C.2), the x-ray beam must be in the [110] direction, where as, for the (044) plane the X-ray beam must be in the [010] direction. Since III-V crystals have {110} type easy cleave planes, the substrate's flat or a cleaved edge must be aligned perpendicular to the X-ray beam in order to axis the {224} planes; to access the {044} planes the substrate must be rotated 45° with respect to a flat/cleave.

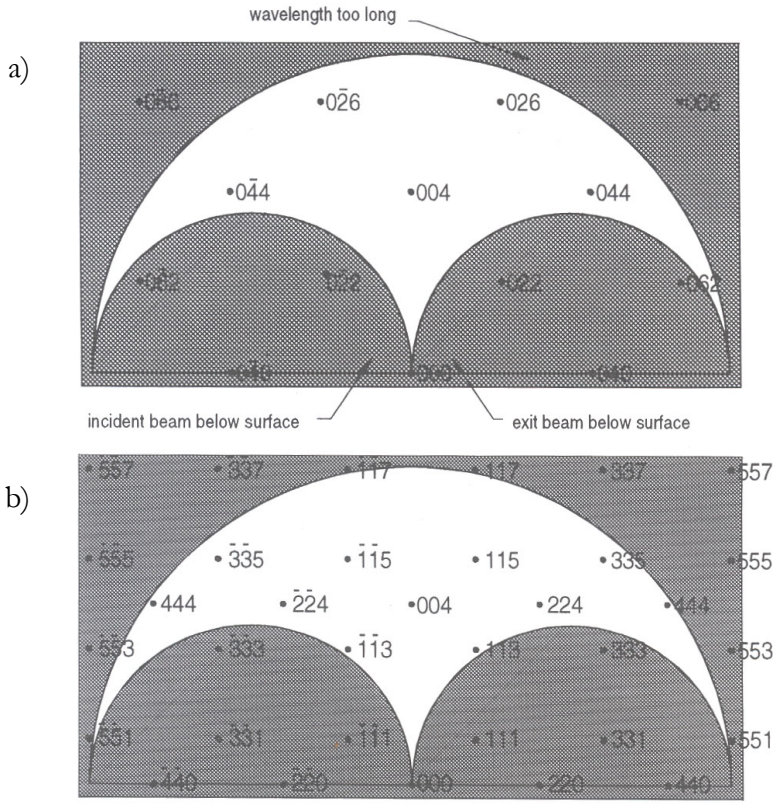


Figure C.4: The accessible and allowed reflections for a (001) Si substrate using Cu $K_{\alpha 1}$ X-rays. a) X-ray beam oriented in the [010] direction. b) X-ray beam oriented in the [110] direction. [after 2]

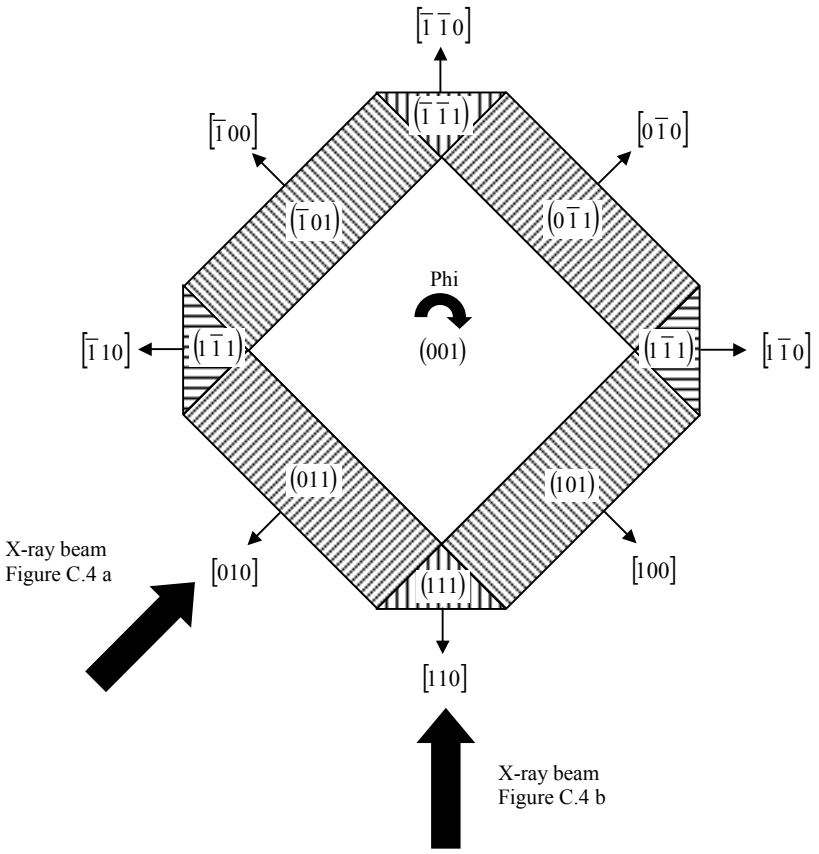


Figure C.5: Geometry of a (001) substrate and the real space orientation of the X-ray beam corresponding to the 2-D RL slices shown in Figure C.4.

C.6 Symmetric and Asymmetric Diffraction

Symmetric diffraction assumes that the diffraction planes are parallel to the surface; this is true for an on-axis (001) wafer diffracting from the (004) planes. In this case, measuring θ_{004} allows us to determine the interplanar spacing d_{004} and thus the perpendicular lattice parameter (c or $a_{\perp}$). Since epitaxial layers are generally grown on a substrate with a known lattice constant and thus a known Bragg angles, the diffraction from the substrate is most often used as a reference and the difference in Bragg angles between the substrate and epitaxial layer for a given set of planes allows the extraction of the perpendicular lattice parameter for the epitaxial layer. The geometry of diffraction usually assumes that the input X-rays and diffracted X-rays are both at the Bragg condition, however, in practicality, the X-ray source is both heavy and fragile and is left stationary. As a result, the sample axis (omega) moves to $\omega=\theta_{004}$ and the detector (2-theta) moves to twice omega, $2\theta=2\theta_{004}$. An X-ray scan or rocking curve is then taken by scanning omega while the detector (2-theta) moves at twice omega, thus, there will be optimum detection for the epitaxial layer as well as the substrate.

For an asymmetric scan, the proper geometry is obtained by moving to the appropriate Phi to access the desired planes and then moving to the Bragg angle. For this discussion, we will assume that diffraction from the {224} planes is desired. Again, the Bragg condition assumes that your planes are parallel to the surface (symmetric diffraction) and that the incident and diffracted X-rays are at θ_{224} with respect to the surface. Therefore, in order to obtain the proper geometry, the sample must be moved to the angle ϕ and then moved to the Bragg angle, where ϕ is the angle between [004] and

[224]. The angle ϕ can be determined using Equation C.4. As shown in Figure C.4 and Figure C.5, two sets of planes (or RLPs) with the same d_{hkl} are accessible at a given Phi ([001] azimuth). However, a different X-ray diffraction geometry is needed to access each RLP; these geometries are described as glancing incidence (GI) and glancing exit (GE). The real space diffraction geometries are shown in Figure C.6. For those that prefer to think in reciprocal space, imagine rotating the Ewald's Sphere in Figure C.4 until it intersects the origin and the (224) RLP versus rotating the sphere until in intersects the origin and the ($\overline{2}\overline{2}4$) RPL. These conditions represent the GI and GE geometries respectively.

$$\cos\phi = \frac{\frac{h_1 h_2}{a^2} + \frac{k_1 k_2}{b^2} + \frac{l_1 l_2}{c^2}}{\sqrt{\left(\frac{h_1^2}{a^2} + \frac{k_1^2}{b^2} + \frac{l_1^2}{c^2}\right)\left(\frac{h_2^2}{a^2} + \frac{k_2^2}{b^2} + \frac{l_2^2}{c^2}\right)}}$$

Equation C.4

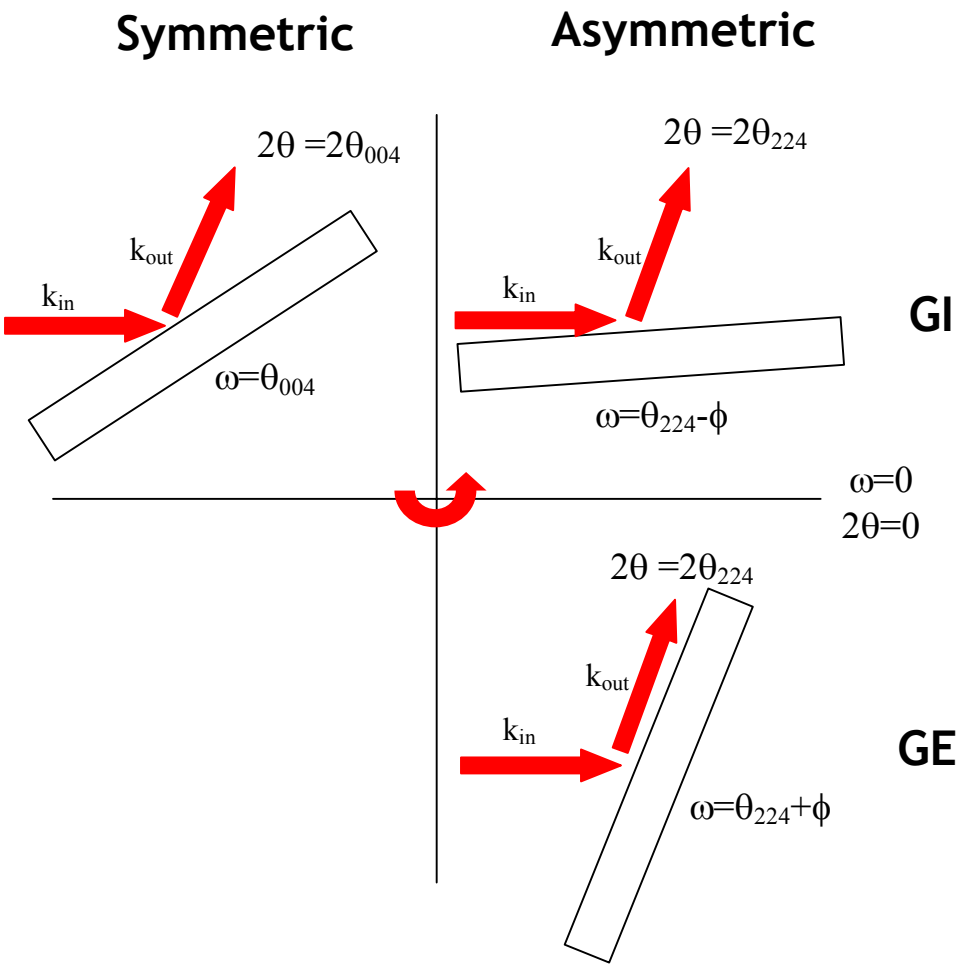


Figure C.6: Real space geometry of both symmetric and asymmetric diffraction conditions.

If both the epitaxial layer and substrate are cubic then no information is gained by performing an asymmetric scan since a=b=c and c= $a_{\perp}$ can be determined from an (004) symmetric scan. However, in reality, lattice-mismatched epitaxial layers are not usually fully relaxed and are therefore not cubic. Since the dominant relaxation planes in III-V compounds are the {111} type planes, tetragonal distortion of the lattice is assumed such that the in-plane lattice parameters relax together. By measuring {224} interplanar spacing, the {004} spacing the {220} spacing can be resolved assuming the all lattice angle are 90°, then assuming a=b=$a_{\parallel}$ for tetragonal distortion a and b are determined. The fact that the epitaxial layer is not cubic changes the asymmetric diffraction geometry since the relaxation process changes both the interplanar spacing and the angle between the diffracting planes of the epitaxial layer and the sample surface (004). The geometry of asymmetric diffraction from a tetragonally distorted epitaxial layer is described in Figure C.7. For compressive strain, the lattice distortion increases ϕ by $\Delta\phi$, for glancing incidence diffraction, the apparent omega decreases thus increasing the angular splitting between the layer peak and the substrate peak, while for glancing exit, the apparent omega increases, hence decreasing the splitting. Therefore, in order to determine the difference in Bragg angle between the substrate and a strained epitaxial layer, both glancing incidence and glancing exit measurements are required.

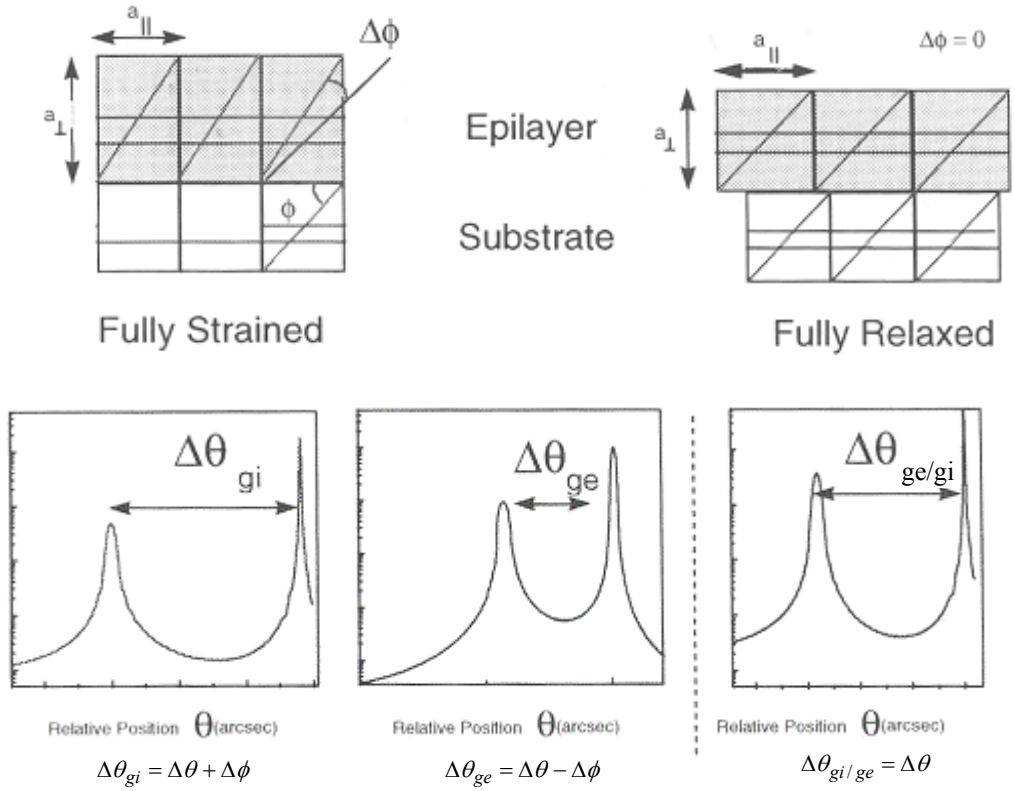


Figure C.7: This figure illustrates the impact of tetragonal lattice distortion on the angular separation between epitaxial layer diffraction planes and the substrate diffraction planes and the affect on the measured angular splitting between the epitaxial layer and the substrate for the various asymmetric diffraction geometries. [after 2]

C.7 Reciprocal Space Mapping

A reciprocal space map (RSM) is generated by completing ω-2θ scans at various ω values as indicated by the dashed lines in Figure C.8. For the symmetric RSM (in this case (004)) of an epitaxial layer in compressive strain, the in-plane lattice parameter, $a_{\perp}$, is larger than the relaxed layer lattice parameter and thus the reciprocal lattice vector is smaller. This appendix thus far has only considered crystals with {004} planes that are parallel to the crystalline surface. If there is a mis-orientation of the substrate surface in a particular direction then all scans are technically asymmetric; however, if the Phi azimuth can be oriented such that the mis-cut direction is perpendicular to the X-ray beam, the {004} planes are effectively parallel to the surface. The epitaxial layer lattice can also develop a tilt with respect the substrate thus changing the orientation of its RL with respect to the substrate's RL. In order to accurately determine the tilt of the substrate and layer the Bragg angle must be determined as a function of Phi. By fitting this data with a sine wave, the magnitude and average tilt directions can be determined as shown in Figure C.9. Although an arbitrarily orientated (004) RSM cannot determine the magnitude of tilt or the tilt direction of a layer, it does provide the projection of the tilt that is needed in the determination of the layer's lattice parameters and the degree of relaxation when used in conjunction with an asymmetric RSM at the same Phi. The shape of the RLPs in RSMs can also give a great deal of information about a crystal lattice. If there are variations in strain within a crystal this may cause broadening in ω/2θ. Moreover, if there are mis-orientations of crystalline planes within a crystal there may be broadening in ω; this is called mosaic tilt. Such effects are noted in Figure C.9.

Finally, it should be noted that the term RSM has been used in this appendix to refer to both 3-D plots of ω-2θ versus ω as well as 3-D plots of $\mathbf{k}_{\perp}$ versus $\mathbf{k}_{\parallel}$. Technically only the latter is the a RSM since it is plotted in reciprocal units; however, the conversion to RSM units is complicated by epitaxial tilt as well as substrate mis-orientation, so that data analysis provided in this exam has been completed using 3-D plots of ω-2θ versus ω.

If the epitaxial layer is fully strained with respect to the substrate, then both the layer and the substrate will have the same in-plane lattice parameter and thus the same reciprocal lattice vector, $\mathbf{k}_{220}$. Thus, a fully strained layer RLP should lay on the 100% strained line. On the other hand, if the layer is relaxed to some degree than neither the in-plane nor perpendicular lattice parameters are the same; for a fully relaxed layer the angular separation between the film and the substrates is representative of the difference in Bragg angle (as shown in Figure C.7) and thus lays on the 100% relaxed line. Since triple-axis X-ray diffraction provides high resolution in omega, such maps can be generated. It is evident from this figure that if only an ω-2θ scan is measured at a single ω, it may be difficult to determine the peak position of a strained film since the intensity of diffraction measured may be very low. As a result, many researchers rely on RSMs for determination of alloy composition and relaxation, especially when films with significant lattice-mismatched are grown.[3]

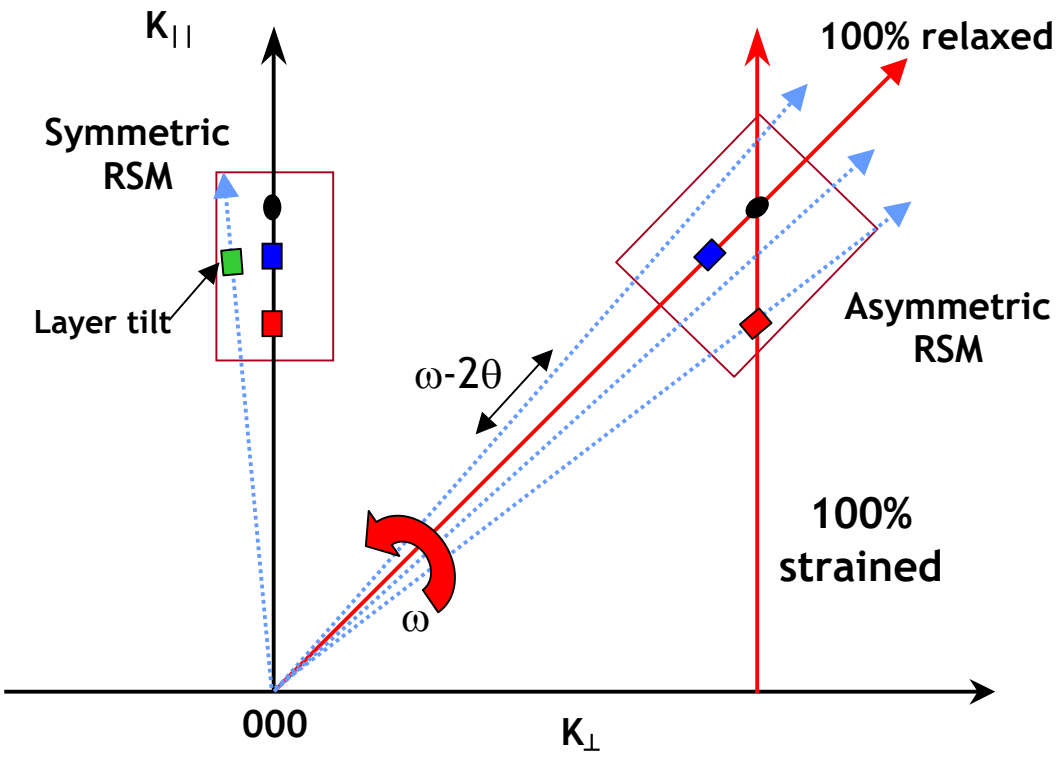


Figure C.8: Representation of reciprocal space for a full-strained and a fully-relaxed layer with a larger relaxed lattice parameter than the crystalline substrate on which was grown. Omega-2Theta X-ray scans are indicated by the dashed lines. It is clear that a single ω-2θ scan may not give a strong (224) diffraction for both the substrate and the layer if the epitaxial layer is strained. Moreover, a strong (004) diffraction may not be achieved for a layer with significant epitaxial tilt.

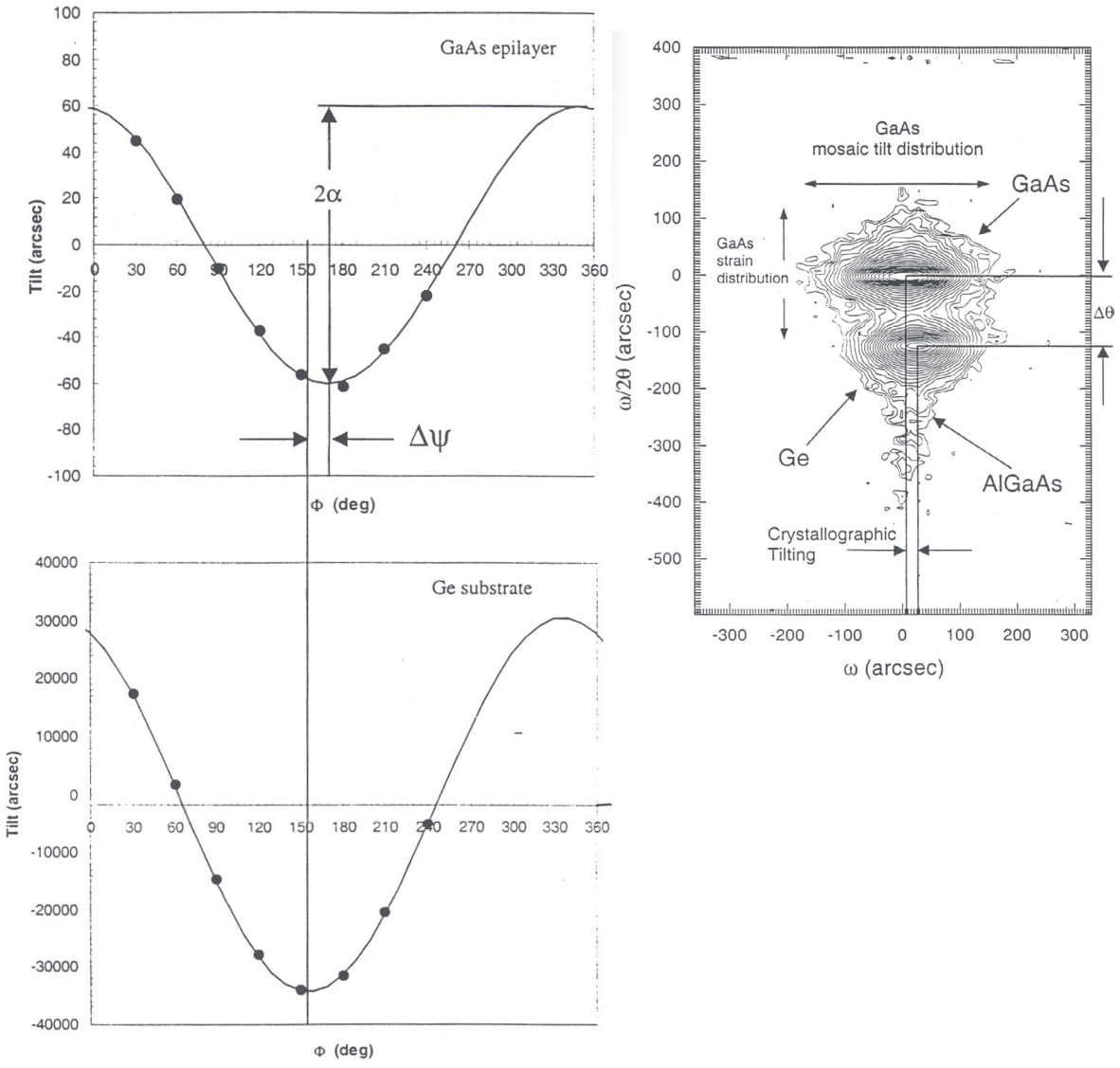


Figure C.9: Measured tilt of the GaAs layer relative to the Ge substrate and the relative tilt of the Ge substrate. The Ge substrate was mis-cut ~ 9° (~ 32400 a-sec) 26° from the [110] direction (Phi=180°); the GaAs layer is tilted an extra 60 a-sec but this tilt is out of phase with that of the substrate by an angle ΔΨ. The RSM map was taken at phi=102° which is the average tilit direction for the substrate, since the substrate and layer tilts are only slightly out of phase, the amplitude of the tilt in the RSM is ~ 60 a-sec. [after Ref. 4]

C.8 Analysis of RSM

For the reasons given above, RSMs are often used for determination of alloy composition and relaxation of epitaxial layers. In order to proceed with this analysis, the determination of reciprocal space vectors from both glancing incidence and glancing exit RSMs will be presented. The analysis given is based on using data obtained from the ω-2θ vs ω maps. Many software programs sold with diffractometers can transform the diffractometer data into RS and thus the maps can be plotted in RS units, in such cases the in-plane and perpendicular reciprocal space vectors can be measured directly. As mentioned before, the {224} map can be used in conjunction with the {004} map at the same Phi to extract the in-plane and perpendicular reciprocal space vectors and thus the in-plane and perpendicular lattice parameters. The deviation in the omega position in the {004} map (ie. GaAs layer position in RSM of Figure C.9) is used in such analysis to account for layer tilt and any apparent tilt due to substrate mis-orientation that alters the measured $\mathbf{k_{224}}$ vector. After resolving the reciprocal lattice vector components Equation 1.5 - Equation 1.10 are used to determine the layer properties. From the relaxed lattice parameter, a_r, the composition of a given a III-V ternary alloy can be ascertained using Vegard's Law or a model that calculates ternary alloy composition as a function of lattice parameter. Since the Poisson ratio, ν, as a function of alloy composition is not always known Vegard's Law may also be employed; however, a value of 0.33 is typically used for most III-V alloys.

$$a_{\parallel} = \frac{(h^2 + k^2)^{1/2}}{k_{\parallel}}$$ Equation C.5

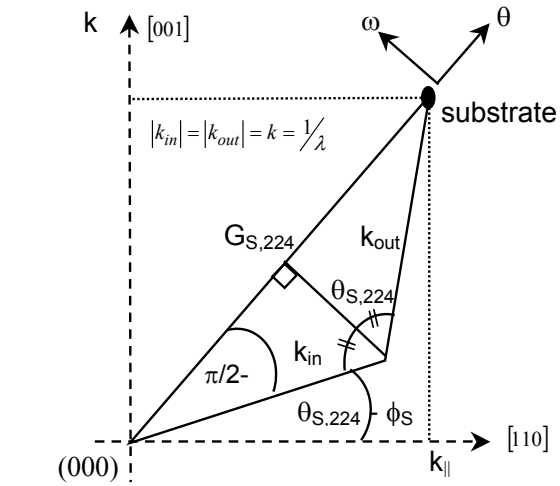
$$a_{\perp} = \frac{l}{k_{\perp}}$$ Equation C.6

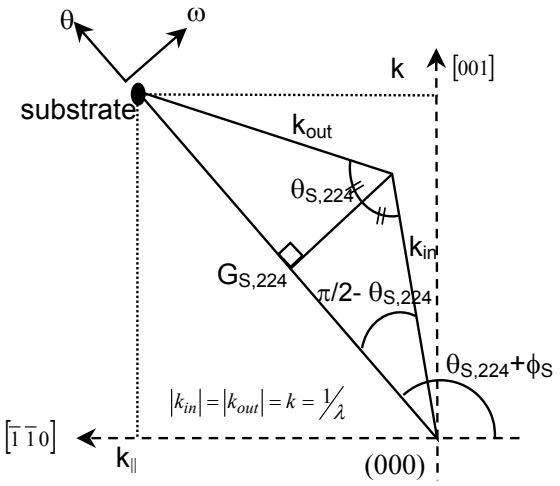
$$a_r = \frac{(1-\nu)}{(1+\nu)} a_{\perp} + \frac{(2\nu)}{(1+\nu)} a_{\parallel}$$ Equation C.7

$$strain = \frac{a_{\parallel} - a_r}{a_r}$$ Equation C.8

$$misfit = \frac{a_s - a_r}{a_r}$$ Equation C.9

$$\%\ \text{relaxation} = [1 - \frac{|\ strain\ |}{|\ misfit\ |}] \cdot 100$$ Equation C.10





{224} glancing incidence

Substrate: $G_{S,224} = 2 \cdot k \cdot \sin(\theta_{S,224})$

$$k_{||} = G_{S,224} \cdot \cos((\pi/2 - \theta_{S,224}) + (\theta_{S,224} - \phi_S)) = (2/\lambda) \cdot \sin(\theta_{S,224}) \cos(\pi/2 - \phi_S)$$

$$k_{\perp} = G_{S,224} \cdot \sin((\pi/2 - \theta_{S,224}) + (\theta_{S,224} - \phi_S)) = (2/\lambda) \cdot \sin(\theta_{S,224}) \sin(\pi/2 - \phi_S)$$

Layer: $\theta_{L,224} = \theta_{S,224} + \Delta\theta_{224}$ and $\phi_L = \phi_S - \Delta\omega_{224} + \Delta\omega_{004}$

$$k_{||} = \frac{2}{\lambda} \sin(\theta_{S,224} + \Delta\theta_{224}) \cdot \cos(\frac{\pi}{2} - (\phi_S - \Delta\omega_{224} + \Delta\omega_{004}))$$

$$k_{\perp} = \frac{2}{\lambda} \sin(\theta_{S,224} + \Delta\theta_{224}) \cdot \sin(\frac{\pi}{2} - (\phi_S - \Delta\omega_{224} + \Delta\omega_{004}))$$

{224} glancing exit

Substrate: $G_{S,224} = 2 \cdot k \cdot \sin(\theta_{S,224})$

$$k_{||} = G_{S,224} \cdot \cos(\pi - (\pi/2 - \theta_{S,224}) - (\theta_{S,224} + \phi_S)) = (2/\lambda) \cdot \sin(\theta_{S,224}) \cos(\pi/2 - \phi_S)$$

$$k_{\perp} = G_{S,224} \cdot \sin(\pi - (\pi/2 - \theta_{S,224}) - (\theta_{S,224} + \phi_S)) = (2/\lambda) \cdot \sin(\theta_{S,224}) \sin(\pi/2 - \phi_S)$$

Layer: $\theta_{L,224} = \theta_{S,224} + \Delta\theta_{224}$ and $\phi_L = \phi_S + \Delta\omega_{224} - \Delta\omega_{004}$

$$k_{||} = \frac{2}{\lambda} \sin(\theta_{S,224} + \Delta\theta_{224}) \cdot \cos(\frac{\pi}{2} - (\phi_S + \Delta\omega_{224} - \Delta\omega_{004}))$$

$$k_{\perp} = \frac{2}{\lambda} \sin(\theta_{S,224} + \Delta\theta_{224}) \cdot \sin(\frac{\pi}{2} - (\phi_S + \Delta\omega_{224} - \Delta\omega_{004}))$$

Figure C.10: Determination of reciprocal space vectors from glancing incidence and glancing exit RSMs.

C.9 Sample Analysis

The sample used in this analysis was an InGaAs layer grown on InAsP graded buffer layers grown on an (001) InP substrate with no mis-orientation. An 004 RSM and a GI 115 RSM were measured and the analysis described above was performed. The RSMs used in this analysis were measured by Yong Lin at OSU and are shown in Figure C.12; the (ω, ω-2θ) coordinates for the substrate and InGaAs layer that are used in analysis are given in this figure. The 115 RSM was also plotted in reciprocal space units (in Figure C.11) to demonstrate the RS geometry presented in Figure C.8. The angle between the fully relaxed line and the fully strained line is ϕ (from Equation C.4) which is ~15.8° for 115 and 004 planes. Since this layer has very little tilt (especially when considering the broadening in omega) the fact that the InGaAs RLP lies on the fully relaxed line suggested that it is mostly relaxed. Therefore, when viewing this structure in diffractometer units, the substrate and layer should have approximately the same omega position. Based on the analysis presented in Figure C.13 it was determined that the InGaAs composition was ~ 68% In and the layer was ~ 90% relaxed.

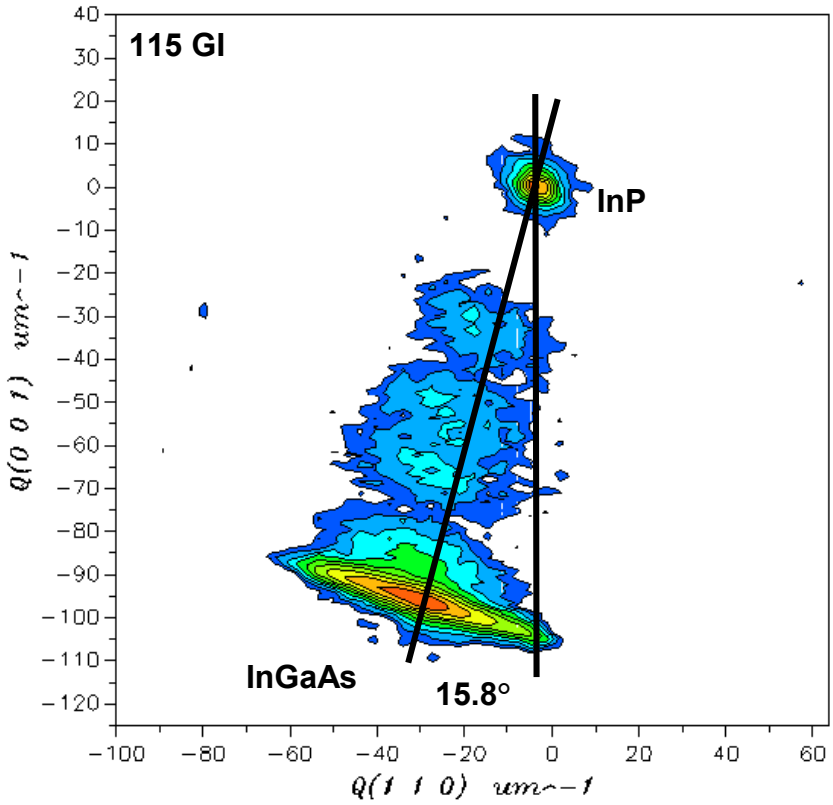


Figure C.11: GI 115 RSM in reciprocal space units. The angle indicated represents the fully strained and the fully relaxed lines denoted in Figure C.8.

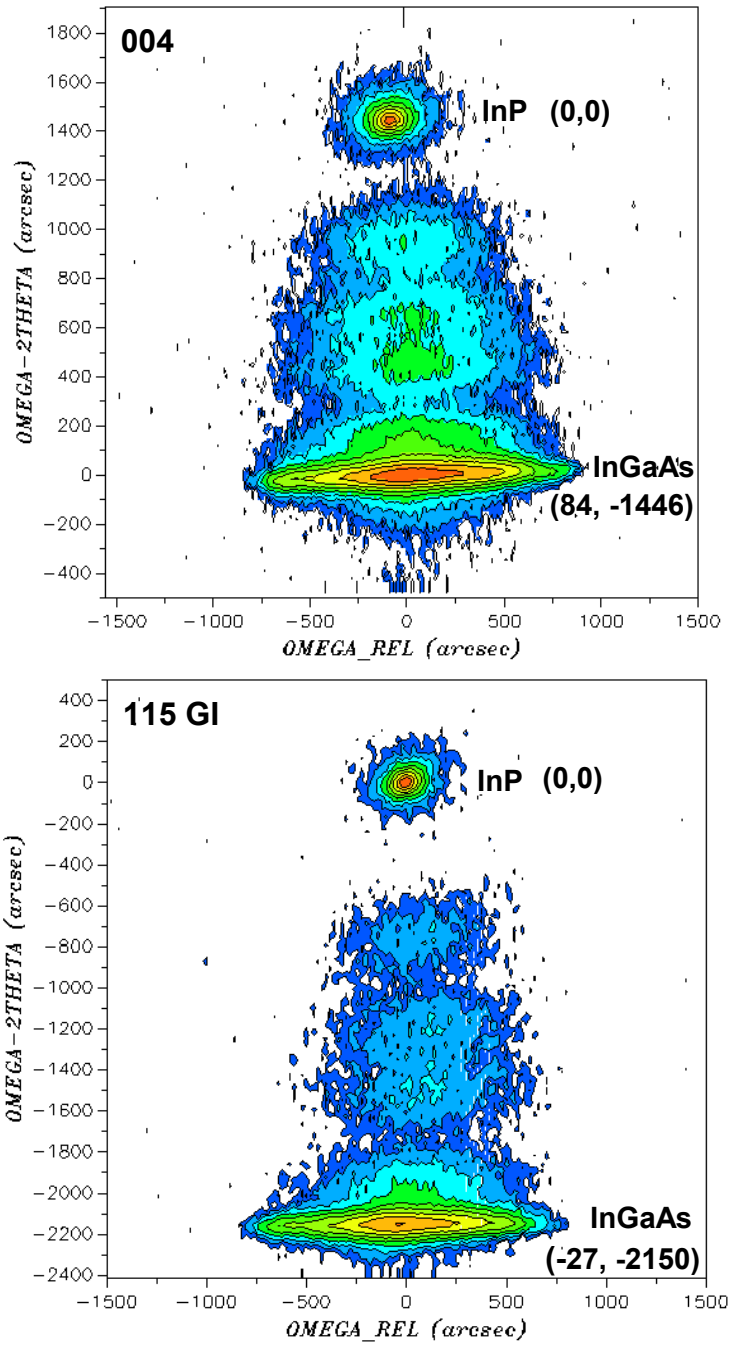


Figure C.12: The RSM plotted in diffractometer units (ω-2θ vs. ω). The (004) RSM indicates that at this Phi, the layer is tilted ~ 86 a-sec with respect to the substrate. The 115 map indicates that the substrate and layer peaks are essentially aligned in omega and since there is little tilt in this epitaxial system, that the epitaxial InGaAs layer should be almost fully relaxed. (The RSM data was taken by Yong Lin at OSU.)

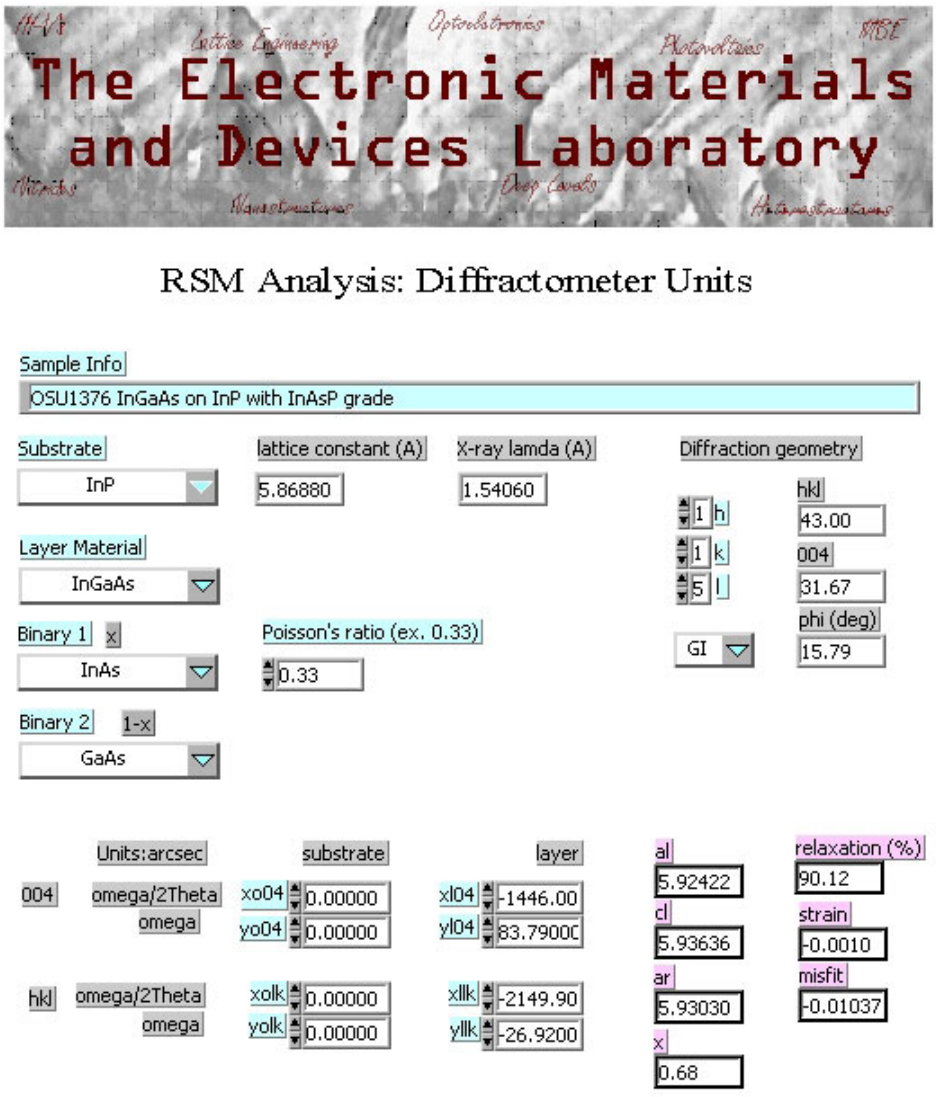


Figure C.13: A simple Labview program was written which employs the analysis method described in this document in order to provide a convenient graphical user interface for calculating layer composition and relaxation from RSM data.

C.10 References

1 J. W. Edington, *Practical Electron Microscopy in Material Science*, Virginia: TechBooks, 1976.

2 D. K. Bowen and B. K. Tanner, *High Resolution X-ray Diffractometry and Topography*, London:Taylor and Francis, 1998.

3 P. F. Fewster, *X-ray Scattering from Semiconductors*, London: Imperial College Press, 2000.

4 R. R. Hess, *A Structural Investigation of GaAs Based Solar Cells Using X-ray Diffraction*, Master's Thesis, (UCLA), 1999.

APPENDIX D

SOLAR CELL FABRICATION

The general processing information (equipment, etchants, contacts, etc.) for solar cell and diode fabrication are outlined in Section D.1. A detailed outline for the fabrication of an InGaP/GaAs DJ solar cell is presented in Section D.2. For further information on EMDL processing procedures see Ref. 1.

D.1 Processing Information

D.1.1 Processing Equipment

Specific instructions for the operation of each piece of equipment can be obtained from the Clean Room Manager. Included here are some general notes about the use of this equipment as they pertain to EMDL processing procedures.

1 Dektak - for measuring step height of PR, etch depth, metal thickness etc.
   - Place the tip down and then begin the scan.
   - Do not use auto level, level manually.
   - Do not move the x-y stage it may cause the tip to go out of range. If the tip goes out of range (a flat profile that should not be flat) then adjust the level adjustment until a scan is within range of the tip.

2 Thermal Evaporator - for thick Au or Al depositions
   - Refurbished by clean room manager, see him for current operation information.
   - Do not use boats more than 3 times. It may be best to change boats each use to avoid accidental breakage.

- Au: ~ 2.5 μm
    - Stack gold pellets end to end to achieve a more uniform deposition.
    - Increase the current slowly (over ~ 10-15 min.) and watch Au melt (~ 4 x 20A).
    - Au deposits at ~ 6 x 20A as Au depletes current will drop, increase current back to ~6 x 20A.
    - Should take ~ 10-12 min per boat for 6-7 Au pellets (~ 3 g). (Can see by eye when the Au is depleted.)
- Al depositions: ~ 1.5 μm
    - Use 2 boats with ~ 13.5" of Al in each boat.
    - Al was cleaned with DI:HCL (10:1) for 30 sec
    - Increase current slowly:
        - 3 x 40 A boat glowing
        - 3.5x 40 A Al melting
        - 4.2 x 40 A Al evaporating for ~ 4 min.

3 E-beam Evaporator - for thin or multi-layer metal deposition < 3000Å
- Usually deposit at < 3Å/s.
- Always watch the e-beam position since it can drift.
- Increase power slowly (over ~ 10 min) in order to heat up metal slowly and avoid spitting.

4 Spinner (4000 rpm, 10000 rpm/sec, 30 sec, with AZ5129)
- Always clean and inspect spinner and chuck before use.
- Select chuck based on sample size, thin wafers may bow with an o-ring.
- Spin a test wafer of similar size to your sample.
- Pry up on the edge to check vacuum for test wafer and real wafer.
- Clean chuck after each wafer.
- Do not spray acetone on sample on chuck to clean off PR.
- Cover shield with tex-wipes for easy clean up and to minimize backsplash of PR.

5 MJB3 Mask aligner (10 sec, 405 nm, Int =22.6mW/cm^2)
- Test exposure to ensure bulb and timer are operating.
- Put in contact mode with Z-position such that the substrate is not in contact with the mask, then coarsely align wafer, decrease Z-position (Clockwise rotation) and bring up the wafer further, then perform fine align. Once the wafer is in close proximity and aligned, bring wafer into contact.
- Wafer is in contact when:
    - PR is touching the mask (look at corners)
    - You can see the surface morphology of the SiGe in focus with the mask.
    - The resistance in the turning the Z-position knob increases.
- Turn off microscope bulb and return Z-position to default when finished.

6 Soft bake oven (96-97^{o}C)
   - Check the temperature when you enter.
   - Do not open the door fully and load quickly to minimize heat loss
   - Do not load more that 4 wafers with watch glasses at one time, otherwise the thermal load is too high.

7 Hard bake oven (110^{o}C)
   - Generally not need, be careful PR will burn if at 120°C for too long.

8 Small Tube Furnace - contact annealing
   - Check Furnace temperature before use. If furnace is left at > 700°C it will take hours for the temperature to reduce to 400°C.
   - Check temperature with TC and decide where the boat will sit for your anneal.
   - Capable of handling 1.4"x1.7" SiGe pieces cannot handle entire 2" wafers.

9 Thermal evaporator for evaporation of anti-reflection coating
   - See Section D.1.6 and D.2 for further details

10 Dicing Saw (WPAFB)
   - WPAFB Technician performs dicing; dicer is capable of dicing small cells and diodes.
   - It cannot stop in the middle of a cut, so plan cuts appropriately.
   - Provide a wafer map and explicit instructions for dicing and clear packaging and labels for diced samples.
   - EMDL has blades for Si substrates to be sent with samples; we have been using WPAFB blade for GaAs.
   - Specify substrate material and substrate thickness if known.

D.1.2 Etchants

These are the common etches used in EMDL device processing. It is always important to verify that you are using fresh chemicals in order to maintain consistent etch rates. In all cases acid etching should be followed by a DI rinse unless stated otherwise. Before using an etchant is a good idea to research it and test it prior to device processing use especially if a selective etch is desired.[2] Moreover, LMM layers may etch a different rate due to the presence of dislocations.

Oxide etches:

1 GaAs oxide etch
- 1:5 HCl : DI (~30s)
- Removes GaAs oxides, but does NOT etch GaAs
- Etches InGaP, AlInP, InP, AlGaAs

2 Ge oxide etch:
- 1 DI (~30s)

3 Si oxide etch:
- 1: 1 HF: DI (~30s)
- Etches Al compounds

III-V Etches:

1 Ammonium Hydroxide / Peroxide Etch
- 2 : 1 : 50 $NH_4OH : H_2O_2 : DI$
- GaAs etch rate ~3000-4000 Å/min (was ~ 6000Å/min recently)
- Ge etch rate ~slightly lower than GaAs etch rate
- Etches AlGaAs at a slower rate than GaAs
- Does not etch InGaP or AlGaInP

2 Citric Acid Etch
- 4 : 4 : 1 Citric : DI : H_2O_2
- Mix 40 grams with 40 mL of DI and use magnetic stirrer to agitate, typically 1 hour. Once mixed add 10 mL of H_2O_2.
- Etch rate ~3000 Å/min.
- GaAs with a selectivity of ~ 200 over $Al_{0.85}Ga_{0.15}As$
- Selectivity varies for Al composition and mix percentages.[3]

3 HCl Etch
- 1:1 HCl:DI
- InGaP etch rate ~1000 Å/min for InGaP (varies greatly)
- Uneven etching can be experienced, may need to use straight HCl especially if etching AlGaInP. HCl etches very quickly and is more anisotropic than diluted HCl. HCl: DI may also cause heating and cracking in epi-layers may use straight HCl for better results.
- Does not etch GaAs
- Etches Al compounds (AlGaAs)

D.1.3 Contacts and Contact Annealing

The contacts are deposited in the e-beam evaporator. If a thick contact is need for the grid metallization of a solar cell, this is performed in the thermal evaporator after the initial e-bean evaporation. Prior feeling was that the e-beam process would damage the emitter and result in poor device performance. Using "slow" deposition rates (< 3.0 Å/sec) and thin layers (< 1000 Å), results do not support this conclusion. However, recent cells with n/p configuration and thin emitter (~ 0.5 μm) had poor junction quality, and so the e-beam evaporation of ~ 2μm may have contributed to this. Contact recipes and annealing conditions used for each material will be listed as well as comments pertaining to said contacts.

GaAs contacts:

n-contact - Ni/Ge/Au
50 Å Ni 328Å Ge 672Å Au
Anneal: 400^{o}C (5 sccm N_2 for small 2" furnace)
5 min (30 sec push / 4 min anneal / 30 sec pull)

p-contact - Cr/Au
100 Å Cr 1000Å Au

The Cr-Au contact provides better "sticking" than the thermally evaporated Au-Zn contact. Moreover, due to the concerns about Zn diffusion even without a contact anneal, the Cr-Au contact that is un-annealed, appears to be a good solution. The e-beam evaporated Au/Zn/Au and Cr/Au contacts were compared by measured the IV between two adjacent contacts pads deposited on a p-type wafer. We found a similar resistance for each contact and so concluded that the Cr/Au was adequate. (This is not the best test

since we maybe dominated by the substrate and therefore cannot sense any small differences in the actual contact resistivity. TLM measurements were performed on Cr/Au and Ti/Au on an epitaxial p-type layer. It was found that the un-annealed Cr/Au provided the best contact with a contact resistance of ~ 5.3e-4 Ωcm^2 which seemed adequate.

Ni/Ge/Au contact has not been characterized on GaAs. When deposited on the front of the wafer the contact appears rough/speckled. Deposition of Ni and Ge needs to be done with care since both metals may spit. Ni takes a along time to heat up so if you do not heat slowly the deposition rate can jump quickly. This contact is not ohmic without an anneal.

Ge contacts:

n-contact - Ni/Ge/Au
50 Å Ni 328Å Ge 672Å Au
Anneal: 400^oC (5sccm N_2 for small 2" furnace)
5 min (30 sec push / 4 min anneal / 30 sec pull)

p –contact - Cr/Au
100 Å Cr 1000Å Au

Work was performed on improving n-type Ge contact using Au-Sb, however, this caused pitting on SiGe substrate and so was not used further. The measured contact resistance was 8.7e-3 Ωcm^2 for AuSb. Due to the large area of the back contacts we have resorted to using Ni/Ge/Au. Studies have not been performed on p-type Ge contacts. Cr/Au has been used on n/p Ge cells and did not exhibit FF problems. If p-Ge is going to be used further, an ohmic p-Ge contact should be investigated further.

Si contacts:

UHVCVD SiGe:

n-contact - Ni/Ge/Au
50 Å Ni 328Å Ge 672Å Au
Anneal: 400^{o}C (5sccm N_2 for small 2" furnace)
5 min (30 sec push / 4 min anneal / 30 sec pull)

p –contact - Al
~3000Å Al
Anneal: 400^{o}C (5sccm N_2 for small 2" furnace)
15-30 min (30 sec push / 15-30 min anneal / 30 sec pull)

LPCVD SiGe:

n - contact - no ohmic contact obtained

p - contact - Al
~3000Å Al
Anneal: 400^{o}C (5sccm N_2 for small 2" furnace)
15-30 min (30 sec push / 15-30 min anneal / 30 sec pull)

MIT wafers (UHV or TPS) have SiGe grown on the back-side of the wafers. Thus the back of the wafer are 100% Ge. One can conduct though the SiGe layers and make contact the Ge back side. It is unclear what the resistance ramification of this and it needs to be further studied. In some case this Ge was etched from the back and contact was made to a SiGe alloy and in other cases a Si oxide etch was used. Al contacts made to SiGe in the thermal evaporator were ~ 1.5 μm thick showed ohmic behavior; however, more recent test on different SiGe substrates and only 3000Å of Al deposited by e-beam was very resistive behavior, 53 Ωcm^2. As a result Al contact use was discontinued and Ni/Ge/Au was used instead. Moreover, since solar cells with this back contact did not degrade after dicing, this back-contact seemed suitable. E-beam evaporated Al contacts to

p-type SiGe from MIT have produced contact resistivity of ~ 5e-6 Ωcm^2 and thus this might be a suitable contact for p-Ge as well.

Amberwave substrate (ASC) have a Si exposed back-side since they are grown by a LPCVD process. The edge of the wafer have some deposits from LPCVD growth; however, since we are generally cleaving the substrate and not using the edges this is not an issue. The biggest problem was that we were unable to obtain an ohmic n-type contact. The Al contact was so bad that the FF of the cells was significantly degraded, especially after dicing. This problem was not remedied. However, since Al is a p-type dopant in Si, it worked very well for p-type ASC SiGe wafers and resulted in a contact resistivity of ~ 2e-6 Ωcm^2.

D.1.4 Photo-resist

It is import when using a new photo-resist (PR) to determine the lithography conditions prior to device processing. Although a thinner resist is suitable for most diode properties a PR thickness of ~ 3μm is needed for thick metallization. Using the Carl Suss MJB3 aligner photolithography process is much more reproducible than with the Cobilt Aligner. The basic conditions for AZ-1529 PR have been 10 sec for +PR and 10s/10s for –PR. The Developer must be mixed up for each use (4:1 AZ-351:DI).

The AZ-1529 PR has a nominal thickness of ~ 2.9 μm. This PR has an expiration date of less than 1 year after purchase. If the resist is refrigerated it will last well past expiration. How long past expiration the resist is useful has not been determined. In the "as received" form the AZ-1529 acts as a +PR. In order to refrigerate the "stock" AZ-

1529, portions should be transferred to “amber” bottles for daily use. The daily use AZ-1529 should only sit for ~3 months before being dumped and replenished from the main stock. Note, when taking the AZ-1529 from the refrigerator, allow the bottle to warm-up (a few hours or overnight) to avoid water condensation when opening.

The –PR form is made by an AZ-1529 and 1% Imidazole mixture (by weight), which should only be used for ~3 month. This is mixed by weighing a 50 ml beaker, adding ~30 ml of AZ-1529 and measuring the net weight of the PR, ex. 27.3g. Then 1% or ~ 0.27 g of Imidazole is weighed out. The Imidazole is then added to the PR in the beaker and let it sit for a couple hours (with a watch glass on top) so it can dissolve. Once dissolved the mixture can be put in an amber bottle for use; wait at least 12 hours before use. The resist thickness is also ~ 2.9 μm which is needed for thick front contact metallization. When the resist is old it will appears spotty when spun and the developing time is lengthened.

D.1.5 Masks

All mask sets have 3 levels: Front Contact, Mesa, and ARC. All new masks are generated in Auto-cad so that rendering charges are reduced. If it is conceivable that multiple copies will be need, have a mask master made. All masks are made by Advanced Reproductions and 4" glass plates are used. Masks are cleaned by spraying them with acetone, then methanol, and then thoroughly rinsing them with DI water. The DI rinse is needed to avoid residue. After the final DI rinse, the mask is dried with N2.

Solar cell mask sets:

SET1:
Designer: Essential Research (Navid Fatemi)
Solar cell size (metal coverage): 1.0 cm^2 (4%), 0.36 cm^2 (8%)
Diode sizes: ~1 mm^2 (diodes only at edges)
TLM: no

SET 2:
Designer: John Boeckl and John Carlin
Program: power point slide (Data/PV/maks/JB_0.6and0.4/cell.ppt)
Solar cell size (metal coverage): 0.36 cm^2 (8%), 0.16 cm^2 (10%)
Diode sizes: 0.79 mm^2, 0.441 mm^2, 0.196 mm^2, 0.049 mm^2
TLM: yes

SET 3:
Designer: John Carlin
Program: Autocad (Data/PV/maks/JC_0.2_solar_mask/ final_mask_2_2sq.dwg)
Solar cell size (metal coverage): 0.044 cm^2 (10% and 16%)
Diode sizes: 1 mm^2, 0.5625 mm^2, 0.25 mm^2
TLM: yes

SET 4:
Designer: Aurangzeb Khan
Program: Autocad (Data/PV/maks/Khan_0.5_1_2/ khan-final-8-combine-backup.dwg)
Solar cell size: 4 cm^2, 1 cm^2, 0.25 cm^2
Diode sizes: 1 mm^2, 0.3025 mm^2
TLM: no

D.1.6 Anti-reflection coating

Do not expose the ARC to water or high humidity since it will cause the ARC to deteriorate!

The thermal evaporator used for anti-reflection coatings (ARCs) is currently operated by Dr. Mark A. Smith at NASA Glenn Research Center. The ARC calibration will usually be completely by M. A. Smith. It is important that it is completed prior to ARC depositions on important devices, to identify the tooling factors that need to be used, to ensure the boats are pointed in the proper direction, and to identify the sweet spot for evaporation. This sweet spot is typically less than < 2-2.5 inches in diameter. Past problems with ARC's "lifting off" in an acetone dip were attributed to excess oil in the bell jar, which was then incorporated into the film. In order to ensure a clean evaporation, it is helpful to wipe down the bell jar with acetone either before or after every run. Beakers for processing at NASA are in the characterization Lab. (Ask Dave M. Wilt if you need to locate beakers.) Chemicals are in the lithography lab under the fume hood. These chemicals are from OSU. The etch rates seem to be impacted by the DI water at NASA, the cap etch with NH_4OH/H_20_2 takes longer than when performed at OSU. If you have a piece of the sample to spare you can cap etch it and coat it with the ARC in order to measure the reflectivity.

Calibration Procedure:

MgF_2 Calibration:

1 Deposit a thick layer of MgF_2 (~ 3000A) on a patterned 3" wafer.
2 Lift-off ARC with Acetone.
3 Measure layer thickness with Dektak as a function of position.
4 Compare this thickness to that measured on the crystal monitor.

5 Use this ratio as a tooling factor to determine the crystal monitor reading for the desired ARC thickness.

ZnS Calibration:

1 Deposit a thin layer of MgF_2 (~ 100A) on a patterned 3" wafer.
   - Use the tooling factor just determined if possible, otherwise you can correct after the fact.
   - This layer is needed for "sticktion"
2 Deposit a thick layer of ZnS (~ 3000A).
3 Lift-off ARC with Acetone
4 Measure layer thickness with Dektak as a function of position
5 Subtract the expected thickness of initial MgF_2 layer.
6 Compare the ZnS thickness to that measured on the crystal monitor
7 Use this ratio as a tooling factor to determine the crystal monitor reading for the desired thickness

Confirm that the sweet spots for ZnS and MgF_2 overlap

ARC design:

ARC can be designed using a program called TFCALC. EMDL owns 1 copy of this and the parallel port key needs to be in place before the program is opened. This program has data files for most materials. The accuracy of these files is unknown and they are no longer available free of charge from www.sopra.com. You can use this data for both ARC layers and material layers, or you can use the ZnS and MgF_2 files measured by NASA using ellipsometry. You can also use the reflectivity measured on a wafer (ie. a solar cell with a cap etch) as input to TFCALC for optimization of ARC designs. A previous ARC design consisted of 75Å MgF_2/ 480Å ZnS / 990 Å MgF_2. This produced a reduction in collection at short wavelengths that appears to result partly from the ARC design. It seemed to be deficient for use with an InGaP window, but more ideal for an 87% AlGaAs window. After further modeling, is seems that 75Å MgF_2/ 480Å ZnS / 1030 Å MgF_2 is a better ARC design for an InGaP window.

D.2 Sequence for processing a InGaP/GaAs DJ cell

The processing sequence outlined pertains to the AZ-1529 photo resist. The same basic procedure can be implemented with other photo-resists by altering the spinning conditions, exposure times and sequences, baking times and sequences, and developing conditions.

Wafer Cleaning: A/M/DI

This is the basic cleaning procedure employed and will be referred to as A/M/DI. In some cases this is used with ultrasonic agitation.

1 Submerge wafer in acetone
2 Spray wafer with fresh acetone
3 Submerge wafer in methanol
4 Spray wafer with fresh methanol
5 Submerge wafer in DI
6 Spray wafer with fresh DI
7 Dry wafer with N2

Back Contact (BC) Metallization

1 Clean the sample with A/M/DI.
   - This will be the only time a solvent can be used on the sample prior to metal deposition.
2 Spin + PR on front of the wafer.
   - This protects the front of the wafer when mounted face-down.
   - Do not spray acetone on the wafer to clean off PR while the wafer is spinning. It deposits residue on the back of the wafer; therefore, remove the wafer from the spinner and repeat step 1.
3 Soft bake PR at 90-100 ^{o}C for 15-20 min.
   - Make sure PR is hardened.
4 Etch the back of the wafer.
   - In some cases an oxide etch is performed in other cases the substrate material is etched.
   - Be careful when rinsing the back of the wafer; if the wafer is set on a wet text wipe this may cause the BC to peel or discolor.
   - Be careful while etching, if there are pinholes or cracks in the PR it may etch device layers.
5 Load sample in evaporator.

- It is usually best to use kapton tape to avoid sliding the wafer on the surface of the plate or applying too much pressure.

6 Deposit the appropriate back contact.
7 Remove PR with acetone.
8 Clean sample with A/M/DI.
    - Any remaining PR will burn in the furnace during the contact anneal and cannot be removed afterward.
    - If the ultrasonic bath is used in this step and there was PR on the back of the wafer that was coated with metal, it may redeposit on the front so watch for any residue on the front of the wafer.
9 Perform contact anneal if only BC anneal is needed.

Front Contact (FC) - image reversal lithography

1 Inspect the mask to ensure it is clean before use.
2 Clean wafer with A/M/DI.
    - This may have been performed before the contact anneal.
3 Spin on –PR.
4 Soft bake PR at 96-97 ^{o}C for 15 minutes.
    - After removing wafers from the oven let them cool for 5 minutes.
5 Select orientation of sample and mask.
    - Masks sets are chrome; the reddish, discolored side should contact the wafer; the shiny side should be away from the wafer.
    - Use mask template to indicate wafer orientation for exposure.
    - For small wafers, consider the range of motion of the microscope.
    - Always orientate the solar cells with the substrate cleave planes. In case of accidental breakage you will maximize the number of cells retained.
6 Confirm aligner settings and operation.
    - Lower Z-position, move CCW from default setting ~1.15 to ~ 8.0.
    - Check the exposure to make sure the bulb and timer are operational.
        - Sensor selected: 405 nm, CI2
    - Intensity: 22.6 mW/cm^2
7 Adjust Z-position for contact.
    - Record final Z-position used for each wafer.
    - Contact is critical; if the wafer is too far away from the mask the PR is over exposed and a thin residue of PR remains, which is not noticeable by microscope until areas do not etch later in processing.
    - Use of an asher, PR stripper, or O2 plasma might be employed to remove this residue.
    - Be careful not to crack cleaved samples or SiGe samples when contacting.
8 Expose with Front Contact mask. (~10s)
9 Soft bake at 96-97 ^{o}C for 40 minutes.
    - After removing from oven let wafers cool for 5 minutes.
    - Mix developer during bake. (4 : 1, DI : AZ-351)

10 Flood exposure (no mask). (~10s)
11 Develop. (~ 30s / 5s)
    - Use a 2 beaker developing method. Fully develop the pattern in Beaker 1 and then give and extra 5 s in Beaker 2 to confirm developing.
    - Rinse wafer thoroughly (~ 1 min in flowing DI).
    - Record developing time.
    - Developing time may be a function of when the wafer was exposed and the temperature. We suggest developing immediately after exposure and bake for consistent developing times. Age of PR and developing will impact developing times
12 Examine wafer with microscope to check developing.
    - Solar cell fingers are a good indicator of complete development.
    - Develop further if needed.
13 Large areas of wafer with no pattern maybe difficult to lift-off. It may be necessary to tape areas off or add extra PR to these areas before deposition.
14 Dektak PR and record thickness.
    - Do not deposit metal thicker than the PR thickness.
15 After use, clean the mask with A/M/DI.

Front contact (FC) - metallization and liftoff

1 GaAs Oxide Etch.
2 Metal deposition in e-beam evaporator.
3 Metal deposition in thermal evaporator. (Au ~13 pellets = ~2.5μm)
    - Au deposition in thermal evaporator.
4 Perform metal lift-off metal immediately after deposition.
    - Submerge sample in acetone.
    - Metal should begin to swell at the edges of the pattern after 10-30 s.
    - It is helpful to spray fingers off with acetone bottle. Aggressive spraying may be required to dislodge final fingers and TLM patterns.
    - Do not let acetone evaporate from wafer until lift-off is complete.
    - Use of the ultrasonic cleaner is not recommended since it tends to redeposit gold on the surface.
    - If liftoff is stubborn, try using scotch tape. Tape wafer to the table, apply a small portion (<1/4") of a piece of tape on wafer service, and gently peel. Try this before attempting more extreme methods.
5 Clean wafer A/M/DI.
6 Dektak metal and record thickness.
7 Contact anneal, if necessary.
    - Is especially important for both InGaP cells and DJ cells to perform any contact annealing prior to mesa etching. The InGaP sidewalls are exposed in the mesa etch, and if annealed, it can cause shunting in the InGaP junction.

Mesa - lithography

1 Inspect the mask to ensure it is clean before use.
2 Clean wafer with A/M/DI.
    - This may be performed after lift-off is complete.
3 Spin on +PR on front of the wafer.
4 Soft bake PR at 90-100^{o}C for 35 minutes.
    - After removing wafers from oven let samples cool for 5 minutes.
    - Mix developer during bake. (4 : 1, DI : AZ-351)
5 Orient the mask and sample in the same position used for FC lithography.
    - It helps to have made a map of the wafer and mask positions.
6 Confirm aligner settings and operation.
    - Lower Z-position, move CCW from default setting ~1.15 to ~ 8.0.
    - Check the exposure to make sure the bulb and timer are operational.
        - Sensor selected: 405 nm, CI2
        - Intensity: 22.6 mW/cm^2
7 Align wafer and adjust Z-position for contact.
    - Get a rough alignment by eye.
    - Then offset the mesa area and the cell fingers so that you can use this straight line to align wafer rotation.
    - Use alignment marks for fine alignment.
    - To check alignment contact must be made; however, after contact is made and then lowered, the wafer can move. If the alignment is "close enough" do not lower sample to realign, instead proceed with exposure.
    - Z-position should be similar to that used in Front Contact lithography; however, Z-position is sensitive to PR on the back of the wafer.
    - Record final Z-position.
8 Expose with Mesa mask. (~ 10s)
9 Develop. (~ 30s / 5s)
    - Use a 2 beaker developing method. Fully develop the pattern in Beaker 1 and then give and extra 5 s in Beaker 2 to confirm developing.
    - This developing step should be easier than FC.
    - Rinse wafer thoroughly (~ 1 min in flowing DI).
    - Record developing time.
10 Examine wafer with microscope to check developing.
    - Develop further if needed.
11 Paint the back of the wafer with PR to protect the back contact from the mesa etches. (Do not paint to think or make time will be too long.)
12 Soft bake PR at 90-100^{o}C for 10-15 minutes.
    - Make sure PR is hardened.
13 Record PR thickness using the Dektak.
    - This is your reference for measuring the etch depth (D1), so always measure at the same location in subsequent etching steps.
14 After use, clean the mask with A/M/DI.

Mesa - etching

Cap etch:

1 Etch the GaAs cap using the NH_4OH/H_20_2 etch.
   - For 1000Å cap (~ 10-20 s) or 3000Å cap (~ 45 s).
   - Watch for color change and don't over etch.

2 Dektak mesa edge (D2). (D2-D1 = cap layer thickness)

Top Cell:

1 Etch completely through the InGaP cell using HCl etch.
   - Do not mix HCl:DI until immediately before use since etching properties change rapidly.
   - If using straight HCl then mix time is not an issue.
   - The etch rate is not reproducible.
   - The best way to etch though InGaP is to watch the color change. The wafer will appear multi-colored due to thin film interference as the InGaP layer thins non-uniformly. When the wafer color becomes uniform it has reached the "etch-stop" at the GaAs cell.
   - Partway through etching, examine the edges of cell near an alignment mark to help identify any etching problems. If a circle is seen around the square alignment marks or alignment marks and the corner of the cell look "attached" use straight HCl to finish etching.
   - Although the etch time is not critical since the GaAs acts as an etch stop, over etching may cause detrimental undercut of InGaP layers especially at the corners of the cells.

2 Dektak mesa edge (D3). (D3-D2 = InGaP cell thickness)
   - It is good to measure this height in order to check the InGaP growth rate.

Bottom cell:

1 Etch the GaAs cell using the NH_4OH/H_20_2 etch.
   - Do not etch entirely through the GaAs cell to avoid isolating the GaAs/Ge interface. This may cause added series resistance.
   - Etch to the desired depth usually ~ 1μm into the base.

2 Dektak mesa edge (D4). (D4-D3 = GaAs etch depth)
   - It is important to verify cell isolation before removing Mesa PR, otherwise, the mesa lithography will need to be repeated.

Finish:

1 Remove PR in straight acetone.

2 Dektak mesa edge (D5). This is the mesa height.

3 If cap etch is performed at this time, etch the GaAs cap using NH_4OH/H_20_2 etch.
   - Paint the back of the wafer with PR to protect the back contact before the cap etch.
   - Dektak mesa edge after cap etch (D6). This is the final mesa height.

ARC - lithography

1 Inspect the mask to ensure it is clean before use.
2 Clean wafer with A/M/DI.
3 Spin on +PR on front of the wafer.
4 Soft bake PR at 90-100^{o}C for 35 minutes.
    - After removing from oven let samples cool for 5 minutes.
    - Mix developer during bake. (4 : 1, DI : AZ351)
5 Orient the mask and sample in the same position used for FC lithography.
6 Confirm aligner settings and operation.
    - Lower Z-position, move CCW from default setting ~1.15 to ~ 8.0.
    - Check the exposure to make sure the bulb and timer are operational.
        - Sensor selected: 405 nm, CI2
    - Intensity: 22.6 mW/cm^2
7 Align wafer and adjust Z-position for contact.
    - Get a rough alignment by eye.
    - Then offset the ARC pad and the cell fingers so that you can use this straight line to align wafer rotation.
    - Use alignment mark and procedures for fine alignment.
    - Z-position should be similar to that used in Front Contact lithography; however, Z-position is sensitive to PR on the back of the wafer.
    - Record final Z-position.
8 Expose with ARC mask. (~ 10s)
9 Develop. (~ 30 s / 5 s)
    - Use a 2 beaker developing method. Fully develop the pattern in Beaker 1 and then give and extra 5 s in Beaker 2 to confirm developing.
    - Rinse wafer thoroughly (~ 1 min in flowing DI).
    - Record developing time.
    - Use fresh solution for each wafer since the majority of the PR on each wafer is being removed.
10 Examine wafer with microscope to check developing.
    - Develop further if needed.
11 Paint the back of the wafer with PR to protect the back contact from the cap etch.
12 Soft bake PR at 90-100^{o}C for 15 minutes (or until hardened).
13 Do not clean in acetone or methanol since this will remove the pattern!

ARC

Confirm ARC design:

Confirm ARC calibration:

1 Calculate thickness for crystal monitor reading using the tooling factors.
2 Record both desired thickness and crystal monitor thickness in the logbook.

Contact layer removal:

1 Etch GaAs cap layer with the NH_4OH/H_20_2 etch.
   - Will not etch for an InGaAlP window of the InGaP cell
   - Cap layer must be completely removed to avoid excess absorption; however, do not over-etch to avoid undercutting fingers and etching completely through the GaAs cell and potentially into Ge.
2 Rinse well with DI, if not rinsed well residue can form and ARC will deteriorate.

ARC deposition:

1 Chill diffusion pump trap.
   - Chill for at least 1 hour prior to use.
2 Load ZnS and MgF_2 source material.
   - Remove any MgF_2 that looks black/charred.
3 Load samples near sweet spot.
   - Use kapton tape to mount samples.
4 Pump down procedure currently takes more than 1.5 hours.
5 Set the crystal monitor to 1 for MgF_2.
6 Increase current manually while watching the pressure.
   - Record information in their logbook.
   - Usually takes ~ 15-20 minutes to reach deposition current.
   - Once depositing the chamber pressure drops.
7 When desired deposition rate is achieved, rotate plate down and re-start crystal monitor.
8 At desired thickness reading, rotate plate up to terminate deposition and then decrease the current.
9 To change between MgF_2 and ZnS, need to switch power cables and change crystal monitor to 2 for ZnS.
10 Give ~ 5-10 min between layers for pressure to decrease and sample to cool.
11 Deposit all layers in this manner.
12 Let wafer/chamber cool for at least 30 min before unloading.
13 Submerge wafer in acetone for ARC lift-off from contact pads.
14 Make sure to clean in fresh Acetone and then methanol after lift-off.
15 Do not rinse with DI since this will deteriorate the ARC.

Solar Cell Fabrication is finished!

D.3 References

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APPENDIX E

SUBSTRATE DEFECTS AND THE IMPACT OF GROWTH PROCESS ON DEVICE PERFORMANCE

During the course this research, defects in the UHV SiGe substrate were identified and the impact of these defects on GaAs device performance characterized. Specifically, a defect coined the "bat defect" produced catastrophic failure in p-n diodes grown by solid source molecular beam epitaxy (SSMBE). Therefore, the ability to manufacture solar cells and the size of solar cells produced were influenced by the density of these defects. Fortunately, experimental studies found that bat defects in p+/n diodes grown by metal organic chemical vapor deposition (MOCVD) did not produce catastrophic device failure and thus large area solar cells were manufactured as presented in Chapter 11.

E.1 Substrate defects

There has been concern about whether large area cells on SiGe are possible, due to the potential for epilayer cracking posed by the large thermal expansion coefficient difference between GaAs and Si. However, a particular defect present in the SiGe substrates posed a much larger problem for the realization of large area solar cells by

SSMBE. Figure E.1 shows an image of a "bat defect" that are present in the SiGe substrate grown by ultra high vacuum CVD (UHV-CVD) at MIT. Depending on the growth conditions, the cleanliness of the reactor, growth temperature, and other unknown variables, these defects appear with varying density, anywhere from 25 to 200 cm^{-2}. However, the low pressure CVD (LP-CVD) SiGe substrates provided by Amberwave Systems Corporation had defect densities of less than 2 cm^2. Since LP-CVD SiGe substrates have been produced with similar TDDs and strain balance compared with UHV-CVD substrates [1, 2], this defect does not represent a fundamental limitation for the commercialization of SiGe technology for use in III-V/Si integration or SiGe microelectronics.

Figure E.1 shows a plan-view secondary electron microscopy (SEM) image of this defect; this defect was called the "bat defect" due to the ear-like protrusions that are similar to the helmet of "Batman", a popular super-hero from comics, television, and the movies. These defects are large in size typically ~ 20-30 μm in diameter and are deep, typically 2-3 μm. In some cases, smaller versions of these defects are present and may result from the defect being introduced at a different point in the growth process. On all substrates, the defects are orientated with the "ears" in the direction of the substrates 6° off-cut. This is described pictorially in Figure E.1. Also shown is a SEM image of a $Si_{0.7}Ge_{0.3}$ layer grown on a Si substrate which shows a similar type of defect; however, since the Si substrate had no off-cut the defect is symmetric, no ears. The crystallographic guide for (100) substrate is provides to demonstrate that the defect sidewalls in the symmetric direction are ~ 55°, which corresponds to the {111} type

planes, and in the asymmetric directions are ~49° and ~61°, which similarly correspond to the angle of the {111} planes with a correction for the 6° off-cut.

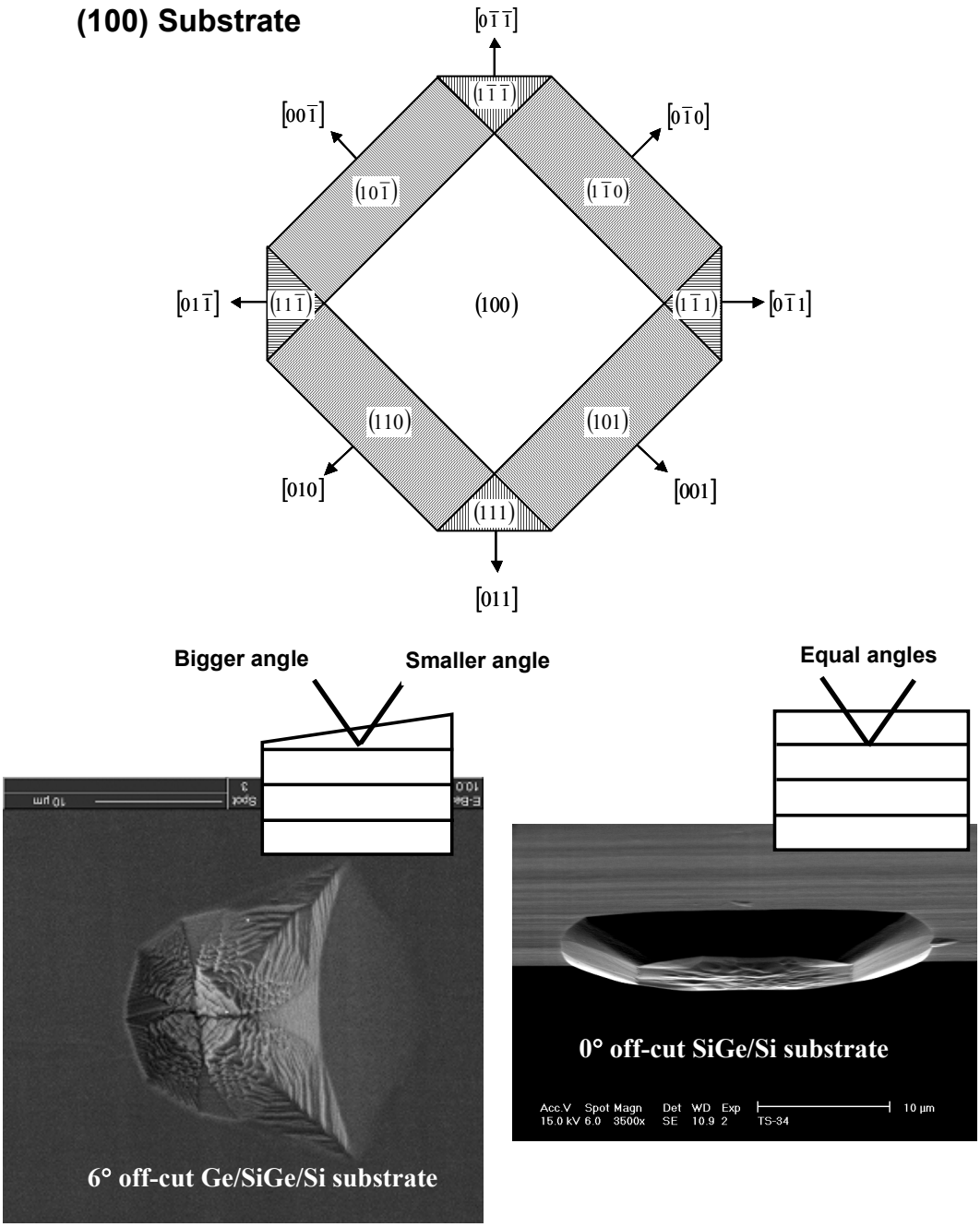

Figure E.1 SiGe substrate orientation and the orientation of the "bat defect" with respect to the substrate off-cut.

E.2 MOCVD versus SSMBE

Experimentally we determined that when growing GaAs by SSMBE the defect provided an effective shunt path for current flow and thus good diode and solar cell performance could not be achieved with the presence of just one such defect. These defects are catastrophic with or without metallization over the defect; its presence is enough to turn the device into an effective resistor. The low shunt resistance severely degrades the *FF* of a solar cell as well as the open-circuit voltage (V_{oc}), which makes device characterization virtually impossible. However, growth by MOCVD proved to provide suitable growth with in the defect that the diode and solar cell performances were not significantly hampered. An example of representative diodes grown on the same SiGe substrate by SSMBE and MOCVD are shown in Figure E.2. Clearly the device grown by SSMBE shows significant degradation with a bat defect present.

Examining these defects after GaAs over-growth we found that the characteristics of the GaAs growth with in the defect appear different. Figure E.3 compares the SEM images of a bat defect before GaAs growth and growth by MOCVD and SSMBE. In each case SSMBE was used for GaAs initiation (~ 1000Å) prior to the deposition of 3 μm of GaAs by the respective growth methods. The sample grown by MOCVD seems to have "accelerated" growth rates in particular crystallographic directions, as a result, the GaAs over-growth by MOCVD does not mimic the shape of the substrate defect as does GaAs over-growth by SSMBE. These defects were also examined by atomic force

microscopy and it was found that the depth of the defects with GaAs overgrowth were the same by both methods.

Recently advances in transmission electron microscopy (TEM) foil preparation, collaborator John Boeckl used a dual beam focused ion beam to mill TEM foils with in these bat defects. In this manner he was able to slice through the bat defect and image it in cross-section. Although this is a major body of his work [3], it is provided here as it pertains to the solar cell application. X- TEM images of the MOCVD and SSMBE GaAs on SiGe samples are shown in Figure E.4. These samples were grown on the same UHV-CVD SiGe substrate and had the same SSMBE GaAs initiation conditions. A cartoon of the defect is provided to help orient the defect and the cross-section selected. It is clear that the SSMBE samples as a higher defect density and thus worse material quality.

As a result, solar cells were grown by MOCVD when high bat defect densities were present. To achieve solar cells by SSMBE a small area solar cell mask (~ 0.04 cm^2) was used when bat defect densities of less than 25 cm^{-2}, in this case ~ 40-50% of the solar cells were "bat free". With bat defect density of ~ 200 cm^{-2}, all small area cells have bat defects and thus MOCVD must be used to produce working solar cell devices. As a result many of the devices and test structures presented in this thesis were grown by MOCVD; with the initial GaAs initiation layer grown by SSMBE since the MOCVD process for this has not yet been optimized. It should be noted that since LP-CVD SiGe substrates have much lower bat defect densities and in most cases no bat defects, solar cells grown by SSMBE have produced excellent results for cells on SiGe with areas up to 0.36 cm^2, the largest area tested to date.

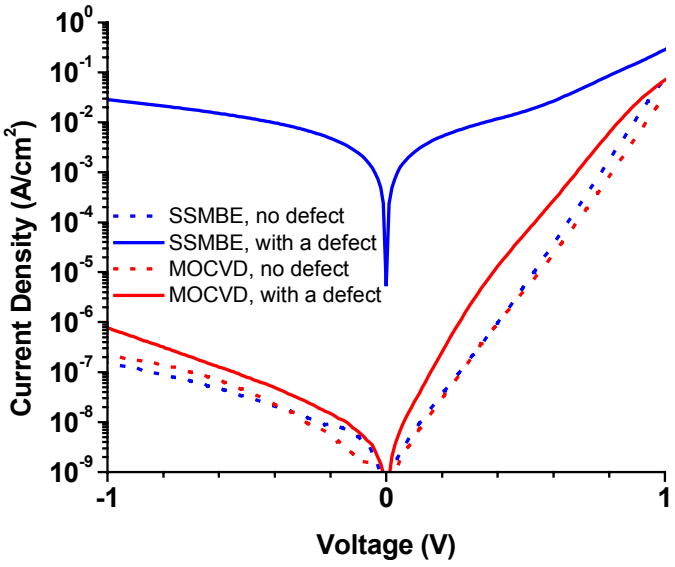

Figure E.2 Current density-voltage (J-V) characteristics from representative p+/n diodes on the MOCVD and SSMBE overgrowth samples showing the effect of the bat defect on diode performance.

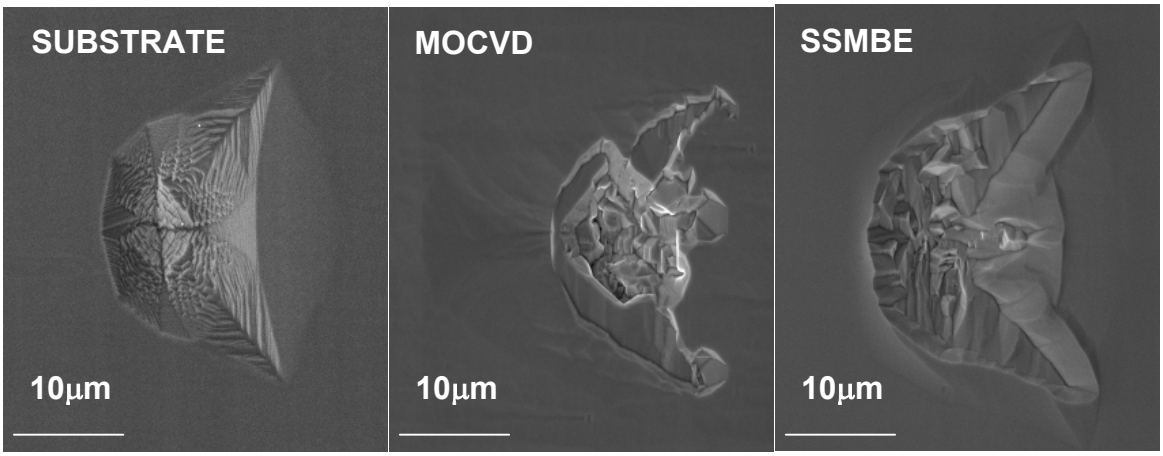

Figure E.3 SEM images of the bat defect. Although GaAs what deposited in the defect by both MOCVD and SSMBE the characteristic of the growth with in the defect is fundamentally different for these two growth methods.

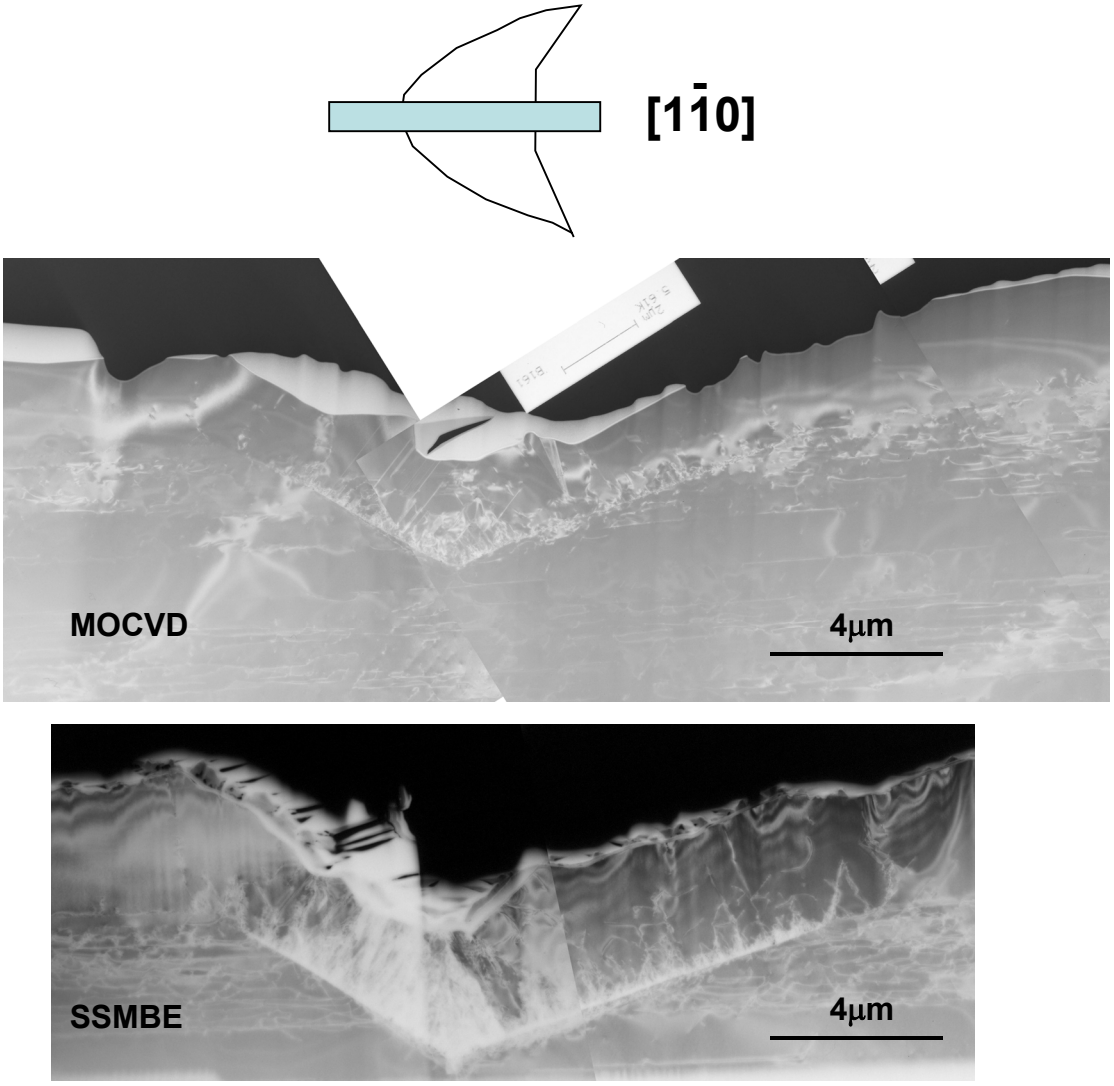

Figure E.4 Cross-sectional TEM image of a 3 μm layer of GaAs grown on a SiGe by MOCVD and SSMBE. This X-TEM shows higher defect densities on the steep angle of the defect for the sample grown by SSMBE.

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