CIRCUIT DESIGN FOR LOW VOLTAGE WIRELESS RECEIVER WITH IMPROVED IMAGE REJECTION

DISSERTATION

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By

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ABSTRACT

In a typical wireless receiver incoming RF (Radio Frequency) signal is down-converted to a lower IF (Intermediate Frequency) signal to relax the signal processing requirements of subsequent stages. A down-conversion mixer is used for translating desired signal to a signal with lower frequency. Mixer has two input-one comes from local oscillator, with a signal frequency of ω_{LO} and other from incoming RF signal with frequency $\omega_{RF.}$ After mixing with analog mixer the desired RF signal is down-converted to a lower IF signal such that $\omega_{IF} = \omega_{RF} - \omega_{LO}$. But due to the properties of sinusoidal multiplication with this analog mixer, signal band that is located symmetrically below ω_{LO} , such that $\omega_{IM} = \omega_{LO} - \omega_{IF,}$ also downconverted to IF frequency. Here ω_{IM} is the location of another signal. Hence, besides desired RF signal, another undesired signal located at ω_{IM} also translated to ω_{IF}. This undesired signal is known as image interferer, must be rejected to prevent aliasing with desired signal. External high Q filters are required to remove the image. This off-chip filter continues to be a bottleneck for realizing complete receiver integration. Image-reject receiver such as Weaver and Hartley architecture does not use off-chip image reject filter. But they are sensitive to mismatches of the two quadrature signal path that limit the image rejection ratio (IRR). In this thesis issues with image problem has been observed. The effect of mismatch has been studied for Weaver and

Hartley image reject receiver by mismatch modeling. A simple but effective phase calibration technique without using any external calibrating tone has been developed to improve the IRR. It has been implemented for Weaver and Hartley image reject receiver. In both cases image rejection ratio (IRR) of more than 59dB can be achieved for phase mismatch of 2 degree and small gain mismatch. Hence integrated receiver with improved IRR can be implemented without off-chip image reject filter and can be realized for standard like GSM (Global Systems for Mobile Communication), WCDMA (wideband Code Division Multiple Access) where higher IRR are required. Also to achieve programmability and multi-standard capability, low voltage low power circuits are essential. Designing such circuits always has been a major challenge. After downconversion of RF signal, entire signal processing is done in baseband. Low voltage and low power baseband circuits are necessary to provide low cost integrated receiver with added portability. In this dissertation low voltage circuit design techniques have been discussed for some essential baseband blocks of receiver such as variable gain amplifier (VGA), buffer and filter. VGA is used for gain variation between different block of the baseband and thus reduce noise requirements of subsequent blocks. CMOS realization of low noise and high bandwidth VGAs are presented. The simulation for the VGA is performed in TSMC .18µ technology. VGA's can be designed for input referred noise as low as 6nv/√Hz at 100 KHz and 3-dB bandwidth of more than 500 MHz. Highly linear baseband filters are required for channel selection of receiver. In this dissertation a novel low voltage buffer with low power consumption and low input referred noise,has been used in Sallen-Key structure to realize channel select filter [3].

Dedicated to my parents, family and son

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PUBLICATIONS

Research Publication

1. Hassan. O. Elwan, M. I. Younus, H. A. Al-Zaher and Mohammed Ismail. "A buffer based baseband analog front end for CMOS Bluetooth receivers". IEEE Trans. On Circuits and Systems-II: Analog and Digital Signal Processing, 49(8):545-554, Aug. 2002.
2. Hassan. O. Elwan, M. I. Younus and Mohammed Ismail. "A buffer based CMOS baseband chain for bluetooth receivers". IEEE International Symposium on Circuits and Systems, pages 26-29, May. 2002.

3. A. Ravindran, A. Savla, M. I. Younus and Mohammed Ismail. “ 0.8 V CMOS filter based on a very low voltage operational transresistance amplifier”. IEEE Midwest Symposium on Circuits and Systems, pages 4-7, Aug. 2002.

FIELDS OF STUDY

Major Field: Electrical Engineering

Studies in:

Analog VLSI

Wireless Communication

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CHAPTER 1

INTRODUCTION

1.1 Motivation

During the past few years the wireless market has grown rapidly and it's area of application has increased as well, not just limited to cell phone. This highly competitive wireless market demands lost cost, low power [3,4] and small form factor devices. This requires monolithic integration of receiver with multistandard capability. Hence low voltage, low power circuits are essential to achieve programmability and short design cycle with low cost. One major problem most of today's receiver share is the image problem, which usually comes from the adjacent channel. In order to eliminate the image problem high Q off chip image reject filters are required. So, receiver integration can not be achieved. However there are some receiver topologies that eliminate the image problem without using image reject filter. But the problem is that their image rejection ratio (IRR) is limited by the mismatch of the components. It can be shown that for a small mismatch IRR can be badly affected. Hence a calibration circuit is required to achieve good IRR.

1.2 Research Goals and Objectives

The main objectives of the research discussed in this dissertation can be summarized as follows:

Study different receiver architectures and understand the trade-off involving receiver's performance figure of merit with respect to monolithic integration.

Investigate image rejection problem in receiver, understand the effect of mismatch on receiver's performance (IRR), find a way to improve the image rejection ratio in image reject receiver. Also realize the algorithms in CMOS circuit.

Explore low voltage, low power circuits for baseband, since it is one of the major requirements to achieve multistandard capability with low cost.

Develop baseband circuit element like filter, VGA [2] in order to achieve fully integrated receiver in low cost. Low power dissipation is also required for small form factor.

1.3 Organization

The whole dissertation can be divided in two parts. First part deals with integration of receiver by using image reject receiver topology. Calibration techniques are required to improve IRR, since these receivers are sensitive to mismatches. Second part describes the low voltage, low power baseband circuits such as VGA, Filter in order to provide a low cost solution for integrated receiver. Circuit design techniques for low noise and high

bandwidth VGA and low noise, highly linear filter have been discussed. In this section we present the organization and an overview of the thesis.

Chapter 2- The demand for higher bandwidth and high speed data communication continues to increasing for ever. Also, latest development in the technology and devices made it possible to come up with new standard each time. For example data rate in 4G is 100Mbps compared to 54Mbps in 3G system. So it is necessary to have a good knowledge of different wireless standard. In this chapter specifications for different standards have been summarized and the migration from 1G to 3G [4] is presented as well. This chapter also highlights some issues and challenges [1] with respect to full receiver integration. Different receiver architectures such as Heterodyne, zero-IF, low-IF, digital-IF, image reject receiver, software radio etc. along with their trade-off with respect to receiver's performance figure of merit has also been investigated.

Chapter 3-Standards like GSM, DCS 1800, WCDMA require low noise and high image rejection ratio. This is difficult to achieve without any extra circuit, since non-ideal factors affect the IRR. In this chapter the basis of image problem is studied. Also mismatch modeling is presented to show the signal corruption due to image. Different calibration systems have been described and their performances are compared. Finally an algorithm for a calibration system (for both image reject receivers) is proposed and implemented.

Chapter 4- Depending on the application and system requirement, different VGA's are available. System like GSM requires low noise and highly linear VGA. On the other hand in order to achieve programmability for multistandard system, high bandwidth VGA's are

needed. Two different types of VGA's are described in this chapter to realize low noise and high bandwidth application.

Chapter 5-Low voltage, low power is one of the major requirements to have multistandard capability. A novel low voltage class AB buffer is reviewed in detail. Highly linear filter has been developed using this novel buffer. Filter design technique and issues in selecting different filter topology has been investigated.

Chapter 6- All the results and there trade-off are tabulated here. Future research direction has been suggested in this section as well

CHAPTER 2

RECEIVER ARCHITECTURES

2.1 Introduction

The objective of any receiver system is usually to provide filtering, gain and frequency translation of the received signal spectrum before the desired signal information is recovered through some method of detection. The distribution of gain, filtering and the method as well as frequencies used for frequency translation all will have an impact on receiver's selectivity and sensitivity performance. The trade off between gain, noise figure and linearity makes it difficult to realize an integrated receiver system on a single chip. In this chapter several receiver topologies will be investigated and the trade off in each of those architectures will be observed. Selection of receiver depends on the application or required performance of a system.

2.2 Wireless Standards

In this section specifications and system requirements of different wireless standards will be described. In the first generation (1G) systems, a lot of analog standards were developed independently thus leading to highly incompatible mobile phones and very limited roaming capabilities. An example of this generation is the advanced mobile phone

services (AMPS), which was developed in North America and used analog modulation techniques. However, this standard had limited capacity.

The real expansion of the wireless industry depends on second-generation (2G) systems, which were developed to establish common standards in certain parts of the world. Examples of this generation are:

(1) GSM (Global system for mobile communication) was developed by the European countries as a lack of standardization and compatibility of the 1G mobile phones deployed in Europe.

(2) DECT (Digital European cordless phone) was originally adopted as a cordless phone framework in Europe, and was designed to allow connection to other systems such as GSM. Thus this system provides mobility to local area network users. This standard operates with time division duplexing (TDD) in the frequency band 1800 MHz to 1900 MHz. This system uses time division and frequency division multiple access techniques (TDMA/FDMA) to increase user capacity.

(3) NADC (North America digital cellular) was developed in North America as the first digital 2G cellular system. The standard name is IS-54. Other standards sharing the use of TDMA as in IS-54 to increase the capacity is IS-136.

(4) IS-95 (interim standard 95) was developed in North America. This standard uses code-division multiple access (CDMA) to achieve higher capacity and better overall performance.

(5) PDC (personal digital cellular) was developed in Japan. Table 2.1 [4] provides a comparison of some 2G systems

Property	IS-54/IS-136	GSM	IS-95
Region	North America	Europe	North America
Forward Band	869-894 MHz	935-960 MHz	869-894 MHz
Reverse Band	824-849 MHz	890-915 MHz	824-849 MHz
Bandwidth	50 MHz	50 MHz	50 MHz
Multiple Access	TDMA/FDMA	TDMA/FDMA	CDMA/FDMA
Channel Spacing	30 KHz	200 KHz	1250 KHz
No. of Channels	832 (3 users/ch.)	124 (8 users/ch.)	798 (20 users/ch.)
Frame Period	40 ms	4.6 ms	20 ms
Duplexing	FDD	FDD	FDD
Channel Bit Rate	48.6 Kbps	271 Kbps	1.2288 Mbps
Voice Bit Rate	8 Kbps	13 Kbps	1.2 – 9.6 Kbps
Modulation	OQPSK	GMSK	BPSK/QPSK
Mobile Avg. Pwr	0.6-3 W	0.25-2.5 W	0.2-2 W
Cell Radius	30 miles	1-5 miles	30 miles

Table 2.1: Comparison of some 2G digital cellular systems

It is clear that different 2G standards employ different multiple access techniques, different modulation and coding, and different channel bandwidth assignments. Also, 2G systems are developed to handle voice and low data rates; however, current and future applications require handling of image, multimedia applications, and higher data rates. From this discussion we can see that 2G mobile systems prevent global roaming and thus 3G wireless systems were developed.

3G is the new generation of wireless communication and its development is based on the initiative of ITU (International Telecommunication Union) called IMT-2000 (International Mobile Telecommunication 2000). Since most of the 3G systems are evolved from different incompatible 2G systems like CDMA (Code Division Multiple Access), GSM (Global System for Mobile Communication) and TDMA (Time Division Multiple Access), therefore the IMT-2000 standard will ensure the compatibility and interoperability of different systems in 3G. The goal of 3G wireless system is to integrate both in applications field and in physical chip fabrication. As for the application area, consumer electronics, computer, and communication markets are to be combined. As for the chip integration, the goal is to have a single chip transceiver with no (or minimum) off-chip components, and in the same time, achieve wider compatibility and higher data rate capability. Some Examples of this generation are:

(1) WCDMA (wideband code division multiple access) is the radio access technology selected by ETSI (European Telecommunications Standards Institute) in January 1998 for wideband radio access to support third generation multimedia services .

Optimized to allow very high speed multimedia services such as voice, Internet access and videoconferencing, this technology provides access speeds at up to 2 Mbit/s in the local area and 384Kbit/s wide area access with full mobility. These higher data rates require a wide radio frequency band, which is why WCDMA with 5MHz carrier has been selected compared with 200 KHz carrier for narrowband GSM.

(2) CDMA2000: South Korea's SK Telecom launched the world's first 3G system in October 2000. The system is based on CDMA2000 1X. It supports both voice and data capabilities within a standard 1.25 MHz CDMA channel. The system doubles the voice capacity of cdmaOne systems and also supports high-speed data services. Peak data rates of 153 Kbps are currently achievable with figures of 307 Kbps quoted for future. Other versions of CDMA2000 are CDMA2000 1XEV-DO and CDMA2000 1XEV-DV etc.

(3) TD-SCDMA (Time Division Synchronous CDMA): This 3G standard was developed by China in 2002. It uses the same bands for transmit and receive, allowing different time slots for base stations and mobiles to communicate. Unlike other 3G systems it uses only a time division duplex (TDD) system. 3rd generation is not the end point. Fourth generation communication systems are currently being developed and are pushing data rates further up to 100 Mbps. It has been proposed to use VSF-OFCDM (variable spreading factor orthogonal frequency and code division multiplexing). Table 2.2 shows a comparison of some 3rd generation wireless standards. A road of migration from 2G to 3G is shown in figure 2.1.

Internet technology is also moving very fast. Therefore, there is also a need to provide effective short range communication through the wireless network. Some of the standards developed for providing high speed networking services will be discussed below.

(1) Bluetooth technology was developed in 1998 by a consortium that included Ericsson, Nokia, IBM, Toshiba and Intel. Its aim was to replace the old cable technology and provide effective short range communication between various devices complexity ranging from cellular phone to lap top computer. It also provides low cost low power solution. Bluetooth uses unlicensed ISM band between 2.4-2.485 GHz, frequency hopping over 79 channels, 1600 hops/s and with a throughput of 723 Kbps. Depending on different classes it can be used starting from 1 meter to 100 meter. Power consumption also varies from 1 mW to 100 mW respectively.

(2) WLAN (wireless local area networks) developed in 1999 by IEEE referred to as IEEE 802.11x standard. The purpose was to provide highly scaleable and fast wireless networking solution that integrates with the existing setup of IEEE networks and also provides support for mobile users. Depending on applications different varities of WLAN are available such as:

    a. 802.11: This was original WLAN standard developed in March 1999. It provides radio communication at 1-2 Mbps over the 2.4 GHz ISM band.

    b. 802.11b: It was approved in September 1999. This standard enhanced the data rate up to 5.5/11 Mbps on 2.4 GHz Carrier Frequency. DSSS modulation technique is used.

c. 802.11a: This standard was also approved in September, 1999 providing data rate up to 54 Mbps. It uses OFDM modulation at a carrier frequency of 5 GHz.

d. 802.11g: Approved in 2002. Aims to bring 54 Mbps data rate to more widely used 2.4 GHz frequency. This standard uses OFDM for faster data-rate but also includes CCK as a compulsion to maintain backward compatibility with 802.11b radios.

Technology	**Channel Spacing**	**Access Method**	**Data rate**	**Since**
WCDMA (UMTS)	5 MHz	CDMA/ TDMA	3.84 Mbps to 2 Mbps	1998
CDMA2000	1.25 MHz	CDMA	3.84 Mbps to 2 Mbps	2000
TD-SCDMA	1.6 MHz	CDMA	3.84 Mbps to 2 Mbps	2002
4G Mobile	-	VSF-OFCDM	100Mbps	-

Table 2.2: Comparison of some 3G standards

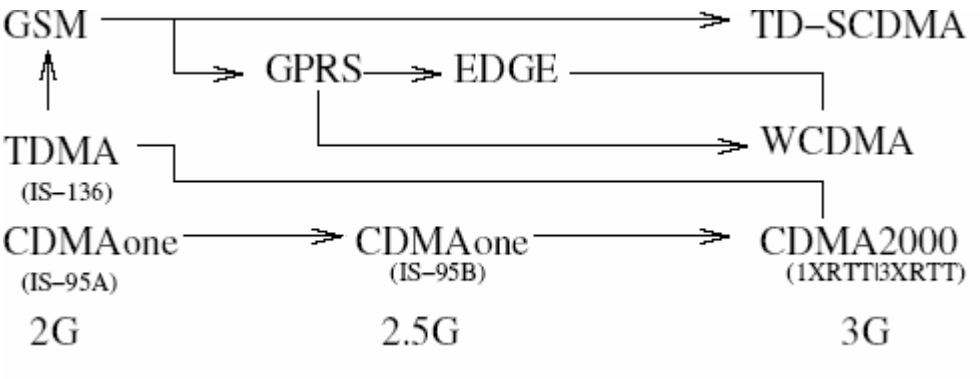

Figure 2.1: Road map to 3G

2.3 Receiver Topology

In a typical wireless receiver, received signal consists of modulated desired signal, along with other undesired (noise, interferers, image etc) signals. Usually these undesired signals are strong compare to desired signal. So, receiver front-end must provide certain functions such as: (1) Signal amplification to compensate for transmission losses, (2) Selectivity to separate the desired signal from other, (3) Tune ability to select desired signal. These qualities are also known as receiver figure of merit. In the following subsection different wireless different wireless architectures [38] and their trade off with receiver figure of merit will be discussed.

2.3.1 Heterodyne Receiver

A heterodyne receiver with single IF stage is presented in Figure 2.2. It can be divided into two parts. Signal is downconverted in first part and it consists of a duplexer, a low noise amplifier (LNA), and RF image-reject filter (RF bandpass filter) and an RF mixer with local oscillator. The second part consists of a channel-select filter (IF bandpass

filter), an auto gain control (AGC) unit and an I and Q demodulator. RF and IF bandpass filters are usually off-chip components. Figure 2.3 shows the downconversion of the input signal. First, the input signal is shifted to a lower frequency f_{IF} by the RF mixer, then passes through a channel filter to remove the adjacent interferers. Finally, the channel-selected signal is demodulated into I (in phase) and Q (quadrature) components in baseband.

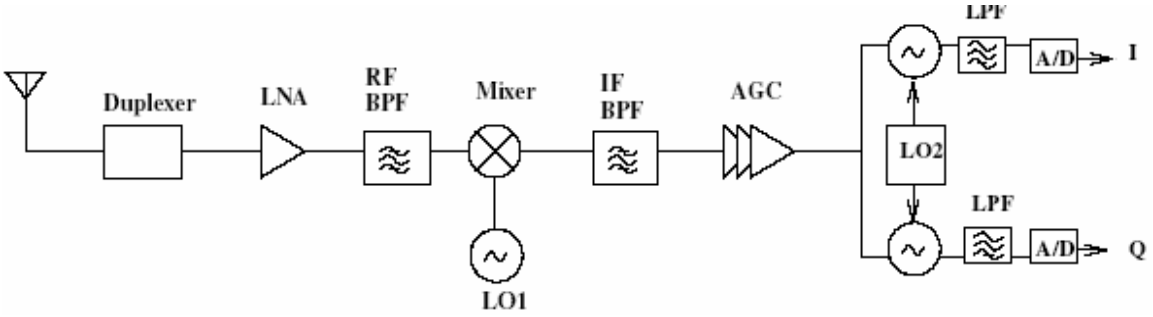

Figure 2.2: A typical heterodyne receiver architecture

In heterodyne receiver, image-reject filter is used to cancel the image signal. The cause of image can be explained as the following. Let $\cos(\omega_{RF}t)$ and $\cos(\omega_{LO}t)$ are RF and LO signal respectively. After mixing with LO signal, RF input is downconverted to an intermediate frequency $\omega_{IF,}$ such that, $\omega_{IF} = \omega_{RF} - \omega_{LO}$. This can be illustrated as the following:

$$\cos(\omega_{RF}t)\cos(\omega_{LO}t) = \frac{1}{2}[\cos(\omega_{RF} - \omega_{LO})t + \cos(\omega_{LO} + \omega_{RF})t]$$

$$= \frac{1}{2}[\cos(\omega_{IF}t) + \cos(2\omega_{LO} - \omega_{IF})t]$$

Now if an undesired signal $\cos(\omega_{IM}t)$ is located at $2\omega_{IF}$ distance from RF input, such that $\omega_{IM} = \omega_{RF} - 2\omega_{IF}$, then it will also produce a component at ω_{IF}, can be shown as:

$$\cos(\omega_{IM}t)\cos(\omega_{LO}t) = \frac{1}{2}[\cos(\omega_{RF} - 2\omega_{IF} - \omega_{LO})t + \cos(\omega_{LO} + \omega_{RF} - 2\omega_{IF})t]$$
$$= \frac{1}{2}[\cos(\omega_{IF}t) + \cos(2\omega_{LO} - \omega_{IF})t]$$

This undesired signal corrupts the downconverted desired signal and hence known as image signal (interferer). So, image band signal will appear at IF, if not filtered away before the downconversion. That is why heterodyne receiver use off-chip high Q, image reject (RF) filter to suppress image interferer.

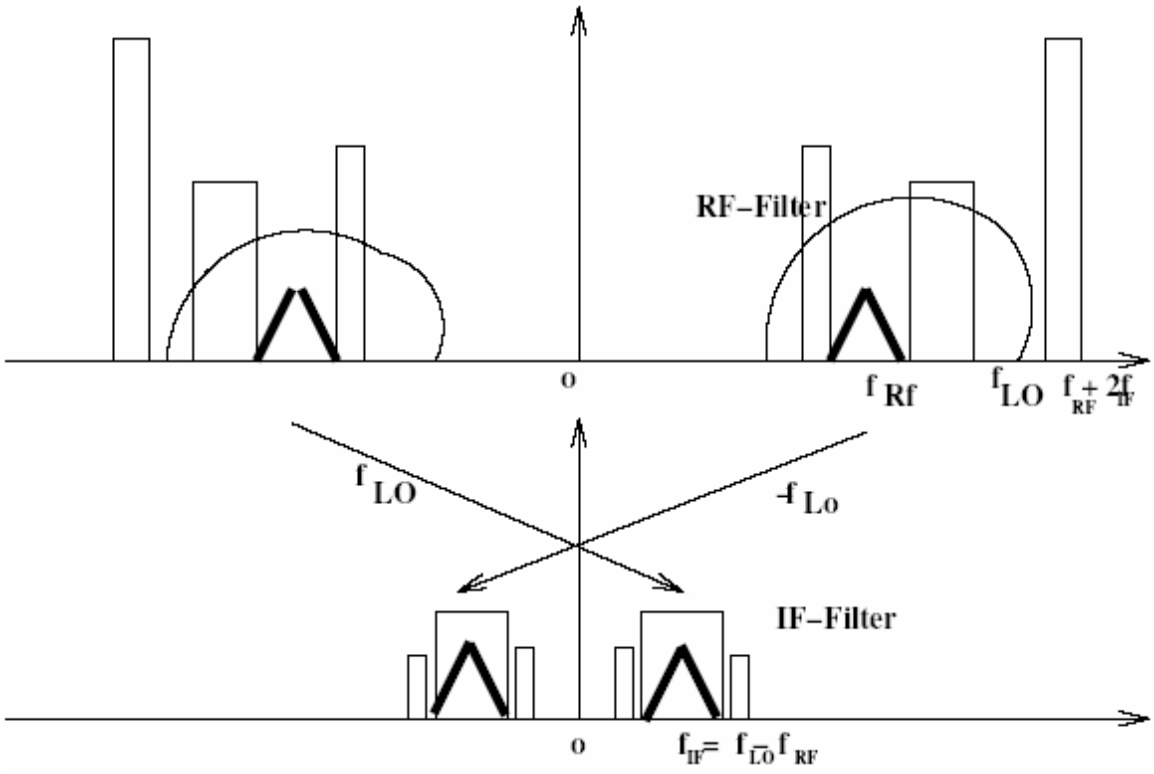

Figure 2.3: Downconversion of RF signal in heterodyne receiver

There exists a trade off in selecting IF frequency. For example, high enough IF should be used, since desired signal and undesired image bands are separated by $2f_{IF}$ and also image rejection is performed at RF, but a low IF is also required in order to make the implementation of IF channel selectivity filtering as feasible as possible. In the case where the input frequency is very high such as GSM, more IF stages are usually adopted to solve this issue with cost of more hardware, including off-chip image-reject filters [54, 55, 56, 57]. Because of high Q factor requirement for image-reject filter, off-chip, SAW filters are conventionally used. But it suffers from two major issues. Firstly, LNA must drive 50 Ω input impedance of the filter. This leads to more difficult trade off between gain, noise figure (NF), stability and power dissipation. Secondly it is a bottleneck in realizing on-chip receiver integration. A notch filter [9, 10] is an alternate solution to overcome these issues. Performance parameters of notch filters are listed in Table 2.3. From the table it can be found that notch filters have good performance in image rejection, but have disadvantages in NF, linearity and power consumption. Another drawback of these notch filters is that frequency tuning is required. The advantages of heterodyne receiver are summarized as follows: (1) selectivity is very good, (2) requirements on the channel selection filter is low, (3) DC offset of the first few stages is eliminated by the BPF and (4) I-Q mismatch occurs at low frequency and is easier to control and correct. The main drawback is that high Q image eject filters are required. This makes it very hard to achieve full integration. Other disadvantages of this receiver are: high power consumption, complicated structure, spurious response due to signal leakage.

	SAW filter [11]	Integrated LC notch filter [9]	Integrated active notch filter [10]
Passband	935-960 MHz	1900 MHz	947 MHz
NF/Insertion loss	3.1 dB	4.8 dB	7.2 dB
Image Rejection	50 dB @ 140 MHz	65 dB @ 600 MHz	60 dB @ 140 MHz
IIP3		$-19dB_m$	$-20dB_m$
Power consumption			27 mW

Table 2.3: Performance of different image-reject filters

2.3.2 Direct Conversion Receiver

Complete elimination of IF stage in heterodyne receiver, yields a simplified structure with reduced number of components. A quadrature (complex) downconversion mixer can be used to downconvert RF signal directly to baseband. So IF is reduced to zero and

hence this architecture is also known as zero-IF receiver. A block diagram of zero-IF receiver with quadrature output is shown in Figure 2.4. It consists of only an LNA, a I/Q mixer, two low pass filters for anti-aliasing and channel selection, two A/D converters and two AGC units. The simplicity of this receiver offers many advantages over the heterodyne receiver such as easy image rejection, elimination of RF image reject filter, and use of low pass filter and baseband amplifiers which make integration easier.

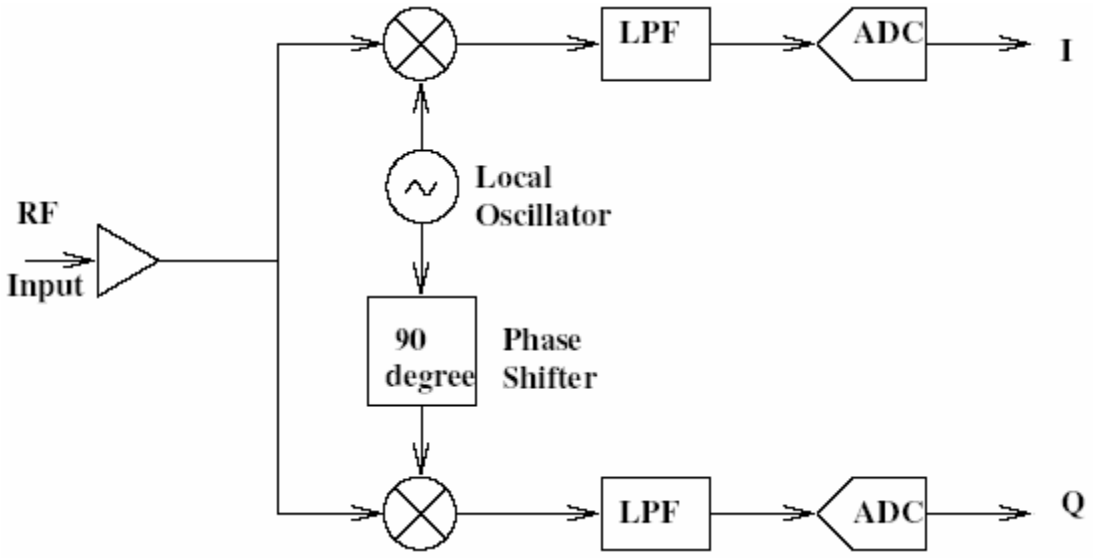

Figure 2.4: A zero-IF receiver with quadrature output

But it has also significant drawbacks. The most important one is the DC offset which often varies with time. Due to zero-IF, local oscillator frequency is on the same frequency as the desired channel. Then, if the LO signal leaks into the mixer input port, it self mixes down to baseband causing interfering signal components at zero frequency. These are called DC offsets and can be orders of magnitude larger than the desired channel signal.

Another source of DC offsets is the leakage of RF signal to LO port, resulting in self-mixing of possible interferes [5, 12] to baseband. This phenomenon is illustrated in figure 2.5. Sophisticated DC offset cancellation is therefore required [13, 14, 15]. Other drawbacks include I/Q mismatch, even-order distortion, flicker noise and LO leakage. The following demonstration describes the image problem. As the IF is now DC, the

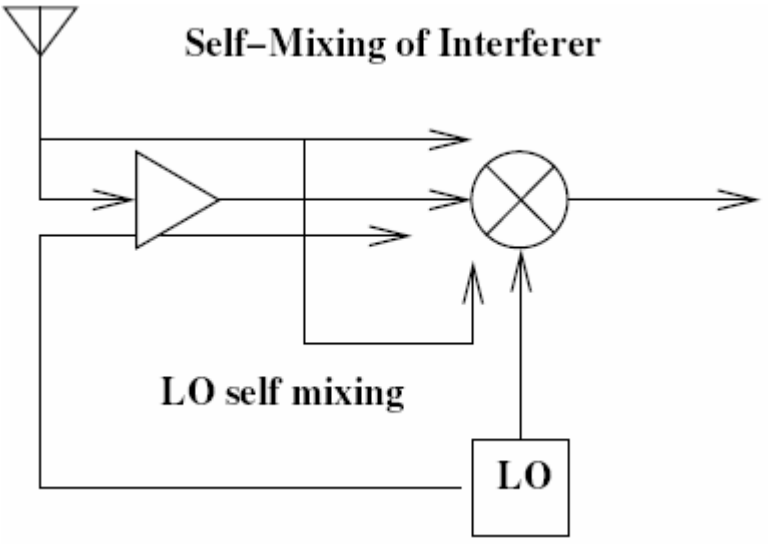

Figure 2.5: DC offset problem in direct conversion

image frequency is therefore $-f_{RF}$. In other words, the image is the mirrored version of the desired signal about DC. The image is therefore called as self image. As the complex (I/Q) mixer is used, the self image is rejected. But due to the I/Q imbalances, the rejection is not complete and depends on how good the matching is. The mismatches include the quadrature LO phase errors and the gain and phase imbalances between any circuit components of the two paths. Figure 2.6 illustrates the self-image problem in the

frequency domain. To gain more insight of the self image problem, suppose the received signal $x_{in} = a\cos\omega_c t + b\sin\omega_c t$, where a and b are either +1 or –1. Assume that the I and Q phases of the LO signal are $x_{LO,\,I}(t) = 2\cos\omega_c t$, $x_{LO,\,Q}(t) = 2(1+\alpha)\sin(\omega_c t+\varepsilon)$, where the factor two is included to simplify the results and α and ε represent gain and phase error respectively. Multiplying $x_{in}(t)$ by the two LO phases and lowpass filtering the result, we obtain the following baseband signals:

$$x_{BB,I} = \alpha \tag{2.1}$$

$$x_{BB,Q} = (1+\alpha)b\cos\varepsilon - (1+\alpha)a\sin\varepsilon \tag{2.2}$$

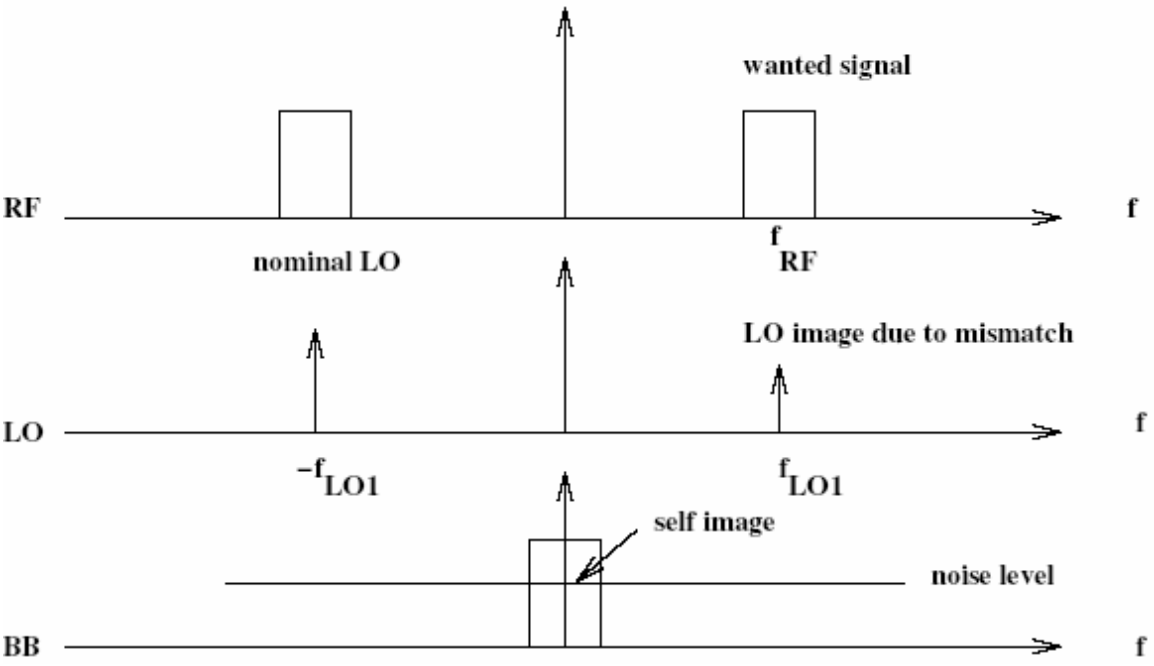

Figure 2.6: Self image problem in a zero-IF receiver

Therefore, the gain and phase error corrupt the downconverted signal constellation, thereby raising the bit error rate. Figure 2.7 (a) and (b) shows the resulting signal constellation with finite α or ε. This effect can be better seen by examining the downconverted signal in the time domain. Gain error simply appear as a non-unity scale factor in the amplitude. Phase imbalance, on the other hand, corrupts one channel with a fraction of the data pulses in the other channel, in essence degrading the signal-to-noise ratio (SNR) if the I and Q data streams are uncorrelated. The problem of self image is not serious in a single channel receiver with digital modulations which require typically only about 10dB of SNR. However, it becomes very troublesome in a wideband receiver where the channel selection is carried out in digital domain, for example in a multi-band receiver [46].

2.3.3 Low-IF Receiver

If IF is translated to a low, non-zero value, then most of the problems that are present in zero-If receiver such as, dc offsets, 1/f (flicker) noise etc., can be solved. This kind of receiver where IF is low but not exactly equals to zero, is known as low-IF receiver. Strictly speaking any other types of receivers can be categorized to this class as well if their IF is low. Due to low IF, normal monolithic filtering techniques such as g_m –C or active RC continuous time filters or SC filters can be used for channel selection, which makes the integration easier. A complex IF [16] stage is required for image rejection. LO phase error and I/Q mismatch will limit the image rejection performance of the receiver. Two kind of low-IF receiver will be discussed in the next subsection.

2.3.3.1 Double Quadrature Downconverter

Double quadrature downconverter was proposed in [17] in order to improve the image rejection in the complex RF-to-IF mixer. Figure 2.8 shows a block

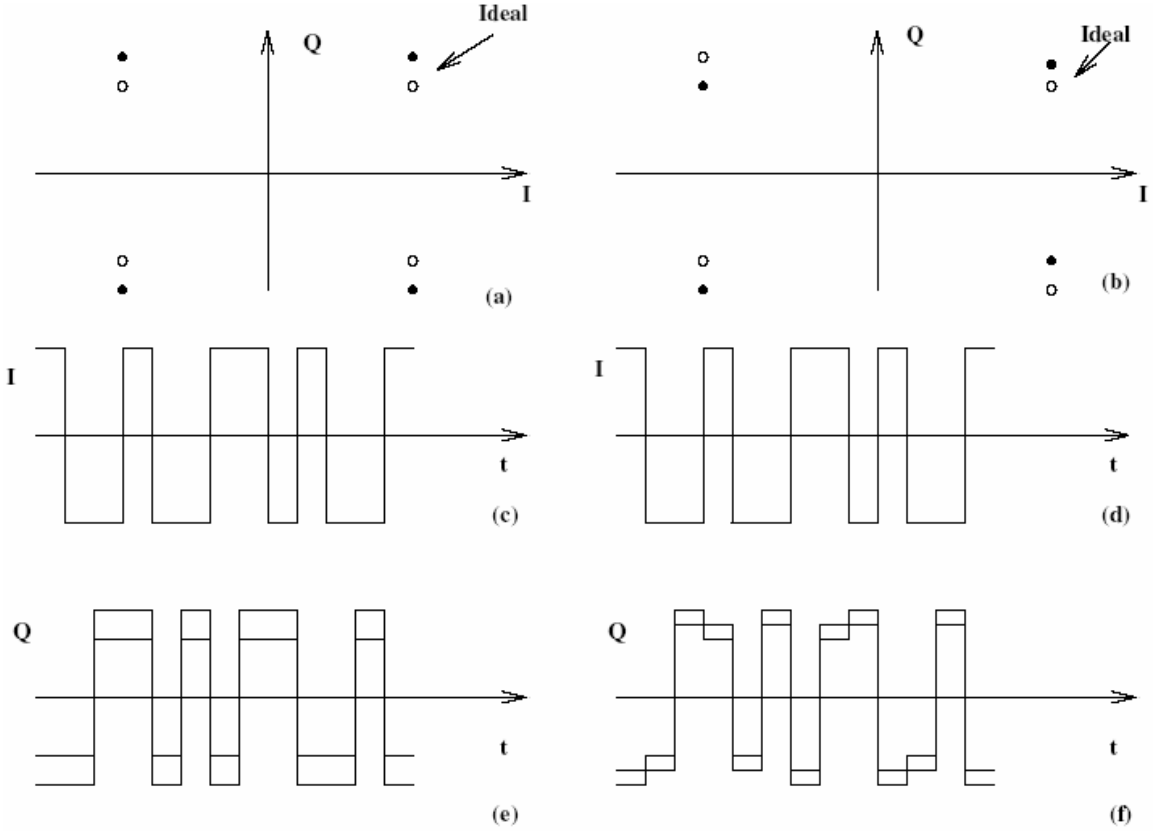

Figure 2.7: Self image effect. Constellation (a) with gain error; (b) with phase error. Time domain waveforms (c & e) with gain error, (d & f) with phase error

diagram of the double quadrature downconverter. It employs two quadrature generators (90 degree phase shifter), one in the LO path and another in the RF signal path, and two pairs of quadrature RF mixers that constitute an equivalent complex mixture. The quadrature generator in the RF path is a massive asymmetric polyphase filter which exhibits very high phase accuracy in a broad bandwidth.

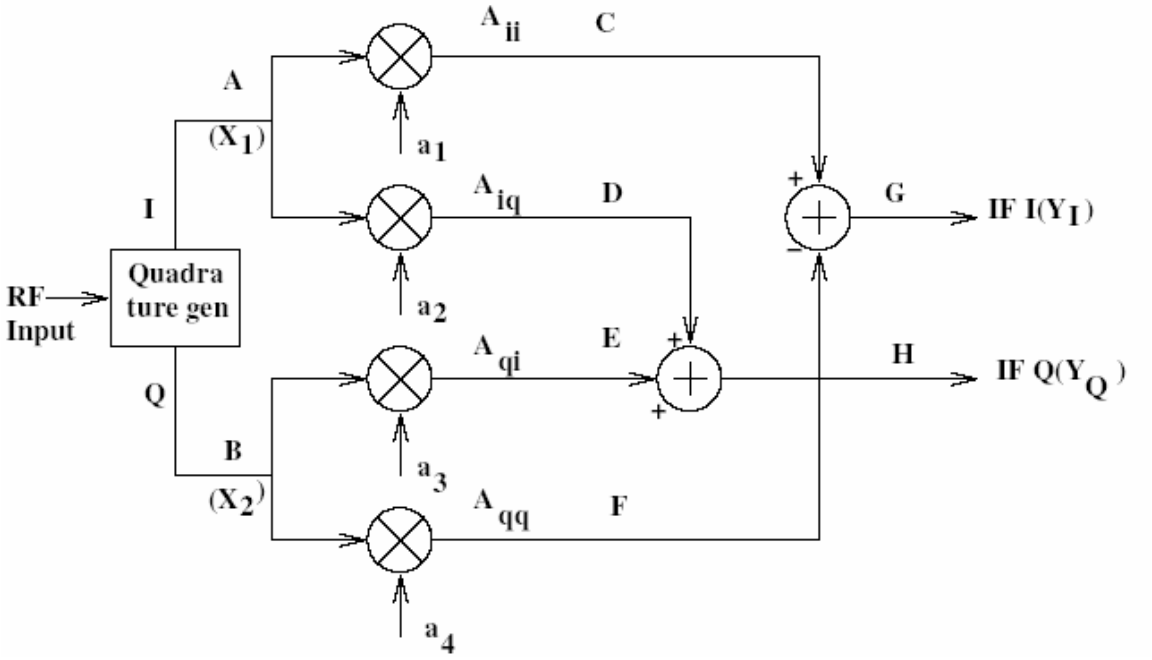

Figure 2.8: Low-IF receiver with double quadrature downconverter

Figure 2.9 shows the spectrum of the double quadrature downconversion. The idea behind this is that only the image interferer situated at positive frequency (if the complex LO is situated at the positive axis) can be superimposed on the wanted signal after complex downconversion. This means that it is not necessary to suppress the image

interferer at negative frequency axis, as is done with the classical high-Q RF filter. The superposition of only the negative frequency components does not require a high Q factor, even when the wanted and image frequency are situated very close to each other. The filtering can be done by a sequence asymmetric polyphase filter. The image is suppressed twice in a double quadrature downconverter, once by the polyphase filter and the other by the complex downconverter. So even with moderate phase accuracy of both LO and polyphase filter, very high image suppression can still be achieved. Obviously

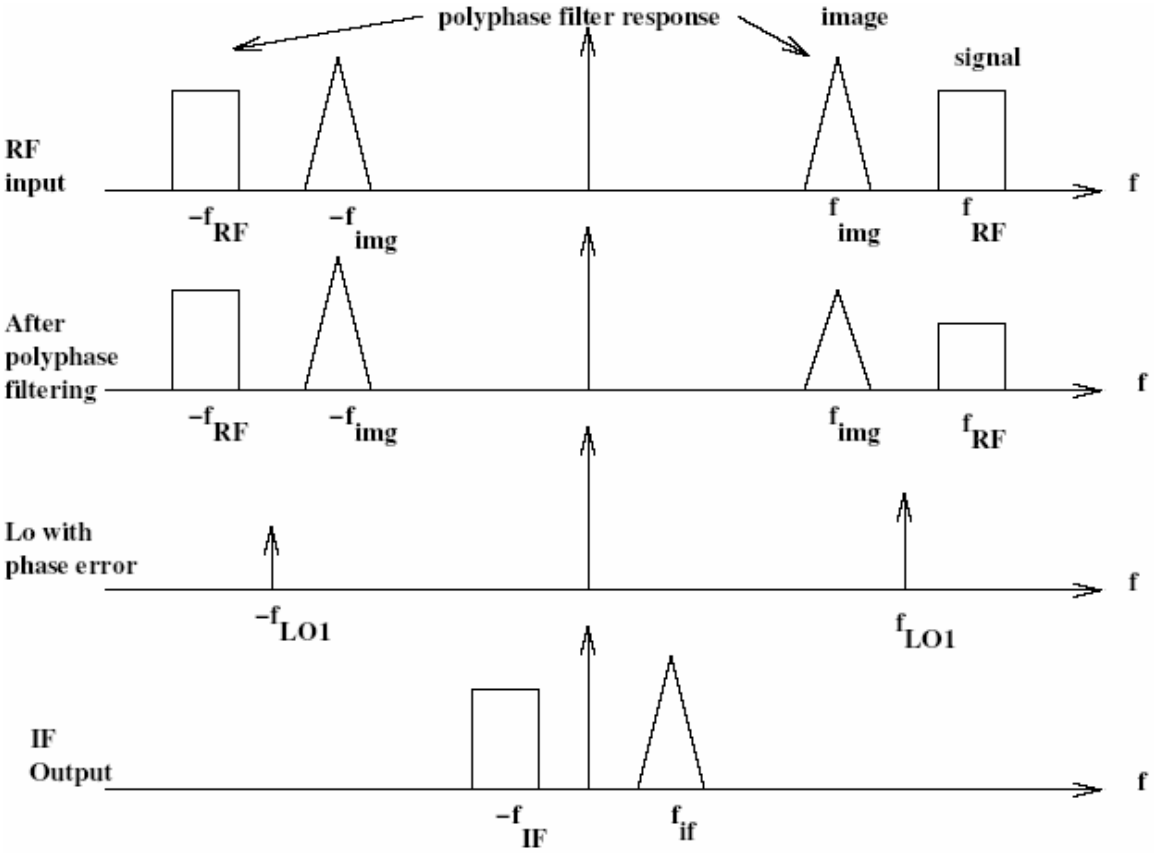

Figure 2.9: Spectrum of the double quadrature downconversion

the receiver has the drawback of using twice the number of RF mixers. The following analysis shows the effect of mismatch. In order to find the effect, let us denote the mixer gain in the four paths as $A_{ii,}$ $A_{iq,}$ A_{qi} and A_{qq} as shown in Fig 2.8. Output $Y(j\omega) = (Y_1(j\omega)+jY_Q(j\omega))$ can be written in frequency domain as:

$$\begin{aligned} Y(j\omega) &= \left[A_{ii}LO_I(j\omega)\otimes X_I(j\omega) - A_{qq}LO_Q(j\omega)X_Q(j\omega)\right] \\ &\quad + j\left[A_{iq}LO_Q(j\omega)\otimes X_I(j\omega) + A_{qi}LO_I(j\omega)\otimes X_Q(j\omega)\right] \\ &= LO_{cm}(j\omega)\otimes\left[X_I(j\omega) + jX_Q(j\omega)\right] + LO_{diff}(j\omega)\otimes\left[X_I(j\omega) - jX_Q(j\omega)\right] \end{aligned} \tag{2.4}$$

Where $\otimes$ denotes convolution, $LO_I(j\omega)$ and $X_Q(j\omega)$ are the Fourier transform of I and Q LO signals respectively, $X_I(j\omega)$ and $X_Q(j\omega)$ are the Fourier transforms of I and Q input signals respectively, and

$$\begin{aligned} LO_{cm}(j\omega) &= \frac{A_{ii}+A_{qi}+A_{iq}+A_{qq}}{4}\left[LO_I(j\omega) + jLO_Q(j\omega)\right] \\ &\quad + \frac{A_{ii}+A_{qi}-\left(A_{iq}+A_{qq}\right)}{4}\left[LO_I(j\omega) - jLO_Q(j\omega)\right] \end{aligned} \tag{2.5}$$

$$\begin{aligned} LO_{diff}(j\omega) &= \frac{A_{ii}-A_{qi}+A_{iq}-A_{qq}}{4}\left[LO_I(j\omega) + jLO_Q(j\omega)\right] \\ &\quad + \frac{A_{ii}-A_{qi}-\left(A_{iq}-A_{qq}\right)}{4}\left[LO_I(j\omega) - jLO_Q(j\omega)\right] \end{aligned} \tag{2.6}$$

Denoting $X(j\omega) = X_I(j\omega)+jX_Q(j\omega)$. As x_I and x_Q are real signals, $X^*(-j\omega)=X_I(j\omega)-jX_Q(j\omega)$, where * represents complex conjugate. Therefore (2.18) becomes:

$$Y(j\omega) = LO_{cm}(j\omega) \otimes X(j\omega) + LO_{diff}(j\omega) \otimes X^{*}(-j\omega) \tag{2.7}$$

The output consists of two parts: input X(jω) convolved with LO_{cm}(jω) and the image of the input X^{*}(-jω) convolved with LO_{diff}(jω). The first part is the desired one and shown in Fig 2.9. The second part is illustrated in Fig 2.10. It explains that the image interferer can be folded to the desired signal. The conversion gains of image and the desired signal are $(A_{ii}-A_{qi}-A_{iq}+A_{qq})/4$ and $(A_{ii}+A_{qi}+A_{iq}+A_{qq})/4$ respectively, The image rejection ratio is given by:

$$IRR = \frac{\left(A_{ii} + A_{iq} + A_{qi} + A_{qq}\right)^2}{\left(A_{ii} - A_{iq} - A_{qi} + A_{qq}\right)^2} \tag{2.8}$$

Let A_{ii}, A_{qi}, A_{iq}, A_{qq} = A±ΔA. The worst IRR is $(A/\Delta A)^2$. As an example for a gain mismatch of 1% among mixer, IRR is limited to 40 dB, which makes this receiver architecture difficult to achieve higher IRR.

Digital-IF Receiver

In this architecture, RF signal is downconverted to a low If signal (close to baseband), passes through a low pass filter and amplified before converted to digital domain by the ADC (analog-to-digital converter). A digital mixer is used for the final downconversion to baseband where digital channel filtering is used using DSP techniques. This topology has many advantages over other receivers, such as, elimination of off-chip IF SAW filter and external RF image reject filter. Using this topology, higher integration, scalability,

design flexibility can also be achieved in low cost CMOS process. DC offset problem and I/Q mismatch problem can also be avoided with this architecture.

The drawback of this architecture is high power consumption in data converter, high dynamic rang and high sampling frequency of the converter. Since sampling frequency is high in digital IF receiver, nyquist rate ADC's are difficult to achieve required dynamic range within reasonable power consumption. The dynamic range requirements may necessitate resolutions greater than 14 bits. Current application examples using this architecture are reported in [20-22].

2.3.4 Software Radio

In order to take advantage of DSP, wideband RF signal is downconverted closer to baseband as a whole and the entire service band is digitized in some receivers. The final channel selection filtering, downconversion and demodulation can be done with DSP. The ultimate aim of this architecture is to locate ADC just after LNA as shown in Figure 2.12. This concept is known as software radio [18]. This greatly increases receiver flexibility and multistandard capability.

The software radio will cover all frequency bands, regardless of wireless standards. The functions of modulation/demodulation, up/down conversion, channel selection, etc., will be all implemented by real time software. The output of the device can be voice, video, fax, data or any other forms of media. Therefore total flexibility will be provided. Also it can easily adapt to new wireless standards without any hardware change.

There is only one signal path and no IF stage. I/Q mismatch, LO phase errors and so on are all circumvented by using this topology. Much of the analog blocks can be replaced by using advanced signal processing, can be summarized as: (1) Efficient multirate signal

processing technique for digital channel selection filtering, (2) All digital synchronization technique can be implemented in DSP part without feedback loops to analog section, (3)

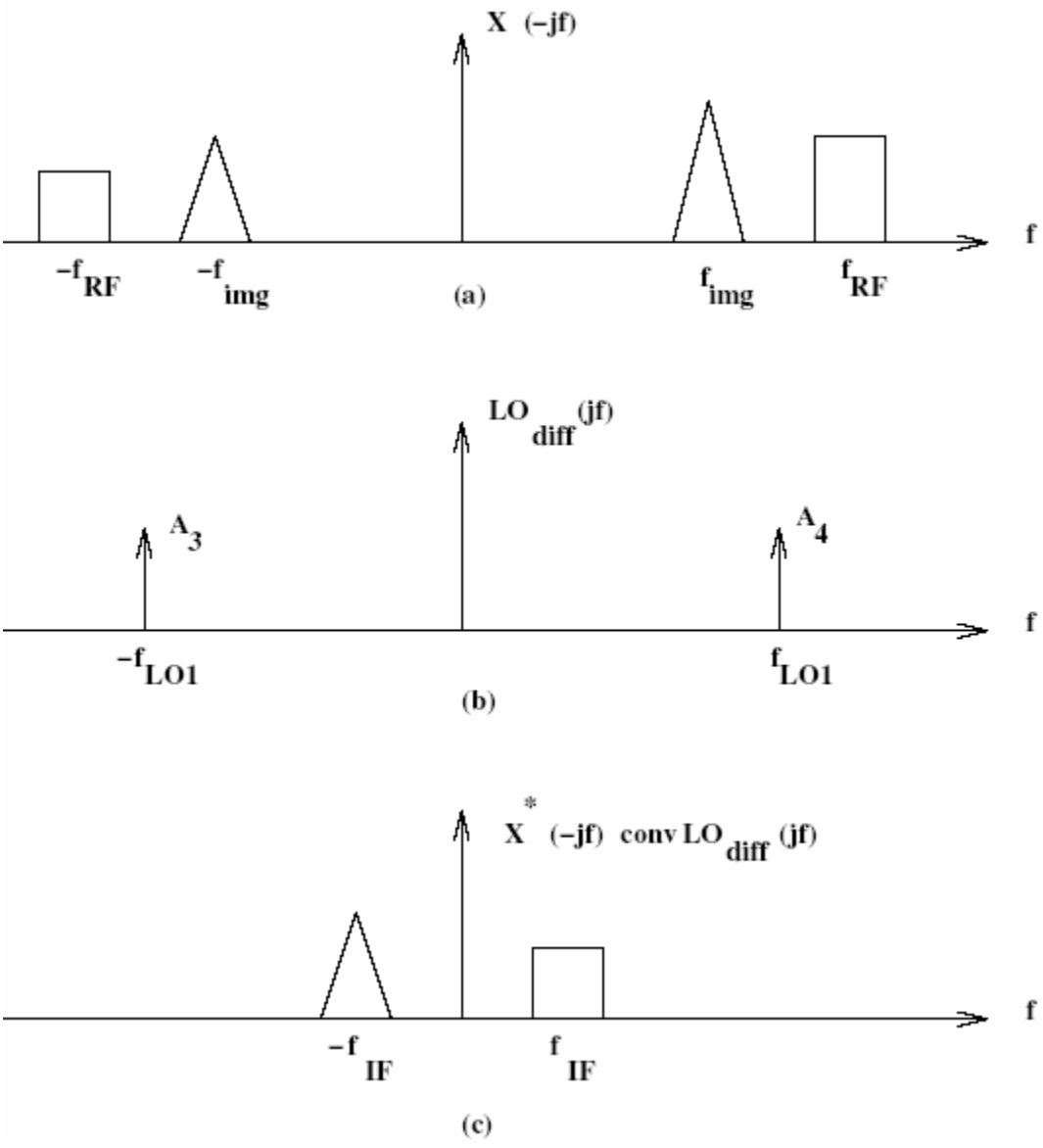

Figure 2.10: Image aliasing in a double quadrature downconverter

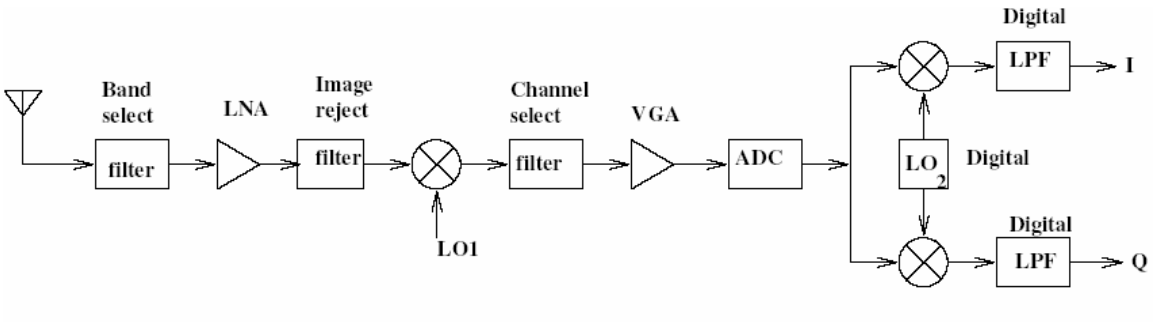

Figure 2.11: Digital-IF receiver

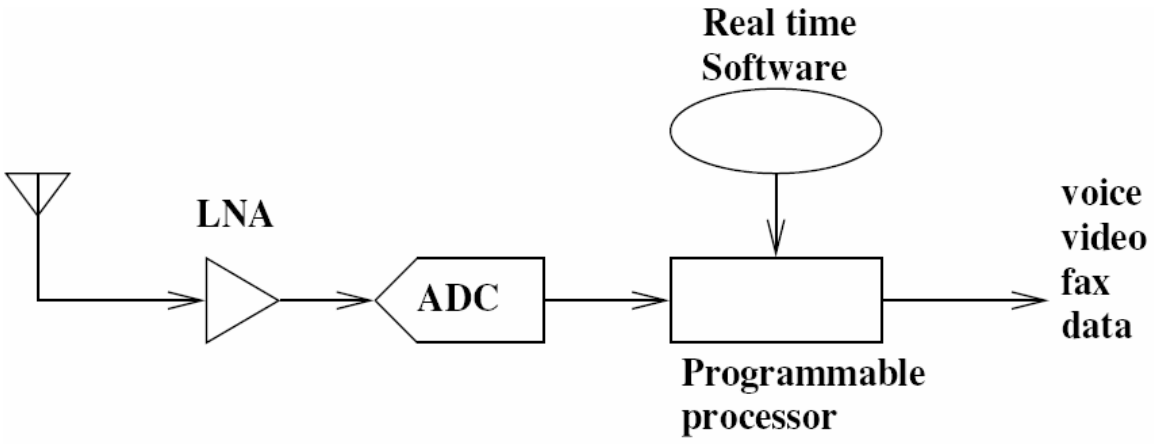

Figure 2.12: The concept of software radio

Some distortion effect due to the imperfections of the analog part can be compensated by advanced digital signal processing in the baseband etc,. So plenty of nice features are available with software radio, but in order to build a software radio system, extremely large sampling rate, bandwidth and dynamic range are required in the ADC [19]. These difficulties make it unrealizable with today's technologies.

2.3.5 Image-Reject Receivers

The basic objective of an image-reject receiver is to process and suppress the image tone without utilizing an explicit, external filter. Various image-reject receiver architectures and their strengths and limitations are described in this section.

The Hartley architecture is the most basic image-reject architecture and is shown in Figure 2.13. In this architecture, the incoming RF input is mixed with the quadrature outputs of the local oscillator, low pass filter and shift the results by 90^0 before adding them together. The quadrature outputs of the LO are presented as shown in Fig. 2.13 (a) and (b), whereas, the desired and image signal bands are shown at different points in the architecture in Fig. 2.13 c. The desired and image signals have different polarity before addition at the IF output, results in cancellation of the image, and leaves only the desired signal. The 90^0 phase-shift can be implemented as shown in Fig. 2.14 using RC-CR phase shift network. The principal drawback of Hartley architecture is its sensitivity to mismatches. The image rejection ratio (IRR) is limited because of the phase and gain mismatches. Sources of mismatch include I/Q generation errors and the inaccuracy of R and C parameters due to process and temperature variation, and these effects severely

limiting IRR of the receiver. To alleviate the mismatch problem with 90- degree phase shift network in Hartley architecture, another architecture known as weaver architecture has been introduced as shown in Figure 2.15.

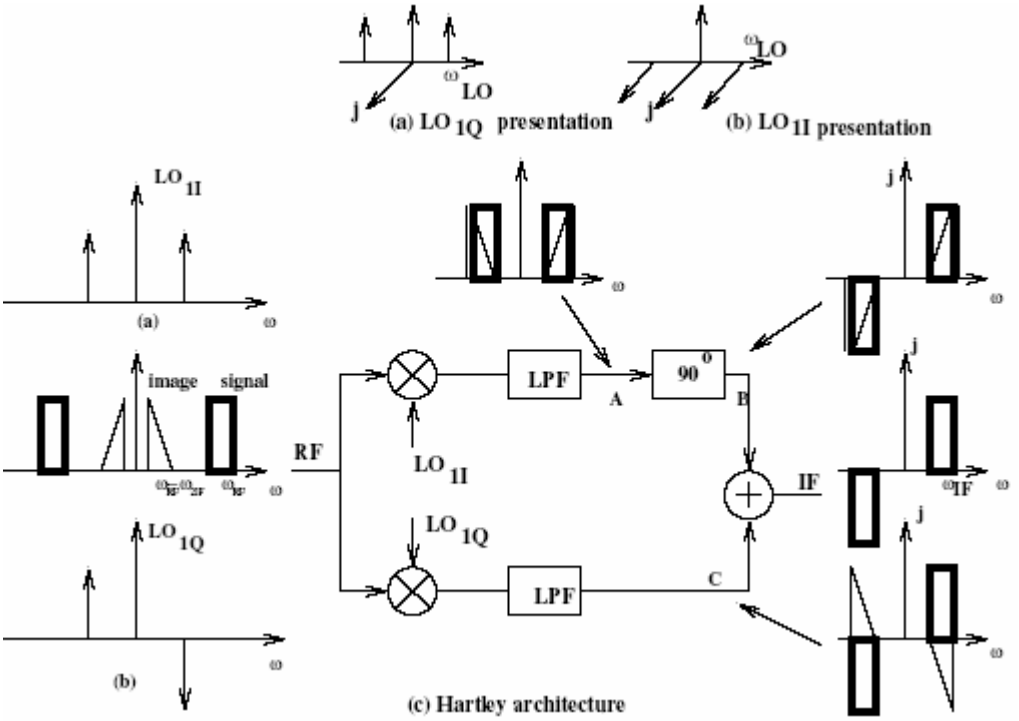

Figure 2.13: Hartley architecture with image rejection

In this architecture, the 90^0 phase shifter is replaced with a second quadrature mixer. By following the spectrum of the desired and image signals, it is clear that they have 180^0 phase difference before subtraction and so the output spectrum is free from the image signal component. An example of using this architecture in dual-band wireless applications is reported in [23].

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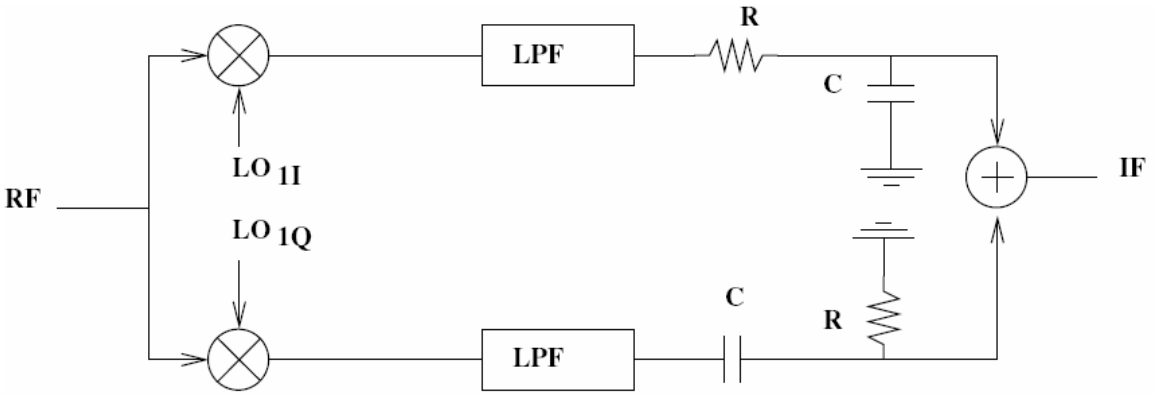

Figure 2.14: RC-CR phase shift network for Hartley receiver

The Weaver architecture is also sensitive to phase and gain mismatches between it's two quadrature paths, however it avoids the use of RC-CR phase shift network and therefore, it can achieve larger IRR. However, it introduces the problem of a secondary image, if the second mixer translate the spectrum to a non-zero frequency. This can be avoided either by down-converting the signal directly to base-band, or by using band-pass filters instead of the low-pass filters in the architecture [24]. Similar to Hartley architecture, the Weaver architecture is also sensitive to mismatches in phase and gain of the LO quadrature signals. Image reject architectures are suitable for high integration on-chip as no image filter is required (ideally). It is also suitable for multi-standard design as channel selection is done at IF or base-band by adequate filtering.

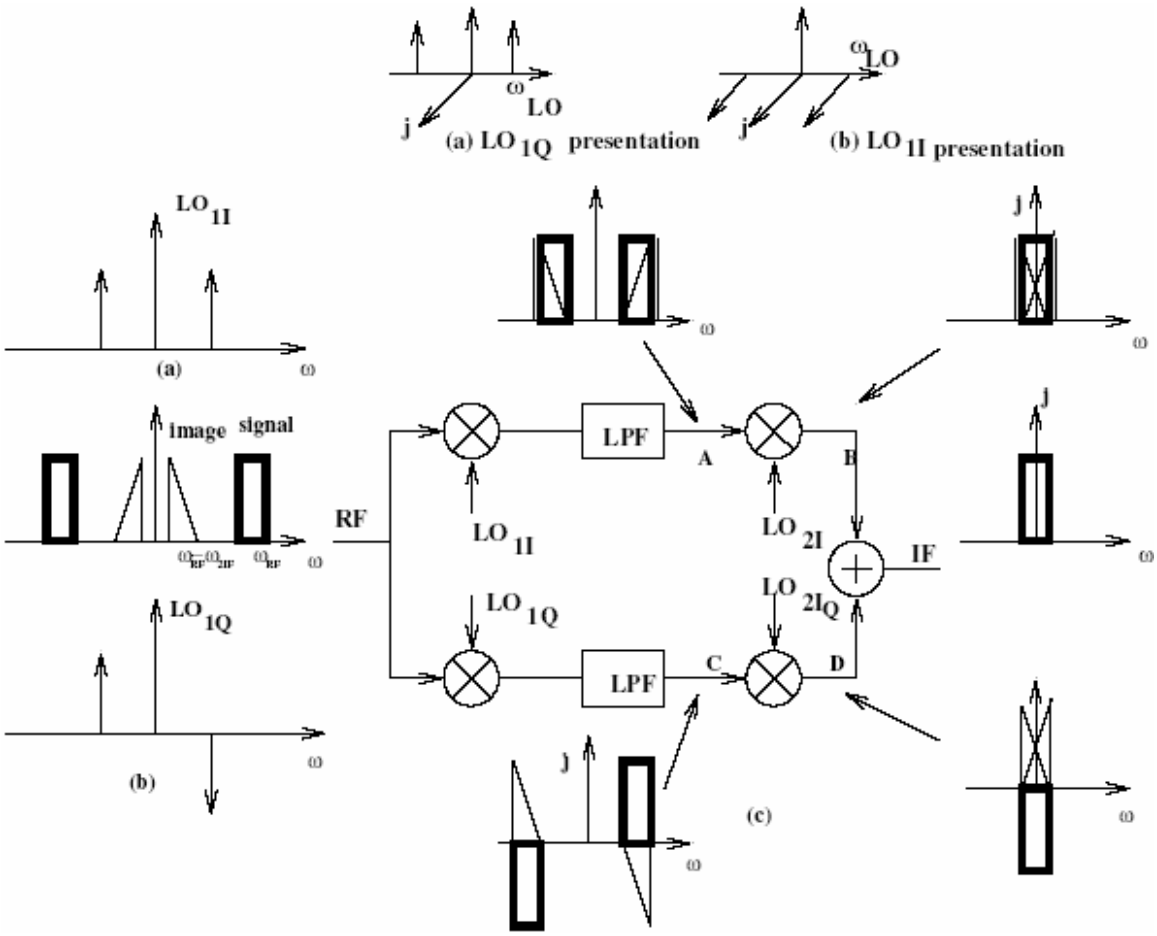

Figure 2.15: Weaver image reject receiver

CHAPTER 3

CALIBRATION TECHNIQUES FOR IMAGE-REJECT RECEIVERS

3.1 Introduction

Heterodyne receivers provide a robust solution for the processing of small RF signals in the presence of large interferers. Such architectures, however suffer from a trade-off between image rejection and channel selection. A higher intermediate frequency allows a more relaxed image-reject filtering but requires a more difficult channel-select filtering. Furthermore, the external image reject filter interposed between the low noise amplifier and the first mixer leads to a greater cost and greater power dissipation. Image-reject architectures offer a method of improving the above trade-off, but their performance is very sensitive to phase and gain mismatches. In this dissertationt some calibration techniques have been proposed to reduce the mismatches and improve the image rejection. Also some previous work on calibration technique has been reported and their pros and cons are discussed.

3.2 Mismatch Modeling for Weaver Architecture

Figure 3.1 presents a typical Weaver receiver [32] with mismatches in the LO's.

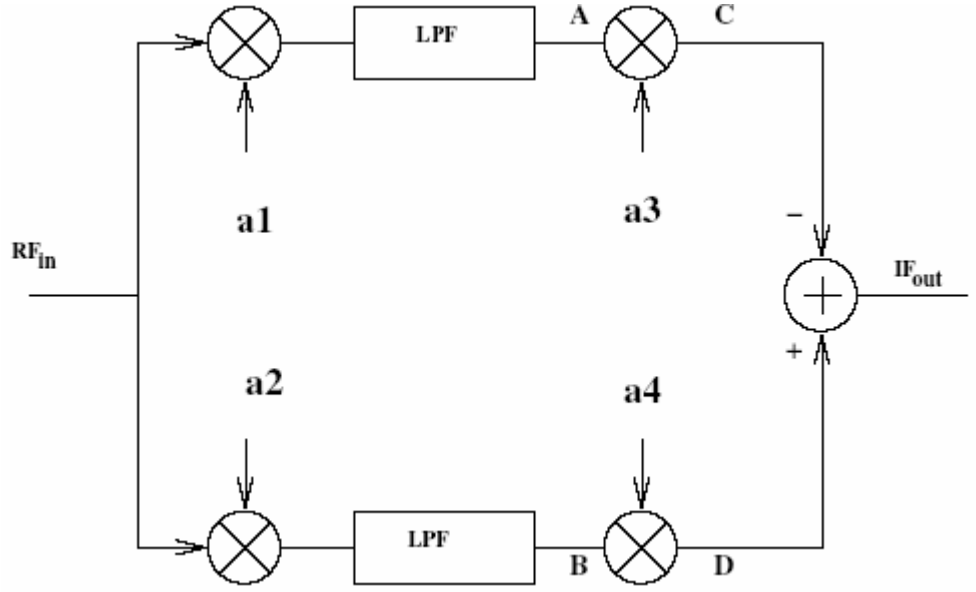

Figure 3.1: Weaver Image-reject receiver and mismatch modeling

Here a1, a2, a3, a4 represent the LO terms and mismatch components in the two quadrature path. In circuit level, fully differential blocks for each circuit element will be used. Define:

$$a_1 = \left(A_1 + \frac{\Delta A_1}{2} \right) \sin\left(\omega_1 t + \frac{\theta_1}{2} \right) \tag{3.1}$$

$$a_2 = \left(A_1 - \frac{\Delta A_1}{2} \right) \cos\left(\omega_1 t - \frac{\theta_1}{2} \right) \tag{3.2}$$

$$a_3 = \left(A_2 + \frac{\Delta A_2}{2} \right) \sin\left(\omega_2 t - \frac{\theta_2}{2} \right) \tag{3.3}$$

$$a_4 = \left(A_2 - \frac{\Delta A_2}{2} \right) \cos\left(\omega_2 t + \frac{\theta_2}{2} \right) \tag{3.4}$$

Here gain mismatches are distributed as ΔA_1 and ΔA_2. Phase mismatches are distributed as θ_1 and θ_2. We apply an image tone $\cos\omega_{IM}t$ at the input to see the effect of mismatch.

$$X_A(t) = \frac{1}{2}\left(A_1 + \frac{\Delta A_1}{2} \right)\left\{ \sin\left(\omega_1 t - \omega_{IM} t + \frac{\theta_1}{2} \right) \right\} \tag{3.5}$$

$$X_B(t) = \frac{1}{2}\left(A_1 - \frac{\Delta A_1}{2} \right)\left\{ \cos\left(\omega_1 t - \omega_{IM} t + \frac{\theta_1}{2} \right) \right\} \tag{3.6}$$

$$\begin{aligned} X_C(t) &= \frac{1}{2}\left(A_1 + \frac{\Delta A_1}{2} \right)\left(A_2 + \frac{\Delta A_2}{2} \right)\left\{ \sin\left(\omega_1 t - \omega_{IM} t + \frac{\theta_1}{2} \right) \sin\left(\omega_2 t - \frac{\theta_2}{2} \right) \right\} \\ &\cong \frac{1}{4}\left(A + \frac{\Delta A}{2} \right) \cos\left(\omega_{IF} t + \frac{\theta}{2} \right) \end{aligned} \tag{3.7}$$

$$\begin{aligned} X_D(t) &= \frac{1}{2}\left(A_1 - \frac{\Delta A_1}{2} \right)\left(A_2 - \frac{\Delta A_2}{2} \right)\left\{ \cos\left(\omega_1 t - \omega_{IM} t - \frac{\theta_1}{2} \right) \cos\left(\omega_2 t + \frac{\theta_2}{2} \right) \right\} \\ &\cong \frac{1}{4}\left(A - \frac{\Delta A}{2} \right) \cos\left(\omega_{IF} t - \frac{\theta}{2} \right) \end{aligned} \tag{3.8}$$

$$X_{out}(t)=\frac{1}{4}\left(A-\frac{\Delta A}{2}\right)\cos\left(\omega_{IF}t-\frac{\theta}{2}\right)-\frac{1}{4}\left(A+\frac{\Delta A}{2}\right)\cos\left(\omega_{IF}t+\frac{\theta}{2}\right) \tag{3.9}$$

Here,

$$\omega_{IM}=\omega_1-\omega_2\pm\omega_{IF}$$

$$A = A_1A_2$$

$$\theta=\theta_1+\theta_2$$

$$\Delta A=\Delta A_1A_2+\Delta A_2A_1$$

We have assumed here low side injection and in general view the spectrum can be seen as 3.2:

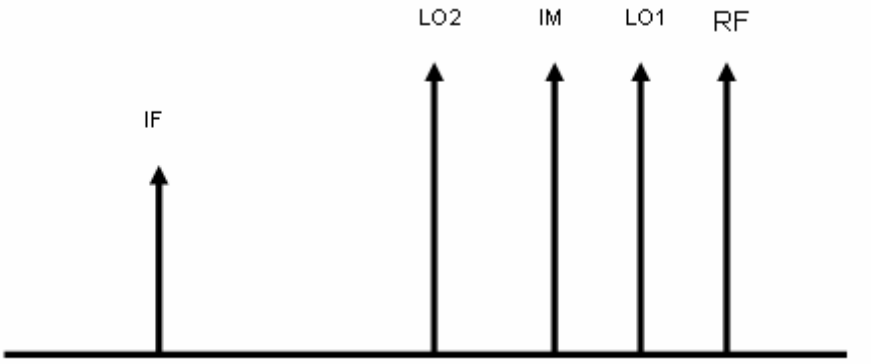

Figure 3.2: Relative position of RF signal, image and LO signal in frequency scale.

So if we put $\cos\omega_{RF}t$ at the RF input, we can write

$$X_{out}(t)=\frac{1}{4}\left(A-\frac{\Delta A}{2}\right)\cos\left(\omega_{IF}t-\frac{\theta}{2}\right)+\frac{1}{4}\left(A+\frac{\Delta A}{2}\right)\cos\left(\omega_{IF}t+\frac{\theta}{2}\right) \tag{3.10}$$

So, we can see that if there is no mismatch, then image will be completely canceled & signal will be doubled in amplitude. Now, the ratio of image-P_{im} to average power of signal-P_{sig} can be written as:

$$\frac{P_{im}}{P_{sig}}=\frac{\left(A+\frac{\Delta A}{2}\right)^2-2\left(A+\frac{\Delta A}{2}\right)\left(A-\frac{\Delta A}{2}\right)\cos\theta+\left(A-\frac{\Delta A}{2}\right)^2}{\left(A+\frac{\Delta A}{2}\right)^2+2\left(A+\frac{\Delta A}{2}\right)\left(A-\frac{\Delta A}{2}\right)\cos\theta+\left(A-\frac{\Delta A}{2}\right)^2} \tag{3.11}$$

This is called image rejection ratio (IRR) and in dB we can write:

$$\text{IRR}|_{\text{dB}}=10\log\frac{\left(1+\frac{\Delta A}{2A}\right)^2-2\left(1+\frac{\Delta A}{2A}\right)\left(1-\frac{\Delta A}{2A}\right)\cos\theta+\left(1-\frac{\Delta A}{2A}\right)^2}{\left(1+\frac{\Delta A}{2A}\right)^2+2\left(1+\frac{\Delta A}{2A}\right)\left(1-\frac{\Delta A}{2A}\right)\cos\theta+\left(1-\frac{\Delta A}{2A}\right)^2} \tag{3.12}$$

Here $\Delta A/A$ is the relative gain mismatch. The total gain mismatch in dB between two paths can be written as

$20\log(A+\Delta A/2)-20\log(A-\Delta A/2)=20\log\{(1+\Delta A/2A)/(1-\Delta A/2A)\}$

In the absence of gain mismatch ($\Delta A=0$) the IIR can be written as: $\text{IIR}|_{\text{dB}}=10\left(\log\left(\tan\frac{\theta}{2}\right)^2\right)$

A matlab plot is provided in fig. 3.3 to show the effect of IIR due to gain and phase mismatch.

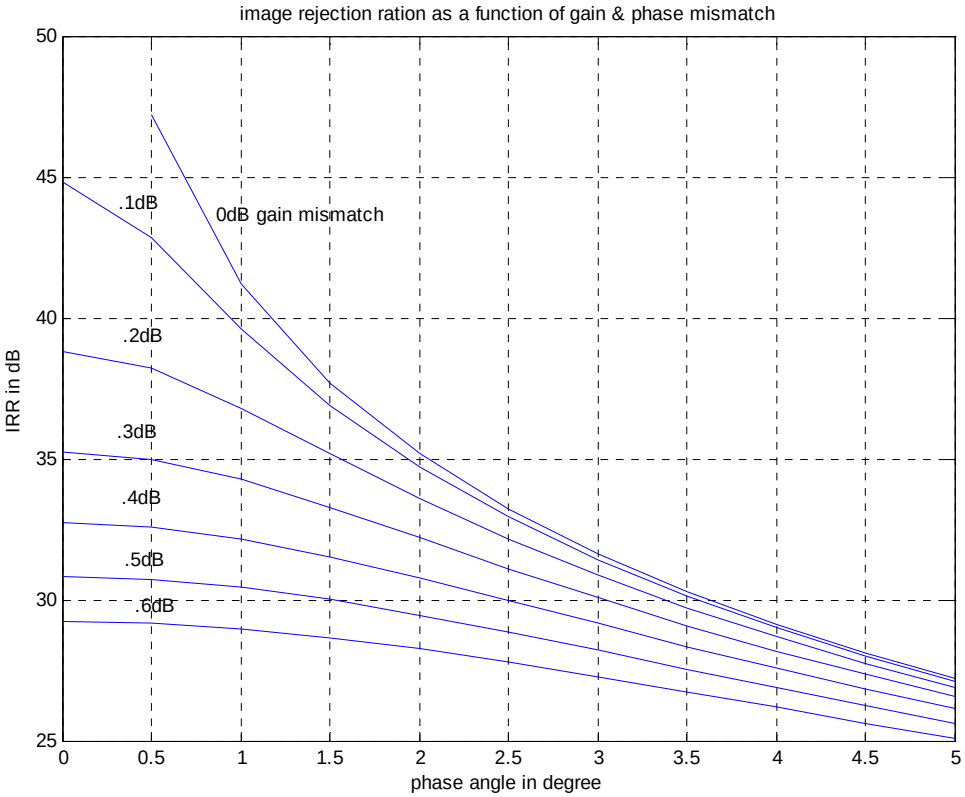

Figure 3.3: IRR as function of phase and gain mismatches

3.3 Previously Reported work:

There are two types of calibration work can be found in literature. One is calibration using a calibrating tone. For this case periodic calibration with external image tone is needed. This is also known as analog calibration [28]. But system like TDMA does not allow this type of periodic calibration. Digitally storing the calibration coefficients solve the problem of periodic calibration. However an external image tone is still needed in the calibration [25]. The other type of calibration does not use any external calibrating tone.

Calibration can be done continuously on-line with some restriction [26, 37]. Another calibration system is reported by [34, 35, 38].

The paper [28] reported an IIR of 57dB with only phase calibration. Addition of gain calibration will increase this number. This calibration method has problem with limited accuracy and excessive power consumption. Mismatch between auxiliary path & signal paths can corrupt this ideal error signal & introduce error that can not be calibrated out. Total 3 mixers are used for phase calibration. In order to generate $\cos(\omega_{IF}t)$, Lo1 & Lo2 mismatches have been ignored.

The paper [25] reported an IRR of 57dB. Two extra (RF) analog mixers are required. Algorithm is slow and not having guaranteed stability. Conditions could arise where algorithm becomes unstable and does not converge to a solution for tuning variables.

The paper [26, 37] reported an IRR of 59dB. The problem with this calibration is that error modeling is complex and lengthy. So recalibration is not possible in short time. Many mixers & multipliers have been used to implement the algorithm, where extra mismatch will corrupt calibration. Although h some IF multipliers have been used, but output equation of those multipliers contains two v_t (each multiplier), which is clearly process, temperature dependent parameter. So, use of more mixers/multipliers will not help to reduce mismatches.

The paper[34, 35, 38] reported an IRR of 47 dB. This modified receiver system is called sampled-data image reject receiver. Here switched-capacitor Hilbert transformer is used

as 90 degree phase shifter. This is not suitable due to low IRR achieved. Also extra mismatches caused by switch-cap filters. Since switch-cap circuit is involved, it is not suitable for continuous time system.

3.4 Proposed Techniques:

Our main focus is to reduce number of mixers/multipliers in order to keep the mismatch minimum and hence attain higher IRR. Two techniques have been investigated.

3.4.1 Calibration without external calibrating tone:

Calibration is done in two step. In first step error signal is generated due to mismatches. This error signal is used to adjust the phase shift of 2^{nd} LO in next step. After adjusting the phase shift of LO signal a_3 and a_4, signals arrive at point C and D of figure 3.1 become free from phase mismatches. This will be shown by equation later in this section. When receiver is not receiving (off line) as in TDMA, we can disconnect the RF input using switch s_1. During this period of time error signal C_θ is generated using an algorithm as shown in figure 3.4. This algorithm does not need any external calibrating tone and can be explained below.

We generate two signal b_1 and b_2 according to the proposed algorithm as given by equation 3.13 and 3.14 respectively. Signals b_1 and b_2 are passed through the low pass filter, such that the low frequency (dc term) term can be filtered out. Each of those terms are multiplied by the gain factor as given by equation 3.15 and 3.16 respectively.

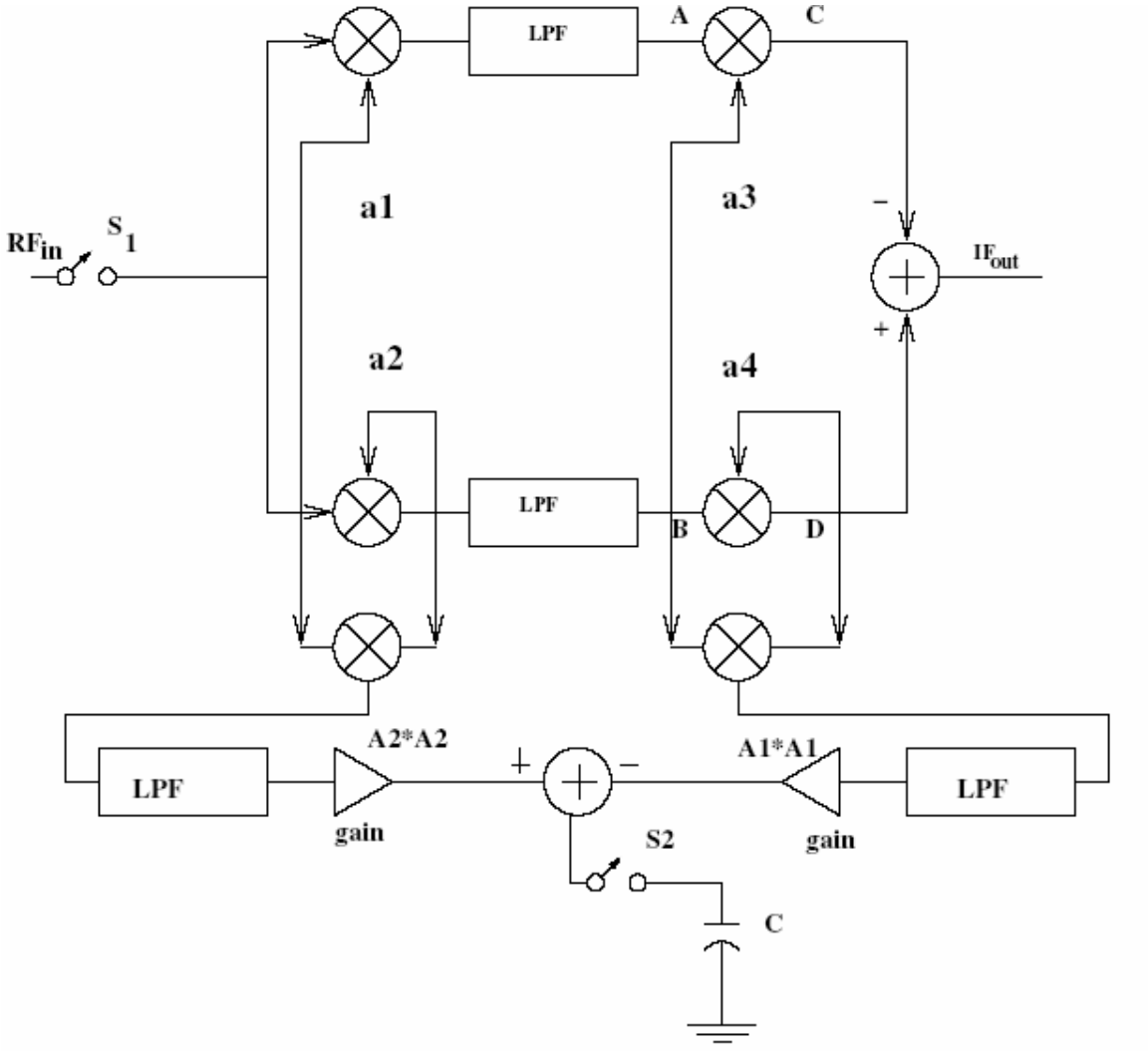

Figure 3.4: Error generation algorithm

$$b_1 = a_1 a_2 = \frac{1}{2}\left(A_1^{\,2} - \frac{\Delta A_1^{\,2}}{4} \right)\{\sin(2\omega_1 t) + \sin\theta_1\}$$
$$\cong \frac{1}{2} A_1^{\,2}\{\sin(2\omega_1 t) + \sin\theta_1\} \qquad (3.13)$$

LPF(b_1) $\cong \frac{1}{2} A_1^2 \theta_1$ when θ_1 is small.

$$b_2 = a_3 a_4 = \frac{1}{2}\left(A_2^{\,2} - \frac{\Delta A_2^{\,2}}{4} \right)\{\sin(2\omega_2 t) - \sin\theta_2\} \cong \frac{1}{2} A_2^{\,2}\{\sin(2\omega_2 t) - \sin\theta_2\} \tag{3.14}$$

LPF(b_2) $\cong -\frac{1}{2} A_2^2 \theta_2$ when θ_2 is small

$$A_2^{\,2} LPF(b_1) = \frac{1}{2} A_1^{\,2} A_2^{\,2} \theta_1 \tag{3.15}$$

$$A_1^{\,2} LPF(b_2) = -\frac{1}{2} A_1^{\,2} A_2^{\,2} \theta_2 \tag{3.16}$$

Subtracting (3.16) from (3.15)we can write error C_θ=0.5*A^2*θ where $\theta=\theta_1+\theta_2$ and $A=A_1A_2$

So we can tell that when θ=0 then C_θ=0 i.e., error will be zero. This error signal is stored in the capacitor through switch s_2 to compensate for mismatches when receiver is in receiving mode. Error generation algorithm is used as a subsystem for the whole correction phase when receiver is in receiving mode. This simulink subsystem named as myerror is shown in figure 3.5, where a_1, a_2, a_3, and a_4 are the input signal. For a phase mismatch of 2^0 ($\theta_1/2=.45^0$ and $\theta_2/2=.55^0$) and small gain mismatch the error signal $C_\theta = 1^0$ (.0175) which is half of the total phase mismatch. However we want to find and nullify the effect of mismatches at IF frequency. That's why a higher order (greater than 8) Low pass filter with cut off frequency 72 MHz (IF) has been chosen in figure 3.4.

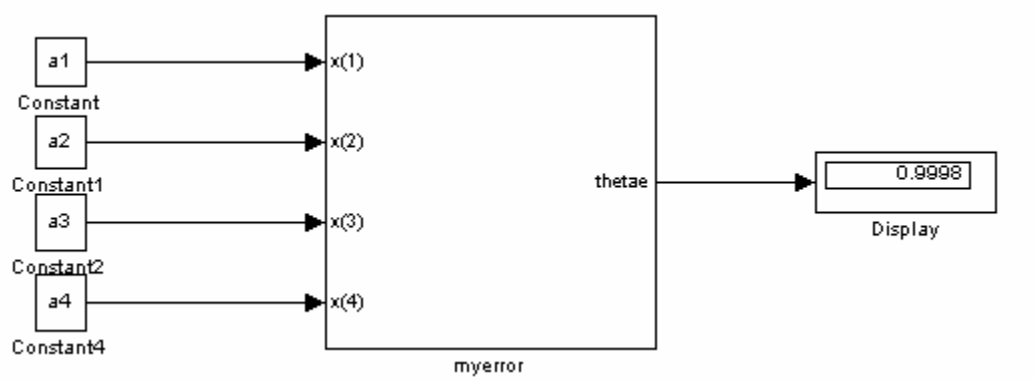

Figure 3.5: Simulink subsystem "myerror"

During the correction phase, error signal that was stored earlier in the capacitor is fed to a subsystem block named as "phase correction block" as shown in figure 3.7. The input for this subsystem is 2nd LO signal with differential mismatch (a_3, and a_4), mismatch control signal thetaT of 2nd LO, and error signal from figure 3.5. We are using a mismatch control signal as thetaT in order to see the effect of different mismatches that can be place in the system from outside. This "phase correction block" is nothing but an all pass filter, which is used to change the phase of the 2nd LO. CMOS version of all pass filter is shown in figure 3.26, is known as variable-delay gain circuit. This all pass filter (phase correction block) shift the phase of 2nd LO signal (a_3, and a_4) by either - C_θ or C_θ depending on the phase of a_3, and a_4. That's why a switch is needed in simulink to make sure that the phase of LO signal has been shifted correctly. Otherwise instead of reduced mismatch effect at IF, we will observe more mismatch effect. However for circuit implementation of all pass filter as shown in figure 3.26, no switch is required. The change of phase at the input V_{in}^+ and V_{in}^- is reflected at output V_o^+ and V_o^- according to

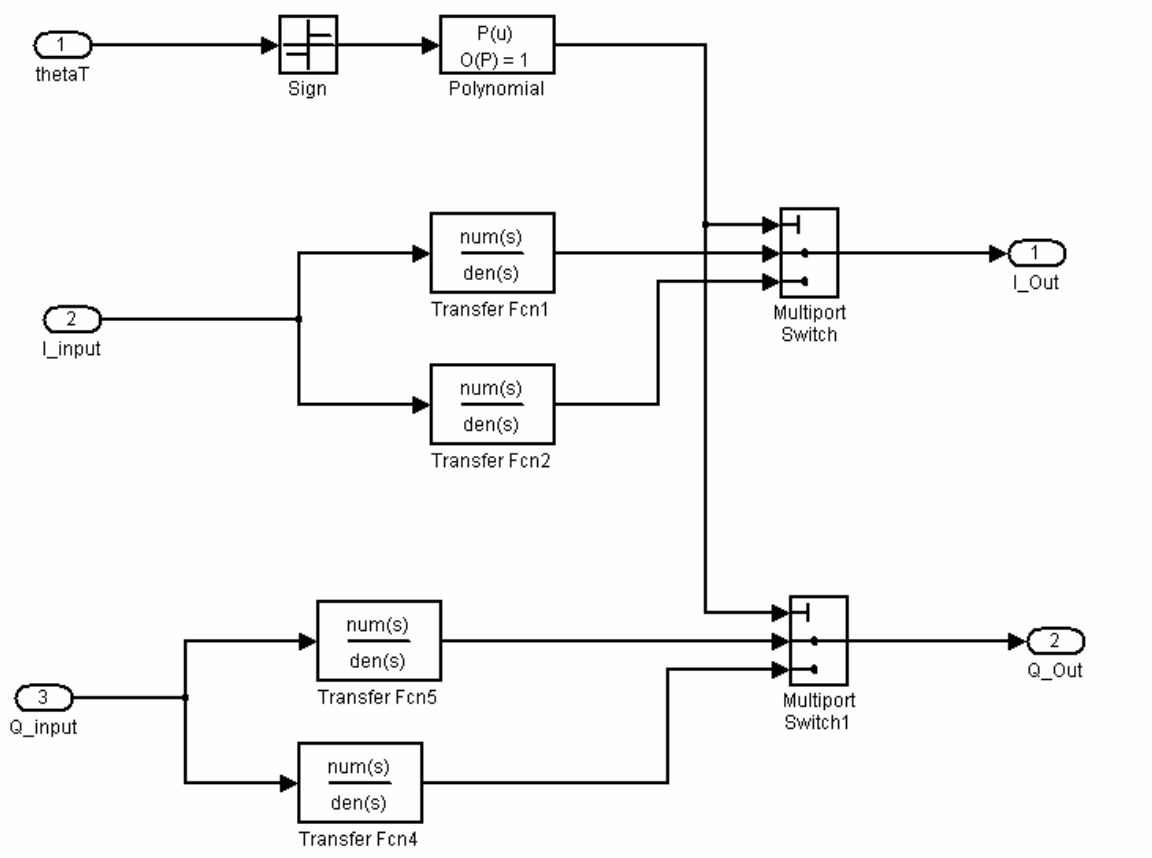

Figure 3.6: Switching in subsystem "phase correction block"

equation 3.29 and 3.30 respectively. The switching arrangement is shown in figure 3.6. When phase is shifted by a negative phase angle, then the transfer function of the all pass filter is given by (s-a/(s+a)). However, if phase is shifted by a positive angle the transfer function can be written as: -(s-a/(s+a)). In this figure thetaT is the control signal for 2nd LO mismatches. Signal $a_{3,}$ and a_4 can be written as:

$$a_3 = \left(A_2 + \frac{\Delta A_2}{2}\right)\sin\left(\omega_2 t - \frac{\theta_2}{2}\right) \text{ and } a_4 = \left(A_2 - \frac{\Delta A_2}{2}\right)\cos\left(\omega_2 t + \frac{\theta_2}{2}\right).$$

Now, we can see that phase of a_3 is delayed by $\theta_2/2$ and phase of a_4 is delayed by $-\theta_2/2$. So, signal a_3 will be delayed by $-C_\theta$ and signal a_4 will be delayed C_θ. In our case, $a_3 = 1.015\sin(\omega_2 t - .0096)$ and $a_4 = .9850\cos(\omega_2 t + .0096)$. After the phase shifted by $\pm.0175$ we can write $a_3 = 1.015\sin(\omega_2 t + .0079)$ and $a_4 = .9850\cos(\omega_2 t - .0079)$. Using equation 3.7 image signal at point C in figure 3.4 can be written as:

$$X_C(t) = \frac{1}{2}(1.01)(1.015)\{\sin(\omega_1 t - \omega_{IM} t + .0079)\sin(\omega_2 t + .0079)\}$$
$$\cong \frac{1}{4}(1.0250)\cos(\omega_{IF} t)$$

Similarly signal at point D for this case can be written as:

$$X_D(t) = \frac{1}{2}(.99)(.9850)\{\cos(\omega_1 t - \omega_{IM} t - .0079)\cos(\omega_2 t - .0079)\}$$
$$\cong \frac{1}{4}(.9750)\cos(\omega_{IF} t)$$

Thus the phase mismatch has been eliminated. The only mismatch present at that point is due to the difference in gain only. Signal $X_C(t)$ and $X_D(t)$ are subtracted at IF frequency. So for the image signal a low value (amplitude) is observed in the time domain as shown in figure 3.9. It is not completely zero because of small gain mismatches present in those two paths. However in order to find the IRR, amplitude of this image signal is stored in workspace and a matlab program is used to calculate the FFT of the signal. Similarly for RF signal FFT is calculated. For RF signal the amplitude increases as given by equation 3.10. The matlab program is presented at the end of the chapter.

3.4.2 Calibration using external tone:

In this section error generation using calibrating tone is presented. Once the error is generated, the same procedure as described in previous section can be applied to eliminate phase mismatch. An image tone of $\cos(\omega_{IM}t)$ is used and the output can be written as:

$$X_{out}(t) = \frac{1}{4}\left(A - \frac{\Delta A}{2}\right)\cos\left(\omega_{IF}t - \frac{\theta}{2}\right) - \frac{1}{4}\left(A + \frac{\Delta A}{2}\right)\cos\left(\omega_{IF}t + \frac{\theta}{2}\right)$$

For simplicity we will neglect ¼ term and at the end of the derivation we will introduce it. So we can write:

$$X_{out}(t) = A\left\{\cos\left(\omega_{IF}t - \frac{\theta}{2}\right) - \cos\left(\omega_{IF}t + \frac{\theta}{2}\right)\right\} - \frac{\Delta A}{2}\left\{\cos\left(\omega_{IF}t - \frac{\theta}{2}\right) + \cos\left(\omega_{IF}t + \frac{\theta}{2}\right)\right\}$$

$$= A\left\{2\sin\omega_{IF}t\sin\frac{\theta}{2}\right\} - \frac{\Delta A}{2}\left\{2\cos\omega_{IF}t\cos\frac{\theta}{2}\right\} \tag{3.17}$$

$$X_{out}\left\{\left(A + \frac{\Delta A}{2}\right)\cos\left(\omega_{IF}t + \frac{\theta}{2}\right)\right\}$$

$$= A^2\left\{\sin\left(2\omega_{IF}t + \frac{\theta}{2}\right)\sin\frac{\theta}{2} - \sin^2\frac{\theta}{2}\right\}$$

$$+ \frac{\Delta AA}{2}\left\{\sin\left(2\omega_{IF}t + \frac{\theta}{2}\right)\sin\frac{\theta}{2} - \sin^2\frac{\theta}{2}\right\} \tag{3.18}$$

$$- \frac{\Delta AA}{2}\left\{\cos\left(2\omega_{IF}t + \frac{\theta}{2}\right)\cos\frac{\theta}{2} + \cos^2\frac{\theta}{2}\right\}$$

$$- \frac{\Delta A^2}{4}\left\{\cos\left(2\omega_{IF}t + \frac{\theta}{2}\right)\cos\frac{\theta}{2} + \cos^2\frac{\theta}{2}\right\}$$

$$
\begin{aligned}
X_{out}\left\{\left(A-\frac{\Delta A}{2}\right)\cos\left(\omega_{IF}t-\frac{\theta}{2}\right)\right\} &= A^2\left\{\sin\left(2\omega_{IF}t-\frac{\theta}{2}\right)\sin\frac{\theta}{2}+\sin^2\frac{\theta}{2}\right\} \\
&-\frac{\Delta AA}{2}\left\{\sin\left(2\omega_{IF}t-\frac{\theta}{2}\right)\sin\frac{\theta}{2}+\sin^2\frac{\theta}{2}\right\} \\
&-\frac{\Delta AA}{2}\left\{\cos\left(2\omega_{IF}t-\frac{\theta}{2}\right)\cos\frac{\theta}{2}+\cos^2\frac{\theta}{2}\right\} \\
&+\frac{\Delta A^2}{4}\left\{\cos\left(2\omega_{IF}t-\frac{\theta}{2}\right)\cos\frac{\theta}{2}+\cos^2\frac{\theta}{2}\right\}
\end{aligned}
\tag{3.19}
$$

After low pass filtering above two expressions we can write

$$
LPF(3.18) = -A^2\sin^2\frac{\theta}{2}-\frac{A\Delta A}{2}\sin^2\frac{\theta}{2}-\frac{\Delta AA}{2}\cos^2\frac{\theta}{2}-\frac{\Delta A^2}{4}\cos^2\frac{\theta}{2} \tag{3.20}
$$

$$
LPF(3.19) = A^2\sin^2\frac{\theta}{2}-\frac{A\Delta A}{2}\sin^2\frac{\theta}{2}-\frac{\Delta AA}{2}\cos^2\frac{\theta}{2}+\frac{\Delta A^2}{4}\cos^2\frac{\theta}{2} \tag{3.21}
$$

$$
\frac{4}{16}\{LPF(3.19)-LPF(3.18)\} = \frac{4}{16}\left\{2A^2\sin^2\frac{\theta}{2}+2\frac{\Delta A^2}{4}\cos^2\frac{\theta}{2}\right\} \cong \frac{4}{8}A^2\frac{\theta}{2} \tag{3.22}
$$

So we can write $V_{c\theta} = \frac{1}{2}A^2\theta$. Figure 3.7 illustrates this idea.

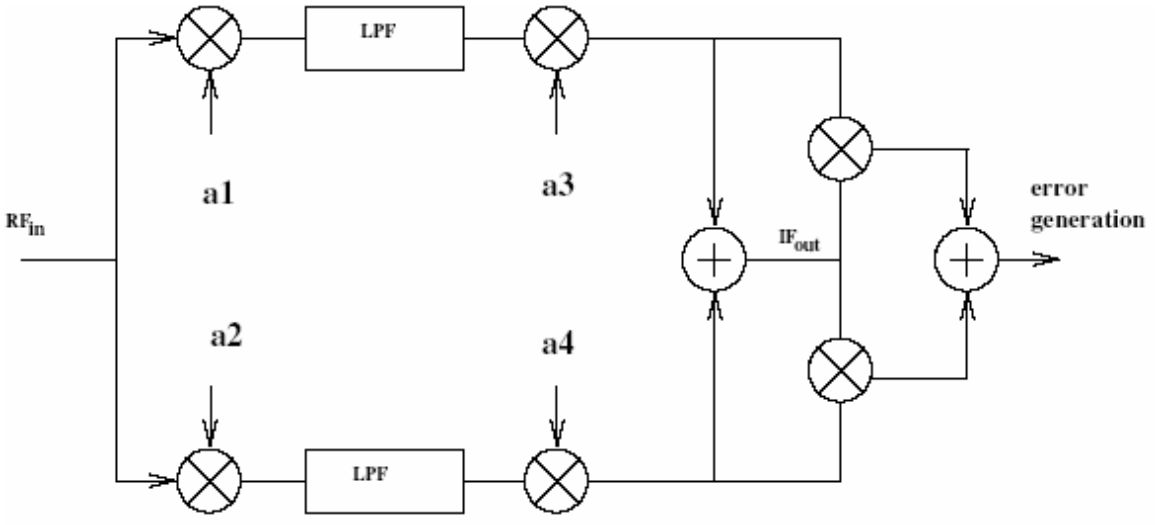

Figure 3.7: Error generation using external tone

3.4.3 System Implementation:

The calibration circuit has been implemented using simulink and cadence. In this report simulink implementation is presented. Fig.3.5. presents the error modeling of Weaver receiver without using external tone. We have already seen from figure.3.3 the degradation of IRR due to gain mismatch of .1 to .6dB and phase mismatch of .5 to 5 degree. In this dissertation we have assumed phase mismatch of 2 degree and a relatively small gain mismatch. Once we generate the error for this particular mismatch, then we try tried to correct the mismatch using the following circuit. Here the phase correction has been done in the second LO. The following parameters [37] have been chosen for simulation:

1st LO frequency =1.6GHz

2nd LO frequency =200MHz

RF signal and its image are chosen as:

RF_{in} frequency = 1872 MHz

Image frequency = 1328 MHz

IF frequency = 72 MHz

Phase error signal is shown in Fig. 3.5. This model determine the error for a small gain mismatch and a phase mismatch of 2 degree. This signal is used in a phase shifter to correct the phase in second LO. A modified all pass filter is used to shift the LO phases. Simulink model of the system when phase correction is applied, shown in Fig. 3.8. Fig. 3.9 and Fig. 3.10 represent the time domain image and RF signal at 72 MHz after the correction has been made. We notice that ideally we should get zero for image signal and in this simulation after the calibration our image signal is very small which matches the criteria. FFT of the RF and image signal is shown in Fig. 3.11 and Fig.3.12 without calibration . Image and RF signal after calibration is presented in Fig. 3.13 and 3.14 respectively. The sampling frequency is 500MHz. From this plot we can find the IRR after calibration. IRR after calibration is (3.5+56)=59.5dB. Without calibration IRR is limited to 36 dB. So it is a net improvement of 24 dB. For simplicity also the amplitudes have been normalized, so that A_1 & A_2 as well as image and RF signal amplitude is 1.

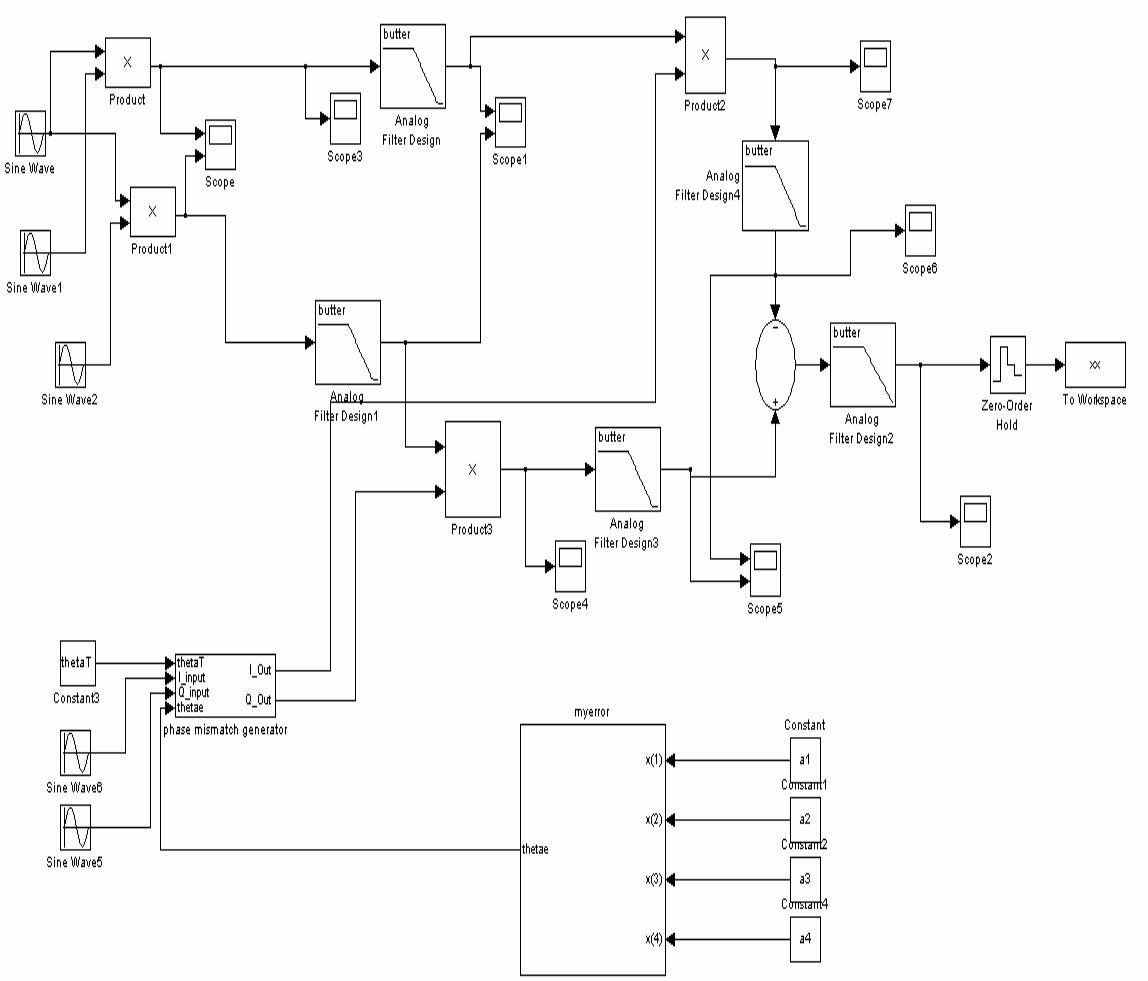

Fig. 3.8: Simulink model of the system when phase correction is applied to RF+image signal

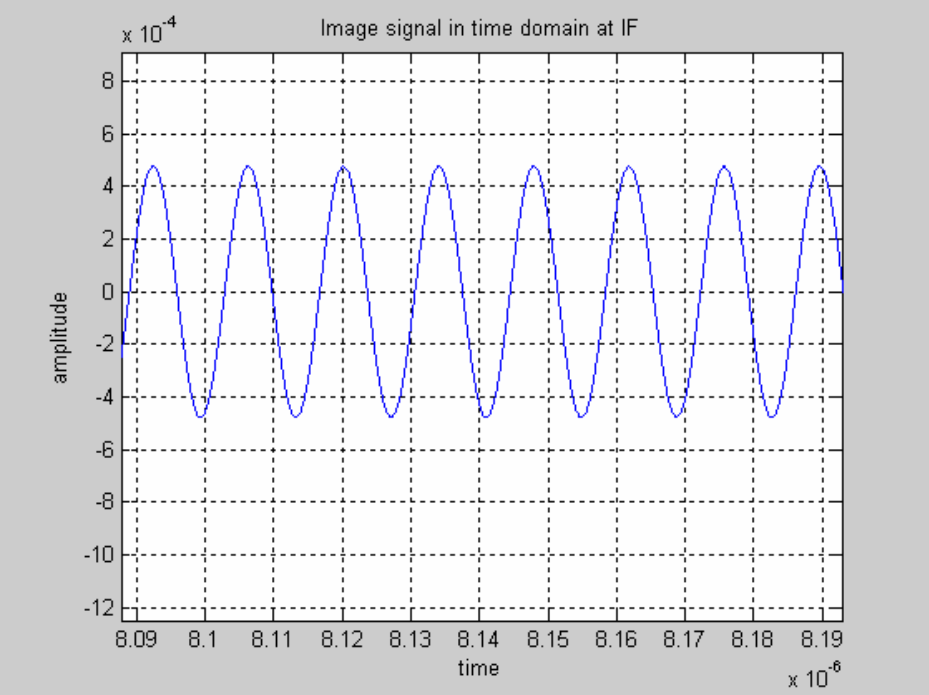

Fig. 3.9: Time domain representation of image signal at IF(72MHz) frequency

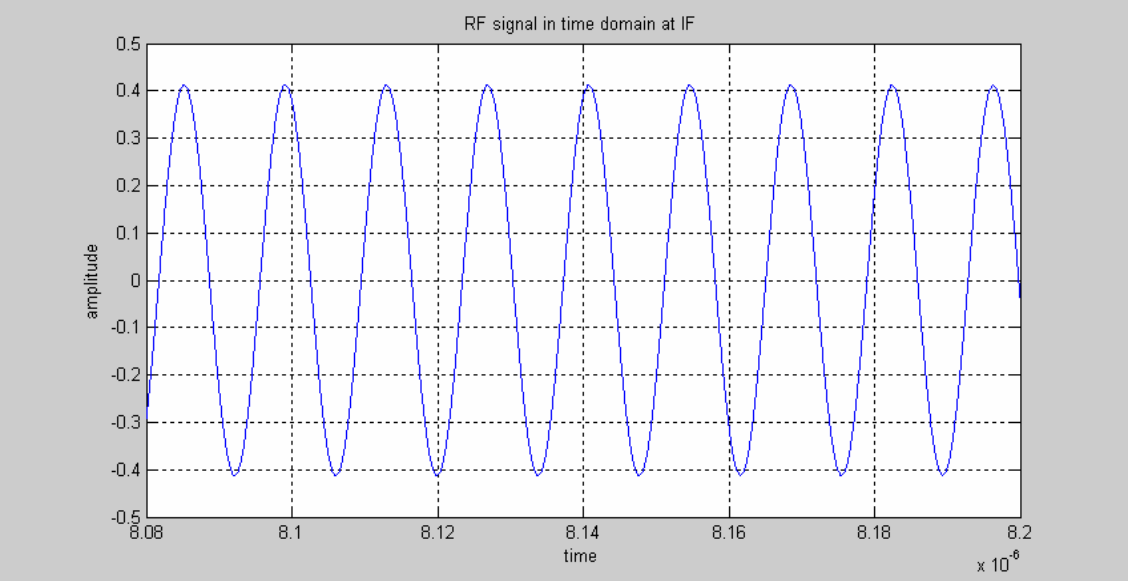

Fig. 3.10: Time domain representation of RF signal at IF(72 MHz) frequency

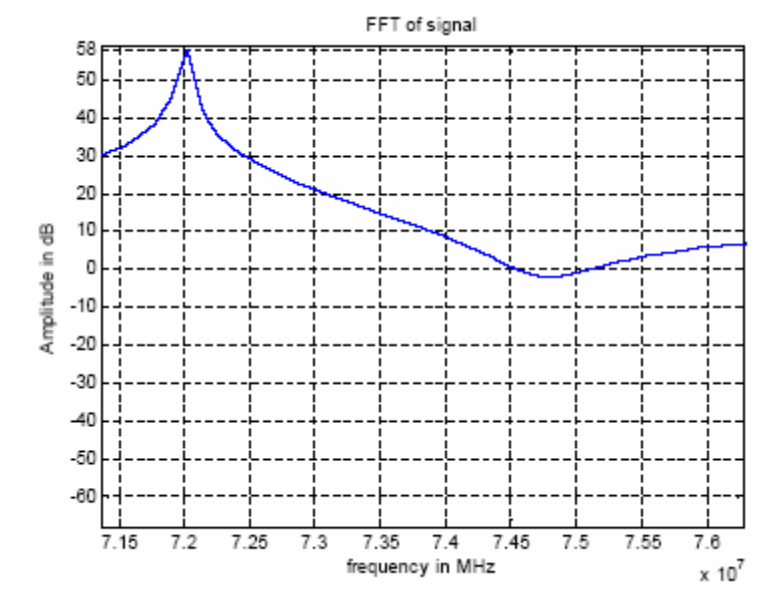

Figure 3.11: Content of the signal at 72 MHz before calibration

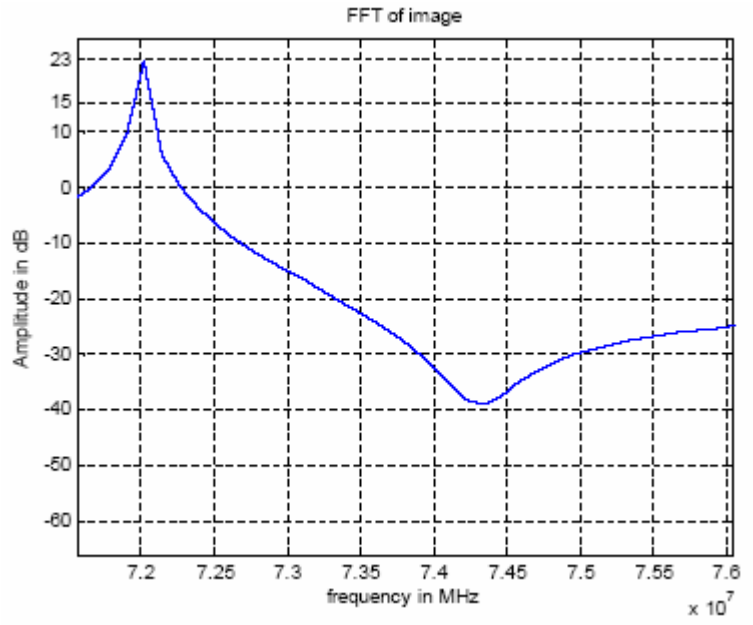

Figure 3.12: Content of the image at 72 MHz before calibration

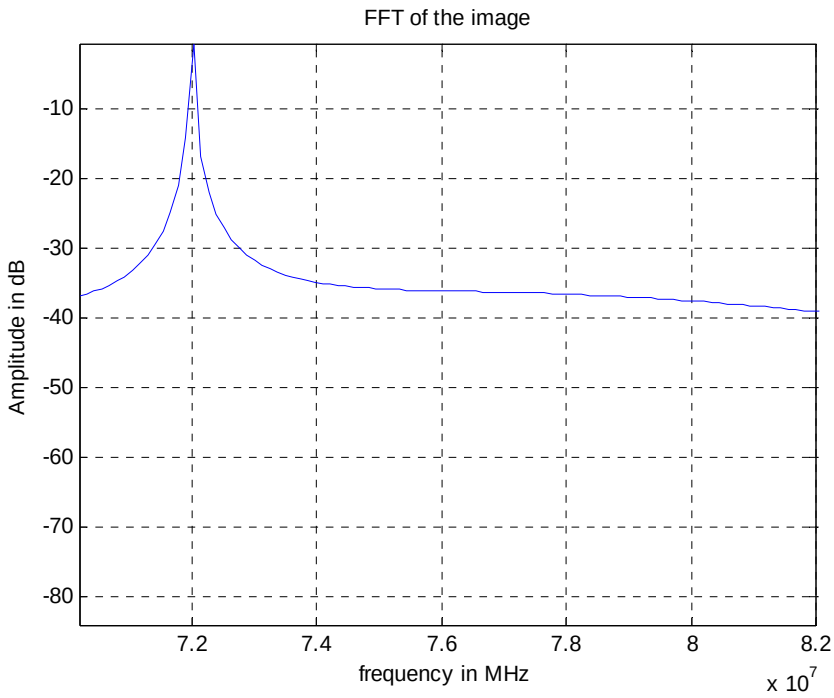

Figure 3.13: Content of the image signal at 72 MHz after calibration

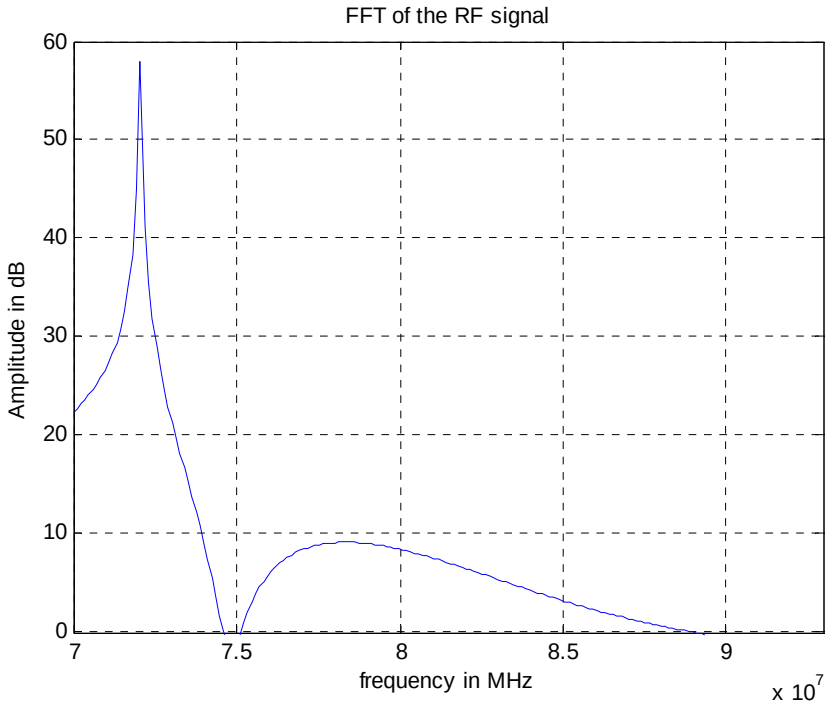

Figure 3.14: Content of the RF signal at 72 MHz after calibration

Weaver architecture is less sensitive to mismatches, but it suffers from the secondary image if the second down conversion translates the spectrum to a nonzero frequency. Also, harmonics of second LO frequency may downconvert unfiltered interferers from the first IF to the second. Hartley receiver [31] does not suffer from those problems but it is more sensitive to mismatches. Figure 3.15 shows the mismatch model of the modified Hartley receiver.

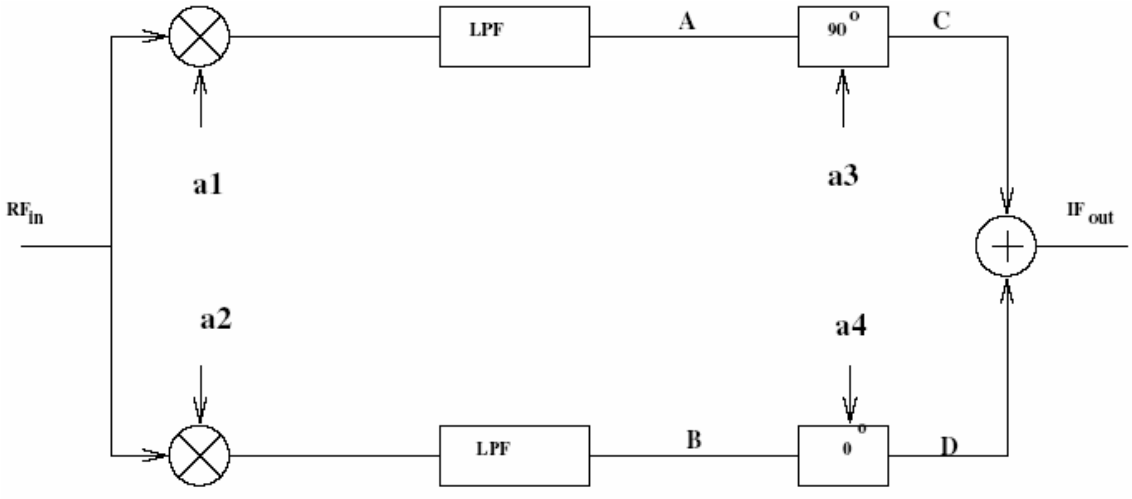

Figure 3.15: Hartley receiver with mismatches

3.5 Mismatching Modeling for Hartley Receiver

In this figure a_1, a_2, a_3, a_4 represent mismatches caused by the Lo signals and phase shift network. Here,

$$a_1 = \left(A_1 + \frac{\Delta A_1}{2} \right) \sin\left(\omega_1 t + \frac{\theta_1}{2} \right)$$

$$a_2 = \left(A_1 - \frac{\Delta A_1}{2} \right) \cos\left(\omega_1 t - \frac{\theta_1}{2} \right)$$

$$a_3 = \left[\left(A_2 + \frac{\Delta A_2}{2} \right), \left(90^o - \frac{\theta_2}{2} \right) \right]$$

$$a_4 = \left[\left(A_2 - \frac{\Delta A_2}{2} \right), \frac{\theta_2}{2} \right]$$

In reality the 90 degree phase shift network is realized using an RC-CR circuit shown in figure 3.16. It gives +45 degree in one path and -45 degree in the other path. The mismatches in this phase shift network comes from the variation of r and C due to process or temperature. Gain mismatch between the two phase shift stages can also arise from frequency deviation. This is because complete image cancellation occurs at only $\omega_{IF} = 1/(RC)$. For example, if the channel bandwidth is not much less than ω_{IF}, then IRR degrades substantially near the edges of the channel. Here gain mismatches are distributed as ΔA_1 & ΔA_2. Phase mismatches are distributed as θ_1 & θ_2. We apply an image tone $\cos\omega_{IM}t$ at the input to see the effect of mismatch.

$$X_A(t) = \frac{1}{2}\left(A_1 + \frac{\Delta A_1}{2} \right) \sin\left(\omega_{IF} t + \frac{\theta_1}{2} \right) \tag{3.23}$$

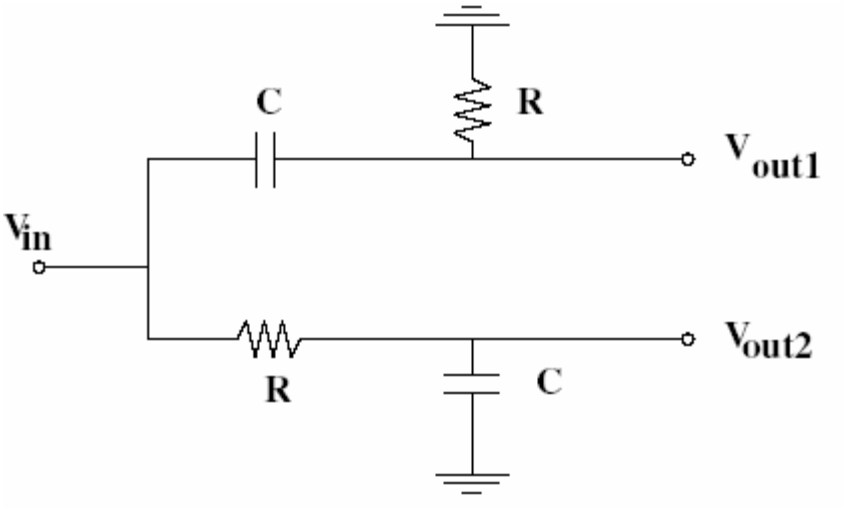

Figure 3.16: RC-CR phase shift realization

$$X_B(t) = \frac{1}{2}\left(A_1 - \frac{\Delta A_1}{2}\right)\cos\left(\omega_{IF}t - \frac{\theta 1}{2}\right) \tag{3.22}$$

$$\begin{aligned} X_C(t) &= \frac{1}{2}\left(A_1 + \frac{\Delta A_1}{2}\right)\left(A_2 + \frac{\Delta A_2}{2}\right)\left\{-\cos\left(\omega_{IF}t + \frac{\theta_1 + \theta_2}{2}\right)\right\} \\ &= -\frac{1}{2}\left(A + \frac{\Delta A}{2}\right)\cos\left(\omega_{IF}t + \frac{\theta}{2}\right) \end{aligned} \tag{3.24}$$

$$\begin{aligned} X_D(t) &= \frac{1}{2}\left(A_1 + \frac{\Delta A_1}{2}\right)\left(A_2 - \frac{\Delta A_2}{2}\right)\cos\left(\omega_{IF}t - \frac{\theta_1 + \theta_2}{2}\right) \\ &= \frac{1}{2}\left(A - \frac{\Delta A}{2}\right)\cos\left(\omega_{IF}t - \frac{\theta}{2}\right) \end{aligned} \tag{3.25}$$

$$X_{out}(t) = X_{IF}(t) = \frac{1}{2}\left(A - \frac{\Delta A}{2}\right)\cos\left(\omega_{IF}t - \frac{\theta}{2}\right) - \frac{1}{2}\left(A + \frac{\Delta A}{2}\right)\cos\left(\omega_{IF}t + \frac{\theta}{2}\right) \quad (3.26)$$

Here, $\omega_{IM}=\omega_{LO}-\omega_{IF,}$ $A=A_1A_2$, $\theta=\theta_1+\theta_2$, and $\Delta A=\Delta A_1A2+\Delta A_2A_1$. So we can see that once the mismatches are gone, we get complete image cancellation.

3.5.1 Calibration Algorithm

The calibration for this system can also be divided in two parts. First part involves with error generation and second part involves with phase correction at the phase shifter. Error generation algorithm can be described as shown in figure 3.17.

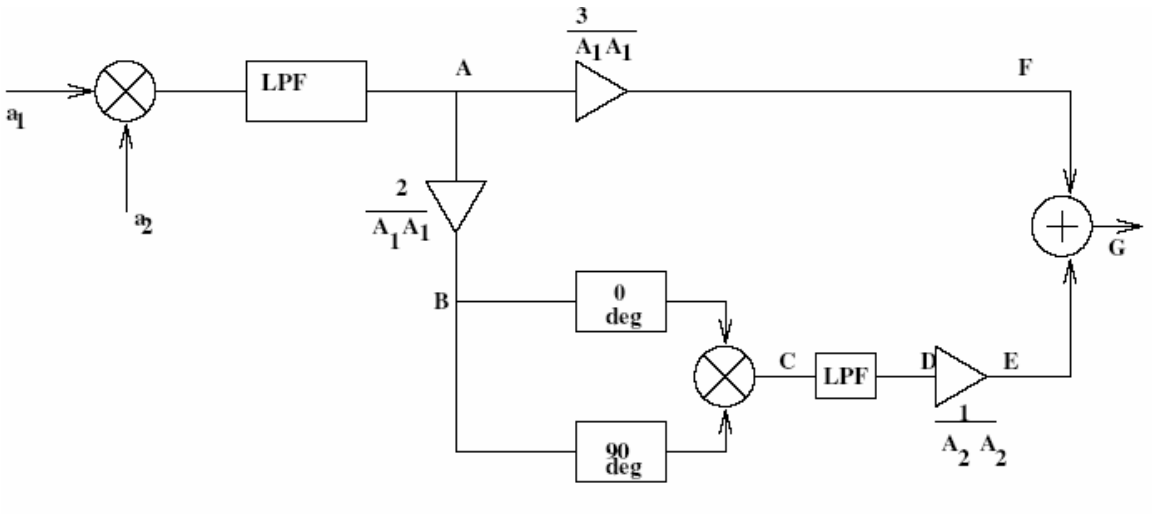

Figure 3.17: Calibration system for Hartley receiver

In this method we do phase calibration without using any calibrating tone. In order to do so, we generate two signal b_1, and b_2 such that

$$b_1 = a_1 a_2 = \frac{1}{2}\left(A_1^{\,2} - \frac{\Delta A_1^{\,2}}{4} \right)\{\sin(2\omega_1 t) + \sin\theta_1\} \cong \frac{1}{2} A_1^{\,2}\{\sin(2\omega_1 t) + \sin\theta_1\} \qquad (3.27)$$

$\text{LPF}(b_1) \cong \frac{1}{2} A_1^2 \theta_1$ when θ_1 is small. We collect this signal at point A. This is amplified by $3/A_1^2$ and the output signal b_2 goes to point F. Signal b_1 is passed through another amplifier with gain $2/A_1^2$. Once it arrive at point B the signal is pass through two phase shifters in order to get phase shift signals $b_3 = (1/2)A_1^2(A_2 - \Delta A_2/2)\sin(\theta_1 - \theta_2/2)$ and $b_4 = -(1/2)A_1^2(A_2 - \Delta A_2/2)\cos(\theta_1 + \theta_2/2)$ respectively. b_3 and b_4 are multiplied and produce another signal b_5 (= $b_3 b_6$) at point C. Signal b_5 passes through a low pass filter and an amplifier with gain $1/A_2^2$ to produce a signal $b_6 = (1/2)A_2^2\theta_2 - A_2^2\theta_1$. Signal b_6 and b_2 are added and finally collected at point G to get the error signal $C_\theta = 0.5\theta$. This error signal is stored in the capacitor through a switch to compensate for mismatches when receiver is in receiving mode. Error generation algorithm is used as a subsystem for the whole correction phase when receiver is in receiving mode. This simulink subsystem named as myerror1 is shown in figure 3.18, where a_1, a_2, a_3, and a_4 are the input signal. For a phase mismatch of 2^0 ($\theta_1/2 = .45^0$ and $\theta_2/2 = .55^0$) and small gain mismatch the error signal $C_\theta = .0175$ (1^0) which is half of the total phase mismatch. However we want to find and nullify the effect of mismatches at IF frequency. That's why a higher order (greater than 8) Low pass filter with cut off frequency 100 MHz (IF) has been chosen in figure 3.16.

During the correction phase, error signal that was stored earlier in the capacitor is fed to a subsystem block named as “phase correction block” as shown in figure 3.8. Phases of LO signal a_3, and a_4 are adjusted the same way as described in section 3.4.1. Signal and image content at IF frequency for those phase corrected signal can be calculated using the FFT program as described in section 3.7. RF & Image frequency for Hartley receiver simulation has been chosen as 1.8 and 1.6 GHz respectively.

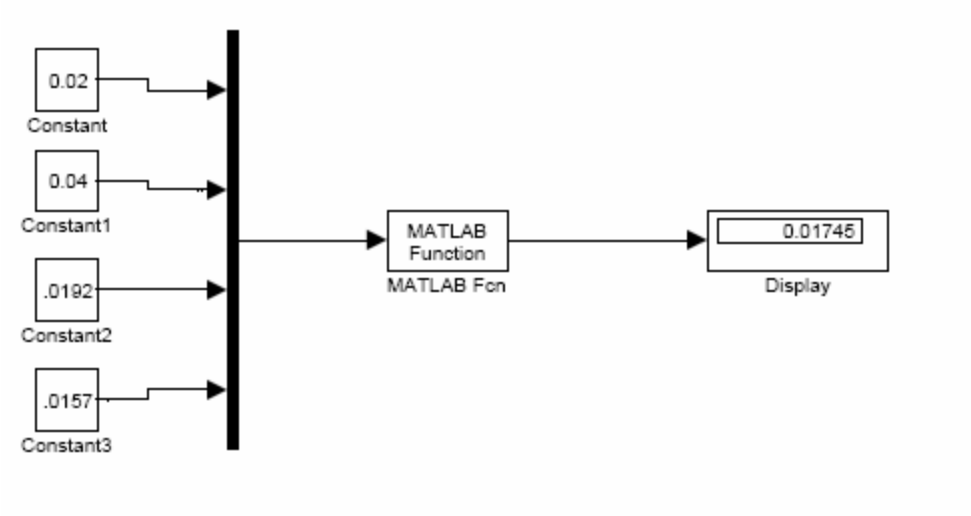

Figure 3.18: Simulink Subsystem “myerror1” for Hartley receiver

3.5.2 Simulink Simulation

The simulink model of the system when phase correction signal is applied, shown in Fig. 3.19. The FFT of the RF and image signal is presented in figure 3.20 and 3.21 respectively without calibration. Those have been shown in figure 3.22 and 3.23 respectively after the calibration. From the figures it can be shown that IRR before calibration is limited to 34 dB and it jumps to above 59 dB after the calibration. Hence a net improvement of 25 dB has been achieved.

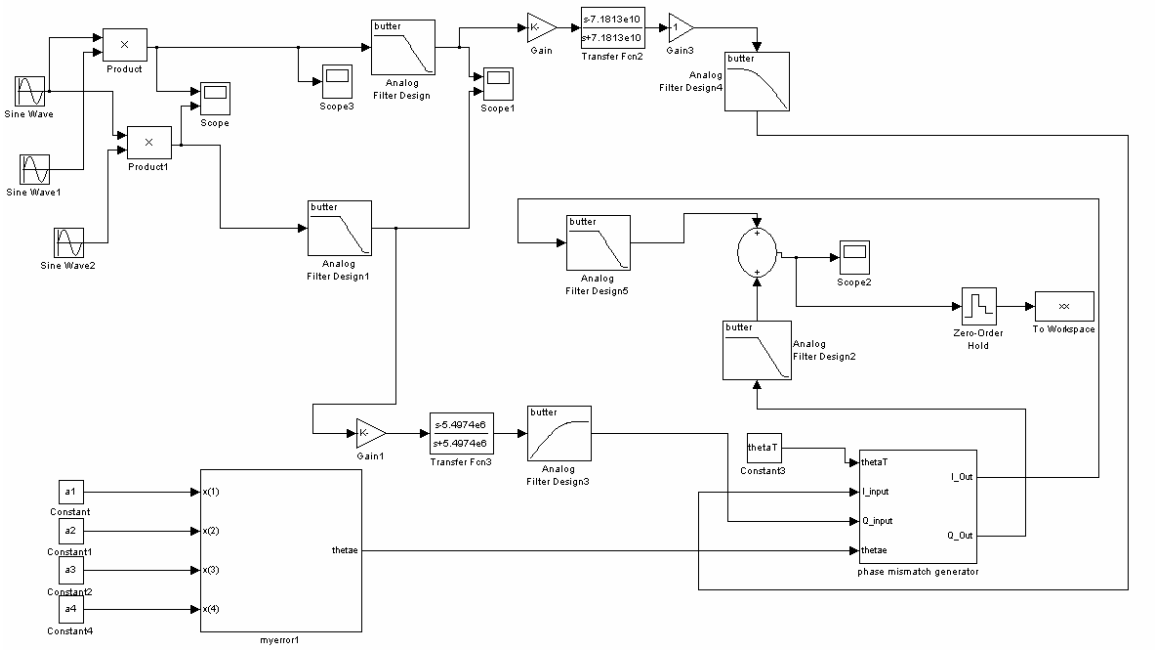

Figure 3.19: Simulink model with calibration for Hartley receiver

3.6 CMOS realization of Receiver

We will now discuss realization of some components in CMOS technology. Here any high gain single stage op-amp will be sufficient for amplifier. A simple folded cascade op-amp with PMOS load is chosen as shown in Figure 3.24. In order to calculate it's small signal gain, first R_{out} and G_m need to be calculated. Using the half circuit technique we can show that $G_m = g_{m1}$. Also $R_{out} \approx R_{op} \| [(g_{m3}+g_{mb3})r_{o3}(r_{o1} \| r_{o5})]$, where $R_{op} \approx (g_{m7}+g_{mb7})r_{o7}r_{o9}$. Gain can be written as:

$$|A_v| \approx g_{m1}\{[(g_{m3}+g_{mb3})r_{o3}(r_{o1} \| r_{o5})] \| [(g_{m7}+g_{mb7})r_{o7}r_{o9}]\} \quad (3.28)$$

Since it is a differential circuit, a common-mode feedback is need as shown in Figure 3.25.

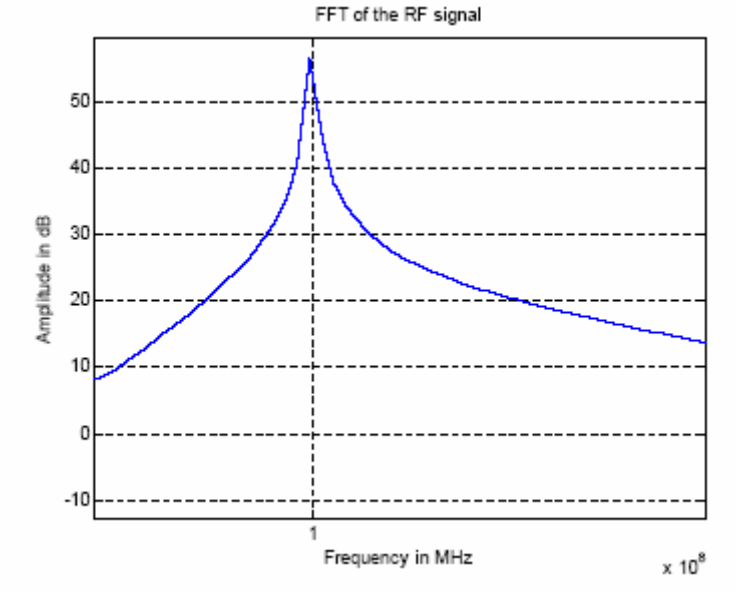

Figure 3.20: Content of RF signal at 100 MHz before calibration

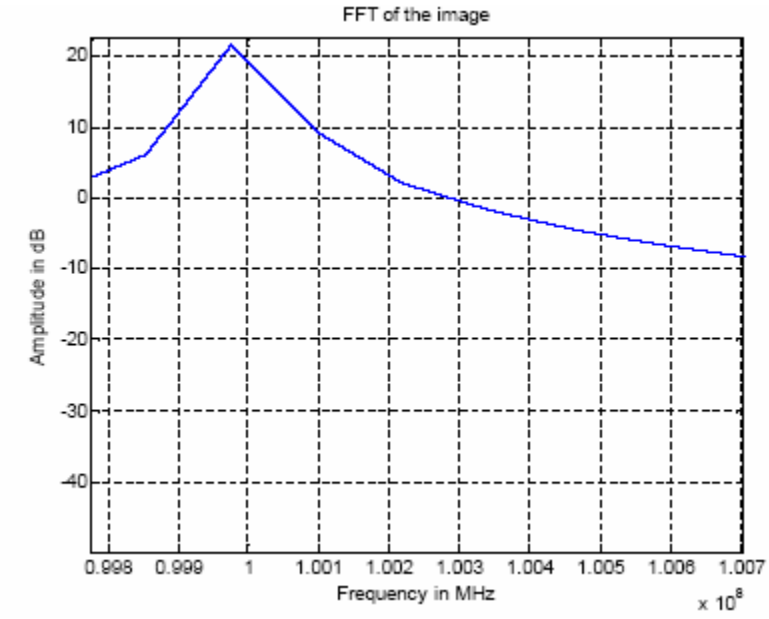

Figure 3.21: Content of image signal at 100 MHz before calibration

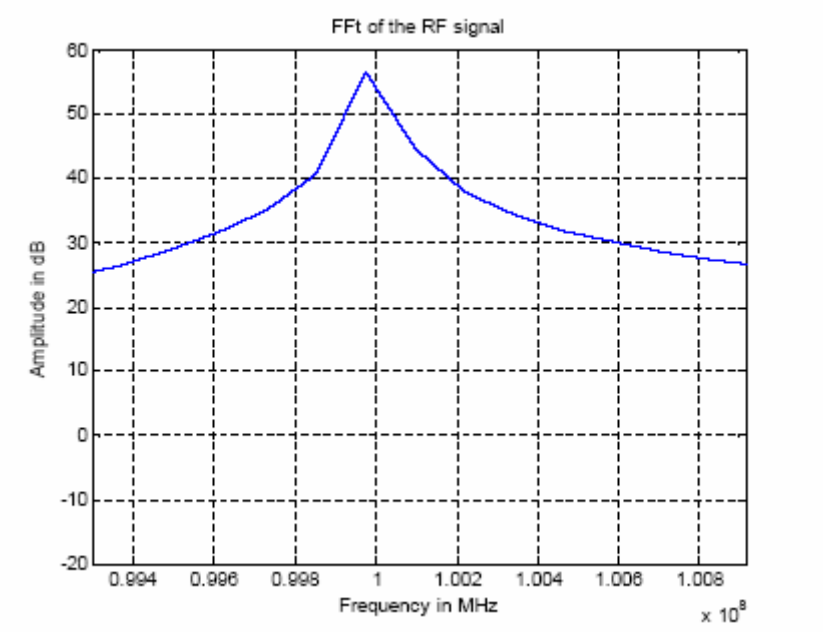

Figure 3.22: Content of RF signal at 100 MHz after calibration

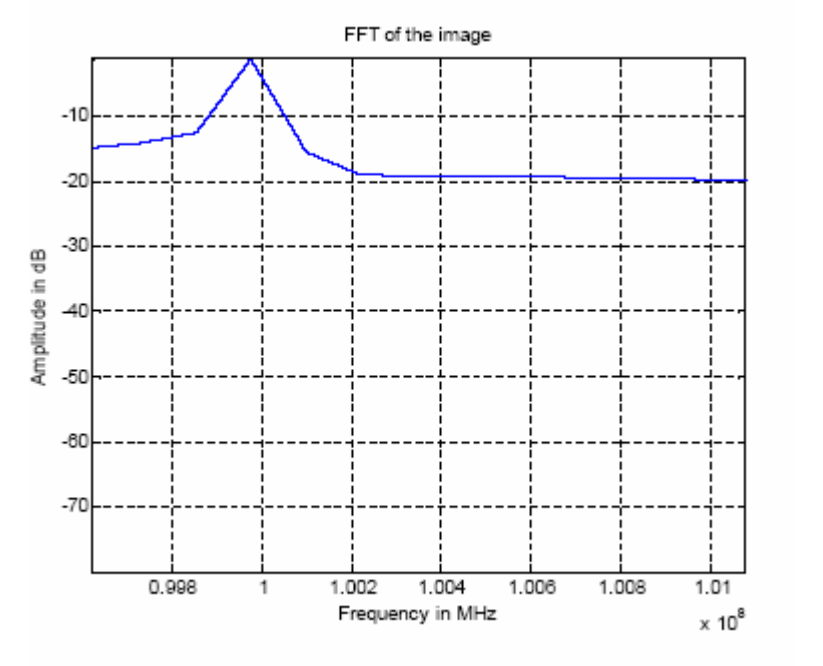

Figure 3.23: Content of image signal at 100 MHz after calibration

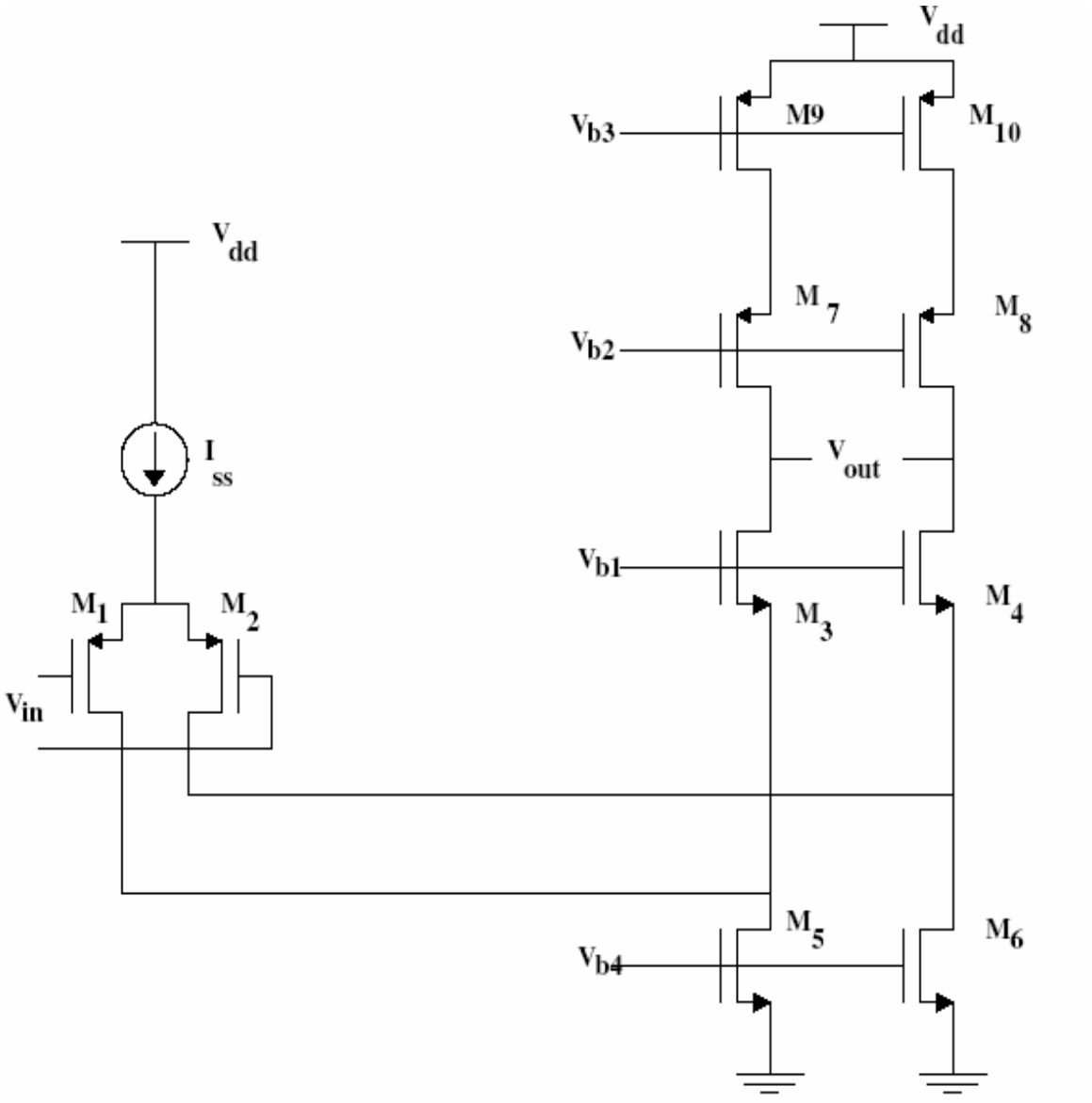

Figure 3.24: Folded cascade op-amp

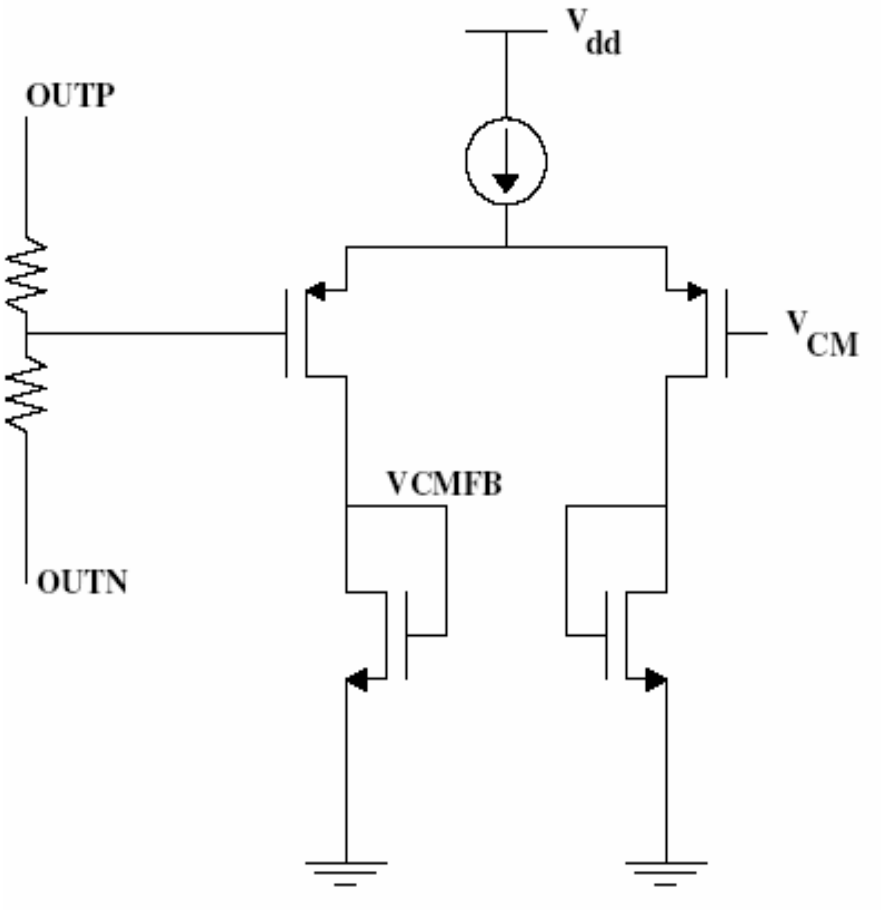

Figure 3.25: Common mode circuit for the op-amp

The phase shifter in this simulink model implemented as all pass filter. A variable Delay-Gain circuit [28, 37] can provide the same all pass function with gain changing capability. Hence it can be used for CMOS realization as shown in Figure 3.26. The output of the circuit is the superposition of two paths from input.

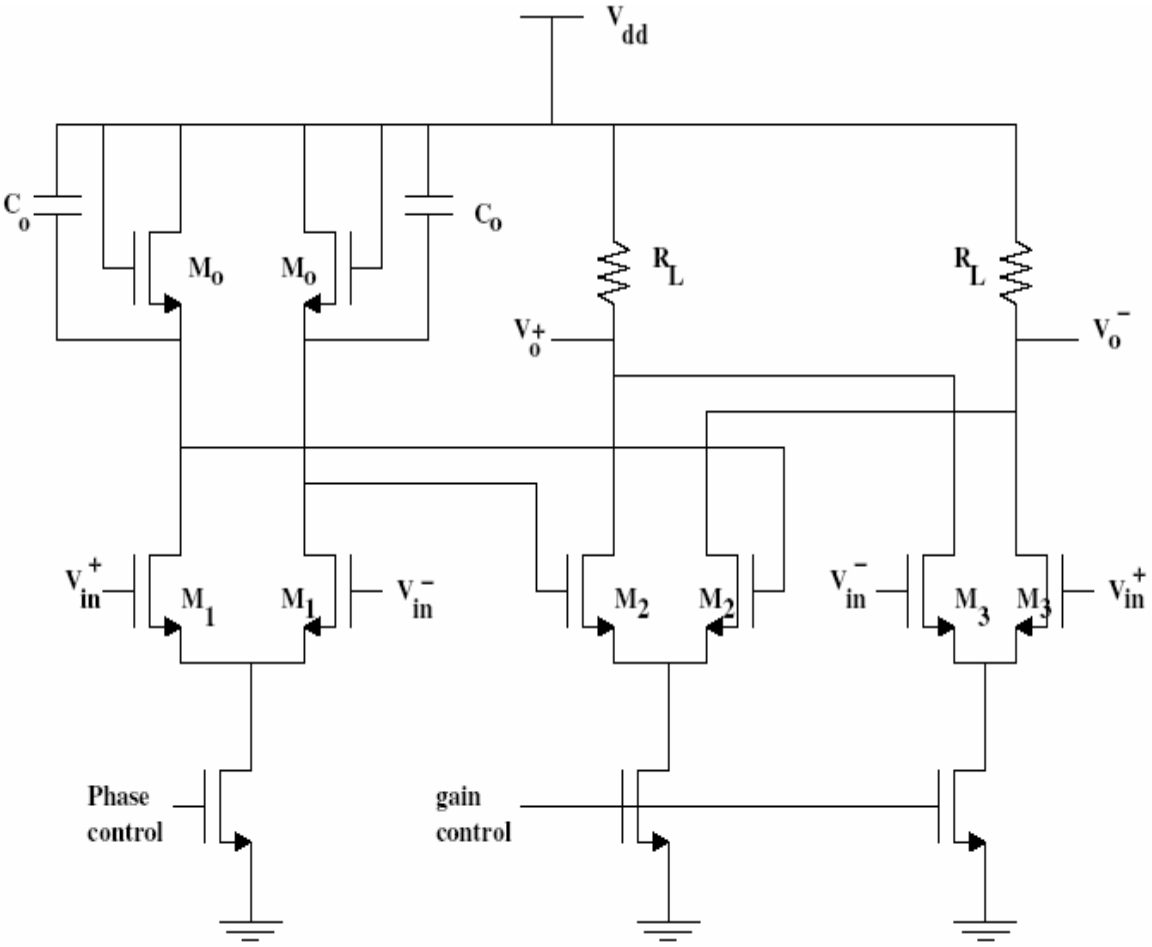

Figure 3.26: CMOS realization of all pass filter

Here two paths go through two different delay path. Signal that arrives from input pairM_1 faces more delay than signal from input pair M_3. Output voltage of M_1 input pair goes to gate of M_2 and serves as input for that transistor. It's output finally goes to the load. So we can write the following equations:

$$\left(g_{m1}V_{in}^{+}\frac{-1}{g_{mo}+SC_o}g_{m2}+g_{m3}V_{in}^{+}\right)(-R_L)=V_o^{-}$$
$$\left(g_{m1}V_{in}^{-}\frac{-1}{g_{mo}+SC_o}g_{m2}+g_{m3}V_{in}^{-}\right)(-R_L)=V_o^{+}$$
$$\Rightarrow\left[\frac{-g_{m1}g_{m2}}{SC_o+g_{mo}}+g_{m3}\right]\left(V_{in}^{+}-V_{in}^{-}\right)(-R_L)=\left(V_o^{-}-V_o^{+}\right) \tag{3.29}$$
$$\therefore\frac{V_{out}}{V_{in}}=\left[\frac{-g_{m1}g_{m2}}{g_{mo}+SC_o}+g_{m3}\right]R_L$$

Let $g_{m2} = g_{m3} = g_m$ and $g_{m1} = 2g_{mo}$, so we can write:

$$\frac{V_{out}}{V_{in}}=\left[\frac{-2g_{mo}}{g_{mo}+SC_o}+1\right]g_mR_L=\left[\frac{S-\frac{g_{mo}}{C_o}}{S+\frac{g_{mo}}{C_o}}\right]g_mR_L \tag{3.30}$$

The first part of the equation will be used for the phase by changing the value of g_{mo}, which essentially alter the pole, zero location due to the correction signal. The second part can be used for gain control, by varying $g_{m.}$ Hence phase and gain can be controlled independently. Simulation of this circuit with error correction is shown in figure 3.27. From the simulation we can see that this circuits create same amount of phase offset with reverse polarity. So once it is properly added with polarity to the respective LO signal, the image will be cancelled and IRR will be enhanced.

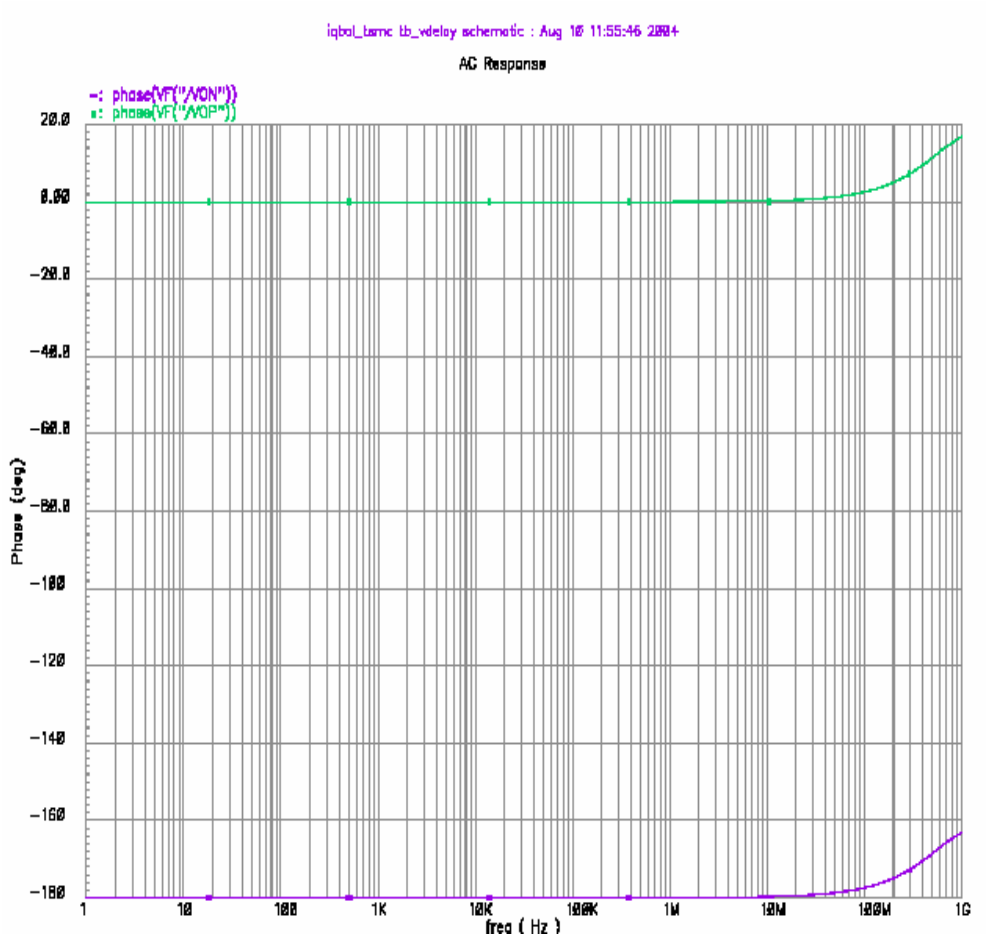

Figure 3.27: Differential phases by delay circuit

3.7 Matlab Code

```
% This is code to generate FFT from sample that was saved in workspace.
% x is the samples, obtain as x=x'; In simulink simulator parameter is set at 4095*2e-9
y=fft(x,4096);
yy=abs(y);
% Sampling frequency is 500MHz
f=500e6*(0:4095)/4096;
plot(f,20*log10(yy(1:4096)))
% This code is used to compare the simulink error generation with ideal error generation
%  for weaver receiver. Here it is  implementing the algorithm directly in matlab. It has
% been used as function
function[C_theta_noamp]=rr4(x)
% Normalized LO amplitude
A1     = 1;
A2     = 1;
% Amplitude error
delA1  = x(1);
delA2  = x(2);
% LO frequency
f1     = 1e9;
f2     = 200e6;
w1     = 2*pi*f1;
w2     = 2*pi*f2;
```

```
% Phase error
theta1 = x(3);
theta2 = x(4);
% Although in simulink it is given by a1, a1, a3, a4 directly, here we are only giving as
% input the gain and phase mismatches, so that it is more convenient to create mismatch
% version. Generating b1, b2 according to algorithm
b1     = 0.5*(A1*A1-0.25*delA1*delA1)*(sin(2*w1*t)+sin(theta1));
b2     = 0.5*(A2*A2-0.25*delA2*delA2)*(sin(2*w2*t)-sin(theta2));

% LPF with amplitude error. Here we are directly taking the DC term. In simulink it
% comes through a LPF with cut-off frequency of 72 MHz. This code was generated to
% verify error with simulink
lpf_b1_amp = 0.5*(A1*A1-0.25*delA1*delA1)*theta1;
lpf_b2_amp = -0.5*(A2*A2-0.25*delA2*delA2)*theta2;
% LPF after neglecting amplitude error
lpf_b1_noamp = 0.5*A1*A1*theta1;
lpf_b2_noamp = -0.5*A2*A2*theta2;

% Error signals without considering amplitude error
C_theta_noamp = A2*A2*lpf_b1_noamp-A1*A1*lpf_b2_noamp;
% Error signals considering amplitude error
C_theta_amp = A2*A2*lpf_b1_amp-A1*A1*lpf_b2_amp;
```

CHAPTER 4

VARIABLE GAIN AMPLIFIER

4.1 Introduction

Variable gain amplifier (VGA) is one of the important block in the baseband circuit of the receiver. It is used for adjusting the received signal amplitude. By adjusting the signal level between different baseband blocks, VGA improves the noise figure of receiver and relaxes the dynamic range of the ADC (Analog-to-Digital Converter). It is critical for VGA to maintain it's linearity over the entire signal band width as well as gain range. High-speed VGA's [39, 41, 42] have been realized using variable MOS transconductance in disk-drive applications. The linearity is limited by the transconductance, and given realization schemes are required to obtain wide input range. Using degenerated source coupled pair with transconductance enhancement can improve linearity. However open loop nature of the above circuit makes the linearity of the circuit depend heavily on inherent linearity of input stage, although closed loop architecture can achieve high

linearity. Previous designs involved trade-off among gain range, bandwidth, linearity and power dissipations.

In general two types of VGA are available. One is discrete gain-step type with digital control and other is a continuously variable gain type which is controlled by an analog gain-control gain. Depending on the specification one can choose the required topology. For example, WCDMA system, continuous type VGA is preferred because it can avoid the signal phase discontinuity. In addition accurate transmission power control & accurate received signal strength measurement are required to optimize system capacity.

Also architecture topology affects the VGA choice. For example VGA for GSM standard must satisfy the high linearity requirement. This limits the variable gain realization to linear poly-poly or metal capacitors & poly resistors. In addition, having the amplifier in feedback topology also improves the linearity of the VGA. In this chapter we will discuss about two type of VGA in order to achieve low noise and high bandwidth. One is current sensed VGA and the other is tansconductance amplifier (high gain) based VGA.

4.2 Current sensed VGA

One simple way to implement a VGA is to use a source degenerated differential amplifier as shown in fig 4.1. This gives good noise performance but it is not used because dc voltage drop across R_1 limits the output swing. Instead the following topology is used as in fig 4.2. This circuit relies on converting input voltage to a current using linear resistor "R_1". The current is then allowed to flow through resistor R_2. Using the half circuit concept of fully differential amplifier we can draw the circuit as drawn in fig 4.3. The low frequency differential gain can be written as:

$|V_{od}/V_{id}|$ = Resistance seen in drain/Total resistance seen in source path

So, gain

$$|A_v| = \frac{R_2}{R_1 + \frac{1}{g_m}} \tag{4.1}$$

The 3-dB bandwidth of such circuit can be approximated by the dominant pole, which can be written as :

$$\omega_{3-dB} \approx \frac{1}{R_2 C_2} \tag{4.2}$$

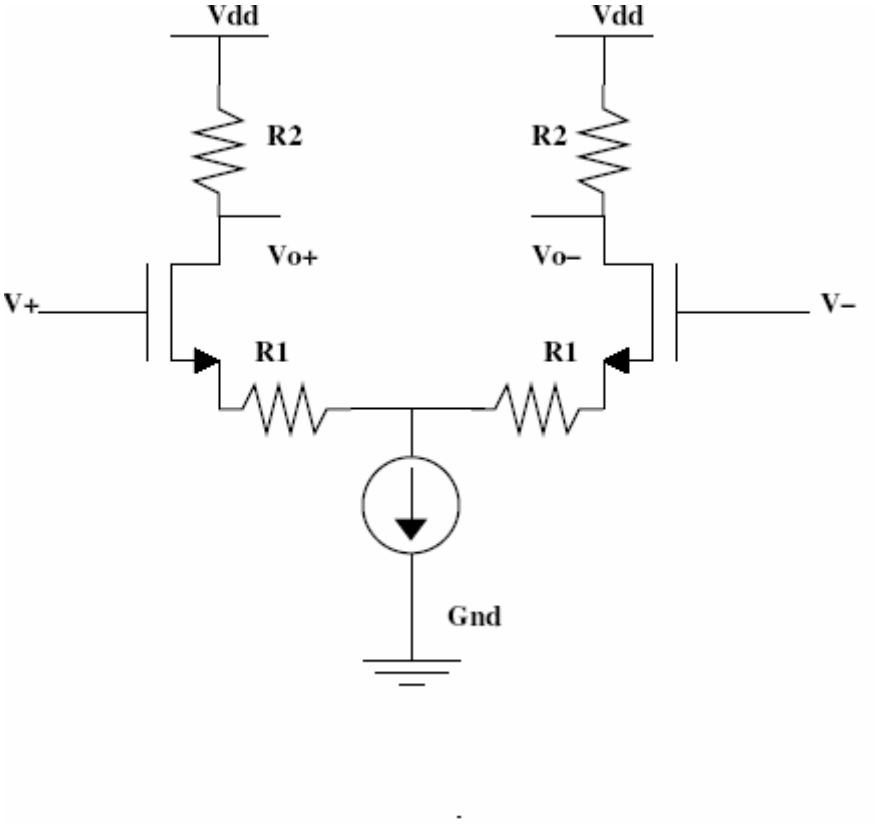

Figure 4.1: Simple Differential Amplifier

Now we can see that gain can be changed by changing only R_1 and it also does not hurt the bandwidth of the circuit. But this simple circuit has some major issues. The gain equation contain the term g_m which depends on mobility, drain current and aspect ratio of devices. So this is a process, temperature dependent term. Hence gain cannot be controlled accurately. Also it cannot achieve high gain and linearity due to the finite g_m. It also suffers from the body effect which makes the g_m effect worse in the denominator

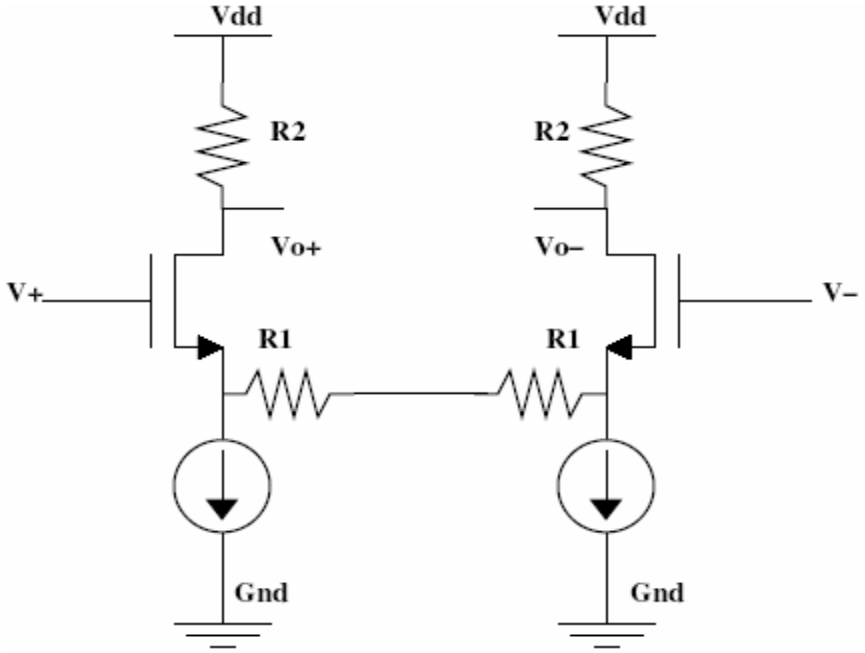

Figure 4.2: Modified Differential Amplifier

of the gain equation. It's output swing is also limited by the supply, so gain range is limited as well. Noise performance is not also satisfactory. In order to achieve high gain and well noise performance R_1 must be small. Also finite g_m problem will be eliminated if transistors with high g_m can be used. So the circuit needs to modify by the following way. Figure 4.4 presents a gain boosting circuit. The output impedance of such circuit can be calculated as follows.

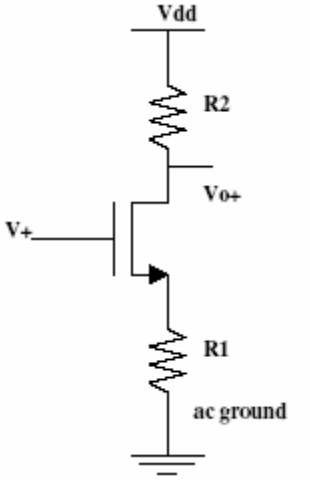

Figure 4.3: Half circuit of modified differential pair

$$R_{out} = \frac{\Delta V}{\Delta I} \tag{4.3}$$

$$\begin{aligned} \Delta V_s &= \Delta I \bullet R_s \\ \Delta V_g &= A(0 - \Delta V_s) = -AR_s \bullet \Delta I \end{aligned} \tag{4.4}$$

$$\Delta I_m = g_m(\Delta V_g - \Delta V_s) = g_m(-AR_s \bullet \Delta I - \Delta I R_s) = -g_m(A+1)\Delta I \bullet R_s \tag{4.5}$$

$$\Delta I_{r_{01}} = \frac{\Delta V - \Delta V_s}{r_{01}} = \frac{\Delta V - \Delta I \bullet R_s}{r_{01}} \tag{4.6}$$

$$\Delta I = \Delta I_M + \Delta I_{r_{01}} = -(1+A)g_m R_s \bullet \Delta I + \frac{\Delta V - \Delta I R_s}{r_{01}} \tag{4.7}$$

$$\frac{\Delta V}{r_{01}} = \Delta I\left\{1+(1+A)g_m R_s + \frac{R_s}{R_{01}}\right\} \Rightarrow \frac{\Delta V}{\Delta I} = r_{01}\left\{1+(1+A)g_m R_s + \frac{R_s}{r_{01}}\right\} \tag{4.8}$$

$$\therefore \frac{\Delta V}{\Delta I} \approx A g_m R_s r_{01}$$

This increased output impedance when multiplied by g_m enhances the gain of such circuits. The following analysis reveals how g_m effect can be reduced using the above topology for a VGA circuit. If we can employ an ideal op-amp (infinity gain) in the gain

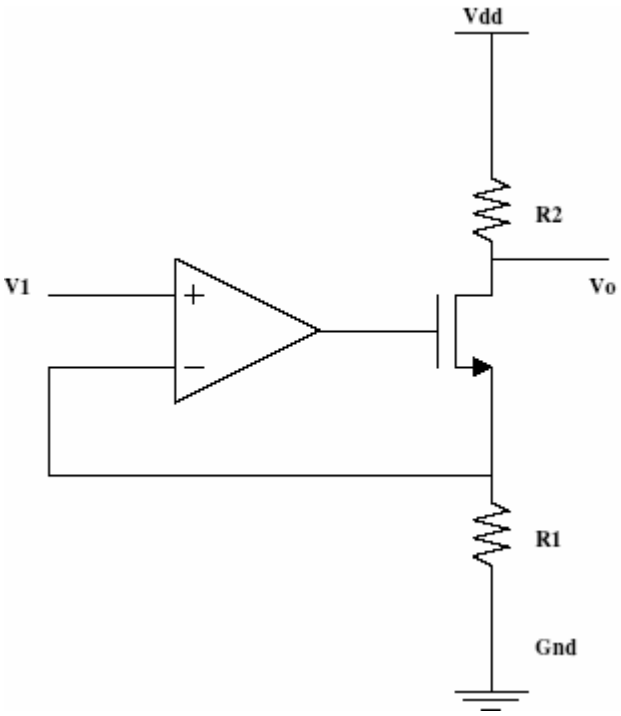

Figure 4.4: Gain boosting amplifier

boosting circuit, then from figure we can tell that voltage V^+ will appear across R_1. Similarly voltage V^- will also appear at the symmetrical differential side. Now the same current that follows through source will go through drain. It will eventually pass through the load resistor R_2. Now the gain equation can be written as:

$$\left|A_v\right| = \left|\frac{V_{out}}{V_{in}}\right| = \frac{R_2}{R_1} \tag{4.9}$$

Clearly g_m effect has been eliminated. But ideal op-amp is not possible in reality. The following analysis will show when there exists a finite gain A, we also can reduce the g_m Effect from the circuit. Let the small signal current is ΔI and ignoring r_{01} we can write,

$$\begin{aligned}
&\Delta V_s = \Delta I R_1 \\
&\Delta V_g = (V_{in} - \Delta I R_1)A \\
&\Delta I = g_m(\Delta V_g - \Delta V_s) = \{(V_{in} - \Delta I R_1)A - R_1 \Delta I\} g_m = g_m(AV_{in} - (1+A)R_1 \Delta I) \\
&\Rightarrow (1 + (1+A)R_1 g_m)\Delta I = g_m A V_{in}
\end{aligned} \tag{4.10}$$

$$\begin{aligned}
&\Rightarrow \frac{V_{out}}{R_2}(1 + (1+A)g_m R_1) = -g_m A V_{in} \\
&\Rightarrow \frac{V_{out}}{V_{in}} = -\frac{R_2 A g_m}{(1 + (1+A)g_m R_1)} \\
&\therefore \left|A_v\right| \approx \frac{R_2 A g_m}{A g_m R_1} = \frac{R_2}{R_1}
\end{aligned} \tag{4.11}$$

Now we can see using the above topology body effect has been eliminated and a good linearity is also attained. But still it suffers from two potential problems. Here signal swing is limited by the supply voltage (V_{dd}). Also any disturbance (noise) in power

supply directly couple to output through R_2. So power supply rejection ratio (PSRR) for the single ended version of the above topology is bad. Of course PSRR of differential version is much better. But it is severely limited by the matching of resistors R_2. A small mismatch will make PSRR much worse.

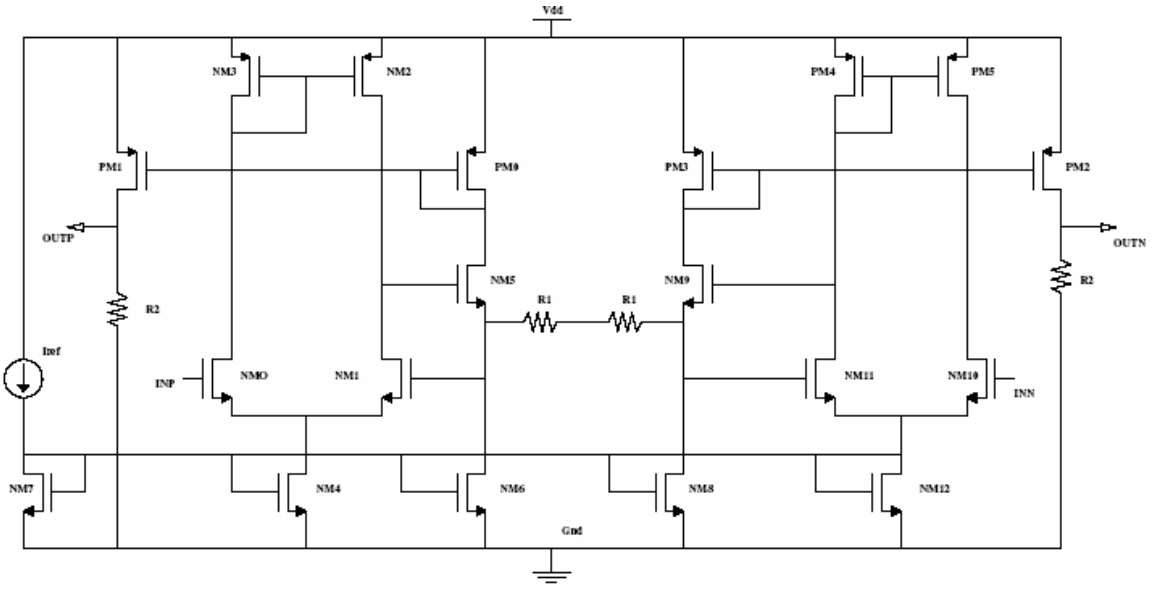

Figure 4.5: Current sensed mirror based vga

In order to avoid the swing problem and increase the range of the gain we can use a current mirror which will sense the output current, mirror replica of that current and pass it through load resistor R_2. Figure 4.5 illustrates this architecture with considering load capacitance as well. There is a trade off between noise and speed with this structure. Noise part will be discussed in details later. Here current mirror is in the signal path. Since bandwidth of this circuit is high, it put limitation on device dimensions. So length

(L) & width (W) are kept small, so that capacitance introduced by the mirror is small. Now if L is increased g_m is decreased capacitance will increase and eventually bandwidth will decrease. Also if W is increased capacitance will increased, circuit will be slow. So there is no way we can make W & L large simultaneously. Here mirror matching is critical in order to avoid offset problem. Ideally offset is kept as low as possible. Again from Pelgrom [44, 45] matching is inversely proportional to the product of W and L. Since both are small, so very bad matching and offset problem is likely to happen in this topology. That's why we need large W & L simultaneously. Before refer to the noise problem of this circuit, the noise sources and different types of noises is discussed.

4.2.1 Noise

Noise is introduced primarily by resistors and transistors. There are two important types of noise that dominates noise contribution of a circuit. One of them is thermal noise by resistors. The random motion of electrons in a conductor introduces fluctuations in the voltage measured across the conductor even if the average current is zero. Thus spectrum of thermal noise is proportional to the absolute temperature. The thermal noise of a resistor R can be modeled by a series voltage source, with the one sided spectral density,

$S_v(f) = 4KTR$, f>0.

Here K=1.38e^{-23} J/K is the boltzmann's constant. Unit of $S_v(f)$ is expressed in V^2/Hz. The average noise voltage is equal to 4KTR. For our convenience we take the rms value of the noise, so unit becomes $V/\sqrt{Hz}$. The noise equation for resistors suggests that the

thermal noise is white. In reality, $S_v(f)$ is flat up to roughly 100THz, dropping at higher frequencies. MOS transistors also exhibit thermal noise. The most significant source is the noise generated in the channel. It can be proved [3] that for long channel MOS devices operating in saturation, the channel noise can be modeled by a current source connected between the drain and source terminals.

The coefficient γ is derived to be equal to 2/3 for long channel transistors and may need to be replaced by a larger value for submicron, MOSFET. The ohmic sections of a MOSFET also contribute thermal noise. But it is negligible compare to the channel noise and hence we will neglect it. There is also another type of noise which dominates at low frequency, called flicker noise. The interface between gate oxide and the silicon substrate in a MOSFET entails an interesting property. Since the silicon crystal reaches an end at this surface, many "dangling" bonds appear, giving rise to extra energy states. As charge carriers move at the interface, some are randomly trapped and later released by such energy states, introducing "flicker" noise in the drain current. In addition to trapping, several other mechanisms are believed to generate flicker noise. Unlike thermal noise, the average power of flicker noise cannot be predicted easily. Depending on the "cleanness" Of the oxide-silicon interface, flicker noise may assume considerably different values and as such varies from one CMOS technology to another. The flicker noise is more easily modeled as a voltage source in series with gate & roughly given as:

$$\overline{V_n}^2 = \frac{K}{C_{ox}WL} \bullet \frac{1}{f} \tag{4.12}$$

Where K is a process dependent constant on the order of 10^{-25} V^2F. The trap and release phenomenon associated with dangling bonds occur at low frequencies more often. For this reason flicker noise is also called 1/f noise. The inverse dependence on WL suggests that to decrease 1/f noise, device sizes must be increased. It is also believed that PMOS device exhibit less 1/f noise than NMOS transistors, because the former carry holes in a "buried channel" i.e., at some distance from the oxide silicon interface. In order to quantify the significance of 1/f noise with respect to thermal noise for a given device, we plot both spectral densities on the same axis, called the 1/f noise " corner frequency", the intersection point serves as a measure of what part of the band is mostly corrupted by flicker noise, f_c generally depends on device dimensions and bias current. Nonetheless, since for a given L, the dependence is relatively weak, 1/f noise corner is relatively constant, falling in the vicinity of 500 KHz to 1 MHz for submicron transistors. Now it will be convenient to talk about the noise in the mirror VGA. Due to the bad matching V_t can be different for transistors. It produces extra noise. Mirror signal also introduce noise. In order to avoid these extra noise, L has to be large, which in turn tells us to avoid mirror topology. So the conclusion is we do not want mirror in signal path. Also other requirements are to reduce noise and increase L.

4.2.2 Folded Cascode Topology

The following topology can take care of the issues suffered from mirror VGA circuits. A folded cascode VGA topology enhance the VGA performance. So instead of mirror, we

will use a folded cascode circuit and eventually pass the current through load resistor R_2. First improvement that we notice is that any disturbances in V_{dd} do not affect the drain of the PMOS current source. Since, the gain from source to gate is 1. So any disturbances occur is absorbed by the gate to keep the current constant through the current source. So much better PSRR can be achieved. Another important advantage is PMOS current source is not in the signal path. So capacitance associated with it will not affect the speed of the circuit. Now L & W can be changed simultaneously. This means good matching. L of transistors are big, so less noise. Swing is not limited by supply, extended gain range is

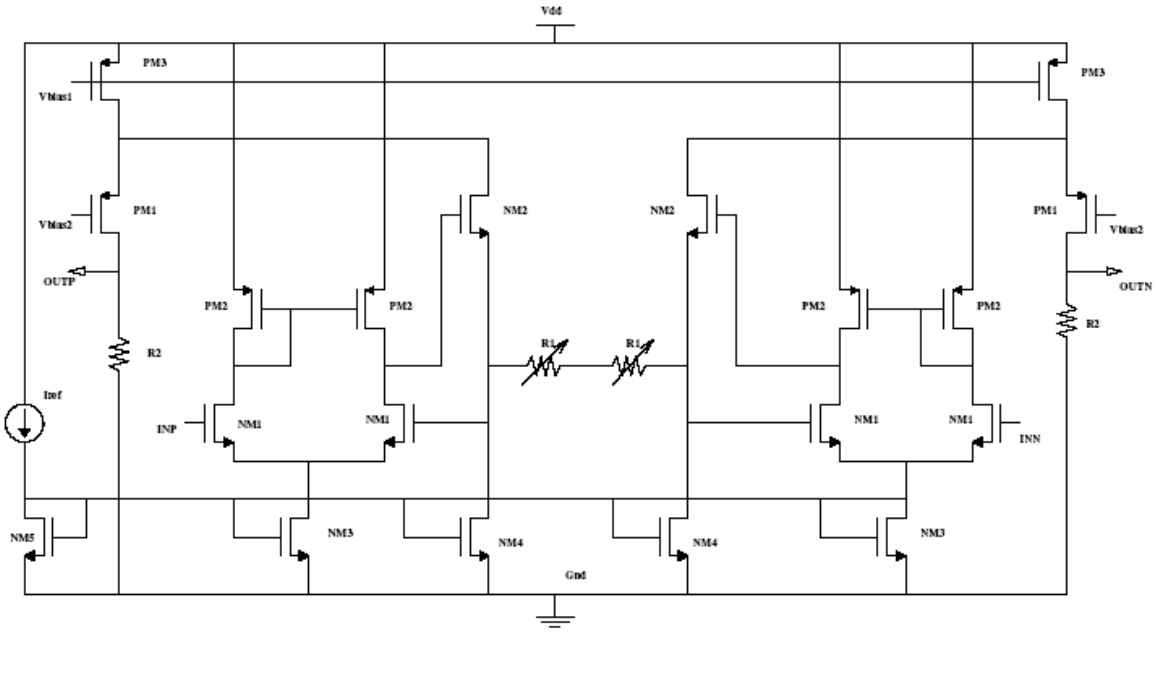

Figure 4.6: Current sensed VGA with folded cascode topology

observed. No current mirror matching is required for linearity. But here current source also introduce some noise.

Here input transistors, amplifier load transistors, current source and transistor are believed to be contributing most of the noises. Here flicker noise will be the dominating factor. Since most of the noise are flicker noise, input referred noise can be further reduced by changing NMOS by PMOS, since flicker noise for PMOS is small. But this will make some problem with stability, so additional arrangement for compensation circuit is necessary.

4.3 Simulation Results

VGA's have been simulated in cadence using TSMC .18μ technology. Available gain range is from –13 dB to 23 dB, a total of 36 dB range. It Frequency response for this VGA is shown in fig 4.7. From the figure we can see that available 3-dB bandwidth is more than 100 MHz .

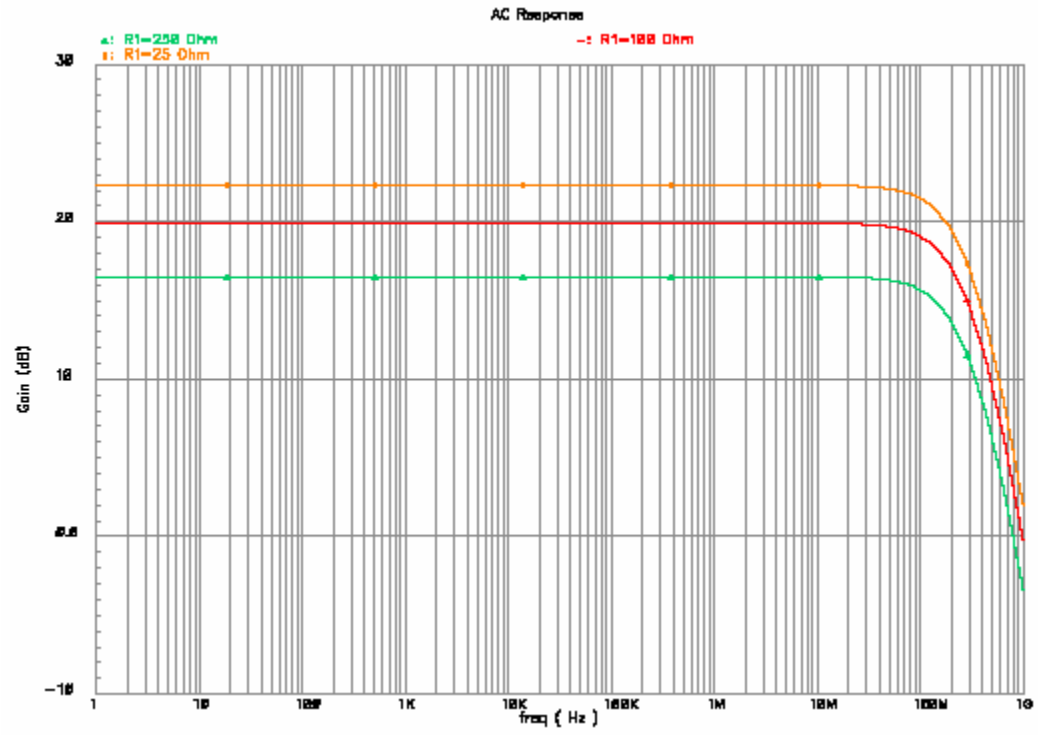

Figure 4.7 Frequency response of current sensed VGA

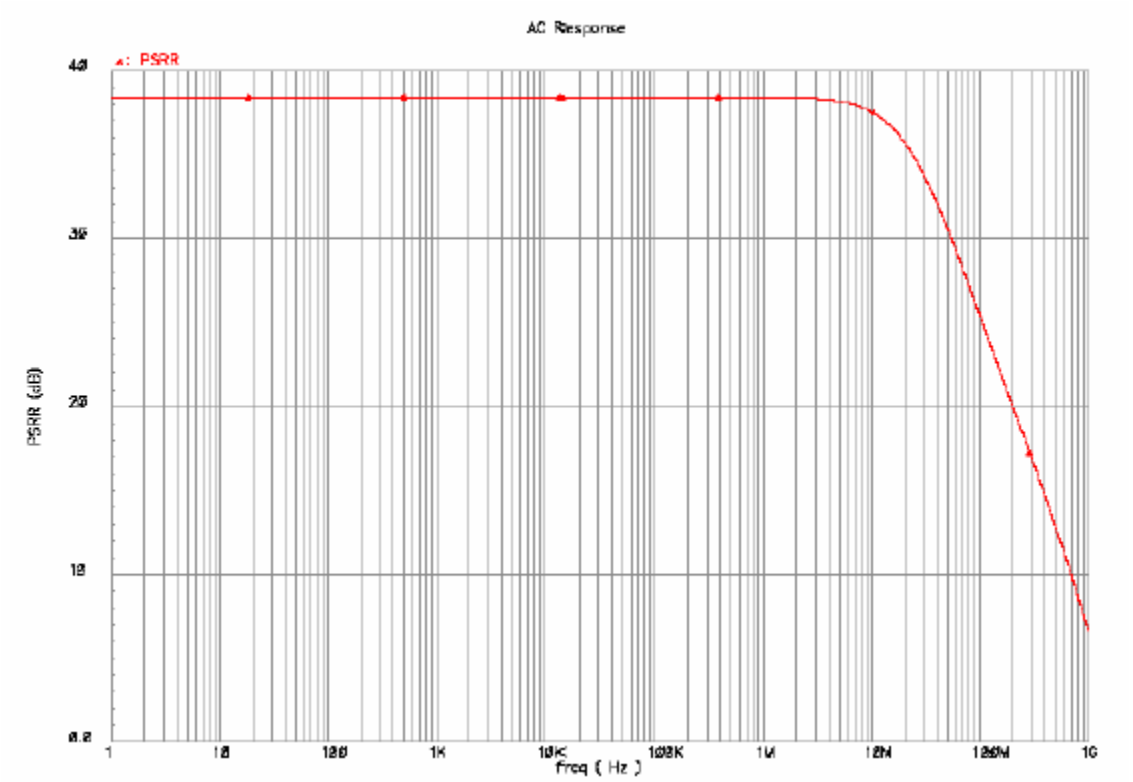

Figure 4.8: PSRR of the VGA with mirror topology

The noise performance of the VGA is shown in fig 4.9. Integrated input referred noise 8.5nV/√Hz. Noise is 110nV/√Hz at 100KHz. As mentioned earlier that for mirror topology there has always been a trade off between noise, bandwidth and speed. Noise is quite high at low frequency. From simulations we can say that most of the noise contribution is due to flicker noise that dominates the low frequency. Transistors NM1, NM11, NM0, NM10 contribute most of these noises. For wireless standard like GSM noise requirement is very strict at low frequency. So mirror type VGA will not serve the purpose for GSM. On the other hand, using folded cascode topology similar kind of gain

range is achieved. The input referred noise at low frequency (100 KHz) is 9nV/√Hz, shown in Figure 4.10. Proper device optimization will yield upto 6nV/√Hz. PSRR for current sensed VGA is shown in fig. 4.8. It is not very high, since low frequency gain is not that high.

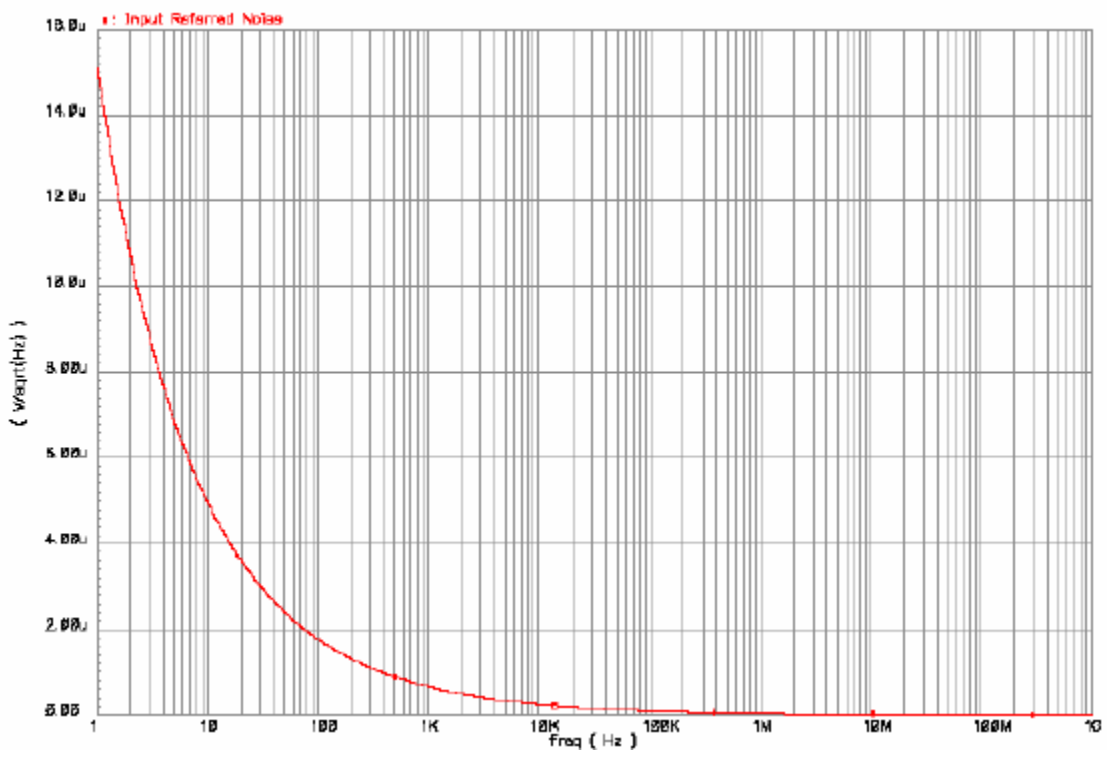

Figure 4.9: Noise simulation for VGA

Figure 4.11 presents THD simulation for current sensed VGA. From then figure it can be shown that 3rd harmonic distortion is for a signal of $1V_{pp}$ @ 1MHz is <-70dB. Total THD is <-57 dB. Folded cascode topology trade off noise with bandwidth, so noise can be

reduced at cost of bandwidth. But for GSM noise is at low frequency is the main issue since channel bandwidth is not high. Hence this architecture works well for GSM.

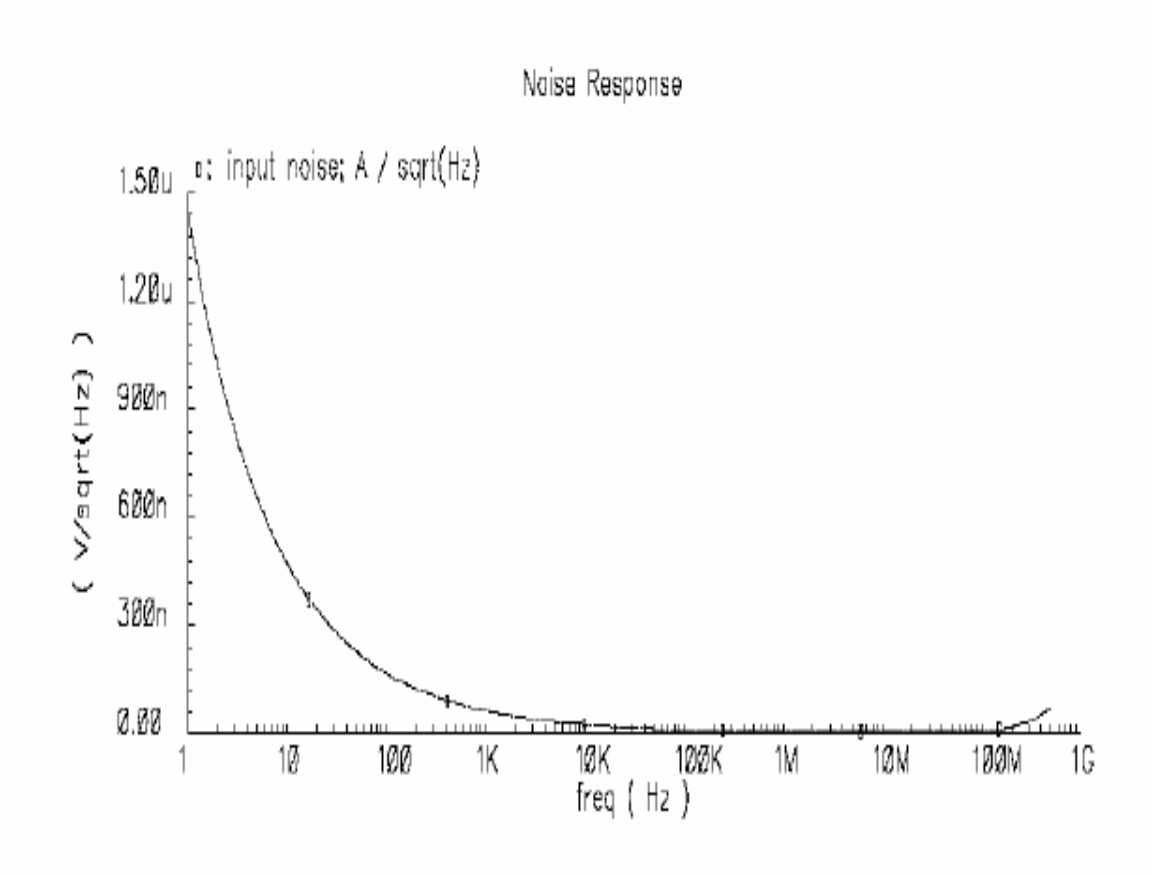

Figure 4.10: Noise simulation for folded cascade topology

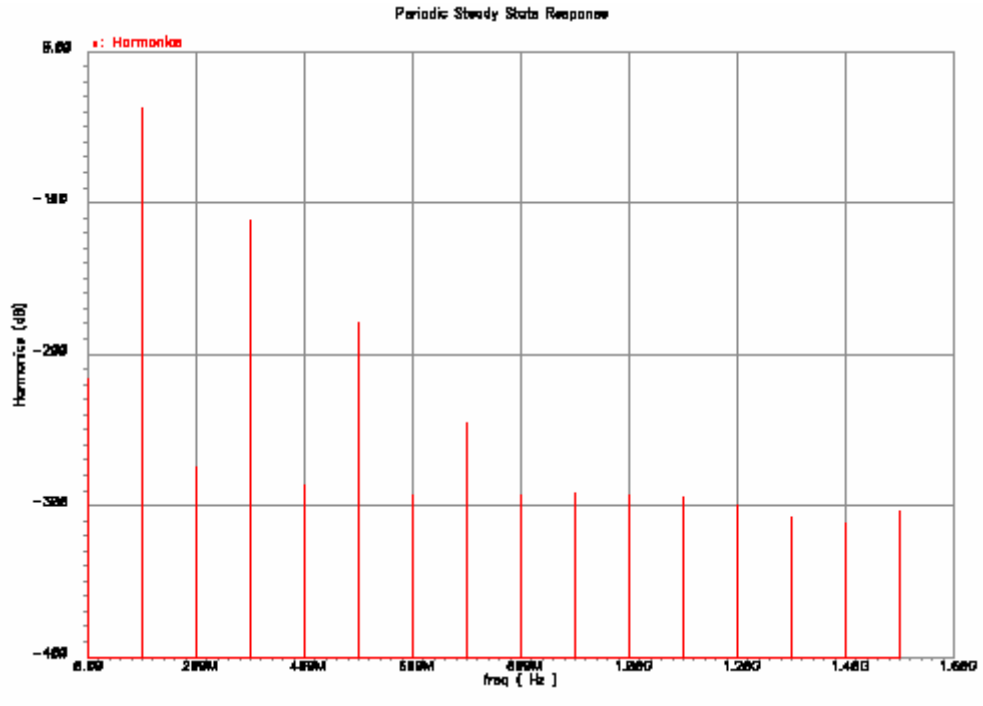

Figure 4.11 THD simulation for current sensed VGA

4.4 Transconductance based amplifier

In some applications we need moderate noise and very high bandwidth in the range of several MHz to few GHz. For such applications different VGA topology will be introduced. A voltage amplifier using negative feedback with a high transconductance gain amplifier can be implemented as shown in fig 4.12.

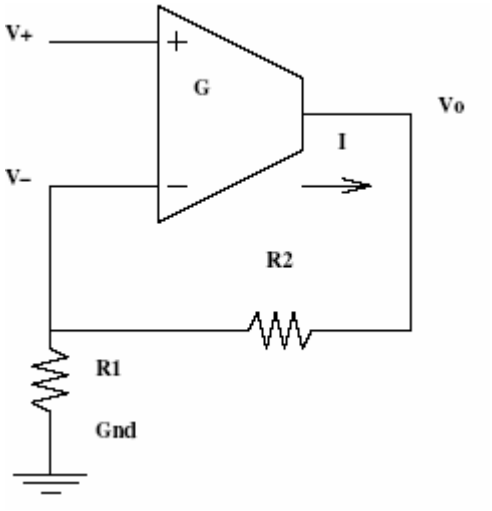

Figure 4.12 Basic G_m based amplifier

$$I = G(V_+ - V_-), \qquad G \to \infty \tag{4.13}$$

This is different from finite g_m based amplifier. In this mode G can be nonlinear. The linearity can be kept high by increasing G (ideally infinity). The following equation leads us the gain for such amplifier.

$$V_o = \left(V_{in} - \frac{V_o R_1}{R_1 + R_2} \right) G(R_2 + R_1) \tag{4.14}$$

$$V_o(1 + GR_1) = G(R_1 + R_2)V_i \tag{4.15}$$

$$A_v = \frac{1 + \dfrac{R_2}{R_1}}{1 + \dfrac{1}{GR_1}} \approx 1 + \frac{R_2}{R_1} \tag{4.16}$$

Loop gain can be written as GR_1 much greater than 1. Here the advantage is we can alter gain (A_v) by changing only R_2. Loop gain is fixed by GR_1. The bandwidth is fixed as well. The trade off for this topology is linearity vs noise. For example if R_1 is increased, high loop gain is expected that translates to better linearity but more noise. The fully differential version can be shown as:

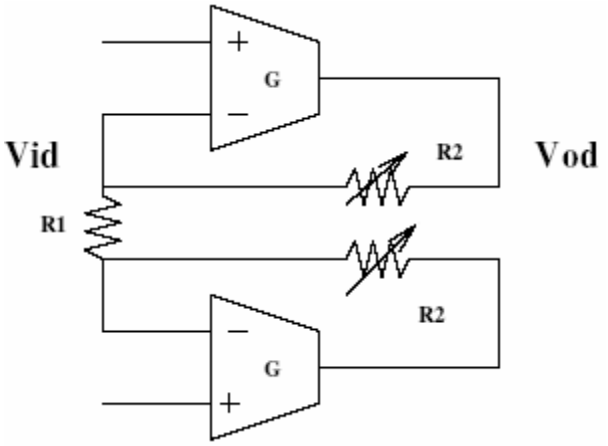

Figure 4.13 Fully Differential version of figure 4.12.

The CMOS realization for the circuit can be described below. Because of the limited g_m of MOS transistors a regular differential pair with g_m boosting can be used to realize G. The following circuit describes the g_m boosting technique. The small signal current through all branches are shown in the Figure 4.15.

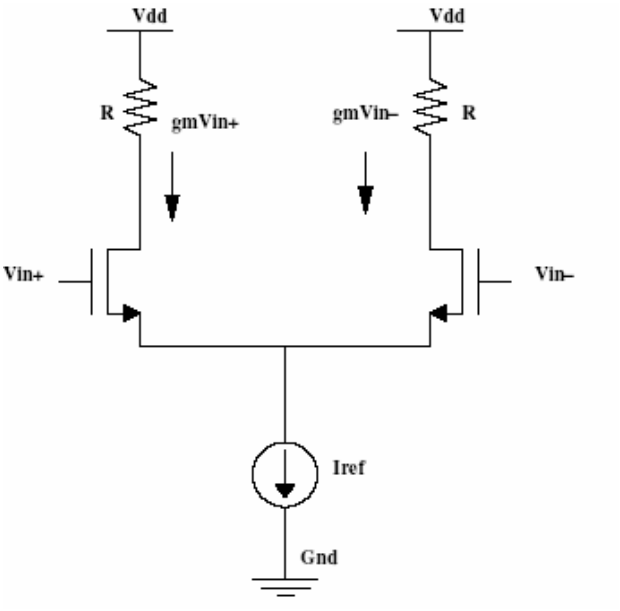

Figure 4.14 G_m of regular differential pair

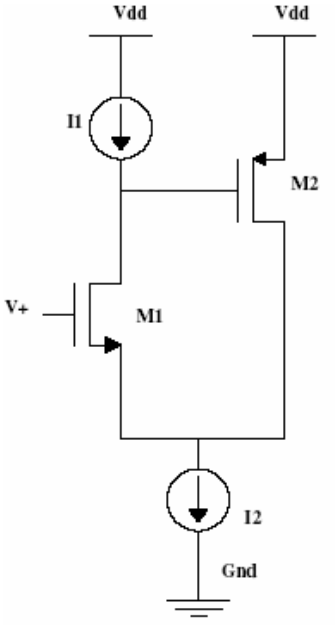

Figure 4.15 G_m Boosting Topology

If we sum the total current at the node b, then $G_{boosted}$ can be given by the ratio of I_{out}/V_{in}, which is equal to $g_m(1+A)$, where A is the gain by the PMOS device. We can get very high G_m (ideally infinity) by this technique. We can also get quite high g_m by using a simple modification of the circuit [40, 43] as shown in fig 4.16 .

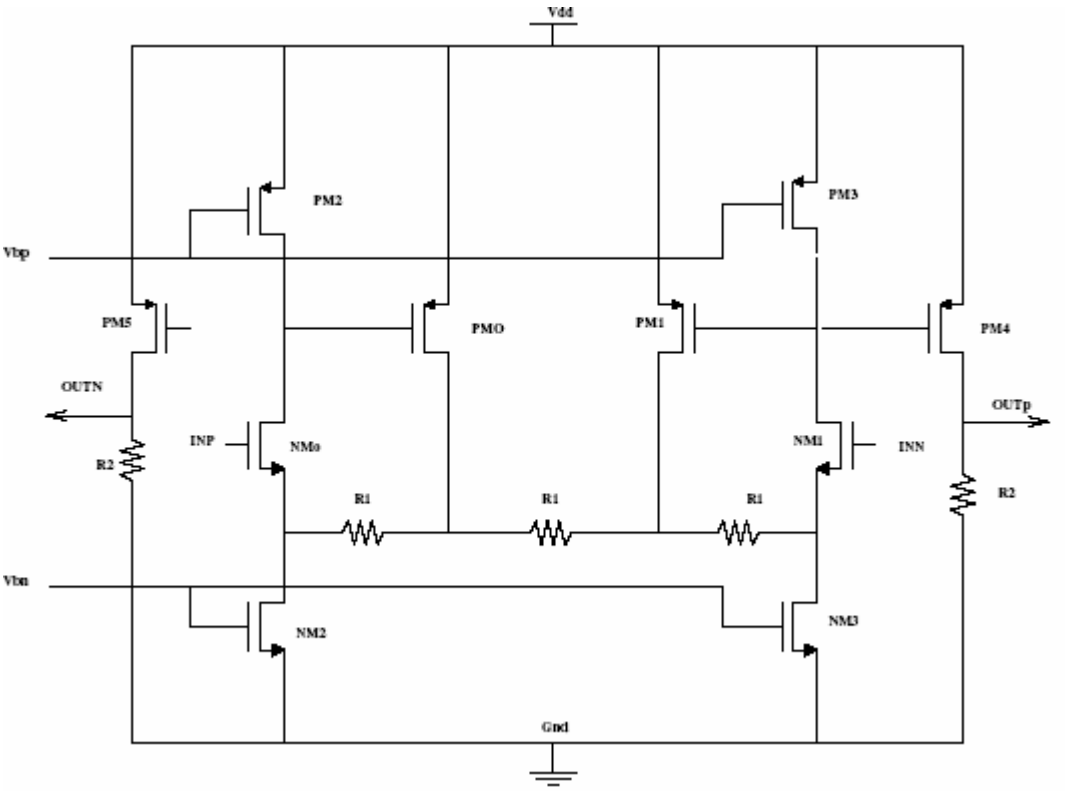

Figure 4.16: Modified version of G_m boosting circuit

Here two PMOS transistor acts as gain stages. As a result these input devices ideally act as a dc level shifters, creating a linear voltage copy of the input signals. The PMOS

transistor conduct a dc current plus the ac signal current. Considering the finite open loop gain A for the amplifier we can write the VI conversion as:

$$i_{ac} = \frac{V_{in}}{R_{\deg en} + \frac{2}{g_m(1+A)}} \bullet \frac{A_o}{(1+A_o)} \tag{4.17}$$

Here also g_m has been boosted by $g_m(1+A)$.

4.5 Simulation Results

Simulation for this VGA has also been done with TSMC .18μ technology. The gain range is 16dB. The frequency response is shown in fig 4.17 . The 3-dB bandwidth is more than .5 GHz. The input referred noise is given by the following figure 4.18. Input referred noise is 7nV/√Hz . Input referred noise at 100KHz is 61nV/ √Hz . From the simulation result we can tell that transistors NM3 and NM2 are contributing most of these noises. Flicker noise also dominates in this case. Better noise performance can be achieved by the following circuit of figure 4.20. Here optimized value of W & L can make noise as low as 14 nv√Hz and current source noise has been eliminated. THD simulation is shown in fig. 4.19. The third harmonic distortion for single ended input of $1V_{pp}$ @ 1KHz is less than -110 dB. THD available is less than -95 dB.

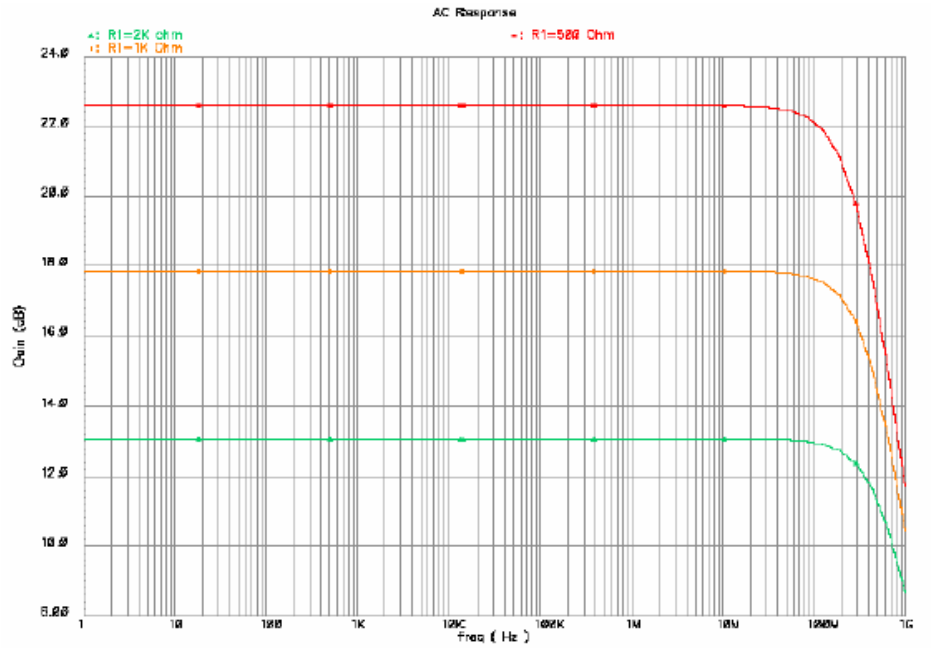

Figure 4.17 Frequency response of G_m based VGA

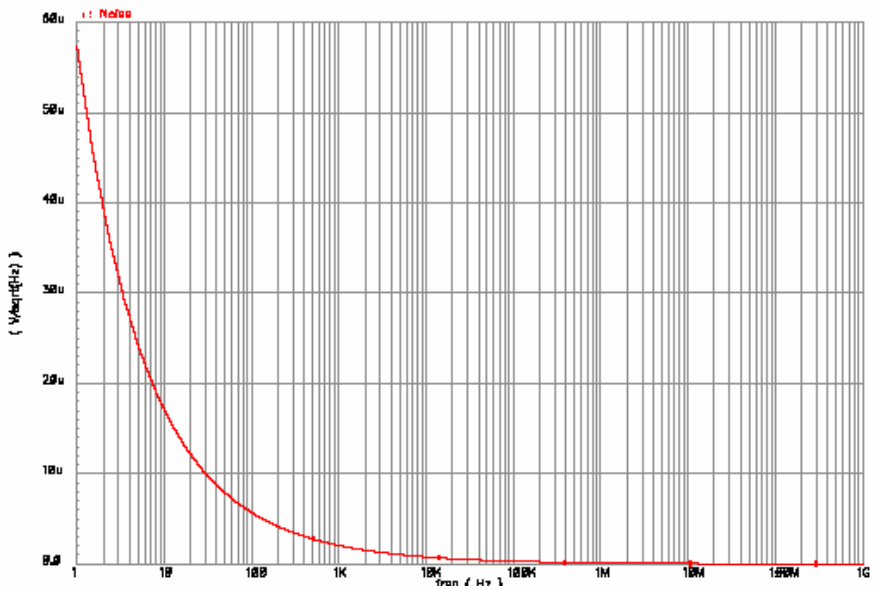

Figure 4.18 Noise simulation of G_m based VGA

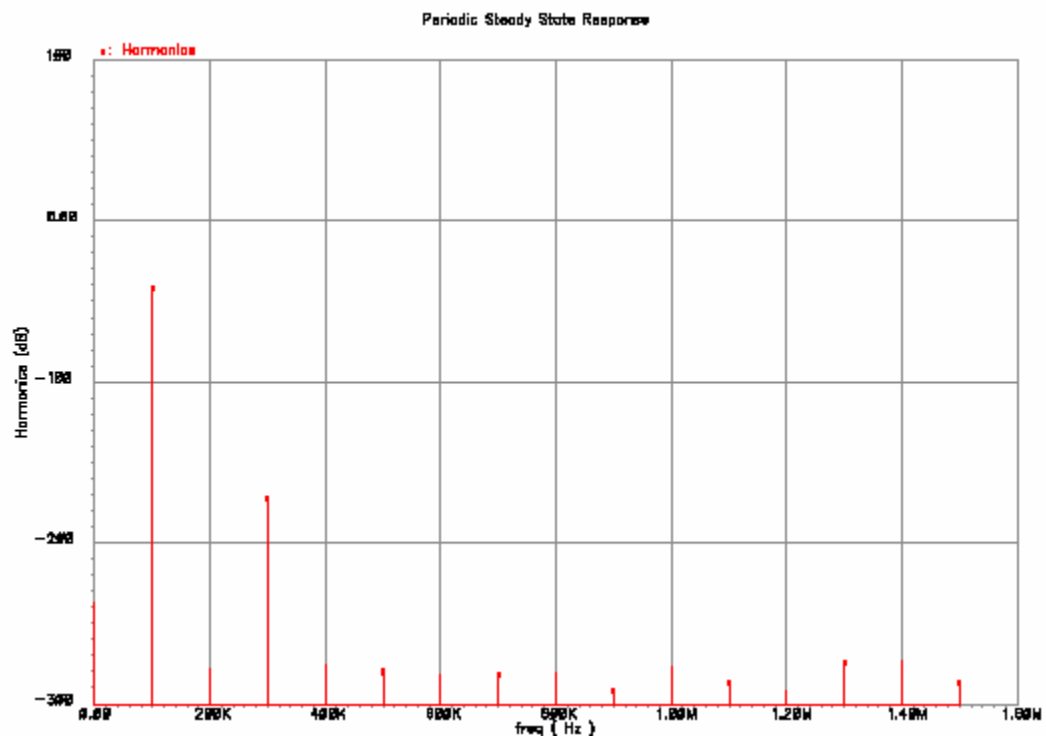

Figure 4.19 THD simulation for G_m based VGA

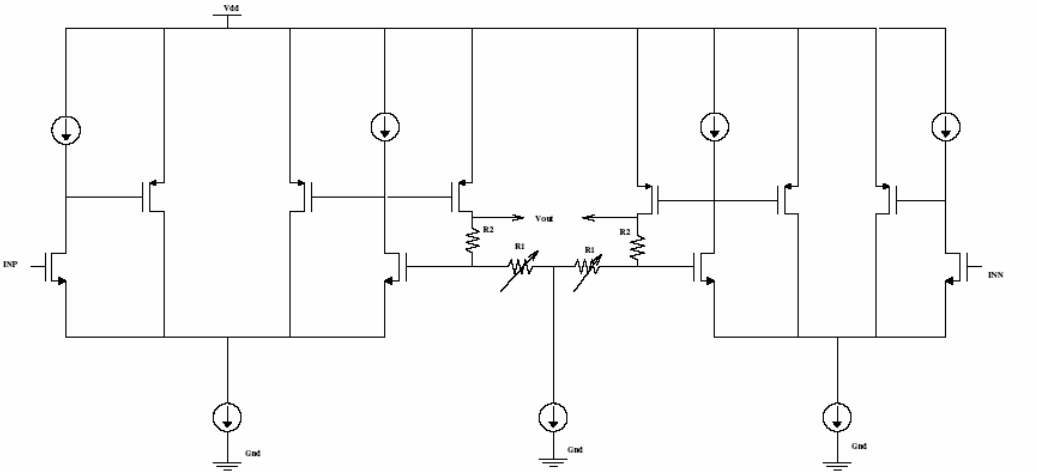

Figure 4.20: Low noise version of G_m based VGA

CHAPTER 5

LOW VOLTAGE BUFFER

5.1 Introduction

In integrated receiver channel filtering is provided in baseband in order to remove adjacent blockers. These filters are required to be highly linear. Unity gain buffers can be used to realize highly linear filter. A unity gain buffer is an important analog building block that is used in many applications [47, 48, 49]. Buffer circuits are used to buffer voltage between different circuit blocks. These circuits are also used in realizing switched capacitor data converters, gain stages and in many current mode building blocks. Buffer circuits are required to exhibit both accurate voltage tracking and low output impedance. Other requirements are low power dissipation and a large dynamic range. In this chapter, we review [46] a novel low voltage CMOS buffer circuit that provides low output impedance, low input referred noise, and high bandwidth using a class AB negative feedback loop. This low voltage buffer has been used to implement a 6^{th} order prefilter for WCDMA application. Filter design are discussed in subsequent sections of this chapter.

5.2 Class AB CMOS buffer realization

The class AB buffer [46] circuit is shown in Figure 5.1. The circuit utilizes a class AB loop to boost the transconductance of a MOS transistor operating in the saturation region. Hence, low output impedance can be achieved with low standby power consumption. The

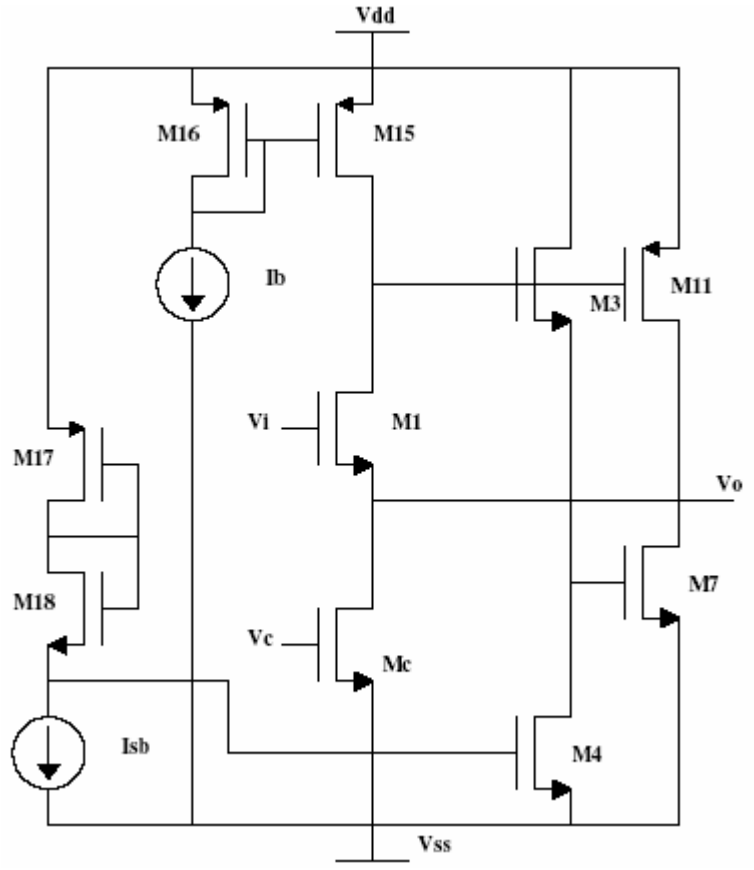

Figure 5.1: Class AB basic circuit

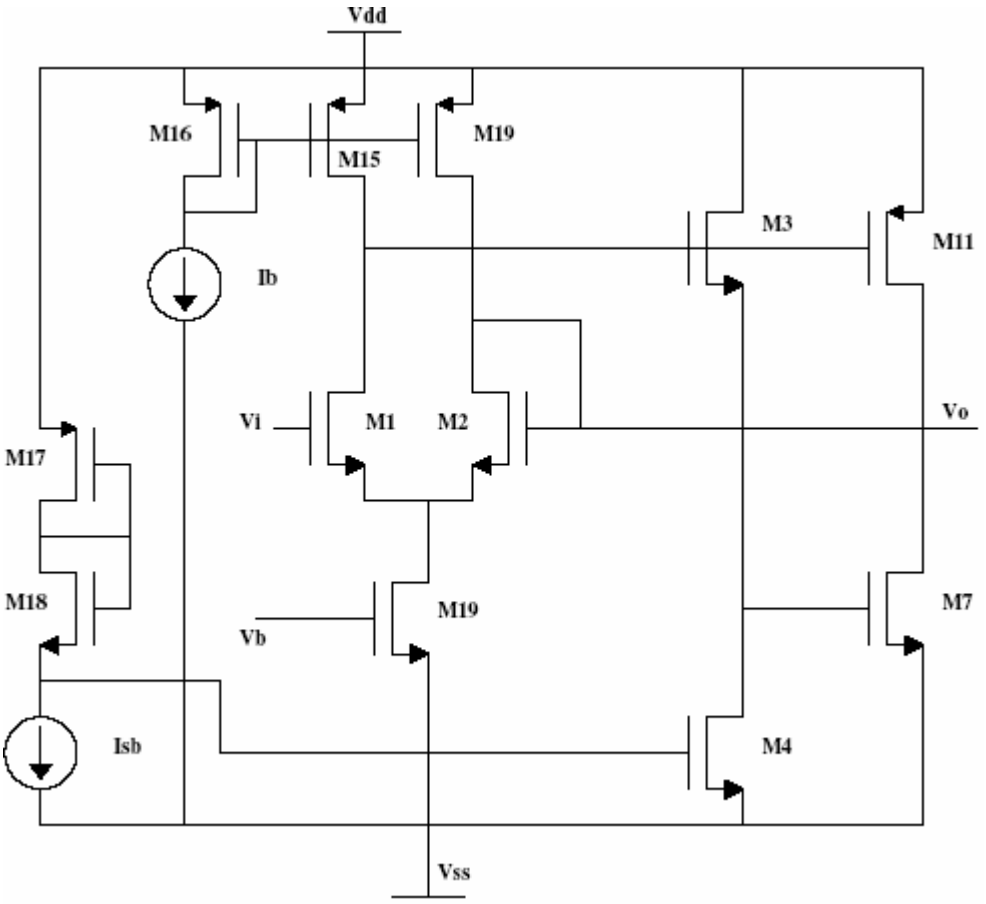

Figure 5.2: Class AB improved buffer

Class AB feedback loop is used in such a way as to make the contribution of the loop to the input referred noise negligible. The voltage tracking of the buffer is achieved by

forcing a constant biasing current I_b through transistor M1 as shown in Fig. 5.1. Assuming that transistor M1 is operating in the saturation region, the gate-to-source voltage of that transistor is constant and therefore:

$$V_0 = V_i - V_T - \sqrt{\frac{2I_b}{K}} \tag{5.1}$$

The low output resistance of the buffer is provided by the action of the class AB negative feedback loop formed by transistors M3, M4, M7 and M11. The feedback loop operates in a class AB mode to minimize the standby power dissipation. The operation of the class AB input stage can be described as follows: if a current is withdrawn from the output terminal, the gate voltage of M11 is lowered. By the action of level shift transistors M3 and M4 the gate voltage of M7 is also lowered. Thus the current through M11 increases and the current through M7 decreases. The result is that the feedback network provides the necessary extra current flowing out of the output terminal. Similarly if the output terminal sinks current, the gate voltage of M11and M7 increases, which decreases the current through M11 and increases the current through M7. The level shift voltage is used to adjust the standby current of the loop. Assuming all transistors are in saturation region and M3 and M4 are matched, it follows that:

$$V_{SG11} + V_{GS3} + V_{GS7} = V_{dd} - V_{ss} \tag{5.2}$$

$$V_{SG17} + V_{GS18} + V_{GS4} = V_{dd} - V_{ss} \tag{5.3}$$

In standby mode no current is with drawn from the output terminal and the current I_b is equal to the current flowing through M_c. Also, in standby mode M7 and M11 have equal currents. Therefore:

$$I_{M7} = I_{M11} = I_{sb} \tag{5.4}$$

The standby power consumption is thus:

$$P_{SB} = V_{DD}\left(I_b + 2I_{sb} + \frac{K_4}{2}\left(V_{DD} - V_{Tn} + V_{Tp}\right)^2 \right) \tag{5.5}$$

The last term in equation (5.5) is the current through the level shift transistors M3 and M4. This current can be kept small by choosing a small aspect ratio for M3 and M4. Transistor M_c can be removed, resulting in a shift in the standby operating point, and the transistor M7 standby current is more than that of M11 by I_b. The small signal output resistance of the buffer circuit is approximately given by:

$$r_{out} \approx \frac{g_{d1} + g_{d15}}{g_{m1}\left(g_{m11} + g_{m7} + g_{d1} + g_{d15}\right)} \tag{5.6}$$

The output resistance is reduced by the class AB negative feedback loop. To characterize the noise behavior of the buffer circuit the input referred noise must be calculated. Since the class AB feedback loop is connected to the drain transistor M1, the input referred noise of this network is divided by the high gain at the drain of M1. Therefore the input

referred noise contribution of transistors M3, M4, M7 and M11 can be neglected. The main noise contribution of the buffer circuit comes from M1 directly and from the current source transistor. The input referred noise is therefore given by:

$$V_{ni} \approx V_{nM1}{}^2 + \left(\frac{g_{m15}}{g_{m1}}\right)^2 V_{nM15}^2 \tag{5.7}$$

The noise contributed by the current source transistor can be minimized by increasing the transconductance of transistor M1and by using long channel transistors for the current source. The disadvantage of the circuit is that the output voltage is level shifted from the input voltage as given by equation 5.1. Although this level shift is constant, it is temperature and process dependent. Furthermore, with this circuit it is assumed that the threshold voltage of transistor M1 is constant. This is only true if source of M1 is connected to its bulk, which can be achieved by using a separate pwell for this transistor. This layout arrangement is necessary to eliminate distortion caused by the body effect. A circuit modification can be used to make the circuit operation independent of the body effect and cancel the level DC shift between the input and output voltage levels. Fig 5.2 shows the modified circuit. The diode-connected transistor M2 is added and a biasing current is used to bias the source terminals of transistors M1 and M2. Since those two transistors have the same source voltage, their threshold voltages match and hence are cancelled out. Furthermore, the current passing through transistors M1 and M2 are forced to be equal by using a current of $2i_b$ to bias the sources of M1 and M2. The biasing arrangement ensures that the gate-to-source voltages of M1 and M2 are equal and hence

the output voltage level is equal to the input voltage with no level shifts. It is worth noting that mismatches between transistors M1 and M2 and mismatches between the biasing currents will cause a small DC voltage offset. This offset can be kept minimum by using common centroid layout technique. Since the added diode-connected transistor M2 is in the signal path, the output resistance of the buffer is approximately doubled and the input referred noise increases by 3 dB.

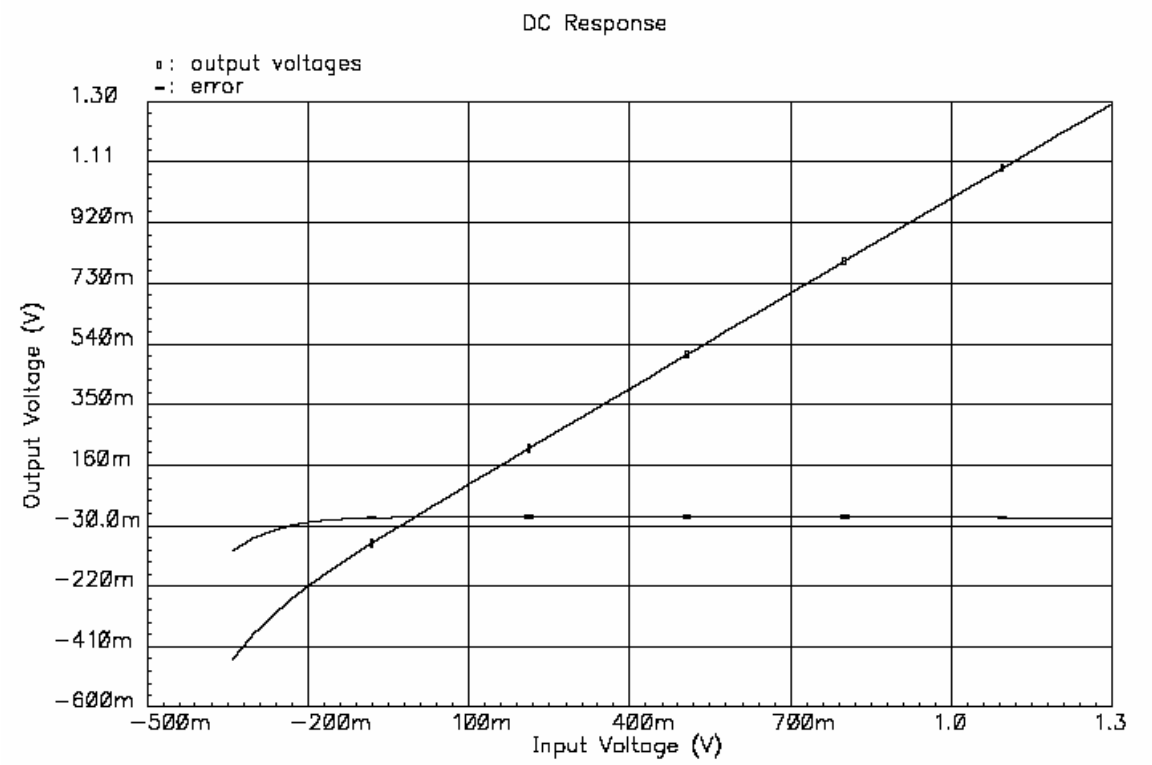

Figure 5.3 Class AB buffer output voltage against input voltage

5.3 Simulation of Class AB buffer

The buffer circuit has been simulated with cadence. The supply voltage was set to be ± 1.5V and the circuit was loaded with a load capacitor of 20 PF and resistor of 8 kΩ. Fig. 5.3 shows that the measured output voltage of the buffer against the input voltage. The dotted line represents voltage tracking error of the buffer circuit. From Fig. 2 it is clear that the circuit provides an operating range of 2Vwhich represents 2/3 of the supply voltage used. The linearity error is found to be less than 0.04% for a 1V signal. The output resistance of the buffer circuit was measured by connecting a current source to the output. The current source was varied

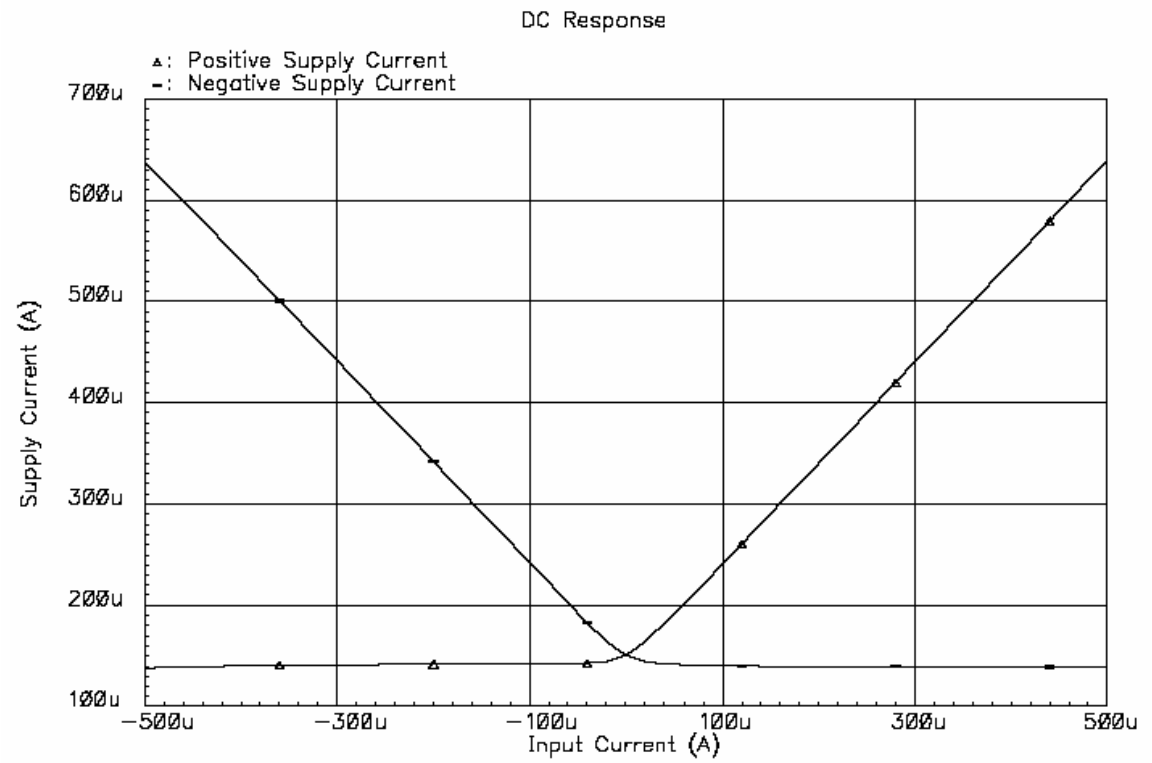

Figure 5.4 Supply current of class AB buffer

from -300μA to 300μA and the variation in the output voltage was recorded. The output voltage varies by 33 mV, indicating an output resistance of 53 Ω. Fig 5.4 shows the supply current of the buffer circuit when the input was grounded and a current source was connected to the output and scanned.

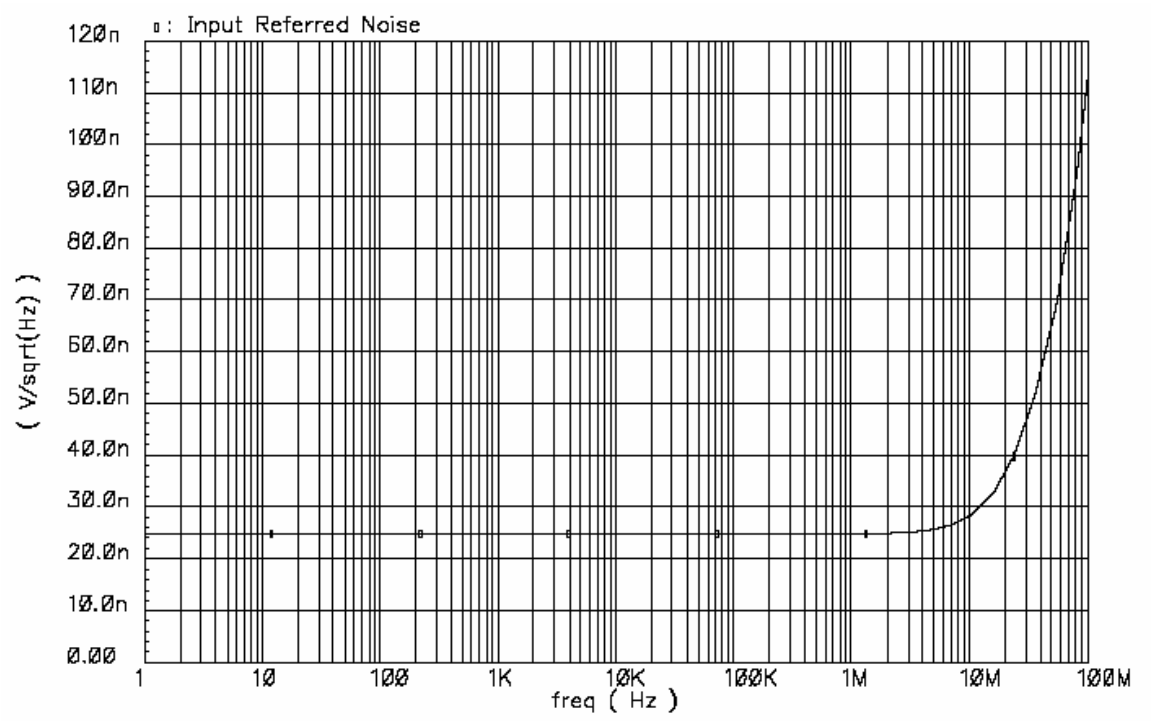

Figure 5.5 Thermal noise simulation of class AB buffer

The buffer circuit consumes a standby current of < 122μA and can provide a current drive capability of > 860μA. The buffer has a bandwidth of 2.8 MHz when driving a

20pF load. It is worth noting that a compensation capacitor can be connected between the gate and drain of transistor M11 to improve the transient performance of the buffer when driving heavy capacitive loads. The input referred thermal noise density is found to be 8.4nV/√Hz. The input referred flicker noise density is 57nV/√Hz at 1 KHz. The flicker noise can be reduced further by using large PMOS input devices instead of NMOS transistors. It is worth noting that lower noise and higher bandwidth can be achieved by increasing the biasing currents and hence the standby power. Figure 5.6 shows the modified low voltage buffer that works with 1.6 V.

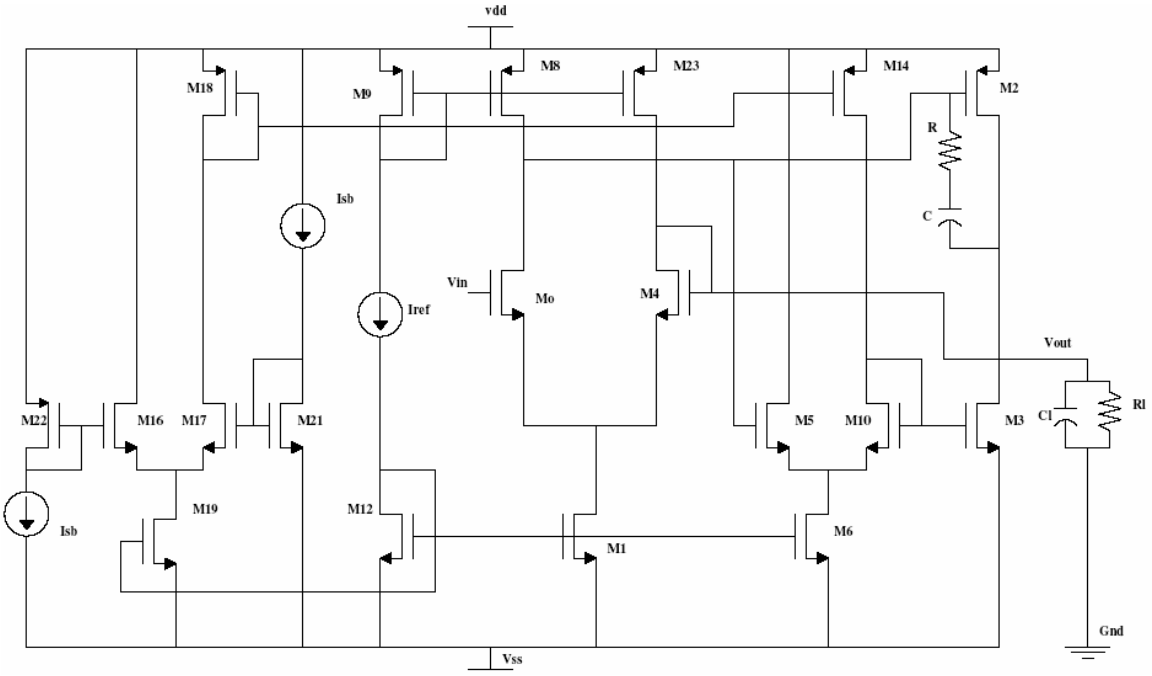

Figure 5.6: Low voltage class AB buffer

5.4 Low Voltage Class AB buffer

Considering the loop formed by transistors M_{11}, M_7 and M_3 in figure 5.1, and using the equation (5.2), we can tell that in order to keep those transistors on, we need at least $3V_T$ Which is more than 2.1 volt in .5 μ Technology. Hence the circuit clearly does not work below 2 V. That's why a modified buffer circuit is needed to work with lower voltages. Now taking the loop equation for figure 5.6 using the transistors $M_{5,}$ $M_{10,}$ M_3 and M_2, we can write:

$$V_{SG2} + V_{GS5} - V_{GS10} + V_{GS} = V_{dd} - V_{ss} \tag{5.7}$$

Considering ideal matching V_{GS5} will cancel V_{GS10}. So this circuit will work for lower voltages. Although, targeted for low voltage it is important to remember that the standby current will also be small. In order to achieve this small standby current through transistor M_{21} and M_{22} are forced. Hence this will fix the gate voltage of matched differential pair M_{16} and M_{17}. These gate voltages are copied to gates of differential pair M_5 and M_{10}. Since gates of class AB stage is connected to gate of M_5 and M_{10}, so same standby current is forced through M_2 and M_3 when the buffer is not driving any load. If a current is withdrawn from the output terminal to the load then gate voltage of M_2 is lowered and hence gate voltage of M_5 is lowered as well. Since the current is fixed by M_{14} for transistor M_{10}, so the gate voltage of M_{10} as well as M_3 will be lowered by the same amount as well. We can see that due to level shift action current of M_2 is increased and current of M_3 is decreased. This extra current will flow through the load. If the current sinks to the output terminal then current through M_3 increases and through M_2

decreases. The other aspects of low voltage buffer is it's low output impedance. The output impedance of the buffer can be approximately written as:

$$r_{out} \approx \frac{2r_{ds4}g_{m4}r_{ds23}}{\left(2r_{ds4}g_{m4} + g_{m4}r_{ds23}\left(1+g_{m4}r_{ds4}\right)\right)\left(1+g_{m2}+g_{m3}\right)} \tag{5.8}$$

Hence output impedance reduces significantly due to feedback effect. Most of the thermal noise for this low voltage buffer are dominated by the transistors M_{12}, M_8, M_9, M_0, M_4, M_{13}, and M_1. The input referred noise can be approximated by:

$$\begin{aligned}\overline{V}^2_{n,in} &\approx 2V^2_{nM4} + \left(\frac{g_{m8}}{g_{m4}}\right)^2 V^2_{nM8} + \left(\frac{g_{m8}}{g_{m4}}\right)^2 V^2_{nM9} + 2\left(\frac{g_{m1}}{g_{m4}}\right)^2 V^2_{nM1} + \left(\frac{g_{m1}}{g_{m4}}\right)^2 V^2_{nM12} \\ &\approx 8KT\left(\frac{2}{3g_{m4}}\right) + 8KT\left(\frac{2}{3g_{m1}}\right)\left(\frac{g_{m1}}{g_{m4}}\right)^2 + 4KT\left(\frac{2}{3g_{m8}}\right)\left(\frac{g_{m8}}{g_{m4}}\right)^2 + \\ &\quad 4KT\left(\frac{2}{3g_{m9}}\right)\left(\frac{1}{g_{m9}}\right)^2\left(\frac{g_{m8}}{g_{m4}}\right)^2 + 4KT\left(\frac{2}{3g_{m12}}\right)\left(\frac{1}{g_{m12}}\right)^2\left(\frac{g_{m1}}{g_{m12}}\right)^2\end{aligned} \tag{5.9}$$

5.5 Low Voltage buffer simulation

The buffer has been simulated using AMI .5μm technology. Fig 5.7 presents the buffer output voltage. From this simulation we can see that the available working range for this buffer is around 50% of the supply voltage. Also the difference between output and input for that range is shown as well. It can be found that linearity error is <.06% for a 1V signal. The input referred thermal noise is presented in fig. 5.8. From the noise analysis we can tell that input referred noise is 3.7 nV/√Hz which is a good measure performance.

Referring the fig. 5.6 it is inferred that most of the noise has been contributed by Transistors $M_{12,}$ $M_{8,}$ $M_{9,}$ $M_{0,}$ and $M_{4.}$

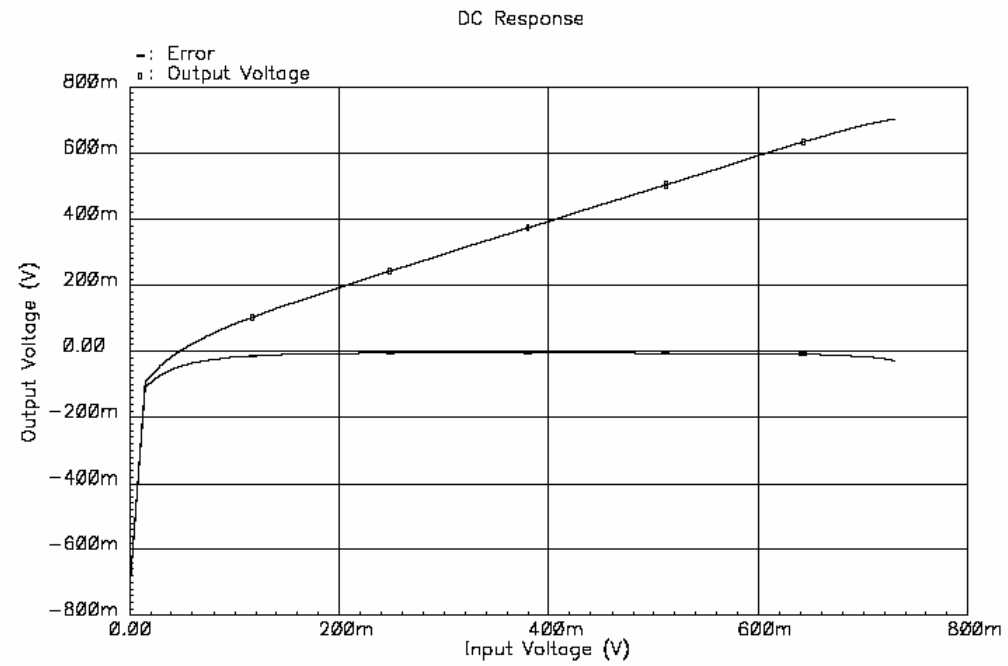

Figure 5.7 Low voltage buffer output against input voltage

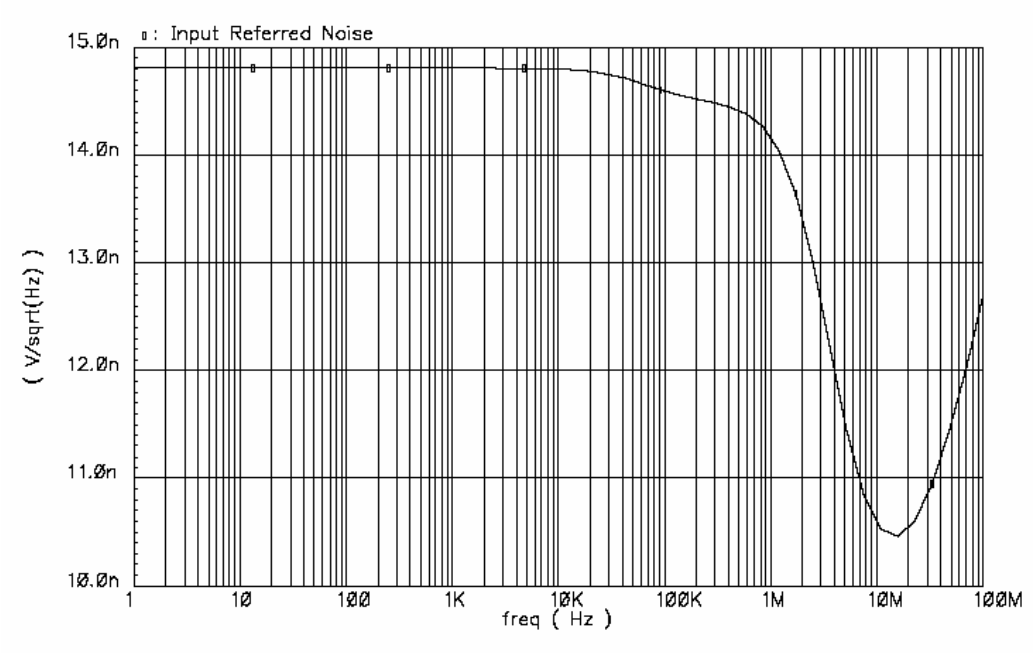

Figure 5.8 Noise Simulation for low voltage buffer

Figure 5.9 shows the supply current of the buffer. It provides a current drive capability of more than 950 μA when driving a load capacitor of 12 pF and resistor of 5KΩ. The standby current for this circuit is less than 179 μA. The supply voltage is 1.6 V and power consumption achieved was 2.8 μW. This buffer can be used in many analog building block such as filter, VGA, A/D etc. In the next section we will describe about filter and at the end an implementation of filter using this buffer for WCDMA will be revealed.

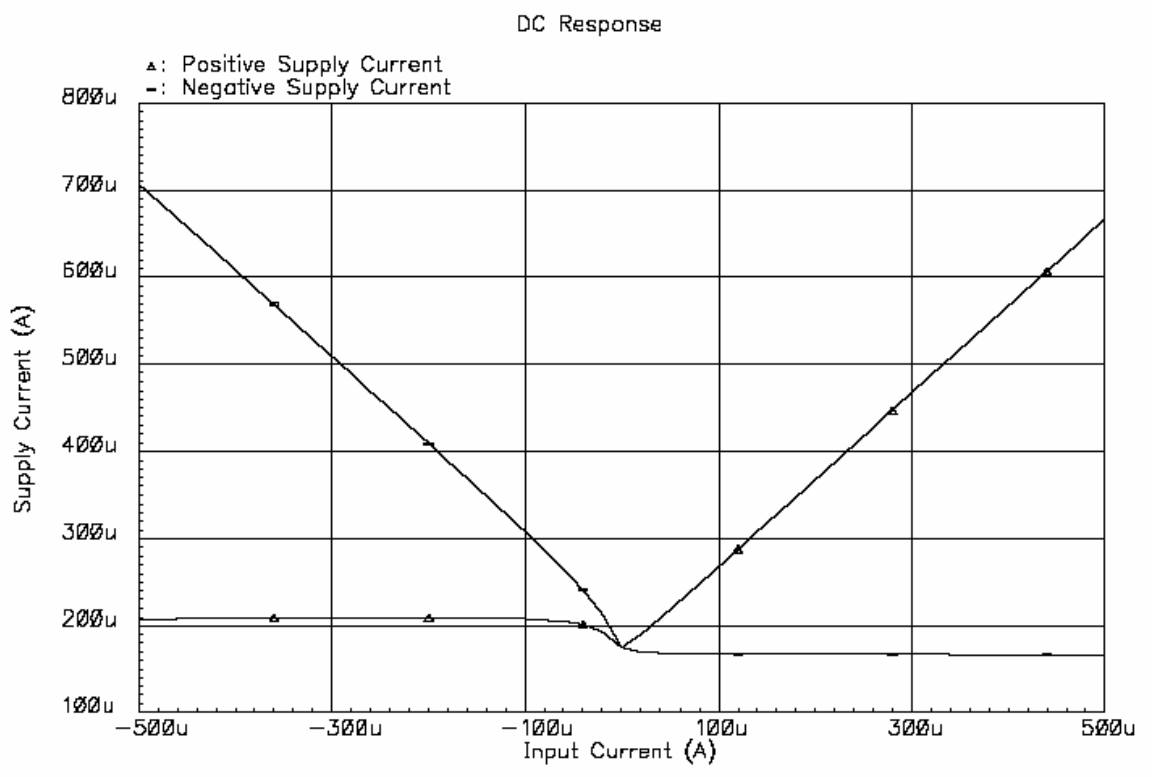

Figure 5.9 Supply current of low voltage buffer

5.6 Filter Design

Many classes of filters [2, 50, 52] are available for different applications such as, switched capacitor filters, LC filters, MOSFET-C filters, G_m/C filters and active-RC filters. Switched capacitor filters are not suitable for continuous-time anti-aliasing application. In LC filters, the poles lie only on the jω axis. Inductors can suffer from nonlinearities due to saturation or wiring and core losses. In addition, high-Q inductors are difficult to realize in a standard CMOS process. A G_m/C filter eliminates the problem

of excess phase from high-frequency non-dominant poles that can cause large errors in the filter response [54]. However, G_m/C filter is very sensitive to parasitic capacitance that may load down the integrating capacitor. This has the effect of increasing the unity gain bandwidth. In addition, the transconductance for the G_m/C filter is nonlinear. The active-RC filter is very linear because only passive poly-poly capacitor and resistors are used. The op-amp in the RC filter can be designed to maximize the performance of the filter. Although the values of resistors and capacitors vary due to process, but for as a low-pass filter it works excellent since it does not affect the passband. It also has high SNR. So for WCDMA application we will chose active RC topology.

5.6.1 Magnitude and Phase response

Magnitude response of ideal low pass filter can be shown in Figure 5.10. The plot, in figure 5.10. shows the low-frequency signal components are transmitted, while high-frequency components are blocked.

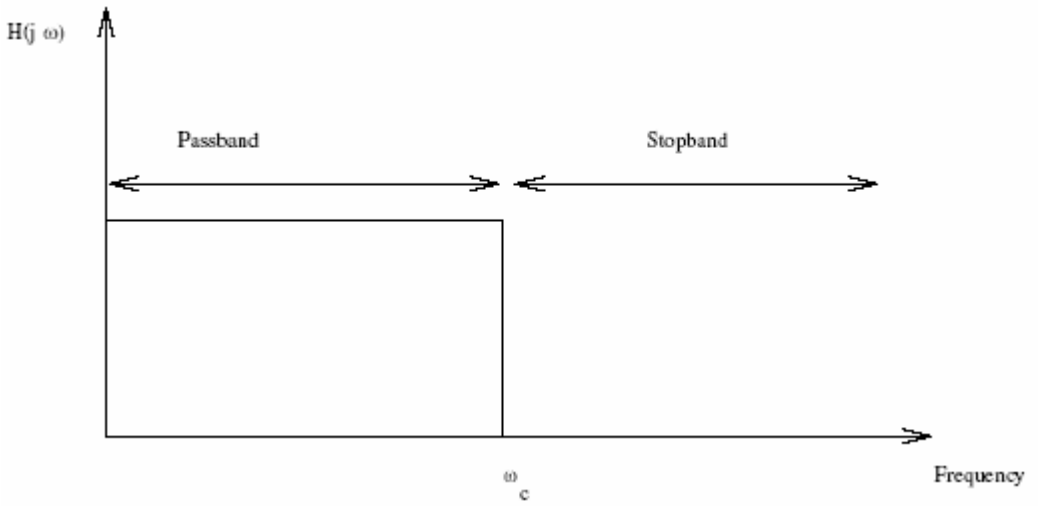

Figure 5.10 Ideal Magnitude Response

The range of low frequencies which are passed is called the passband or bandwidth of the filter. The range of high frequencies which are stopped is known as the cut-off frequency or ω_c. In practice, the sharp transition bandwidth of the ideal brick wall response is difficult to realize. The response thus only can be approximated [50]. One approximation is shown in Figure 5.11, known as Butterworth response.

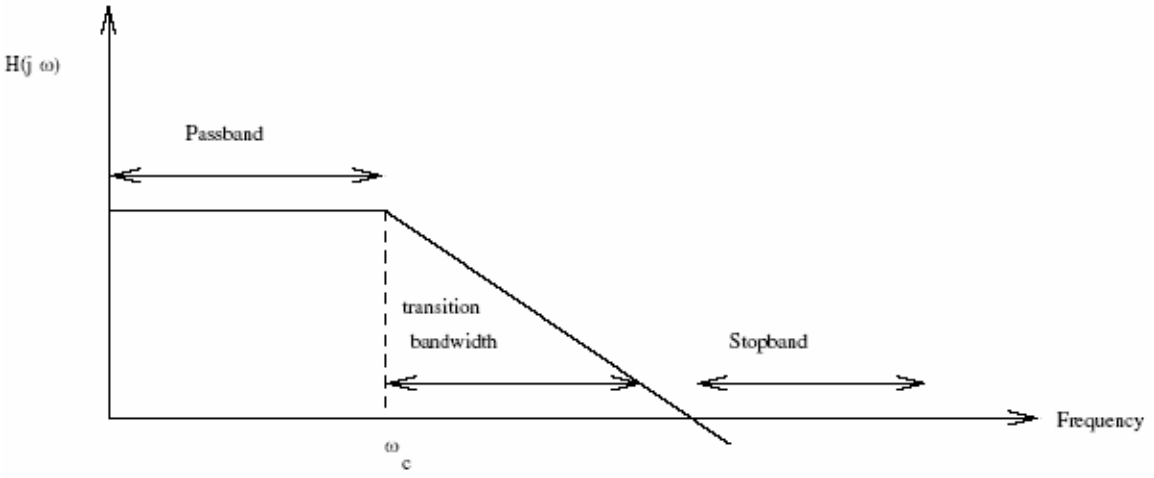

Figure 5.11 Butterworth Magnitude Response

The Butterworth response is monotonic, i.e., the derivative of the magnitude does not change sign over a given range of frequencies. In addition, the passband is maximally flat. All poles for this response lies on a unit circle while all the zero lies at infinite frequencies. Note that the butterworth has a very wide transition bandwidth. Because of this, the stopband attenuation is poor for filters of lower orders.

A better approximation of low pass characteristics is the Chebychev response, shown in Figure 5.12. A characteristics of the magnitude response is ripples in passband. The stopband attenuation for the Chebychev response is higher than that of Butterworth response for filters of same order.

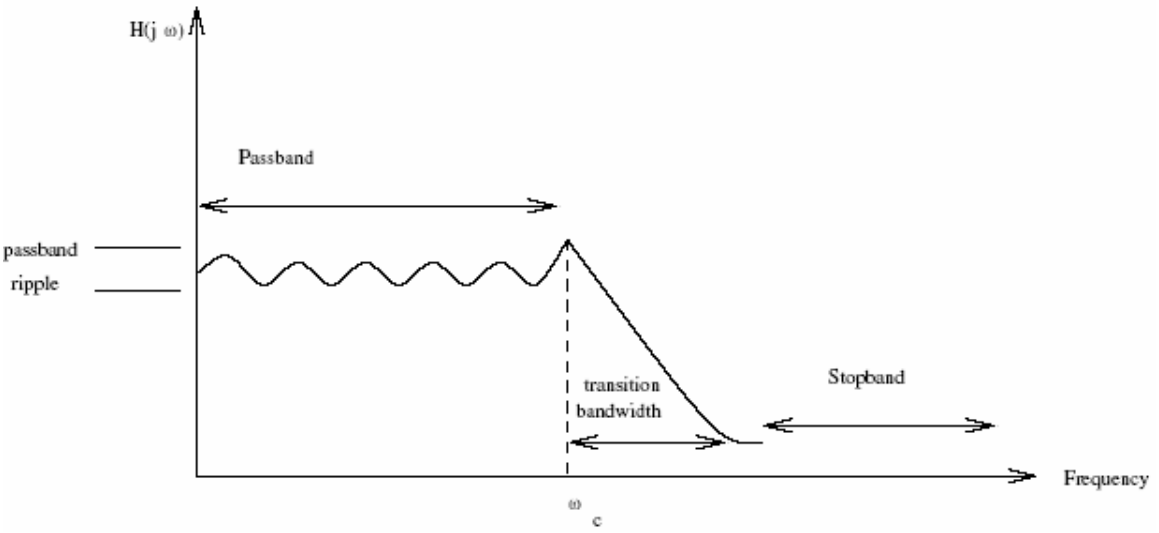

Figure 5.12 Chebychev Magnitude Response:

Because of the ripples, the transition bandwidth of the Chebychev response is also sharper than that of the Butterworth response. The pole of the Chebychev response is on an ellipse and the zeros are all at infinite frequencies.

Another approximation that has ripples in both the passband and the stopband is known as the Elliptic response in Figure 5.13. For the same order filter as the Butterworth and Chebychev, this response provides the smallest transition bandwidth and the largest stopband attenuation. The poles in the Elliptic response lie on an ellipse, and zeros are on the imaginary axis. The zeros provide the ripples in the stopband.

Phase characteristics are equally important, while designing filters, since in an ideal transmission, information content should be same at output and input.

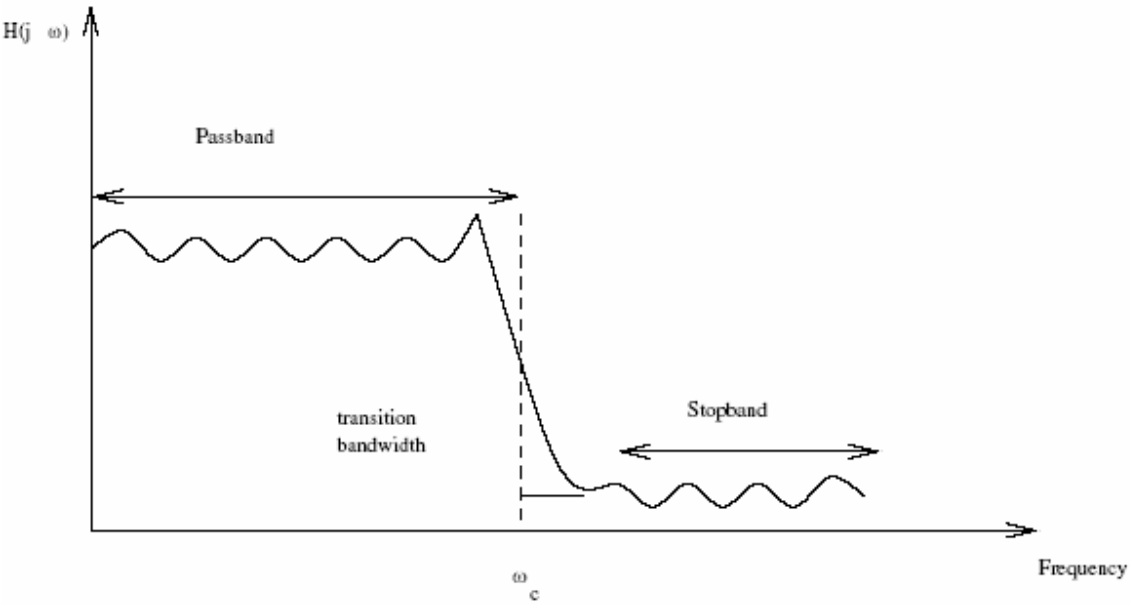

Figure 5.13: Elliptic Magnitude Response

This means that in an ideal filter response, the phase should be linearly proportional to frequency.

The Butterworth, Chebychev and Elliptic responses all have phase characteristics that deviate from the ideal. The Butterworth has the most linear phase among the three, followed by the Chebychev, and the Elliptic response. The characteristics of the three responses is summarized in Table 5.1 [2]. The Elliptic provides the sharpest cutoff between the passband and stopband for a given order. However, the Butterworth provides the most linear phase. The Chebychev appears to be a good compromise between the

three responses. It provides better stopband attenuation than the Butterworth, and the phase response is not as poor as Elliptic. For these reasons, the Chebychev response is selected.

	Butterworth	Chebychev	Elliptic
Pole Location	On unit circle	On ellipse	On ellipse
Magnitude Response	Maximally flat	Ripples in passband	Ripples in passband Ripples in stopband
Phase Response	linear	Less linear	poor
Filter order for same stopband attenuation	high	medium	low

Table 5.1: Comparison of Filter Response

Here poles are implemented with a Sallen-Key filter described next section.

5.6.2 Sallen-Key Filter

The Sallen-Key filter is one of the popular choice in designing filter because it is easy to analyze and design [52]. The low-pass Sallen-Key filter is shown in fig 5.14 [2]. Filter

can be made programmable by changing only resistor or capacitance values. Other advantages can be obtained if op-amp is replaced by a buffer.

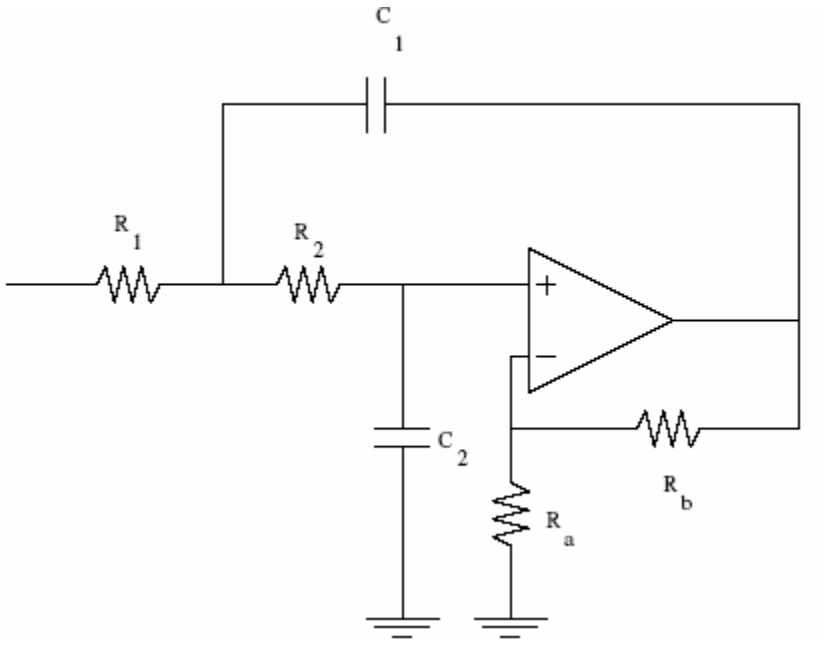

Figure 5.14: Sallen-Key Filter

The general form of the transfer function can be written as:

$$H(s) = \frac{G\omega_0^{\,2}}{s^2 + \left(\frac{\omega_0}{Q}\right)^2 + \omega_0^{\,2}} \tag{5.10}$$

Where G is the DC gain, ω_o is the undamped natural frequency, and Q is the quality factor. The quality factor Q is the relative sharpness at which the peak of the magnitude

response occurs. By analyzing the Sallen-Key circuit, we can find G, ω_o and Q in terms of element values. These are given by [51][52].

$$\omega_0 = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}} \tag{5.11}$$

$$Q = \frac{\omega_0}{\frac{1}{R_1 C_1} + \frac{1}{R_2 C_2} + \frac{1-G}{R_2 C_2}} \tag{5.12}$$

$$G = 1 + \frac{R_b}{R_a} \tag{5.13}$$

An important parameter known as sensitivity is a measure of filter's performance or figure of merit. While designing filter, it is a good idea to find the sensitive components of the circuit in order for a robust design. Sensitivity is the measure of the change in a performance characteristic when there is a change in the nominal value of one or more elements [50][51]. A design which is attractive from a theoretical stand point but has high sensitivities may be useless in practice. The symbol S is used to denote sensitivity. The characteristic that is being evaluated is denoted by the superscript character while the element changed is denoted by the subscript character. For example, if y is the performance characteristic and x is the element, the sensitivity is defined by

$$S_x^{\,y} = \frac{\delta y}{\delta x} \bullet \frac{x}{y} \tag{5.14}$$

The sensitivity of the Sallen-Key filter depends on the choice of the element values in the circuit. Three kinds of designs are evaluated in the next sections, and their sensitivities

will be compared. In the first design, all the capacitances are set to the same value and all the resistances are set to the same value, as given below

$$C_1 = C_2 = C \tag{5.15}$$

$$R_1 = R_2 = R_3 \tag{5.16}$$

Now f_c (cut off frequency) and Q are independent of one another and the design is greatly simplified. The gain of the circuit now determines Q and good matching is also available. RC sets the value of cut off frequency. One draw back is, since gain controls the Q, further gain or attenuation may be necessary to achieve the desired signal gain in pass band. By rearranging the equations we can write,

$$RC = \frac{1}{\omega_0} \tag{5.17}$$

$$G = 3 - \frac{1}{Q} \tag{5.18}$$

The second design has equal capacitance values, and the feedback resistors are set to the same value. The feedback resistors are thus easy to match and the gain is fixed at two. This is shown by,

$$C_1 = C_2 = C \tag{5.19}$$

$$R_a = R_b = R \tag{5.20}$$

With some computation, we find that the following conditions must be true,

$$R_1 = \frac{Q}{\omega_0 C} \tag{5.21}$$

$$R_2 = \frac{1}{R_1 \omega_0{}^2 C^2} \tag{5.22}$$

The final design to be considered is when the gain is set to be 1. The novel buffer can be used in place of the op-amp. The gain is now insensitive, and there is no noise contribution from the feedback resistors which have been set to zero. Again the equation below must hold true.

$$C_1 > C_2\left(4Q^2\right) \tag{5.23}$$

By using the element values from the three design above, it is shown that their sensitivities differ. As shown in Table 5.2 [2], design 1 is the simplest to implement but it has the highest sensitivities. Design 2 is not as sensitive as design 1, but this is at the expense of a wide resistance spread between R1 and R2. Design 3 is the least sensitive but this is at the expense of great capacitor spread between C_1 and C_2. For minimum sensitivity reasons, design 3, the unity gain configuration was selected.

There is a trade off in selecting resistance and capacitance values for the unity-gain Sallen-Key filter. Because the resistors R_1 and R_2 in the filter will generate noise, according to

$$V_R{}^2 = 4KTR\Delta f \tag{5.24}$$

We would like to minimize the resistance. However, for the same cut-off frequency if we decrease the resistance the capacitances C_1 and C_2 will increase. There are a number of disadvantages [2] in increasing the capacitances. First, the area will increase. Second the capacitance C_1 will load down the amplifier. This increases the slew rate of the amplifier,

and the increased current to drive the capacitor will increase the power dissipation. More importantly, a large value of C_1 will create a left-half-plane zero in the transfer function

	Design 1	Design 2	Design 3
G	$3-1/Q$	2	1
$S_{R_1}^{Q}$	$-1/2+Q$	$-1/2+Q$	0
$S_{R_2}^{Q}$	$1/2-Q$	$1/2-Q$	0
$S_{C_1}^{Q}$	$-1/2+2Q$	$1/2+Q$	$1/2$
$S_{C_2}^{Q}$	$1/2-2Q$	$-1/2-Q$	$-1/2$
$S_{R_a}^{Q}$	$1-2Q$	-1	0
$S_{R_b}^{Q}$	$2Q-1$	-1	0
$S_{R_a}^{G}$	$-\frac{2Q-1}{3Q-1}$	$-1/2$	0

Table 5.2 Sensitivity Comparison

which will reduce the attenuation of the filter. The resistance and capacitance values must be chosen to optimize the noise and power dissipation, while preserving the functions of the filter.

5.6 Filter Simulation

Figure 5.15. shows a 6th order Sallen-Key filter meeting the specification for WCDMA standard. The buffer that designed in previously has been taken here as active element. The circuit is highly linear, since buffer bandwidth is high and input referred noise is low as one active element is being used. So it can be used as prefilter for analog baseband front end. Simulation for this filter is done using AMI .5µ technology. The frequency response is shown in fig 5.17. So we can see 3-dB bandwidth is more than 2.4 MHz . Pass band ripple is less than less than .5 dB and stop band attenuation is more than 70 dB at 10 MHz. Use of higher order filters help in removing the out-of-band blockers and reducing the dynamic range of ADC (Analog-to-Digital Converter).

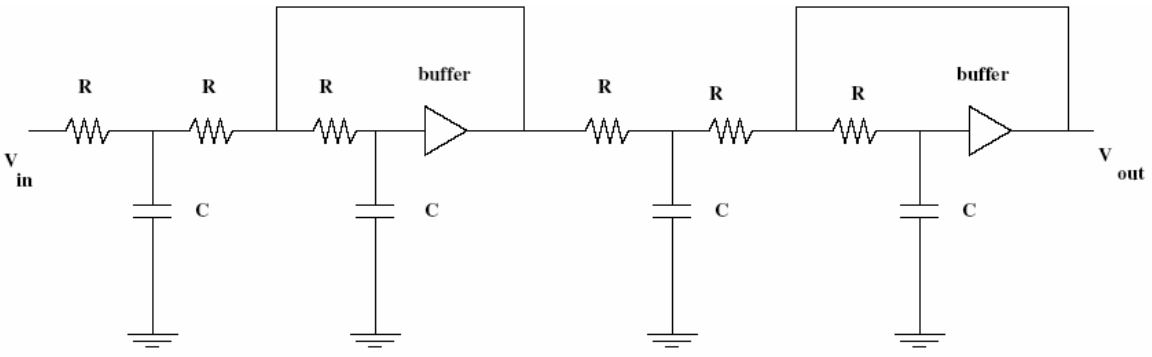

Figure 5.15: A 6th order Sallen-key filter for WCDMA application

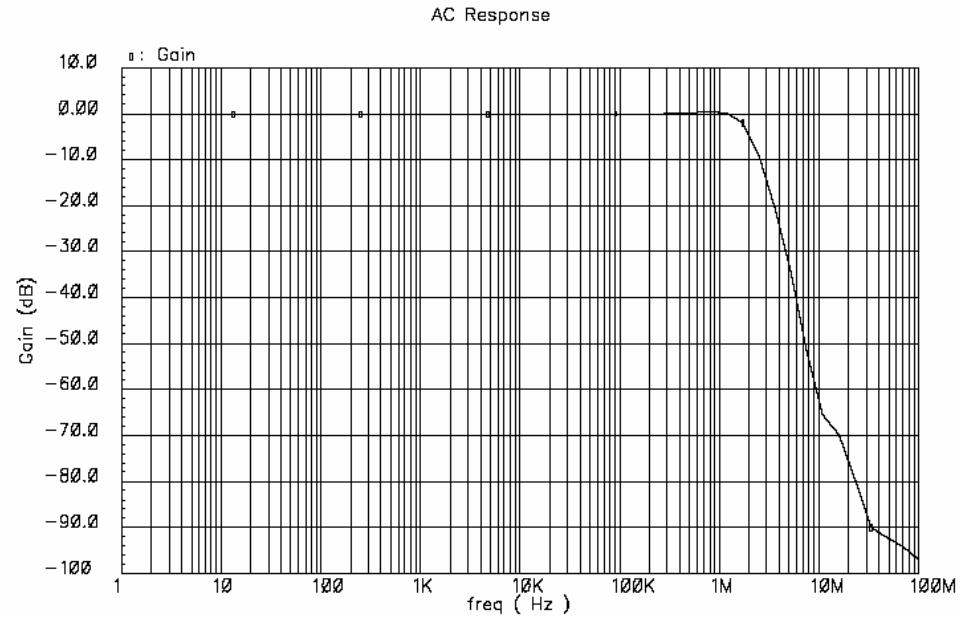

Figure 5.17 Frequency Response of the Filter

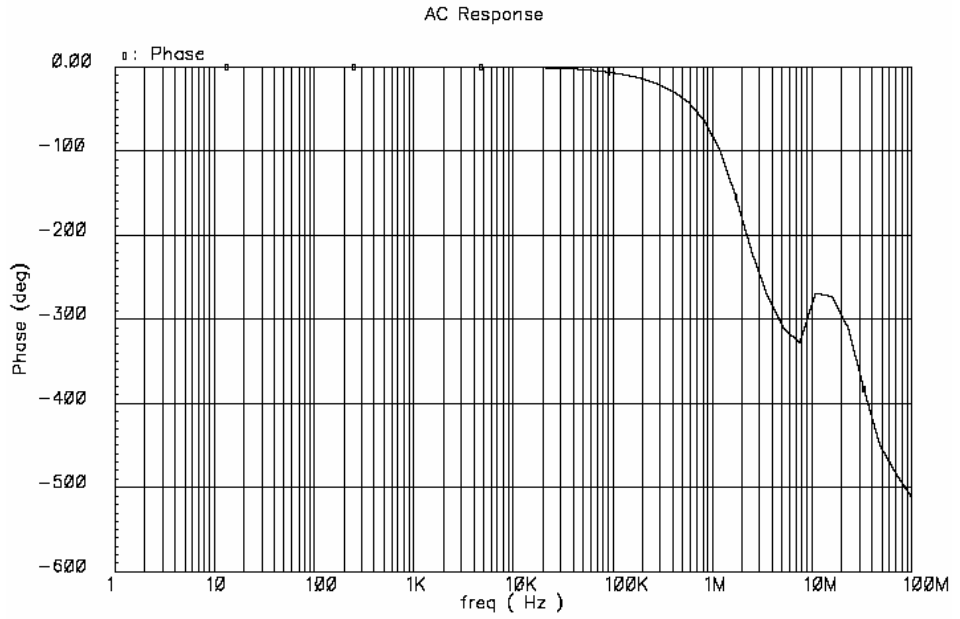

Figure 5.18 Phase of the filter

CHAPTER 6

CONCLUSION

This chapter summarizes the results of all sections and provides recommendations for future work. The trade off between receiver performance and integration continues to pose a challenge in designing receiver circuit. On one hand it is desired to have a receiver with high selectivity and sensitivity at the same time it is required have low cost, low power and small form factor which is the basis of monolithic receiver integration. Also due to the rising demand, receiver is desired to have multi-standard capability. In this thesis, we have studied these issues and proposed some solution to compromise both of those issues.

The continued scaling of CMOS process requires the lowering of available supply voltage. This cause additional problem in achieving low power circuit. In this thesis, we our focus was to achieve low voltage low power solution for the baseband component. For the RF/IF part the concentration is to achieve integration of the receiver by eliminating high Q image reject filter, proving a calibration system to have a sufficient

IRR for the required specification. That's why we tried to come up with an acceptable solution.

An unity gain buffer is an important anlog building block, usually feed in between two stages where output impedance of first stage is very high and load impedance is low. In such cases it is inserted between those two stages and avoid signal losses. This is not the only application for an unity gain buffer. Buffer finds itself useful in many operations. However in a given technology it is always difficult to design a buffer operating with a very low voltage. We have already demonstrated the design technique in chapter 5. The performance of that buffer is given in table 6.1.

Supply Voltage	1.6 V
Technology	0.5 μm AMI technology
Power Consumption	2.84 μW
Available range	700 mV
Drive capability	> 950μA
Bandwidth	5 MHz
Input referred noise	3.7 nv/√Hz

Table 6.1: Performance of low voltage buffer

This buffer has been used in a sallen-key architecture to implement a 6^{th} low pass filter that can be used for WCDMA. The pass band ripple is less than .5dB and stopband attenuation for 10 MHz is higher than 70 dB. Two 3^{rd} order section is cascaded to achieve 6^{th} order. The linearity for this filter will be high, since buffer itself has high bandwidth, extending over to the stopband of filter, so high linear out of band IIP3 is expected. Simple implementation of higher order filter can be observed. Because of high linearity, this type of filter is suitable for implementing first stage of analog baseband front end. It can be make programmable by changing R or C and the order of the filter as well. Low input referred noise is expected as well, since few active elements per each 3^{rd} order section. So programmability can be achieved and design cycle is short. This buffer can be implemented for other circuit blocks such as VGA and the whole baseband can be design using buffer in each of the circuit components. One clever application of such an idea is reported in [3].

GSM is one popular wireless standard. It's channel spacing is 100KHz and one challenging requirement is to have very low noise in low frequency such @ 100KHz. We have noticed earlier that flicker noise dominate at low frequency and hence to make a design for such system is really challenging. In chapter 4 some VGA topologies is explored. The trade off in adopting different current sensed VGA has been discussed as well. These type of VGA achieve a gain range of 36 dB and input referred noise @ 100KHz is 9 nV/√Hz. With optimized device sizing it can be reached around 6 nV/√Hz. It's 3^{rd} harmonic distortion for single ended input of $1V_{pp}$ @ 1MHz is <-70dB. Total THD is <-57 dB. The 3-dB bandwidth available is more than 100MHz. Output resistance R_1 is 5K. we can only change R_1 as shown in the chapter 3 to realize programmable gain.

For such a range R_1 is varied from 50 Ω to 10 K Ω. In some application target is very high bandwidth. Another advantage of using such high bandwidth VGA is that it can be used for multi-standard purposes. To implement such VGA we adopted the topology of high gain g_m based amplifiers. Here a g_m boosting circuit is used as described in chapter 3 to increase bandwidth and linearity. Also their trade off has been discussed. The voltage gain for such circuit is in the range of 20 dB. From the frequency response curve we see that a 3-dB bandwidth of more than 500 MHz (.5 GHz) can be achieved. In order to keep the bandwidth constant we did not disturb the output load impedance R_2. Variable gain setting is realized by changing source degenerated resistance R_1. Input referred noise achieved @ 100 KHz is 61 nV/√Hz. Again with proper device sizing it can be reached at 14 nV/√Hz. The third harmonic distortion for single ended input of $1V_{pp}$ @ 1KHz is <-110 dB. THD available is <-95 dB.

The major bottleneck in realizing monolithic integrated receiver is the high Q image reject receiver. That is also one of the major problem that Heterodyne receiver suffers. To avoid this issue image-reject receiver such as Weaver and Hartley can be adopted. But their performance is limited to the matching of the components in the two quadrature path. For a mismatch of 0.2 to 0.6 dB in gain and 1 to 5 degree in phase limits the image rejection ratio (IRR) to 30-40 dB. That seems reasonable with Bluetooth standard but most of the standard's like GSM require image rejection close to 60 dB due to it's narrow channel spacing. One critical issue in Hartley's architecture is the gain mismatch resulting from the 90 degree phase shift operation. In fig. 3.xx for example, two phase shift stages exhibit equal gain only at $\omega_{IF} = 1/(RC)$. Thus for a given ω_{IF} a gain imbalance arises if the absolute value of R and C varies with temperature or process.

Specially if the resistors are equal to R+ΔR and capacitors equal to C+ΔC, the relative gain imbalance is:

$$\frac{\Delta A}{A} = \frac{(R+\Delta R)(C+\Delta C)\omega - 1}{\sqrt{1+(R+\Delta R)^2(C+\Delta C)^2\omega^2}} \div \frac{1}{\sqrt{1+R^2C\ \omega^2}} \tag{6.1}$$

Since in the vicinity of ω_{IF}, RCω≈1, we have

$$\frac{\Delta A}{A} \approx \frac{\frac{\Delta R}{R}+\frac{\Delta C}{C}}{\sqrt{2+\frac{\Delta R}{R}+\frac{\Delta C}{C}}} \div \frac{1}{\sqrt{2}} \approx \frac{\Delta R}{R}+\frac{\Delta C}{C} \tag{6.2}$$

For example, ΔR/R = 20% limits the image rejection to only 20 dB. So the matching requirement in this topology is stringent, since very sensitive to mismatch. The Weaver architecture is less sensitive in matching than Hartley, but it has the problem of secondary image if the second downconversion translates the spectrum to a non-zero frequency. Also, harmonics of the second LO frequency may downconvert unfiltered interferers from first IF to second IF.

However, to avoid all those issue it is necessary to have a calibrating system which restore the proper IRR. Moslty two types of calibration is available. Calibration using a calibrating tone or without using any calibrating tone. There are also other choices as well. However most of those calibration system has issues such as use of lots of mixer and multiplier which is major source of mismatch. A simple phase analog phase calibration technique with out using any external tone is presented in this thesis. In order

to verify it's performance simulink model has been constructed. The following table will give a comparison [29, 30, 33, 36] to different calibration techniques.

Solution	IRR	Report	Year
Hand Tuning	45 dB	JSSC	1997
Analog Calibration	57 dB	ESSCIRC	2000
Switched-capacitor Hilbert transformer	47 dB	Ph.D Thesis	2002
Sign-Sign LMS	57 dB	JSSC	2003
Analog Calibration	59 dB	JSSC	2004
Proposed solution	59.5		2004

Table 6.2: Comparison of IRR

The simulation uses the following parameters:

1st LO frequency =1.6GHz

2nd LO frequency =200MHz

RF signal and its image are chosen as:

RF_{in} frequency = 1872 MHz

Image frequency = 1328 MHz

IF frequency = 72 MHz

Again this mismatch simulation was done assuming a phase mismatch of 2 degree and small gain mismatches. However if the gain mismatches increases then IRR will be down. Also some algorithm for Hartley receiver with out calibrating tone and algorithm for Weaver using external calibrating tone is presented in the thesis as well.

The contributions of the dissertation are: development of novel phase calibration techniques to improve IRR, circuit design technique for low noise, high bandwidth VGA and implementation of a low voltage buffer for a 6^{th} order WCDMA filter.

The future for this research will be to implement the system in CMOS circuit level and measure the result. Also at that time attempt will be made to include gain mismatches and find more optimize algorithm. CMOS realization for Hartley receiver will also be investigated. For VGA more simulation has to been done to find optimum device sizes and hence the optimum performance in terms of noise, linearity etc. Also new techniques for VGA should be explored.

The buffer circuit will be used to build other blocks such as VGA, low pass filter, converter etc. Also buffer based baseband chain will be implemented. Trade off between the location of VGA, filter, A/D and their order in implementing the system will also be investigated in near future. Hence we will be able to optimize the receiver performance with monolithic integration.

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