Analysis & Design of Radio Frequency Wireless Communication Integrated Circuits with Nanoscale Double Gate MOSFETs

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Abstract

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Analysis & Design of Radio Frequency Wireless Communication Integrated Circuits with Nanoscale Double Gate MOSFETs (214 pp.)

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Today's nanochips contain billions of transistors on a single die that integrates whole electronic systems as opposed to sub-system parts. Together with ever higher frequency performances resulting from transistor scaling and material improvements, it thus become possible to include on the same silicon chip analog functionalities and wireless communication circuitry that was once reserved to only an elite class of compound III-V semiconductors. It appears that the last stretch of Moore's scaling down to 5 nm range, these systems will only become more capable and faster, due to novel types of transistor geometries and functionalities as well as better integration of passive elements, antennas and novel isolation approaches. Accordingly, this dissertation is an example to how RF-CMOS integration may benefit from the use of a novel multi-gate transistors called FinFETs or Double Gate Metal Oxide Semiconductor Field Effect Transistors (DG-MOSFETs). More specifically, this research is to validate how the performance of the radio frequency wireless communication integrated circuits can be improved by the use of this novel transistor architecture.

To this end, in this dissertation, a wide range of radio frequency integrated circuits have been investigated in DG-MOSFETs which include Oscillators, On Off Keying (OOK) Modulator, Power Amplifier, Low Noise Amplifier, Envelope Detector, RF Mixer and Charge Pump Phase Frequency Detector. In all cases, the use of DG-MOSFET devices lead to reduction of transistor count and circuit complexity, while also resulting in tunable circuits owing to local back-gate control available in this device structure. Hence this work provides a unique insight as to how modest geometry changes and 3D device engineering may

result in significant gains in analog/RF circuit engineering in the last stretch of Moores scaling.

To the memory of my father,

Bhanu Kumar Laha

and grandfather,

Sudhanshu Sekhar Laha

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I also remember the wonderful moments that I have spent with all my colleagues during the course of the dissertation.

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1 Introduction & Motivation

1.1 Wireless Communication

Wireless communications today impact and enable a plethora of applications. Among these, the mobile-cellular industries is the backbone of wireless communication and the most promising. In the last few years, the global subscription in mobile-cellular communication has exceeded the number of wireline telephone subscriptions. The worldwide mobile-cellular subscription in 2014 has reached 6.915 billion [21], which is almost equal to the world population of 7.1 billion. This remarkable figure speaks for itself the importance of mobile-cellular services and wireless communication, in general. Today's mobile-cellular handset is no more a device for voice communication but a wholesome digital personal assistant where multimedia products are consumed via wireless communications links ranging from wireless data transfer and high-speed internet access. These features are collectively termed as the fourth-generation (4G) cellular and paved the way for the migration of conventional mobile phones to smart-phones. These smart-phones and 4G have played together an important socio-economic role in motivating research in new wireless signal processing methods and currently research is undergoing towards fifth-generation (5G) cellular, where speed is the primary ingredient intended for ultra fast data communications and internet.

Besides the mobile-cellular telephony, other contexts for wireless communications also exist which are primarily centered around different wireless technologies such as Zigbee, Bluetooth, wireless local area network (WLAN) systems, wireless personal area network (WPAN) systems, wireless metropolitan area network (WMAN) systems etc. [21]. These wireless technologies provide the framework for a variety of applications, which include, wideband internet access, local telephony service, wireless data transfer of high-speed entertainment content of high-definition video and high-quality audio. Similar to 4G, these

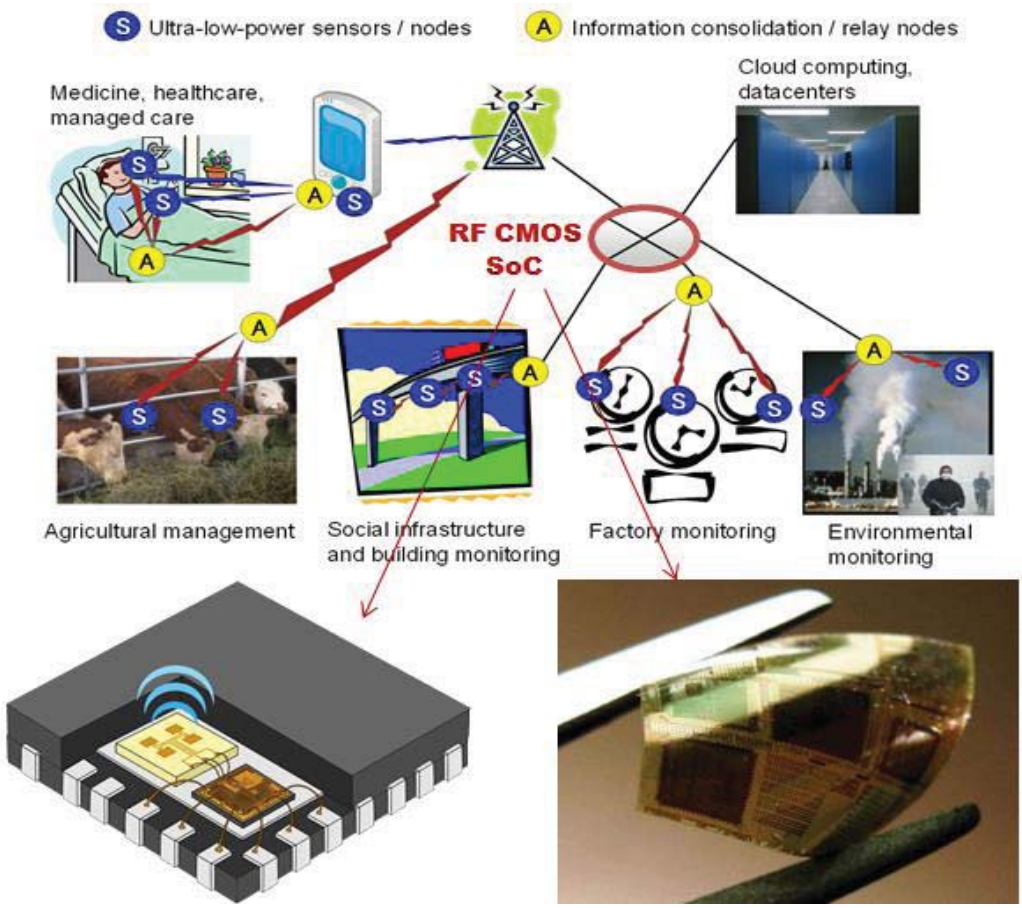


Figure 1.1: Illustration of application of wireless communication in different areas [3], [4],[5].

technologies have spurred significant research in signal coding, transmission, processing as well as hardware development for wireless. In Fig. 1.1, the application of wireless communication in various segments is demonstrated.

Finally, another trend in wireless communication industry is the incessant search for more bands and bandwidth in data links serving content-rich and dynamic multi-media systems, which can only be found at higher speeds > 10 GHz. In fact it is anticipated that 0.1 to 0.5 THz wireless circuits will be readily achievable using standard Silicon materials and CMOS devices. Since, a great majority of circuits and systems developed in this

dissertation operate around 60-100 GHz, our work is at the forefront of this strategically important research area that is likely the final territory, besides optical applications, not conquered by silicon integrated circuits. Work described here is especially relevant and useful for devices and systems currently smaller yet booming segment of wireless communications industry. Particularly, in the spirit of Fig. 1.1, it can be related to the framework of solutions for hig-capacity, low cost, on and off chip wireless data links in conventional computational platforms as well as futuristic highly-connected networks of 'internet of things' with many distributed and non-conventional data collection, processing and analysis systems.

1.2 Integrated Circuits

As we explore hierarchically the context and motivation for this work, next important fact to realize is that today's nanochips contain billions of transistors on a single die that integrates whole electronic systems as opposed to sub-system parts. This can be observed from the Fig. 1.2. Together with ever higher frequency performances resulting from transistor scaling and material improvements, it thus become possible to include on the same silicon chip analog functionalities and communication circuitry that was once reserved to only an elite class of compound III-V semiconductors [14]. It appears that in the last stretch of Moore's scaling down to 5 nm range, only limited by fabrication at atomic dimensions and fundamental physics of conduction and insulation, nanochips will only become more capable and faster, due to novel types of transistor geometries and functionalities as well as better integration of passive elements, antennas and novel isolation approaches [14].

Hence our circuit design efforts have been largely framed within system-on-chip (SoC) and/or fully-integrated single-chip solutions in which we use a single technology platform (CMOS) in its currently available or projected future forms (Double Gate MOSFET) to

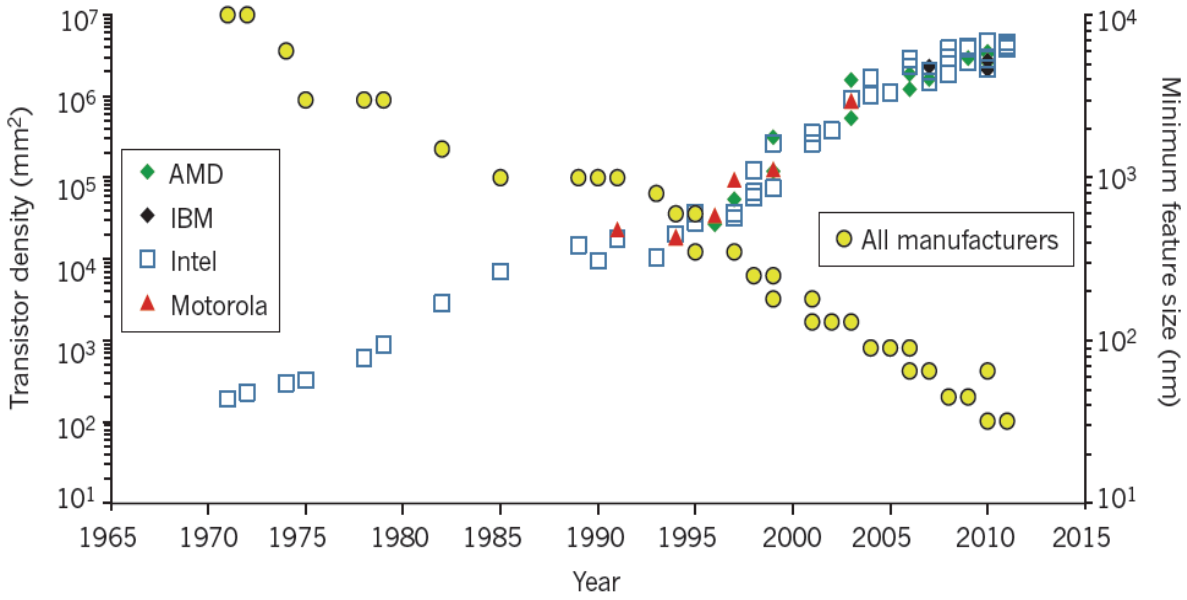


Figure 1.2: The evolution of transistor gate length (minimum feature size) and the concentration of transistors in microprocessors with time. Between the years 1970 and 2011, the gate length of MOSFETs shrank from 10 μm to 28 nm (yellow circles; y axis right), and the number of transistors per mm^2 increased from 200 to over 1 million (diamonds, triangles and squares represent data for the four main microprocessor manufacturers [Motorola (Currently Freescale)]; y axis, left) [6].

implement all necessary digital, analog and mixed-signal system blocks. This approach not only lowers cost and easier to fabricate, it is also the natural conclusion given the fact that Moores scaling is likely to take systems into 0.1-0.5 THz range in clock speed or carrier frequencies [14].

1.3 Novel Multi-Gate & 3D Transistors

As device scaling aggressively continues down to sub-22nm scale, MOSFETs built on Silicon on Insulator (SOI) substrates with ultra-thin channels and precisely engineered source/drain contacts have started to replace conventional bulk devices [22], [23]. Such SOI MOSFETs are built on top of an insulation (SiO_2) layer, reducing the coupling capacitance between the channel and the substrate as compared to the bulk CMOS [23].

The other advantages of an SOI MOSFET include higher current drive and higher speed, since doping-free channels lead to higher carrier mobility [23]. Additionally, the thin body minimizes the current leakage from the source to drain as well as to the substrate, which makes the SOI MOSFET a highly desirable device applicable for high-speed and low-power applications [23]. However, even these redeeming features are not expected to provide extended lifetime for the conventional MOSFET scaling below 22nm and more dramatic changes to device geometry, gate electrostatics and channel material are required. Such extensive changes are best introduced gradually, however, especially when it comes to new materials [23].

Therefore it is still the novel 3D transistor geometries with multi gates and highly optimized electrostatic design and doping landscape, rather than integration of brand new materials such as graphene or paradigm shifts such as spintronics, that is driving transistor development and evolution. Thus in this dissertation, we have also used this very fact as a guideline in research and largely focused on novel multi-gate (double-gate) transistor architecture as the building blocks of novel circuits intended for high-capacity, low-cost, highly integrated wireless solutions mentioned earlier. It is this focus on 3D transistor geometry and electrostatic design [23], rather than novel materials, that make the multi-gate (i.e double, triple, surround) MOSFETs as one of the most suitable candidates for the next phase of evolution in Si MOSFET technology [6]-[10].

Hence, research explained in this dissertation not only incorporates practical considerations and latest trends in systems and circuits aspects, it also includes competitive device elements that will most likely define the next, and final, decade of Moores scaling, making this work quite relevant and interesting for years to come.

1.4 Research Goals & Accomplishments

1.4.1 Research Goals

Based on trends and backdrop provided above, the primary objective of this research is to establish the DG-MOSFET, popularly known as FinFETs, as a better and viable alternative to bulk CMOS in the design of next generation wireless communication integrated circuits operating at radio frequencies. Due to commercial unavailability of the DG-MOSFET technology, this has been verified in academic SPICE models by industry standard computer simulations and/or developing small signal quantitative models and/or qualitative analysis of the various wireless communication circuits. Besides wireless communication, which has been the primary target of the research, these novel circuits are equally suited for applications in satellite communications/navigation, sensor networks and ultra low power wireless body area networks (Fig. 1.1), which are also research directions with extremely large market implication and societal significance.

To fulfill this prime objective and explore novel circuitry, our design efforts have included the following elements which are the building blocks to many electronic systems, not just wireless communication circuits. The circuits investigated include [14]:

- Oscillators (LC, Quadrature and Relaxation)
- OOK Modulators
- Power Amplifiers
- Low Noise Amplifiers
- RF Mixers
- OOK Demodulator/Envelope Detectors
- Charge Pump Phase Frequency Detector

As a product of the primary objective, we have the following specific research goals that define this dissertation:

- Design of ultra-low power non-coherent OOK transciever (TRx) based on DG-MOSFET transistor. Such TRxs are known for their simplicity as well as low-power, compact architecture that is most applicable to our target applications: ultra-short range and extremely efficient (low energy/per transmitted bit) fully integrated wireless data links.

- Design of critical system blocks operating in 60-100 GHz range, such as power amplifiers (PA), low-noise amplifiers (LNA), mixers, oscillators, envelope and charge pump phase frequency detectors, which are found in all types of coherent and non-coherent communication systems, using DG-MOSFET devices. This objective greatly broadens the applicability of the novel circuits developed in this circuit beyond OOK TRx applications.

- Illustration of industry-level design capability and proof-checking of developed system blocks using state-of-the-art CAD design tools and academically available 65 nm CMOS technology platform. In the absence of practically available DG-MOSFET technology at the writing of this dissertation, design of 65 nm CMOS technology kit available via MOSIS academic foundry is to be used to achieve this objective, providing myself and our research group with unique know-how to implement actual chips for a given technology.

1.4.2 Accomplishments

The research establishes DG-MOSFET as an effective and viable alternative to single gate CMOS technology in the design of radio frequency analog integrated circuits mostly in the 60-100 GHz range. Besides several device advantages of DG-MOSFET

over conventional CMOS, the current flag bearer of the semiconductor technology, and described in the next chapter, this research brings out several advantages of DG-MOSFETs in the radio frequency analog circuits domain. Although previous attempts have been successfully made in the design of digital and memory circuits with DG-MOSFETs, no detailed and focussed attempts have been made prior to this work to establish the viability of DG-MOSFET in the design of the radio frequency analog integrated circuits which finds application in wireless communication among others. The specific accomplishments of this research for different radio frequency integrated circuits are as follows:

Oscillators:

- A more lenient oscillatory criterion of common mode DG-MOSFET based LC oscillator than conventional CMOS is analyzed quantitatively.
- An independent mode DG-MOSFET LC Voltage Controlled Oscillator (VCO) is designed in which the voltage controls the oscillation frequency via the back gate bias of the DG-MOSFETs without the requirement of any MOS varactors as needed in single gate conventional CMOS for voltage control of the oscillation frequency thus making the circuit more compact.
- Qualitatively analyzed and verified through simulation a new formulation of the voltage controlled characteristic of the DG-MOSFET LC oscillator.
- Designed the DG-MOSFET LC quadrature oscillator with reduced transistor count from eight in conventional CMOS to four in the DG-MOSFET version, enabling faster performance by reducing parasitics as well as area usage.
- A novel DG-MOSFET based relaxation oscillator is designed in which the comparator circuit required in conventional CMOS is omitted by utilizing back gate

biasing of the DG-MOSFET, making the circuit faster as well as area and power efficient.

- The voltage controlled operation of the relaxation oscillator is demonstrated in addition to the existing current-controlled oscillation operation. The voltage controlled operation aids in high precision frequency tuning, a feature not possible in conventional CMOS based current-controlled relaxation oscillator.

- Through computer simulation verified a better or comparable phase noise performance than CMOS for all the DG-MOSFET oscillators.

OOK Modulator:

- A novel area efficient single DG-MOSFET modulator is designed. A second high-threshold DG-MOSFET is added for better switching operation than CMOS owing to strict channel control.

Power Amplifier:

- Established the adaptive gain tuning capability of DG-MOSFET without any additional transistors for power efficient applications.

- Through simulation verified better or comparable performance metrics of DG-MOSFET power amplifiers compared to CMOS and other III-V technology alternatives.

Low Noise Amplifier:

- Emphasized the area efficiency of the common source inductive degeneration Low Noise Amplifier (LNA), the most widely used LNA topology, via quantitative small signal modelling.

- Verified the gain switching of the DG-MOSFET LNA without any additional transistors, making the circuit much faster and area efficient compared to CMOS.
- Through simulation verified better or comparable performance metrics of DG-MOSFET LNAs compared to CMOS and other III-V technology devices.

Envelope Detector:

- Designed an envelope detector based on two DG-MOSFETs.

RF Mixer:

- Developed the analytical verification of the single DG-MOSFET RF Mixer operation.
- Analysed a novel bias optimization technique for DG-MOSFET RF Mixer.

Charge Pump Phase Frequency Detector:

- Analyzed through computer simulations, DG-MOSFET to be a better alternative for dead zone avoidance in phase locked loops.

OOK TRx in 65 nm RF CMOS:

- Apart from this accomplishments with DG-MOSFETs, in this research a power efficient, high bandwidth OOK transceiver (TRx) in 65 nm RF CMOS technology from IBM in the 60-100 GHz range for on-chip network applications is also implemented. This helped to develop the know-how to design and simulate commercial mm-wave CMOS circuits using industry-grade software and analysis tool.

1.5 Dissertation Organization

In the following, we describe the general organization and structure of the chapters making up this dissertation work.

- Chapter 2 reports the necessary background of MOS technology, DG-MOSFET device, microwave fundamentals and wireless communication.
- Chapter 3 reports the research on DG-MOSFET non-coherent OOK transmitter, which include both the LC and relaxation oscillators, OOK Modulator and Power Amplifiers.
- Chapter 4 reports the research on DG-MOSFET non-coherent OOK receiver, which include the LNA and Envelope Detector.
- Chapter 5 reports the research on DG-MOSFET RF mixer primarily used for down conversions in coherent receivers. It also reports the research on DG-MOSFET Charge Pump Phase Frequency detector which is also used for coherent detection in receiver.
- Chapter 7 reports an extended comparative research onto an OOK TRx design in commercial 65 nm RF CMOS technology from IBM.
- Chapter 8 reports on the conclusion and future work of the dissertation.

1.6 Analysis & Design Tools

The technologies and simulators used in the analysis and design of the transceiver (TRx) circuits in DG-MOSFET are tabulated in this section. The ASU PTM FinFET models [26] and UFDG Model [27] are used to investigate the characteristics of the novel circuits. It should be noted only the technologies reported in this dissertation are mentioned. For instance, the work on Power Amplifier and the 60 GHz Low Noise Amplifier have been done also at ASU PTM 32 nm FinFET technology and published in [16] and [2] respectively, however not reported in the dissertation and hence not mentioned in Table 1.1.

The work in Chapter 6 on OOK TRx design with commercial CMOS has been implemented using the 65 nm RF CMOS technology from IBM. The different circuit blocks used in the design of the TRx are elucidated in Table 1.2.

Table 1.1: Analysis & Design Tools for DG-MOSFET

TRx Circuit	Technology	Simulator
LC Oscillator	ASU PTM 32 nm FinFET	Synopsys HSPICE RF
Relaxation Oscillator	UFDG Model	UFDG SPICE Simulator
OOK Modulator	ASU PTM 32 nm FinFET	Synopsys HSPICE RF
Power Amplifier	ASU PTM 45 nm FinFET	Synopsys HSPICE RF
Low Noise Amplifier (60 GHz & 90 GHz)	ASU PTM 45 nm & 32 nm FinFET respectively	Synopsys HSPICE RF
Envelope Detector	ASU PTM 45 nm FinFET	Synopsys HSPICE RF
RF Mixer	UFDG Model	UFDG SPICE Simulator
Charge Pump Phase Frequency Detector	ASU PTM 32 nm & 45 nm FinFET	Synopsys HSPICE

Table 1.2: Analysis & Design Tools for RF CMOS

TRx Circuit	Technology	Simulator
LC Oscillator+OOK Modulator	65 nm RF CMOS	Cadence SpectreRF
Power Amplifier	65 nm RF CMOS	Cadence SpectreRF
Low Noise Amplifier	65 nm RF CMOS	Cadence SpectreRF
Envelope Detector	65 nm RF CMOS	Cadence SpectreRF

2 Background

2.1 MOSFET Fundamantals

2.1.1 MOSFET Operation

Before proceeding to DG-MOSFET, a short description of its predecessor, the conventional single gate MOSFET is hereby provided. Fig. 2.1 illustrates a single gate conventional MOSFET. The following points are easy to understand on the principle of operation of an n-channel MOSFET.

- Initially, the two terminals, drain and source are electrically isolated and hence there is no net flow of charge, no current, and the MOSFET is switched off
- The diffusion between electrons and holes results in recombination and thus depletes away most mobile charges in the junction region and results in a built-in electric field to be established, that counters further diffusion, making both the source and drain region electrically isolated from the substrate.
- When a positive voltage is applied at the gate minority electrons starts accumulating at the substrate beneath the oxide layer due to vertical electric field established. Thus electron density can rise significantly in this top section of silicon right next to the oxide interface, as compared to bulk of the body of MOSFET, resulting in the formation of a channel layer between source and drain contacts. Due to relatively small gate bias, this regime is called weak inversion.
- As the inversion proceeds (gate become more positive in an n-MOSFET), the electrons from both the source and drain starts appearing in the substrate and populates beneath the gate at the uppermost surface of the substrate. The transistor is now in strong inversion.

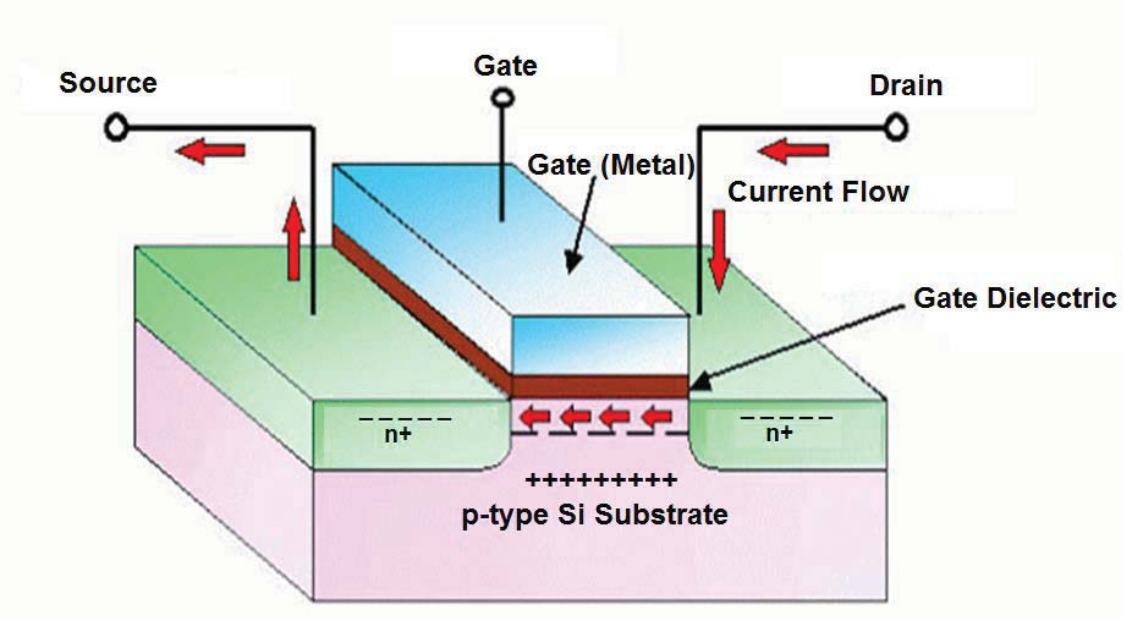


Figure 2.1: nMOSFET device structure and electrical contacts [7].

- The gate voltage at which an inversion channel is just formed is known as the threshold voltage.
- As the gate voltage is increased further, more and more electrons starts accumulating at the channel and simultaneously, a potential difference applied between the drain and source determines the flow of current in the channel along with the gate voltage. Thus the drain current is a function of two voltages.
- As the drain source voltage increases further, the potential difference between gate and silicon is reduced, and the vertical field effect is weakened, thus at the drain end of channel inversion is weakened or the channel is 'pinched off'.
- After the channel gets pinched off, the drain current ceases increasing with the drain source voltage and becomes almost constant. This is called the saturation region.

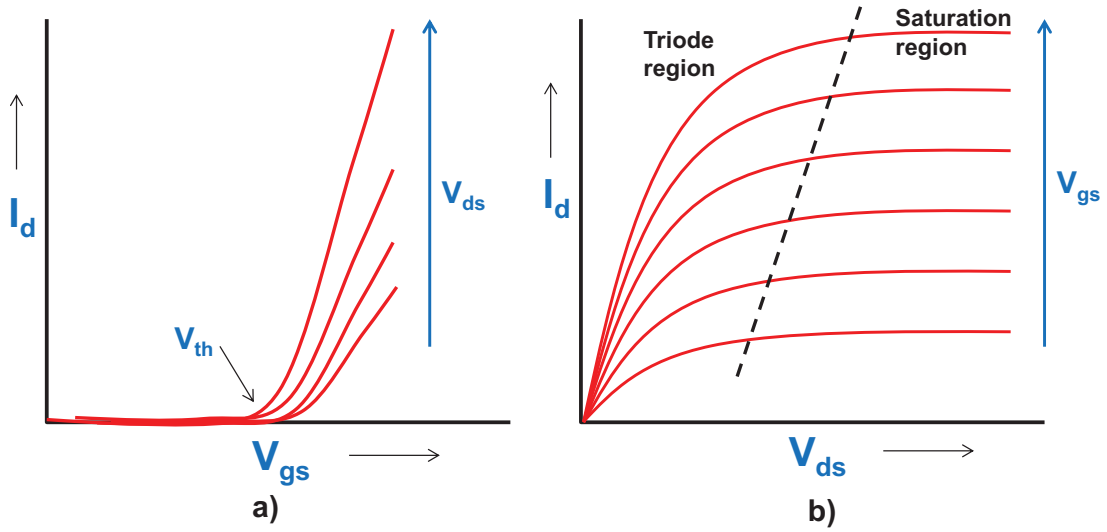


Figure 2.2: The MOSFET I-V Characteristics a) I_d-V_{gs} b) I_d-V_{ds}.

2.1.2 I-V Characteristics

As informed in the earlier section, the drain current, I_d is function of two voltages, the gate-source voltage and the drain-source voltage. The I_d for an nMOS is thus given as [28],

$$I_d = \mu_n C_{ox} \frac{W}{L}[(V_{gs} - V_{th})V_{ds} - \frac{1}{2}V_{ds}^2] \tag{2.1}$$

Here, μ_n is the mobility of charge carrier (electron here), C_{ox} is the capacitance of the insulating oxide layer, W & L are width and length of the MOSFET respectively. The gate-source voltage, drain-source voltage and the threshold voltage are given by V_{gs}, V_{ds} & V_{th} respectively. The voltage term, V_{gs} - V_{th} is called the overdrive voltage and $\frac{W}{L}$ is the aspect ratio of the device. At saturation, $V_{ds} = V_{gs}$ - V_{th}, therefore, eqn. (2.1) can be written as,

$$I_{dmax} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{gs} - V_{th})^2 \tag{2.2}$$

If $V_{ds} \leq V_{gs}$ - V_{th}, the device operates in the active or triode region. In this region, when, $V_{ds} << V_{gs}$ - V_{th}, eqn. (2.1) reduces to,

$$I_d = \mu_n C_{ox} \frac{W}{L}(V_{gs} - V_{th})V_{ds} \tag{2.3}$$

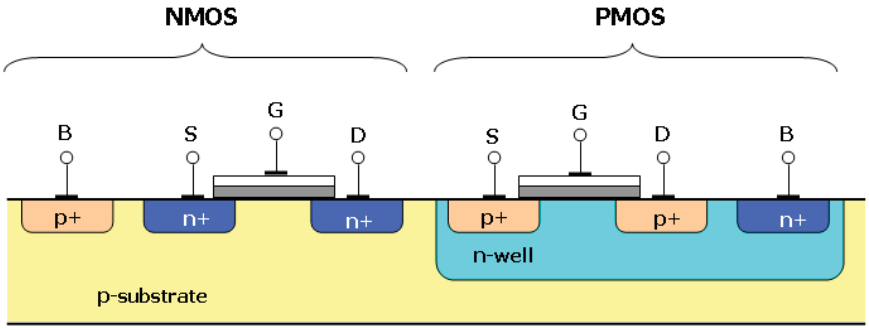


Figure 2.3: The basic CMOS device architecture [8].

The drain current becomes a linear function V_{ds} for a fixed gate-source voltage and the transistor behaves as a resistor following Ohm's law. In Fig. 2.2a & b, the I_d-V_{gs} & I_d-V_{ds} characteristics are illustrated respectively.

2.1.3 Complementary MOS Architecture

In complementary MOS (CMOS) technologies, both nMOS and pMOS transistors are utilized and operated in tandem. The pMOS and nMOS devices are be fabricated in the same wafer or substrate. Hence, one device type is placed on a 'local substrate' usually called a 'well'. In most conventional bulk MOSFET of today's processes, the pMOS device is fabricated in an n-well. The n-well must be connected to a potential such that the source/drain junction always remain reverse biased under all conditions [28]. This is to ensure the source/drain junction does not create and act as a diode in forward biased. In most circuits n-well is tied to the positive supply voltage. Similarly for the nMOS the p-substrate is connected to the ground. This is illustrated in Fig. 2.3.

The two most essential features of CMOS devices are immunity to high noise and low static power consumption (ideally zero). Since one transistor of the pair is always off, the series combination consumes significant power only momentarily when switching between on and off states [8]. Consequently, CMOS devices do not create as much waste heat

as other forms of logic during static operation such as NMOS or transistor-transistor logic (TTL). They usually have some standing current even when not switching state [8]. CMOS also allows a high concentration of logic functions on a chip, since transistors are typically the smallest element of gate-controlled switching and takes less space than resistors [8]. Another important advantage of CMOS is scalability and is discussed later in the section.

2.1.4 Power Dissipation

The power dissipation in CMOS comes from two components. The static dissipation which arises due to non-ideal circumstances such as [28],

- subthreshold conduction through OFF transistors
- tunneling current through gate oxide
- leakage through reverse-biased diodes (p-n junctions formed between source/drain and substrate)
- contention current in ratioed circuits

Dynamic dissipation is due to

- charging and discharging of load capacitances arising out of transistor switching
- short circuit current while both PMOS and NMOS networks are partially ON

The static power dissipation is a serious concern in sub-32 nm devices and among other reasons, the mitigation to this led to the development of advanced CMOS devices [28].

The subthreshold leakage current responsible for static power dissipation during transistor OFF state is given as [29],

$$I_{d_{subth}} = K.e^{(\frac{(V_{gs}-V_{th})q}{nkT}}(1 - e^{\frac{-qV_{ds}}{kT}}) \tag{2.4}$$

where K is a process dependent constant [29]. The tunneling current through gate oxide is caused by carriers tunneling through a classically forbidden energy barrier [30]. Ideally the reverse biased p-n junction between source/drain and substrate will not conduct any current. However, a small amount of current flows due to minority carriers resulting in static power dissipation.

The average power dissipation in any CMOS circuit can be written as [28],

$$P_{av} = \frac{1}{T}\int_0^T i_{supply}(t)V_{supply} \tag{2.5}$$

The primary source of dynamic dissipation is charging of the load capacitance. Suppose a load C_L is switched between the supply, V_{DD} and GND at an average frequency f_{sw}. Over time T, load is charged and discharged Tf_{sw} times. In one complete charge/discharge cycle, a total charge of $Q = CV_{DD}$ is transferred between V_{DD} and GND. Now the average dynamic power dissipation can be written from eqn. 2.5,

$$P_{dyn} = \frac{V_{DD}}{T}\int_0^T i_{DD}(t) \tag{2.6}$$

Taking the integral of the current over the interval T, the total charge delivered during time T is,

$$P_{dyn} = \frac{V_{DD}}{T}[T f_{sw} C V_{DD}] = C V_{DD}^2 f_{sw} \tag{2.7}$$

Therefore, the higher the number of switching events, the greater the dynamic power consumption.

2.1.5 MOSFET Scaling

The scalability of MOSFET in CMOS architecture is one of the primary reason that CMOS became the most dominant technology to be implemented in analog/digital VLSI chips. The ideal scaling theory follows three rules [28]:

- All lateral and vertical dimensions are reduced by α.

- The supply and threshold voltages are reduced by α.
- All the doping levels are increased by α.

The drain current in eqn.(2.2) following the above rules can be rewritten as,

$$I_{dmax,scaled} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs} - V_{th})^2\frac{1}{\alpha} \tag{2.8}$$

The current capability of the transistor drops by a factor of α. The same result applies for the drain current in the triode region too. The advantage of scaling however lies in the reduction of capacitances and power dissipation. The total channel capacitance is written as,

$$C_{ch,scaled} = \frac{1}{\alpha}WLC_{ox} \tag{2.9}$$

The power goes down by a factor of α^2.

However as we go down in technology, there are serious consequences with scaling and the effects are discussed in the next section.

2.2 Evolution to Multigate MOSFETs

2.2.1 Limitations of CMOS

One of the fundamental limits in mixed-signal (digital & analog) CMOS circuit design is the intrinsic gain possible through a single transistor, which is determined by the ratio of transconductance g_m (ratio of output current to input voltage) over output conductance g_{ds} (the device's capacity to shunt its own current to ground or to 'steal useful signal intended for the load at the output) [31]. In CMOS, from the 250 nm to the 45 nm node, this ratio g_m/g_{ds} has decreased from 15 to 5 due to an increased g_{ds}. An extrapolation for 10 nm technology leads to an intrinsic gain close to unity. Moreover, even if we can make gate lengths so small, there are other requirements for proper scaling. From fabrication point of view an oxide thickness t_{ox} of around 1 nm is required for the 10 nm node to allow

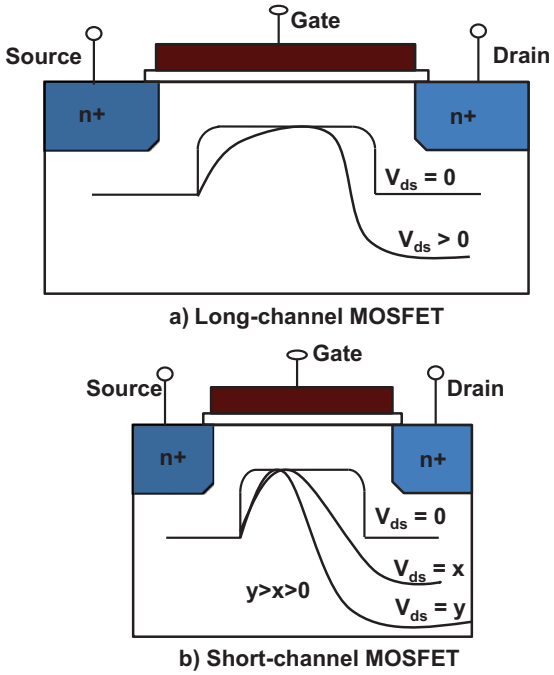


Figure 2.4: Band Bending in Long channel & Short channel MOSFETS

sufficient channel control via the gate [31]. Since 1 nm corresponds to just a few atomic layers, further reduction of t_{ox} is difficult from a gate leakage, noise, and process variation point of view [31].

Another serious limitation of CMOS lies in technology scaling as we have approached the sub 22 nm technology. The ideal scaling properties described in the earlier section deviates considerably. The supply voltage and the MOS threshold voltage cannot be scaled as rapidly as device dimensions. This gives rise to small-geometry effects. The five factors responsible for these effects are as follows [28]:

- The electric fields tend to increase because the supply voltage has not scaled proportionally.
- The built in potential [28] is neither scalable nor negligible.
- The depth of source/drain junctions cannot be reduced easily.

- The mobility decreases as the substrate doping increases, which is necessary to reduce the extent of depletion zones in the p-n junction at the source and drain ends of the channel. Thus mobility, and hence the current drive is reduced as doping is raised to scale devices down.

- The slope of log(I_d)-V_{gs} curves below threshold voltage, which indicates how sensitive is device to ON/OFF transitions, is not scalable.

As the name suggests, these effects are not prevalent in long channel MOSFETs. In long channel MOSFETs, as the proportion is well maintained, the band bending due to increasing V_{ds} does not encroach much into the channel region as can be observed in Fig. 2.4a. However, in short channel MOSFETs, when V_{ds} increases, there is more band bending near drain due to the drain field encroaching into the channel region. The stronger electric field corresponding to a higher V_{ds}, penetrates deeper into the channel causing more pronounced short channel effects (SCEs). As a result of which, the band continues to bend near the drain region to an extent such that, the band lowers and becomes narrower (Fig. 2.4b). The lowering of the band is called Drain Induced Barrier Lowering (DIBL) and results in the decrease of threshold voltage in MOSFETs. The narrower band can results in the electron to zap across from source to drain even in the absence of any gate-source voltage. In ultra-small gates (<100nm), this leads to 'band-to-band tunneling', which is undesirable as it leads to loss of gate-controlled operation (or reduction in g_m) for a MOSFET. Similarly, ultra-thin gate insulators demanded by scaling in nano-scale MOSFETs become ineffective due to quantum mechanical tunneling of electrons between channel and gate, causing additional 'gate leakage. This gate leakage can happen even when CMOS logic are in static state, thus can have severe consequences for power dissipation.

2.2.2 Advanced CMOS

The remedies to these drawbacks are described in the following subsections:

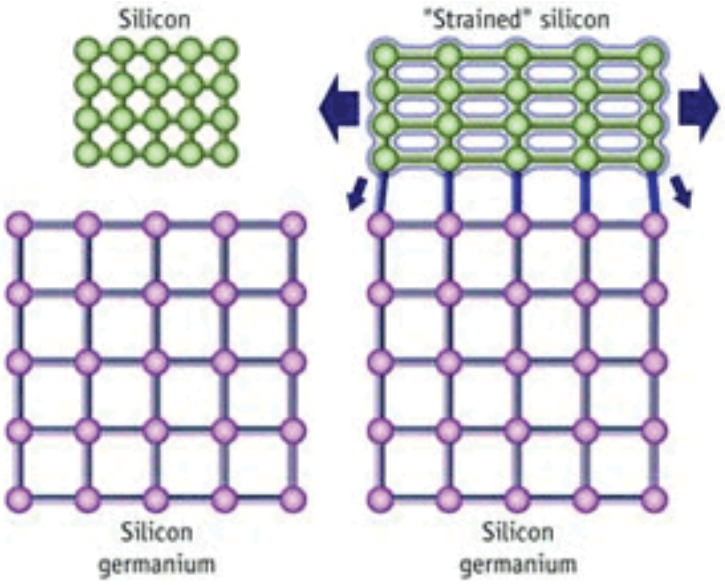


Figure 2.5: Biaxial straining of Si by SiGe [9].

2.2.2.1 Strained Silicon

This enhances the carrier transport properties in Si transistors, particularly by enhancing mobility in the channel. A layer of Si is placed over a SiGe substrate that has a higher lattice constant. As Si layer align with underlying SiGe, the interatomic distance between the Si atoms become stretched due to higher lattice constant of SiGe, thereby leading to tensile strain in Si. The modification leads to a lower scattering probability and thus, to a higher mobility in the channel which also increases the drift velocity. The electron mobility has been enhanced by 70 % leading to a speed improvement around 30 % [32]. The power consumption also reduces decently. An advanced biaxial strained Si architecture can be viewed from Fig. 2.5. However, this technique requires complex growth procedures before CMOS fabrication, thus making it not a top choice to extend CMOS performance in the long run [9].

2.2.2.2 SOI Technology

A further option for enhanced channel length scaling is Silicon on Insulator (SOI) technology, in which a relatively thick oxide isolation layer separates the thin active device layer at the top side from the main substrate. Thus, the resistivity of the active layer determining V_{th} and the resistivity of the main substrate can be chosen independently. Consequently, relatively high resistivity can be chosen for the bulk substrate without degrading V_{th} [31]. This results in reduced parasitics and leakage currents in the substrate. High speed performance improvement in the order of 30% are typically achieved with SOI but at the expense of self-heating and increased reliability issues resulting from reduced thermal conductivity. This technique is very beneficial also for passive RF elements such as inductors and capacitors typically having a strong coupling to the lossy substrate because of their large areas. An SOI isolation layer also reduces static leakage in addition to AC losses, thus alleviates power dissipation as compared to conventional bulk CMOS [31].

2.2.2.3 Multigate MOSFETs

Another promising candidate capable of enhancing the speed and the scaling properties of CMOS architecture is multi-gate MOSFETs. Different varieties of multi-gate MOSFETs are illustrated in Fig. 2.6, which shows that multiple gates can be implemented in many fashion using advanced CMOS fabrication. In Fig. 2.7, different structural parameters of various multi-gate MOSFETs are compared and their implications for device performance are explored.

Nonclassical CMOS includes those advanced MOSFET structures which, combined with material enhancements, such as new gate stack materials, provides a path to scaling CMOS to the end of the roadmap [33]. The scaling challenges for digital applications include controlling leakage currents and SCEs, increasing drain saturation current by reducing the power supply voltage, and maintaining control of device parameters which

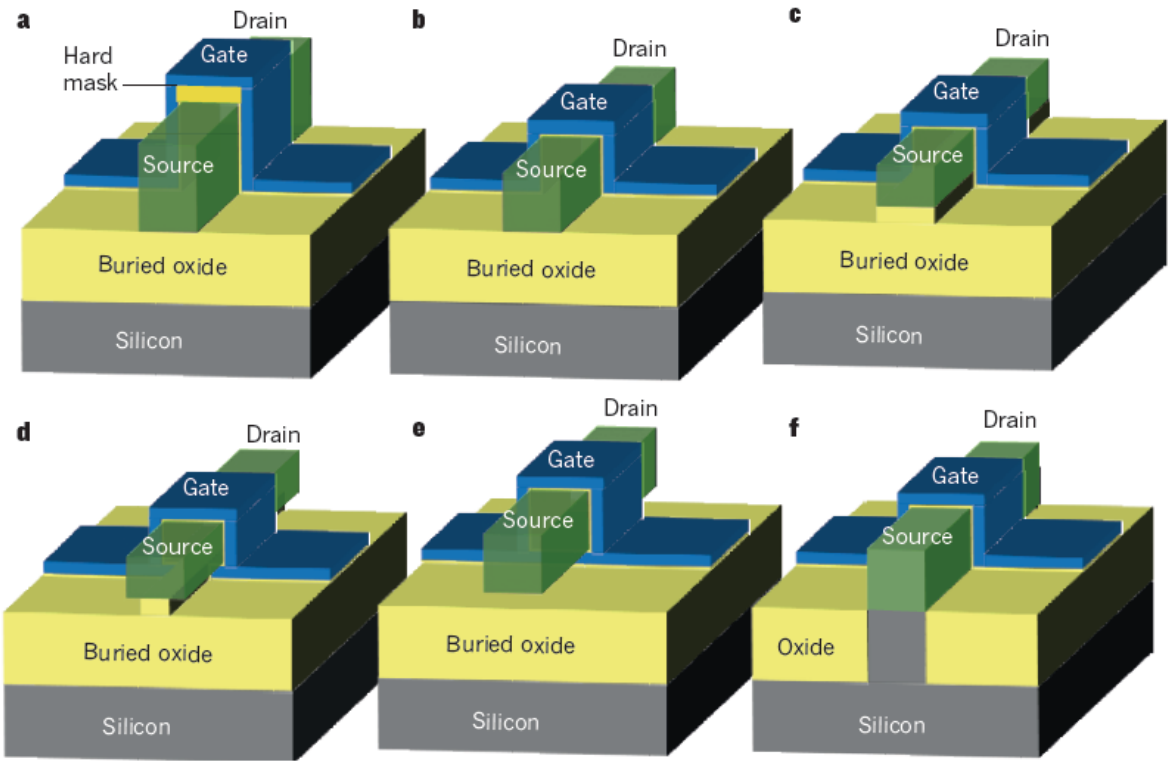


Figure 2.6: Types of multigate MOSFET. The various ways in which the gate electrode can be wrapped around the channel region of a transistor are shown. a) A silicon-on-insulator (SOI) fin field-effect transistor (FinFET). b) SOI Tri-gate MOSFET. Channel control is applied from three sides of the device c) SOI π-gate MOSFET. Channel control is improved over the tri-gate MOSFET shown in b since the electric field from the lateral sides of the gate exerts some control on the bottom side of the channel. d) SOI Ω-gate MOSFET. The gate control of the bottom of the channel region is better than in the SOI π-gate MOSFET. e) SOI gate-all-around MOSFET. Channel control is applied from all four sides of the device. f) A bulk tri-gate MOSFET. Channel control is applied from three sides of the device. In this case, there is no buried oxide underneath the device [6].

include threshold voltage and leakage current, both intra and inter chip [33]. The challenges additionally include sustaining linearity, high power-added efficiency, low noise figure, good transistor matching and large transit and maximum frequencies for analog/mixed-signal/RF applications [33]. All these concepts are elaborated in section 2.4. Some examples of multigate MOSFETS can be found in [34]-[39].

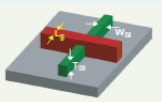
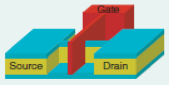
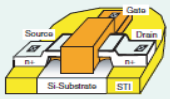
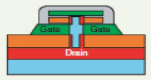
	Multiple Gate MOSFETs				
	N-Gate ($N > 2$)		Double-gate		
Device					
Concept	Tied gates (number of channels >2)	Tied gates, side-wall conduction	Tied gates planar conduction	Independently switched gates, planar conduction	Vertical conduction
Application/Driver	HP, LOP, and LSTP CMOS [2]	HP, LOP, and LSTP CMOS [2]	HP, LOP, and LSTP CMOS [2]	LOP and LSTP CMOS [2]	HP, LOP, and LSTP CMOS [2]
Advantages	• Higher drive current • 2 × thicker fin allowed	• Higher drive current • Improved subthreshold slope • Improved short channel effect	• Higher drive current • Improved subthreshold slope • Improved short channel effect	• Improved short channel effect	• Potential for 3D integration
Particular Strength	• Thicker Si body possible	• Relatively easy process integration	• Process compatible with bulk and on bulk wafers • Very good control of silicon film thickness	• Electrically (statically or dynamically) adjustable threshold voltage	• Lithography independent L_g
Potential weakness	• Limited device width • Corner effect	• Fin thickness less than the gate length • Fin shape and aspect ratio	• Width limited to <1 μm	• Difficult integration • Back-gate capacitance • Degraded subthreshold slope	• Junction profiling difficult • Process integration difficult • Parasitic capacitance • Single-gate length
Scaling Issues	• Sub-lithographic fin thickness required	• Sub-lithographic fin thickness required	• Bottom gate larger than top gate	• Gate alignment	• Si vertical channel film thickness
Design Challenges	• Fin width discretization	• Fin width discretization	• Modified layout	• New device layout	• New device layout
Gain/Loss in Layout compared to Bulk	• No difference	• No difference	• No difference	• No difference	• Up to 30% gain in layout density
Advantage in I_{on}/I_{off} compared to Bulk	• Improved by 20–30% (from MASTAR assuming $E_{eff}/2$ and S = 65 V/decade)	• Improved by 20–30% (from MASTAR assuming $E_{eff}/2$ and S = 65 V/decade)	• Improved by 20–30% (from MASTAR assuming $E_{eff}/2$ and S = 65 V/decade)	• Potential for improvement	• Improved by 20–30% (from MASTAR assuming $E_{eff}/2$ and S = 65 V/decade)
Advantage in CV/I compared to Bulk	• Lowered by 15–20% (from MASTAR assuming $E_{eff}/2$ and S = 65 V/decade)	• Lowered by 15–20% (from MASTAR assuming $E_{eff}/2$ and S = 65 V/decade)	• Lowered by 15–20% (from MASTAR assuming $E_{eff}/2$ and S = 65 V/decade)	• Potential for improvement	• Lowered by 15–20% (from MASTAR assuming $E_{eff}/2$ and S = 65 V/decade)
Analog Suitability G_m/G_d advantage compared to Bulk	• Potential for improvement	• Potential for improvement	• Potential for improvement	• Potential for improvement	• Potential for improvement

Figure 2.7: Multiple-gate Nonclassical CMOS Technologies [10].

2.3 DG-MOSFET Basics

The simpler and relatively easier to fabricate among the multigate MOSFET structures (MIGFET, Π-MOSFET and so on) is the Double Gate MOSFET (DG-MOSFET) (Fig. 2.8a). The DG-MOSFET architecture can efficiently control the channel from two sides instead of one as in planar bulk MOSFETs. The device works in two different modes, the common mode, when the gates are joined and independent mode, when the gates are separated. The $I_D - V_{fg}$ characteristics of the independent mode along with the common mode (in dotted lines) of such a device are observed in Fig. 2.8b. The advantages of DG-MOSFET as a device over conventional CMOS can be summarized as follows:

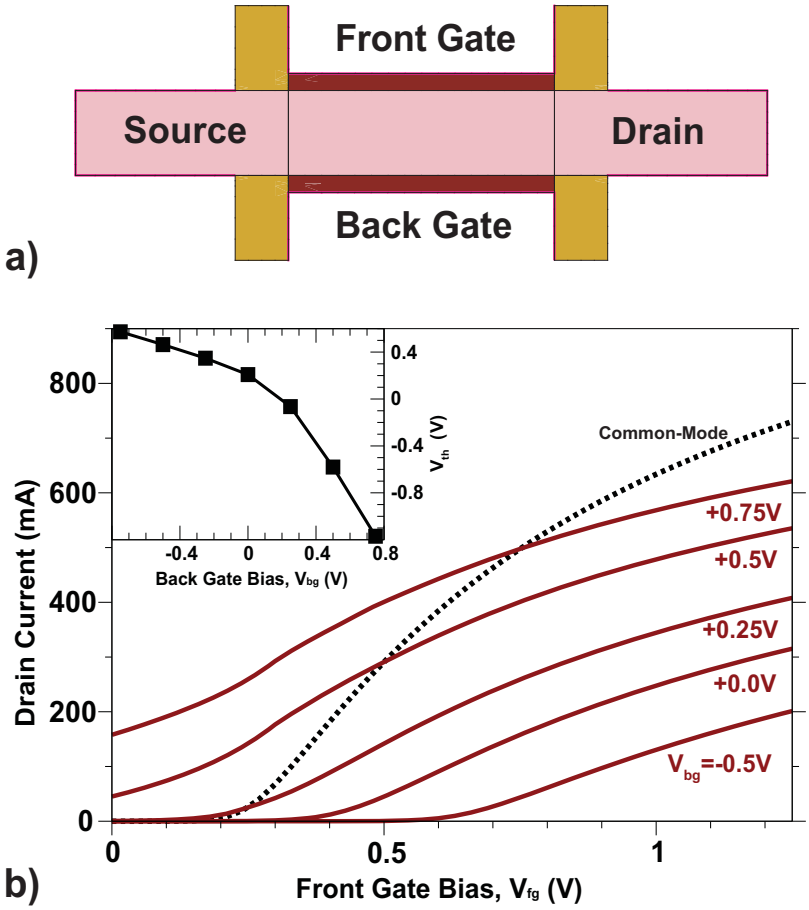


Figure 2.8: a) The generic DG-MOSFET device structure. b) I_D-V_{fg} characteristics of an n-type Independent and Common Mode DG ($V_{bg} = V_{fg}$) transistors. The inset shows the resulting shift in the front gate threshold.

- Excellent control of SCEs due to presence of two gates and ultra-thin body,
- Lower subthreshold leakage current due to reduced SCE,
- Higher ON (drive) current due to two gates, and
- Dual channel control advocates use of thicker gate oxide which in turn reduces gate leakage current.

The above advantages are primarily applicable to the common (symmetric) gate operation. When applied to construct different circuits in this mode many other advantages come into sight. A couple of them are demonstrated in the dissertation. One such is a less stringent stability criterion for Oscillator and the other is the better area efficiency of a Common Source Inductive Degeneration LNA. On the other hand, the advantages entitled to the independent mode primarily materialize through circuit applications and are as follows,

- Implementation of tunable circuits, and
- Circuits with reduced transistor count

These two advantages are also demonstrated in various circuits throughout the dissertation. The first one is demonstrated by the frequency tuning of Voltage Controlled Oscillator and the gain tuning of the Power Amplifier & the Low Noise Amplifier. The second advantage is demonstrated with the design of quadrature oscillator, OOK Modulator, Envelope & Phase Frequency Detectors.

The first structure of DG-MOSFET appeared in [40]. Later, many advanced articles on DG-MOSFET structures [6], [24], [25], [10], [41] have been proposed to improve engineering of the channel electrostatics and to provide independent control of two isolated gates for low-power analog and mixed-signal applications. Some of these architectures are compared in Fig. 2.7 with other multi-gate devices. The three most widely used structures are the DG-FinFETs and DG-MOSFETs (Planar & Vertical). Although they have the similar electrostatic and I-V characteristics, the primary difference between these three lies in the direction of flow of current. This is illustrated in Fig. 2.9.

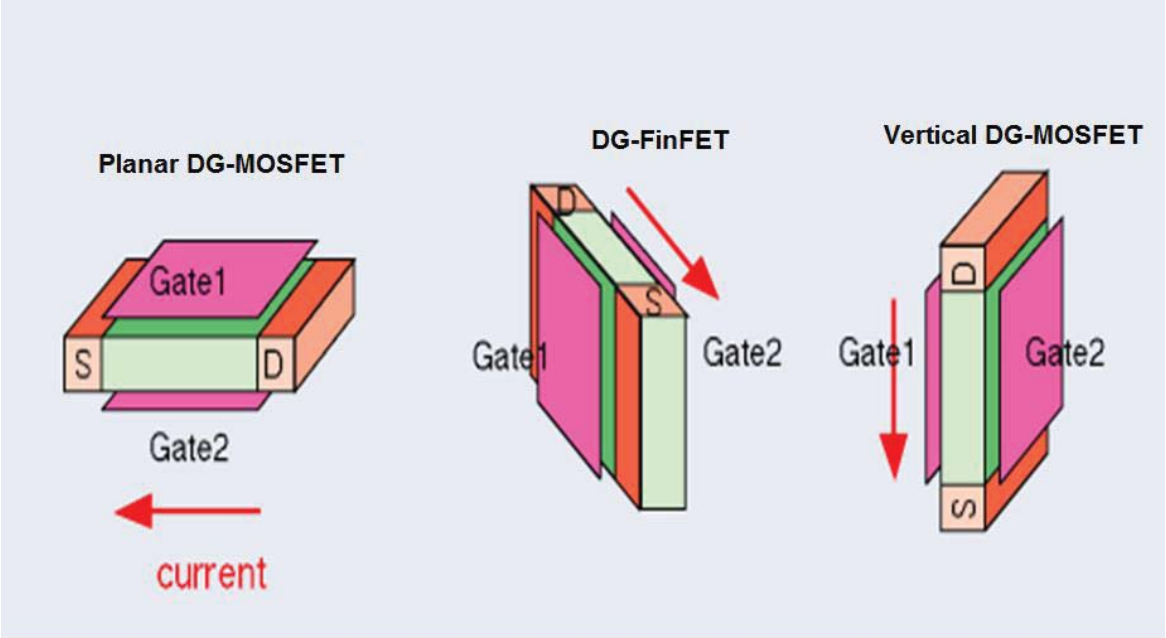


Figure 2.9: The three different varieties of DG-MOSFET. The difference lies in the direction of flow of electric current in the channel of the transistor [11].

2.3.1 Device Models

A plethora of DG-MOSFET charge models have been proposed over the last ten years. In [42] analytical expressions for terminal charges of an independent-gate asymmetric DG-MOSFET are derived. The new charge model is C_∞ continuous, which is valid for all bias conditions without involving charge-sheet approximation. This has been accomplished in this work by developing the symmetric linearization method in the form without requiring identical boundary conditions at the two $SiSiO_2$ interfaces allowing the volume inversion in the DG-MOSFET channel [42].

Another compact model for currents in short channel symmetric DG-MOSFETs is presented which considers a doped silicon layer [43]. In this work, the mobile charge density is computed using analytical expressions obtained from surface potential modeling and the difference of potentials at the surface and at the center of the Si doped layer

without solving any transcendental equations. Analytical expressions for the currentvoltage characteristics are presented here as function of silicon layer impurity concentration, silicon layer thickness, including variable mobility and gate dielectric. The SCEs included are velocity saturation, DIBL, V_T roll-off, channel length shortening and series resistance.

This paper [44] presents an analytic potential model for long-channel symmetric and asymmetric DG-MOSFETs. The model is derived without the charge-sheet approximation, rigorously from the exact solution to Poissons and current continuity equation. This work has accounted the volume inversion in the subthreshold region maintaining the physics. The resulting analytic expressions of the draincurrent, terminal charges, and capacitances for long channel DG-MOSFETs are continuous in all operation regions making it suitable for compact modeling. As no fitting parameters are invoked throughout the derivation, the model is physical and predictive.

A continuous analytic current-voltage (I-V) model for DG-MOSFETs is presented in [45]. It is also derived without the charge-sheet approximation from closed-form solutions of Poissons equation, and current continuity equation. The entire I-V_{ds}, I-V_{gs} characteristics for all regions of MOSFET operation: linear, saturation, and subthreshold, are covered under one continuous function, making it ideally suited for compact modeling. This model readily depicts "volume inversion" in symmetric DG-MOSFETs a distinctively noncharge-sheet phenomenon that cannot be reproduced by standard charge-sheet based I-V models, preserving the physics. It is also shown that the IV curves generated by the analytic model totally agrees with two-dimensional numerical simulation results for all ranges of gate and drain voltages [45].

Besides these, several other models on DG-MOSFET device characteristics have been proposed [46]-[50]. The models proposed focussing on analog, mixed signal and RF circuit applications include [51]-[54].

In any case, analytical models have limited applicability to full-circuit design and optimization because of the dominance of full 3-D electrostatics, complex field and doping dependence of mobility, and the large number of transistors involved in the circuits being designed. Thus, analytical models have been sparingly used in this work that mostly resort to full commercial grade TCAD simulators with finely tuned material and mobility models. In case they have been used, the objective is simply to gain insight.

2.3.2 Small Signal Circuit Models

Since the primary objective of the dissertation is analog/RF circuit design, the analytical small-signal circuit model for DG-MOSFETs is achieved in this section in a simple fashion modified from single gate CMOS models [55]. This is aimed to gain additional insight to the simulated DG-MOSFET behavior. The actual details of these DG-MOSFET circuit models used in commercial software may be much more complex, such as involving parasitics, and often includes the established collaboration between by academia & industry over many years.

Common-Source Input Resistance: The input resistance is ideally infinite because of capacitive effect at the gate terminal. However, in bulk CMOS, because of ultra thin gate oxide, the presence of leakage current makes the resistance to an extent non-infinite. This is not the case for DG-MOSFET where we can afford to use thicker gate oxide as explained earlier, which prevents the leakage.

Common-Gate Input Resistance: Initially disabling the transconductance, the contribution of test current

$$i_{t1} = \frac{v_{test}}{r_{dstot} + R_L} \tag{2.10}$$

where $r_{dstot} = r_{dsf} + r_{dsb}$. Rewriting eqn. (2.10) ,

$$i_{t1} = \frac{v_{test} g_{dstot}}{1 + R_L g_{dstot}} \tag{2.11}$$

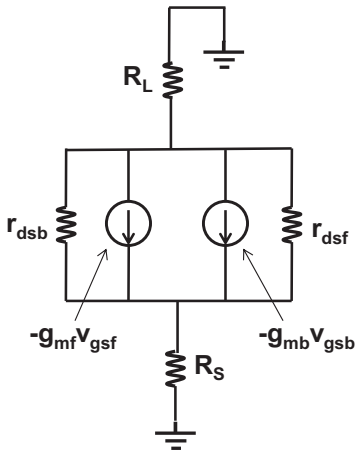


Figure 2.10: Simple Small Signal Circuit Model for DG-MOSFET.

Next, the test voltage source is disabled and the current due to g_{mtot} is added to the current flowing through r_{dstot}.

$$i_{t2} = -g_{mtot}v_{gs} - i_{t2}R_L g_{dstot} \tag{2.12}$$

After a few algebraic steps,

$$i_{t2} = \frac{g_{mtot}v_{test}}{1 + R_L g_{dstot}} \tag{2.13}$$

Therefore, the total current ($i_t = i_{t1} + i_{t2}$) is

$$i_t = \frac{v_{test}(g_{mtot} + g_{dstot})}{1 + R_L g_{dstot}} \tag{2.14}$$

Hence, the resistance looking into the source ($r_{in} = v_{test}/i_t$) is,

$$r_{in} = \frac{1 + R_L g_{dstot}}{g_{mtot} + g_{dstot}} \tag{2.15}$$

Assuming $R_L g_{0tot} \ll 1$, the resistance looking into the source can be approximated as,

$$r_{in} \approx \frac{1}{g_{mtot} + g_{dstot}} \tag{2.16}$$

When $g_{mtot} \gg g_{dstot}$, which is usually the case as the gate voltage has much greater effect to the current flow in the channel than the drain source voltage, eqn. (2.16) reduces to,

$$r_{in} \approx \frac{1}{g_{mtot}} \tag{2.17}$$

Eqn. (2.17) is the similar to that obtained in single gate MOSFET. Common-Drain Input Resistance: Reasons similar to the common source topology, the input resistance is also infinite (ideally).

The DG-MOSFET models for the output resistance and voltage gain of these three topologies can be modified in a similar manner following [55].

2.4 Microwave Basics

2.4.1 RF Figure of Merits

The two most important figures of merit intended for RF or microwave applications are transit frequency (f_T) and the maximum frequency f_{max}. The transit frequency is the frequency at which the short circuit current gain of the transitor becomes unity. An estimate of this is derived as follows [56],

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{2.18}$$

Another important figure of merit of transistor for RF application is the maximum frequency of oscillation, f_{max}, also known as the unity power gain frequency. This is the frequency at which the power gain drops to unity. The power gain is defined as ratio of the load power to the input power. In order to be termed an *active* device, a transistor must have power gain greater than unity [56]. Using the circuit theory [57], the value of f_{max} can be computed. The resulting expression is quite complicated and therefore simpler estimates are obtained using simpler models. Assuming the external resistance to be extremely small

in comparison to the gate resistance, the power gain can be obtained as follows [57],

$$f_{max} = \frac{f_T}{\sqrt{4R_g(g_{sd} + 2\pi f_T C_{gd})}} \tag{2.19}$$

This can be larger or smaller than f_T depending on other aspects [56]. To make f_{max} larger and make the transistor a useful device, the value of the gate resistance, R_g should be small enough so that f_{max} remains larger than f_T. R_g is kept small by implementing silicided gates or implementing multiple fingers at the gate.

2.4.2 Non-Linearity

While analog/RF circuits can be approximated by a linear model for small-signal operation, nonlinearities often lead to interesting and important phenomena that are not predicted by small-signal models. In this section,we study these phenomena for memory less systems whose input/output characteristic can be approximated by [58],

$$y(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) \tag{2.20}$$

The term α_1 can be considered as the small signal gain of the system because the other two terms are negligible for small input swings.

2.4.2.1 Harmonic Distortion

When a sinusoid is applied to a non-linear system, the output exhibits frequency components that are integer multiples or harmonics of the input frequency [58].

$$y(t) = \alpha_1 A cos\omega t + \alpha_2 A^2 cos^2\omega t + \alpha_3 A^3 cos^3\omega t \tag{2.21}$$

$$y(t) = \alpha_1 A cos\omega t + \frac{\alpha_2 A^2}{2}(1 + cos2\omega t) + \frac{\alpha_3 A^3}{4}(3cos\omega t + cos3\omega t) \tag{2.22}$$

$$y(t) = \frac{\alpha_2 A^2}{2} + (\alpha_1 A + \frac{3\alpha_3 A^3}{4})cos\omega t + \frac{\alpha_2 A^2}{2} cos2\omega t + \frac{\alpha_3 A^3}{4} cos3\omega t \tag{2.23}$$

In Eqn. 2.23, the first term is a dc term arising from second order non-linearity, the second term involves the fundamental frequency ω, the third is second harmonic , and the fourth is the third harmonic. It can be noted that, even order non-linearity produces dc offsets. We can infer the following two points from above statements [58]:

1) Even order harmonics cancels out for fully differential systems

2) n^{th} harmonic grows in proportion to A^n

2.4.2.2 Gain Compression

The small signal gain of circuits is usually obtained with the assumption that harmonics are negligible. The gain experienced by the sinusoid $Acos(\omega t$ is given by $\alpha_1 + \frac{3\alpha_3 A^2}{4}$ which implies the gain is proportional to A^2. When $\alpha_1\alpha_3 < 0$, the term $\alpha_3 x^3$ 'bends' the characteristic for large value of x, leading to compressive behaviour or an inverse proportionality between gain and the input amplitude. This compression is measured by *1-dB compression point* which is defined as the input signal level for which the gain drops by 1 dB. The Fig. 2.11 illustrates the concept in terms of power, which is more widely used rather than voltage.

The 1-dB compression point is denoted by P_{-1dB} as is indicated in the plot. To compute the input 1-dB compression point, the compressed gain, $\alpha_1 + \frac{3\alpha_3 A^2_{in,1dB}}{4}$ is equated less than 1 dB to the ideal gain, α_1 [58]

$$20log|\alpha_1 + \frac{3\alpha_3 A^2_{in,1dB}}{4}| \quad = \quad 20log|\alpha_1| - 1dB \tag{2.24}$$

This implies,

$$A_{in,1dB} \quad = \quad \sqrt{0.145|\frac{\alpha_1}{\alpha_3}|} \tag{2.25}$$

and gives the peak value of the input.

An adverse effect arising out of compression occurs if a large interferer accompanies the received signal. The small desired signal is superimposed on the large interferer and

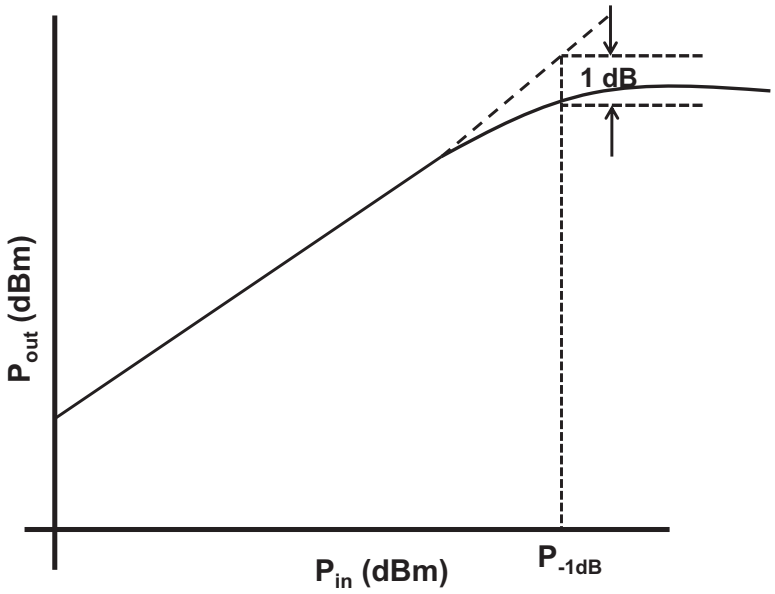


Figure 2.11: 1-dB Compression point.

consequently receiver gain is reduced. This phenomenon of lowering the SNR at the receiver output proves critical and is termed *desensitization* [58].

2.4.2.3 Intermodulation

The phenomenon of intermodulation (IM) arises due to the mixing of two interferers at two different frequencies. When two of the interferers at frequencies ω_1, ω_2 are applied to a non linear system, the output exhibits components that are not harmonics of these frequencies. Assuming, x(t) = $A_1\cos\omega_1 t + A_2\cos\omega_2 t$. Therefore from eqn. 2.20,

$$\begin{aligned} y(t) &= \alpha_1(A_1 cos\omega_1 t + A_2 cos\omega_2 t) + \alpha_2(A_1 cos\omega_1 t + A_2 cos\omega_2 t)^2 + \\ &\quad \alpha_3(A_1 cos\omega_1 t + A_2 cos\omega_2 t)^3 \end{aligned} \tag{2.26}$$

Expanding the RHS and discarding the dc terms, harmonics and components at $\omega_1 \pm \omega_2$, the following intermodulation products are obtained [58].

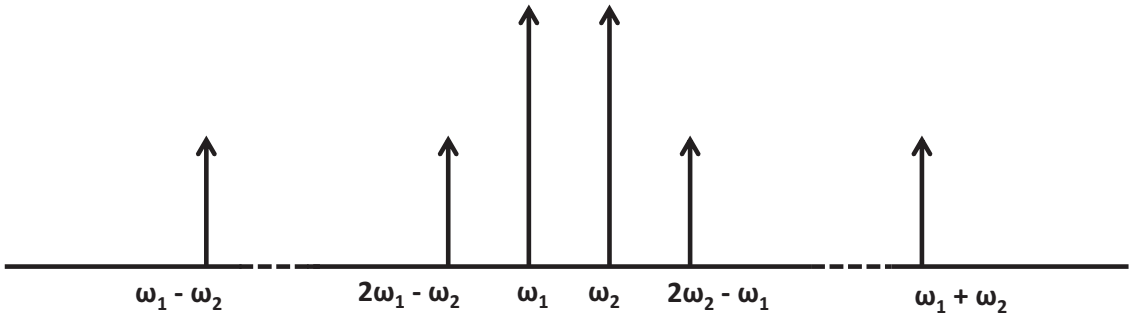


Figure 2.12: Intermodulation Components in two tone test.

$$\omega = 2\omega_1 \pm \omega_2 : \frac{3\alpha_3 A_1^2 A_2}{4} cos(2\omega_1 + \omega_2)t + \frac{3\alpha_3 A_1^2 A_2}{4} cos(2\omega_1 - \omega_2)t \tag{2.27}$$

$$\omega = 2\omega_2 \pm \omega_1 : \frac{3\alpha_3 A_1 A_2^2}{4} cos(2\omega_2 + \omega_1)t + \frac{3\alpha_3 A_1 A_2^2}{4} cos(2\omega_2 - \omega_1)t \tag{2.28}$$

and these fundamental components;

$$\begin{aligned} \omega = \omega_1, \omega_2 : (\alpha_1 A_1 + \frac{3}{4}\alpha_3 A_1^3 + \frac{3}{2}\alpha_3 A_1 A_2^2) cos\omega_1 t \\ +(\alpha_1 A_2 + \frac{3}{4}\alpha_3 A_2^3 + \frac{3}{2}\alpha_3 A_2 A_1^2) cos\omega_2 t \end{aligned} \tag{2.29}$$

The Fig. 2.12 illustrates the results. Among these the 3^{rd} order IM products at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ are of interest. This is because, if ω_1 and ω_2 are close to each other, then $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ appear in the vicinity of ω_1 and ω_2 and can affect the fundamental signals [58].

A common method of IM characterization is the two tone test, whereby two pure sinusoids of equal amplitudes are applied to the input [58]. The amplitude of the output IM products is then normalized to that of the fundamentals at the output. The input amplitude where the amplitude of the IM products becomes equal to that of the fundamental tones is known as the third order input intercept point (IIP_3) and is an important figure of merit for linearity in RF circuits (Fig. 2.13). To determine the IIP_3, the fundamental and third order

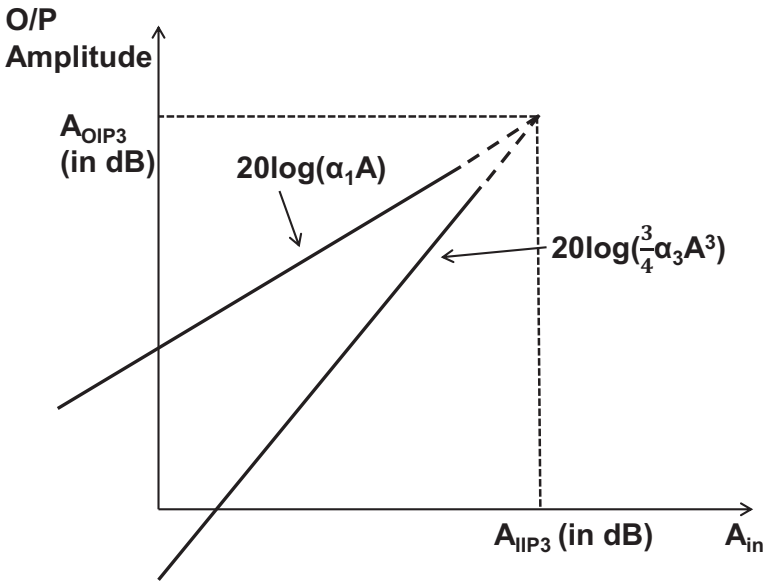


Figure 2.13: Third Order Intercept Point (in terms of voltage).

IM amplitudes (which can be obtained from either eqns. 2.27 or 2.28) are equated,

$$|\alpha_1 A_{IIP3}| = |\frac{3}{4}\alpha_3 A_{IIP3}^3| \tag{2.30}$$

obtaining,

$$A_{IIP3} = \sqrt{\frac{4}{3}(|\frac{\alpha_1}{\alpha_3}|)} \tag{2.31}$$

From above equation and eqn. 2.25,

$$\frac{A_{IIP3}}{A_{1dB}} \approx 9.6dB \tag{2.32}$$

This relationship may not always hold in circuits implemented with transistors with small gate lengths [59].

2.4.3 Noise

2.4.3.1 Randomness and Noise Spectrum

The noise is random, which implies the instantaneous value of noise cannot be predicted and we have to resort to stochastic approaches for the noise computation. Hence we consider the average noise power for our computation of noise at any instant. The average power of noise is defined as,

$$P_n = \lim_{T\to\infty} \frac{1}{T} \int_0^T n^2(t)dt \tag{2.33}$$

where n(t) represents the noise waveform. The computation of area under n_2 for a long period of time, T, followed by normalization, one obtains the average power of noise. The time domain representation of noise provides the information on average power.

2.4.3.2 Device Noise

The device noise in an analog integrated circuit includes the thermal noise of resistors. The ambient thermal energy leads to random agitation of charge carriers in resistors and hence noise. The Thevenin equivalent of the noise can be modeled by a series voltage source with a PSD of

$$\bar{V_n^2} = 4kTR_1 \tag{2.34}$$

The Norton equivalent, in terms of current, the PSD of which can be written as,

$$\bar{I_n^2} = \frac{4kT}{R_1} \tag{2.35}$$

It should be noted in an RLC tank, the PSD of noise determined above is only valid at the resonant frequency [58]. The maximum available noise power in a device is derived as,

$$P_{max} = kT \tag{2.36}$$

The detailed derivation can be referred in [58]. This is independent of the resistor value and is a constant for certain temperature. At room temperature, 300K, the computed value is -173.8 dBm/Hz.

The other source of noise in a device is the noise in MOSFETs. The thermal noise of MOS transistors operating in the saturation region is approximated by a current source tied between the source and drain terminals and is given as,

$$\bar{I_n^2} = 4kT\gamma g_m \tag{2.37}$$

where γ is the excess noise coefficient and gm the transconductance. The value of γ is 2/3 for long channel transistors and could icrease to 2 in short channel devices. Another component of thermal noise arises from the gate resistance of MOSFETs. This effect is more relevant for short channel MOSFETs. The gate resistance is given by

$$R_G = \frac{W}{L}R_{\square} \tag{2.38}$$

where $R_{\square}$ denotes the sheet resistance of the polysilicon gate. Sheet resistance is the resistance of 1 square. The gate resistance is distributed over the width of the transistor and therefore the structure can be reduced to a lumped model having an equivalent gate resistance of $R_G/3$ [58] with a thermal noise of PSD of $4kTR_G/3$. The gate noise must be much less than that of the channel noise. Thus,

$$4kTR_G/3 << 4kT\gamma g_m \tag{2.39}$$

The physical resistances of the gate and drain terminals are minimized by the use of multiple fingers because the equivalent resistance of the multiple fingers is reduced due to their parallel arrangement over the gate length.

The MOS devices also suffer from flicker noise or '$1/f$' noise as it is widely known. The PSD of the noise can modeled by a voltage source that can be expressed as,

$$\bar{V_n^2} = \frac{K}{WLC_{ox}}\frac{1}{f} \tag{2.40}$$

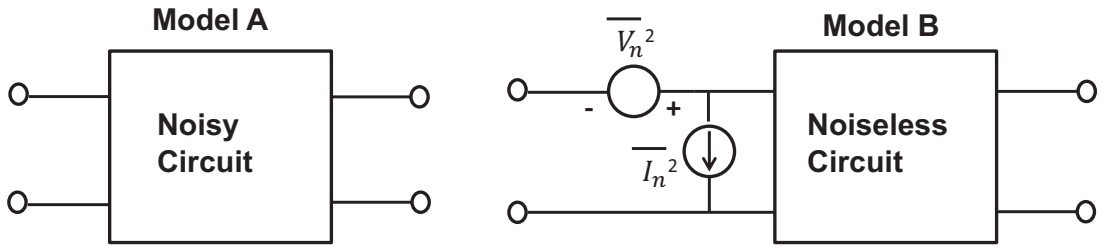


Figure 2.14: Input-referred noise.

where K is the process dependent constant. The value of K is lower in pMOS devices than for nMOS because the former carry charge well below the SiO_2 interface and hence suffer less from "surface states" or dangling bonds. The $1/f$ dependence implies the slowly varying noise components acquire a large amplitude. The $1/f$ noise PSD intercepts the thermal noise PSD at a frequency known as the corner frequency, f_c. Equating the thermal noise and the flicker noise current PSD, we obtain f_c, indicated as follows [58],

$$\frac{K}{WLC_{ox}}\frac{1}{f_c}g_m^2 = 4kT\gamma g_m \tag{2.41}$$

Therefore,

$$f_c = \frac{K}{WLC_{ox}}\frac{g_m}{4kT\gamma} \tag{2.42}$$

2.4.3.3 Noise in Circuits

Input-Referred Noise: The input referred noise is modeled by a series voltage and parallel current source. The former is obtained by shorting the input port of models A and B (Fig. 2.14) and equating their output noises. The current source is computed by leaving the input ports open and equating the output noises. The computation of this noise proves difficult in high frequencies and the concept of 'Noise Figure' for the noise measurement comes into existence.

Noise Factor & Noise Figure: The degradation of the Signal to Noise ratio (SNR) that is defined as the ratio of signal power to the noise power, from an input to the output in a circuit is measured by a factor termed as the noise factor (nf). Mathematically,

$$nf = \frac{SNR_{in}}{SNR_{out}} \tag{2.43}$$

The noise figure is expressed in dB and is given as,

$$NF = 10log(nf) \tag{2.44}$$

The detailed NF computation can be referred in [58].

2.4.4 Sensitivity & Dynamic Range

2.4.4.1 Sensitivity

The sensitivity is defined as the minimum signal level that a receiver can detect with acceptable quality [58]. The receiver sensitivity depends on the SNR_{min} of the signal, the receiver NF and the data bandwidth (B) [58].

$$P_{sen} = P_{RS} + NF + SNR_{min} + 10logB \tag{2.45}$$

The term P_{RS} is a temperature dependent constant and given as P_{RS} = kT = -174dBm/Hz. The first three terms in eqn is the total integrated noise of the system and referred as the noise floor [58].

2.4.4.2 Dynamic Range

The Dynamic Range is defined as the maximum input level that a receiver can tolerate divided by the sensitivity. Another type, called the Spurious Free Dynamic Range (SFDR) represents limitations arising from both noise and interference. The lower end remains the sensitivity whereas the upper end is defined as the maximum input level in a two tone test for which the third-order IM products do not reach the integrated noise of the receiver [58].

2.4.5 Scattering Parameters

Microwave theory deals mostly with power quantities rather than voltage or current quantities. the two reasons that can be explained this approach are as follows [60]:

1) Microwave design is based on power transfer from one stage to the next.

2) Voltages and currents are difficult to measure directly at microwave frequencies. Z matrix requires "opens", and its difficult to produce an ideal open (parasitic capacitance and radiation). Likewise, a Y matrix requires "shorts", again ideal shorts are nearly impossible to achieve at radio frequencies due to the finite inductance.

The concept of scattering parameters is similar to the idea of power flow. The power flow into a one-port circuit can be written as follows [60], [61],

$$P_{in} = P_{avs} - P_r \tag{2.46}$$

where P_{in} is the power flowing into the port, P_{avs} is the available power from the source and P_r is the wasted power that is reflected back due impedance mismatch. The value of P_{avs} is given as,,

$$P_{avs} = \frac{V_S^2}{8Z_0} \tag{2.47}$$

The complex power flowing into the port and absorbed is given by [60],

$$P_{in} = \frac{1}{2}(V_1 I_1^* + V_1^* I_1) \tag{2.48}$$

This implies from eqns. 2.46 & 2.48,

$$P_r = \frac{V_S^2}{4Z_0} - \frac{1}{2}(V_1 I_1^* + V_1^* I_1) \tag{2.49}$$

The factor of 4 instead of 8 is used because of the involvement of complex power. The mean power can be achieved by taking one half of the real component of the complex power. If the one-port has an input impedance of Z_{in}, then the power P_{in} can be expanded as [60],

$$P_{in} = \frac{1}{2}\left(\frac{Z_{in}}{Z_{in} + Z_0} V_S \frac{V_S^*}{(Z_{in} + Z_0)^*} + \frac{Z_{in}^*}{(Z_{in} + Z_0)^*} V_S^* . \frac{V_S}{Z_{in} + Z_0}\right) \tag{2.50}$$

This can be simplified to [60],

$$P_{in} = \frac{{V_S}^2}{2Z_0}\left(\frac{Z_0 Z_{in} + Z_0 Z_{in}^*}{|Z_{in} + Z_0|^2}\right) \tag{2.51}$$

With the exception of a factor 2, the pre-multiplier is simply the source available power, which means that our overall expression for the reflected power is given by [60],

$$P_r = \frac{{V_S}^2}{4Z_0}\left(1 - 2\frac{Z_0 Z_{in} + Z_0 Z_{in}^*}{|Z_{in} + Z_0|^2}\right) \tag{2.52}$$

This can be simplified,

$$P_r = P_{avs}\left|\frac{Z_{in} - Z_0}{Z_{in} + Z_0}\right|^2 = P_{avs}|\tau|^2 \tag{2.53}$$

The τ or the reflection coefficient is defined as,

$$\tau = P_{avs}\left|\frac{Z_{in} - Z_0}{Z_{in} + Z_0}\right| \tag{2.54}$$

This constant τ is also called the scattering parameter of a one-port [60].

The scattering parameter for a two port network is described next and illustarted in Fig. 2.15. The incident and reflected waves at the input port is denoted by V_1^+ and V_1^-, respectively. Similar waves are denoted by V_2^+ and V_2^-, respectively at the output. It should be noted, that V_1^+ denotes a wave generated by V_{in} as if the input impedance of the circuit were equal to R_S. Since that may not be the case, the reflected wave, V_1^-, is included so that the actual voltage measured at the input is equal to $V_1^+ + V_1^-$. Also, V_2^+ denotes the incident wave traveling into the output port, or equivalently, the wave reflected from R_L. These four quantities are uniquely related to one another through the S parameters of the network:

$$V_1^- = S_{11}V_1^+ + S_{12}V_2^+ \tag{2.55}$$

$$V_2^- = S_{21}V_1^+ + S_{22}V_2^+ \tag{2.56}$$

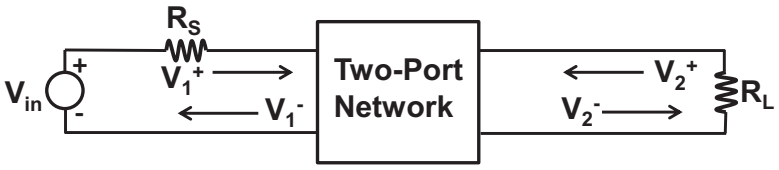


Figure 2.15: Illustration of Incident & Reflected waves at the input and output.

An intuitive interpretation for each parameter is given below [58]. For S_{11},

$$S_{11} = \left.\frac{V_1^-}{V_1^+}\right| V_2^+ = 0 \tag{2.57}$$

Thus, S_{11} is the ratio of the reflected and incident waves at the input port when the reflection from R_L is zero. This parameter represents the accuracy of input matching. For S_{12},

$$S_{12} = \left.\frac{V_1^-}{V_2^+}\right| V_1^+ = 0 \tag{2.58}$$

Thus, S_{12} is the ratio of the reflected wave at the input port to the incident wave into the output port when the input port is matched. This parameter characterizes the reverse isolation of the circuit, i.e., how much of the output signal couples to the input network. For S_{21},

$$S_{21} = \left.\frac{V_2^-}{V_1^+}\right| V_2^+ = 0 \tag{2.59}$$

Thus, S_{21} is the ratio of the wave incident on the load to that going to the input when the reflection from R_L is zero. This parameter represents the gain of the circuit. For S_{22},

$$S_{22} = \left.\frac{V_2^-}{V_2^+}\right| V_1^+ = 0 \tag{2.60}$$

Thus, S_{22} is the ratio of the reflected and incident waves at the output port when the reflection from R_S is zero. This parameter represents the accuracy of output matching.

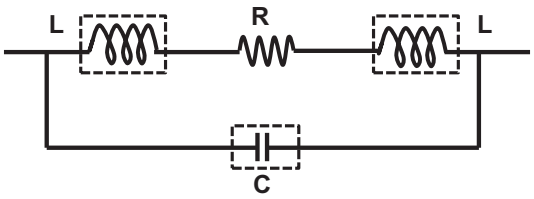


Figure 2.16: Resistor equivalent circuit.

2.4.6 Passives

The passive devices such as resistors, capacitors and inductors are traditionally considered playing a minor role in comparison with active devices. However, they are actually very critical parts in today's RFICs. The passive capacitors and resistors are relatively easy to integrate in comparison with the passive inductors. However, the inductors are widely used in almost all fundamental building blocks of RF circuits, including oscillators, LNA, PA, filters, transforms and matching circuitry. Their quality significantly affects the performance of the overall system.

2.4.6.1 Resistors

Resistor is the property of a material that determines the rate at which electrical energy is converted into heat energy for a given electric current. The equivalent circuit of a resistor at radio frequencies is shown in Fig 2.16 with the non-idealities L, the lead inductance and C, a combination of parasitic capacitances. R is the resistor value itself [12].

Ideally, resistors should act as pure DC, without any reactance characteristics. This ideality is maintained in DC circuits. However, in AC circuits some resistors may have features that make them unsuitable for a specific purpose. At high frequencies, these resistors possess the reactance property and behaves as an inductor or a capacitor [12]. The frequency response of a resistor informs the frequency where the resistor acts as a pure resistor sans any reactance properties and is chiefly of interest in RF circuit design. Many

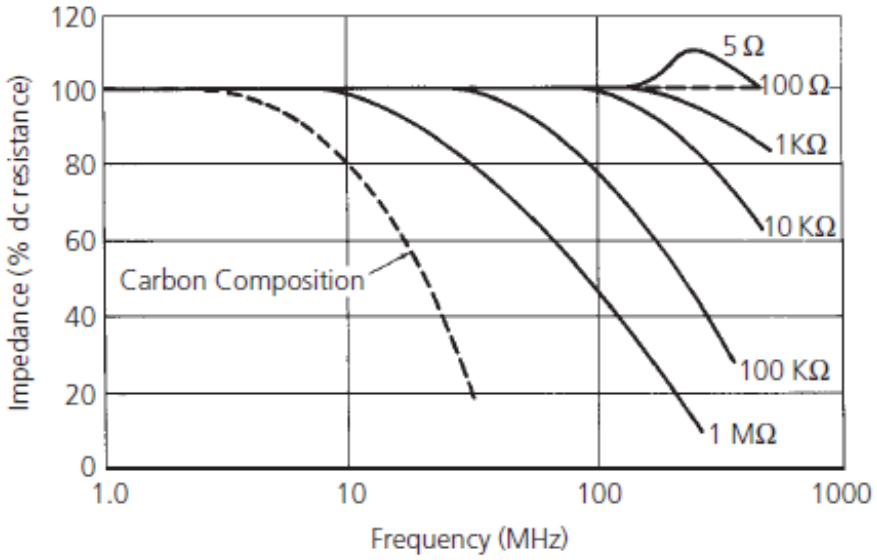


Figure 2.17: Frequency characteristics of metal-film and carbon-composition resistors [12].

types of resistors are used in RF applications. They are wire-wound, metal film, carbon film, carbon composition, adjustable resistors. The details on these can be referred in [12].

2.4.6.2 Capacitors

Capacitors are extensively used in RFIC design, such as in bypassing, interstage coupling, in resonant circuits and filters. There are quite a few types of capacitor used in the design of RF circuits, most common and widely used is the parallel plate capacitor. A parallel plate capacitor is a device which consists of two conducting plates separated by an insulating material or dielectric. The dielectric is usually ceramic, air, mica, plastic, film, glass or oil. The capacitance permits the storage of charge when potential difference exists between the conductors, given by [12],

$$C = \frac{dQ}{dV} \tag{2.61}$$

where, C = capacitance in farads, Q = charge in coulombs, V = voltage in volts. The capacitance of a parallel plate capacitor can be computed from its area, A, distance between

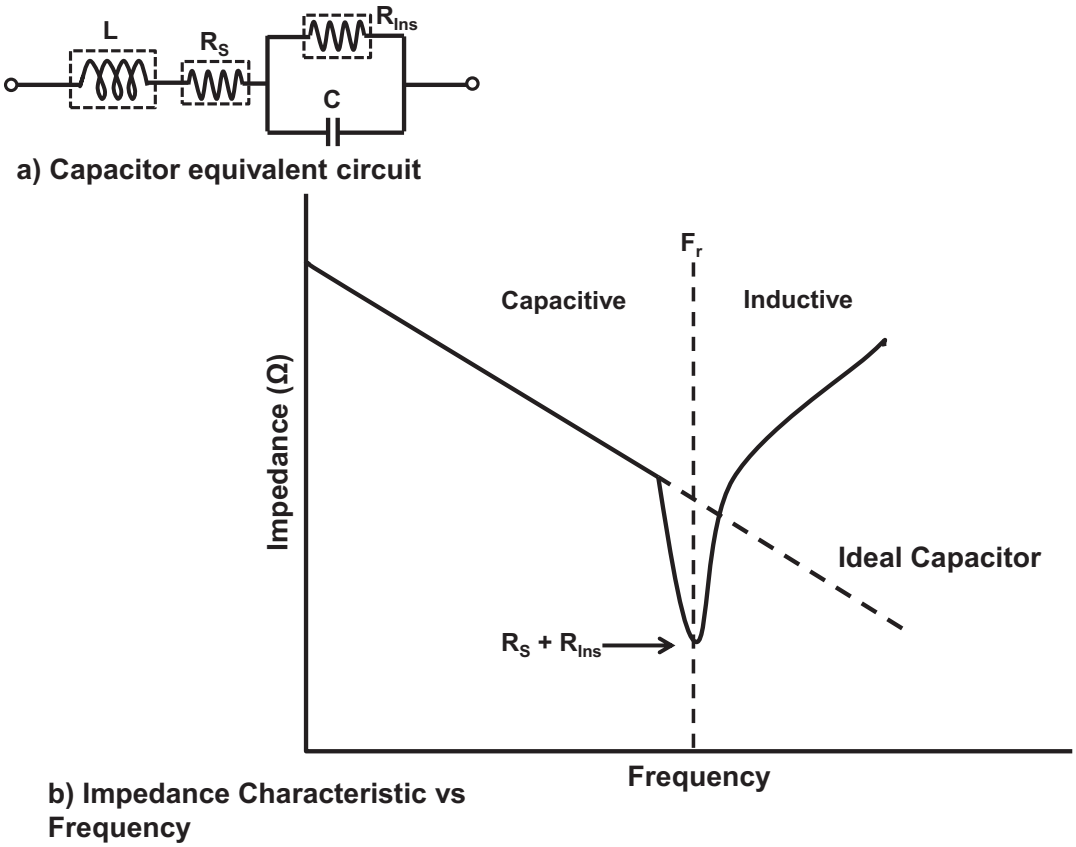


Figure 2.18: a) Capacitor equivalent circuit. b) Impedance characteristic vs. frequency.

the two plates, d, and permittivity of the dielectric material, ϵ,

$$C = \frac{\epsilon A}{d} \tag{2.62}$$

The dielectric characteristics of a capacitor determines the use of the capacitor. The characteristics also determine the voltage levels and the temperature extremes of the device. Therefore, any imperfections or losses in the dielectric have an effect on circuit operation [12].

The equivalent circuit of a capacitor is shown in Fig 2.18a, where C equals the capacitance, R_S is the heat dissipation loss expressed as a power factor or as a dissipation factor, R_{Ins} is the insulation resistance (which should be ideally infinite, but in real world

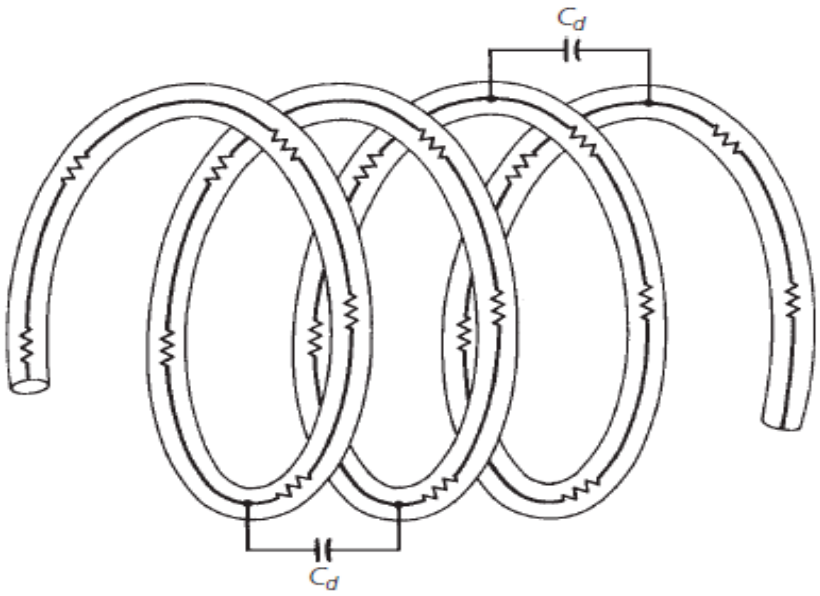


Figure 2.19: Distributed capacitance and series resistance in an inductor [12].

has a typical value of 100,000 MΩ or more), and L is the inductance of the leads and plates [12].

These imperfections become pronounced at ultra high frequencies (typically at 1 GHz or more). As shown in Fig. 2.18b in the impedance characteristic vs frequency plot, as the frequency increases, the inductance becomes appreciable. At a resonant frequency, F_r, the inductance becomes series resonant with the capacitor. As the frequency increases beyond F_r, the capacitor starts acting like an inductor. In general, larger capacitors exhibits more internal inductance than smaller capacitors following the formula, $X_C = \frac{1}{2\pi fC}$. At RF/mm-wave frequencies, however, the opposite may be true, and is considered for the design of mm-wave circuit [12].

2.4.6.3 Inductors

An inductor is a wire wound or coiled to increase the magnetic flux linkage between the turns of the coil. The flux linkage is proportional to the wire's self-inductance. They are

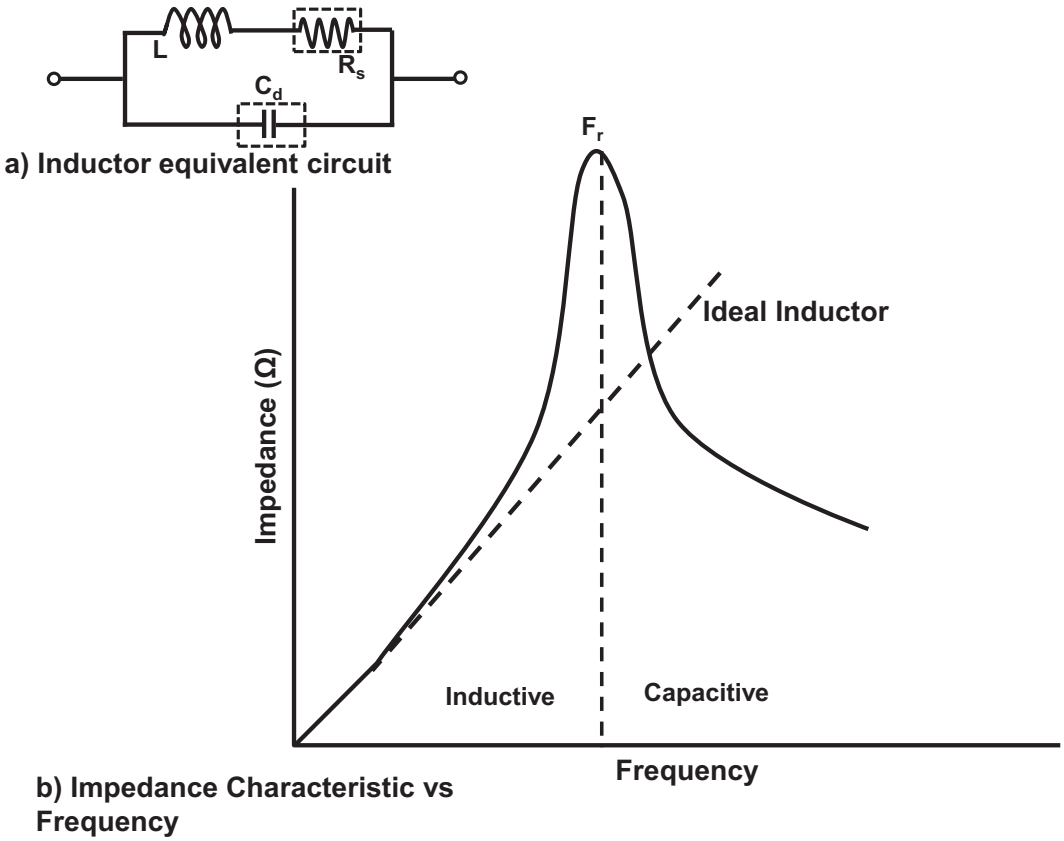


Figure 2.20: a) Inductor equivalent circuit. b) Impedance characteristic vs. frequency for a practical and an ideal inductor.

used extensively in RF design in resonant circuits, phase shift, filters and delay networks, and as RF chokes used to prevent/reduce the flow of RF energy [12].

There is always a capacitance associated with an inductor. This is because, when two conductors are placed in close proximity separated by a dielectric with an applied voltage difference between them, a capacitor is formed. A voltage drop between the windings will result in the formation of small capacitance, if any wire resistance at all exists. This effect is known as distributed capacitance [12] (C_d) as shown in Fig. 2.19. The equivalent inductance arising out of this is shown in Fig. 2.20a.

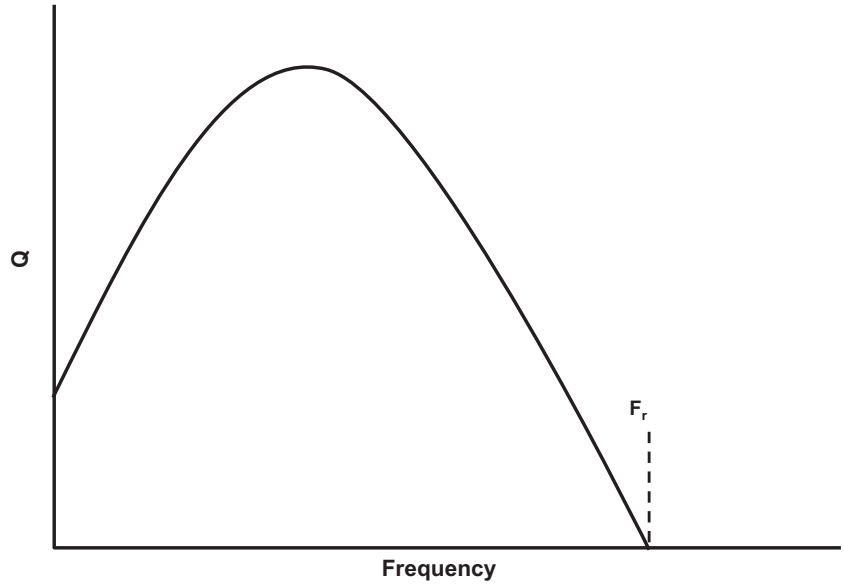


Figure 2.21: Q versus frequency of an inductor.

The effect of C_d upon the reactance of an inductor is shown Fig. 2.20b. Initially, at lower frequencies, the inductor's reactance resembles that of an ideal inductor. With increase in frequency, its reactance deviates from the ideal curve and increase at a faster rate until it reaches a peak at the inductor's parallel resonant frequency, F_r. Above F_r, the inductor's reactance begins to decrease with frequency and thus the inductor starts looking like a capacitor [12].

The Q of an inductor at low frequencies is good, because the only resistance in the windings is the dc resistance of the wire which is negligible. With increasing frequency, the winding capacitance and the skin effect begin to deteriorate the Q of the inductor as shown in Fig. 2.21. At low frequencies, Q will increase directly with frequency because its reactance is increasing and skin effect is not appreciable [12]. With increase in frequency, the skin effect becomes a factor. The Q still increases, but at a slower rate to obtain a gradually decreasing slope in the curve. After this, as the reactance and the series resistance changes at the same rate, the flat portion of the curve in Fig. 2.21 is obtained. Above this,

skin effect of the windings and the shunt capacitance combine to decrease the Q of the inductor at its resonant frequency to zero [12].

2.4.6.4 Microstrip Transmission Lines

RF circuits designed at mm-wave frequencies generally incorporates transmission lines to substitute on chip inductors or on chip transformers. This is because, although not impossible, it is quite difficult to build on chip inductors for circuits operating at mm-wave frequencies. Also, at microwave frequencies, the conventional lumped components cannot work as their desired performance as an inductor or capacitor is significantly dwarfed by the undesired device parasitics, hence replaced by microstrip transmission lines [62].

Considering the above reasons, we adopt microstrip transmission lines to substitute inductors in our 90 GHz mm-wave LNA design. The microstrip transmission line is a transmission line geometry with a single conductor trace on one side of a dielectric substrate and a single ground plane on the opposite side (Inset: Fig. 2.22). These structures achieve inductance with the flow of current in the conductor, whereas the capacitance is associated with the conducting strip separated from the ground plane by the dielectric substrate [63], [62]. The dielectric substrate considered in this paper is GaAs. In the layered structures, microstrip transmission lines and coplanar waveguides are commonly used as the transmission lines. Although microstrip structures have lower Q-factor when compared with the coplanar wave guides, they have less coupling between the adjacent lines and are easier to layout and integrate [64].

The inductor in question can be formed by shorting the microstrip center conductor to the lower level ground plane at one end of the transmission line. This results in an inductance which, for a given geometry and in a specified frequency range, is mostly independent of frequency [65]. Moreover, the microstrip transmission line provides an inductance which could be used on any type of substrate, with either low or high resistivity.

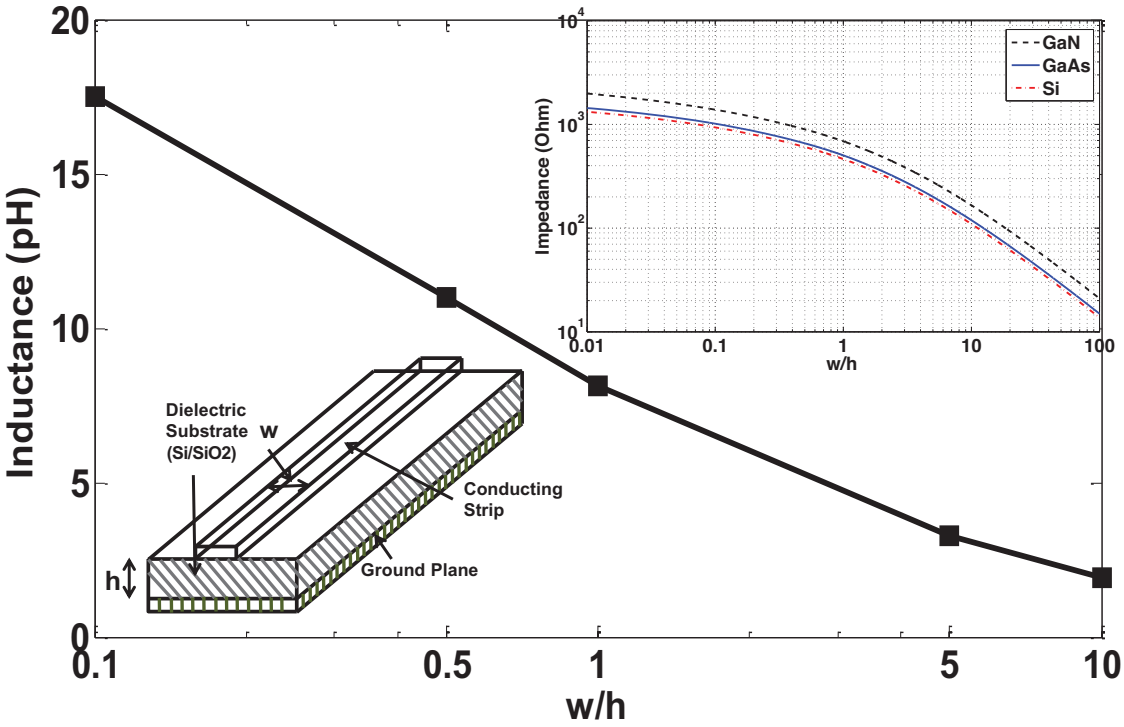


Figure 2.22: The inductance versus microstrip aspect ratio (w/h) at l = 50 μm. The inset plot shows the resulting characteristic impedance of the microstrips TL on alternative substrates.

Beyond the III-V technology, it is worth mentioning that micro-strip inductors can have big impact in silicon CMOS platforms since they could utilize two or all of the metal wiring levels, allowing a wide range of inductance and quality factor design tradeoffs. An important feature in this trade-off is the ability to utilize lower (below the inductor) metal wiring levels, as well as lower silicon and polysilicon areas for other than inductor design purposes, without affecting the operation of the inductor. Thus, silicon RF-CMOS circuits and its evolution to DG-MOSFETs/FinFETs are also well positioned to take advantage of this technique as a way to save area and reduce parasitics.

The microstrip characteristic impedance, Z, and the inductance, L, are computed as follows:

$$Z = \frac{1}{2\pi}\sqrt{\frac{\mu_0}{\epsilon_0\epsilon_e}}log[F\frac{h}{w} + \sqrt{1+(2\frac{h}{w})^2}] \tag{2.63}$$

$$L = \frac{Z}{2\pi f} sin(\frac{2\pi l}{\lambda}) \tag{2.64}$$

where, F & ϵ_e are obtained from expressions in [66]. To illustrate the design process and serve as example, the impedance of the microstrip transmission line is plotted for different substrates along with GaAs in the inset of Fig. 2.22.

At 90 GHz, the free-space wavelength (λ_0) is 3.3 mm. The wavelength in GaAs substrate is given by $\lambda_{GaAs} = \frac{\lambda_0}{\sqrt{\epsilon_{GaAs}}}$. Considering ϵ_{GaAs} to be 10, λ_{GaAs} is given as 1 mm. As the length of the microstrip transmission line considered for realizing the inductance is in the range of 30 μm, which is nearly 3% of the wavelength, we can justify $l << \lambda_{GaAs}$. Hence eqn. 2.64 can be rewritten as,

$$L = \frac{Zl}{\lambda f} \tag{2.65}$$

Considering this equation the inductance L is plotted for different aspect ratio (w/h) of the microstrip transmission line as shown in Fig. 2.22.

2.4.7 Impedance Matching

Impedance matching is required in the design of RF circuitry to provide maximum power transfer and minimize the reflection losses between the source and its load, i.e between two consecutive active components in the transceiver chain. The two most important applications are the impedance matching between the output of a PA and the antenna in the transmitter and the impedance matching between an antenna with the LNA input in a receiver.

The maximum power is transferred when the source impedance equals the load impedance. This can be verified as follows [12], [67]:

$$I = \frac{V_S}{R_S + R_L} \tag{2.66}$$

The power delivered at load is given as

$$P_L = I^2 R_L \tag{2.67}$$

Therefore, from eqns. 2.66 and 2.67,

$$P_L = \frac{V^2}{\frac{R_S^2}{R_L} + 2R_S + R_L} \tag{2.68}$$

Minimizing the denominator for maximum power transfer,

$$\frac{\mathrm{d}}{\mathrm{d}R_L}\left(\frac{R_S^2}{R_L} + 2R_S + R_L\right) = 0 \tag{2.69}$$

This solves to,

$$R_L = \pm R_S \tag{2.70}$$

Neglecting the negative value, we get $R_L = R_S$. To test for minima at R_S, one can find the second order differential of $\left(\frac{R_S^2}{R_L} + 2R_S + R_L\right)$ and prove it to be positive. The above derivation can be extended to solve in reactive circuits as well. The current in a reactive circuit can be written as [12], [67],

$$I = \frac{V_S}{Z_S + Z_L} \tag{2.71}$$

The power delivered to the load can be written as,

$$P_L = {I_{rms}}^2 Z_L \tag{2.72}$$

We know from basic physics, $I_{rms} = I/\sqrt{2}$. Hence,

$$P_L = \frac{1}{2} I^2 Z_L \tag{2.73}$$

We have $Z_S = R_S + jX_S$ and $Z_L = R_L + jX_L$. Hence the above equation is,

$$P_L = \frac{V_S^2 R_L}{2(R_S + R_L)^2 + (X_S + X_L)^2} \tag{2.74}$$

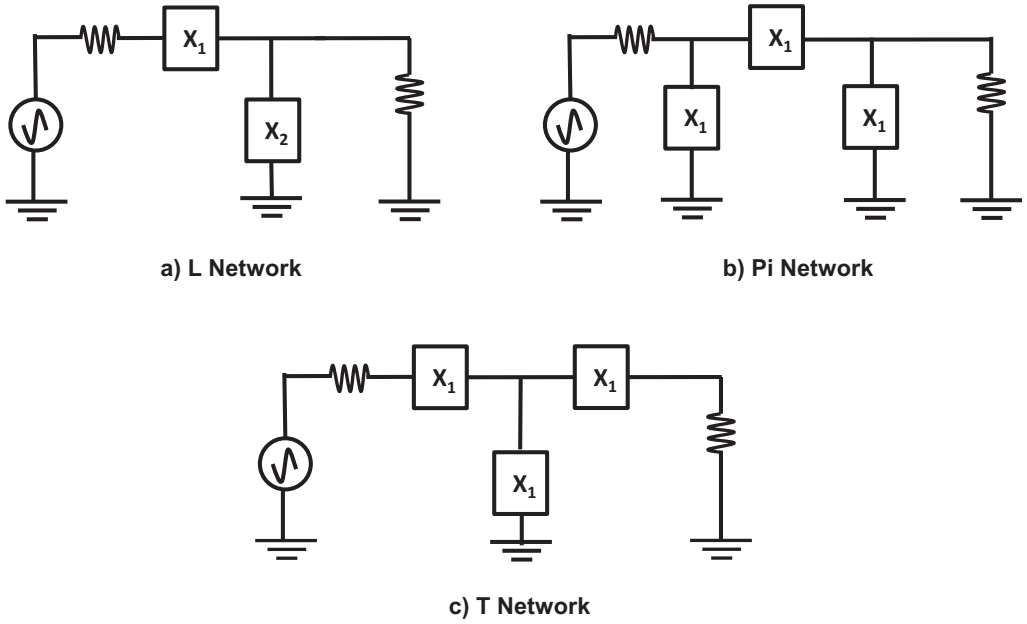


Figure 2.23: Impedance Matching of L-network, Pi-Network & T-network.

To maximize the power transfer, we need to minimize the denominator. Unlike the case for the purely resistive computation, here the minimizing is executed in two steps. In step 1, we observe, the power can be maximized if

$$(X_S + X_L)^2 = 0 \tag{2.75}$$

This implies, X_S = - X_L. The second step is executed similar to that of the resistive computation and it is observed to maximize the power we have also, $R_L = R_S$. Combining the above two conditions, the maximum power transfer in a reactive circuit occurs at [67]

$$Z_S = Z_L^* \tag{2.76}$$

There are an infinite number of impedance matching networks to perform impedance matching. The most popular of which are L-network, Pi-Network & T-network as shown in Fig. 2.23. [12].

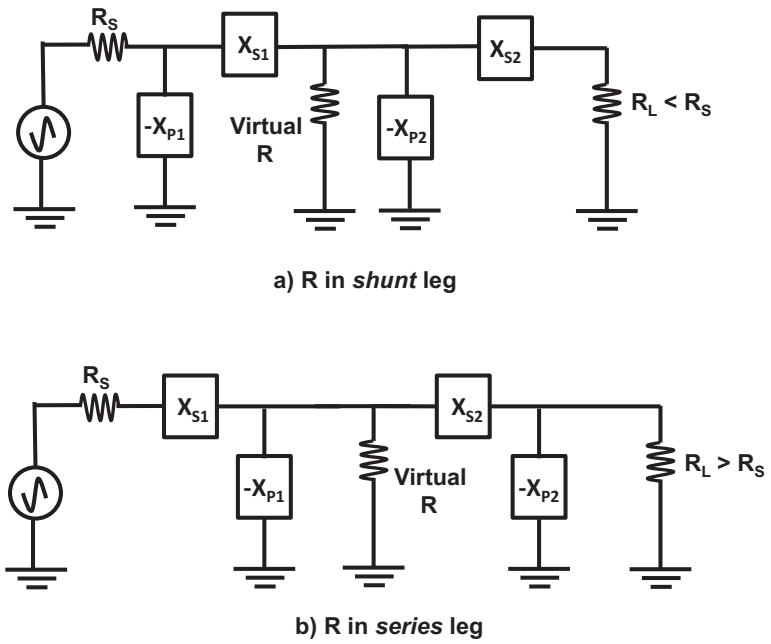


Figure 2.24: Two series-connected L networks for lower Q applications.

Since the reactance is frequency dependent, the perfect impedance match can occur only at one frequency. At all other frequencies from the matching center frequency, the impedance match becomes worse and eventually non-existent. This is an issue in broadband circuits where we try to obtain a perfect match everywhere within the broad passband. This is resolved by decreasing the loaded Q in the impedance matching network, hence increasing the bandwidth

In Fig. 2.24, two series-connected L sections are presented. In this new configuration, the value of the virtual resistor (R) must be larger than the smallest termination impedance and, also, smaller than the largest termination impedance. Any virtual resistance that satisfies these criteria can be chosen. The net result is a range of loaded-Q values that is less than the range of Q values earlier obtained, hence an increased bandwidth [12].

2.5 Wireless Communication

2.5.1 Modulation Fundamentals

Modulation in a wireless transmitter converts a low frequency baseband signal to a high frequency passband signal. The modulation is required primarily for the following three reasons [68]:

- Modulation is used to separate different signals when more than one signal utilizes a single channel
- Reduced size of antenna, because antennas are typically $\lambda/4$ in size, and increase in frequency, f, decreases the λ (λ = c/f), hence the antenna size decreases.
- Higher the frequency, more the available bandwidth, the most important and valued parameter in wireless communication.

Modulation can be both analog and digital. Here the important digital modulation techniques are discussed very briefly which are widely used in today's wireless communication.

2.5.1.1 Amplitude Shift Keying

The general analytic expression of Amplitude Shift Keying (ASK) is,

$$s_i(t) = \sqrt{\frac{2E_i(t)}{T}} cos(2\pi f_c t + \phi), i = 1, ...M. \tag{2.77}$$

where the amplitude $\sqrt{\frac{2E_i(t)}{T}}$ will have M discrete values, and the phase term, ϕ, is an arbitrary constant. The simplest of ASK modulation is termed as On Off Keying (OOK), also known as binary ASK modulation. OOK represents digital data as the presence or absence of a carrier wave. In its simplest form, the presence of a carrier for a specific duration represents a binary one, while its absence for the same duration represents a binary zero. The BER of OOK Modulation is shown in Fig. 2.25 [68], [69].

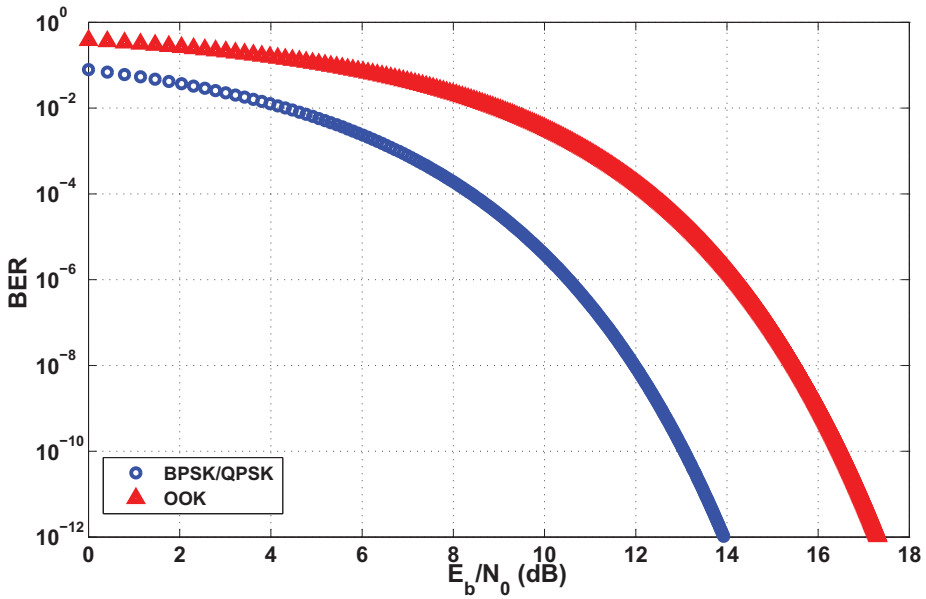


Figure 2.25: Bit Energy to Noise Density ratio (E_b/N_o) for different modulation schemes.

2.5.1.2 Phase Shift Keying

Phase-shift keying (PSK) is a digital modulation technique that conveys data by altering or modulating, the phase of a reference signal which is usually the carrier wave. It uses a finite number of phases, each allocated a unique pattern of binary digits to represent a digital data. Usually, each phase encodes an equal number of bits and each pattern of bits forms the symbol that is represented by the particular phase [68], [69].

Binary PSK: Binary PSK or BPSK is the simplest form of PSK. It uses two phases which are separated by 180°. The two phases represented as two points can be positioned anywhere in the constellation diagram as long they are 180° apart. In Fig. 2.26a they are shown on the real axis, at 0° and 180°. The BPSK overcomes the highest level of noise or distortion and makes the demodulator to reach a correct decision and hence is the most robust. As it is only able to modulate at 1 bit/symbol this technique is unsuitable for high

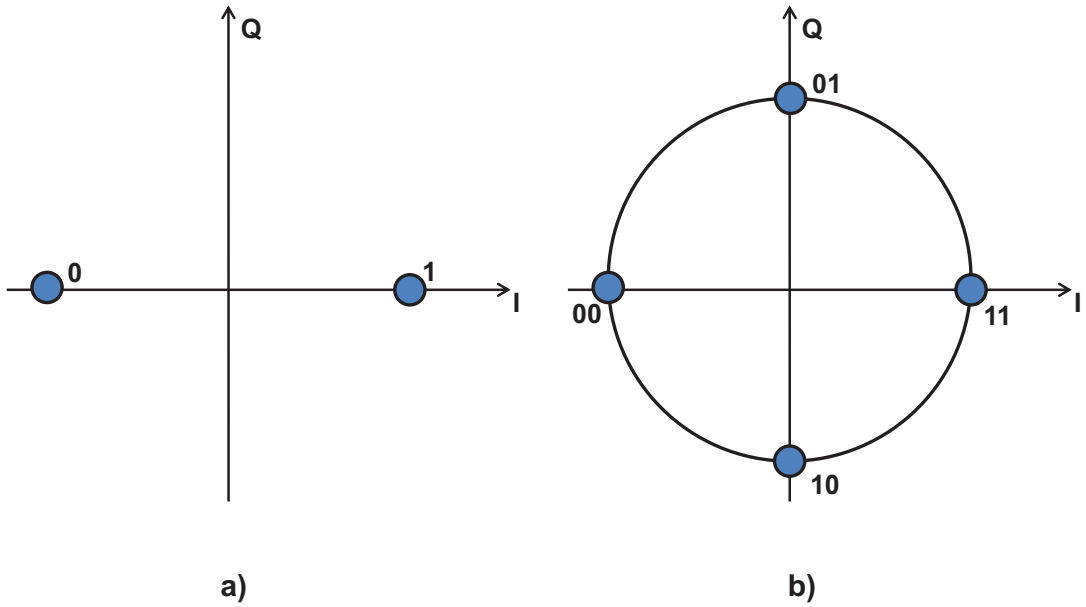


Figure 2.26: Constellation diagram for a) BPSK b) QPSK with gray coding.

data-rate applications. The general form for BPSK can follow the equation:

$$s_n(t) = \sqrt{(\frac{2E_b}{T_b})}cos(2\pi f_c t + n\pi), n = 0, 1 \quad (2.78)$$

This yields two phases, 0 and π. In the specific form, binary data is often conveyed with the following signals [68], [69]:

$$s_0(t) = \sqrt{(\frac{2E_b}{T_b})}cos(2\pi f_c t) for "0" \quad (2.79)$$

$$s_1(t) = -\sqrt{(\frac{2E_b}{T_b})}cos(2\pi f_c t) for "1" \quad (2.80)$$

where f_c is the carrier wave, E_b is the energy per bit and T_b is the bit duration. The assignment of "0" and "1" is arbitrary and can be interchanged in accordance with Eqn. 2.78 [68], [69].

Quadrature PSK: The quadrature PSK or QPSK uses four phases that are separated by $\pi/2$ on the constellation diagram. With four phases, QPSK can encode two bits per shown

in with gray coding. The gray coding is generally used to minimize the bit error rate. The general form of QPSK can follow the equation:

$$s_n(t) = \sqrt{(\frac{2E_b}{T_b})}cos(2\pi f_c t + n\frac{\pi}{2}), n = 0, 1, 2, 3 \quad (2.81)$$

This yields in four phases at 0, $\pi/2$, π and $3\pi/2$. They are illustrated in Fig. 2.26b. Again these phases are completely arbitrary and can be anywhere in the constellation diagram each separated by $\pi/2$ [68], [69].

2.5.1.3 Orthogonal Frequency Division Multiplexing

Orthogonal Frequency Division Multiplexing or OFDM is a frequency-division multiplexing (FDM) scheme used as a digital multi-carrier modulation method. The data is transferred on multiple parallel data streams or channels by using a large number of closely spaced orthogonal sub carrier signals. Each of these sub carrier signals is modulated with a conventional modulation technique (such as phase shift keying) at a low symbol rate. The total data rates and bandwidth in OFDM must be similar to conventional single-carrier modulation schemes in the same bandwidth.

The need for OFDM rises to mitigate the effect of multipath and subsequently reducing / eliminating the inter symbol interference (ISI). The ISI resulting from multipath effect worsens for larger delay spreads or higher bit rates. As a rule of thumb, wirless communication suffer from multipath for data rates greater the 10 Mbps. Hence, a single carrier modulated spectrum which occupies a relatively large bandwidth due to a high data rate of say, r_b bits per second, is demultiplexed by a factor of N, producing N streams each having a symbol rate of r_b/N [58]. The N streams are then impressed on N differential carrier frequencies, f_{c1} - f_{cN}, leading to a “multi-carrier” spectrum [58]. This is illustrated in Fig. 2.27. Each of the N carriers in Fig. 2.27b is called a subcarrier and each resulting

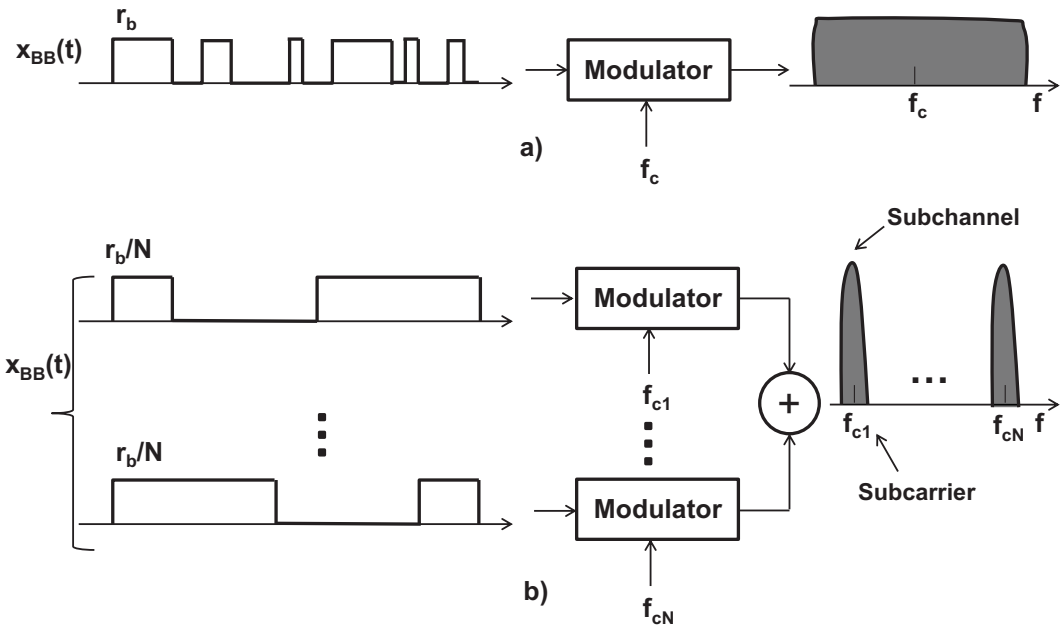


Figure 2.27: a) Single carrier modulation with high-rate input. b) OFDM with multiple carriers.

modulated output a "subchannel". All of the subchannels utilize the same modulation scheme.

It is to be noted, while providing greater immunity to multipath propagation, OFDM imposes severe linearity requirements on power amplifiers. This is because the N orthogonal subchannels summed at the output of the system may add constructively at some point in time creating a large amplitude, and destructively at some other point of time, producing a small amplitude. That is, the OFDM exhibits a large envelope variations even if the modulated waveform in each subchannel does not [58].

2.6 Wireless Transceiver

2.6.1 Basic Architecture

The objective of an Wireless Transceiver is to transmit and receive information. The transmitter (Tx) processes the voice or data signal and applies the result to the antennas.

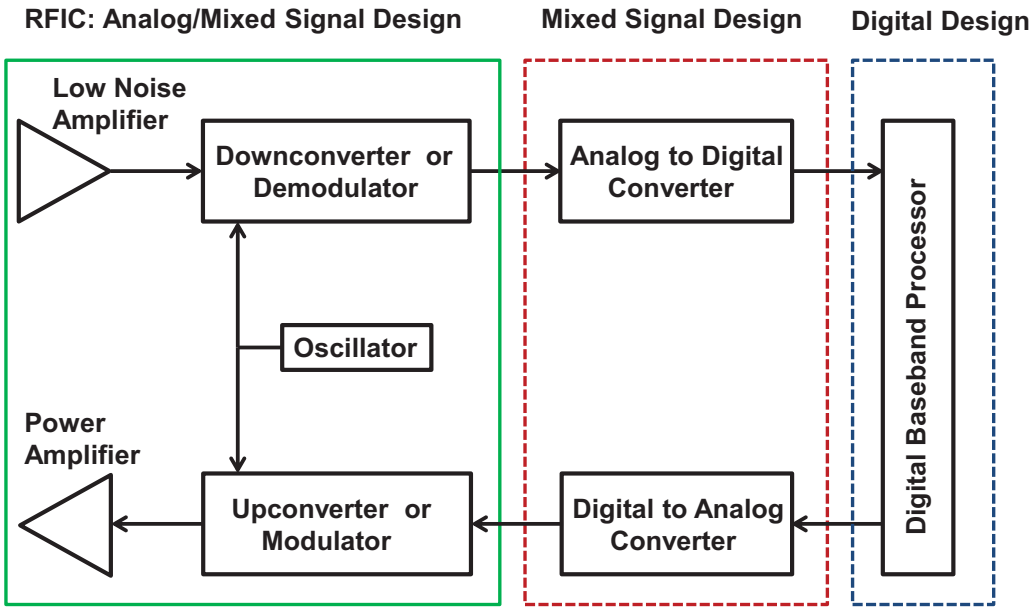


Figure 2.28: The generic wireless transceiver architecture.

Similarly, the receiver (Rx) senses the signal picked up by the antenna and processes it so as to reconstruct the original voice or data information. The signal to be transmitted is first applied to a 'modulator' or 'upconverter' so that its center frequency goes from the low frequency data signal to the high frequency carrier. The result drives the antenna through a 'Power Amplifier'. On the receiver side, the signal is sensed by a 'Low Noise Amplifier' and subsequently by a downconverter (can be RF Mixer) or demodulator (Envelope Detector or Phase Locked Loop (PLL)). The upconversion or downconversion path are driven by an oscillator. The overall transceiver is illustrated in Fig. 2.28.

The current research encompasses the RFICs of the wireless transceiver design which involves mostly analog circuits and some mixed signal circuits such as Phase Frequency Detector (PFD).

2.6.2 System Level Design

Specification and Theoretical Computation: To exemplify on the system level design of a receiver, the specifications of the wireless standard IEEE 802.11p is considered to design the RF Front end including the Variable Gain Amplifier (VGA). The IEEE 802.11p is an amendment to the existing IEEE 802.11 standard, to include Wireless Access in Vehicular Environments [70].

According to the specification of the standard, the OFDM system supports a "half-clocked" operation using 10 MHz channel spacings with data communications of 3, 4.5, 6, 9, 12, 18, 24, and 27 Mb/s [71].

In this research, a superheterodyne receiver (with two intermediate mixer stages) has been designed (Fig. 2.29) for the BPSK modulation with 10 MHz channel spacing and 3 Mbps data rate at a center frequency of 5.875 GHz. The design is implemented for BER of 10^{-6}, at which the SNR is observed to be $\sim$ 11 dB. The 802.11p standard defined receiver sensitivity (P_{sen}) is -85 dBm for this modulation scheme. Therefore, according to the sensitivity equation [58], given as follows, the Noise Figure (NF) of the receiver chain is around 8 dB.

$$NF = P_{sen} - 10log(kTB) - SNR_{min} \tag{2.82}$$

Both transmitted and received signals in OFDM can have a huge range of amplitude variations depending on the instantaneous signal path and the distance between emitter and receiver. This is because the N orthogonal subchannels when summed may add constructively at some point in time creating a large amplitude and destructively at some other point, producing a small amplitude.

The quantitative measure of the signals envelope variation is termed "peak to average power ratio" (PAPR). When N (no of subcarrier) is large, the PAPR of OFDM is given as [72],

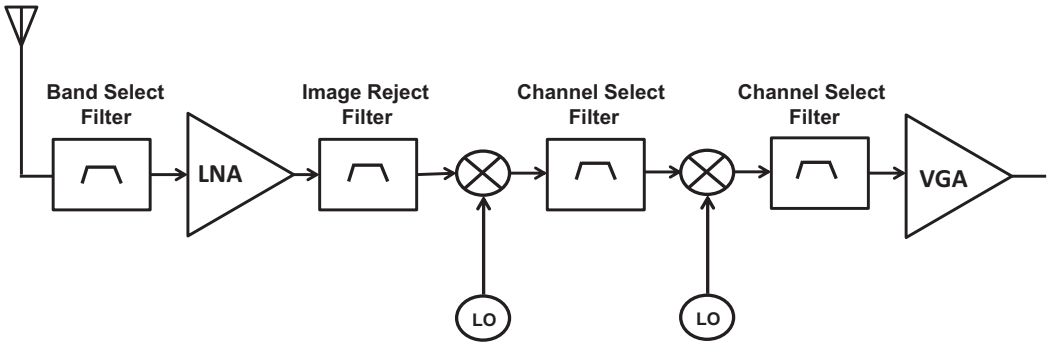


Figure 2.29: The receiver schematic.

$$PAPR = 2lnN \tag{2.83}$$

When N is 52, as in this case, PAPR is 7.8 dB.

To avoid saturation effects of subsequent stages and to meet the linearity requirements, the gain of the LNA and the VGA should be reduced for large input signals. The linearity of the LNA should be also high to meet the linearity requirement of the receiver chain. The 1-dB compression point (P_{1dB}) of the receiver chain can be calculated from the maximum input power level ($P_{in,max}$) and PAPR of the OFDM receiver. It can be written [73],

$$P_{1dB} = P_{in,max} + PAPR \tag{2.84}$$

The $P_{in,max}$ handled by the 802.11p receiver is -30 dBm. Hence P_{1dB} is -22.2 dBm and the IIP_3 is -12.6 dBm. This linearity is a stringent condition and can be achieved using a linear LNA and gain optimisation of the individual receiver blocks.

System Level FoMs Computation & Simulation: The gain of the receiver chain is simply the multiplication of the gain of the individual blocks. In dB, this can be written as,

$$G_{tot} = G_1 + G_2 + ... + G_m \tag{2.85}$$

The conventional method to compute the NF of the receiver chain is given by the decade old Friis equation [74],

$$nf_{tot} = 1 + (nf_1 - 1) + \frac{nf_2 - 1}{G_1} + ... + \frac{nf_m - 1}{G_1 G_2 ... G_m} \tag{2.86}$$

Where nf_i and G_i are the noise factor and power gain of the i^{th} block respectively. The noise figure (in dB) can be written as,

$$NF_{tot} = 10log(nf_{tot}) \tag{2.87}$$

The Eqn. 2.86 suggests that the noise contributed by each stage decreases as the total gain preceding that stage increases. This implies that the first few stages in the receiver chain are the most critical. Hence, the LNA should be designed with minimal NF.

The IIP_3 of the receiver chain can be computed as [58],

$$\frac{1}{IIP^2_{3,tot}} = \frac{1}{IIP^2_{3,1}} + \frac{G_1}{IIP^2_{3,2}} + ... + \frac{G_1 ... G_m}{IIP^2_{3,m}} \tag{2.88}$$

Besides these conventional ways to calculate the important FoMs of the receiver chain, other computational methods have also been proposed [75]-[76] and may find application in some simulators.

The simulation to compute the primary FoMs of the receiver chain has been performed with Agilent ADS. The gain of the receiver is 29.3 dB (Fig. 2.30) and the NF is 7.3 dB (Fig. 2.31). The gain of the chain has to be compromised to meet the linearity requirement of the wireless standard. Also the LNA in the chain should have a high linearity to support the standard specification. After these trade-offs the IIP_3 is observed at -12.4 dBm (Fig. 2.32). The individual figures of merit of the components can be observed from Table 2.1. All these figures meet the specifications of the IEEE 802.11p standard as discussed earlier.

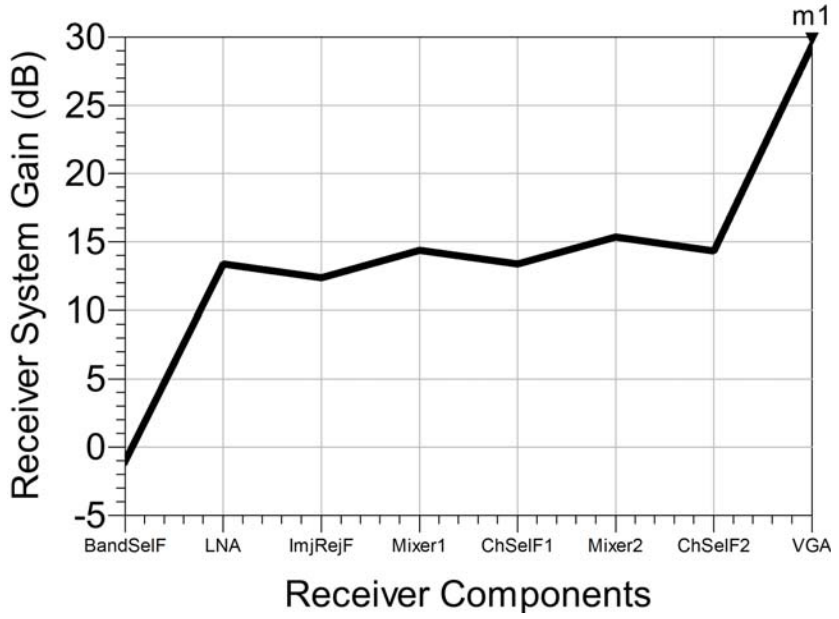


Figure 2.30: The simulated gain of the receiver chain. The marker 'm1' indicates the final gain achieved in the receiver system.

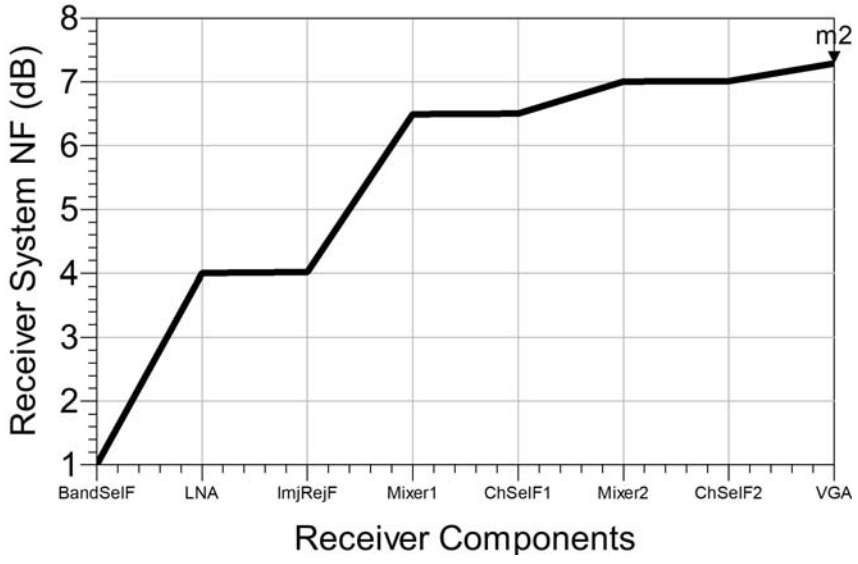


Figure 2.31: The simulated NF of the receiver chain. The marker 'm2' indicates the final NF achieved in the receiver system.

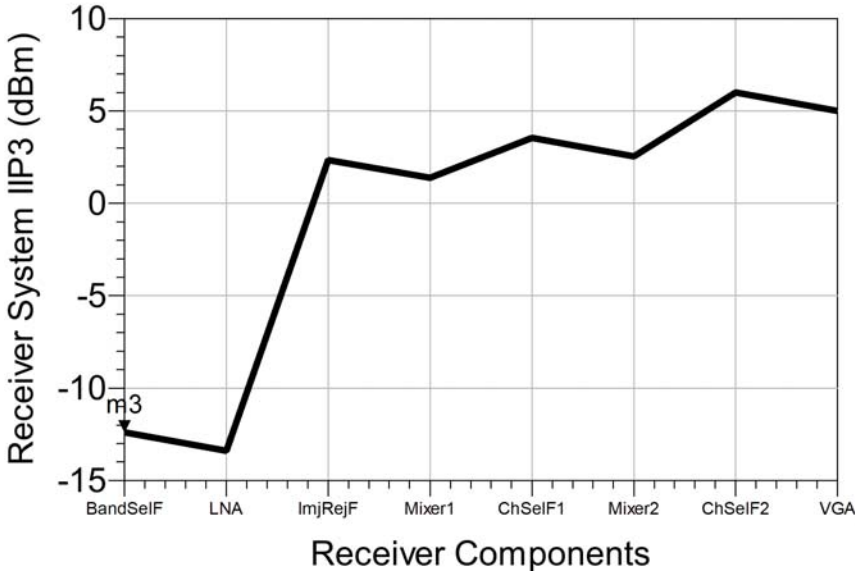


Figure 2.32: The simulated IIP_3 of the receiver chain. The marker 'm3' indicates the final IIP_3 in the receiver system.

Table 2.1: Active Blocks Individual FoMs

Parameters	LNA	Mixer 1	Mixer 2	VGA
Gain (dB)	15	2	2	15
NF (dB)	3	6	6	10
Linearity (dBm)	10	10	10	20

2.6.3 Link Budget Analysis

A link budget is computed to determine the sensitivity of the receiver (P_{Rx}) for different data rates (R_b) and the required transmit power (P_{Tx}) for different d as well as R_b. The typical range for short distance OOK modulated wireless communications lies in the range of 10 cm to 10 m. Both the estimated P_{Tx} and P_{Rx} is measured for R_b between 1 Gbps

and 5 Gbps. Computing the noise floor to be -174 dBm/Hz and assuming a noise figure contribution from receiver to be 3 dB we get the total receiver noise floor to be -171 dBm/Hz. The E_b/N_o (in dB) for OOK Modulation is $\sim$ 17.5 dB for an assumed BER of 10^{-12} as evident from Fig. 2.25. Therefore, energy per bit $(E_b)_{dB}$ is given by -153.5 dBm/Hz. P_{Rx} for different R_b is thus given as

$$P_{Rx} = E_b R_b \tag{2.89}$$

Then P_{Tx} (in dBm) for different d is obtained as,

$$P_{Tx} = P_{Rx} - G_{Tx} - G_{Rx} + L_{fs} + Margin \tag{2.90}$$

where G_{Tx} and G_{Rx} are the antenna directivities at the transmitter and receiver respectively and assumed to be 0 dB for an isotropic antenna. The Margin is assumed to be 3 dB. L_{fs} for different d is obtained from equation (1). Fig. 2.33 provides the estimated P_{Rx} for different R_b and P_{Tx} for different d as well as R_b. The free space propagation loss (L_{fs}) is given by

$$L_{fs} = 20log_{10}(\frac{4\pi d}{\lambda}) + (O_2)_{Abs.loss} \tag{2.91}$$

where λ is the signal wavelength (5 mm) and d is the propagation distance, we can justify the 60 GHz frequency is not ideal for use in long distance communications and is preferred in short distance secured wireless communications. $(O_2)_{Abs.loss}$ is the oxygen absorption loss, appreciable for $d \geq 1$ m with a value of 0.2 dB/m.

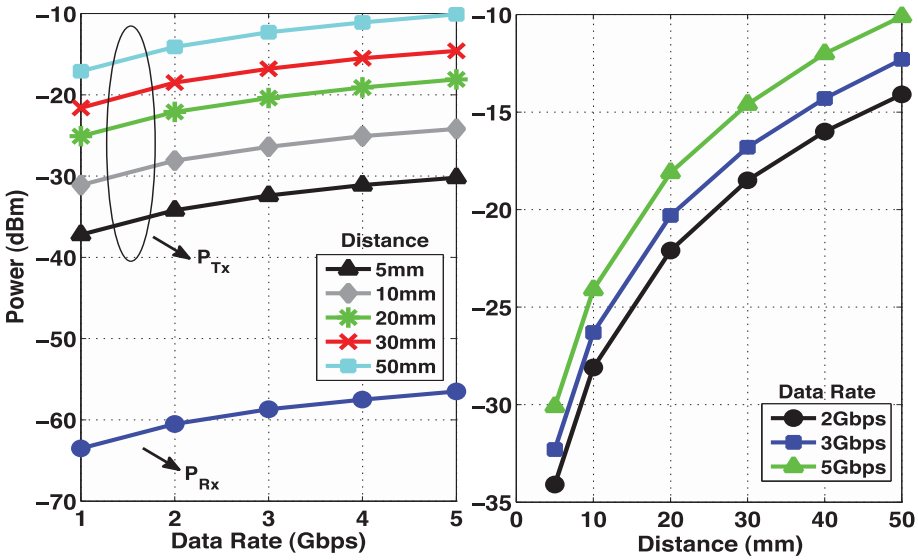


Figure 2.33: The sensitivity of the receiver for different data rates and required transmitter power levels for different propagation distance as well as data rates.

3 DG-MOSFET OOK TRANSMITTER

3.1 Introduction

The OOK transmitter consists of a Voltage Controlled Oscillator (VCO), the On Off Keying (OOK) modulator and the Power Amplifier (PA), apart from the transmitting antenna as shown in Fig. 3.1. A matching network (Z_0 in Fig. 3.1) which maximizes the power transfer and minimizes the reflection losses precedes the 50 Ω antenna. In this section these wireless components have been designed and analysed in DG-MOSFET technology and the merits of such design are explained. LC Oscillator along with the inductorless Relaxation Oscillator are the two different category of oscillators that have been considered in this chapter. Their novel voltage control characteristics have been investigated, which can be applied in an OOK transmitter. After this, a novel OOK Modulator is considered followed by the investigation of two different topologies of PA at two different microwave frequencies.

3.2 Oscillators

The following beneficiary features of the DG-MOSFET LC and relaxation oscillators over conventional CMOS are addressed and analysed in the research on oscillators [13], [15].

- A more lenient oscillatory criterion of common mode DG-MOSFET based LC oscillator than conventional CMOS is analyzed quantitatively.
- An independent mode DG-MOSFET LC VCO is designed in which the voltage controls the oscillation frequency via the back gate bias of the DG-MOSFETs without the requirement of any MOS varactors as needed in single gate conventional CMOS for voltage control of the oscillation frequency.

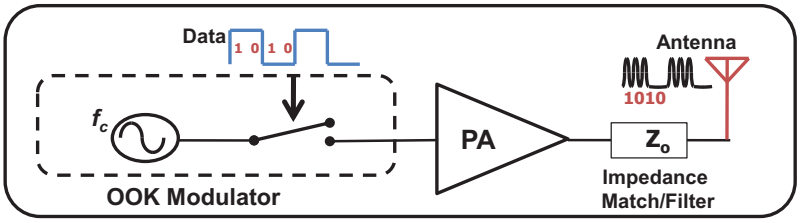


Figure 3.1: The OOK Transmitter Block Diagram.

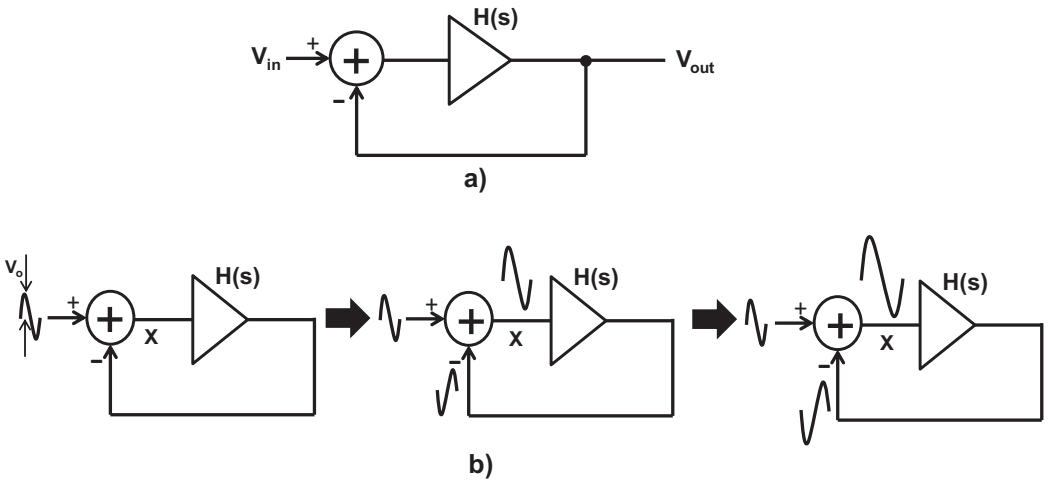


Figure 3.2: a) Feedback System b) Evolution of oscillatory system with time.

- Reduced number of transistors in an LC quadrature oscillator from eight in conventional CMOS to four in the DG-MOSFET version, enabling faster performance by reducing parasitics.

- A novel DG-MOSFET based relaxation oscillator in which the comparator circuit required in conventional CMOS is omitted by utilizing back gate biasing of the DG-MOSFET, making the circuit faster as well as area and power efficient.

- The voltage controlled oscillator (VCO) operation of the relaxation oscillator via back gate tuning, in addition to the existing current controlled oscillator (ICO)

operation. The VCO operation aids in high precision frequency tuning, a feature not possible in conventional CMOS.

3.2.1 Oscillator Fundamentals

Oscillators are critical to the design and performance of a variety of analog and digital blocks in CMOS mixed-signal systems [58]. They can serve as quintessential clock signals in synchronous digital circuits or unique reference (local) oscillators in many analog communication and control systems. Their performance in terms of accuracy and power dissipation is often the most important figure of merit that can determine overall system characteristics since they orchestrate overall signal traffic and/or beat as the fastest element in the system. Moreover, tunable oscillators used in large portion of these applications are the key elements to provide feedback control and signal conversion that would otherwise require complex and specialized transducers. Therefore new oscillators of scalable and tunable characteristics, relying on novel device architectures, are of high importance to circuit engineering at many levels.

To understand the theory behind the oscillation, a unity gain feedback circuit is considered in Fig. 3.2a, where,

$$\frac{V_{out}}{V_{in}} = \frac{H(s)}{1 + H(s)} \tag{3.1}$$

When the amplifier experiences a large phase shift at high frequencies the overall feedback becomes positive, which generates the oscillation. Precisely, if for $s = j\omega_0$, $H(j\omega_0) = -1$, then the closed-loop gain approaches infinity at ω_0. Under this condition, the circuit amplifies its own noise components at ω_0 indefinitely. As conceptually illustrated [28] in Fig. 3.2b, a noise component at ω_0 experiences a total gain of unity and a phase shift of 180°, returning to the subtractor as a negative replica of the input. Upon subtraction, the input anthe feedback signals give a larger difference. Thus the circuit continues to regenerate allowing the component at ω_0 to grow. For the oscillation to begin, a loop gain

of unity or greater is necessary. This can be seen by following the signal around the loop over many cycles and expressing the amplitude of the subtractor's output in Fig. 3.2b as a geometric series (if $\angle$H(jω) = 180°):

$$V_X = V_0 + |H(j\omega)|V_0 + |H(j\omega)|^2 V_0 + |H(j\omega)|^3 V_0 \tag{3.2}$$

If —H(jω)— > 1, the above summation diverges, whereas if —H(jω)— < 1, then

$$V_X = \frac{V_0}{1 - |H(j\omega)|} \leq \infty \tag{3.3}$$

Therefore, if a negative feedback circuit has a loop gain that satisfies two conditions:

$$|H(j\omega)| \geq 1 \tag{3.4}$$

$$\angle H(j\omega) = 180^\circ \tag{3.5}$$

then the circuit may oscillate at ω_0. This is called the Barkhausen criteria and is a necessary but not a sufficient condition.

It can be stated that the second Barkhausen criterion as $\angle$ H(jω) = 180° or a total phase shift of 360°. THis is because, if the system is designed to have a low frequency negative feedback, it already produces 180° of phase shiftin the signal travelling around the loop and $\angle$ H(jω) denotes an additional frequency dependent phase shift that is illustrated in Fig. 3.2b.

The oscillation criteria in terms of the location of poles of a closed loop system in the complex coordinate plane is illustrated and explained in Fig. 3.3. Expressing each pole frequency as s_p = jω_p + σ_p and noting that the impulse response of the system includes a term exp(jω_p + σ_p)t, it can be observed that if the poles lie in the left half plane, all time domain exponential decays to zero and no oscillation happens (Fig. 3.3a). The system is then referred to as a stable system such as amplifiers. Conversely, if s_p falls in the right

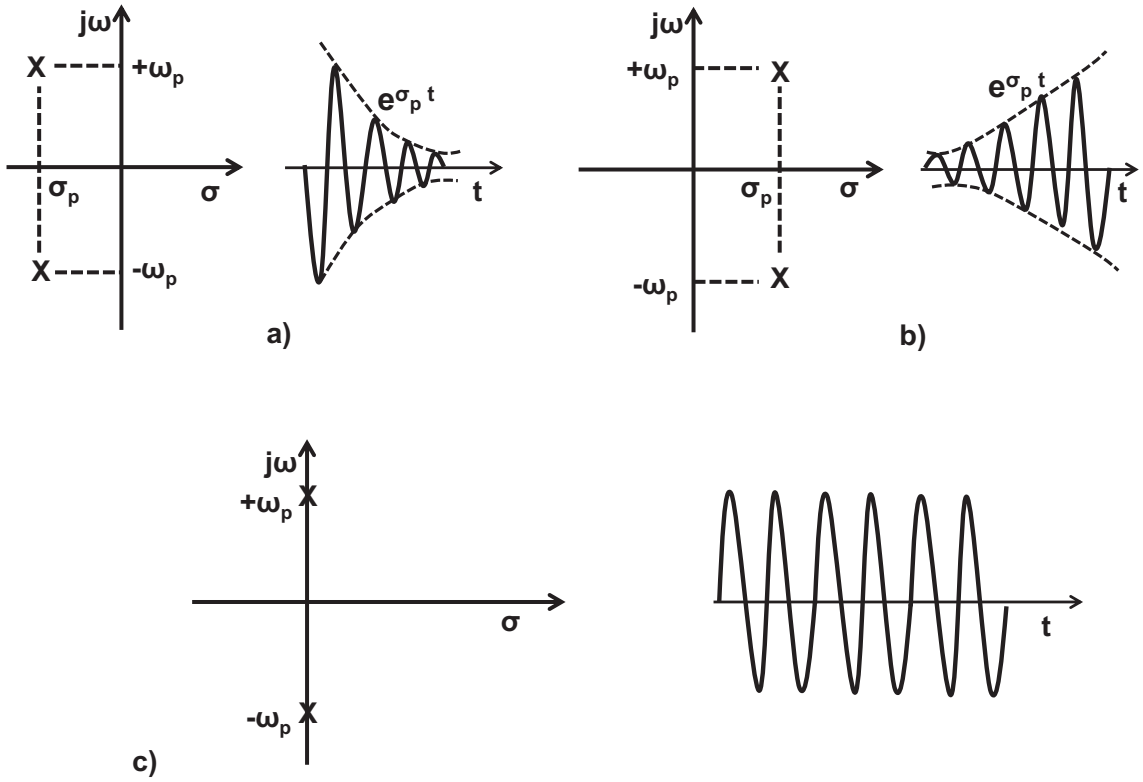


Figure 3.3: Time domain response of a system versus the position of poles: a) Stable with decaying amplitude of oscillation/not oscillating b) Unstable with increasing amplitude of oscillation. c) Unstable with constant amplitude of oscillation (Desired).

half plane, i.e., if $\sigma_p > 0$, then the system is likely to oscillate because its time domain response exhibits a growing exponential (Fig. 3.3b). Even when $\sigma_p = 0$, the system may sustain oscillations (Fig. 3.3c).

3.2.2 LC Oscillator

Oscillator Stability: As we know a simple LC resonance circuit ceases to oscillate primarily due to imperfectness of the inductor, L which gives rise to resistive losses, that determines the quality factor, Q of the inductor/LC tank. The resistive loss, R_p is eliminated by the design of a latch circuit that essentially acts as a negative resistance to nullify the

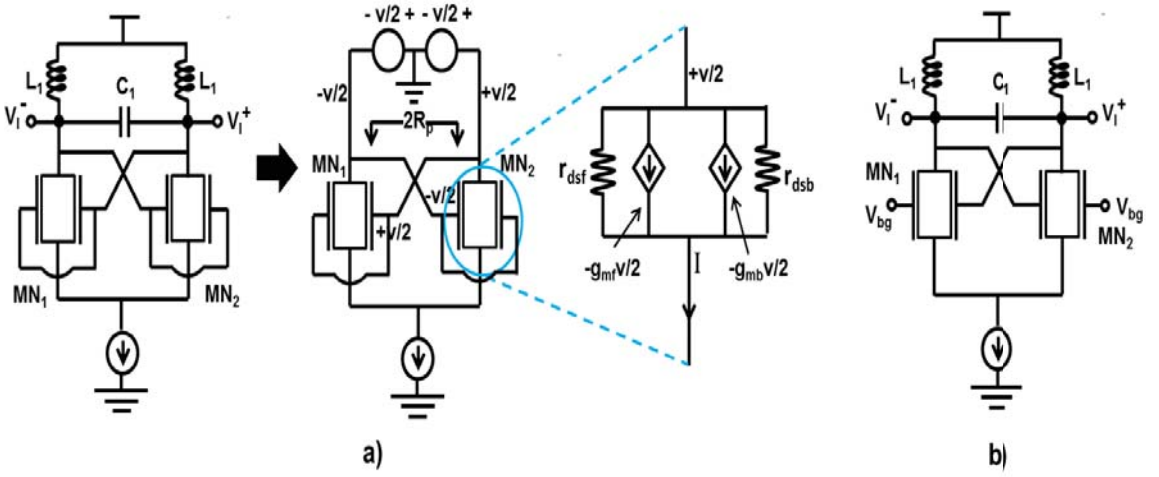


Figure 3.4: a) The negative resistance LC oscillator in common mode DG-MOSFET. At resonance, the LC tank becomes resistive only and the latch circuit acts as negative resistance to nullify its effect. The small signal analysis of a DG-MOSFET is focussed to study the criterion for oscillation. b) The independent mode tunable DG-MOSFET LC oscillator [13].

effect of positive resistance of the lossy tank. The condition to oscillate for the single gate CMOS based LC oscillator is given by [58], [77], [13]

$$g_m R_p \geq 1 \tag{3.6}$$

In this section, we analyze via small signal model the criterion for oscillation of the negative resistance common mode LC oscillator [77], [13]. The criterion is found to be less stringent than that of its single gate CMOS counterpart. To start with the analysis, we design an equivalent differential circuit of the LC oscillator and focus on transistor MN_2 as depicted in Fig. 3.4a. The current, I, determined from the analysis is given by [13],

$$I = \frac{\frac{V}{2}}{r_{dsf} + r_{dsb}} - \frac{(g_{mf} + g_{mb} + \delta g_{mc})V}{2} \tag{3.7}$$

The factor δg_{mc} arises due to a small coupling effect between the two gates of the DG-MOSFET [13]. The DG-MOSFET considered here operates in common mode configuration (two gates are joined) and therefore we can safely assume $g_{mf} = g_{mb} = g_m$

and $r_{dsf} = r_{dsb} = r_{ds}$ [77], [13]. Therefore, the current is modeled as [13],

$$I = \frac{V}{4r_{ds}} - \left(g_m + \frac{\delta g_{mc}}{2}\right)V \tag{3.8}$$

Ignoring r_{ds}, since $g_m >> \frac{1}{r_{ds}}$ in today's transistor, we have,

$$I = -\left(g_m + \frac{\delta g_{mc}}{2}\right)V \tag{3.9}$$

The input resistance of the oscillator (loss of the tank), $2R_p = \frac{V}{I}$ (Fig. 3.4a) is given by,

$$2R_p = -\left(\frac{1}{g_m + \frac{\delta g_{mc}}{2}}\right) \tag{3.10}$$

To sustain oscillation, the negative resistance must cancel the loss of the tank [58]. Therefore,

$$2R_p \geq \frac{1}{g_m + \frac{\delta g_{mc}}{2}} \tag{3.11}$$

After a few steps of arithmetic and rearrangement,

$$g_m R_p \geq \frac{1}{2} - \frac{R_p \delta g_{mc}}{2} \tag{3.12}$$

Assuming δg_{mc} of the order of a few μS, and $R_p (R_p = QX_L)$ of the order of a few kΩ for mm-wave application, the inequality, $R_p \delta g_{mc} << 1$, can be easily validated. Rewriting eqn. (3.12) [13],

$$g_m R_p \geq \sim \frac{1}{2} \tag{3.13}$$

Comparing eqns. (3.6) and (3.13) it becomes obvious that the criterion for oscillation of a DG-MOSFET negative resistance LC oscillator is more lenient than its counterpart in conventional CMOS. The more leniency implies the inductor Q can afford to be inferior to sustain the oscillation [77], [13]. It is to be noted that since the combined g_m (of two gates) of DG-MOSFET is much higher than the g_m of conventional CMOS [78] it can be safely

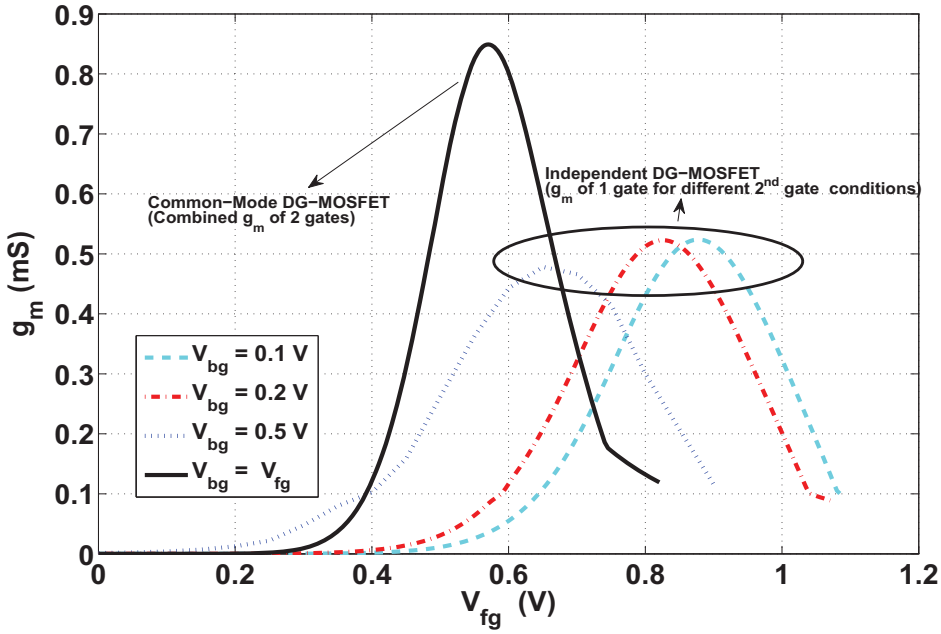


Figure 3.5: Comparative g_m plots of common and independent mode DG-MOSFETs [13].

assumed that the g_m of a single gate of a DG-MOSFET is approximately equal/comparable to the g_m of a conventional CMOS [77], [13]. To give an idea to the reader, the g_m curve of the common-mode DG-MOSFET is plotted and compared with its independent mode counterpart in Fig. 3.5. The g_m of the single gate in the independent mode DG-MOSFET operation depicts conventional CMOS. The observed phase noise of the LC oscillator is -133 dBc/Hz at 1 MHz offset for the 60 GHz carrier frequency (Fig. 3.6) for the common mode operation [77], [13].

Voltage Control Characteristics: The DG-MOSFET LC VCO considered in this section works in the independent mode operation (Fig. 3.4b). The VCO is tuned via back gate for controlling the oscillation frequency. The advantage of the DG-MOSFET LC VCO lies in the fact that it uses no MOS varactors.

Unlike the oscillation frequency trait of the VCO implemented in single gate CMOS with MOS varactors, the oscillation frequency in the compact DG-MOSFET LC VCO

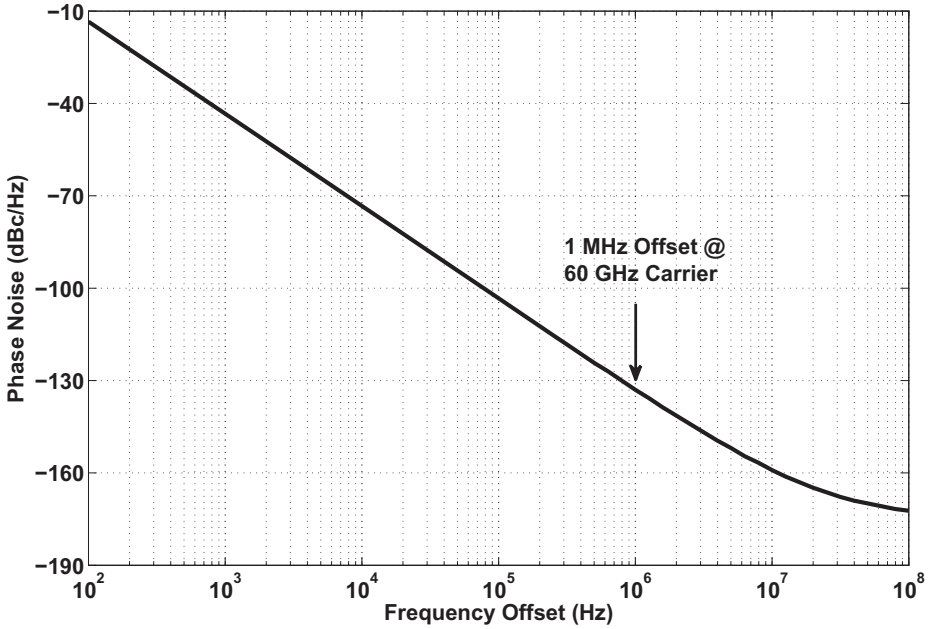


Figure 3.6: The phase noise of the LC oscillator at 60 GHz. The phase noise at 1 MHz offset is observed at -133 dBc/Hz in the linear time variant model [13].

decreases with increase in voltage once the threshold (V_T) is reached (Fig. 3.7) [13]. This is because the inversion charge density, Q_i, varies proportionally to $C_{ox}(V_{bg}$ - $V_T)$ in both the linear and saturation regions [29], where C_{ox} is the oxide capacitance. Therefore as V_{bg} increases beyond V_T, Q_i increases. The increase in Q_i results in the increase of the total gate capacitance of the back gate (C_{bg}) which in turn lowers the oscillation frequency, f. It should be noted that beyond V_T, C_{bg} only depends on C_{ox} [29]. The oscillation frequency beyond V_T is given as [13],

$$f = \frac{1}{2\pi\sqrt{L_1(C_1 + C_{bg})}} \tag{3.14}$$

A novel formulation can be devised for the characteristic of the DG-MOSFET LC VCO which can be written as follows [13],

$$f = K_{DGVCO}(V_{bg} - V_T) + f_c \tag{3.15}$$

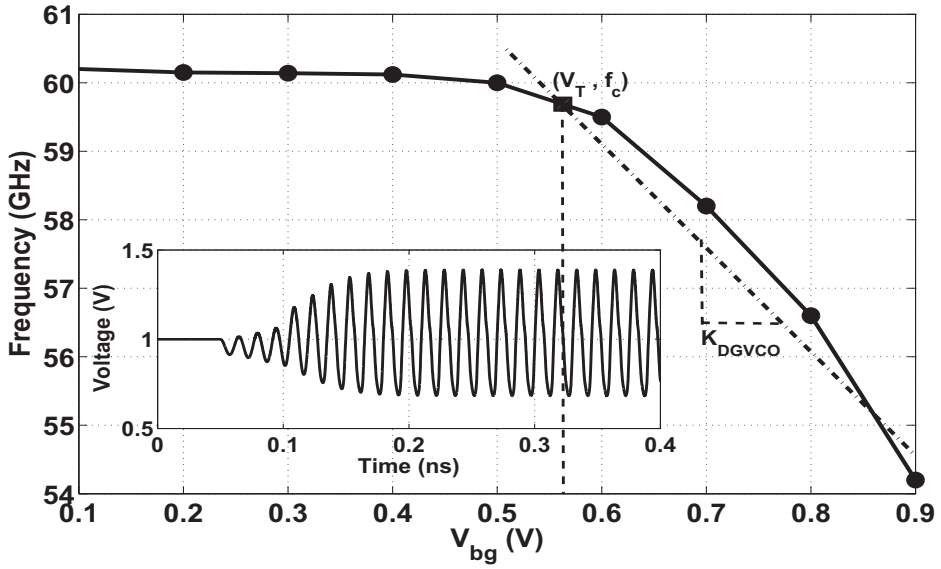


Figure 3.7: The frequency tuning with back gate bias for the independent mode LC Oscillator. Inset: The output waveform of the DG-MOSFET LC oscillator at 60 GHz [13].

The slope of the characteristic, K_{DGVCO}, is termed the sensitivity of the DG-MOSFET VCO and is a negative quantity as can be observed from the curve fitting of the oscillator characteristic in Fig. 3.7. In the above equation, f_c is the oscillation frequency in the subthreshold region of the back gate of the devices and is given as [13],

$$f_c = \frac{1}{2\pi\sqrt{L_1 C_1}} \tag{3.16}$$

The voltage response of the oscillator at 60 GHz can be observed from the inset of Fig. 3.7.

Quadrature Extension: We now extend our basic LC oscillator design with DG-MOSFET to a shunt coupled quadrature LC oscillator (Fig. 3.8) in which the waves are generated at 90° phase difference. Two identical oscillators are coupled to operate in quadrature. The voltage swing of this oscillator at a frequency of 60 GHz is shown in Fig. 3.9. The quadrature oscillator is the key to QPSK modulation and thus plays a significant role in wireless communications. The quadrature extension of the LC VCO is also a classic example of independent mode DG-MOSFET.

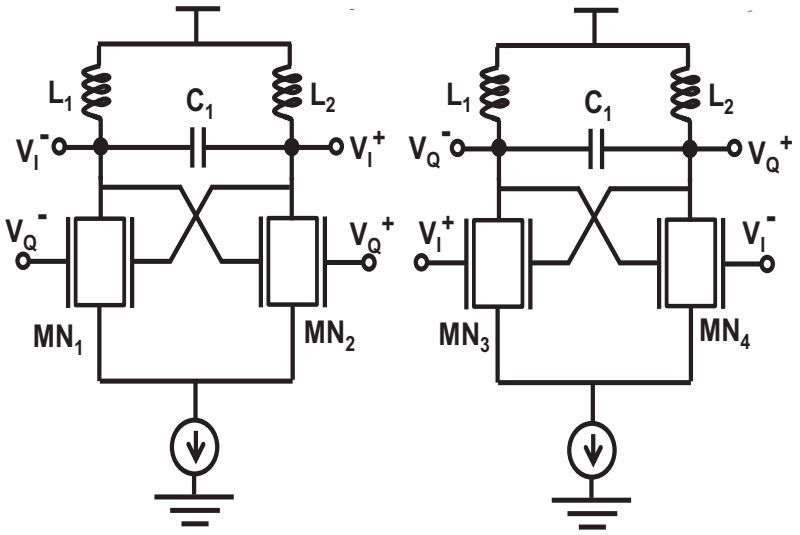


Figure 3.8: The LC quadrature oscillator implemented with only four DG-MOSFETs in independent DG mode configuration [13].

Also, quadrature LO signals are used in wireless systems for image-rejection or in down-conversion and recovery of the in-phase and quadrature components of the received QPSK modulated signal [79]. The simple compact DG-MOSFET Q-VCO explored here can be an alternative to the more complex CMOS based architectures reported in [80]-[84].

The transistor count of the oscillator is reduced by half from eight required in the bulk CMOS technology to four in the DG-MOSFET version [13]. Although the reduction in transistor count reduce power consumption, as it depends primarily on the current which remains same, the reduction certainly makes it faster by reducing parasitics and is area efficient.

The coupling factor, α, of an quadrature oscillator is defined as the ratio of the width of the coupling transistor to the width of the switching transistor [58]. In case of DG-MOSFET, since the transistor is the same MN_x, the switching transistor can resemblance the front gate, while the coupling transistor can resemblance the back gate of MN_x.

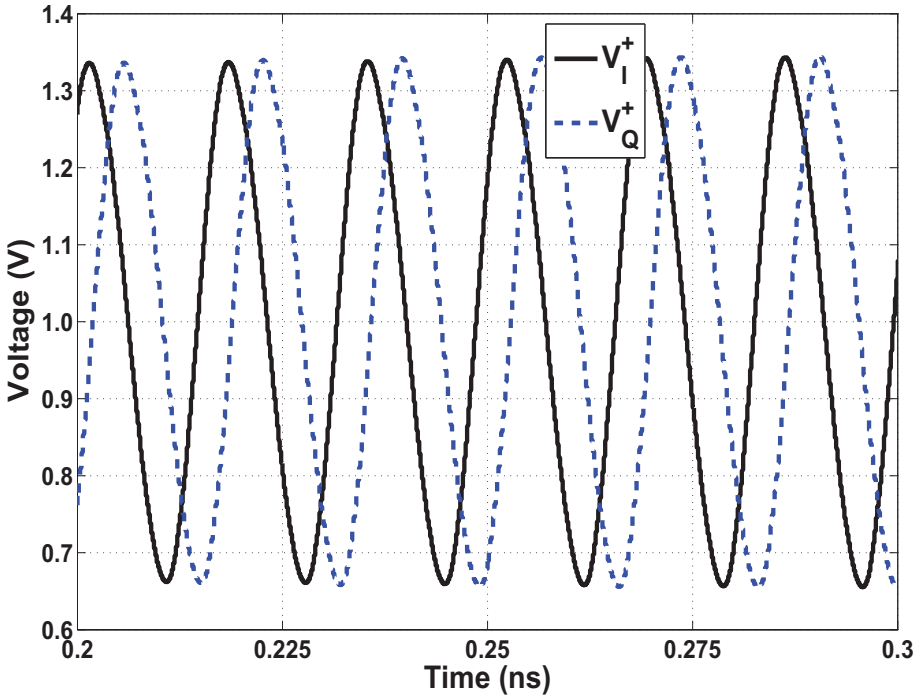


Figure 3.9: The voltage swing of the DG-MOSFET LC quadrature oscillator. The waves are generated at 90° phase difference at a frequency of 60 GHz [13].

Therefore, α is defined for DG-MOSFET as [13],

$$\alpha = \frac{W_{bg}}{W_{fg}} \tag{3.17}$$

and is unity since the widths of the front (W_{fg}) and back gates W_{bg} of MN_1 are usually identical. The first reported single gate MOSFET QVCO [85] is designed with α equals to unity. As we are aware of the inverse proportionality between the coupling factor and the phase error, the phase error is naturally minimised for the DG-MOSFET QVCO based architecture. However, the phase noise increases due to the high coupling factor. The phase noise at 1 MHz offset is observed to be -107 dBc/Hz (Fig. 3.10) and the phase error, defined as the phase difference from 90° between I and Q signals, is 0.6°.

The coupling strength, m, defined as the ratio of the transconductance of the the coupling pair (G_{mc}) to the transconductance of negative resistance pair (G_m) ($m = G_{mc}/G_m$)

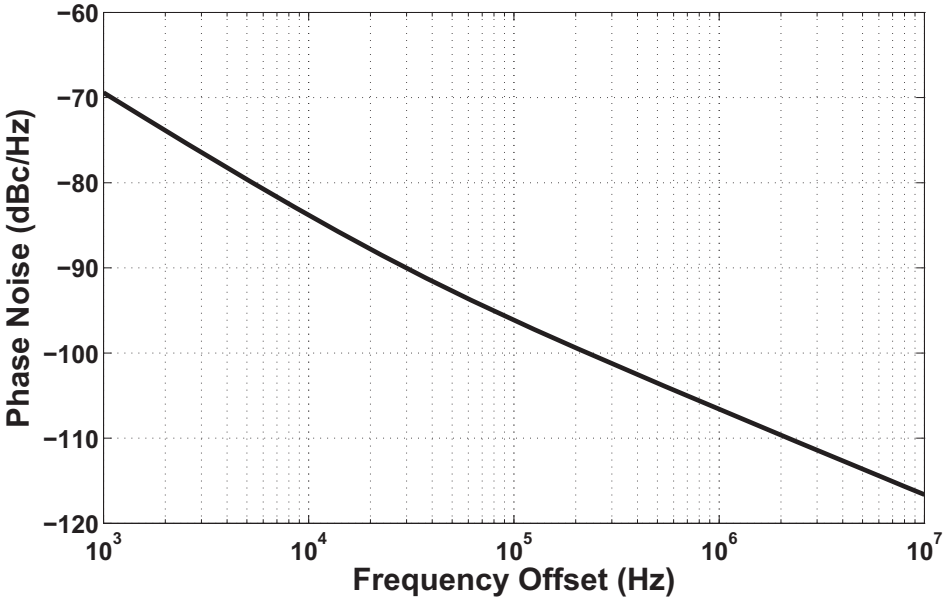


Figure 3.10: The phase noise of the quadrature LC oscillator at 60 GHz. The phase noise at 1 MHz offset is observed at -107 dBc/Hz in the linear time variant model [13].

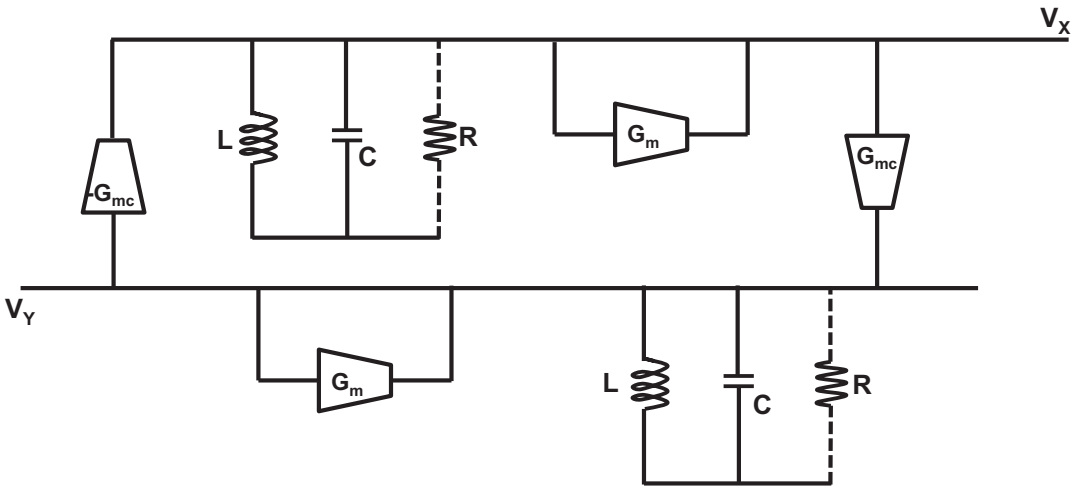


Figure 3.11: Linear model for the negative resistance Quadrature Voltage Control Oscillator [13].

is given as [80],

$$m = \frac{W_{bg}}{W_{fg}} \tag{3.18}$$

Taking into consideration the equality, $W_{fg} = W_{bg}$, and from eqn. (3.18), the coupling strength of the DG-MOSFET QVCO is also determined to be unity [13]. A linear model illustrating these transconductances is introduced in Fig. 3.11.

3.2.3 Relaxation Oscillator

The circuit proposed in [15] is a modified version of a CMOS based current controlled relaxation oscillator [86]. The novel dimension in the DG-MOSFET oscillator circuit (Fig. 3.12) is the exclusion of a comparator circuit by the cleverly utilization of back gate tuning available in DG-MOSFET, making the circuit faster as well as area and power efficient. The back gate bias, V_{bg}^{n}/V_{bg}^{p} plays the role of the comparator "V_{ref}" alongside of the precise frequency tuning. This makes the oscillator acts also as a VCO.

The DG-MOSFET implementation of an ICO/VCO relaxation oscillator has two other advantages, firstly it can be used also as a VCO by virtue of the back gate bias and secondly it operates more efficiently with a higher upper limit as a result of very high transconductance of DG-MOSFETs [87]. Although the accessible frequency range in the VCO mode is dwarfed in contrast to massive ICO response given in logarithmic scale (Fig. 3.13), the operation as a VCO provides the circuit with an extra degree of freedom in tuning. Specifically, the voltage operated fine 'vernier' frequency tuning sets a frequency with precision after it has been 'coarsely' selected by the current operated crude logarithmic tuning [14].

The oscillator consists of a dual input S/R latch, driven directly with equal copies of the input current obtained via two current mirrors. The current from these two branches are the basis of current-controlled operation and are alternately switched via tail inverters that are driven from the S-R latch's outputs ($Q/\bar{Q}$).

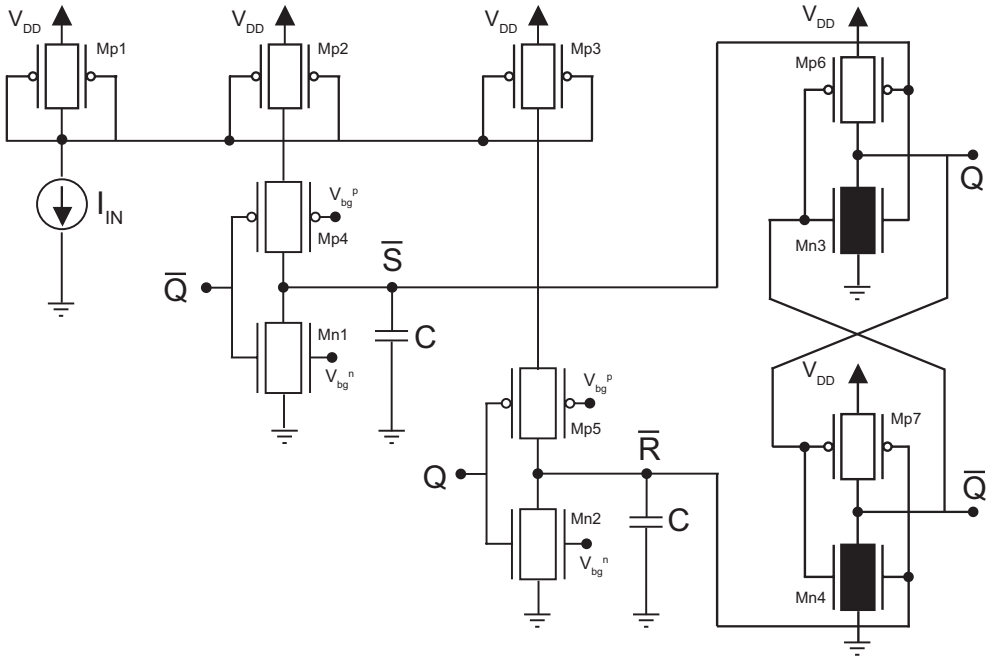


Figure 3.12: The dual-input S/R latch relaxation oscillator circuit built using DG-MOSFETs [14], [15].

The two inverters consist of Mp4/Mn1 and Mp5/Mn2, and are biased with equal copies of the input current, I_{in}, from the current mirrors implemented with three DG-pMOSFETs Mp1, Mp2 and Mp3. The back gate of the two inverters Mp4/Mn1 and Mp5/Mn2 are tuned to vary the frequency. In other words, the voltage control is possible because the inverters can be frustrated/facilitated by the bias in their back-gates. This fine voltage controlled frequency tuning can be implemented in a couple of manners as discussed later in the section. The presence of the two capacitors (C) in the inverters output add yet another degree of freedom to achieve variable frequencies (Fig. 3.13) [14].

It can also be noted that, the NOR gates used to construct the S-R latch consist of only four DG-MOSFETs as opposed to eight required in conventional CMOS architecture. This is possible by using *high-threshold* independently-biased n-MOSFETs and leads to conserve circuit area and reduce parasitics [88].

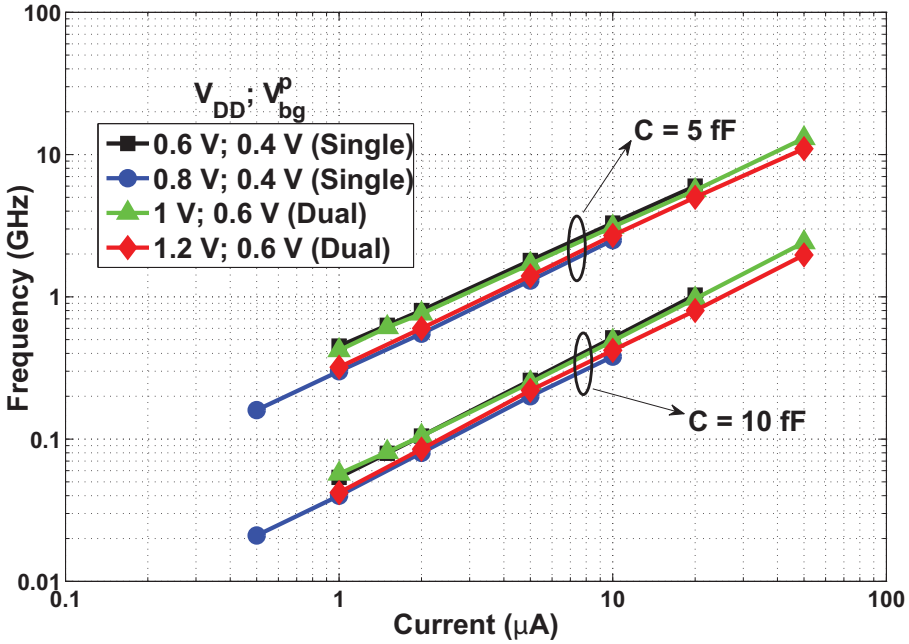


Figure 3.13: The 'crude frequency tuning' of the oscillator, varying I_{in} for two different capacitances [14].

To get an insight into the working principle of the circuit, assume an initial condition when Q is high and $\bar{Q}$ is low. This charges the capacitor C (associated with node $\bar{S}$) and activates Mn3 which makes Q to be discharged and become low. At that instant, Mp7 also gets activated enabling $\bar{Q}$ to go high. This cycle keeps repeating and the instability makes the circuit oscillating. This is illustrated in Fig. 3.14 for three different single bias conditions [14].

The phase noise of this oscillator is found to be -104 dBc/Hz at 1 MHz offset measured for a 1 GHz carrier (Fig. 3.15). The circuit topology works for both single and dual bias configurations as explained below.

Single-Bias Voltage Control: In this configuration, where $V^n_{bg} = V^p_{bg}$, the back gates of pMOSFETs (Mp4 & Mp5) and nMOSFETs (Mn1 & Mn2) are tied to the same supply.

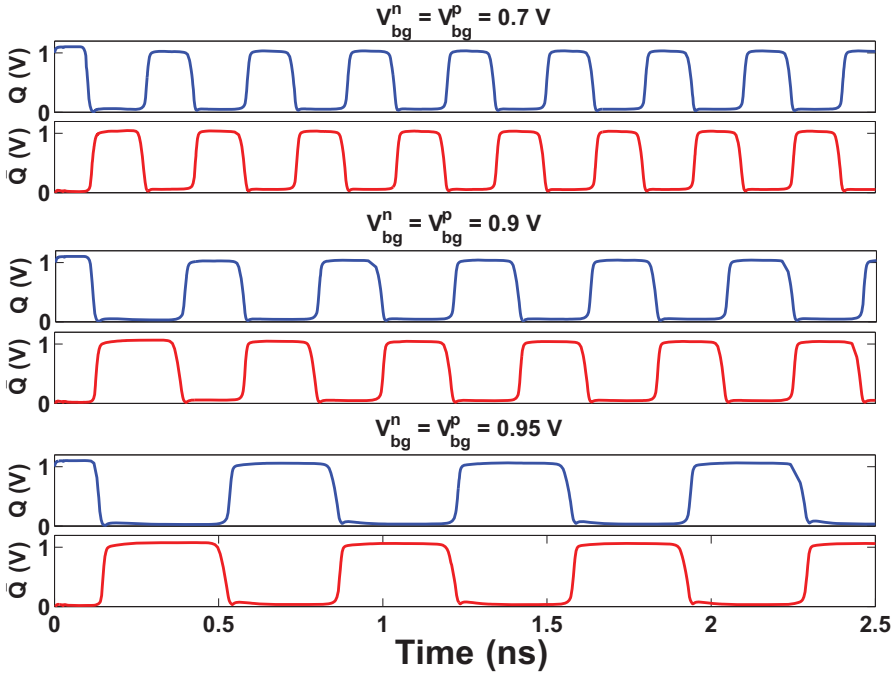


Figure 3.14: The oscillation of the relaxation oscillator at V_{DD} = 1.1 V and I_{in} = 70 μA for three back gate biases. The tuning characteristics is evident from altering frequency with back gate bias.

As the biasing increases in pMOSFETs ($V^n_{bg} = V^p_{bg}$ gets higher), smaller currents can pass through Mp4 & Mp5 and the frequency drops as can be observed from Fig. 3.16. It is also observed, a higher V_{DD} results in a slower oscillation at a fixed input current, because the SR Latch takes longer time to reach a higher switching threshold ($\sim \frac{1}{2}V_{DD}$) as V_{DD} is increased. At a low current of 2 μA and a supply of 0.6 V the frequency remains constant until $V^n_{bg} = V^p_{bg}$ = 0.3 V after which the frequency drops at a steady rate from 100 MHz to ~ 20 MHz. This region where the frequency varies can be used for the purpose of fine tuning as discussed earlier. With the increase of current we can extend the domain for this fine tuning. For instance, when the current is changed to 10 μA the fine tuning is implemented in the region of 90 MHz - 700 MHz for a supply of 0.8 V as can be verified from Fig. 3.16 [14].

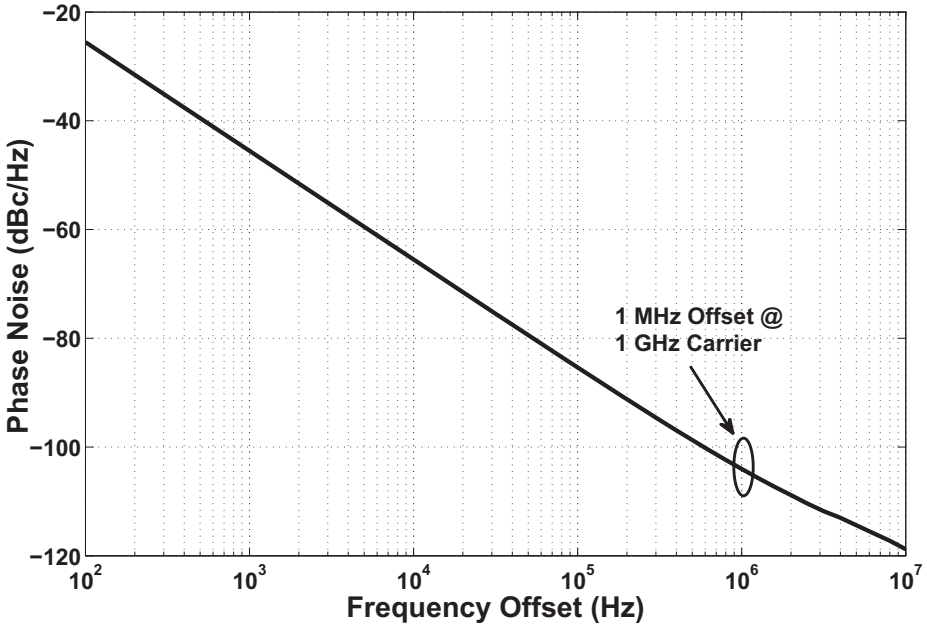


Figure 3.15: The phase noise of the oscillator at 1 GHz. The 1 MHz offset is observed at -104 dBc/Hz.

Dual-Bias Voltage Control: Here, the back gate biases of DG-pMOSFETs (Mp4 & Mp5) and DG-nMOSFETs (Mn1 & Mn2) are related according to the equation, V_{bg}^{n} = V_{DD} - V_{bg}^{p}. Therefore the biases of DG-pMOSFETs and DG-nMOSFETs are inversely related. When the back gate bias on the DG-nMOSFET is minimum and increases, the back gate bias on the DG-pMOSFET slowly reduces, thus in effect both DG-MOSFETs can switch easier than before resulting in an improved frequency of oscillation (Fig. 3.17). It is observed that the frequency does not vary much once the $V_{bg}^{n} = V_{bg}^{p} = \frac{V_{DD}}{2}$ is reached in all cases. This is because going to a higher back gate bias the thresholds of DG-MOSFETs are not substantially lowered anymore and there is no additional current to improve switching speed. The frequency domain is selected in a similar way to that described for the single bias case [14].

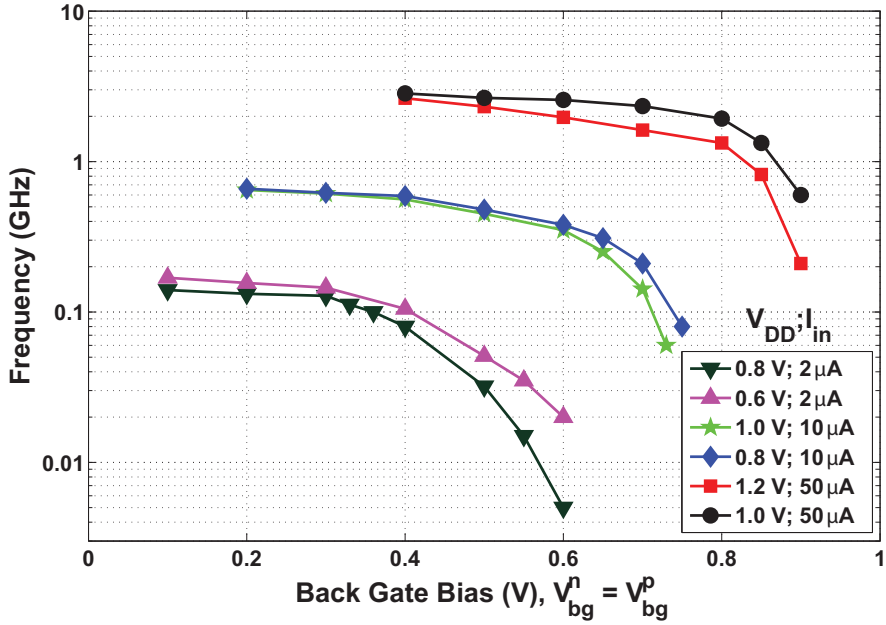


Figure 3.16: The frequency tuning for Single-Bias ($V_{bg}^{n} = V_{bg}^{p}$) Voltage Control [14].

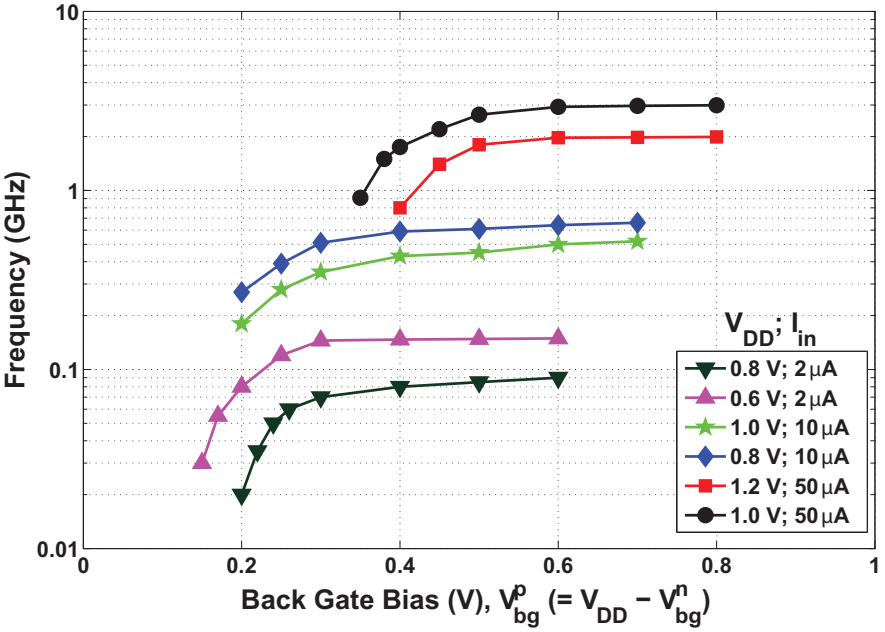


Figure 3.17: The frequency tuning for Dual-Bias ($V_{bg}^{n} = V_{DD}$ - V_{bg}^{p}) Voltage Control [14].

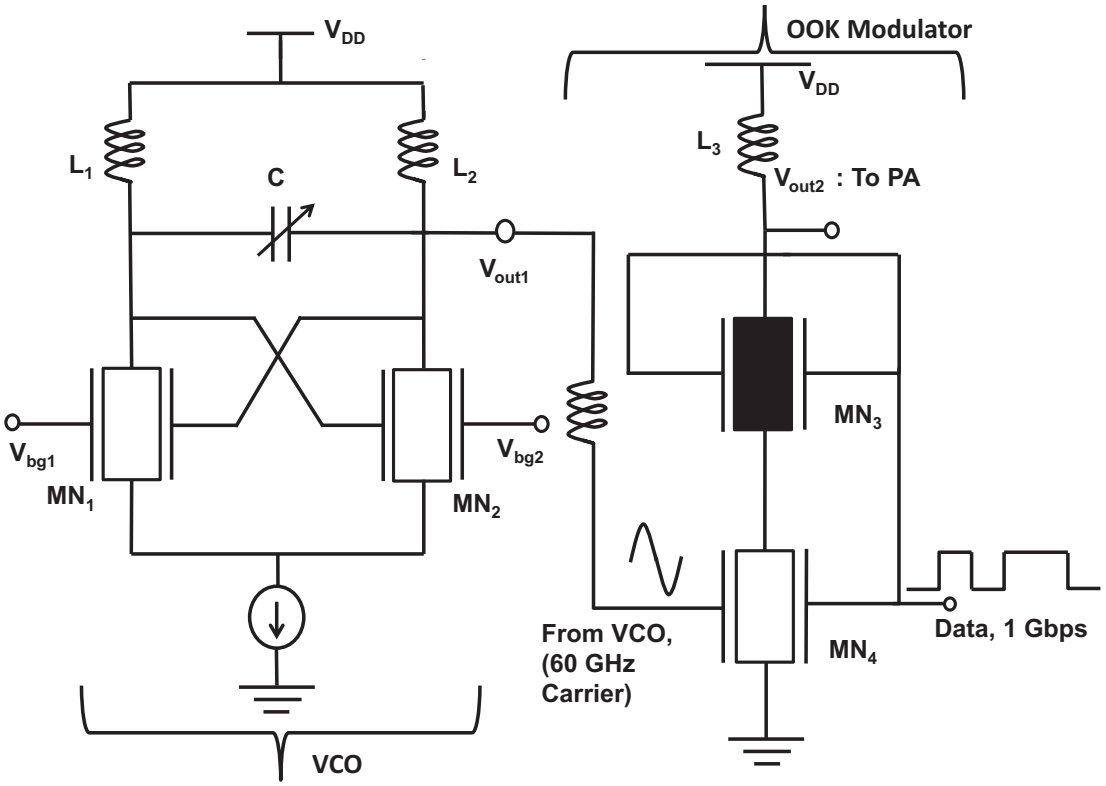


Figure 3.18: The OOK Modulator circuit with the VCO. The DG-MOSFET OOK Modulator uses only two DG-MOSFET for modulation and switching [14], [16].

3.3 OOK Modulator

The novel DG-MOSFET based OOK Modulator consists of only two transistors making it ideal for use in ultra compact and/or low-power systems (Fig. 3.18). The modulator can work up to a data rate of 5 Gbps without any discernible distortion for 60 GHz carrier. The DG-MOSFET MN_4 acts as the key OOK modulating device. The 60 GHz sinusoidal carrier from the VCO is fed into one of the gates of the transistor whereas the pulsed digital data is input to the other gate. The charge capacitive coupling of the two gates provided by the thin Si body determines the modulation, and therefore depends on the bias conditions of the two gates as well as device dimensions.

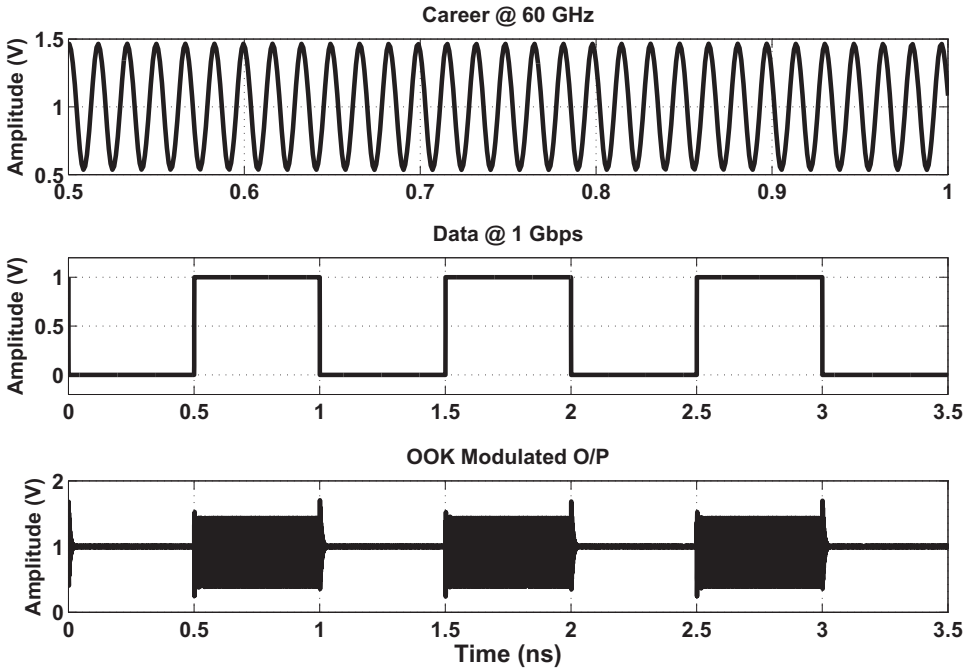


Figure 3.19: The OOK modulated output for a carrier frequency of 60 GHz and data rate of 1 Gbps. The input data sequence resembles 50% duty cycle [14], [16].

The modulation occurs when the device operates in the saturation or in cut-off region, that is when there is either a '1' or '0' respectively emanating from the pulsed digital data. In other words, the modulation takes place at all instants of time. The symmetric DG-MOSFET MN_3 acts as the switch and is kept at a high threshold voltage (filled symbol) for improved device electrostatics that maximizes the I_{ON}/I_{OFF} ratio. MN_3 is turned on at the 'HIGH' state of the pulsed data and remains off at the 'LOW' state, maintaining the principle of OOK Modulation scheme. The modulated output is obtained at the drain of MN_3. This is illustrated in Fig. 3.19. To maximize the power of the signal during transmission, the modulated output is fed to the Power Amplifier [14], [16].

3.4 Power Amplifier

The design of the wide band and high gain Power Amplifier (PA) is a challenging task, especially in ultra-compact MOSFETs with low output impedance. Consequently, in [1],

DG-MOSFET variant of two recent single-gate implementations of PA with competitive features in the GHz range are adapted, which allows a more fair performance comparison to be made between different devices.

In the first PA topology, the architecture in [89] is slightly modified for the DG-MOSFET to explore its gain and bandwidth characteristics as well as its tunability. The second topology reported here is a three stage single-ended, common-source (CS) PA similar to the one reported by Yao et al. [90] for conventional CMOS. The basic difference over the published topologies in both cases is the length of the DG-MOSFET devices (45 nm) that is substantially smaller. There are a number of reasons for this gate length choice. Firstly, the proposed PAs are essentially designed for low-power highly compact Si mixed-signal radio applications where the range and area will be typically quite limited. Secondly, the DG-MOSFET architecture is inherently a narrow width device technology in which very large number of fingers needed to obtain large W/L ratios. Finally, a PA is implemented for ultra-compact wide-band RF CMOS applications such as vehicular anti-collision radar. Given that DG-MOSFET technology is aimed for sub-22 nm digital technologies, 45 nm is a good compromise for analog circuit implementation [1], [14].

The sections will discuss in detail about these design modifications and provide their simulated response including gain tuning, peak gain, bandwidth and linearity.

3.4.1 Power Amplifier Basics

The PA is the final stage of transmitter design before signal transmission through antenna. They are responsible for amplifying the power level of the transmitted signal several times so that the received signal is above the sensitivity of the receiver which is calculated from the link budget analysis. The PAs are divided into various classes such as A, B, AB, C D, E, F etc. Among these classes A, B, AB and C incorporate similar design methodologies differing only in the biasing point. The Class A amplifier is the

most linear and is widely used in RF transmitter design although they have the least Power Added Efficiency (PAE). Several acclaimed literatures [58], [59] are available for interested readers on these concepts. This section of the dissertation focusses on the design of tunable DG-MOSFET Class A PA.

3.4.2 Power Amplifier Design

The circuit topology of the first wide band (3-33 GHz) DG-MOSFET PA is shown in Fig. 3.20, which consists of three DG-MOSFETs in a Darlington cascode arrangement. The common source transistor MN_1 operates in the symmetric mode while the two transistors MN_2 and MN_3 are configured for independent mode operation. The width of MN_1 is taken to be 1 μm while the width for transistors MN_2 and MN_3 are kept higher at 2.4 μm for better input return loss and optimized gain performance. MN_3 is biased at 2.6 V (V_{b1}). The back gate of the transistors MN_2 and MN_3 are biased for gain tuning. The resistors R_1 and R_2 complete a self biasing network for Class A operation. This modified DG-MOSFET darlington configuration is divided into two stages. The first stage is the series peaking stage and inter-stage matching, and the second stage is the output power stage [1], [14]

The series peaking circuit consisting of R_3 and L_1 increases the output load pull impedance, and also provides the peaking impedance for feeding forward signals. The inductor L_3 along with the source degeneration circuit consisting of R_4 and L_2 yields in real part wide band inter-stage impedance matching for maximizing the power transfer between the stages [1], [14]. The common source transistor MN_2 and MN_3 are connected in cascode.

The transistor MN_3 acts in common gate configuration and one of its gate is grounded with the aid of the peaking inductor L_4 and a bypass capacitor C_1 [89]. Along with achieving a near constant gain by maintaining the flatness, the bandwidth of the amplifier is also increased with the aid of this peaking inductor. A high pass L-network (L_5 & C_3) is used as the matching circuit [1], [14].

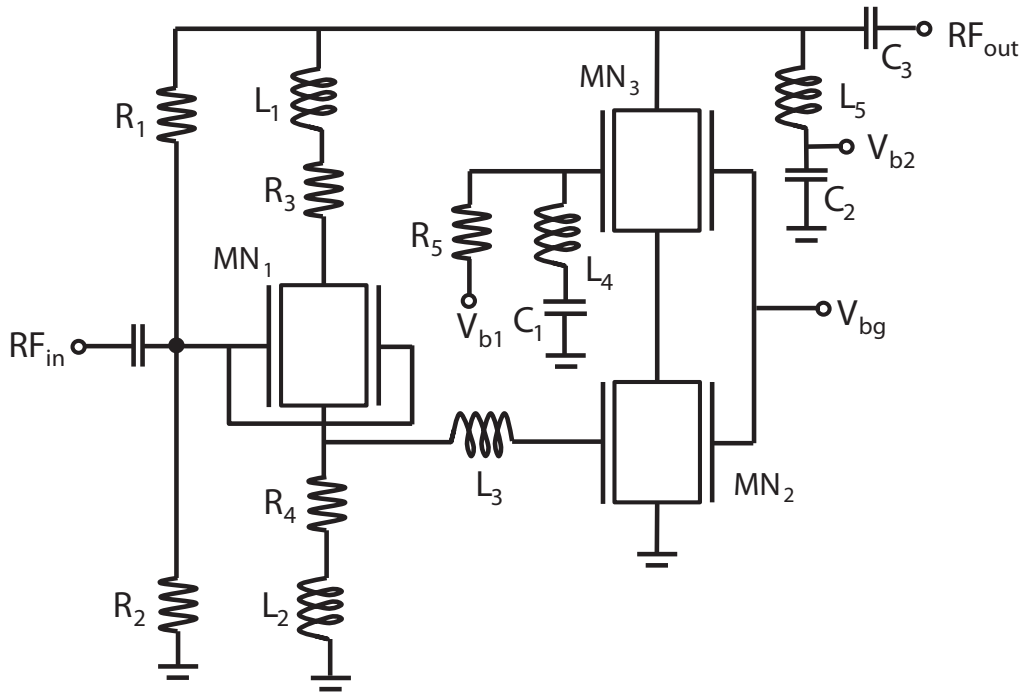


Figure 3.20: The DG MOSFET based power amplifier circuit in modified darlington cascode configuration. Transistors MN_1 operates in the symmetric mode while MN_2 and MN_3 operate in independent mode with the back gates used for dynamic tuning [14], [1].

In the second topology, the DG-MOSFET Class A amplifier is implemented in three stages (Fig. 3.21). Although the earlier cascode topology has higher & flatter gain, and larger output impedance, the CS configuration is advantageous in terms of the lower supply voltage required, leading to higher efficiency. All the transistors in this topology operate in the independent mode. The source degeneration inductors L_3, L_6 and L_9 along with the inter stage inductors L_4 and L_7 maximizes the power transfer and improves linearity [59]. The width of the three transistors are kept fixed at 1.2 μm. The source and the bias voltage (V_b) are both kept at 1 V [1], [14].

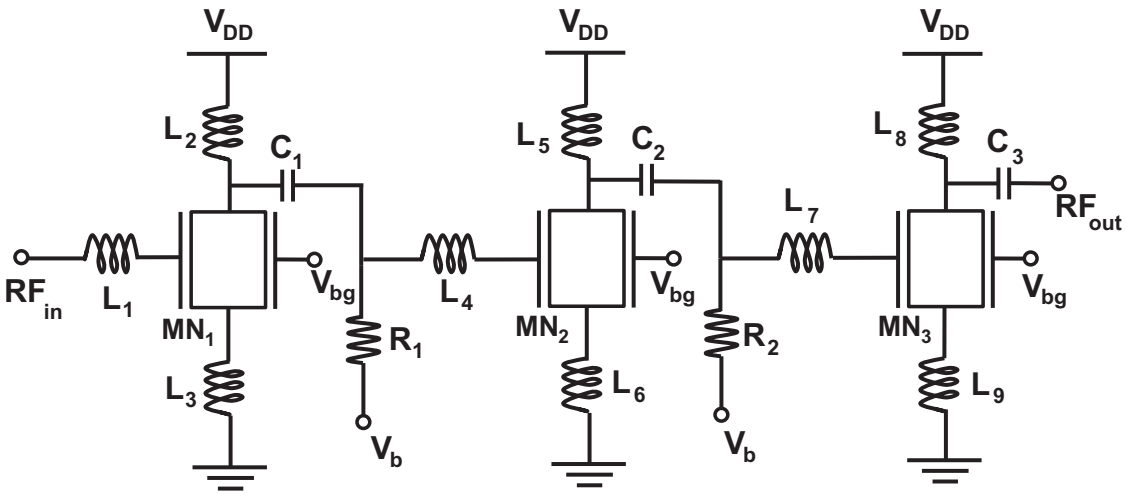


Figure 3.21: The three stage DG MOSFET based power amplifier circuit. All the three transistors operate in the independent mode [14], [1].

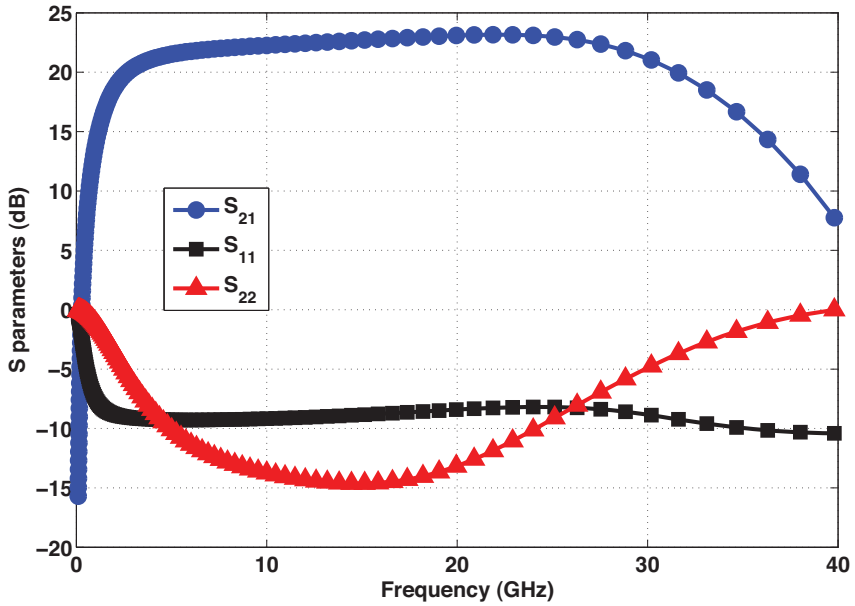


Figure 3.22: The S parameters which provide the gain (S_{21}) and reflection losses (S_{11} & S_{22}) of the power amplifier. This is measured for V_{bg} = 0.2 V [14], [1].

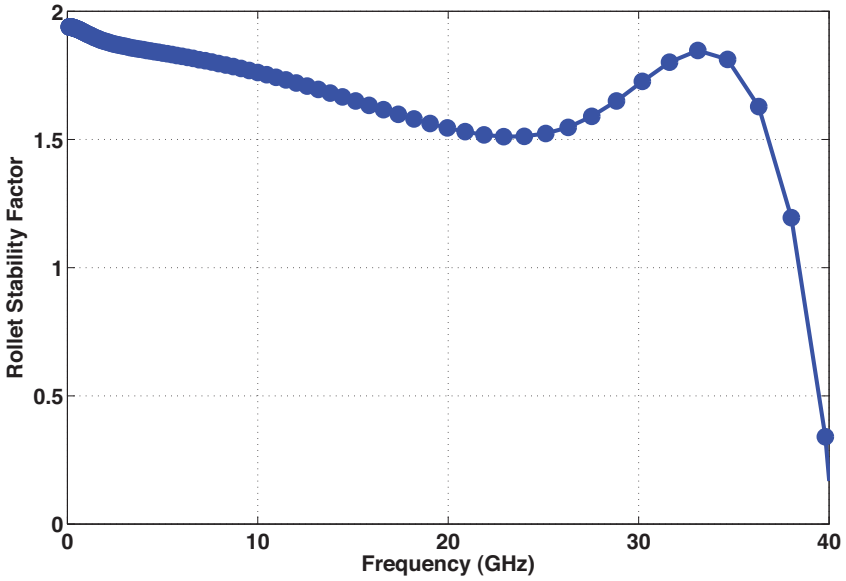


Figure 3.23: The rollet stability factor (K) is above unity in the operating range of 2 - 32 GHz verifying the amplifier to remain unconditionally stable in this range. K drops below unity beyond ~ 38 GHz [14], [1].

3.4.3 Simulation Results

For the darlington cascode topology, the simulation verifies the forward gain (S_{21}) to vary from 3 to 33 GHz, while maintaining a desired flatness (Fig. 3.22). The gain changes by less than 20% in this frequency range, attesting to the extreme flatness. The peak gain is observed at 24.5 dB. The input and output return losses (S_{11} & S_{22}) are also obtained from the simulation. Fig. 3.22 shows these S parameters at a V_{bg} of 0.2 V which is applied at the back gate of the transistors MN_2 and MN_3.

The unconditional stability of the amplifier is verified measuring the rollet stability factor, K which is given as

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\triangle|^2}{2|S_{12}S_{21}|} \tag{3.19}$$

$$\triangle = S_{11}S_{22} - S_{12}S_{21} \tag{3.20}$$

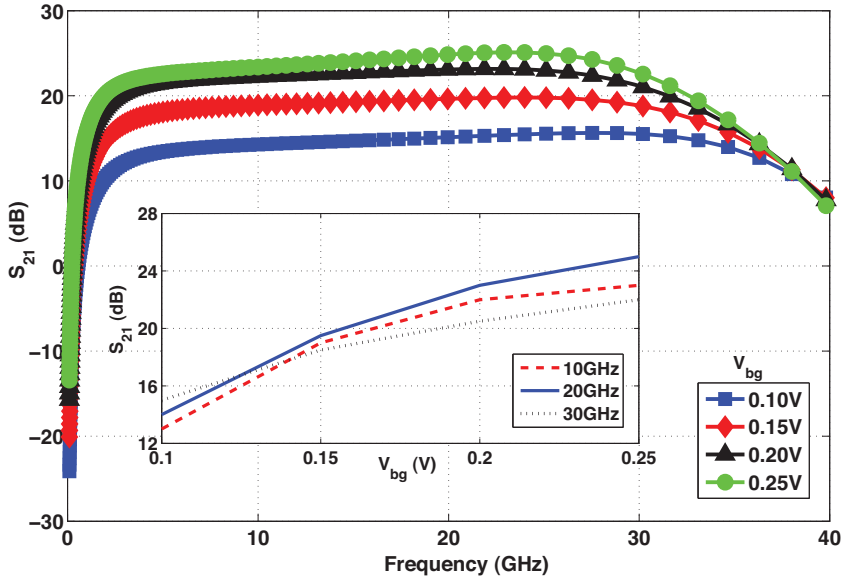


Figure 3.24: The back gate dependence of the gain is clearly evident. The gain changes by ~ 10 dB in the tuning range of V_{bg}. Inset: Gain variation with V_{bg} at different frequencies [14], [1].

The value of K is observed to be above unity in the operating frequency range indicating the unconditional stability of the amplifier (Fig. 3.23). The back gate tuning of the PA is verified from Fig. 3.24. The back gate voltage (V_{bg}) is varied from 0.1 V to 0.25 V for the operating frequency range during which the gain of the amplifier increases considerably. The range of gain tuning is observed to be limited to almost 10 dB. The inset of the figure shows the gain variation with V_{bg} at different frequencies. The 1 dB compression point (P_{1dB}) and the 3rd order Input Intercept Point (IIP_3) are found to be 11.9 dBm and 27.5 dBm, respectively, indicating the suitability of the circuit. The 15.6 dB difference between P_{1dB} and IIP_3 can be attributed to the scaling down of DG MOSFET to 45 nm [59]. The power added efficiency (PAE) and the fractional bandwidth (FB) of the amplifier is ~12% and 176% respectively [1], [14].

For the second topology involving the 3 stage CS PA, although the 3-dB bandwidth is ≥ 50 GHz, as evident from Fig. 3.25, for all cases of back gate voltages (see Fig. 3.26) a

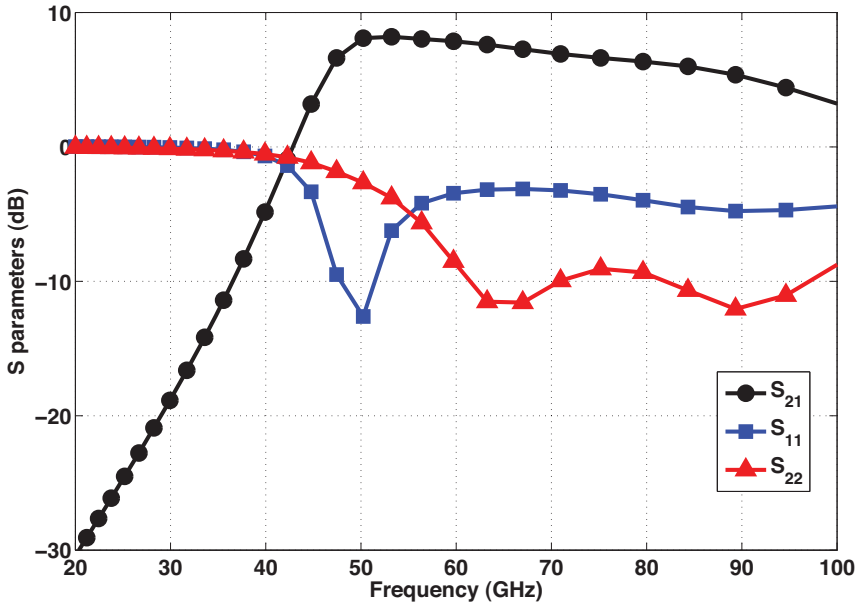


Figure 3.25: The S parameters which provide the gain (S_{21}) and reflection losses (S_{11} & S_{22}) of the power amplifier. This is also measured for V_{bg} = 0.2 V [14], [1].

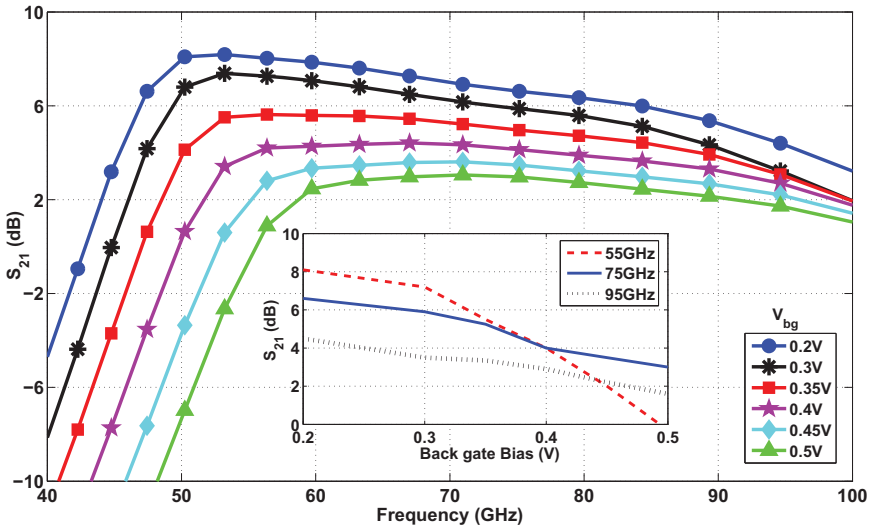


Figure 3.26: The back gate dependence of the gain is clearly evident. The gain changes by ~ 6 dB in the tuning range of V_{bg}. Inset: Gain variation with V_{bg} at different frequencies [1], [14].

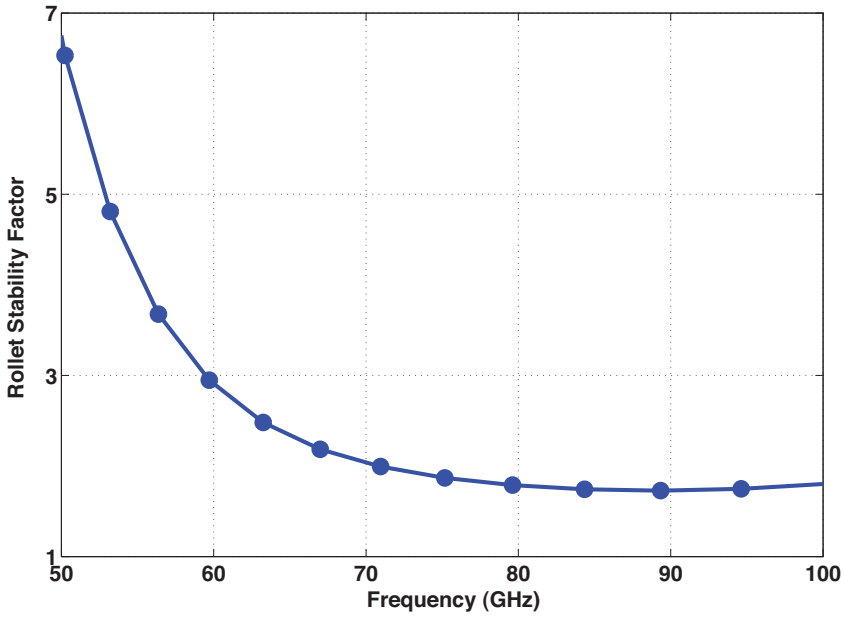


Figure 3.27: The rollet stability factor (K) is well over unity in the operating range of 60 - 90 GHz verifying the amplifier to remain unconditionally stable in the range [1], [14].

more realistic operating range of this amplifier can be considered to be in the range of 60 - 90 GHz. Once again, the inset of the Fig. 3.26 shows the gain variation with V_{bg} at different frequencies. The peak gain achieved is $\geq$ 8 dB. The rollet stability factor remains more than unity for this operating range as shown by simulated data in Fig. 3.27. The P_{1dB} and the IIP_3 are found to be 7.2 dBm and 19.8 dBm respectively. The PAE and the FB of this amplifier is ~14% and 40% respectively [1], [14].

3.5 Summary

The first section of the chapter introduces and analyzes the characteristics and beneficial features of oscillators designed with DG-MOSFETs, a technology expected to dominate in sub-32nm MOSFETs. Firstly, a less stringent oscillatory criterion of DG-MOSFET negative resistance common mode LC oscillator against conventional CMOS is shown quantitatively. Next, the advantageous feature of varying the oscillation frequency of

Table 3.1: Performance comparison of different wide band PAs [1]

Reference	Technology	Architecture	Frequency (GHz)	Gain (dB)	P_{1dB} (dBm)	PAE (%)	Fractional BW (%)
[89]	0.18 μm CMOS	Darlington cascode	4-17	8-12	15-17	11-16	123
[91]	0.5 μm E-mode pHEMT	Darlington cascode	0-16	10-13	7-18	N.A	200
[90]	90 nm CMOS	CS cascade	52-65	2-5.2	6.4	7.4	22.2
[16]	32 nm FinFET	CS cascade	60-100	6-8 (V_{bg}=0.2 V)	5.7	14	50
This work [1]	45 nm FinFET	Darlington cascode	3-33	15-26 (V_{bg}=0.25 V)	11.9	12	167
This work [1]	45 nm FinFET	CS cascade	60-90	5-8 (V_{bg}=0.20 V)	7.2	14	40

the negative resistance LC VCO without the usage of MOS varactors is discussed. The oscillation frequency is tuned via back gate voltage bias. The voltage control characteristic of this oscillator is quantitatively analyzed and supported with physical explanation and simulation verification. This is followed by the design of the quadrature version of the LC oscillator that involved reduced transistors counts from eight in conventional CMOS to four in this DG-MOSFET version, enabling faster performance by reducing parasitics. The coupling strength of the quadrature oscillator is unity.

After this, a novel relaxation oscillator is introduced, in which the comparator circuit required in conventional CMOS is omitted by utilizing back gate tuning of the DG-MOSFET, making the circuit faster as well as area and power efficient. Finally, the VCO operation of the relaxation oscillator via back gate biasing, in addition to the existing ICO operation, is introduced. The back-gate biasing provides the circuits with an additional degree of freedom that is particularly useful for fine 'vernier' tuning of frequency, a feature not possible in conventional CMOS without resorting to additional transistors. The back gate introduction does not lead to excessive phase noise in both the proposed architectures.

In the second section of the chapter, a novel DG-MOSFET OOK Modulator has been proposed. The circuit is designed only with two DG-MOSFETs, one for modulation and another high threshold device for strong switching.

At last, this chapter presents an compact, wide-band, high-efficiency PA designed in DG-MOSFET. The work validates DG-MOSFET to be a viable alternative to conventional CMOS in PA design where range and area are limited. The simulated results of the two PA topologies affirm significant improvements in bandwidth, flatness and peak gain over conventional CMOS and III-V technologies. Moreover, dynamic gain tuning available in the proposed PA implementations cannot be efficiently achieved with conventional single-gate MOSFETs without additional area overhead.

4 DG-MOSFET OOK Receiver

4.1 Introduction

In this chapter, DG-MOSFET circuits developed as part of a simple, efficient OOK receiver system is explored. The receiver compliments the transmitter design introduced earlier and can impact performance of wireless communication systems just as dramatically.

The front end of the non-coherent OOK receiver consists of a Low Noise Amplifier and Envelope Detector as depicted in Fig. 4.1. In this chapter, the analysis and design of these two components in DG-MOSFET technology are investigated.

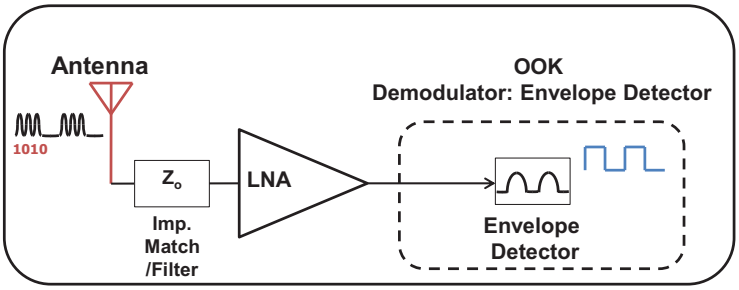


Figure 4.1: OOK Receiver block diagram.

4.2 Low Noise Amplifier

The DG-MOSFET LNA considered for the research [2], [14] follows the widely popular common source (CS) inductive degeneration topology. The following three specific beneficiary features are addressed in the research,

- The better area efficiency of the DG-MOSFET CS inductive degeneration LNA than a conventional CMOS based structure is analyzed and verified quantitatively.

- A novel LNA in this topology is designed at 60 GHz that has comparable FoMs with some of the recent 60 GHz LNAs designed in different conventional technologies. This is followed by another LNA designed at 90 GHz. Here the inductors in the circuit are replaced by microstrip transmission lines. The FoMs are also comparable to some recent mm-wave designs which asserts the compatibility of the DG-MOSFET LNA for the sub THz regime.

- The advantage of gain switching in DG-MOSFET LNA over its CMOS counterpart is explained qualitatively and demonstrated with the design of a novel 60 GHz novel two-stage common source cascade inductive degeneration LNA in 45 nm DG-MOSFET. The gain switching properties is studied via the tuning of its back gate that leads to variable and reconfigurable device performances not found in comparable amplifiers built with conventional CMOS architectures without resorting to additional hardware.

4.2.1 Low Noise Amplifier Basics

The LNA or Low Noise Amplifier is the first active block in the receiver chain and follows the antenna. The performance of the receiver depends significantly on the LNA, hence stringent design considerations are followed in its implementation. The primary metrics that determine the quality of design of an LNA are stated.

Noise Figure: The LNA should have a low noise figure as the name suggests. The noise figure of the LNA directly adds to the receiver. The LNA is followed by a plethora of blocks that too contributes noise to the receiver. Therefore it is essential to minimize the LNA NF to reduce the cumulative NF in the receiver. According to Friis equation [58] the NF of the first few blocks add more to the total receiver NF than that of the later blocks. This has been exemplified earlier in Section 2.6.2.

Gain: LNA is an amplifier and therefore it should provide sufficient gain to the incoming signal at the frequency band of interest. The signal retrieved by the antenna is usually of considerable low power, hence the necessity to amplify arises to implement downconversion, demodulation and other signal processing stages later in the receiver chain. Moreover, the gain of the LNA must be large enough to minimize the noise contribution of the subsequent stages of the receiver. However, the gain should not be too large because it will then reduce the linearity of the subsequent stages. Considering these trade-offs, the gain optimisation of the LNA is a significant step in its design. Input Return Loss: The off-chip band select filter interposed between the antenna and the LNA is typically designed and characterized as a high frequency device with a standard termination of 50 Ω. Antenna / LNA co-design could improve the overall performance

Stability: The LNA must interface with the outside world which includes the source impedance of the antenna. The user when wraps his/her palm around the antenna in a cell phone, say for example, the impedance changes which makes the LNA unstable. Therefore, it is essential for the LNA to remain stable for all source impedances at all frequencies. The instabilty will make the LNA oscillate. The parameter used to characterize the stability of circuits is the Stern or Rollet stability factor, as already introduced in section 3.4.3.

$$K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{21}||S_{12}|} \tag{4.1}$$

where $\Delta = S_{11}S_{21} - S_{12}S_{21}$. The condition when, K > 1 and $\Delta < 1$, the circuit do not oscillate with any combination of source and load impedances.

Linearity: The linearity is an important figure of merit particularly for some modulations schemes such as OFDM, which exhibits large envelope variations and has high ‘peak to average’ (PAR) ratio.

Bandwidth: The LNA ought to provide a relatively flat response for the frequency range of interest, preferably with less than 1 dB of gain variation. The LNA ω_{-3dB} bandwidth must

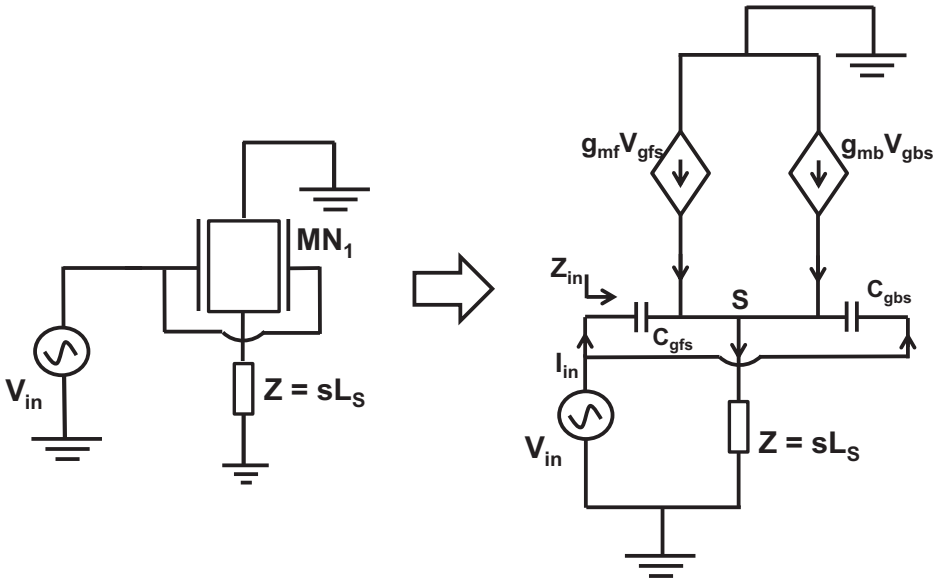


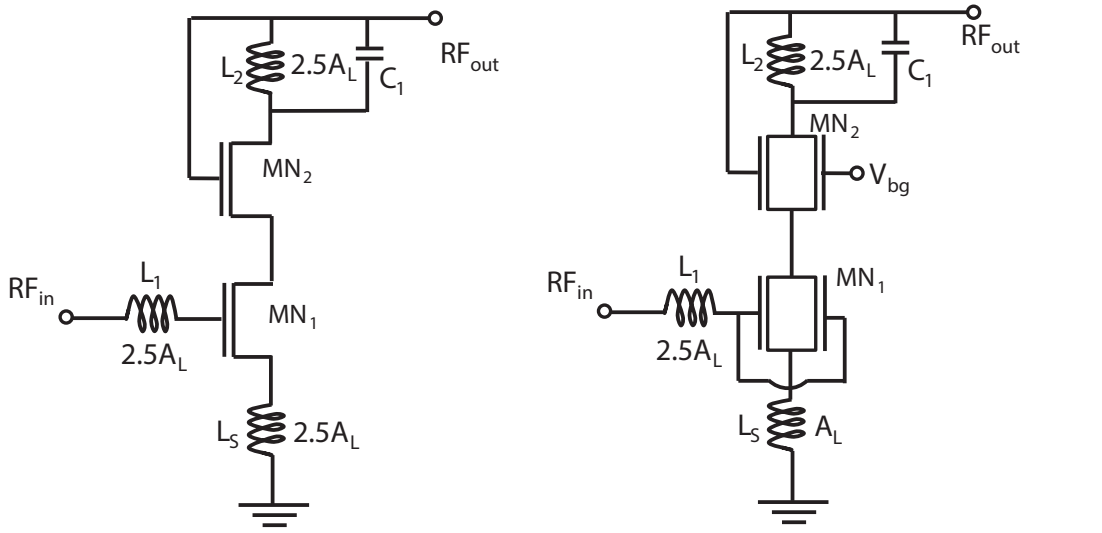
Figure 4.2: Small Signal Equivalent of the DG-MOSFET with parasitics.

therefore be substantially larger than the actual band so that the roll-off at the edges remains below 1 dB. The factor fractional bandwidth, defined as the ratio of the ω_{-3dB} bandwidth to the center frequency of the signal is a measure to quantify the bandwidth performance in a circuit.

4.2.2 Quantitative Analysis: CS Source Degeneration LNA

In this section, with the help of a quantitative small signal analysis, the area efficiency for the widely used common source inductive degeneration LNA in DG-MOSFET over conventional CMOS has been validated. The small signal model of a DG-MOSFET based CS cascode source degeneration LNA is depicted in Fig. 4.2. Solving Kirchoff's current law at node S we get,

$$\begin{aligned}(V_{in} - V_S)sC_{gfs} + (V_{in} - V_S)sC_{gbs} + \\ g_{mf}(V_{in} - V_S) + g_{mb}(V_{in} - V_S) \quad &= \quad \frac{V_S}{Z}\end{aligned} \tag{4.2}$$



Total Inductor Area: 2.5 A_L+2.5A_L+ 2.5A_L = 7.5A_L [Conventional CMOS]

Total Inductor Area: 2.5A_L+2.5A_L+ A_L = 6A_L [DG-MOSFET]

Figure 4.3: The area comparison of a simple CS cascode LNA in single gate MOSFET and DG MOSFET.

The DG-MOSFET considered here is a symmetric device and therefore we can safely assume $C_{gfs} = C_{gbs} = C_{gs}$ in this analysis. Also $g_{mf} = g_{mb} = g_m$, since the DG-MOSFET is considered to operate in common mode configuration (two gates are joined). Therefore, the current law can be modeled as,

$$2(V_{in} - V_S)sC_{gs} + 2g_m(V_{in} - V_S) = \frac{V_S}{Z} \tag{4.3}$$

After arrangement we have,

$$\frac{V_S}{V_{in}} = \frac{2sC_{gs} + 2g_m}{\frac{1}{Z} + 2sC_{gs} + 2g_m} \tag{4.4}$$

The input current, I_{in} can be written as,

$$I_{in} = sC_{gs}(V_{in} - V_S) \tag{4.5}$$

The input impedance ($Z_{in} = \frac{V_{in}}{I_{in}}$) is thus,

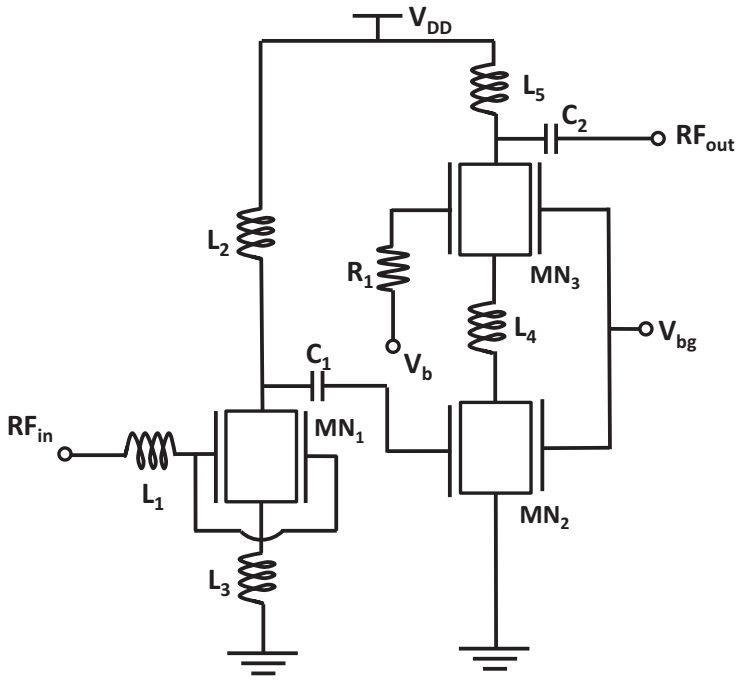


Figure 4.4: The DG MOSFET based LNA in common source cascode configuration. Transistors MN_1 operates in the symmetric mode while MN_2 and MN_3 operate in the independent mode with the back gates used for dynamic tuning[2], [14].

$$Z_{in} = \frac{1}{sC_{gs}(1 - \frac{V_S}{V_{in}})} \tag{4.6}$$

Inserting the value for $\frac{V_S}{V_{in}}$ from eqn. (4.4) in the above equation and after a few algebraic steps we obtain the following,

$$Z_{in} = \frac{1}{sC_{gs}} + 2Z + \frac{2Zg_m}{sC_{gs}} \tag{4.7}$$

Replacing Z by sL_S the input impedance is rewritten as,

$$Z_{in} = \frac{1}{sC_{gs}} + 2sL_S + \frac{2g_mL_S}{C_{gs}} \tag{4.8}$$

The last term of eqn. (4.8) is the resistive term and of our interest. The other two reactance terms resonate and cancel each other. The *factor '2'* in the term is absent in design with conventional CMOS [58]. Also it is known, the expression $\frac{g_m}{C_{gs}}$ is the transit frequency (ω_T)

of the device and therefore a constant for a particular device. The ω_T of DG-MOSFET is almost equal to its single gate counterpart for channel lengths of 75 nm and above while higher for channel lengths shorter than 75 nm owing to the good gate control on the channel and reduced SCE [78]. As can be observed in [78], for channel lengths lower than 50 nm, the ω_T of DG-MOSFET is almost a third to that of single gate CMOS. Therefore, the above statements confirm the inductance (L_S) in DG-MOSFET can be a sixth to that of single gate CMOS in a CS inductive degeneration topology to achieve the same 50 Ω input impedance for antenna matching (for an LNA). Approximating, $L_S \propto N^2$ (N = number of turns) aid with the fair assumption of proportionality of area and N, the area is reduced by nearly 2.5 times in DG-MOSFET based design.

Considering a basic Cascode CS Inductive degeneration LNA that consists of three inductors [58] (including the source degeneration inductor, L_S) and assuming the two inductors L_1 and L_2 are of equal dimensions for both the CMOS and DG-MOSFET based LNA designs (with channel lengths 45 nm and lower), the LNA area in DG-MOSFET design can be decreased by almost 20% when compared to single gate CMOS. This is illustrated in Fig. 4.3. The inductor being the major cause for area in the RF-Front end circuits, with several orders in magnitude higher than that of the active and other passive devices, the above mentioned figures verify the DG-MOSFET to be a viable alternative to RF CMOS for *area efficient* nanoscale LNA designs in the CS inductive degeneration topology.

4.2.3 LNA Design

Firstly a tunable DG-MOSFET LNA is designed for 60 GHz operation as shown in Fig. 4.4. The LNA consists of three DG-MOSFETs in an advanced 2 stage CS inductive degeneration cascode topology [2]. The common source transistor MN_1 operates in the symmetric mode while the two transistors MN_2 and MN_3 are configured for independent

mode operation. The common source transistor MN_2 and MN_3 are connected in cascode. The transistor MN_3 acts in common gate configuration. The width of MN_1 is taken to be 1 μm while the width for transistors MN_2 and MN_3 are kept higher at 2.4 μm for better input return loss and optimized gain performance. The supply, V_{DD} is kept constant at 1.2 V. MN_3 is biased at 2 V (V_b). The back gate of the transistors MN_2 and MN_3 are biased for gain switching [2].

The series peaking circuit consists of an inductive load, L_2, that allows for low voltage operation and resonates with the inter stage capacitance, C_1, enabling a higher operating frequency [58]. The inductor L_1 is set to resonate with the gate source capacitance of MN_1. The source degeneration circuit consisting of L_3 yields (in real part) wide band impedance matching to maximize the inter-stage power transfer. The inductor L_4 tunes out the middle pole of the cascode, thus compensating for the lower f_T.

Later the LNA is modified to make it work at 90 GHz as shown in Fig. 4.5. Here instead of three the circuit consists of four DG-MOSFETs, in the similar 2 stage cascade common source inductive degeneration cascode topology [90]. The inductors used in the earlier design have been replaced by microstrip transmission lines (MTLs). Here, the common source transistors MN_1 and MN_2 operate in the symmetric mode while the two transistors MN_3 and MN_4 are configured for independent mode operation. The common source transistor MN_3 and MN_4 are connected in cascode. The transistor MN_4 acts in common gate configuration. The width of MN_1 is taken to be 1 μm while the width for transistors MN_3 and MN_4 are kept higher at 2.4 μm for better input return loss and optimized gain performance. The supply, V_{DD} is kept constant at 1.2 V. MN_3 is biased at 1 V (V_b). Similar to the 60 GHz LNA, the back gate of the transistors MN_3 and MN_4 are biased for gain switching.

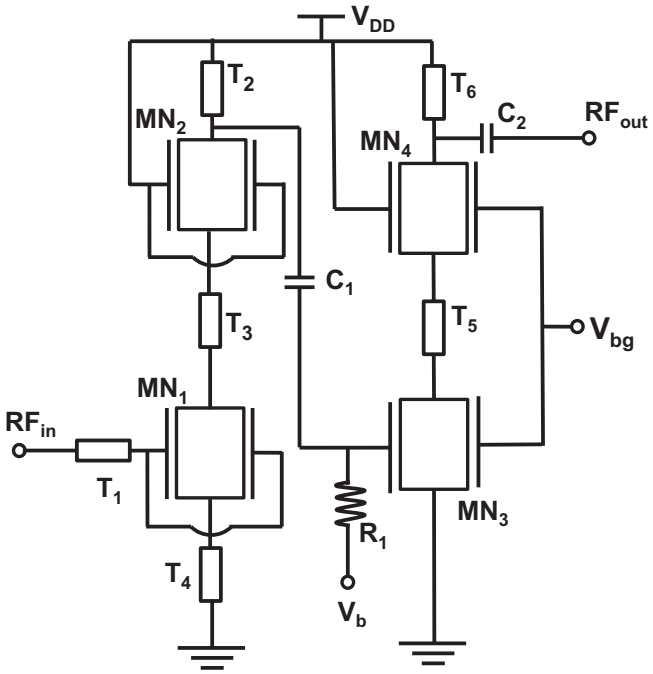


Figure 4.5: The DG MOSFET based LNA in common source cascode configuration. Transistors MN_1 and MN_2 operate in the symmetric mode while MN_3 and MN_4 operate in the independent mode with the back gates used for dynamic tuning. Unlike the 60 GHz LNA, in this circuit, the inductors are replaced by microstrip transmission lines.

4.2.4 LNA Gain Switching

The LNA needs to switch its gain to assimilate the dynamic range of the signal sensed by the receiver which may approach 100 dB. The dynamic range varies because a mobile device may receive a signal level as high as -10 dBm if it is close to a base station or as low as -110 dBm if it is inside a basement. While designed for the highest sensitivity, the receiver chain must still detect the signal correctly as the input level continues to increase. This requires that the gain of each stage be reduced so that the subsequent stages remain sufficiently *linear* with the high power level, as with increasing power level the linearity decreases [58]. LNA being the first stage must play the critical role in gain switching. While the gain of the receiver is reduced its noise figure rises. The gain must therefore

be lowered such that the degradation in sensitivity (that depends on NF) is less than the increase in the received signal level such that the SNR remains constant [58].

Therefore the gain switching in an LNA must deal with several issues [58]:

- It must negligibly affect the input matching. The remedy lies in the gain switching operation performed preferably in the cascode stage. The variation of voltage bias of a transistor alters the g_m of that transistor. The change in g_m in turn affects the input matching of the LNA, which should ideally be unaffected for maximum power transfer and minimized reflection losses between the antenna and the LNA.

- It must provide sufficiently small gain steps such that it does not introduce non-linearity.

- The gain switching operation must not degrade the speed of the LNA. Usually an additional transistor is required to perform the gain switching in single gate conventional CMOS which introduces additional delay.

The variable voltage bias introduced in the back gate of the two cascode transistors MN_2 and MN_3 implements the gain switching operation of the DG-MOSFET LNA as indicated earlier. The two cascode transistors are considered for the gain switching primarily because the cascode here is not a part of the input transistor at the first stage as can be seen from Figs. 4.4 & 4.5. The variation of the back gate voltage of a transistor alters the g_m of that transistor. The change in g_m in turn affects the input matching of the LNA, which should ideally be unaffected for maximum power transfer and minimized reflection losses between the antenna and the LNA. The cascode switching is also attractive because it reduces the current flowing through the load by a well defined ratio that aids in the achievement of small gain steps, which is yet another important issue that must be taken into consideration. As observed in the next section, the small step size considered in the biasing of the two transistors also assist in attaining the small gain steps. Therefore, the back gate bias should

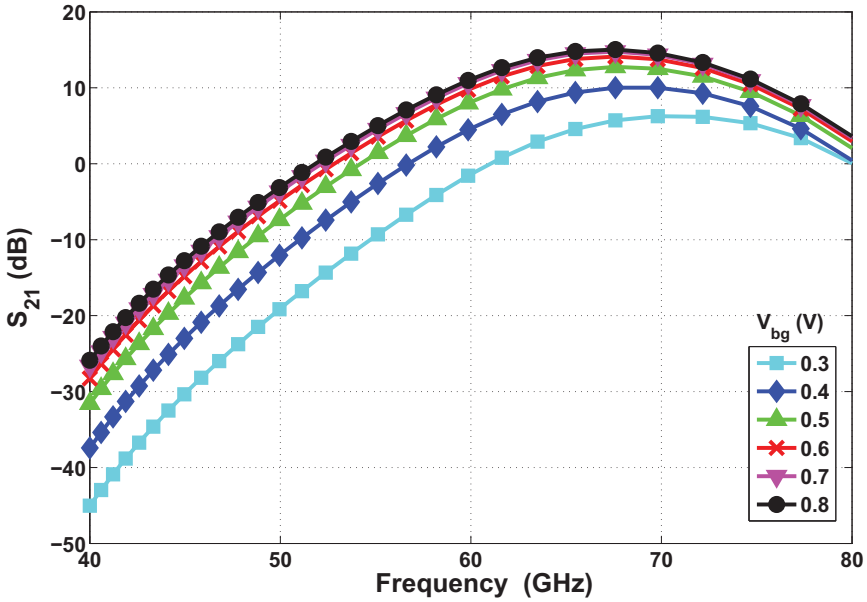


Figure 4.6: The gain (S_{21}) of the 60 GHz LNA varies with V_{bg}. This is measured for V_{bg} = 0.3 V to 0.8 V [14].

not be applied at the input transistor at the first stage (MN_1) which plays the crucial role of impedance matching in this CS inductive degeneration LNA. Another valid reason of not applying the bias to the input transistor is to avoid the thermal noise arising out of the transistor which can degrade the LNA noise figure when g_m is high [14], [2].

On the contrary, in LNA implemented with conventional CMOS, the gain switching is usually achieved with the addition of extra transistor(s) that alters the total transconductance of the transistor which in turn alters the gain. The added transistor that essentially acts as a switch can degrade the original speed of the LNA operation. Therefore, the DG-MOSFET based LNA gain switching is advantageous over its CMOS counterpart since it does not require any additional hardware and therefore results in no supplementary delay. Also the extra transistor in CMOS adds noise to the LNA deteriorating the noise figure [14], [2].

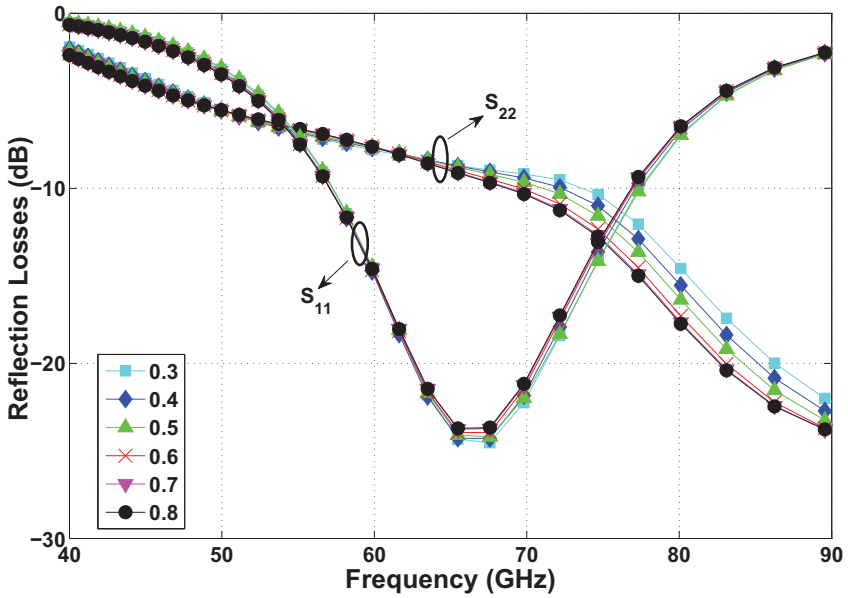


Figure 4.7: The input and output return losses of the 60 GHz LNA (S_{11} and S_{22}) for different V_{bg}.

4.2.5 Simulation Results

60 GHz LNA: The simulation of the 60 GHz LNA shows the 3-dB bandwidth to be 15 GHz, ranging from 60 to 75 GHz. The forward gain (S_{21}) achieves a peak value of 15 dB at 65 GHz for V_{bg} = 0.8 V (Fig. 4.6). Beyond this maximum operating voltage the gain gets saturated and is independent of V_{bg}. The peak gain reduces gradually as V_{bg} is reduced and drops to ~5 dB for V_{bg} = 0.3 V. The power dissipated (P_{dc}) by the LNA also varies with V_{bg}, reaching 18.1 mW at V_{bg} = 0.8 V. The reflection losses (S_{11} & S_{22}) obtained from the same simulations are shown in Fig. 4.7. The additional gate maintains nearly the same input matching while the gain is switched without any additional hardware/physical resistance. The LNA noise figure (NF) depends upon the back gate bias, dropping to a minimum at peak gain as expected. It ranges from 7.1 dB at V_{bg} = 0.8 V to 11.4 dB at V_{bg} = 0.3 V (Fig. 4.8). Clearly, the back gate tuning provides a convenient tool to optimize

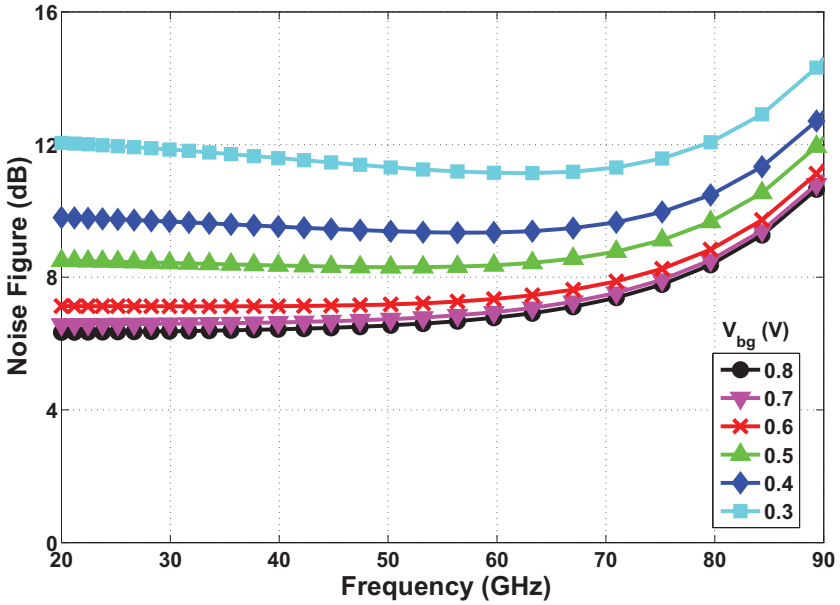


Figure 4.8: The noise figure dependence on V_{bg} of the LNA is evident. The NF changes by 4.3 dB in the tuning range of V_{bg} at 65 GHz [14].

specific device performance parameters, setting up unique trade-offs such as that between power and gain.

The proposed LNA is unconditionally stable in the operating frequency range, as can be seen from the simulated rollet stability factor, i.e. K > 1 (Fig. 4.9) (Also $\triangle < 1$ from easy computation) [58]. The circuit is also simulated for linearity performance using a two tone frequency analysis near 60 GHz and the observed maximum 3^{rd} order Input Intercept Point (IIP_3) is −5.2 dBm (for 0.3 V). The linearity does not vary considerably because of the source degeneration and the minimum is observed at −6 dBm (0.8 V). Table 4.1 lists the performance trade-offs for different operating V_{bg}s among gain, NF and P_{dc} at 65 GHz for our design [14]. [14].

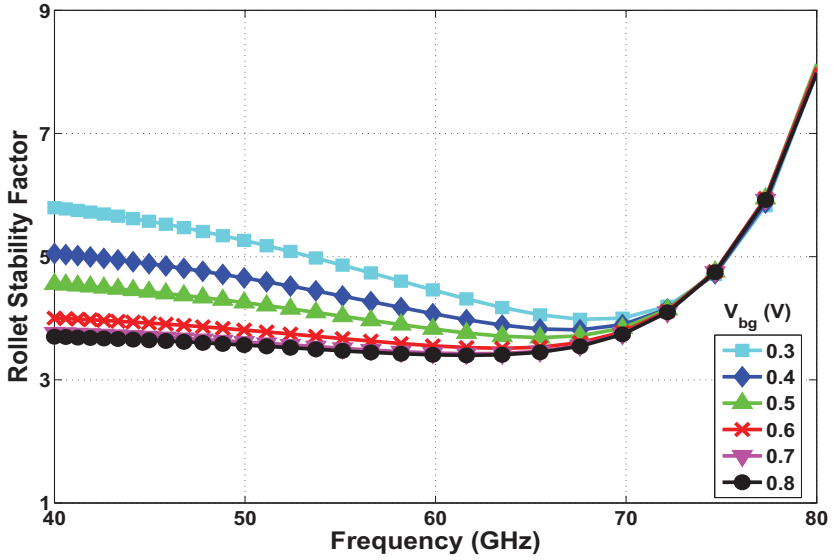


Figure 4.9: The value of K > 1, as one of the necessary condition, indicates the unconditional stability of the circuit.

Table 4.1: 60 GHz LNA Performance Trade-Offs for different V_{bg}s

V_{bg} (V)	Gain (dB)	NF (dB)	P_{dc} (mW)
0.3	5	11.4	15.2
0.4	8.8	10	16.4
0.5	12.4	8.8	17.2
0.6	14.6	7.6	17.7
0.7	15.0	7.2	18
0.8	15.0	7.1	18.1

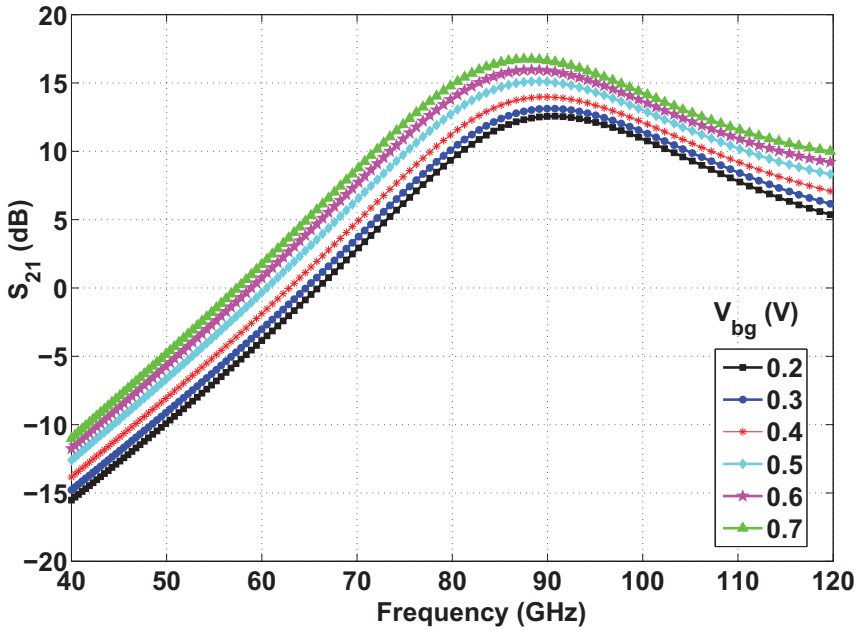


Figure 4.10: The gain (S_{21}) of the 90 GHz LNA varies with V_{bg}. This is measured for V_{bg} = 0.2 V to 0.7 V.

90 GHz LNA: The simulation of the 90 GHz LNA shows the 3-dB bandwidth to be 20 GHz, ranging from 80 to 100 GHz. The forward gain (S_{21}) achieves a peak value of 17 dB at 90 GHz for V_{bg} = 0.7 V (Fig. 4.10). Beyond this maximum operating voltage the gain gets saturated and is independent of V_{bg}. The peak gain reduces gradually as V_{bg} is reduced and drops to ~12.5 dB for V_{bg} = 0.2 V. The power dissipated (P_{dc}) by the LNA also varies with V_{bg}, reaching 12.1 mW at V_{bg} = 0.7 V. The reflection losses (S_{11} & S_{22}) obtained from the same simulations are shown in Fig. 4.11. The additional gate maintains nearly the same input matching while the gain is switched without any additional hardware/physical resistance. The LNA NF depends upon the back gate bias, dropping to a minimum at peak gain as expected. It ranges from 6.8 dB at V_{bg} = 0.7 V to 7.5 dB at V_{bg} = 0.2 V (Fig. 4.12). This LNA is also unconditionally stable in the operating frequency range, as can be seen from the simulated rollet stability factor, i.e. K > 1 (Fig. 4.13) (Also $\triangle$ < 1 from easy computation) [58]. Clearly, the back gate tuning provides a convenient tool to optimize

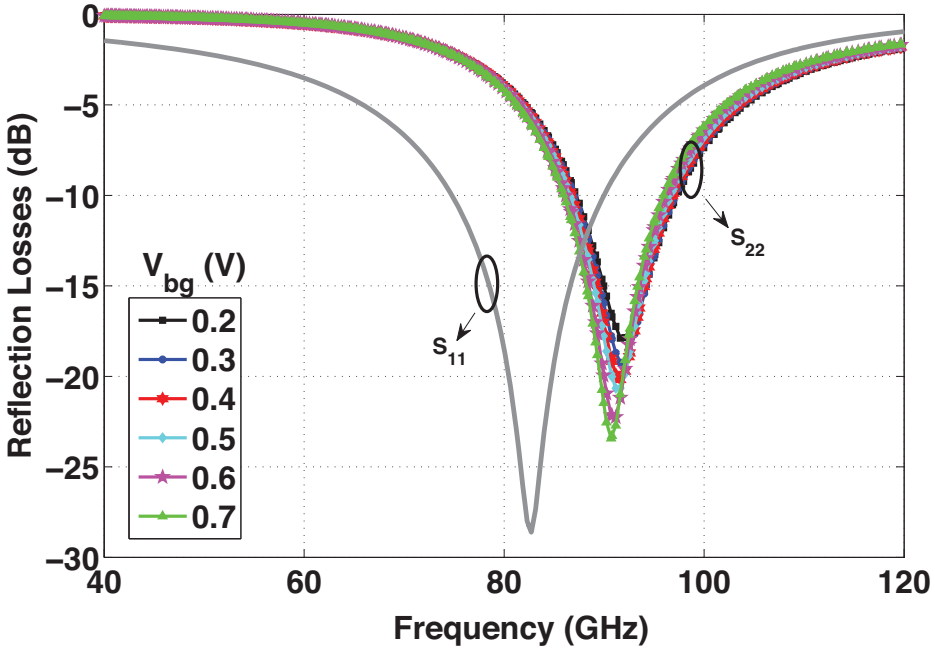


Figure 4.11: The input and output return losses of the 90 GHz LNA (S_{11} and S_{22}) for different V_{bg}.

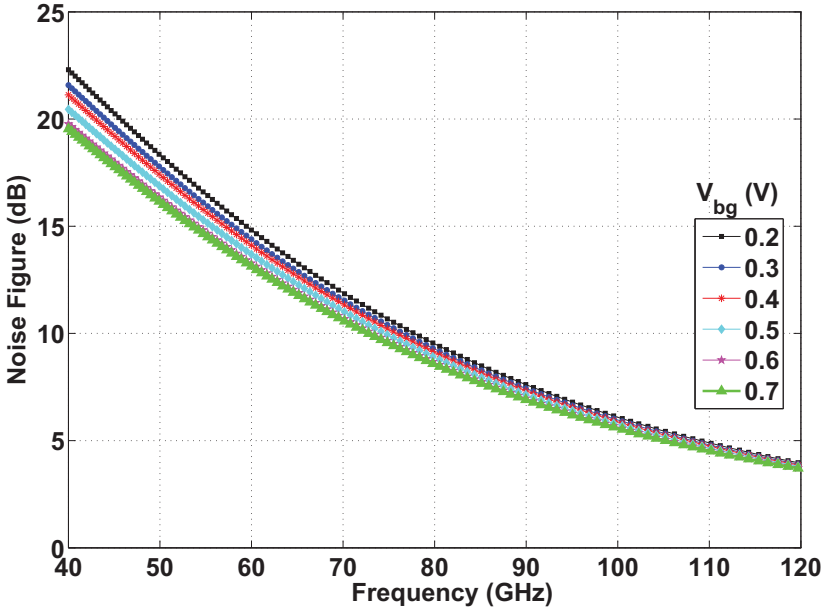


Figure 4.12: The noise figure dependence on V_{bg} of the LNA is evident. The NF changes by 1.5 dB in the tuning range of V_{bg} at 90 GHz.

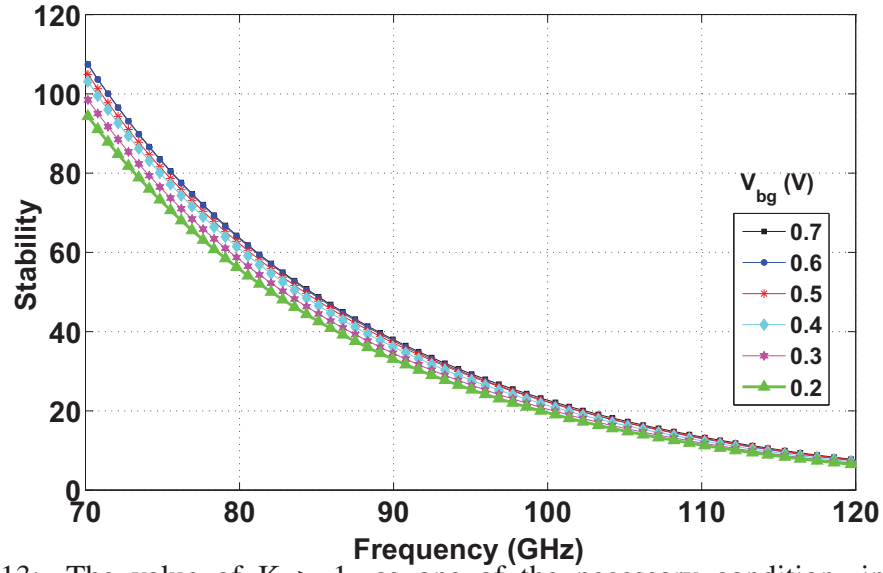


Figure 4.13: The value of K > 1, as one of the necessary condition, indicates the unconditional stability of the circuit.

Table 4.2: 90 GHz LNA Performance Trade-Offs for different V_{bg}s [2]

V_{bg} (V)	Gain (dB)	NF (dB)	P_{dc} (mW)
0.3	5	11.4	15.2
0.4	8.8	10	16.4
0.5	12.4	8.8	17.2
0.6	14.6	7.6	17.7
0.7	15	7.2	18
0.8	15	7.1	18.1

Table 4.3: Performance comparison of different mm-Wave LNAs [2]

Reference	Technology	Frequency / 3-dB BW (GHz)	Gain (dB)	NF (dB)	IIP_3 (dBm)	P_{dc} (mW)
[92]	35 nm HEMT	90/24	18	2.2	NA	NA
[93]	50 nm mHEMT	90/20	20	2.0	NA	NA
[94]	120 nm SiGe HBT	61.5/12	14.7	4.5	−8.5	10.8 @1.8 V
[95]	90 nm CMOS	64/8	15.5	6.5	NA	86 @1.26 V
[96]	65 nm CMOS	61/17	24 (Max.)	6.1 (Min.)	−5 (Max.)	30.4(Max) @1.2 V
This work (60 GHz) [2]	45 nm FinFET	60/15	15 (V_{bg} = 0.7 V)	7.1 (V_{bg} = 0.7 V)	−5.2 (Max.)	18.1(Max.) @1.2 V
This work (90 GHz)	32 nm FinFET	90/22	17 (V_{bg} = 0.7 V)	7 (V_{bg} = 0.7 V)	−5 (Max.)	12.1(Max.) @1.2 V

specific device performance parameters, setting up unique trade-offs such as that between power and gain. Table 4.2 lists the performance trade-offs for different operating V_{bg}s among gain, NF and P_{dc} at 90 GHz for our design. The figure of merits of this LNA are compared against some recent mm-wave LNA designs in different technologies as listed in Table 4.3.

4.3 Envelope Detector

The demodulation of a non-coherent modulated wave requires an envelope detector. The envelope detector is fundamentally a rectifier circuit that generates an envelope of the incoming high frequency carrier signal and retrieves the data from the carrier.

In Fig. 4.14a, we have illustrated a 45 nm DG-MOSFET envelope detector circuit [14], [17], in which the output is inverted to that of binary input (Refer Fig. 3.19). The output signal needs further to be passed through an inverter for the recovery of the original signal. Although requires additional hardware, this circuit has an advantage over the straightforward recovery as the former has a better output swing over the latter [97]. The simulation (Fig. 4.14b) illustrates the recovered binary input information as same as that is shown in Fig. 3.19. The high frequency noise present with logic 1 data at the output can be easily filtered out [14], [17].

4.4 Summary

The first section of the chapter put forward DG-MOSFET as a viable and better alternative to conventional CMOS in high-efficiency nano scale mm-wave LNA design primarily intended for high speed compact indoor wireless applications. The better area efficiency of CS inductive degeneration DG-MOSFET LNA with use of lower dimension inductance than its RF CMOS counterpart, that is verified quantitatively, along with the dynamic gain switching available in the proposed LNA implementation which cannot be

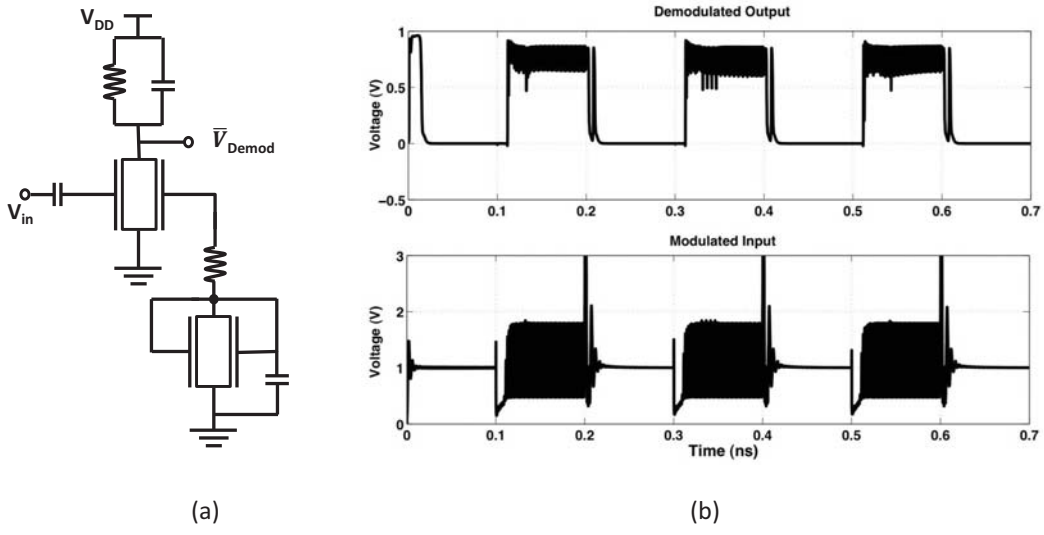


Figure 4.14: a) Envelope Detector Circuit with only two DG MOSFETs. b) The modulated input consisting of the both the carrier and data and the recovered demodulated output consisting only of data sans the carrier [17].

efficiently achieved in conventional CMOS without additional area and delay overhead, aid to this prospect. Later, the simulation results indicate competitive figure of merits for the LNA.

In the last section, the envelope detector designed in DG-MOSFET technology successfully demodulates the OOK Modulated signal.

5 DG-MOSFET Circuits for Coherent Detection

5.1 Introduction

The earlier chapter deals with incoherent detection with an envelope detector for OOK modulation. The requirement of a down conversion mixer is not a necessity because of demodulation by the analog envelope detection circuit which can function and robust even at the range of radio/mm-wave frequency. However in coherent detection, we need to down-convert the incoming signal for effective sampling for demodulation and detection by mixed signal circuits such as phase locked loops. In this chapter, the two essential circuit blocks in the front-end for a coherent detection receiver, RF Mixer and Charge Pump Phase Frequency Detector are discussed in the DG-MOSFET technology.

The RF Mixer is investigated at a lower frequency of 2.4 GHz because of its relevance to many wireless standards such as Bluetooth and IEEE 802.11b/g/n which uses coherent modulation schemes.

It must be pointed out that, no attempt to build and simulate the entire Phase Locked Loop (PLL) circuit has been carried out in this research, but indicated the essential active circuit blocks (Oscillator & Charge Pump Phase Frequency Detector) to be used towards this goal. The design and simulation of an entire PLL at the transistor level via transient simulations is not a trivial task that may require supercomputer resources. For this reason it is often done using system analysis via behavioral model, which is outside the scope of this work and constitutes a dissertation on its own.

5.2 DG-MOSFET RF Mixer

In this section, at first the DG-MOSFET mixer theoretical operation is verified qualitatively. After which the optimum biasing points and structural design parameters for a novel nano-scale DG-MOSFET radio frequency (RF) mixer is investigated at 2.4 GHz [18]. This is a detailed research and an extension of an earlier work at low frequency

[98]. The objective is to analyze and identify the correlation of the conversion gain of the mixer circuit with the signal amplitude of the local oscillator (LO) as well as different device parameters, such as the gate length (L_{gate}), doping concentration (N_A) and body thickness (t_{Si}), thus minimizing signal loss and power consumption and increasing stability. The most important figure of merit is found to be the LO DC bias that determines the level of non-linearity in the transconductance response. Furthermore, we observe that in properly designed DG-MOSFETs ($L_{gate} \geq 3t_{Si}$), L_{gate} and N_A have limited impact on the conversion gain of the mixer, while t_{Si} has a more significant role to play. Although the mixing performance of DG-MOSFETs is ultimately limited by the SCEs perpetrated by any given structural constraint, an optimum body thickness t_{Si} exists in each case to maximize the conversion gain. How 2D and quantum-corrected simulations can identify the optimum body thickness and optimum bias conditions in such compact nano-scale mixers, are illustrated.

The RF Mixer is not investigated at the 60-100 GHz range in commensuration with the non coherent OOK transceiver discussed in the earlier two chapters. The analysis is undertaken at a lower frequency of 2.4 GHz because the UFDG Model which is used for the analysis is less reliable at the 60-100 GHz frequency range due to lack of detailed parasitics. The 2.4 GHz frequency band is particularly chosen owing to the fact that this frequency band is used in many wireless standards which mostly use coherent modulation schemes such as Bluetooth, Zigbee and IEEE 802.11b/g/n.

5.2.1 RF Mixer Theory

The RF mixer is a non-linear electrical circuit that performs frequency translation by multiplying two waveforms and their harmonics. The new frequencies (sum & difference) are called the intermediate frequencies (IF). The sum frequency has its application on the up conversion whereas the difference frequency is used in the down conversion of an

input signal. In this section, we have concentrated on the down conversion property and optimized our design accordingly. The conversion gain (CG) of the mixer, which is the ratio of the magnitude of the Intermediate signal and the RF signal, determines the mixing performance of the circuit [59]. The mixers have three different ports. In the receive path, the downconversion mixer senses the RF signal at the RF port and the local oscillator waveform at the LO port. The IF at the output is called the IF port in a heterodyne receiver or the baseband port (IF = 0) in a direct-conversion receiver. In the transmit path, the upconversion mixer input, sensing the IF or the baseband signal is called the IF port or baseband port, and the output port is called the RF port. The input driven by the local oscillator is called the LO port.

Mathematically, if the frequencies of the RF and LO signals are represented by f_{RF} and f_{LO} with amplitudes V_{RF} & V_{LO} respectively, the two signals are given as:

$$v_{RF} = V_{RF} sin(2\pi f_{RF} t) \tag{5.1}$$

$$v_{LO} = V_{LO} sin(2\pi f_{LO} t) \tag{5.2}$$

The mixing operation is the multiplication of the two signals and thus the output intermediate signal is given by:

$$v_{IF} = \frac{V_{RF} V_{LO}}{2} [cos2\pi t(f_{RF} - f_{LO}) - cos2\pi t(f_{RF} + f_{LO})] \tag{5.3}$$

The first term (f_{RF} - f_{LO}) is the down converted intermediate frequency is used in the downconversion of an input RF signal and is the primary focus of the current research.

The downconversion mixer is used in the receiver architecture and its performance parameters are described as follows:

Gain: The downconversion mixers must provide sufficient gain to adequately suppress the noise contributed by subsequent stages. The voltage conversion gain is the most significant figure of merit of a down conversion mixer is given by the ratio of the rms

voltage of the IF signal to the rms voltage of the RF signal. In traditional RF and microwave design, mixers are characterized by a power conversion gain defined as the output signal power divided by the input signal power. However, the voltage quantities are preferable because the input impedances are mostly imaginary, making the use of power quantities difficult and unnecessary.

Noise & Linearity: In a receiver, the input noise of the mixer following the LNA is divided by the LNA gain when referred to the receiver input. Similarly, the P_{1dB} of the mixer is scaled down by the LNA gain. The design of downconversion mixers therefore entails a compromise between noise figure and the P_{1dB}. In direct-conversion receivers the IP_2 of the LNA/mixer cascade must be maximized.

Isolation: Isolation is the amount of local oscillator power that leaks into either the IF or the RF ports. There are multiple types of isolation which are LO to RF, LO to IF and RF to IF isolation [99]. LO component in the RF input can pass back through the mixer and be modulated by the LO signal, and a DC and $2f_{IF}$ components are created at the IF output. This has no consequence for a heterodyne system, but a concern for homodyne systems. LO to RF isolation is one of the biggest challenge [99] in Mixer design and advanced structures those uses differential methods are proposed.

5.2.2 RF Mixer Operation

The DG-MOSFET mixer (Fig. 5.1a) occupies a special status among analog applications given the compact and high performance nature of an active mixer using only one transistor.

The DG-MOSFET Mixer's multiplicative/non-linear property has been analyzed here from Fig. 5.1b. The RF signal which is applied at the front gate is represented by small signal model. This is justified because the power level of RF signal is very small on reception at the antenna and remains small even amplified by the LNA [18]. Therefore,

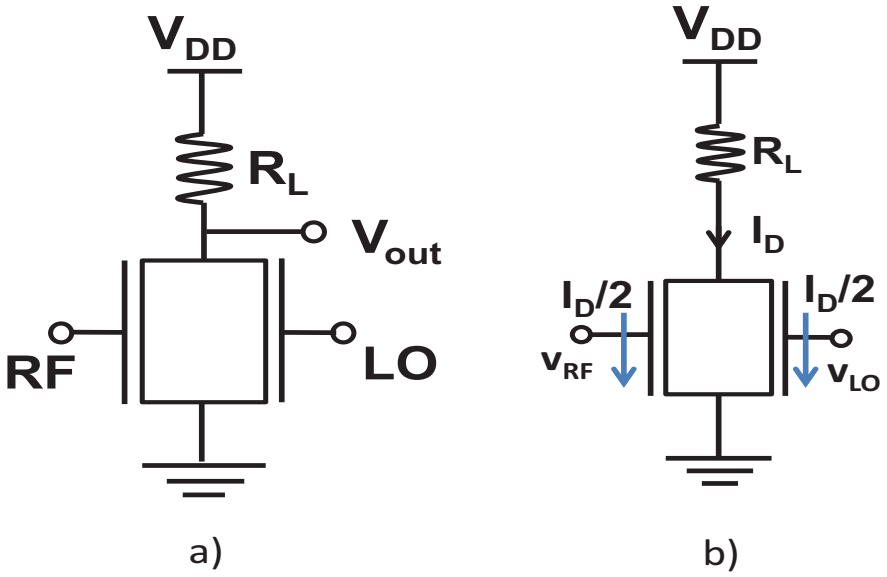


Figure 5.1: DG-MOSFET a) RF Mixer Circuit b) Analysis for Non-Linearity

the output voltage, V_{out} is given as:

$$V_{out} = g_m v_{RF} R_L \tag{5.4}$$

where g_m is the transconductance of the device at the front gate. The I-V characteristics of DG-MOSFET at saturation is modeled as [45]

$$I_D = K[(V_{gs} - V_T)^2 - K' e^{\frac{V_{gs}-V_0-V_{ds}}{kT}}] \tag{5.5}$$

where K & K' are process and device constants and V_0 is a second order term of the threshold voltage, V_T [45]. Here the drain current at the front gate (I_{Df}) is modeled by ignoring the exponential term assuming a large V_{ds} at saturation, where the numerator at the exponent goes negative.

$$I_{Df} = K(V_{gs} - V_T)^2 \tag{5.6}$$

Assuming equal current distribution at the two gates ($I_{Df} = \frac{I_D}{2}$) we have,

$$\frac{I_D}{2} = K(V_{gs} - V_T)^2 \tag{5.7}$$

The transconductance at the front gate is,

$$g_m = \frac{1}{2}\frac{\partial I_D}{\partial V_{gs}} \tag{5.8}$$

From eqns. (5.7) and (5.8) we can write,

$$g_m = 2K(V_{gs} - V_T) \tag{5.9}$$

Now from eqns. (5.7) and (5.9)

$$g_m = \sqrt{(2KI_D)} \tag{5.10}$$

A large signal model is assumed for the back gate as the LO signal is locally generated and usually has high amplitude levels [18]. Therefore the back gate current (I_{Db}) is,

$$I_{Db} = K(v_{LO} - V_T)^2 \tag{5.11}$$

Also $I_{Db} = I_D/2$. Therefore,

$$I_D/2 = K(v_{LO} - V_T)^2 \tag{5.12}$$

implies,

$$I_D = 2K(v_{LO} - V_T)^2 \tag{5.13}$$

Therefore from eqns. (5.4), (5.10) & (5.13),

$$V_{out} = K''(v_{LO} - V_T)v_{RF} \tag{5.14}$$

here K'' is a constant which include the process and device parameters and the resistor R_L [18]. The eqn. (5.14) gives an analysis of the non-linear RF Mixer operation of the DG-MOSFET device. The process dependent parameter V_T can be eliminated if we consider a balanced/differential mixer mode. However, typically the balanced mode is avoided because in a receiver design the mixer follows the LNA which is generally single ended as it follows a single ended antenna. A balun which consumes a large area is thus required to construct before the mixer for the balanced mode use.

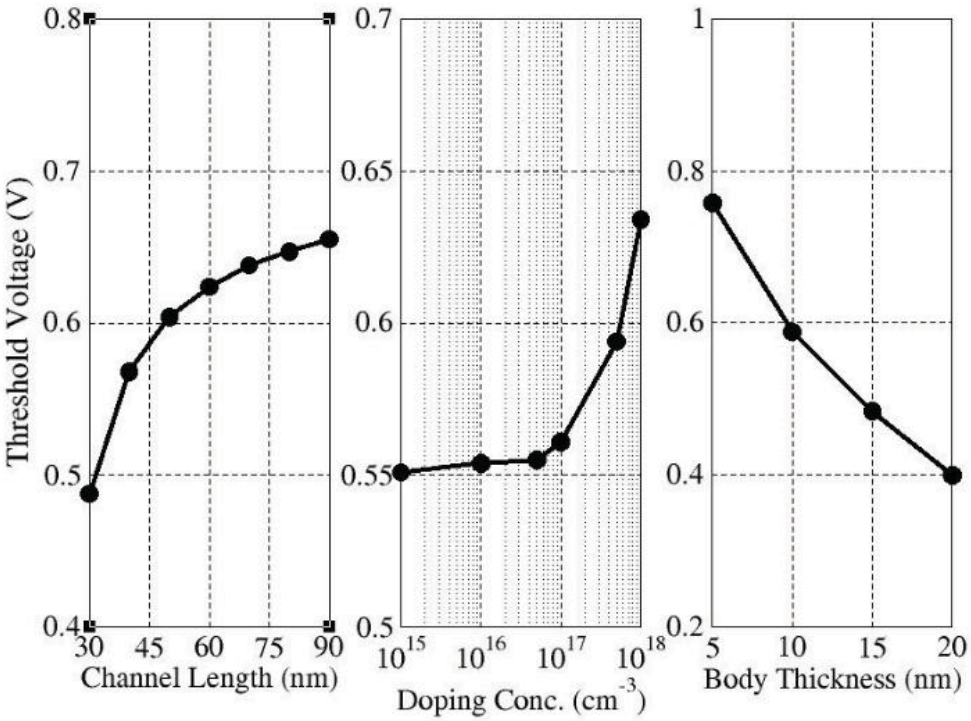


Figure 5.2: The variation of V_T for the different device parameters L_{gate}, N_A and t_{Si} [18].

5.2.3 Operating Point Analysis

In performing the operating point analysis, we first explore the dependence of threshold voltage (V_T) (Fig. 5.2) on each of the device parameters for a fair comparison of mixing performance obtained from varying the important structural parameters. This way we can ensure an appropriate gate overdrive can be set for varying structural parameters. Assuming a 1D Analytical Model for long-channel MOSFETs, the V_T for an Independent DG-MOSFET can be modeled as [100]

$$\begin{aligned} V_T &= n_i u_t ln\Big[\frac{2n_i C_{oxi} u_t}{qN_A t_{Si}}\Big] - (n_i - 1)V_{gj} \\ &\quad -n_i u_t ln\left[\frac{tanh\Big[\frac{C_{eq}(V_{gj}-V_{gi})}{2C_{Si}u_t}\Big]}{\frac{C_{eq}(V_{gj}-V_{gi})}{2C_{Si}u_t}}\right] \end{aligned} \tag{5.15}$$

In this equation, n_i is the capacitive coupling factor for either front or the back gate, and is given by

$$n_i = 1 + \frac{C_{Si}C_{oxj}}{C_{oxi}(C_{Si} + C_{oxj})} \tag{5.16}$$

u_t is the thermal voltage and is a function of temperature. V_{gj} and V_{gi} are the gate voltages to either the front or the back gate, the indices i & j refer to either the front or back gates but never the same. C_{oxi}, C_{Si} and C_{eq} are the oxide, body and equivalent capacitance respectively. The C_{eq} is defined as

$$C_{eq} = \frac{1}{\frac{1}{C_{oxi}} + \frac{1}{C_{Si}} + \frac{1}{C_{oxj}}} \tag{5.17}$$

Extending the definition of 1D Poisson Solver to a 2D Analytical Model with quantum corrections and considering the SCEs, equation 5.15 modifies to

$$V_{T2D} = V_T + K(L_{gate}, \phi) \tag{5.18}$$

The term K is the correction term and is a strong function of the gate length and other device parameters, ϕ as described in [100]. The equations 5.15 and 5.18 show the V_T dependence on the structural parameters considered here and the importance for their determination for ensuring an appropriate gate overdrive.

As stated earlier, the DG-MOSFET RF Mixer circuit explored in this section consists of only one transistor [14], [18]. For this analysis, the source voltage (V_{DD}) is kept at the typical value of 1 V and the circuit load, R_L, is kept at 6 kΩ. The sinusoidal RF signal is considered at the frequency f_{RF} of 2.4 GHz while the sinusoidal local oscillator signal is chosen at a frequency f_{LO} of 2.5 GHz so to down convert the incoming frequency to 100 MHz to work effectively with the demodulation of the input signal at the baseband frequency. In this DG MOSFET based architecture, the RF input signal ((v_{RF} = (v_{rf} + V_{RF}) sin($2\pi f_{RF}$t)) is applied at one gate while the local oscillator (LO) signal (v_{LO} = (v_{lo} + V_{LO}) sin($2\pi f_{LO}$t) is applied at the another gate of the transistor. Here, v_{rf} and v_{lo} are the

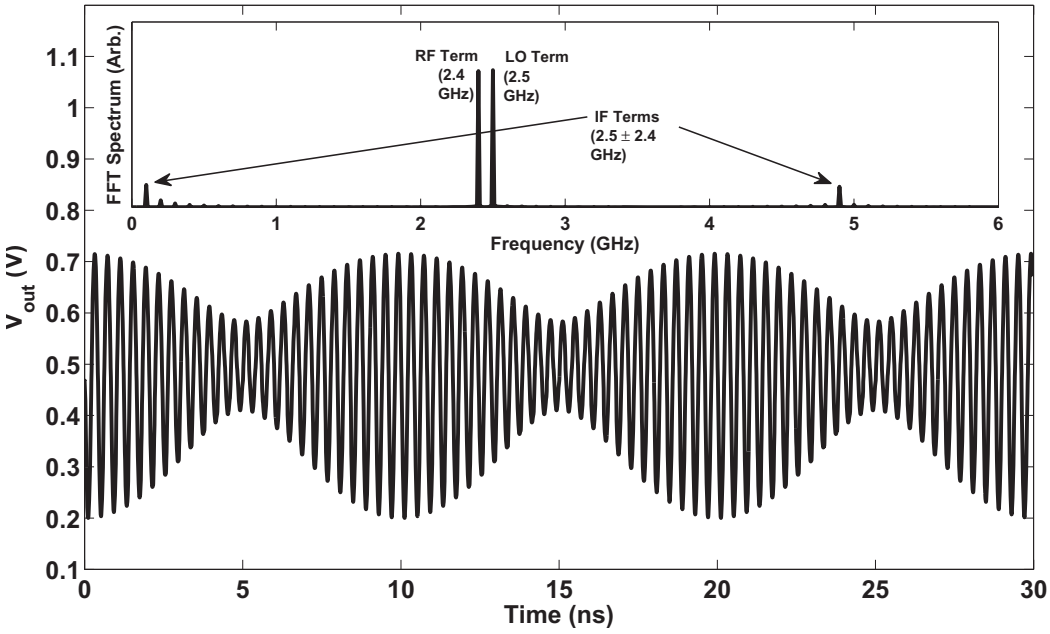


Figure 5.3: The FFT (inset) of the voltage at the mixer output (main panel) shows both the sum & difference terms as well as additional higher order harmonics [18].

AC components of RF and LO signal respectively, while V_{RF} and V_{LO} are the respective DC bias components. The output signal (V_{out} = A_v[cos2πt(f_{RF} - f_{LO}) - cos2πt(f_{RF} + f_{LO})]) consisting of the two intermediate frequencies is observed at the drain of the DG MOSFET and A_v is (v_{rf} + V_{RF})(v_{lo} + V_{LO})/2. The conversion gain (CG) by definition, then becomes (v_{lo} + V_{LO})/2. However, this theoretical linear proportionality of CG on LO amplitude is not valid everywhere and there is a strong dependence on the device geometries and threshold as evident from this analysis, and this necessitates the requirement for bias optimization with quantum corrected simulations. It can be noted, although the LO-RF isolation is not nullified using independent inputs, however is reduced significantly compared to single gate CMOS non-balanced mixers. The LO-IF feedthrough is however present, and can be ignored as the IF frequency lies in a different band of interest and the LO effect can be filtered using a low pass filter [14], [18]. After the FFT analysis (Inset: Fig. 5.3) of the output at a very high temporal resolution, we observe significant spectral lines at the two

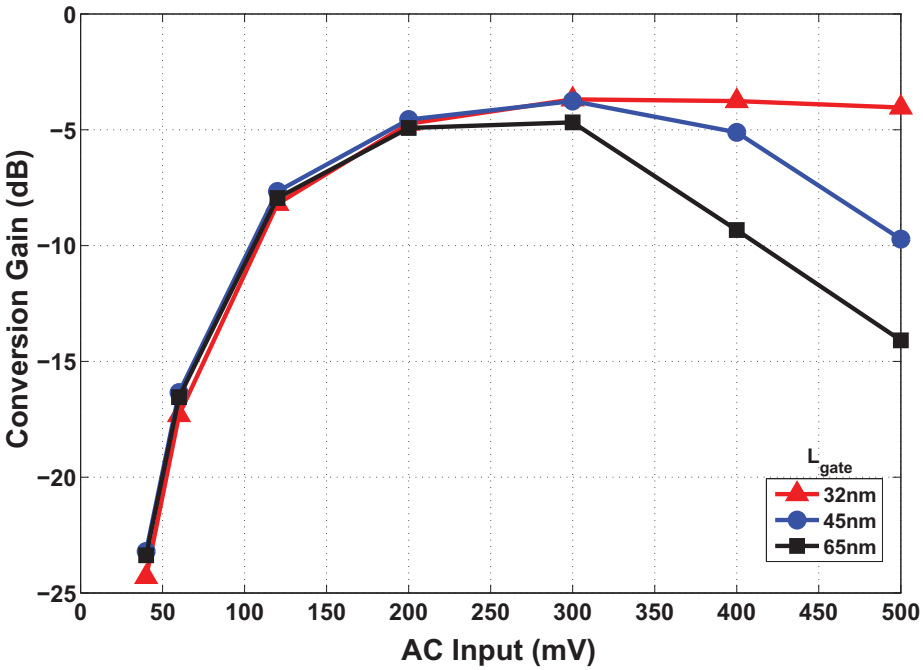


Figure 5.4: Variation of conversion gain with v_{lo} for different L_{gates} [18].

intermediate frequencies of 100 MHz ($f_{RF} - f_{LO}$) and 4.9 GHz ($f_{RF} + f_{LO}$) indicating the appropriate double gate mixing performance and non-linearity [18].

Alternatively, in the time domain, one can also observe the envelope that seemingly corresponds to the down converted frequency of 100 MHz (Fig. 5.3). The presence of other harmonics in the FFT spectra indicates higher-order non-linearities arising out of the undesired higher order intermodulation products and can be easily filtered out to work with the desired down converted frequency. For the analysis purposes and simplification of the observed spectra, the LO signal used in our study is a pure sine-wave with a DC offset providing the operating point for the device, while the v_{rf} at the another gate is held constant without a DC offset ($V_{RF} = 0$) at 40 mV.

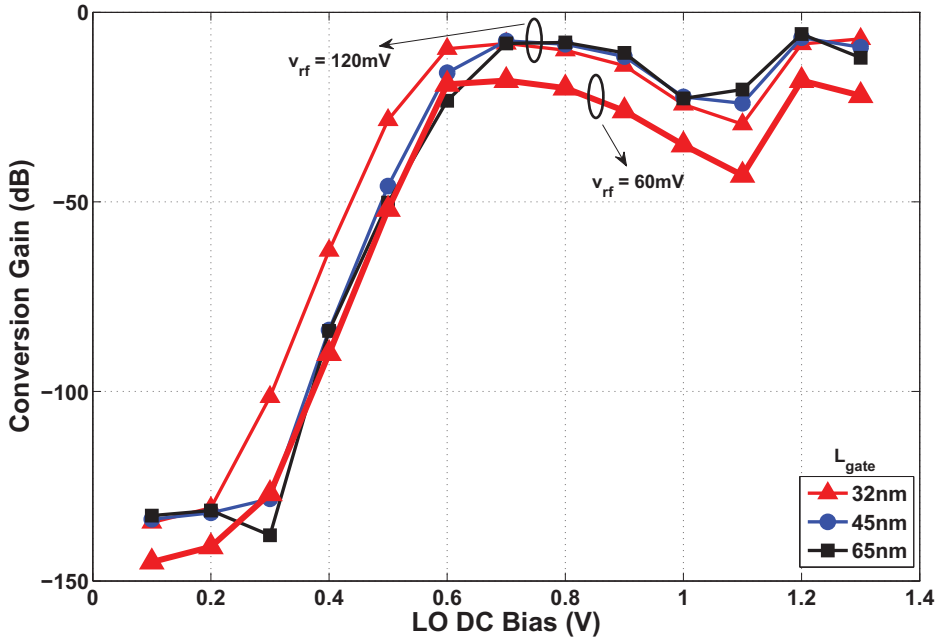


Figure 5.5: Variation of CG with V_{LO} at different L_{gate}s [18].

Our study indicates that the conversion gain of the mixer rapidly changes with v_{lo} rising to 200 mV (Fig. 5.4), beyond which the increase is limited and stabilizes. After 300 mV there is a dip in the CG with an increasing slope from 32 nm to 65 nm mainly arising out of distortion. For this analysis, it is to be noted that V_{LO} is held at its optimized value for highest conversion gain, obtained from Fig. 5.5. For instance, for 32 nm the V_{LO} is held constant at 0.7 V. Hence, for all L_{gate} values, the operating point of the mixer is chosen to be set around 120 mV for optimum power efficiency and conversion gain. Similar results were also obtained for different $N_A s$ and $t_{Si} s$ from similar analyses [14], [18].

The conversion gain is particularly sensitive to the V_{LO} (Fig. 5.5) with a 'Camel'-shape dependence, where the middle 'dip' could be −20 dB. Seemingly there are two bias conditions that provide similar performance in conversion gain of the mixer (Fig. 5.5). For instance, these two bias points are observed at 0.7 V and 1.2 V for L_{gate} = 32 nm and v_{lo} = 120 mV. Moreover, this 'Camel'-shape is a very weak function of v_{lo} and L_{gate}.

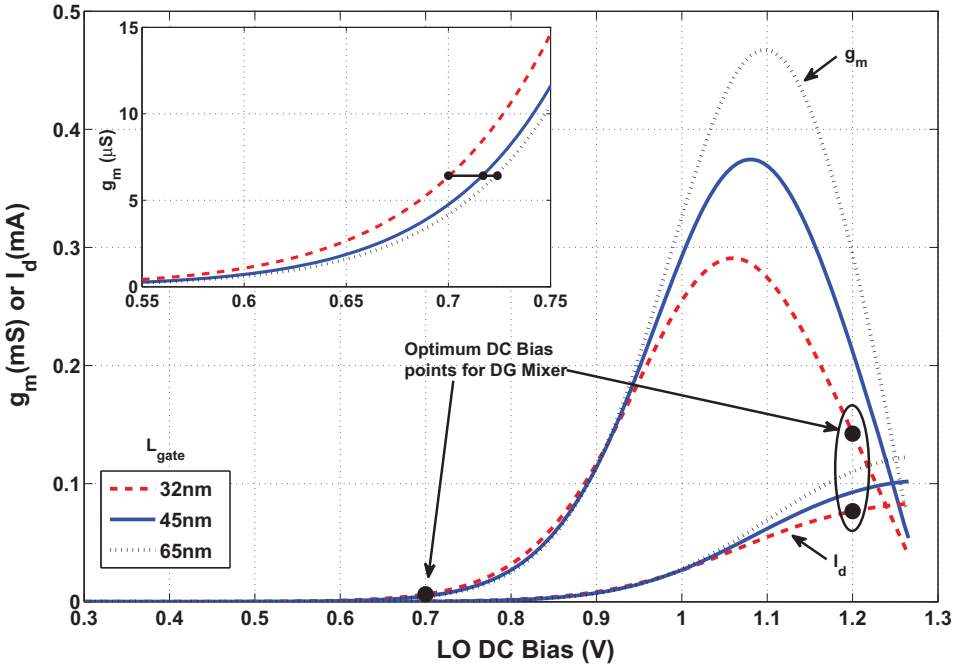


Figure 5.6: Transconductance (g_m) & drain current (I_d) over DC bias for different L_{gate}s. Out of two optimum bias points, the lower one at 0.7 V (32nm) is chosen for better stability and power efficiency [18].

Data recorded with v_{lo} of 120 mV with 60 mV shift mainly vertically with a large lateral similarity in terms of DC bias dependence. Likewise, the peak position shifts roughly 0.1 V only, as the gate length is varied from 32 nm to 65 nm [14], [18].

It is interesting to note that these optimum DC-bias ranges correspond to the least 'linear' sections of the device operation, as can be seen from the transfer characteristics and transconductance (g_m & I_d) curves in Fig. 5.6. The current changes non linearly around the optimum bias position and the g_m peak corresponds to the central dip in Fig. 5.5. Clearly, the lower bias point (~ 0.7 V in Fig. 5.5) is preferred because of power efficiency and better stability indicated by the broader plateau. Similar analyses conducted for different N_A and t_{Si} of the DG MOSFET mixer yield in similar results to our study of L_{gate}. A double-peaked LO-DC behavior persists in all cases as verified from Figs. 5.7 & 5.9 for N_A and

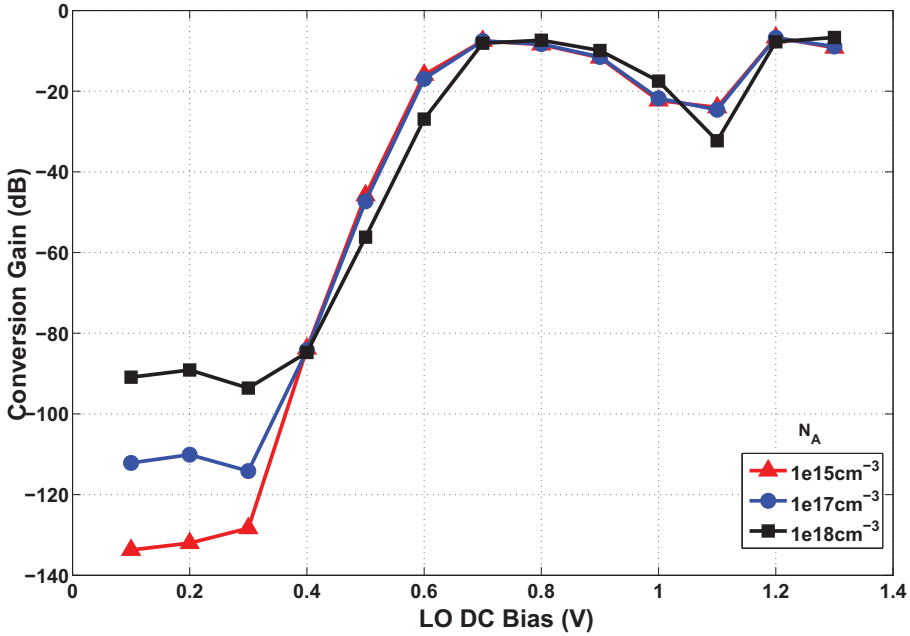


Figure 5.7: Variation of CG with V_{LO} at different N_As. The V_{LO} has a weak correlation with different N_As [18].

t_{Si} respectively. The central dip can be as low as −90 dB which is attained for 10 nm t_{Si} (Fig. 5.9). It can be observed V_{LO} to be very weakly correlated with N_A at the optimal bias, while we envisage the strong function of V_{LO} for t_{Si}. This asserts the body thickness as the most important structural parameter to be considered for optimization. Similar to our study of L_{gate}, the g_m curves for N_A and t_{Si} (Figs. 5.8 & 5.10) notify as well that the optimum DC-bias ranges correspond to the least 'linear' sections of the device operation [14], [18].

Similar to conventional CMOS, for DG-MOSFETs the g_m attains a peak primarily due to the mobility dependence on gate-field. The mobility due to surface roughness scattering (μ_{sr}) and phonon scattering (μ_{ph}) reduces by E_{eff}^{-2} and $E_{eff}^{-\frac{1}{3}}$ respectively, where E_{eff} is the normal field averaged over the inversion layer. This leads to the g_m peak [101]. The fact, CG $\propto -g_m$ explains the phenomenon of the middle dip in the CG characteristic when the g_m attains maximum. The dependence of the gain upon the signal level further leads to nonlinearity in mixer characteristics [102]. The current changes nonlinearly around the

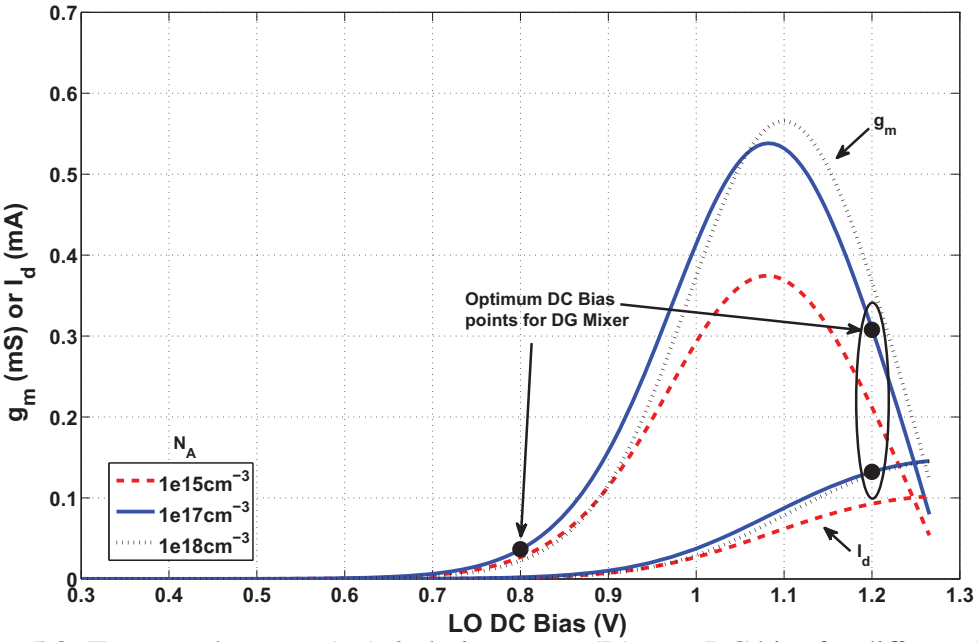


Figure 5.8: Transconductance (g_m) & drain current (I_d) over DC bias for different N_As. Out of two optimum bias points, the lower one at 0.8 V (1e17cm^{-3}) is chosen for better stability and power efficiency [18].

optimum bias ranges and the g_m peaks for these two parameters correspond to the central dip as well. Summarizing results from these simulations, Table 1 lists the optimum (lower) bias points for the three different structural parameters studied [14], [18].

5.2.4 Structural Parameters

Next studied is the dependence of conversion gains recorded at the various LO AC amplitudes and at optimum DC (lower peak) bias conditions as a function of significant structural parameters of the DG MOSFET. The results are summarized in Figs. 5.11 & 5.12, which show the dependence of conversion gain with L_{gate}, N_A & t_{Si}, respectively [14], [18].

Clearly, the L_{gate} has almost no impact on the conversion gain at higher values while at lower value the impact becomes more pronounced. For the N_A, the conversion gain almost remains constant at low doping levels whereas it slightly increases at very high

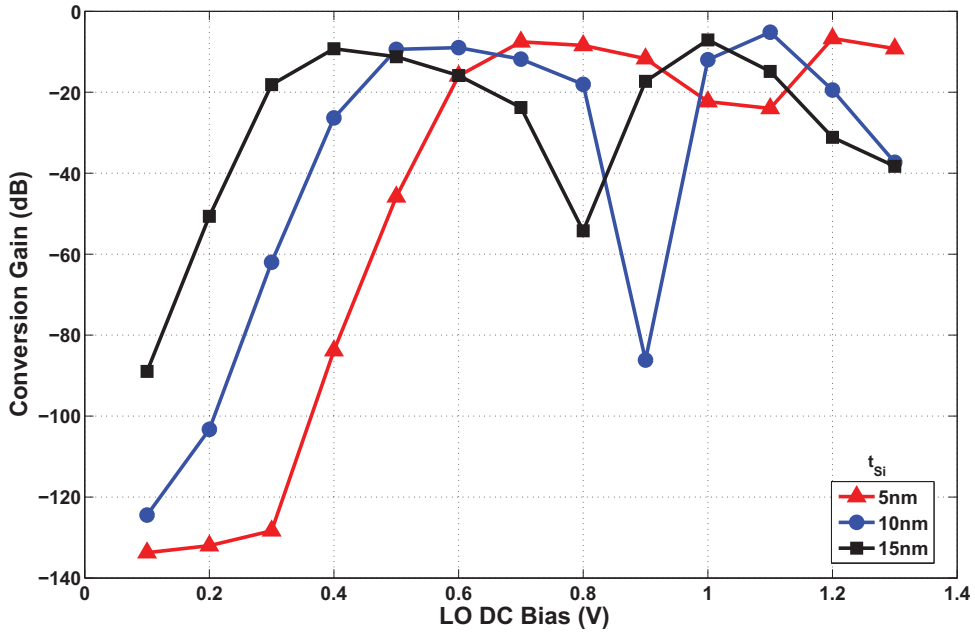


Figure 5.9: Variation of CG with V_{LO} at different t_{Si}s. The strong correlation of V_{LO} with different t_{Si}s can be noted. There is a shift of 0.4 V in the V_{LO} for the optimum CG in moving from 15 nm to 5 nm [18].

Table 5.1: Optimum V_{LO} for the different structural parameters at f_{RF} = 2.4 GHz

L_{gate}(nm) [N_A=10^{15}cm^{-3}, t_{Si}=5nm]	DC Bias (V)	N_A(cm^{-3}) [L_{gate}=45nm, t_{Si}=5nm]	DC Bias (V)	t_{Si}(nm) [L_{gate}=45nm, N_A=10^{15}cm^{-3}]	DC Bias (V)
32	0.70	10^{15}	0.75	5	0.75
45	0.75	10^{17}	0.77	10	0.60
65	0.80	10^{18}	0.80	15	0.45

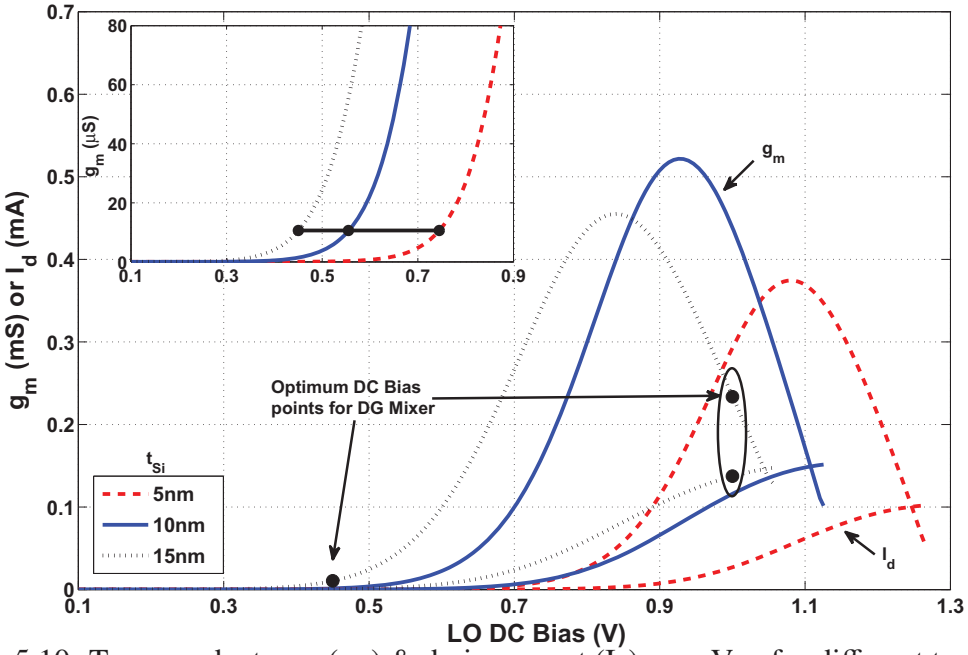


Figure 5.10: Transconductance (g_m) & drain current (I_d) over V_{LO} for different t_{Si}s. Out of two optimum bias points, the lower one at 0.45 V (15nm) is chosen for better stability and power efficiency [18].

(impractical) doping levels. However, from Fig. 5.12 we find that t_{Si} is a more significant parameter for conversion gain optimization. In a given gate length there appears to be an optimum body thickness that maximizes the conversion gain. For example, at L_{gate} of 45 nm and 90 nm, the optimum body thickness is 10 nm and 30 nm, respectively. At either extreme of these values, the conversion gain is compromised due to the SCEs in the higher end and quantum size effects at the lower end. Thus it is important to include both 2D/3D simulations and quantum corrections to optimize mixing performance in such nano-scale transistors, as with the case in this study [14], [18].

We like to draw attention that the weak dependence of performance on the structural parameters here is a result of careful bias optimization. It also indicates that the choice of bias conditions, particularly the LO DC bias, is the most dominant handle in using DG-MOSFET active mixer. Admittedly, this observation may be counter intuitive, because

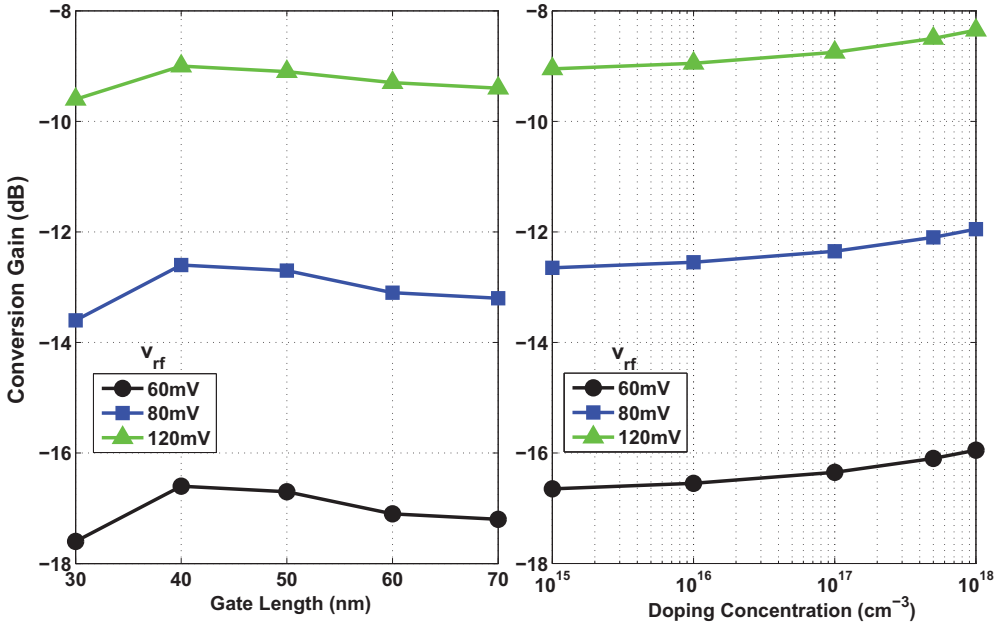


Figure 5.11: Dependence of CG on the gate length (L_{gate}s) & doping concentration (N_A) for different AC Inputs. The weak correlation of these two parameters on the CG is clearly evident [18].

the SCE are well known to adversely impact analog performance of the conventional MOSFETs in sub-100 nm regime. However, these adverse impacts are mostly related to the increase of the non-linearity in g_m which is certainly helpful for a mixer. In any case the well-scaled nature of the DG-MOSFET minimizes the emergence of strong SCEs for the mixer performance [14], [18].

Moreover, the apparent stability of mixer performance with device geometrical scaling could affect the phase noise in both positive and negative fashion. In terms of inter-device performance variations, the DG-MOSFETs will not suffer as much as the logic applications as the process variations in geometry does not appear to be a worry. However, since the LO-DC bias is the most important figure of merit, variations in threshold among devices and biasing errors/variations in circuits can be the main source of noise and limit the performance [14], [18].

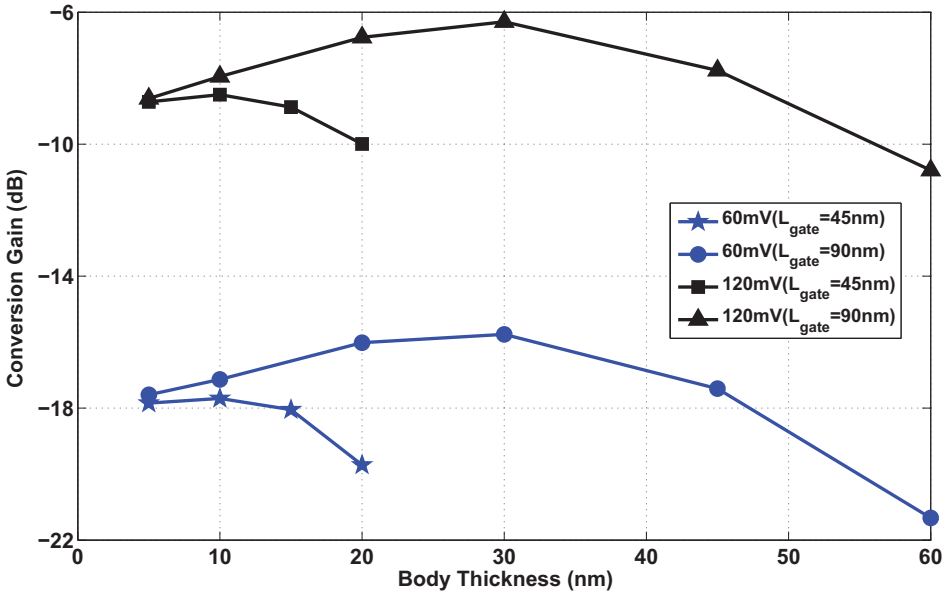


Figure 5.12: Dependence of CG on the body thickness (t_{Si}) for different AC Inputs. CG varies with L_{gate} because of short channel effects [18].

5.2.5 Noise & Linearity Performance

The mixer noise is dominated by the channel thermal noise of the MOSFET and the load resistor, R_L. The thermal noise can be approximated as a white noise implying the power spectral density is bandwidth independent. Therefore the mixer noise mainly arises due to the structural parameters of that depends on thermal and the load resistor used in the circuit. The body thickness being the most significant parameter, we have determined the noise figure (NF) of the circuit for its three different values. As expected from the V_T (Fig. 5.2) plot earlier, lower the body thickness higher the NF. The NF ranges between 7.9 dB to 9.1 dB for 2.4 GHz frequency (Fig. 5.13). We also examine the circuit for linearity implementing the two tone frequency analysis around 2.4 GHz (Fig. 5.14). The 3rd order Input Intercept point (IIP_3) is found to be 14.1 dBm for 2 dBm LO power, indicating its impressive suitability for RF applications [14], [18].

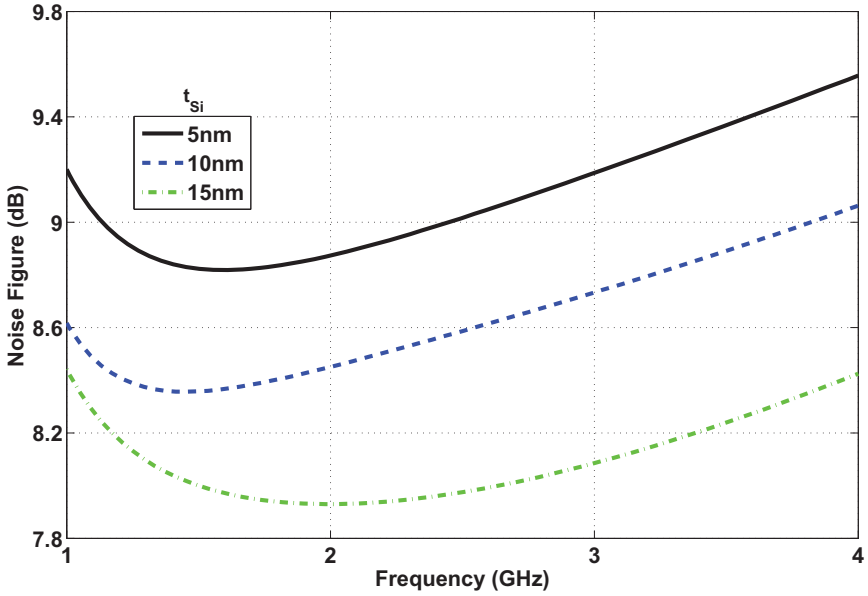


Figure 5.13: The Noise Figure for the three different values of t_{Si}s are measured against frequency [18].

5.3 DG-MOSFET Phase Frequency Detector

In this section, the use of DG-MOSFET in the design of Charge Pump Phase Frequency Detectors (PFD)s in 32 nm and 45 nm DG MOSFET technologies is implemented [14], [19]. The DG-MOSFETs are used to design the universal NOR gate which is the only building block for the PFD. The DG-MOSFET NOR gate consists of half the transistor count compared to NOR gate designed in conventional CMOS. Thus 2 transistors make up the DG-MOSFET 2-input NOR gate as opposed to 4 needed in conventional CMOS. This reduction in transistor count makes the PFD area efficient. The reduced transistor count also lowers the parasitic capacitances which enhances speed. Here, it has been demonstrated that for tiny phase errors of 60 ps and 80 ps the rise time of the output of a DG-MOSFET based PFD reaches the desired threshold of logic 'HIGH' required to initiate the charge pump switches that follows the PFD, whereas it fails for conventional CMOS, in 32 nm

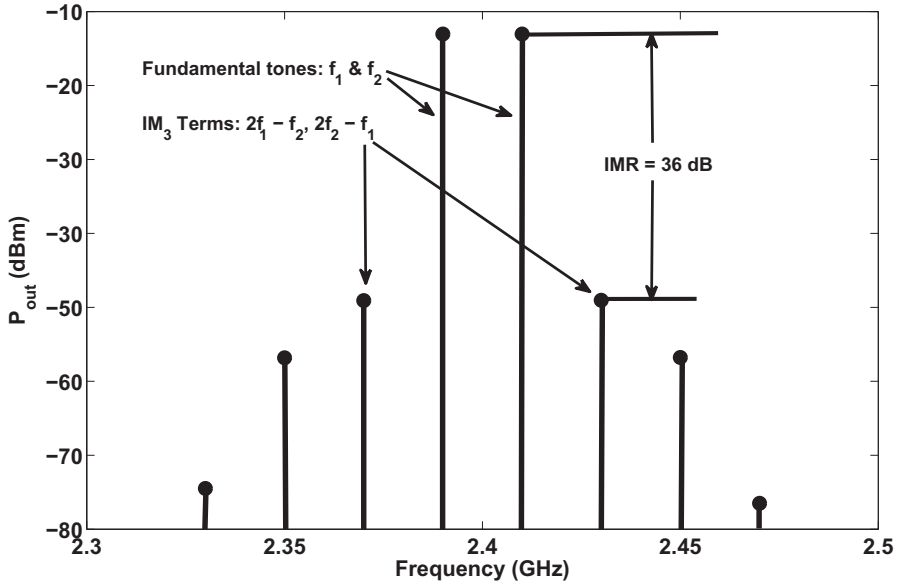


Figure 5.14: Computation of IIP_3 using two tone frequency analysis (2.39 GHz and 2.41 GHz) around 2.4 GHz [18].

and 45 nm technologies respectively. The DG-MOSFET thus finds application as a better alternative to conventional CMOS for dead zone avoidance in Phase Locked Loops (PLLs).

5.3.1 DG-MOSFET NOR Gate

The DG MOSFET NOR gate consists of only two DG transistors instead of four as in conventional CMOS architecture (Fig. 5.15). This was first proposed by Chiang et. al [88]. The design employs the threshold-voltage (V_T) difference between double-gated and single-gated modes in a *high* V_T DG device to reduce the number of transistors by half. When one of the gates in the *high* V_T device is turned on, the channel current is still insufficient to turn 'ON' the device due to *higher* V_T and large subthreshold swing [88]. Therefore, the device is still considered switched 'OFF' for all practical applications. When both gates are turned on, (which is only possible for a DG device) due to the gate to gate coupling, the V_T and subthreshold swing are significantly reduced, and large 'ON' current flows through the

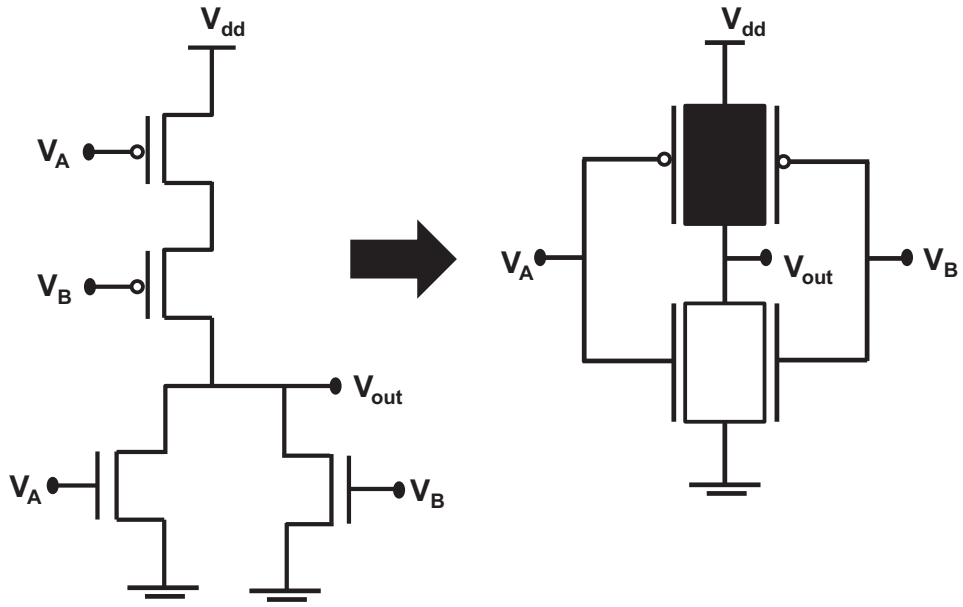


Figure 5.15: 2-Input NOR Logic Gate in Conventional CMOS and its equivalent in DG-MOSFET. Two transistors are required in the DG-MOSFET. The PMOS in DG-MOSFET is kept at a high-V_T symbolized by a filled transistor [14], [19].

device channels. Thus, the device is 'ON' and conducts current *only* when both gates are switched on [88]. The PMOS in the NOR logic circuit is kept at this *high* V_T configuration as indicated by a filled transistor symbol in Fig. 5.15. Therefore, when both the inputs A and B are 'LOW' *only* then the PMOS is 'ON' and the output goes to the 'HIGH'. In all other cases the output remains 'LOW' in conformity with the NOR logic.

It is worth noting although the *high* V_T devices have a poor performance for SCEs [29], the SCE for the high V_T DG PMOS device can be overcome due to the gate capacitive coupling of the DG device. On the other hand, the regular V_T NMOS is 'ON' when any one of the gates is 'HIGH'. The NOR logic with DG-MOSFETS is shown in Fig. 5.16. One of the major advantages of using NOR gates using DG-MOSFETs is speed.

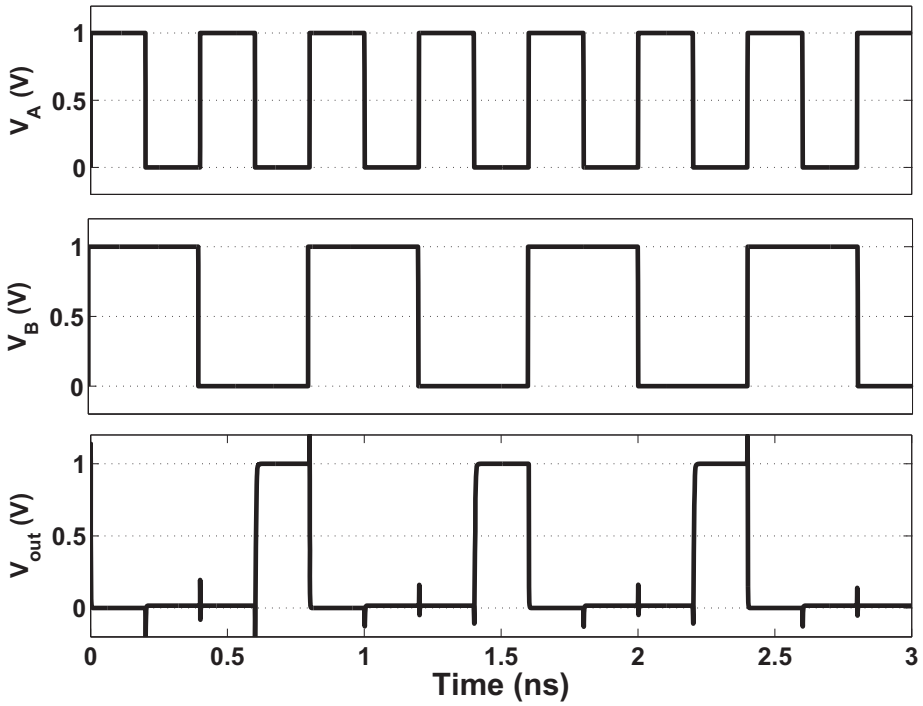


Figure 5.16: 2-Input DG-MOSFET NOR Logic waveform as simulated in HSPICE for V_{DD} = 1 V [14], [19].

The area and capacitance of the DG-MOSFET NOR gate is almost 2x less than the conventional CMOS due to reduced transistor count (half that of conventional CMOS)and associated isolation and wirings which lowers the capacitance and speeds up the circuit. In Fig. 5.17 this fact is demonstrated for different supply voltages [14], [19]. The advantage in higher speed is crucial for tiny phase error detection and is the subject of the following section.

5.3.2 Charge Pump PFD

The Charge Pump PFD which is widely used in PLL applications usually consists of two D Flip Flops and a reset circuit. The two D Flip Flops shown in Fig. 5.18 are implemented with eight NOR gates. The reset path consists of another NOR gate. In this

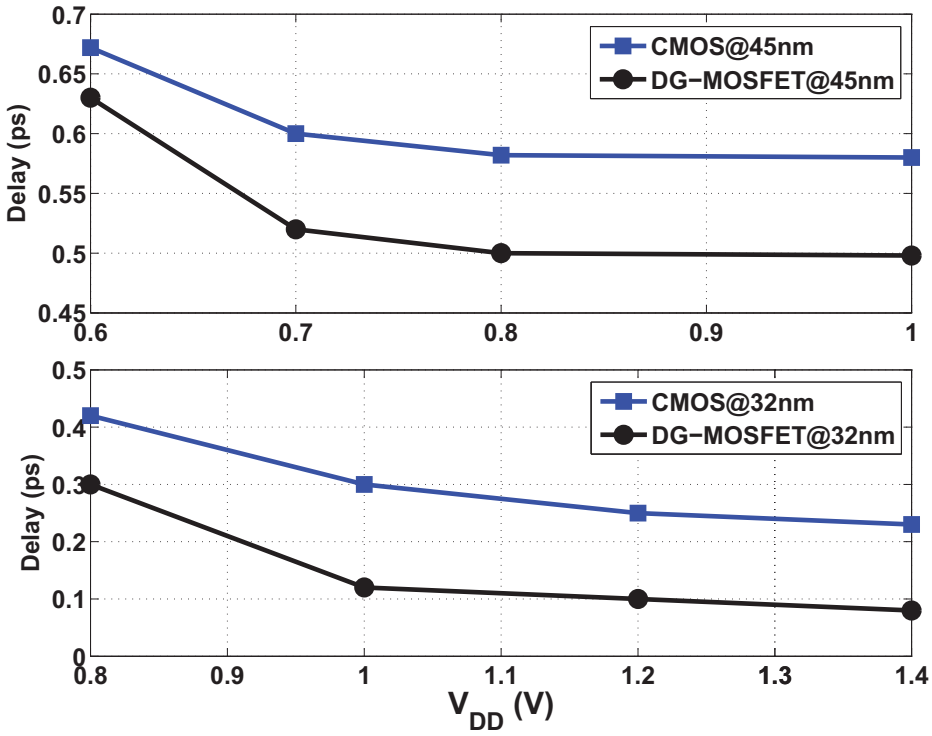


Figure 5.17: Delay comparison of 2-input NOR gate between conventional CMOS and DG-MOSFET for different supply voltages [14], [19].

paper, each of the NOR gates are constructed with DG-MOSFETs as described earlier and shown in Fig. 5.15. The Charge Pump which is basically a current steering DAC consists of two DG-MOSFET NMOS switches implemented in regular V_T configuration [14], [19].

The analysis at 32 nm gate length is carried with a supply of 1.2 V for $(W/L)_p$ = 2.84 μm / 32 nm and $(W/L)_n$ = 0.7 μm / 32 nm while at 45 nm gate length it is carried with a supply of 1.0 V for $(W/L)_p$ = 4 μm / 45 nm and $(W/L)_n$ = 1 μm / 45 nm for both the DG-MOSFET and conventional CMOS. The BSIM4 model that explicitly addresses many issues in modeling sub-0.13 micron technology and mixed signal high-speed CMOS circuit simulations is used and simulated in Synopsys HSPICE for the conventional CMOS [14], [19].

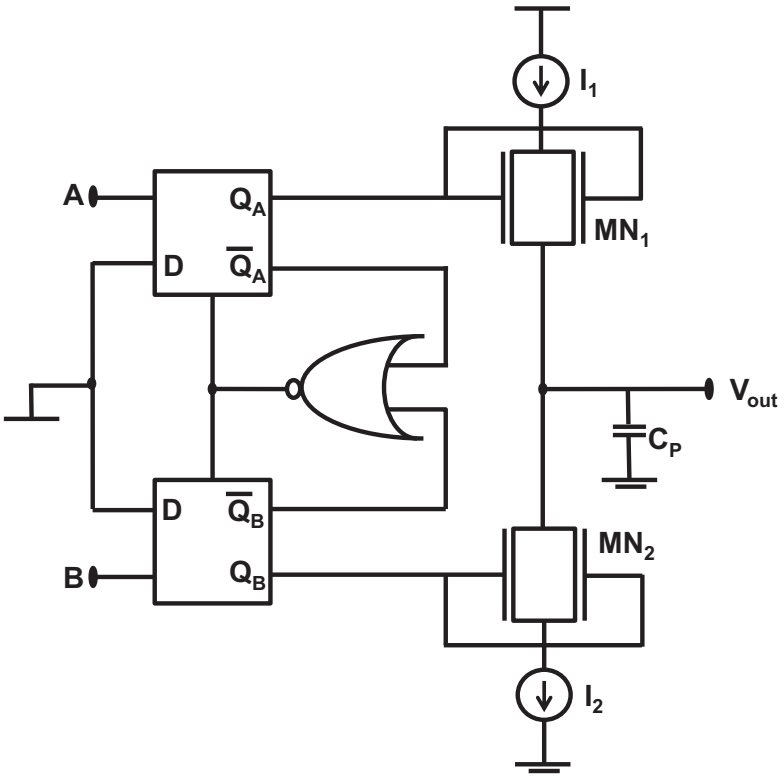


Figure 5.18: The Charge Pump PFD circuit implemented with DG-MOSFETs [14], [19].

It is to be noted, that although the drive current (I_{ON}) for DG-MOSFET is higher for both regular and high V_T configurations than that of a conventional CMOS, the reduction in the number of transistor counts, reduces the power consumption marginally in DG-MOSFET for both the gate lengths. The area is also reduced almost by half resulting from this [14], [19].

The phase error between two pulses A and B can be correctly detected for both conventional CMOS and DG-MOSFET when the phase error between the two pulses (T_{pe}) is above a certain threshold. This is illustrated in Fig. 5.19 for T_{pe} = 1 ns. Referring to the previous section on speed enhancement of DG-MOSFET based NOR architecture it can be deduced that the rise time of the DG-MOSFET (T_{thDG}) is faster than that for rise time of conventional CMOS (T_{thSG}) to reach the desired threshold of logic 'HIGH' and thus we

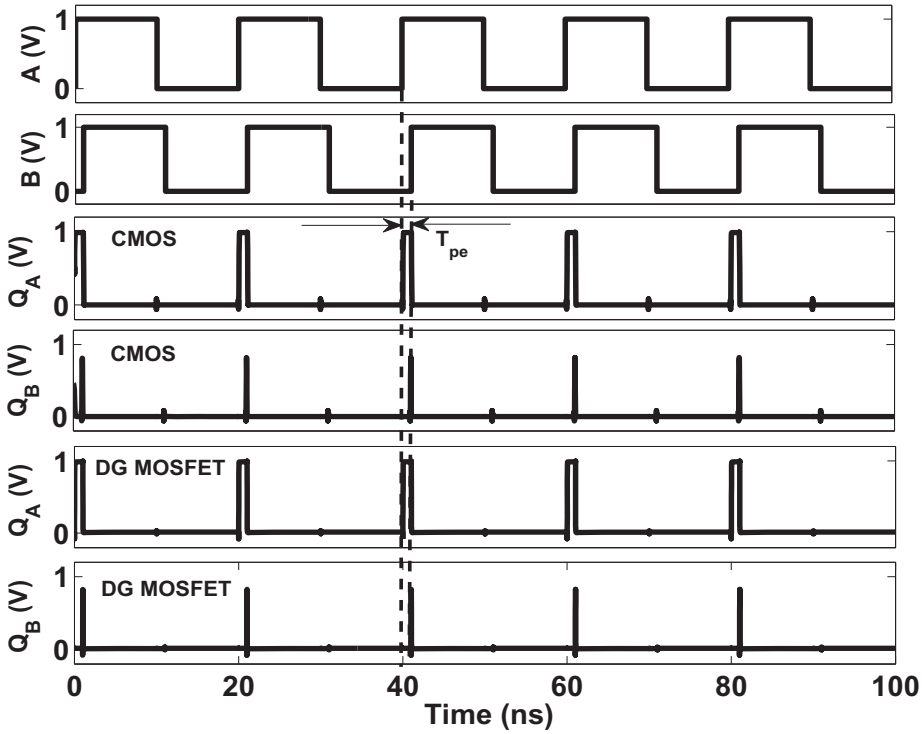


Figure 5.19: Phase error characteristics of two pulses A & B for conventional CMOS and DG-MOSFET for a phase error of 1 ns [14], [19].

can write $T_{thDG} < T_{thSG}$. However, for low phase error applications, when $T_{thDG} \leq T_{pe} \leq T_{thSG}$, the PFD ceases to work correctly for the conventional CMOS.

As observed at 32 nm gate length from Fig. 5.20, for $T_{pe} = 60$ ps, for the conventional CMOS, the voltage at the output Q_A of the flip flop fails to reach the threshold to switch on the current steering DAC transistor MN_1 in the period when A is 'HIGH' and B is 'LOW'. The voltage *only* reaches the threshold when both A and B are HIGH. When B is high the voltage at Q_B also reaches 'HIGH' which turns the transistor MN_2 'ON' [14], [19].

Therefore, when both Q_A and Q_B are 'HIGH' (reaches the V_T) simultaneously, the current I_1 instead of charging the capacitor C_P passes through the switch MN_2. Thus the output voltage (V_{out}) remains nearly constant and changes only by a fraction of what should be in order to send the accurate message of phase error to the VCO, which follows the PFD

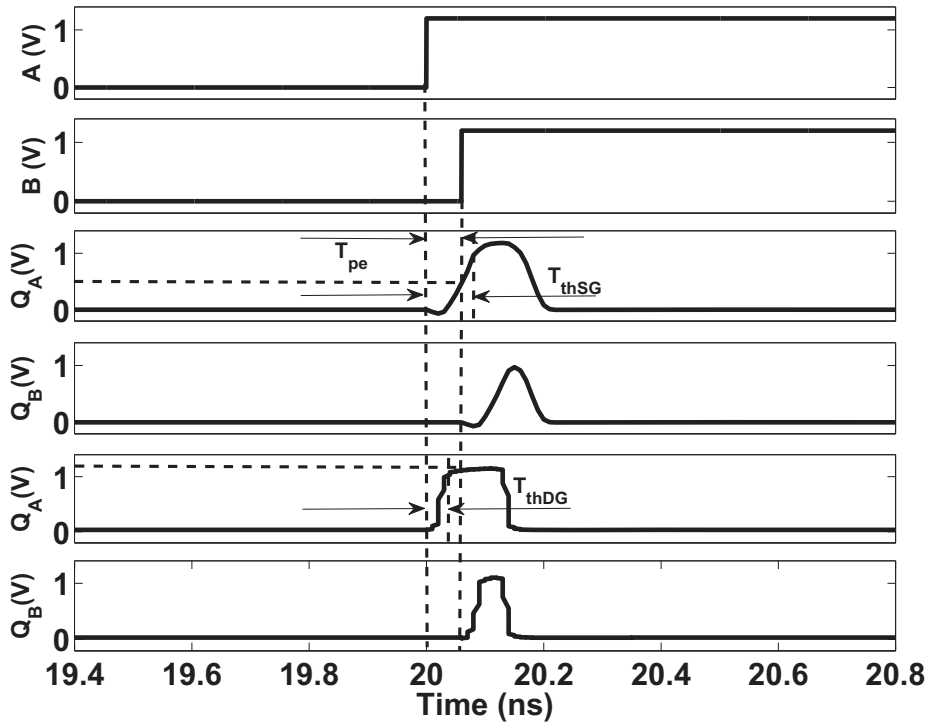


Figure 5.20: Phase error characteristics of two pulses A & B for conventional CMOS and DG-MOSFET for a phase error of 60 ps at 32 nm gate length. ($T_{thDG} \leq T_{pe} \leq T_{thSG}$) [14], [19]

in a PLL architecture. As a matter of fact, the V_{out} changes negligibly by an erroneous 0.005 mV for 100 ns. This is certainly an incorrect feedback to the VCO. The V_{out} characteristics is verified from Fig. 5.21. This is the familiar dead zone condition where there is no or negligible charge pump current that contributes to an unchanged V_{out} [14], [19].

On the contrary, the advantage of DG-MOSFET is clearly evident from Fig. 5.20 where it can be confirmed that for the same period the threshold for the DG-MOSFET reaches the logic 'HIGH' when A is 'HIGH' and B is 'LOW'. Thus the current I_1 cannot escape through MN_2 and charges C_P instead. This is clearly because even when $T_{pe} \leq T_{thSG}$, the inequality $T_{pe} \geq T_{thDG}$, is still valid due to the fact that $T_{thDG} < T_{thSG}$ owing to the lower capacitance as discussed in the previous section. Thus the dead zone is avoided with the

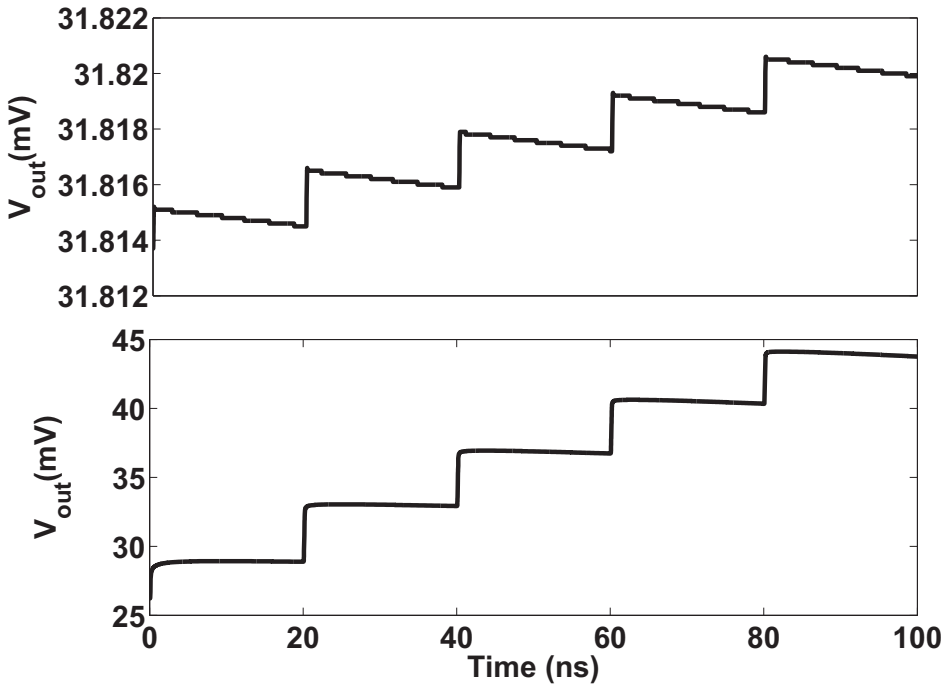


Figure 5.21: Charge Pump output voltage characteristics of Conventional CMOS and DG-MOSFET when $T_{thDG} \leq T_{pe} \leq T_{thSG}$ [14], [19].

correct and significant change of 15 mV in V_{out} for the same duration as that of conventional CMOS [14], [19] (Fig. 5.21).

It is to be noted as the gate length increases the conventional CMOS ceases to work correctly at higher phase errors. The output of the PFD is illustrated at 45 nm gate length for T_{pe} = 80 ps for both DG-MOSFETs and conventional CMOS in Fig. 5.22.

5.4 Summary

In the first section of the chapter, a systematic study of performance and design space for a single DG-MOSFET active mixer has been presented. The rigorously maintained temporal resolution in this simulation study, a careful bias conditioning and an accurate comparative analysis of device geometry are the distinguishing features of this study, which sets it apart from earlier efforts to evaluate this nanoscale compact mixer

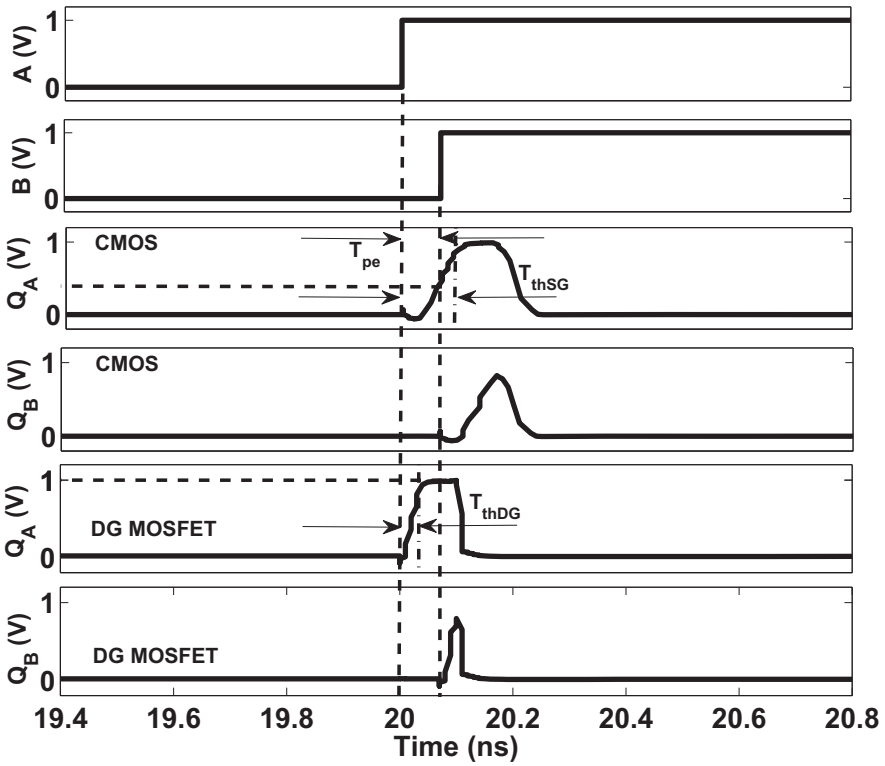


Figure 5.22: Phase error characteristics of two pulses A & B for conventional CMOS and DG-MOSFET for a phase error of 80 ps at 45 nm gate length. ($T_{thDG} \leq T_{pe} \leq T_{thSG}$) [14], [19]

topology. The optimum DC bias operating points have been established for different device geometrical constraints parameters, providing guidelines in the design of power efficient high-performance DG-MOSFET based mixer circuits. The investigation of the dependence of conversion gain on the device structural parameters indicates a rather weak correlation of the conversion gain with the gate length, doping concentration and body thickness. Thus we find that DC biasing conditions determine the final mixer performance most readily. Our observations affirm the body thickness as the most important parameter to optimize structurally and implicates the SCEs as still present but a weaker force to limit the performance of the DG-MOSFET mixer.

It can be noted that although we have studied and established general trends between the physical design (channel length, doping concentration and body thickness) of DG-MOSFETs and the conversion gain, we have not attempted to define general 'empirical' relationships for the operating point firstly because DG-MOSFET is a three dimensional structure and in extremely small devices true 3D simulations may be needed before general conclusions can be validated. Secondly, the actual implementations of DG-MOSFETs may vary considerably among the manufacturers and significant changes to the channel geometry and gate stack may limit the validity of the analytical relationships. Thus, further 3D simulations and precise optimizations may be required to obtain a unique relationship between the operating point and other physical parameters such as V_T in a given implementation of a DG-MOSFET.

In the next section of the chapter, the impressive characteristics of the charge pump PFD implemented with nanoscale DG-MOSFETs have been investigated. The dead zone free execution and improved area efficiency of the circuit owe to the use of reduced number of transistors which in turn reduce the parasitics. The faster rise time of DG-MOSFET charge pump PFD, due to lower parasitics allows successful application for tiny phase error detections to avoid dead zones in PLLs, something not possible in conventional CMOS without resorting to additional delay networks.

6 RFIC IN COMMERCIAL CMOS TECHNOLOGY

6.1 Introduction

Circuits introduced in the previous sections are all novel and interesting building blocks for communications systems, all to be built using DG-MOSFET technology. However, the research with these novel MOSFET technology currently suffer from the following limitation:

The RF wireless circuit design with DG-MOSFET is a highly advanced nanoscale research and commercial processes for the device are not yet available. TSMC is planning to bring the first process for FinFET/DG-MOSFET commercially available by the end of 2016 [103]. As a result currently the circuits implemented with DG-MOSFET cannot be fabricated and be verified through measurements for better accuracy.

The primary objective of the current research is to establish the advantage in functional and behavioral characteristics of the different wireless integrated circuits implemented with DG-MOSFETs. These characteristics have been accurately determined from the design simulation and qualitative analysis. However, the numerical values of different figure of merits of different wireless integrated circuits are determined with some degree of error because of the exclusion of device parasitics in the academic DG-MOSFET process, that can be incorporated only in commercial/practical processes.

To fill this gap and to gain experience with the ‘practical/accurate’ commercial process that is eventually required in the industry or in higher academic/commercial research, an extended work on OOK TRx design with the conventional CMOS technology such as described in this section has been completed. This eventually paves the way for a comparative analysis between the commercial RF CMOS model and the academic DG-MOSFET model. The comparison affirms the correctness of the academic DG-MOSFET

model through the similarity in the fundamental characteristics of the different wireless TRx blocks implemented in both the technologies.

6.2 Transceiver in 65 nm RF CMOS

To address above concerns, we have used the commercial process design kit available through MOSIS academic foundry, provided to us with a special 'research only' permission (it costs > $100k to get 25 chips produced on these technologies, even under MOSIS license), to design an OOK transciever, which is introduced in this section. The design kit is termed CMOS 10LPE/10RFE and is based on 65 nm CMOS technology from IBM, and comes with necessary RF components added on such as inductors and RF MOSFETs with multi-finger gates. The system is designed to operate around 90 GHz for ultra-short range and efficient wireless on/off-chip interconnects.

6.2.1 Transmitter Design

In this section, simple component by component breakdown of OOK transmitter, which is very similar in principle to one introduced earlier with DG-MOSFET is provided.

6.2.1.1 VCO

To achieve higher oscillation frequency, push-push VCOs are reported [104],[105]. Transistors MN_1 and MN_2 form the cross-coupled VCO core in the architecture. The transmission lines, T_1, and T_2, and varactor C_1, serve as the LC tank to determine the fundamental oscillation frequency of 90 GHz. The schematic is shown in Fig. 6.1. MN_3 and MN_4, are the output buffers for the differential fundamental signals. The second-harmonic signal is extracted from the center of T_1, and T_2. The phase noise of the VCO is determined to be -97 dBc/Hz at 1 MHz offset for the 90 GHz center frequency and is shown in Fig. 6.2. The DC power dissipation is 11.6 mW. The OOK switching is implemented in the tail of

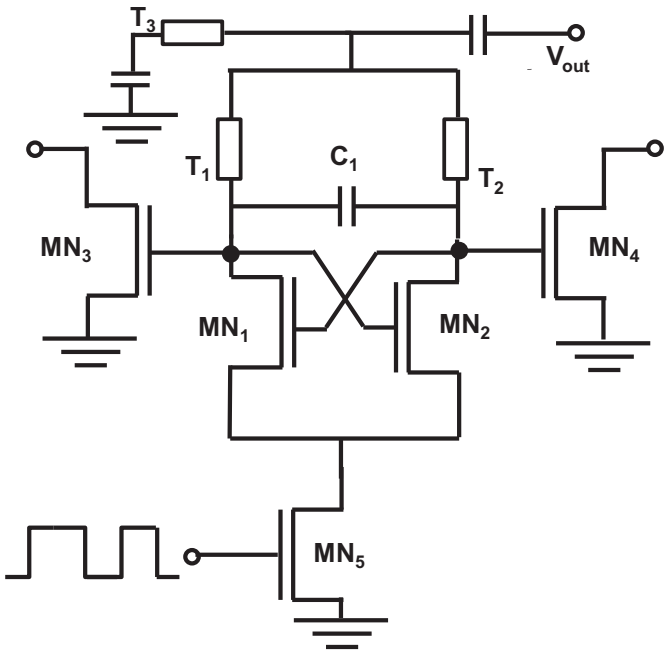


Figure 6.1: Push-Push VCO with OOK Modulation in 65 nm CMOS.

the VCO by the MOSFET switch MN_5 (Fig. 6.1).

6.2.1.2 Power Amplifier

The PA is designed in 65-nm IBM RF CMOS technology. It is a 2 stage common source (CS) cascade design. The simplified schematic is shown in Fig. 6.3. The CS configuration is chosen because it provides high gain and output power under low voltage operation. As we do not require very high gain, the cascode topology is eliminated for the design as it requires higher bias voltage (hence consumes more power) and degrades the PAE. The S_{21} of the PA is intentionally reduced to gain in power efficiency. The ultra-short range on chip communication does not necessitate high gain PA. The 3-dB bandwidth is $\geq$ 20 GHz, as evident from Fig. 6.4. The input and output return losses (S_{11} & S_{22}) are also obtained from the simulation. The output return loss is 10% or less for the frequency range of nearly 20

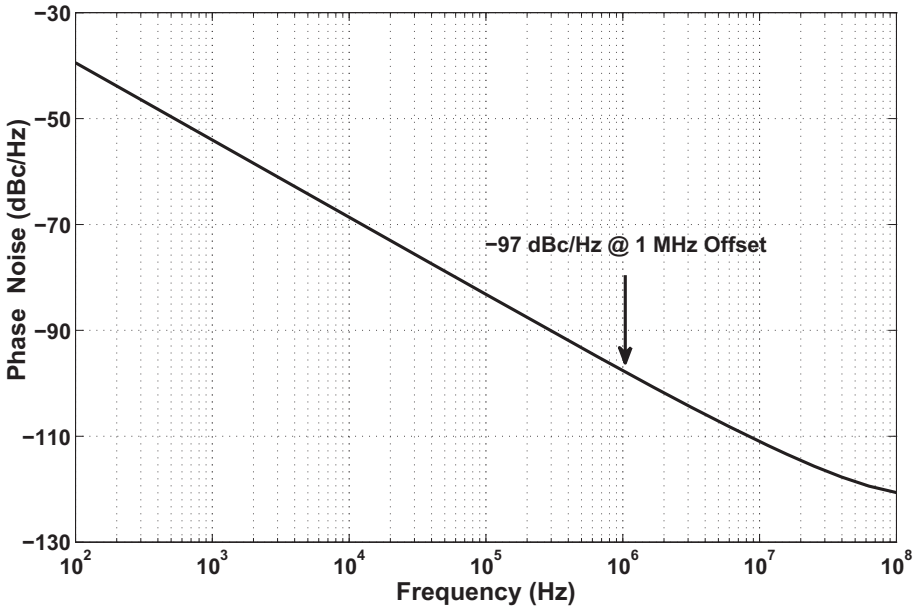


Figure 6.2: The phase noise of the VCO. The Push Push VCO configuration has a phase noise of -97 dBc/Hz at 1 MHz offset.

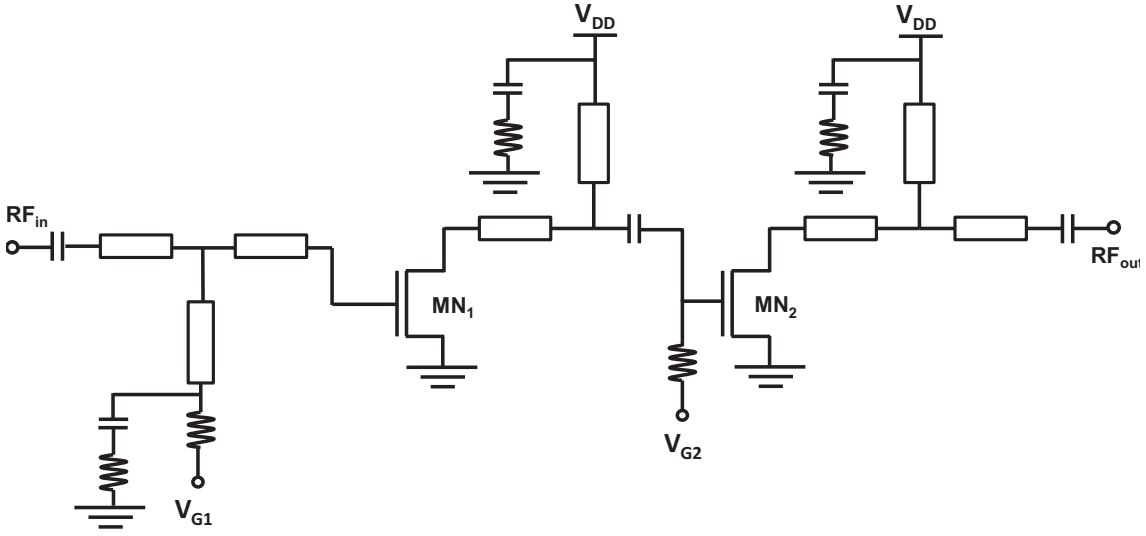


Figure 6.3: Power Amplifier circuit in 65 nm CMOS.

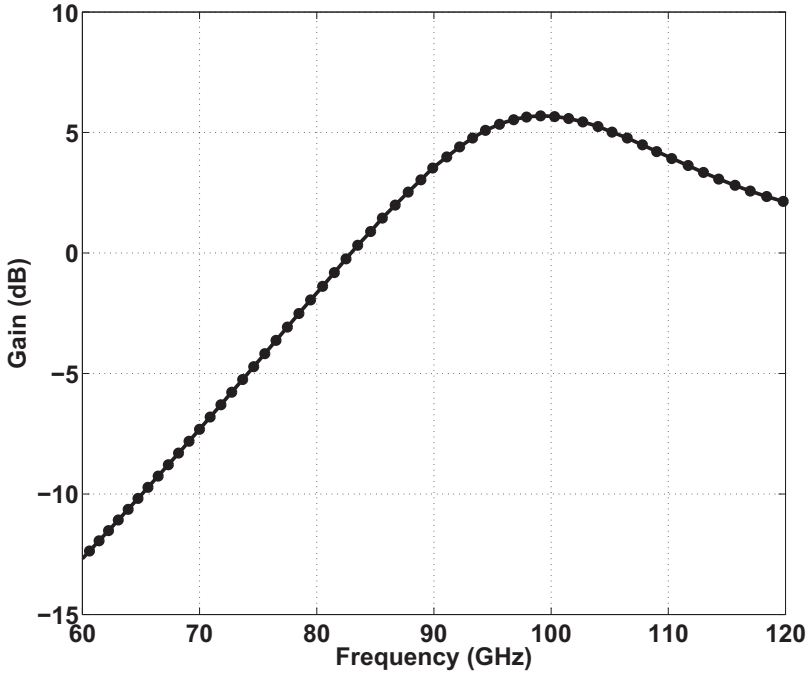


Figure 6.4: The gain of the Power Amplifier.

GHz, centered on the 90 GHz frequency (Fig. 6.5) attest to the wideband application of the PA. The rollet stability factor remains more than unity for this operating range and the IIP3 are found to 16.8 dBm respectively. The PAE of this amplifier is 16%. The DC power dissipation is 11.3 mW. The total layout area of the Tx is 0.42 mm^2.

6.2.2 Receiver Design

Likewise, here simple component by component breakdown of OOK receiver is illustrated.

6.2.2.1 LNA

The LNA designed is a 2 stage cascode structure consisting of four transistors in the combined CS and CG configuration. The source degeneration circuit consisting of T_4

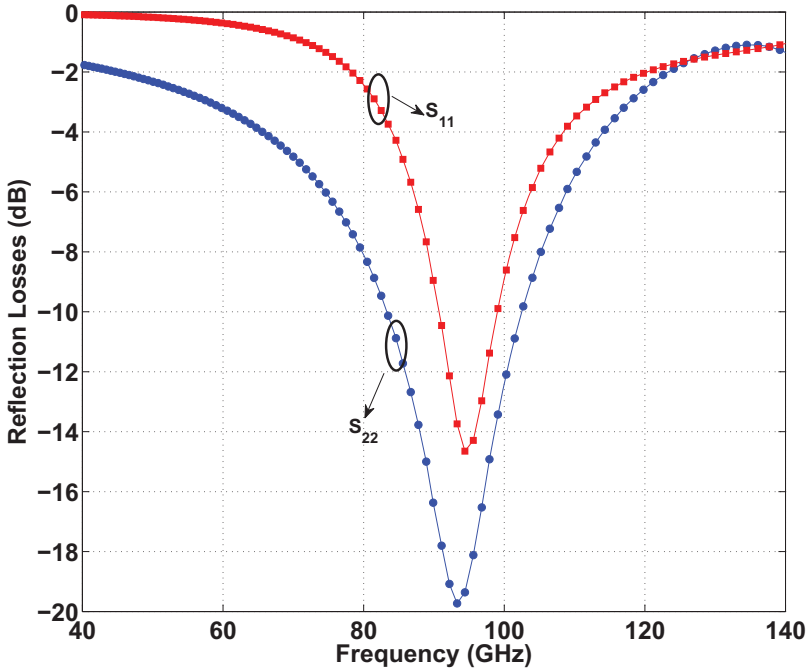


Figure 6.5: The reflection losses of the Power Amplifier.

yields in real part wide band inter-stage impedance matching for maximizing the power transfer between the stages. The source degeneration also stabilizes the LNA (Fig. 6.6). The transistor MN_3 acts in common gate configuration and one of its gate is grounded with the aid of the peaking T-line T_6 and a bypass capacitor C_2. Along with achieving a near constant gain by maintaining the flatness, the bandwidth of the amplifier is also increased with the aid of this peaking inductor. A high pass T-network (T_7 & C_3) is used as the matching circuit

The simulation verifies the S_{21} to vary from 90 to 120 GHz, while maintaining a desired flatness. The gain changes by less than 10% in this frequency range, attesting to the extremity of the flatness and ultra-wideband application. The peak gain is observed at 10 dB (Fig. 6.7). The input return loss is 10% or less for the frequency range of more than 40 GHz, centered around the 100 GHz (Fig. 6.8). This certainly indicates the ultra-

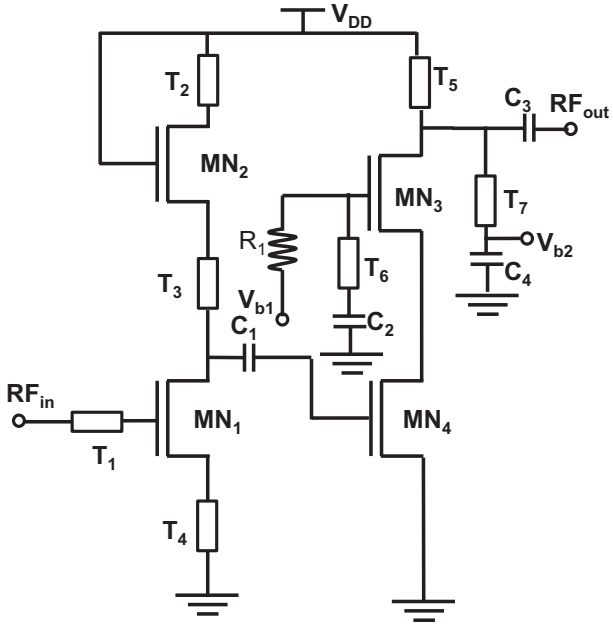


Figure 6.6: Low Noise Amplifier circuit in 65 nm CMOS.

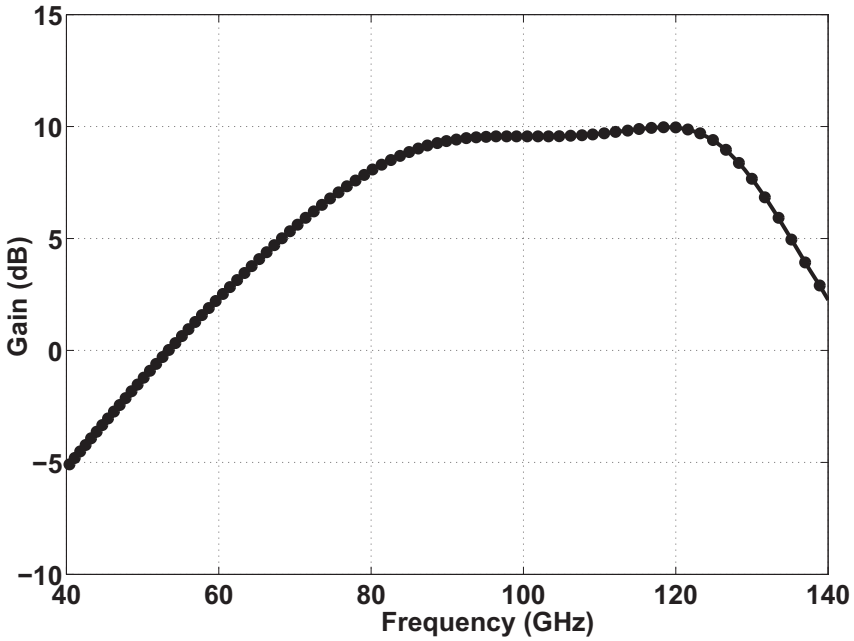


Figure 6.7: The gain of the LNA.

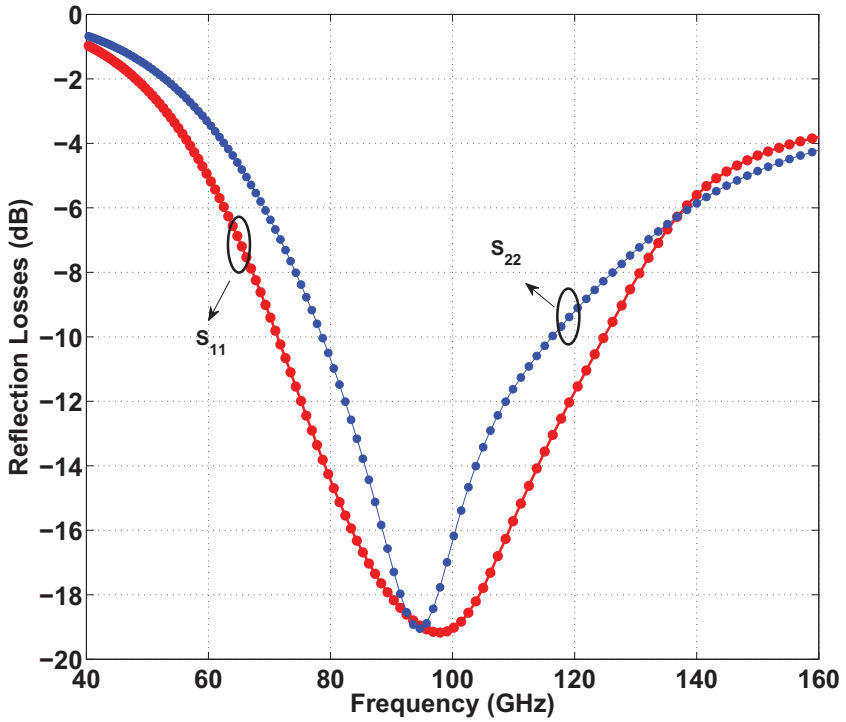


Figure 6.8: The reflection losses of the LNA.

wideband application of the LNA. The Noise Figure varies from 6 dB to 10 dB in the same frequency range (Fig. 6.9). The IIP_3 of the LNA is -6.1 dBm. The unconditional stability of the amplifier is also verified from the Rollet Stability Factor. The DC power dissipated by the LNA is 11.8 mA.

6.2.2.2 Envelope Detector

The demodulation of a non-coherent modulated wave requires an envelope detector. The envelope detector is basically a rectifier circuit that generates an envelope of the incoming high frequency carrier signal and strips off the carrier to recover the data. In Fig. 6.10, we have illustrated an envelope detector circuit in which the output is inverted to that of binary input. The output signal needs further to be passed through an inverter for the recovery of the original signal. Although requires additional hardware, this circuit has an

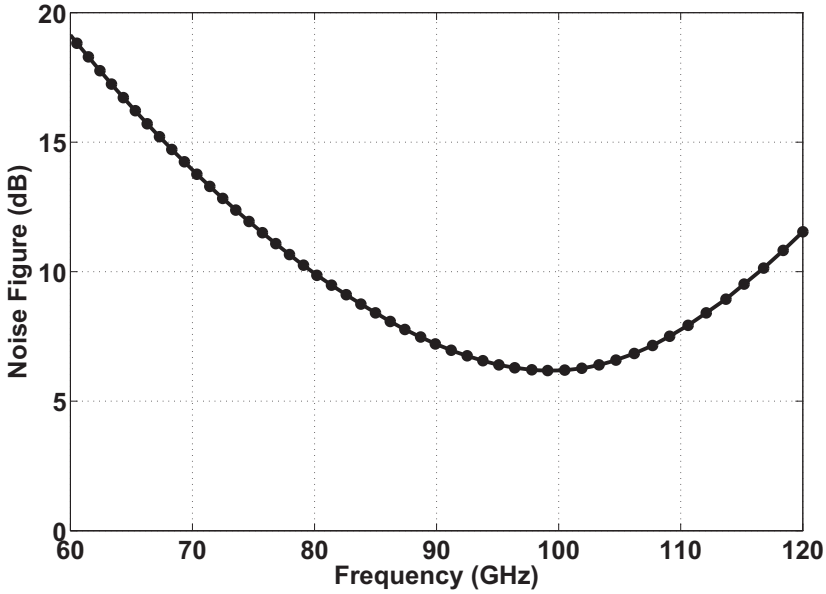


Figure 6.9: The noise figure of the LNA.

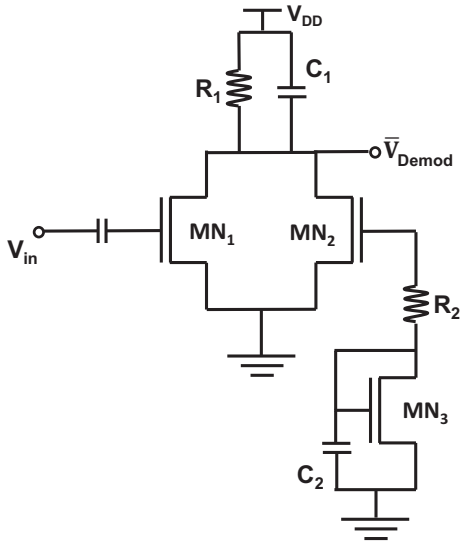


Figure 6.10: The Envelope Detector in 65 nm CMOS.

advantage over the straightforward recovery as the former has a better output swing over the latter [97]. The modified circuit rectifies the input by the common-source amplifier MN_1.

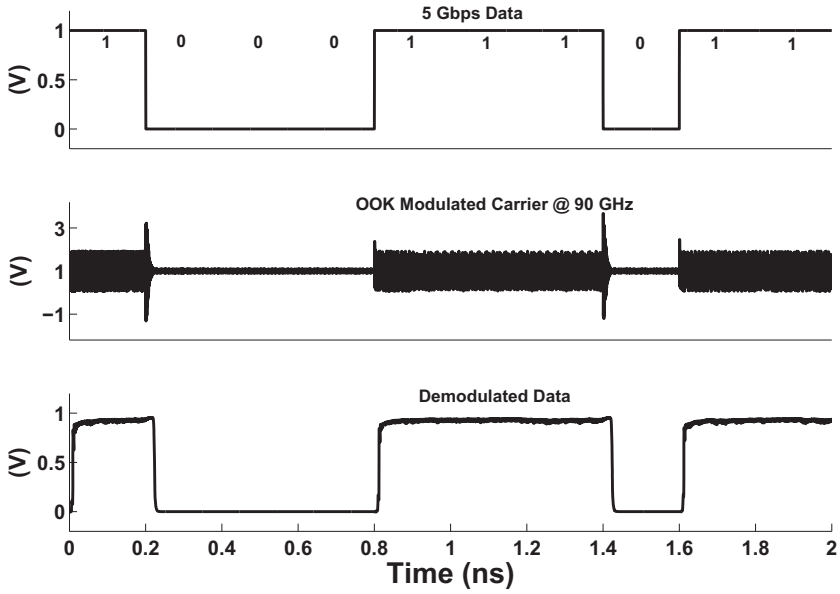


Figure 6.11: The verification of OOK demodulation.

Here, the network R_1-C_1 filters out the undesired ripple allowing the recovered data to pass through it. The simulation (Fig. 6.11) illustrates the recovered binary input information. The high frequency noise present with logic 1 data at the output can be easily filtered out. The DC power dissipation is 3.9 mW. The total layout area of the Rx is 0.20 mm^2.

6.3 Summary

The chapter introduces a wideband 90 GHz power efficient OOK transceiver in 65 nm RF CMOS technology. In the entire design of the transceiver, inductors are replaced with microstrip transmission lines. The transmitter circuit consists of a push push VCO in which a tail switching is implemented for OOK modulation. A wideband 2 stage power amplifier is designed in which the gain is intentionally optimized for power efficiency. The receiver end constitutes a 2 stage inductive degeneration cascode LNA for greater bandwidth. The detection of the incoherent OOK modulated signal is accomplished with the design of an envelope detector.

7 Conclusion & Future Work

7.1 Conclusions

The primary objective of the current research is to establish the advantage in functional and behavioral characteristics of the different wireless integrated circuits implemented with DG-MOSFETs. This objective is validated from the design simulation and qualitative analysis and established the DG-MOSFET as a viable and better alternative to bulk CMOS in the design of nano scale wireless communication integrated circuits operating at mm-wave frequencies. A wide array of analog and mixed-signal circuits implemented in DG-MOSFET technology, which can be used in next generation integrated wireless communication, satellite communication systems and sensor networks, are verified.

In particular, for oscillators, the research documents the tunable frequency response in both the LC and relaxation oscillators. This tuning characteristic is achieved by back gate biasing in both the oscillators. In LC oscillator the back gate tuning replaces the need for any MOS varactors, otherwise required in conventional CMOS. For the relaxation oscillator, the tuning makes the oscillator voltage-controlled in addition to the usual current controlled capability, and the omission of a comparator circuit present in the original design. A quantitative small signal modelling validates the better leniency of the stability criterion for DG-MOSFET in comparison to CMOS. The LC oscillator is extended to the design of a quadrature oscillator, which is designed with only four transistors instead of eight as would have been required in CMOS.

A novel power and area efficient OOK modulator is designed which requires only two DG-MOSFETs, one for modulation and another high threshold device for strong switching.

The power amplifier designed in this research also make use of the advantage in back gate biasing. Here, the gain of the amplifier is varied for adaptive power efficient

applications. The figures of merit achieved through industry-standard SPICE simulations validate the viability of DG-MOSFET for nanoscale mm-wave applications over CMOS.

In the receiver end, a low noise amplifier is designed in which the significant gain switching characteristic is also achieved via back gate biasing. The conventional CMOS requires additional switching transistor to achieve the same, hence DG-MOSFET based design makes the LNA much faster by avoiding transistor switching and area efficient. Additionally, the area efficiency of the widely used common source inductive degeneration topology of the LNA is established via quantitative small signal modelling. Similar to PA, the LNA figures of merit achieved through industry-standard SPICE simulations further validate the viability of DG-MOSFET for nanoscale mm-wave applications over CMOS.

To demodulate an OOK modulated signal in the receiver, an envelope detector is required. This work presents a novel power and area efficient DG-MOSFET envelope detector. When comparing with the envelope detection in RF CMOS (from section 6.2.2.2) we can observe the DG-MOSFET based detection is noisy compared to its RF CMOS counterpart. This is primarily because of additional parasitic capacitances associated with the second gate in DG-MOSFETs. The current comparison is also not fair because of the inconsistencies in gate length, operating frequency, parasitics and simulation tool used for the two circuits as indicated in Tables 1.1 and 1.2.

A coherent receiver requires an RF Mixer to down convert the RF frequency to smaller intermediate frequencies. Keeping in mind the necessity of a coherent receiver for most wireless telecom applications, in this work, an RF Mixer is designed. A single DG-MOSFET RF mixer is utilized for the mixing of the RF and LO signals. The signals are applied to two gates of the DG-MOSFET device as opposed to the gate and source of the conventional CMOS. This reduces the RF-LO isolation improving the performance and avoiding the need of any power and area inefficient balanced version. In this work the mixing property of the DG-MOSFET is verified qualitatively. More importantly, the

research introduces a novel bias optimization technique to obtain the conversion gain/loss in DG-MOSFET mixers.

To demodulate the information from the carrier, a coherent receiver needs a Phase Locked Loop (PLL). In this dissertation, a charge pump phase frequency detector (CP-PFD), which is an essential ingredient in PLL architecture is designed. The DG-MOSFET based CP-PFD has the capability for better dead-zone avoidance in PLL compared to CMOS and is validated by computer simulation.

Finally, a low power wideband OOK TRx is designed in commercial RF CMOS to compare with the behaviorial and functional characteristics of the DG-MOSFET based OOK TRx.

With fabrication processes of DG-MOSFETs soon coming up with initiation from TSMC [106], [107] and rapidly expanding system-level efforts led by several national and international programs in US, Japan and Europe, along with several companies (such as Intel [25]) and academic centers focussing on these DG-MOSFET/FinFET/3DMOSFET technologies, we should expect a wide range of tunable analog RF circuits, reconfigurable logic blocks, on-chip power management blocks and mixed-signal system-on-chip applications to come into existence in the next few years. Electronic Design Automation (EDA) giants such as Cadence, Synopsys and Mentor Graphics are all gearing up to incorporate the technology in their simulator platforms [108].

Ultimately, with the ongoing nanotechnology revolution further performance improvements and architectural changes in devices are to be expected in the next decade and beyond. Our work here shows that such changes can be utilized by circuit engineering to result in very compact and capable systems, even when the actual change is to include merely an additional gate in the MOSFET architecture. This indicates that circuit engineering has a lot more to say not only in the final stretch of Moore's scaling, extending perhaps until 2020, but also in post-Moore area where fundamental fabric of building circuits may be al-

tered significantly, and novel devices architectures and materials such as graphene, carbon nanotube, nanowire or molecular transistors are likely to play a significant role.

Exciting recent developments on various DG-MOSFET devices can be found in [109]-[113] which is encouraging for this work. However, a word of caution is necessary. Despite the many advantages of DG-CMOS technology, there are still many technical challenges in implementing DG-MOSFETs, particularly in the independent-gate mode [114], used in many circuits found in this work. These are listed below:

- Achieving satisfactory self-alignment between the upper and lower gates.
- Fabrication of a thin silicon 'fin' tens of nanometers wide.
- Fabrication of fully impedance-matched gates on two sides of the fin.
- Setting up of DC bias in independent-gate operation of the device, which may require using an adjustable reference, DAC, or digital potentiometer combined with a temperature compensation source, which is not trivial.
- Dual routing required for both the gates in independent mode which will invariably add to the cost, area and parasitics.

Hence, these technical issues must be resolved before the proposed circuits and design advantages for DG-CMOS architecture can be fully realized.

7.2 Future Work

The current research has the necessary potential to implement the following extended works in the near future.

- The current work in DG-MOSFET is primarily implemented in 32nm & 45nm FinFET predictive technology model which is basically a non-commercial academic model modified from fully depleted SOI model of BSIM. Therefore although the

design simulation has been accurately possible, the post layout simulation and subsequently the tape out could not be implemented because of the absence of layout design rules in the predictive models of DG-MOSFET. Therefore, in this research, although the behavioral characteristics of the different wireless integrated circuits are accurately determined from the design simulation, quantitative and qualitative analyses, the numerical values of different figure of merits of different wireless integrated circuits are determined with some degree of error. This is because of the exclusion of device parasitics in the academic DG-MOSFET processes, which are incorporated only in commercial/practical processes. The tape out can be targeted in future when commercial technologies with layout design rules are available in the next 3-4 years.

- The current research is primarily targeted for mm-wave applications for wireless communication. In future, wireless circuits can be designed in DG-MOSFET for low frequency and ultra-low power applications such as in medical electronics and sensor networks.

- DG-MOSFET is equally competent technology in the mixed-signal domain such as in the implementation of various Analog to Digital Converters (ADCs) like the Delta-Sigma Modulator ADC. This can be a significant research project in the future. In this research, a charge pump PFD is designed in the mixed signal domain which can be further extended in the design of Phase Locked Loops (PLLs) in the future.

- In the present work, the primary focus was on the non-coherent TRx circuits and basic circuit blocks for more complex and higher fidelity coherent signal transmission and reception using Phase-locked loops (PLLs). However, the design and analysis of full PLL block was avoided. This is because transistor-level design and simulation of a PLL is not a trivial undertaking since 1000s of clock cycles in CPU and memory

intensive SPICE transient simulations are needed in the presence of randomizing signal sources to capture 'realistic' locking events, let alone identifying locking performance under different constraints. As a result, PLL design often involves behavioral models in which transfer function of fundamental system blocks are used in MATLAB Simulink (or any other capable systems simulation) package to deduce performance figures of merit such as stability, lock-range, jitter and power dissipation and so on. This work has already captured the basic information for many of the PLL building blocks (mixer, low-pass filter, VCO, and charge pump). Thus it would be highly desirable to succeed this work with a behavioral PLL design effort, using the transfer functions deduced from our work and designing missing blocks such as divider, ADC/DAC and so on.Such a study of PLL design using DG-MOSFET should also include comparable designs in established conventional RF-CMOS technology at the time (likely to be 45 or 32nm), so that a comparison can be made.

- To implement power efficiency further in both DG-MOSFET and RF CMOS circuits at very high frequencies, the supply voltage can be further reduced to operate near the device threshold. This can be effectively materialized when transistors with gate lengths < 28 nm are available in next 1-2 years. Even a 100 to 200 mV reduction in the supply can result in substantial power savings.

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Appendix A: Some Wireless Standards

GSM The Global System for Mobile Communication is a TDMA/FDD system with GMSK modulation, operating in different bands and called GSM 900, GSM 1800 and GSM 1900. The Fig. A.1 shows the Tx & Rx bands. Each channel is 200 kHz wide accomodating eight time multiplexed users. The data rate per user is 271 kbps. The Tx and Rx paths are offset by about 1.73 ms so that the two paths do not operate simultaneously. The total capacity of the system is 25 MHz BW and the numbers per channel is around 1000. The defined sensitivity of GSM 900 & 1800 are -104 dBm & -101 dBm. [58]. [58].

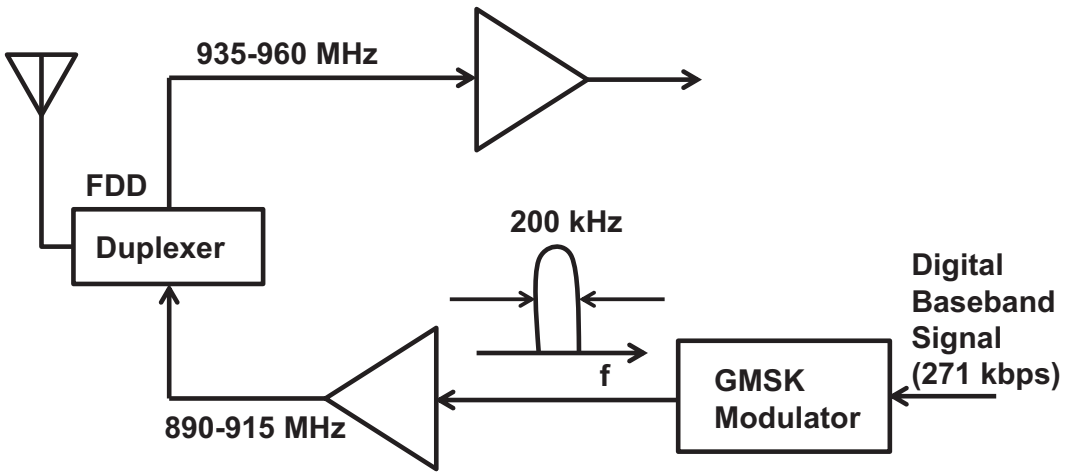

Figure A.1: GSM air interface.

IS 95 CDMA The CDMA uses FDD system with OQPSK modulation in the mobile unit. The Fig. A.2 shows the Tx & Rx bands. Each channel is 1.23 MHz wide with a data rate per user of 9.6 kbps. The link from the base station to the mobile unit incorporates QPSK modulation. The reason is that the mobile must use a power efficient modulation scheme,

whereas the base station need to have a linear power amplifier that transmits many channels simultaneously and hence OQPSK is not used

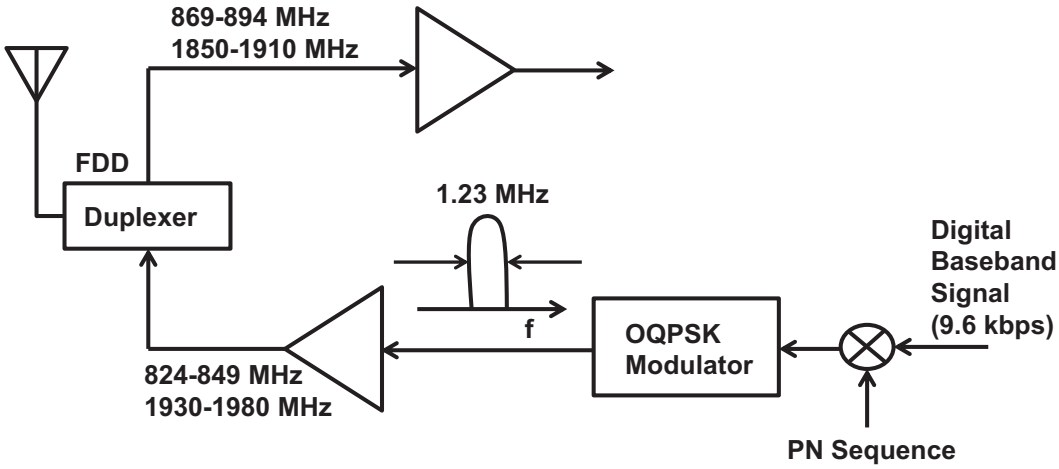

Figure A.2: CDMA (IS-95)air interface.

Wideband CDMA This is an extension of the IS 95 CDMA to achieve a higher data rate. Wideband CDMA (WCDMA) achieves a data rate of 384 kbps with the channel bandwidth of 5 MHz. IMT 2000, one of the several variants of WCDMA has an available bandwidth of 60 MHz from 1920-1980 MHz uplink and 2110-2170 MHz downlink. The receiver sensitivity is -107 dBm [58]. This is illustrated in Fig. A.3.

Bluetooth Bluetooth used TDD system and operates in the 2.4 GHz ISM band. Each channel carries 1 Mbps, occupies 1 MHz, and has a carrier frequency equal to (2402 + k) MHz, for k=0,...,78. The Tx uses GFSK modulator. The sensitivity is -70 to -80 dBm (for BER 10^{-3}). Mostly used for indoor wireless applications, hence this low sensitivity is readily met [58]. This is illustrated in Fig. A.4

IEEE 802.11a This standard allows high speed wireless connectivity, providing maximum data rate of 54 Mbps. It works in 5 GHz band with a channel spacing of 20 MHz

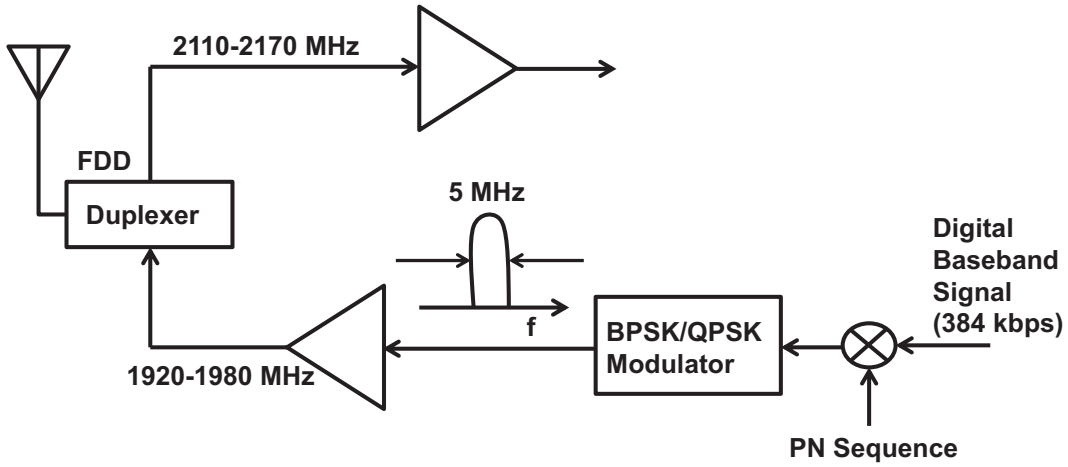

Figure A.3: WCDMA (IMT-2000)air interface.

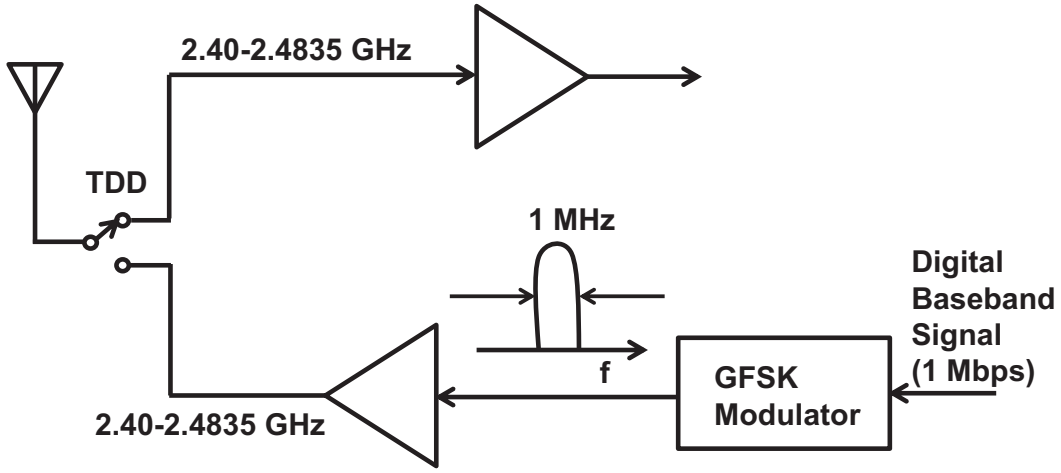

Figure A.4: Bluetooth air interface.

with different modulation schemes for different data rates. higher data rates use denser modulation schemes, posing tougher demands on TRx design. This illustrated in Fig. A.5

To minimize the effect of delay spread, wireless systems employ OFDM for data rates of a few megabits per second or more. The OFDM standard incorporates a total of 52

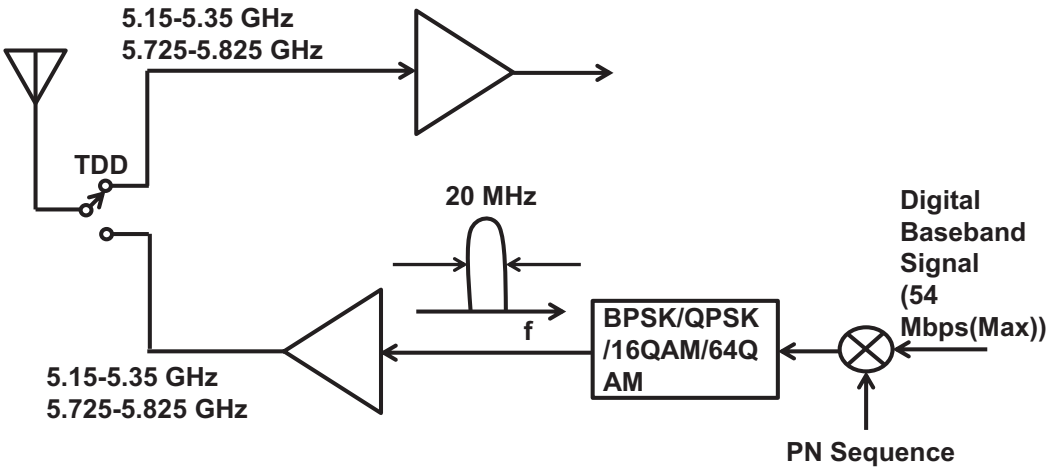

Figure A.5: IEEE 802.11a air interface.

subcarriers with a spacing of 0.3125 MHz. The middle subchannel and the first and the last five are unused. Four of the subcarrier are occupied by BPSK modulated "pilot" to simplify the detection in the receiver in the presence of frequency offsets and phase noise. Each OFDM symbol is 4 μs long.

Advanced wireless standards such as IEEE 802.11ad are intended for 60 GHz communication and can be referred from [115].

Appendix B: Phase Noise Fundamentals & Models

Phase Noise Basics An ideal oscillator produces a perfectly-periodic output of the form x(t) = Acos(ω_ct). The zero crossings occur at exact integer multiples of $T_c = 2\pi/\omega_c$. However, in reality the noise of the oscillator devices randomly creates perturbation in the zero crossings. The perturbation is modeled by x(t) = Acos(ω_ct + ϕ_nt), where ϕ_nt is a small random phase quantity that deviates the zero crossings from integer multiples of T_c. The term ϕ_nt is called "phase noise". This is illustrated in Fig. B.1a.

As can also be seen the frequency of the ideal wave remains constant, whereas the frequency varies randomly for the perturbed oscillator. This observation leads to the frequency response of the oscillator. The ideal wave consists of a single impulse at the operating frequency, ω_c, whereas for the perturbed oscillator the frequency experiences random variations, the consequence of which is a broadened spectrum. These are shown in Fig. B.1b. It can be noted, that the focus on noise on oscillator is on zero crossings rather than noise on amplitude which can be removed by hard switching in stages following the oscillator.

The phase noise falls at frequencies farther from the carrier, ω_c, hence it is quantified by a frequency offset from ω_c. As shown in Fig. B.1c, 1 Hz bandwidth of the spectrum at an offset of Δf is considered, the power of is measured in this bandwidth and the result is normalized to the carrier power. The carrier power can viewed as the peak of the spectrum given by $A^2/2$. The unit of phase noise is dBc/Hz, which means dB with respect to the carrier, and signifies normalization of the noise power to the carrier power. The importance of phase noise can be analysed from Fig. B.1d.

Leeson's Model: Phase noise performance is a critical specification for VCOs. The phase noise models describe the phase noise generation mechanism in oscillators. With the help of these models, the phase noise can be estimated before the oscillators are fabricated. The models also provide the design trade-offs and insights, which are very valuable for

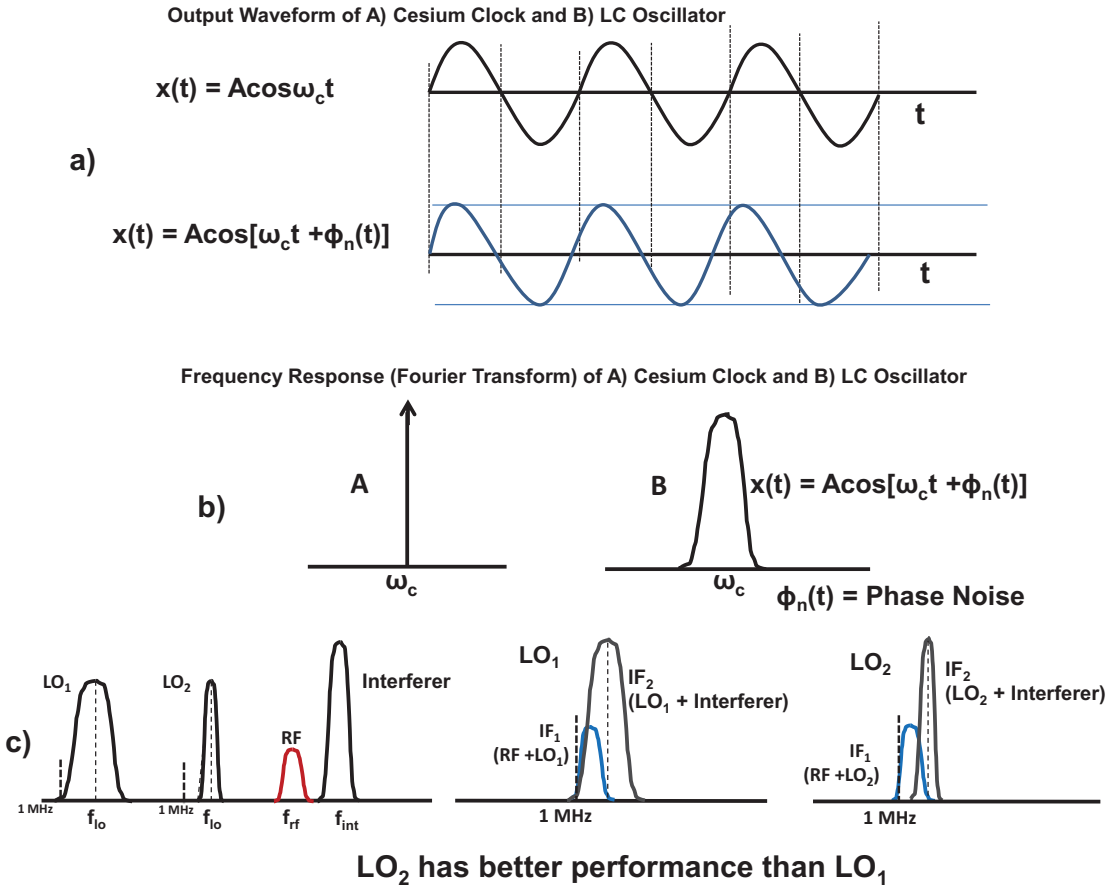

Figure B.1: a) Illustration of the definition phase noise b) Illustration of the importance of the phase noise.

circuit designers.

This model is an empirical model and is illustrated in Fig. B.2. At a small offset frequency, the phase noise decreases with the increase of the cube of the offset frequency (i.e. the slope is 30dB/dec). This is due to the contribution from the flicker noise. The slope changes to 20dB/dec above a corner-frequency, $\Delta\omega_{1/f^3}$. The phase noise plot finally becomes flat at a large offset frequency. This noise floor is determined by the active devices noise floor or the instrumentation used in measurement. The is primarily due to the effect of thermal noise. The phase noise expressed by an oscillator can be expressed as,

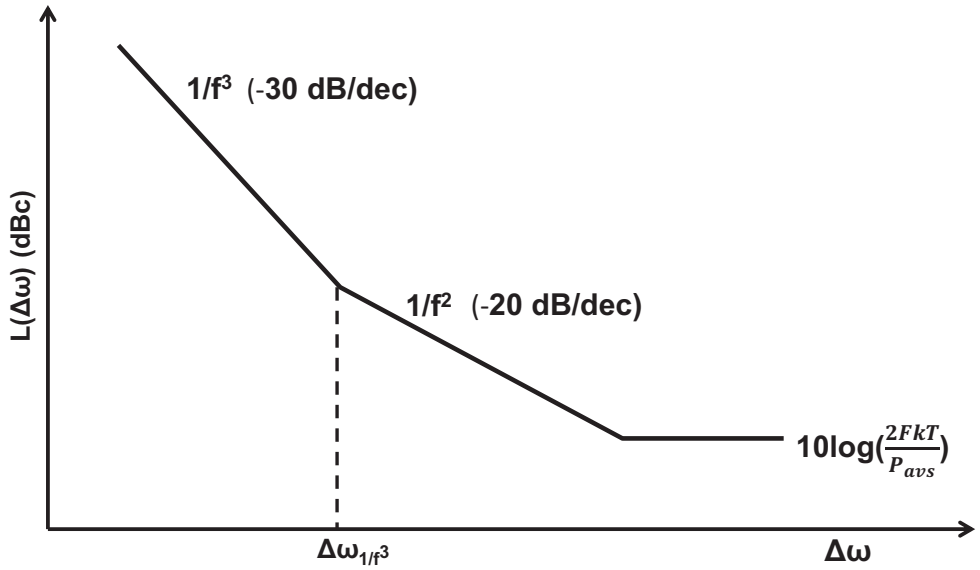

Figure B.2: Plot of the phase noise of an oscillator versus offset from carrier showing different noise regions.

$$L\Delta\omega \quad = \quad 10log\left[\frac{2FkT}{P_{avs}}\left[1+\left(\frac{\omega_0}{2Q_L\Delta\omega}\right)^2\right]\left(1+\frac{\omega_{1/f^3}}{|\Delta\omega|}\right)\right] \tag{B.1}$$

where ω_0 is the oscillation frequency, $\Delta\omega$ is the frequency offset at which the phase noise is defined, T is the absolute temperature, k is the Boltzmanns constant, P_{avs} is carrier power, Q_L is the loaded Q factor of the tank. The parameter F, is an empirical parameter which can only be found from fitting the measurement data. Also, this model asserts that the corner frequency between the $1/f^3$ and $1/f^2$ region is precisely equal to the 1/f corner frequency of the device noise. However, measurements frequently show this equality does not exist. Therefore, this parameter is usually a fitting parameter too [116].

In summary, the Leesons model cannot be used to predict the phase noise generated by an oscillator because it has two empirical parameters which have to be obtained from measurement. Also, it does not describe the mechanism of the phase noise generation and thus provides little design insight. More accurate phase models are necessary to investigate the phase noise. Although there are several models of phase noise being proposed, the most

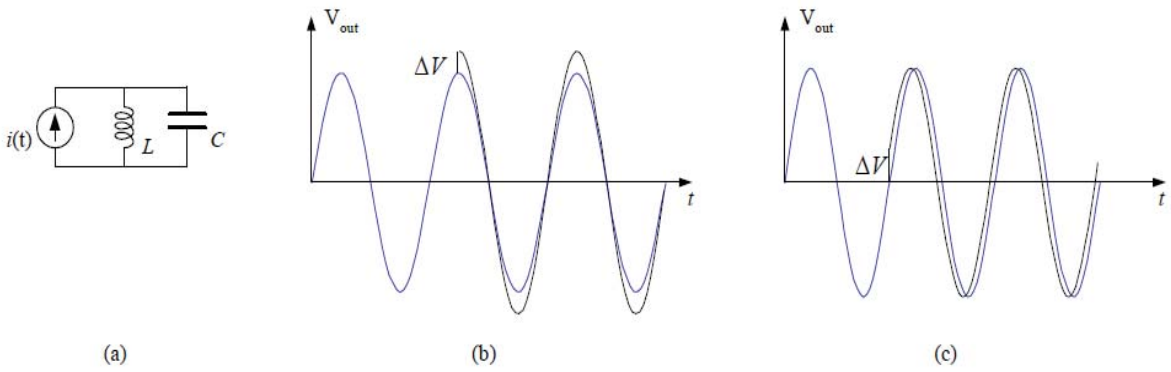

Figure B.3: Impulse injected into an ideal LC tank (a) at the peak (b) and the zero crossing (c) [20].

widely used is the Linear Time variant Hajimiri-Lee model. This is the topic of the next subsection.

Linear Time-Variant Hajimiri-Lee Model: The oscillators are essentially time variant. The voltage and current in an oscillator have to be changed periodically to produce the oscillation. Therefore, earlier models assuming the time invariant approximation was incorrect and as result this time variant model [116] gained quick acceptance. Noise near the carrier is particularly important in communication systems with narrow channel spacings. In fact, the allowable channel spacings are frequently constrained by the achievable phase noise. Unfortunately, it is not possible to predict close-in phase noise correctly with LTI models [116].

Linearity Assumption: The linearity assumption for oscillators are valid if the noise level is much smaller than the oscillation signal. The linearity in oscillator refers to the noise to phase transfer characteristics in oscillators. The practical oscillators have noise level much smaller than the signal and the linear noise to phase characteristic is valid for almost all kinds of oscillators [116].

Impulse Sensitivity Function: The same perturbation occurring at different times will result in different phase shifts due to the time-variant nature of oscillators. Supposing a perturbation charge is injected into an ideal LC tank (Fig. B.3a), the oscillation amplitude will increase ΔV if the injection occurred at the peak (Fig. B.3b). The zero crossing time is not changed in this case. In practical oscillators, this amplitude variation will disappear quickly due to their loss. So, the perturbation at the peak introduces little or no phase noise. On the contrary, if the same perturbation is injected at the zero crossing, it has no effect on the oscillation amplitude but generates a phase shift as shown in (Fig. B.3c) [116].

Therefore, noise creates amplitude modulation if injected at the peaks & only phase modulation if injected at the zero crossings. The foregoing observation suggest the need for a method of quantifying how and when each source of noise in an oscillator "hits" the output waveform. While the transistors turn on and off, a noise source may only appear near the peaks of the output voltage, contributing negligible phase noise, whereas another may hit the zero crossings, producing substantial phase noise. Thus, noise varies with time and hence becomes linear time variant [116].

The convolution property holds in a time variant system, however the impulse response varies with time and is expressed as,

$$h_\phi(t,\tau) = \frac{\Gamma(\omega_0\tau)}{q_{max}}u(t-\tau) \tag{B.2}$$

where q_{max} is the maximum charge displacement on the node, and u(t) is the unit step function. This time variant impulse response, precisely the function Γ(x) is referred to as the impulse sensitivity function (ISF) in [116]. This is a dimensionless, frequency and amplitude independent periodic function with a period of 2π which describes how much phase shift results from applying a unit impulse at t = τ. The ISF is a function of the waveform, which in turn is governed by the nonlinearity and the topology of the oscillator [116].

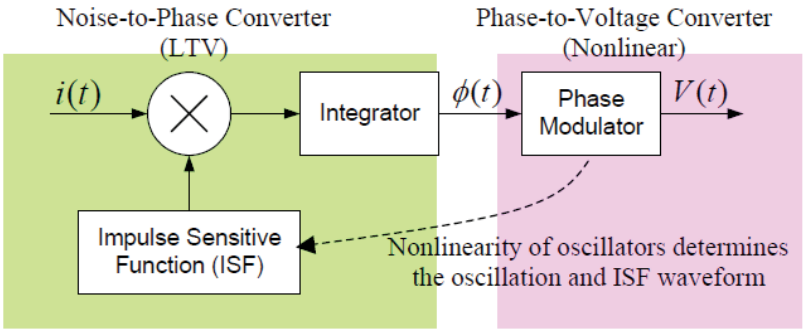

Figure B.4: Block diagram of the LTV phase noise model [20].

The output excess phase,ϕ(t), can be calculated using the superposition integral for a given ISF,

$$\phi(t) = \int_{-\infty}^{\infty} h_{\phi}(t,\tau)\, i(\tau)d\tau = \frac{1}{q_{max}} \int_{-\infty}^{t} \Gamma(\omega_0\tau)\, i(\tau)d\tau \tag{B.3}$$

where i(t) is the input noise current injected into the node. The periodic ISF can be expanded into a Fourier series,

$$\Gamma(\omega_0\tau) = \frac{c_0}{2} + \sum_{n=1}^{\infty} c_n cos(n\omega_0\tau + \theta_n) \tag{B.4}$$

Phase to Voltage Conversion: To calculate the phase noise, the power spectral density (PSD) of the oscillator output voltage needs to be computed, which requires knowledge of how the output voltage relates to the excess phase variations. As shown in Fig. B.4, the conversion of the device noise current to the output voltage is treated as the result of a cascade of two processes. The first LTV current-to-phase process discussed in ISF section earlier, while the second system is a nonlinear phase modulation (PM) system which transforms the excess phase to output voltage. A PM cosine signal can be written as [116]

$$V_{out} = V_0 cos(\omega_0 t + V_m sin\Delta\omega t) \tag{B.5}$$

This results in two extra sidebands at the frequencies of $\omega_0 \pm \Delta\omega$ (Assuming V_m is small). Mathematically, V_{out} is given as,

$$V_{out} = V_0 cos\omega_0 t - \frac{V_m V_0}{2}[cos(\omega_0 - \Delta\omega)t - cos(\omega_0 + \Delta\omega)t] \quad \text{(B.6)}$$

Therefore, for the excess phase generated by an injected current at nω0 + $\Delta\omega$, the resulting two equal sidebands at ω0 ± $\Delta\omega$ have the sideband power relative to carrier given by,

$$P_{SBC}(\Delta\omega) = \left(\frac{I_n c_n}{4q_{max}\Delta\omega}\right)^2 \quad \text{(B.7)}$$

Replacing the injected single-tone current by a noise current with a white power spectral density $\overline{i_n^2}/\Delta f$. Since, I_n represents the peak amplitude, $I_n^2/2 = \overline{i_n^2}/\Delta f$ for a unit bandwidth. Also, an injected current at nω_0 - $\Delta\omega$ will result in the same two equal sidebands. Thus, eqn. B.7 should be multiplied by a factor 2. Finally, the bandwidth of the injected white noise current is very wide, and the superposition for different n has to be applied. Based on this analysis, the output phase noise in dBc/Hz resulted by the white noise current is given by,

$$L(\Delta\omega) = 10log\left(\frac{\overline{i_n^2}/\Delta f \sum_{n=0}^{\infty} c_n^2}{4q_{max}^2\Delta\omega^2}\right) \quad \text{(B.8)}$$

It is clear from Fig. B.5 that minimizing the various coefficients (by minimizing the ISF) will minimize the phase noise. According to Parseval's relation, the summation term in (*l*) is given as,

$$\sum_{n=0}^{\infty} c_n^2 = \frac{1}{\pi}\int_0^{2\pi} |\Gamma(x)|^2 dx = 2\Gamma_{rms}^2 \quad \text{(B.9)}$$

where Γ_{rms} is the rms value of the ISF. The phase noise therefore becomes,

$$L(\Delta\omega) = 10log\left(\frac{(\overline{i_n^2}/\Delta f)\Gamma_{rms}^2}{2q_{max}^2\Delta\omega^2}\right) \quad \text{(B.10)}$$

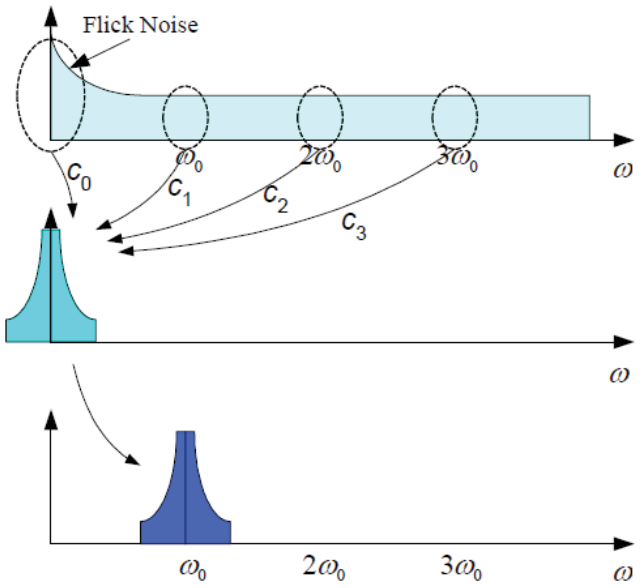

Figure B.5: Conversion of noise to phase fluctuations and phase-noise sidebands [20].

This equation represents the phase noise spectrum of an arbitrary oscillator in $1/f^2$ region of the phase noise spectrum. This LTV model is illustrated in Fig. B.5 in the frequency domain. In the first LTV system, the white noise near the frequency is folded down to the near-DC frequency according to the Fourier coefficients. In the second phase-to-power transformation procedure, the low frequency noise is upconverted to the carrier band.

Flicker Noise & Cyclostationary Noise: The relationship between the device 1/f corner and the flicker noise $1/f^3$ is derived here. Although, these two corner frequencies are usually assumed to be the same, however, measurements frequently rejects such equality. The device noise spectrum in the flicker noise dominated portion can be denoted as,

$$\overline{i_{n^2}, 1/f} = \overline{i_n^2}\frac{\omega_{1/f}}{\Delta\omega} \tag{B.11}$$

The phase noise resulting from flicker noise is thus,

$$L(\Delta\omega) = 10log\left(\frac{(\overline{i_n^2}/\Delta f)\Gamma_{rms}^2}{4q_{max}^2\Delta\omega^2}\frac{\omega_{1/f}}{\Delta\omega}\right) \tag{B.12}$$

Comparing (B.12) with (B.10), the corner frequency can be solved as,

$$\omega_{1/f^3} = \omega_{1/f} \frac{c_0^2}{2\Gamma_{rms}^2} \tag{B.13}$$

Therefore, the flicker noise, $1/f^3$, depends not only on the device $1/f$ noise, but also on the Fourier coefficients of the ISF. Since the ISF is determined by the waveform, the first coefficient, c_0 can be significantly reduced if certain symmetry properties exist in the waveform. Therefore, (B.13) suggests $1/f$ device noise need not imply poor flicker noise.

Due to the periodic nature of the oscillations, the stochastic properties of some random noise sources in oscillators may vary temporally. These sources are termed as cyclostationary noise sources [116]. The channel noise of a MOS device used in oscillators is cyclostationary because the noise power is modulated by the gate source overdrive voltage which periodically changes with time. There are other sources of noise in the circuit whose stochastic characteristics do not depend temporally and the operation point of the circuit, and are therefore called as stationary noise sources. The thermal noise of a resistor is a stationary noise source. The LTV model provides a simple way to deal with cyclostationary noise sources. A white cyclostationary noise current, i_n(t), can be decomposed by [116],

$$i_n(t) = i_{n0}(t)\alpha(\omega_0(t)) \tag{B.14}$$

where i_{n0}(t) is a white stationary noise current and $\alpha(\omega_0$(t)) is a deterministic periodic function describing the noise amplitude modulation. It has been normalized to 1 and can be derived easily from device noise characteristics and operation point. By this decomposition, an effective ISF can be expressed as [116]

$$\Gamma_{eff}(x) = \Gamma(x)\alpha(x) \tag{B.15}$$

Replacing the original ISF by this effective ISF in the previous derivation, the phase noise contributed by the cyclostationary noise sources in oscillators can be computed by (B.13) easily.

Appendix C: Refereed publications arising out of the Dissertation

Book Chapter

- **S. Laha** and S. Kaya, "**RFIC Design with Nanoscale DG MOSFETs**", Analog Circuits, ISBN: 980-953-307-694-7, INTECH, Dec 2012.

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