PROGRAMMED HARMONIC REDUCTION IN SINGLE PHASE AND THREE PHASE VOLTAGE-SOURCE INVERTERS

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TABLE OF CONTENTS

List of Figures		iii
List of Tables .		vii
Chapter One	Preview	1
1.1	Introduction	1
1.2	Harmonics	2
1.3	Pulse Width Modulation For Harmonic Elimination	3
1.4	Purpose of this Thesis	6
1.5	Organization of this Thesis	7
Chapter Two	Optimization Technique	8
2.1	Technique Description	8
2.2	Solution Method for Non-linear equations	10
2.3	Comparison with SPWM	12
2.4	Applications discussed in this Thesis	15
Chapter Thre	e Optimal Harmonic Elimination in Single Phase	
	Voltage-Source Inverters	16
3.1	Harmonic Elimination	16
3.1.1	Optimal Harmonic Elimination in the Single Phase Half	
	Bridge Voltage-Source Inverter	16
3.1.2	Optimal Harmonic Elimination in the Single Phase Full	

		Bridge Voltage-Source Inverter	18
3	.2	Experimental Results	21
Chapter	r Four	Optimal Harmonic Elimination in the Three Phase	
		Voltage-Source Inverters	32
4	.1	Harmonic Elimination	32
4	.2	Experimental Results	34
Chapter	r Five	Hardware Description	42
5	.1	Functional Description of the 48 Channel Digital I/O Board	42
5	.2	8255 Programmable Peripheral Interface (PPI)	44
	5.2.1	8255 PPI Operational Description	46
	5.2.2	8255 PPI Control Word Register	47
	5.2.3	8255 PPI Data Access	47
5	5.3	8255 PPI Programming	49
Chapter Six		Conclusions	53
6	5.1	Conclusions	53
. 6	5.2	Recommendations for Further Work	54
6	5.3	Bibliography	56
Chapter Sev		en Appendices	59
		Appendix A	60
		Appendix B	76

LIST OF FIGURES

Figure 2.1	Comparison of the WDFs for the proposed scheme and the	
	SPWM scheme applied to a 3 pulse full bridge single phase	
	voltage-source inverter	13
Figure 2.2	Comparison of the WDFs for the proposed scheme and the	
	SPWM scheme applied to a 5 pulse three phase voltage	
	voltage-source inverter	13
Figure 3.1	Circuit diagram of a single phase half bridge voltage-source	
	inverter	17
Figure 3.2	Switching functions and output voltage for the 3 pulse half	
	inverter of Fig. 3.1	17
Figure 3.3	Optimal switching pattern for the 3 pulse single phase half	
	inverter, eliminating 3rd and 5th harmonics	19
Figure 3.4	Weighted Distortion Factor for the switching pattern in Fig. 3.3	19
Figure 3.5	Circuit diagram of a single phase full-bridge voltage-source	
	inverter	20
Figure 3.6	Switching functions and output voltage for the 5 pulse full	
	bridge inverter of Fig. 3.5	20

.

Figure 3.7	Optimal switching pattern for the 5 pulse full-bridge single	
	phase inverter eliminating the 3rd, 5th, 7th and 9th harmonics	22
Figure 3.8	Weighted Distortion Factor for the switching pattern in Fig. 3.7	22
Figure 3.9	Lab circuit of single phase half bridge inverter	24
Figure 3.10	Gate driver circuit for the MOSFETs S_1 and S_2 of the circuit in	
	Fig. 3.9	25
Figure 3.11 (a)	Output voltage waveform for the single phase 3 pulse half	
	bridge inverter	26
Figure 3.11 (b)	Frequency spectrum for the output voltage waveform of	
	Fig. 3.11 (a)	26
Figure 3.12 (a)	Output voltage waveform for the single phase 5 pulse half	
	bridge inverter	27
Figure 3.12 (b)	Frequency spectrum for the output voltage waveform of	
	Fig. 3.12 (a)	27
Figure 3.13	Lab circuit of single phase full bridge inverter	28
Figure 3.14 (a)	Output voltage waveform for the single phase 3 pulse full	
	bridge inverter	29
Figure 3.14 (b)	Frequency spectrum for the output voltage waveform of	
	Fig. 3.14 (a)	29
Figure 3.15 (a)	Output voltage waveform for the single phase 5 pulse half	
	bridge inverter	30

Figure 3.15 (b)	Frequency spectrum for the output voltage waveform of	
	Fig. 3.15 (a)	30
Figure 4.1	Circuit diagram of a three phase voltage-source inverter	33
Figure 4.2	Standard line to neutral output voltage waveform for a wye	
	connected load in Fig. 4.1	33
Figure 4.3	Optimal switching pattern for the three phase 3 pulse inverter,	
	eliminating the 5th and 7th harmonics	35
Figure 4.4	Weighted Distortion Factor for the switching pattern of	
	Fig. 4.3	35
Figure 4.5	Optimal switching pattern for the three phase 5 pulse	
	inverter, eliminating the 5th, 7th, 11th and 13th harmonics.	36
Figure 4.6	Weighted Distortion Factor for the switching pattern of	
	Fig. 4.5	36
Figure 4.7	Diagram of the circuit used in the lab for the three phase	
	voltage-source inverter	38
Figure 4.8	Standard line to neutral output voltage waveform for the	
	circuit of Fig. 4.7	38
Figure 4.9 (a)	Output voltage waveform of the three phase 3 pulse	
	voltage-source inverter	39
Figure 4.9(b)	Frequency spectrum corresponding to the output voltage	
	waveform of Fig. 4.9 (a)	39

Figure 4.10 (a)	Output voltage waveform of the three phase 5 pulse	
	voltage-source inverter	40
Figure 4.10(b)	Frequency spectrum corresponding to the output voltage	
	waveform of Fig. 4.10 (a)	40
Figure 5.1	Block diagram of the 48 channel Digital I/O Board	43
Figure 5.2	8255 PPI Block Diagram	45
Figure 5.3	8255 PPI Control Word Bit Functions	48
Figure 7.B.1	Connector Pin Assignments	78

LIST OF TABLES

Table 3.1 (a)	Switching angles for the 3 pulse single phase half bridge	
	inverter	31
Table 3.1 (b)	Comparison of theoretical and experimental values for the	
	switching pattern in (a)	31
Table 3.2 (a)	Switching angles for the 5 pulse single phase full bridge	
	inverter	31
Table 3.2 (b)	Comparison of theoretical and experimental values for the	
	switching pattern in (a)	31
Table 4.1(a)	Switching angles for the three pulse case	41
Table 4.1 (b)	Comparison of theoretical and experimental values	41
Table 4.2 (a)	Switching angles for the five pulse case	41
Table 4.2 (b)	Comparison of theoretical and experimental values	41

Chapter One

Preview

1.1 Introduction

In an industrialized nation today, an increasingly significant portion of the generated electrical energy is processed through power electronics for various applications in industrial, commercial, residential, aerospace and military environments [1]. The technological advances made in the field of power semiconductor devices over the last two decades, have led to the development of power semiconductor devices with high power ratings and very good switching performances. Also, the development of microprocessors and microcomputer technology has had a great impact on the control strategy for the power semiconductor devices [2]. Some of the popular power semiconductor devices available in the market today include Power MOS Field Effect Transistors (Power MOSFETs), Insulated Gate Bipolar Transistors (IGBTs) and Gate Turn Off Thyristors (GTOs) [3]. As a result of these rapid advancements in power semiconductor technology, substantial amount of research is being devoted to the area of static power converters. The input and output currents and voltages of static power converters are generally associated with harmful low-order harmonics. This thesis

inverstigates an optimal strategy for harmonic reduction in the dc/ac converters (Inverters).

1.2 Harmonics

Harmonics are undesirable currents and/ or voltages. They exist at some multiple or fraction of the fundamental frequency. Harmonic pollution in static power converters is a serious problem. For example in many residential, commercial and office buildings the triplen harmonics create high neutral currents to the extent that they may start fires, although the fundamental neutral current is within allowable limits [4]. The harmonics can arise in three ways [5]:

- (a) Through the application of a nonsinusoidal driving voltage to a circuit containing nonlinear impedance.
- (b) Through the application of a sinusoidal driving voltage to a circuit containing nonlinear impedance.
- (c) Through the application of a nonsinusoidal driving voltage to a circuit containing linear impedance.

The harmonic orders and magnitudes depend on the converter type and the method of control. For example in single-phase voltage-source inverters, the output voltage waveform typically consists only of odd harmonics. The even harmonics are absent due to the half wave symmetry of the output voltage harmonics. In three phase voltage-source inverters, in addition to the even harmonics, the triplen (third and

multiples of third harmonics) are also absent. The harmonic spectra depend on the switching frequency and the control method [6...8].

1.3 Pulse Width Modulation for Harmonic Elimination

Pulse Width Modulation (PWM) techniques are extensively used for eliminating harmful low-order harmonics in input and output voltage and current of static power converter [2, 9]. PWM does not reduce the total distortion factor of the current or the voltage, but the non-zero harmonics are of high order. This results in low design values for the inductor and capacitor components of the output filter and hence an overall reduction in the filter size. In PWM control, the converter switches are turned on and off several times during a half cycle and the output voltage is controlled by varying the pulse widths. In this section, the discussion is mainly focused on the application of PWM techniques for harmonic elimination in voltage-source inverters, as this is relevant to the thesis.

The performance characteristics of an inverter power conversion scheme largely depend on the choice of the particular PWM strategy employed. Present-day available PWM schemes can be broadly classified as carrier-modulated Sinusoidal Pulse Width Modulation (SPWM) and pre-calculated programmed PWM schemes [8]. In SPWM a triangular waveform of certain amplitude and frequency is compared to a sinusoidal waveform in phase with the output voltage of the inverter [2, 9]. The widths of the pulses are varied by changing the amplitude of the sinusoidal waveform. In this method the lower order harmonics are eliminated. As the switching frequency increases, more harmonics can be eliminated. The limiting factors are the switching device speed, switching loss and the power ratings.

Programmed PWM techniques optimize a particular objective function such as minimizing losses [10], reducing torque pulsations [11], selective elimination of harmonics [6], etc. Hence, this flexibility offered by the programmed PWM techniques offers a more effective means of obtaining high performance results. Generally, the objective functions chosen to optimize are such that the unwanted effects due to the harmonics present in the inverter output spectra are minimized. The programmed PWM techniques are generally associated with the difficult task of computing specific PWM switching instants such as to optimize a particular objective function [11]. This difficulty is particularly encountered at lower-output frequency range, where there is a need for a large number of PWM switching instants. Despite these difficulties, programmed PWM techniques exhibit several distinct advantages in comparison to the conventional carrier-modulated PWM schemes, as listed below [8]:

(a) About 50% reduction in the inverter switching frequency is achieved when comparing with the conventional carrier modulated SPWM scheme.

(b) Higher voltage gain due to overmodulation is possible. This contributes to higher utilization of the power conversion process.

(c) The reduction in switching frequency contributes to the reduction in switching losses of the inverter and permits the use of gate-turn-off (GTO) switches for high power inverters.

(d) Elimination of lower-order harmonics results in reduced harmonic
interference such as resonance with external lines in networks typically employed
in inverter power supplies.

(e) The use of precalculated optimized programmed PWM switching patterns avoids on-line computations and provides straightforward implementation of a high performance technique.

With the present-day enhancement in computing power and calculating procedures, the nonlinear equations associated with selective elimination of harmonics can be solved for small and large degrees of freedom [12]. Also with the availability of inexpensive large memory components, this approach is now feasible for power control applications over a wide frequency range [13]. In view of this, programmed PWM techniques with the choice of eliminating several lower-order harmonics of any degree in the inverter output spectra have emerged as an important and viable means of power control. This thesis is basically a study in the effectiveness of programmed PWM applied to the voltage-source inverters

It should be mentioned here again that unlike SPWM which is typically a "real time" control technique, the programmed PWM technique is not a "real time" control technique. In other words, the switching patterns are not computed and implemented on-

line, but are precalculated using optimization programs. A microprocessor is required for converting the precalculated switching instants into gating signals for the relevant inverter switches.

1.4 Purpose of this Thesis

Before discussing the purpose of this thesis, a brief history of the research in the area of programmed PWM at the Power Electronics Research facility of Ohio University, Athens, is given. The ongoing research at the Power Electronics Research facility is primarily in the area of optimal PWM techniques for harmonic reduction in various power electronic circuits [14....16]. Initially, the theory for a general optimal PWM scheme for harmonic reduction in various power electronic circuits was developed [17]. Then the optimal PWM scheme was applied to a single-phase current source ac/dc converter and successfully tested on the bench. This thesis contributes to this ongoing research by thoroughly exploring the application of the optimal PWM technique to a different type of static power converter - The voltage-source dc/ ac converter (inverter).

The purpose of this thesis is to investigate and successfully implement the optimal firing strategy for harmonic elimination in single-phase and three-phase voltage-source inverters. Optimization programs are developed to generate optimal switching patterns for the single-phase and three-phase inverter configurations. Next, a control scheme for implementing the firing strategies is developed. The hardware for realizing the control scheme included a 48 channel Input/ Output board mounted on a computer. The circuits

for the single-phase inverter configuration (single-phase half-bridge and single-phase fullbridge) and the circuit for three phase inverters are individually built on the bench and their corresponding firing strategies are implemented through the control scheme. Experimental results obtained are verified with the design values obtained from the optimization programs to ensure effective harmonic elimination and high-quality output spectra.

1.5 Organization of this Thesis

This thesis is organized into seven chapters. Chapter One provides a general introduction and the purpose of this thesis. Chapter Two describes the optimization technique used for optimal harmonic elimination in the voltage-source inverters. Chapter Three discusses the optimal PWM scheme applied to single phase inverters, including the experimental results. Chapter Four discusses the optimal PWM scheme applied to three phase inverters, including the experimental results. Chapter Four discusses the optimal PWM scheme applied to three phase inverters, including the experimental results. Chapter Five describes the hardware used for developing the control scheme needed to implement the optimal switching strategy. Chapter Six contains conclusions, recommendations for further work and the bibliography for this thesis. The appendices for this thesis is given in Chapter Seven.

Chapter Two

Optimization Technique

2.1 Technique Description

This thesis proposes an optimal harmonic elimination strategy for harmonic reduction in the output spectra of voltage-source inverters. Switching patterns for the inverter switches are developed to optimize a particular objective function such as to obtain selective elimination of harmonics.

Harmonic elimination schemes for the voltage-source inverters are generally judged by factors called quality factors, which accurately describe the extent to which the unwanted effects of the harmonics in the output spectra are minimized. In this thesis the first order weighted harmonic distortion factor (WDF), is the quality factor chosen as the objective function to minimize. Most of the PWM inverter circuits employ a filter circuit between the inverter and the load, to filter out the higher order harmonics that have not been eliminated [18, 19]. A first order low-pass filter provides harmonic attenuation which is proportional to the order (n) of the harmonic. A first order weighted distortion factor represents the total harmonic content at the output of a first order filter. The weighting factor in the WDF for the nth harmonic is 1/n. Hence the weighted distortion factor can be defined as

$$WDF = \frac{100}{V_{L_1}} \sqrt{\sum_{n=m}^{n=M} \left[\frac{V_n}{n}\right]^2}$$
(2.1)

where

- V_{L_1} is the fundamental output voltage (rms)
- V_n is the harmonic voltage (rms)
- m is the minimum-order harmonic
- M is the maximum-order harmonic

The output voltage waveforms of both the single phase and three phase inverter configurations discussed in this thesis are half-wave symmetric. This implies that the even harmonics are absent. Hence for single-phase inverters, the minimum order harmonic (m) is equal to 3. In three phase inverters, typically both the even and triplen (third and multiples of third) harmonics are absent. Hence for three phase inverters m is equal to 5. The maximum-order harmonic to be considered (M) is chosen to be 23 for both the single phase and three phase inverters. Harmonics higher than the order of 23 can be safely ignored since they would have attained negligible values due to attenuation by the first order filter. In this thesis the emphasis is on eliminating the lower order harmonics. This is because the lower order harmonics are more difficult and more expensive to filter.

After identifying the objective function (2.1), the proposed approach is to minimize (2.1) using numerical techniques, such as to obtain selective elimination of harmonics.

Section 2.2 gives more details on this approach.

2.2 Solution Method for Nonlinear Equations

The equations for the harmonic output voltages can be derived directly from the equation for the Fourier coefficients of the switching function for the relevant inverter circuit. The equation for the Fourier coefficients is described in more detail in Chapter 3 (equations 3.1 and 3.2). It is to be noted here that these equations are nonlinear and multiple solutions are possible. The solution for these equations generates the switching pattern for the relevant inverter circuit.

The objective function (2.1) subject to the constraints in (2.2) to (2.4) is minimized using the subroutine CONSTR from the Optimization Tool Box in MatlabTM [14]. The constraints that are imposed on the solution are

$$0 \leq \alpha_1 \leq \alpha_2 \quad \dots \leq \alpha_N \leq \frac{\pi}{2} \tag{2.2}$$

$$V_{ll} \leq V_L \leq V_{ul} \tag{2.3}$$

$$\sqrt{\sum V_{L_n}^2} \leq \varepsilon \tag{2.4}$$

where

 $\alpha, \alpha_2, \dots, \alpha_N$ are the switching angles per quarter cycle

- V_{μ} is the lower limit for the fundamental output voltage
- V_{ul} is the upper limit for the fundamental output voltage
- V_L is the desired rms fundamental output voltage
- V_L is the rms nth harmonic output voltage
- ε is a very small value, nearly equal to zero

Equation (2.2) ensures that the solution is physically realizable. The constraints $0 \leq \alpha_1$ and $\alpha_N \leq \frac{\pi}{2}$ (N is the number of pulses per half cycle) constrain the circuits to pure inverter operation. In this thesis, the switching functions for both the single phase and three phase inverter configurations are quarter wave symmetric. Hence only the first ninety degree interval (per half cycle) of the switching function needs to be determined. The constraint (2.3) forces the fundamental output voltage to be between upper and lower limits typically on the order of 0.00005 per unit (on a base value of V_L). This ensures that the switching angles obtained by solving the nonlinear equations correspond to the desired fundamental output voltage. The constraint (2.4) is used to eliminate up to N - 1 harmonics. ε was chosen to be $4 \ge 10^{-5}$ per-unit.

It is essential that good initial guess values for the switching angles are provided in the optimization program. Reasonable initial guess values would be the values obtained for the carrier-modulated SPWM method. The optimization programs are written in MATLABTM and run on a Sun SPARC 20 workstation.

2.3 Comparison with SPWM

The carrier-modulated SPWM control method for harmonic elimination is widely used in the power electronics industry. In this section, the proposed optimal PWM method is compared with the SPWM method and the superiority of the proposed method over the SPWM method is established. This is done by comparing the variation of the first order weighted distortion factor (WDF) with the per unit fundamental output voltage for the SPWM scheme and the proposed scheme, applied to both the single phase and three phase inverter configurations. In order that the comparison be valid, the two techniques are compared for the same number of pulses per half cycle and same frequency of the output. In other words, the two techniques are compared for the same switching frequency (Switching frequency of the inverter switches).

Fig. 2.1 compares the variation of the WDF with the per unit (pu) fundamental output voltage for the SPWM scheme and the proposed scheme applied to a 3 pulse single phase full bridge voltage-source inverter. It can be seen from this figure that for a particular value of per unit fundamental output voltage, the values of WDF for the SPWM scheme and the proposed scheme are almost equal. This is because, in single phase inverters it is mandatory to eliminate the triplen harmonics along with the other odd harmonics, to generate a high quality output. Hence for the same switching frequency, the quality of the output for a single phase inverter with SPWM control is almost equal to that obtained by applying the proposed scheme. Thus the proposed optimal PWM scheme does not have any significant advantage over the SPWM scheme



Fig. 2.1 Comparison of the WDFs for the proposed scheme and the SPWM scheme applied to a 3 pulse full bridge single phase voltage-source inverter. (a) - proposed scheme and (b) - SPWM scheme



Fig. 2.2 Comparison of the WDFs for the proposed scheme and the SPWM scheme applied to a 5 pulse three phase voltage-source inverter. (a) - proposed scheme and (b) - SPWM scheme

in single phase inverters, as far as the quality of the inverter output spectra is concerned. It must be noted here that typically the SPWM scheme has a high quality output spectra for switching frequencies greater than 1000 Hertz. Hence for single phase inverter applications involving low switching frequencies, the proposed scheme may prove to be a better choice. But the proposed optimal PWM scheme performs much better than the SPWM scheme when applied to a three phase inverter. Fig. 2.2 compares the variation of WDF with pu fundamental output voltage for the SPWM scheme and the proposed scheme applied to a 5 pulse three phase voltage-source inverter (for example). It can be seen from this figure that for a particular per unit fundamental output voltage the WDF for the proposed scheme is significantly lower than the WDF for the SPWM scheme. The reason for this is that the SPWM method eliminates the harmonics in a sequence, starting from the lowest order harmonic, including triplens, for the given switching frequency. Hence for 5 pulses per half cycle the SPWM method eliminates the 3rd, 5th, 7th and the 9th harmonics. But as mentioned earlier in this chapter, the triplen harmonics are typically absent in the output of a 3 phase inverter. In the proposed scheme, since there exists the flexibility to eliminate harmonics selectively, only the non-triplen harmonics can be chosen as the harmonics to eliminate. Hence for 5 pulses per half cycle the proposed scheme can be used to eliminate the 5th, 7th, 11th and 13th harmonics. Hence for the same switching frequency, the order of the dominant harmonic at the output of the 3 phase inverter for the proposed scheme (17th harmonic) is higher than that for the SPWM scheme (11th harmonic). For a large number of pulses per half cycle, the order of the dominant harmonic for the proposed scheme will be much higher than that for the SPWM scheme and hence this contributes to a lower WDF and a much better quality of output spectra for the proposed scheme as compared to the SPWM scheme.

2.4 Applications discussed in this thesis

The proposed optimal PWM method can be used in many applications. The following applications are demonstrated in chapter three and chapter four.

- 1. *Single phase voltage-source inverters*. The proposed scheme is applied to both the half bridge and full bridge inverters. In both the cases it is shown that the output voltage harmonics can be effectively eliminated, resulting in low harmonic distortion in the inverter output. The proposed scheme was applied to these inverters for two different switching patterns 3 pulses and 5 pulses per half cycle.
- 2. Three phase voltage-source inverter. The proposed scheme is applied to three phase voltage source inverters for both 3 pulses and 5 pulses per half cycle. In this case also it is shown that the output voltage harmonics can be comprehensively eliminated, resulting in very low harmonic distortion. The flexibility offered by the proposed scheme in eliminating harmonics of choice is exploited to eliminate non-triplen harmonics only (since the output spectrum of three phase inverter does not contain triplen harmonics), and hence ensure a very high quality output.

Chapter Three

Optimal Harmonic Elimination in Single Phase Voltage-Source Inverters

Voltage-source inverters have several industrial applications. Applications include uninterruptible power supplies, standby power supplies, induction heating and variable ac motor drives. The input to the inverter may be a battery, fuel cell, solar cell or other dc source.

3.1 Harmonic Elimination

3.1.1 Optimal Harmonic Elimination in the Single Phase Half Bridge Voltage Source Inverter

Fig. 3.1 shows the circuit diagram of a single phase half bridge voltage-source inverter. Two MOSFETs are required for this configuration. Fig 3.2 shows the output voltage waveform and the quarter-wave symmetric switching function for the MOSFETs (S_1, S_2) for a 3 pulse half bridge single phase inverter. The Fourier coefficients of the switching function are given by



Fig. 3.1 Circuit diagram of a Single Phase Half-Bridge Voltage-Source Inverter, where G1 and G2 are the gating signals for switches S_1 and S_2



Fig. 3.2 Switching functions and output voltage for the 3-pulse half bridge inverter of Fig. 3.1

$$a_{n} = \frac{4}{n\pi} \left[\sum_{i=1}^{N} (-1)^{i+1} \cos(n\alpha_{i}) \right]$$
(3.1)

$$b_n = 0 \tag{3.2}$$

where N is the number of pulses per half cycle.

Equation (3.1) has N variables $(\alpha_1 to \alpha_N)$ and a set of solutions for the switching angles is obtained by equating N - 1 harmonics to zero and assigning a specific value to the amplitude of the fundamental. The N - 1 harmonics are eliminated such that the weighted distortion factor in the output voltage is minimized. Since the switching function is quarter wave symmetric, only the first ninety degree interval (per half cycle) of the switching function is needed to be determined by the solution the nonlinear equations. Fig. 3.3 shows the solution trajectories for N=3. Fig 3.4 shows the variation of the weighted distortion factor with the per unit fundamental output voltage.

3.1.2 Optimal Harmonic Elimination in the Single Phase Full Bridge Voltage -Source Inverter

The full bridge inverter is similar to the half bridge inverter as far as the quality of the output voltage and the reverse blocking voltage of each MOSFET is concerned. However, for the same dc input voltage, the output power of a full bridge inverter is four times higher and the fundamental component is twice that of the half bridge inverter.

Fig. 3.5 shows the circuit diagram of a single phase full bridge voltage-source inverter. Four MOSFETs are required for this configuration. Fig. 3.6 shows the output



Fig. 3.3. Optimal switching pattern for the 3-pulse single phase half bridge inverter, eliminating 3rd & 5th harmonics



Fig. 3.4 Weighted Distortion Factor for the switching pattern in Fig. 3.3



Fig. 3.5 Circuit diagram of a Single Phase Full-bridge Voltage-Source Inverter where G1, G2, G3 and G4 are the gating signals for the switches S_1 , S_2 , S_3 and S_4



Fig. 3.6 Switching functions and output voltage for 5- pulse full bridge inverter of Fig. 3.5

voltage waveform and the quarter wave symmetric switching function of the $MOSFETs(S_1, S_2, S_2, S_4)$ for a 5 pulse full bridge single phase inverter. The Fourier coefficients of this switching function are same as equation (3.1). Fig. 3.7 illustrates the solution trajectories for N = 5 (5 pulses per half cycle). As in case of the half bridge inverter, the solutions for the switching angles are obtained such that the distortion factor in the output voltage is minimized. Fig. 3.8 shows the variation of the weighted distortion factor with the per unit fundamental output voltage.

3.2 Experimental Results

This section contains selected results, verified experimentally on the laboratory configurations of the single phase half bridge and full bridge inverters. The inverter switches used for both the configurations were power MOSFETs. Fig 3.9 shows the circuit used in the Lab for a single phase half bridge inverter. Fig. 3.10 shows the gate drive circuit for MOSFETs S₁ and S₂ in the circuit of Fig. 3.9. The two diode bridge rectifiers (D₁ - D₄ and D₅ - D₈) rectify the sinusoidal supply input. Voltage regulators (T₁ and T₂) and capacitors (C1, C2, C3 and C4) regulate and filter the rectified dc outputs. This output along with the signal from the relevant output line of the 8255 Programmable Peripheral Interface (PPI) is fed to the optocouplers (X₁ and X₂). The optocouplers provide isolation between the 8255 PPI and the power MOSFETs. Fig. 3.11 shows the



Fig. 3.7 Optimal switching pattern for the 5-pulse full bridge single phase inverter eliminating the 3rd, 5th,

7th & 9th harmonics



Fig. 3.8 Weighted Distortion Factor for the switching pattern in Fig. 3.7

output voltage waveform for 3 pulses per half cycle for the circuit in Fig. 3.9, and its corresponding frequency spectrum. Fig. 3.13 shows the output voltage waveform for 5 pulses per half cycle for the same circuit (Fig. 3.11) and its corresponding frequency spectrum. The optimal switching angles for the inverter switches in Fig. 3.11 (for both the 3 pulse and 5 pulse cases) were calculated such that the per unit fundamental output voltage is 0.7 pu. Table 3.1 (a) gives the optimization program solution values for the switching angles of a 3-pulse half bridge inverter. Table 3.1 (b) compares the calculated normalized harmonic output voltage values (including the first significant harmonic) with the experimental values obtained from the frequency spectrum, for 3-pulses/ half cycle.

Fig. 3.14 shows the circuit used in the Lab for a single phase full bridge inverter. The gate drive circuit for the MOSFETs in each of the two legs of the circuit in Fig. 3.14 is similar to the circuit in Fig. 3.12. Fig. 3.15 shows the output voltage waveform for 3 pulses per half cycle for the circuit in Fig. 3.14 and its corresponding frequency spectrum. Fig. 3.16 shows the output voltage waveform for 5 pulses per half cycle for the same circuit and its corresponding frequency spectrum. The optimal switching angles for the inverter switches in Fig. 3.14 (for both the 3 pulse and 5 pulse cases) were calculated such that the per unit fundamental output voltage is 0.7 pu. Tables 3.2 (a) and 3.2 (b) are similar to 3.1 (a) and 3.2 (b) and they show the results for a 5 pulse full-bridge inverter. Chapter five provides a more detailed hardware description.



Fig. 3.9 Lab circuit of the single phase half-bridge inverter, where P_{A1} and P_{A2} are the gating signals for S_1 and S_2 , obtained from the gate driver circuit.



Fig. 3.10 Gate driver circuit for the MOSFETs $S_1\,$ and $S_2\,$ of the circuit in Fig. 3.9



Fig. 3.11 (a) Output voltage waveform for the single phase 3 pulse half bridge inverter



Fig. 3.11 (b) Frequency spectrum for the output voltage waveform of Fig. 3.11(a)



Fig. 3.12 (a) Output voltage waveform for the single phase 5 pulse half bridge inverter



Fig. 3.12 (b) Frequency spectrum for the output voltage waveform of Fig. 3.12 (a)


Fig. 3.13 Lab circuit of the single phase full-bridge inverter where P_{A4} , P_{A0} , P_{A6} and P_{A2} are the gating signals for S_1 , S_2 , S_3 and S_4 , obtained from the gate driver circuits.



Fig. 3.14 (a) Output voltage waveform for the single phase 3 pulse full bridge inverter



Fig. 3.14 (b) Frequency spectrum for the output voltage waveform of Fig. 3.14 (a)



Fig. 3.15 (a) Output voltage waveform for the single phase 5 pulse full bridge inverter



Fig. 3.15 (b) Frequency spectrum for the output voltage waveform of Fig. 3.15 (a)

Firing angles	α1	α2	α3	α4	α5	α6
Magnitude (Degrees)	26.89	48.46	56.71	123.29	131.54	153.11

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Harmonic Order	1	3	5	7
Theoretical Value	1.0	0.0	0.0	0.2068
Experimental Value	1.0	0.00037	0.0186	0.1998

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Table 3.1 (a) Switching angles for the 3 pulse single phase half bridge inverter, and (b) comparison of theoretical and experimental values for the switching pattern in (a)

Firing Angles	α ₁	α2	α3	α4	α5
Magnitude (degrees)	20.45	31.33	41.70	62.15	65.07
Firing Angles	α ₆	α ₇	α8	α,	α ₁₀
Magnitude (degrees)	114.9	117.8	138.3	148.7	159.5

(a)

Harmonic Order	1	3	5	7	9	11
Theoretical value	1	0.0	0.0	0.0	0.0	0.1909
Experimental value	1.0	0.0042	0.0082	0.0086	0.0160	0.177

(b)

Table 3.2 (a) Switching angles for the 5 pulse single phase full bridge inverter, and (b) comparison of theoretical and experimental values for the switching pattern in (a)

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Chapter Four

Optimal Harmonic Elimination in the Three Phase Voltage-Source Inverters

Three phase inverters are generally used for high power applications. Applications include HVDC transmission systems, Static VAR generation for supplying reactive power to an ac bus and speed control of three phase induction motors. A distinct feature of the three-phase inverter output voltage is the absence of triplen harmonics.

4.1 Harmonic Elimination

Fig. 4.1 shows the circuit diagram of a three phase voltage-source inverter. Six MOSFETs ($S_1 - S_6$) are required for this configuration. The load may be connected in wye or delta. If each MOSFET is allowed to conduct for 180 degrees, a typical line to neutral output voltage (V_L) waveform for a wye connected load is as shown in Fig. 4.2. Fig. 4.3 illustrates the optimal switching pattern to eliminate 2 non-triplen harmonics namely the fifth and seventh harmonics, in the line to neutral output voltage V_L . All triplen harmonics are absent in V_L due to a 120-degree rotation for a balanced three phase operation.



Fig. 4.1 Circuit diagram of a Three Phase Voltage-Source Inverter



Fig. 4.2 Standard line to neutral output voltage waveform for a wye connected load in Fig. 4.1

The Fourier coefficients for the quarter-wave symmetric line-to-neutral switching function for the three phase inverter configuration, is same as that for the single phase inverters (Equation 3.1, chapter 3). As in case of the single phase inverters, the optimal switching angles are obtained such that the weighted distortion factor (WDF) in the output voltage is minimized. Fig. 4.4 shows the variation of the WDF for the switching pattern in Fig. 4.3. Fig. 4.5 shows the optimal switching pattern to eliminate 4 non-triplen harmonics namely the fifth, seventh, eleventh and thirteenth harmonics, in the line to neutral output voltage V_L . Fig. 4.6 shows the variation of the corresponding WDF with per-unit fundamental output voltage.

It should be noted here that for the same per-unit fundamental output voltage the WDF for the 3 pulse and 5 pulse three phase inverter configurations is distinctly lower than the WDF for the corresponding single phase inverter configurations. This is because of the improved quality of the three phase inverter output voltage, due to the absence of triplen harmonics.

4.2 Experimental Results

This section contains selected results, verified experimentally on the laboratory configuration of the three phase voltage-source inverter. The inverter switches used were Power MOSFETs. The three-phase load was resistive in nature and wye connected. Fig. 4.7 shows the circuit used in the lab for a three-phase inverter. The



Fig. 4.3 Optimal switching pattern for the three phase 3 pulse inverter, eliminating the 5th and 7th harmonics



Fig. 4.4 Weighted distortion factor for the switching pattern of Fig. 4.3



Fig. 4.5 Optimal switching pattern for the three phase 5 pulse inverter, eliminating the 5th, 7th, 11th and 13th harmonics



Fig. 4.6 Weighted distortion factor for the switching pattern of Fig. 4.5

gate drive circuit for the two MOSFETs on each of the three inverter legs is same as the circuit used for the single phase inverter configurations (Fig. 3.10, Chapter 3). Fig. 4.8 shows the standard line-to-neutral output-voltage waveform of the three-phase voltage-source inverter (without applying any harmonic elimination techniques). Fig. 4.9 (a) shows the line to neutral output voltage waveform for 3 pulses per half cycle. Fig. 4.9 (b) shows the frequency spectrum for the output voltage waveform of Fig. 4.9 (a). Fig. 4.10 (a) shows the line to neutral output voltage waveform for 5 pulses per half cycle. Fig. 4.10 (b) shows the corresponding frequency spectrum. The optimal switching angles for the MOSFETs (for both the 3-pulse and 5-pulse cases) were calculated such that the per-unit fundamental output voltage is 0.82 pu (an arbitrary value). Also, it should be noted that both the frequency spectra (Fig. 4.9 (b) and Fig. 4.10 (b)) show the harmonic values normalized with respect to the fundamental. Table 4.1 (a) gives the optimization program's solution values for a 3-pulse three phase inverter. Table 4.1 (b) compares the calculated normalized harmonic output voltage values (up to the first significant harmonic) with the experimental values obtained from the frequency spectrum, for the 3-pulse case. Table 4.2 does the same for the 5pulse case.

As mentioned in Chapter 3, a detailed description of the hardware used in translating the precaculated PWM switching instants into gating signals is provided in Chapter 5 of this thesis.



Fig. 4.7 Diagram of the circuit used in the lab for the three phase voltage source inverter



Fig. 4.8 Standard line to neutral output voltage waveform for the circuit of Fig. 4.7



Fig. 4.9 (a) Line-to-neutral output voltage waveform of the three-phase 3 pulse voltage-source inverter



Fig. 4.9 (b) Frequency spectrum corresponding to the output voltage waveform of Fig. 4.9(a)



Fig. 4.10 (a) Line-to-neutral output voltage waveform of the three phase 5 pulse voltage-source

inverter



Fig. 4.10 (b) Frequency spectrum corresponding to the output voltage waveform of Fig. 4.10(a)

Firing angles	α ₁	α2	α3	α4	α5	α ₆			
Magnitude (Degrees)	14.66	25.77	31.23	148.77	154.23	165.34			
(a)									

Harmonic Order	1	3	5	7	9	11		
Theoretical Value	1.0	0.0	0.0	0.0	0.0	0.022		
Experimental Value	1.0	0.0018	0.0005	0.0007	0.0018	0.027		
(b)								

Table 4.1 (a) Switching angles for the 3 pulse case and (b) comparison of theoretical and experimental

values

Firing Angles	α ₁	α ₂ .	α3	α4	α,
Magnitude (degrees)	12.84	20.15	26.52	39.19	40.99
Firing Angles	α ₆	α,	α ₈	α,	α ₁₀
Magnitude (degrees)	139.01	140.81	153.48	159.85	167.16

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l	a	J

Harmonic Order	1	3	5	7	9		
Theoretical value	1	0.0	0.0	0.0	0.0		
Experimental value	1.0	0.0016	0.001	0.0004	0.0004		
Harmonic Order	11	13	15	17	19		
Theoretical value	0.0	0.0	0.0	0.0922	0.1479		
Experimental value	0.0006	0.0004	0.0005	0.0292	0.0292		
(b)							

Table 4.2 (a) Switching angles for the 5 pulse case and (b) comparison of theoretical and experimental

values

Chapter Five

Hardware Description

In this chapter, the hardware used to translate the precalculated switching instants $(\alpha_1 \text{ to } \alpha_N)$ into gating signals for the respective inverter switches is described. First a brief functional description of the 48 Channel I/O Board [20] (used as a controlling device between the computer and the gate drive circuits for the inverter switches) is given. Next, the 8255 Programmable Peripheral Interface (PPI) [21...23] is described. This description is mainly focused on those aspects of 8255 PPI which are relevant to this thesis.

5.1 Functional Description of the 48 Channel Digital I/O Board

The 48-channel digital I/O board provides a general purpose TTL interface for the IBM PC/XT and AT Computers. The digital I/O lines are provided by industry standard 8255 parallel port IC's, each grouped into three ports of eight lines each. These ports are configured by software control as either inputs (read) or outputs (write). The block diagram of the 48 channel digital I/O board is as shown in Fig. 5.1.

All counters and digital I/O for the 48 channel digital I/O board are accessed



Fig 5.1 Block Diagram of the 48 channel Digital I/O Board

through a standard 37-pin D type male connector that projects through the rear panel of the computer. The 37-pin D type male connector is connected to the 26 pin and 16 pin female type connector through a ribbon cable. The 48 channel digital I/O board uses two sets of above mentioned connector pin assignments. The connector pin assignments and the complete assembly are shown in Fig. 7.B.1 in Appendix B. The specifications of the I/O board are available in Appendix B.

5.2 8255 Programmable Peripheral Interface (PPI)

The 8255 PPI is a popular programmable parallel I/O device. It can be programmed to transfer data under various conditions, from simple I/O to interrupt I/O. It is flexible, versatile, economical and simple to use when multiple I/O ports are required.

The 8255 PPI has 24 I/O pins that can be grouped into two 8-bit parallel ports: A and B, with remaining 8 bit ports as PORT C. The eight bits of PORT C can be used as individual bits or can be grouped in two 4 bit ports: PORT C UPPER and PORT C LOWER. Fig. 5.2 shows the block diagram of the 8255 PPI.

In this thesis, the maximum number of output lines needed is six - for the experimental setup for three phase voltage source inverters (six output lines for the six inverter switches). Hence any six lines of an 8 bit parallel port, configured as an output port, are sufficient for the experimental setups in this thesis. The lines $P_{A0} - P_{A2}$ and $P_{A4} - P_{A6}$ of Port A, which is configured as an output port, are used as the output lines for the



Fig. 5.2 8255 PPI Block Diagram

45

three phase inverter setup. Similarly, for the single-phase half-bridge inverter, lines P_{A1} and P_{A4} are used for the two inverter switches and for the single-phase full-bridge inverter, lines P_{A2} , P_{A4} , P_{A0} and P_{A6} are used for the four inverter switches. In general, the 8 bit ports (A, B and C) can all be configured in a wide variety of functional characteristics by the system software, but each has its own special features or "personality" to further enhance the power and flexibility of 8255. Details on the 8255 PPI operation that are relevant to this thesis is given in the next section.

5.2.1 8255 PPI Operational Description

There are basically three modes of operation for the 8255 PPI :

- 1. Mode 0 Basic Input/ Output
- 2. Mode 1 Strobed Input/ Output
- 3. Mode 2 Bi-Directional Bus

In this thesis, the simplest and most common mode of operation - Mode 0 basic Input/ Output operation was used. The Mode 0 mode of operation provides simple input and output operations for each of the three ports: PORT A, PORT B and PORT C. In this mode, the data is simply written to or read from a specified port. The Input/ Output features of Mode 0 operation are as follows:

- 1. Two 8 bit ports and two 4 bit ports.
- 2. Any port can be Input or Output.
- 3. Outputs are latched.

4. Inputs are not latched.

5.2.2 8255 PPI Control Word Register

The operating characteristics of the 8255 PPI can be configured under software control. It contains a 8 bit internal control word register for this purpose. Figure 5.3 provides the functional description of the control word register. Logic 0 or 1 can be written to the bit positions in this register to configure the individual ports for input or output operation and to enable one of its three modes of operation. Prior to any activity, the 8255 PPI control register must be initialized. This is accomplished by writing a 8 bit control word to the 8255 control register address. Once this is done, the 24 I/ O lines on the 8255 PPI may be accessed at any time by reading or writing to the appropriate port register A, B or C.

For all the experimental setups in this thesis, Port A and Port C (both upper C and lower C ports) are configured as output ports and Port B is configured as an input port. It is evident from the function description in Fig. 5.3 that in order to implement the above configuration, D_0 , D_2 , D_3 , D_4 , D_5 , and D_6 are to be set to 0 and D_1 , D_7 to 1. Setting D_7 to 1 activates the mode set flag. These values for $D_0 - D_7$ constitutes a binary number for the control word, whose hexadecimal value works out to be 82_{16} , and the control word register is initialized with this value.

5.2.3 8255 PPI Data Access



Fig. 5.3 8255 PPI Control Word Bit Functions

Once the control word register is set, the 8255 is ready to perform digital I/O. The ports configured as output ports are write only ports, and ports configured as input ports are read only ports. Since, in this thesis PORT A is configured as an output port, an 8 bit data written to this port is a representation of the voltage levels on $P_{A0} - P_{A7}$. P_{A0} is the Least Significant Bit (LSB) and P_{A7} is the Most Significant Bit (MSB). A TTL low is represented by the 0 bit and a TTL high is represented by the 1 bit. The control word and the data are written to the respective registers by using the addresses of the control word register and the port register. The DIP switch of the 48 channel digital I/ O board is set to 280H. This acts as the base address of the digital I/ O board and from this base address the addresses of the control word register and the port register and the port register and the port register and the port register of the digital I/ O board and from this base address the addresses of the control word register and the port register are obtained.

5.3 8255 PPI Programming

The 8255 PPI is programmed using embedded 'C' language. The code is basically C language with some 8086 Assembly Language functions embedded in it. Two C functions are extensively used - "outpw" and "sleep". The "outpw" function is a standard C library function. The function declaration for the function is:

unsigned outpw(unsigned portid, unsigned value);

The "outpw" function writes to the output port specified by portid. This function writes the low byte of value to portid, and the high byte to portid + 1, using a single 16-bit OUT

instruction. In all the programs for the 8255 PPI, developed for different experimental setups of this thesis, the "outpw" function was used extensively for two purposes:

1. Writing 8-bit data to the output port (Port A for this thesis) register using the given port id (port address).

2. Initializing the control word register of 8255 PPI at the beginning of this program.

The other function which is also used extensively is a local function called as "sleep". This function is basically a C function with a small section of assembly language code embedded in it. This function is declaration for this function is:

void sleep(unsigned value);

The "sleep" function is used to generate pulses of optimal widths in the output waveform. If the output waveform is in a particular state when this function is called, this function ensures that the waveform remains in the same state for a particular period of time or in other words, "sleeps" for a particular amount of time. This corresponds to the value of the function's argument. The section of assembly language code embedded in this function is just three instructions in length and is as below :

_asm{

mov cx, a

pol: dec cx

jnz pol

)

where "a" is the hexadecimal value passed to this function. It is obvious that the above code is a simple loop and that the computer executes the loop "a" times. It was determined that the computer takes 3.7 micro-seconds to execute the loop once. Hence by simple calculation, the value "a" corresponding to the time for which the output should "sleep" is determined.

In all the experimental setups in this thesis, the idea is to turn the inverter switches on for a precalculated amount of time and turn them off for a precalculated amount of time so as to obtain the desired number of pulses per half cycle, whose widths are such that optimal harmonic reduction is achieved. In single phase half bridge inverters, the switch S_1 is turned on and off for optimal amounts of time for the first half cycle and the same is repeated for the switch S_2 in the next half cycle. Similarly, for the full bridge inverters, the pair of switches S_1 and S_2 are turned on for optimal amounts of time for the first half cycle and the same is repeated for switches S_3 and S_4 in the next half cycle.

For both the above configurations, the "outpw" function is used to write an 8 bit data to the port A register such that the desired switch or switches go on or off as the case may be. Then the "sleep" routine is used to keep these switches in this particular state for a precalculated amount of time, until the switches are again turned on or off by the use of the "outpw" function. In three phase inverters, under normal operation (without applying the optimal PWM scheme), at any instant three switches are conducting and each switch conducts for 180° . When the optimal PWM scheme is applied to the three phase inverter, the combined switching pattern of the three switches in the first 60° period is determined

from the results of the optimization program. This switching pattern is the same for the next five 60° periods, but for different set of 3 switches in each of these periods. Again, in each of the 6 periods, the three switches for that period are turned on and off for the precalculated instants of time by using the "outpw" and "sleep" routines. Appendix A has a few sample programs used to program the 8255 PPI.

Chapter Six

Conclusions

6.1 Conclusions

This thesis investigates and successfully implements optimal switching strategies for harmonic elimination in single phase and three phase voltage-source inverters. Optimal switching patterns for the voltage-source inverter configurations were generated through optimization programs. Then a simple low cost control scheme was developed to implement the switching strategies. The single phase and the three phase inverter configurations were individually built on the bench and selected results were verified experimentally by applying the corresponding switching patterns to these circuits, through the control scheme. The results obtained were compared with that obtained through the advantages of the proposed method over the SPWM scheme were established. The main advantages established were:

1. Added flexibility in optimizing a particular objective function such as to obtain selective elimination of harmonics, when compared to the SPWM scheme.

- 2. Lower inverter switching frequency needed for eliminating the same number of harmonics as the SPWM scheme, when both the schemes were applied to a three phase inverter.
- 3. A significantly better quality of output voltage for the same number of pulses per half cycle as the SPWM scheme, when both the schemes were applied to a three phase inverter.

6.2 Recommendations for Further Work

This thesis provides a solid foundation for exploring the industrial applications of these optimal PWM voltage-source inverters. One very important application would be the variable voltage/ variable frequency speed control of three phase induction motors. In this thesis, the optimal switching strategies developed for the three phase inverter was for a fixed per unit fundamental voltage and a fixed switching frequency. A switching strategy could be developed such that for a particular frequency of inverter output, an optimal switching pattern is developed for the per-unit fundamental output voltage which corresponds to that frequency. Hence a large array can be generated with switching patterns for the frequency varying smoothly from a very small value (say 0.5 Hertz) to the standard frequency of operation (say 60 Hertz). For low frequencies of operation, the switching patterns could be adjusted to have large number of pulses per half cycle (to eliminate the large number of troublesome lower order harmonics at low frequencies) and progressively lower number of pulses for higher frequencies of

operation. Also, since in an induction motor, high torque is desired at starting and high efficiency while running, the inverter switching strategies can be optimized to satisfy both conditions, by having one solution for starting and another for running.

Another industrial application that could be investigated, based on the work in this thesis, is the application of optimal PWM single phase inverters in fixed frequency, variable voltage power supplies (uninterruptible power supplies).

It must be mentioned here that although the operation of the experimental setups for the voltage-source inverters was quite satisfactory, some practical difficulties remained, which arose from the specific limitations of the hardware used for the control scheme. The computer on which the I/O board was mounted is an IBM 286 PC. There were difficulties in turning on (or turning off) an inverter switch for very small amounts of time. This difficulty arose only for high frequencies of operation. The obvious solution for this would be to use a much faster computer. Also, in place of a bread-board design, a printed circuit board could be used to prevent loose connections and for high current ratings.

55

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Chapter Seven

Appendices

This chapter on appendices is divided into two sections - Appendix A and Appendix B. Appendix A contains the listings of two sample programs written to program the 8255 programmable peripheral interface (PPI) for implementing the optimal switching strategies. The first program - "spfb3.c" programs the 8255 PPI for implementing a switching strategy for a 3 pulse single phase full bridge inverter, for a per-unit fundamental output voltage of 0.7 pu. The second program - "tph5.c" programs the 8255 PPI for implementing a switching strategy for a 5 pulse three phase inverter, for a per-unit fundamental output voltage of 0.83 pu (an arbitrary value).

Appendix B contains the specifications of the 48 Channel Digital I/ O board, which is used to as a controlling device between the computer and the gate drive circuits for the inverter switches. It also contains the a figure showing the pin assignments of the standard 37 pin D type male connector (used to access the I/O board), 16 and 26 pin female type connectors.

Appendix A

/*	*	*	*	*	*	*	*	*	*	*	*	
*	Progra	m:	spfb3.c	;							*	
*	Progra	mmer:	Rajiv k	Kumar							*	
*	Purpos	e:	To pro	To program the 8255 PPI such as to implement an optimal *								
*			switchi	switching strategy for a 3 pulse single phase full bridge								
*			inverte	r for a p	oer unit	output	voltage	of 0.7 p	ou and a		*	
*			frequer	ncy of 6	60 Hz.						*	
*	*	*	*	*	*	*	*	*	*	*	*/	

#include <stdio.h> #include <stdlib.h> #include <graph.h> #include <time.h> void sleep(unsigned); void ON(unsigned); void ON1(unsigned); void OFF(unsigned); unsigned in port=0x2c1; /* Port ID of the input port (Port B) */ unsigned out_port=0x2c0; /* Port ID of the output port (Port A) */ /* Port ID of the control port */ unsigned con_port=0x2c3; unsigned con_data=0x82; /* Control Word for the Control port */

{

{

```
int m=0, z=0, y=0;
```

outpw(con_port,con_data);

/* Control word is initialized */

for(m=0;m <20000;m++)

/* Start of 0 - 180 degrees period */ sleep(0xff); /* Sleep for 26.89 degrees */ sleep(0x6f); ON1(out_port); /* G1, G2 ON */ sleep(0xff); /* Sleep for 21.60 degrees */ sleep(0x1f); outpw(out_port,0x00); /* G1, G2 OFF */ sleep(0x65);/* Sleep for 8.25 degrees */ ON1(out port); sleep(0xff); /* Sleep for 66.58 degrees */ sleep(0xff); sleep(0xff); sleep(0xb5); outpw(out_port,0x00);

sleep(0x65);

ON1(out_port); sleep(0xff); sleep(0x1f); outpw(out port,0x00); sleep(0xff); sleep(0x6f); /* End of 0 - 180 degrees period */ /* Start of 180 - 360 degrees period */ sleep(0xff); sleep(0x6f); ON(out_port); /* G3, G4 ON */ sleep(0xff); sleep(0x1f); outpw(out_port,0x00); /* G3, G4 OFF */ sleep(0x65); ON(out_port); sleep(0xff); sleep(0xff); sleep(0xff); sleep(0xb5); outpw(out_port,0x00); sleep(0x65);

63
```
ON(out_port);
   sleep(0xff);
   sleep(0x1f);
  outpw(out_port, 0x00);
   sleep(0xff);
  sleep(0x6f);
 }
                                          /* End of 180 -360 degrees period */
  OFF(out_port);
}
/* FUNCTIONS */
void sleep(unsigned a)
{
 _asm{
     mov cx,a
     pol: dec cx
       jnz pol
    }
}
```

```
void ON(unsigned oport_num)
```

```
outpw(oport_num, 0xc0);
```

}

```
void OFF(unsigned oport_num)
```

{

```
outpw(oport_num, 0x00);
```

}

void ON1(unsigned opo_num)

{

outpw(opo_num, 0x11);

}

/*	*	*	*	*	*	*	*	*	*	*	*
*	Progra	m:	tph5.c								*
*	Progra	mmer:	Rajiv k	Kumar							*
*	Purpos	se:	To prog	gram th	e 8255	PPI suc	h as to	implem	ent an o	ptimal	*
*			switchi	ng strat	tegy for	a 5 pul	se three	phase i	inverter	for a	*
*			per-uni	t outpu	t voltag	e of 0.8	3 pu. ai	nd frequ	ency of	20 Hz	*
*	*	*	*	*	*	*	*	*	*	*	*/

<pre>#include <stdio.h></stdio.h></pre>	
<pre>#include <stdlib.h></stdlib.h></pre>	
<pre>#include <graph.h></graph.h></pre>	
<pre>#include <time.h></time.h></pre>	
void sleep(unsigned);	
void OFF(unsigned);	
unsigned in_port=0x2c1;	/* Port id of the input port (PORT B) */
unsigned out_port=0x2c0;	/* Port id of the output port (PORT A) */
unsigned con_port=0x2c3;	/* Port id of the control port */
unsigned con_data=0x82;	/* Control word for the Control Register */
/* Note that the gating signals for th	ne MOSFETs S1, S2, S3, S4, S5 and S6 are G1, G2,
G3, G4, G5 and G6 respectively */	

void main(void)

•

{

```
int m=0,z=0,y=0;
outpw(con port,con data);
                                  /* Initializes the Control Register */
outpw(out_port, 0x03);
                                  /* G5, G6 ON, G1 OFF */
for(m=0;m <23000;m++)
{
                                  /* Start 0 - 60 degree period*/
 sleep(0xff);
                                  /* Sleep for 10.589 degress */
sleep(0xb9);
outpw(out port,0x13);
                                  /* G5, G6, G1 ON */
sleep(0xd6);
                                  /* Sleep for 5.359 degrees */
outpw(out_port,0x03);
                                  /* G5, G6 ON, G1 OFF */
sleep(0xff);
                                  /* Sleep for 6.837 degrees */
sleep(0x0d);
outpw(out_port,0x13);
sleep(0x06);
                                  /* Sleep for 0.823 degrees */
outpw(out_port,0x11);
                                 /* G1, G6. ON, G5 OFF */
sleep(0x60);
                                 /* Sleep for 2.659 degrees */
outpw(out_port,0x13);
sleep(0xff);
sleep(0x28);
                                 /* Sleep for 7.467 degrees */
outpw(out port,0x03);
```

```
sleep(0x60);
```

outpw(out_port,0x13);

```
sleep(0x06);
```

```
outpw(out_port,0x11);
```

sleep(0xff);

sleep(0x0d);

```
outpw(out_port,0x13);
```

sleep(0xd6);

```
outpw(out_port,0x11);
```

sleep(0xff);

```
sleep(0xb9);
```

```
/* stop 0 - 60 degrees period*/
```

sleep(0xff);	/* Start 60 -120 degrees period*/
sleep(0xb9);	
outpw(out_port, 0x31);	/* G6, G1, G2 ON */
sleep(0xd6);	
outpw(out_port, 0x11);	/* G6, G1 ON, G2 OFF */
sleep(0xff);	
sleep(0x0d);	

outpw(out_port, 0x31);

sleep(0x06);

outpw(out_port, 0x30); /* G1, G2 ON, G6 OFF */

sleep(0x60);

outpw(out_port,0x31);

sleep(0xff);

sleep(0x28);

outpw(out_port, 0x11);

sleep(0x60);

```
outpw(out_port, 0x31);
```

sleep(0x06);

outpw(out_port, 0x30);

sleep(0xff);

sleep(0x0d);

```
outpw(out_port, 0x31);
```

sleep(0xd6);

```
outpw(out_port,0x30);
```

sleep(0xff);

sleep(0xb9);

/* Stop 60 - 120 degrees period */

sleep(0xff);

/* Start 120 - 180 degrees period*/

sleep(0xb9);

outpw(out_port, 0x70); /* G1, G2, G3 ON */ sleep(0xd6); outpw(out_port, 0x30); /* G1, G2 ON, G3 OFF */ sleep(0xff); sleep(0x0d); outpw(out_port, 0x70); sleep(0x06); outpw(out_port, 0x60); /*G2, G3 ON, G1 OFF */ sleep(0x60); outpw(out_port, 0x70); sleep(0xff); sleep(0x28);outpw(out_port, 0x30); sleep(0x60); outpw(out_port, 0x70); sleep(0x06); outpw(out_port, 0x60); sleep(0xff); sleep(0x0d); outpw(out_port, 0x70); sleep(0xd6);

70

outpw(out_port, 0x60);

sleep(0xff);

```
sleep(0xb9); /* Stop 120 - 180 degrees period */
```

outpw(out_port, 0x60); /* G2, G3 ON, G4 OFF */

sleep(0xff);

sleep(0x0d);

outpw(out_port, 0xe0);

sleep(0x06);

outpw(out_port,0xc0);

/* G4, G3 ON, G2 OFF */

sleep(0x60);

outpw(out_port, 0xe0);

sleep(0xff);

sleep(0x28);

outpw(out_port, 0x60);

sleep(0x60);

outpw(out_port, 0xe0);

sleep(0x06);

outpw(out_port, 0xc0);

sleep(0xff);

sleep(0x0d);

outpw(out_port, 0xe0);

sleep(0xd6);

outpw(out_port, 0xc0);

sleep(0xff);

sleep(0xb9); /* Stop 180 - 240 degrees period */

sleep(0xff);

/* Start 240 - 300 degrees period */

sleep(0xb9);

outpw(out_port,0xc2); /* G3, G4, G5 ON */

sleep(0xd6);

outpw(out_port, 0xc0); /* G3, G4 ON, G5 OFF */

sleep(0xff);

sleep(0x0d);

outpw(out_port, 0xc2);

sleep(0x06);

outpw(out_port, 0x82); /* G4, G5 ON, G3 OFF */

sleep(0x60);

```
outpw(out_port, 0xc2);
```

sleep(0xff);

sleep(0x28);

outpw(out_port, 0xc0);

sleep(0x60);

outpw(out_port, 0xc2);

sleep(0x06);

outpw(out_port, 0x82);

sleep(0xff);

sleep(0x0d);

```
outpw(out_port, 0xc2);
```

sleep(0xd6);

```
outpw(out_port, 0x82);
```

sleep(0xff);

sleep(0xb9);

/* Stop 240 - 300 degrees period */

sleep(0xff);

/* Start 300 - 360 degrees period*/

sleep(0xb9);

outpw(out_port, 0x83); /* G4, G5, G6 ON */

sleep(0xd6);

outpw(out_port, 0x82); /* G4, G5 ON, G6 OFF */

sleep(0xff);

sleep(0x0d);

outpw(out_port, 0x83);

sleep(0x06);

outpw(out_port, 0x03);

sleep(0x60);

outpw(out_port, 0x83);

sleep(0xff);

sleep(0x28);

outpw(out_port, 0x82);

sleep(0x60);

outpw(out_port, 0x83);

sleep(0x06);

outpw(out_port, 0x03);

sleep(0xff);

sleep(0x0d);

outpw(out_port, 0x83);

sleep(0xd6);

outpw(out_port, 0x03);

sleep(0xff);

sleep(0xb9);

/* Stop 300 - 360 degrees period*/

}

OFF(out_port); /* Sets all output lines to zero */

}

```
/* FUNCTIONS */
```

void sleep(unsigned a)

{

_asm{

mov cx,a

pol: dec cx

jnz pol

}

}

void OFF(unsigned oport_num)

{

outpw(oport_num, 0x00);

}

.

Appendix B

Specifications of the 48 Channel Digital I/O Board

1. Digital I/O

Quantity	48
Input logic low voltage	-0.5 V min. to 0.8 V max.
Input logic high voltage	2.0 V min. to 5.0 V max.
Input load current	-10 μA min to +10 μA max.
Output low voltage	0.45 V max.
Output high voltage	2.4 V min.

Note: Digital lines are TTL/ DTL compatible and will drive 1 standard (74XX type) TTL load or 4 (74LSXX type) LSTTL loads. A 10 K ohm resistor to +5 V DC is supplied on each digital I/O line providing CMOS compatibility.

2. Counter I/O: (8253 IC's)

Quantity	6
Resolution	16 bits
Frequency	DC to 2.6 Mhz.
Input logic low voltage	-0.5 V min. to 0.8 V max.
Input logic high voltage	2.0 V min. to 5.0 V max.
Input load current	-10 μA min to +10 μA max.
Output low voltage	0.45 V max.
Output high voltage	2.4 V min.



Fig. 7.B.1 Connector Pin Assignments

78