THE HIGH-POWER EFFICIENCY AND HIGH-POWER DENSITY CONVERTERS FOR DATA CENTER APPLICATION SYSTEM

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THE HIGH-POWER EFFICIENCY AND HIGH-POWER DENSITY CONVERTERS FOR DATACENTER APPLICATION SYSTEM

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ABSTRACT

THE HIGH-POWER EFFICIENCY AND HIGH-POWER DENSITY CONVERTERS FOR DATACENTER APPLICATION SYSTEM

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This dissertation focuses on the new energy resources based power supply system for the Datacenter application. A family of the matrix auto-transformer switched capacitor DC-DC converters and a decoupled active and reactive power control method for cascaded microinverter system are proposed in this dissertation. The matrix auto-transformer switched capacitor DC-DC converters are mainly for the 48V DC bus structure which is proposed by Google company, and they convert the 48V DC bus voltage to different intermediate bus voltages, i.e. 6V, 5V, 3.2V and so on. Moreover, the converters mainly focus on the high-efficiency and high-power density goals which are very important indexes in the datacenter application, especially with the dramatic increase demand of the artificial intelligence. The proposed converters in this dissertation can further increases the performance of the DC-DC converters compared to the state of art converters. The control method for the cascaded microinverter systems can decouple the active and reactive power distribution among different submodules, which means the more flexible power arrangement among different submodules, and the commutations among different submodules are also saved. As a result, not only the whole system cost but also the robustness get largely improved.

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CHAPTER 1

INTRODUCTIONS OF THE POWER SUPPLY SYSTEM

With the development of artificial intelligence (AI), cloud computing, and mobile internet, a growing number of data-centers have been built all over the world. Currently, the DC distribution system for data center applications has started to be adopted in the industry to replace the AC distribution system due to its high-power efficiency. Figure 1-1 shows the new energy resources-based datacenter application structure. Firstly, the power from grid or solar panel is transferred to the AC power grid. Next AC power is converted to 48V DC voltage and finally the 48V DC voltage is converted to the voltage that chip adopted, i.e. 1.8V, through one or two stages. The converter in the first stage is usually called intermediate bus converter (IBC) since it converts the 48V DC to an intermediate voltage like 12V DC in Figure 1-1. The converter in the second stage converts 12V DC to the chip-level voltage. Moreover, the 480V AC bus with 60Hz can be generated by power grid through the line transformers. Or it can also be generated through the solar PV panel through the DC to AC inverters.

The state of art DC-DC converter for the first stage is studied shown in Figure 1-2. The line shown in red block is designed by our group. The orange color line shows the 48-V to 12-V(4x) converter, the green color line shows the 48-V to 8-V(6x) converter and the purple color line shows the 48-V to 6-V(8x) converter. Although the power density as well as power efficiency of 8x converter is lower than 4x converter, the high conversion ratio issue of the second stage could be solved. If the more detailed compassion is made, it can be found that the efficiency doesn't decrease much when compare 4x and 8x converter among full load range. In this thesis, we mainly focused on the cascaded microinverter system under island mode and the DC-DC converter that converts 48V DC to an intermediate bus voltage for the datacenter application.

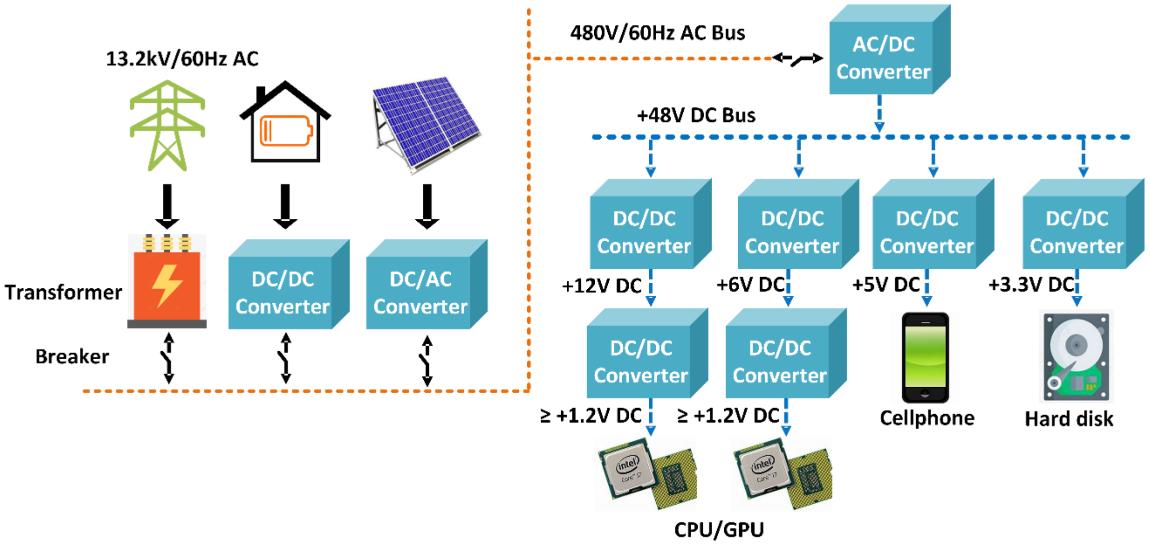

Figure 1-1 The power supply system for the datacenter application

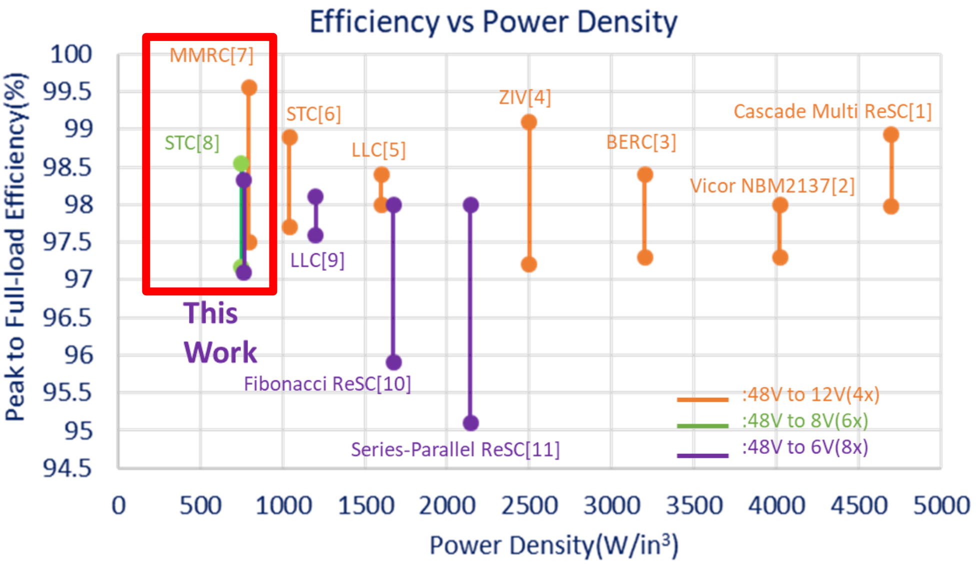

Figure 1-2 The state of art DC-DC converter of the first stage for datacenter application

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CHAPTER 2

CASCADED CONNECTED MICROINVERTER UNDER ISLAND MODE

2.1 The Introduction of the Cascaded Microinverter System

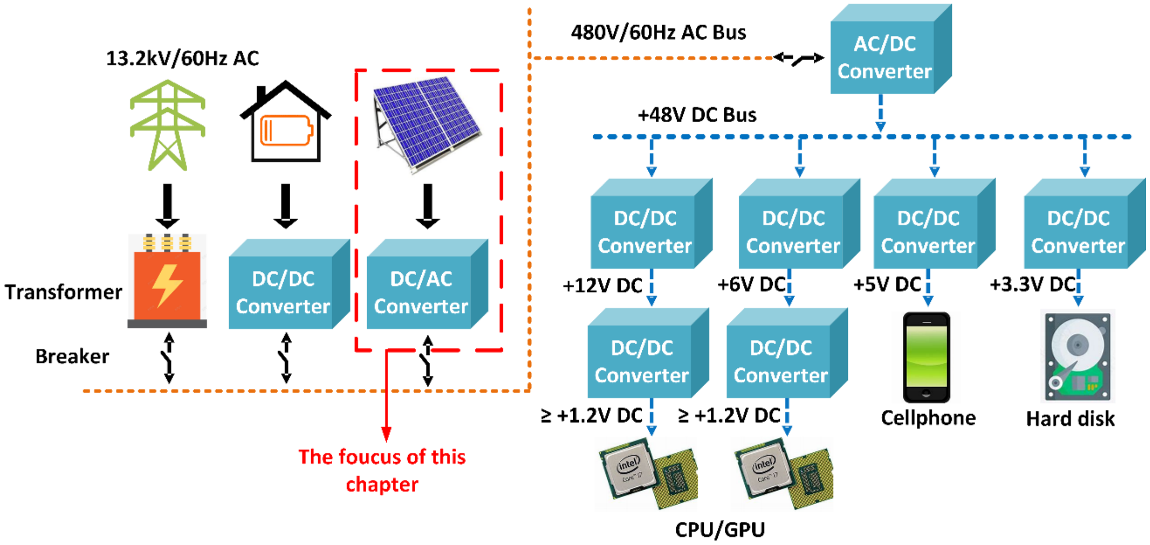


Figure 2-1 This chapter focuses on the cascaded microinverter

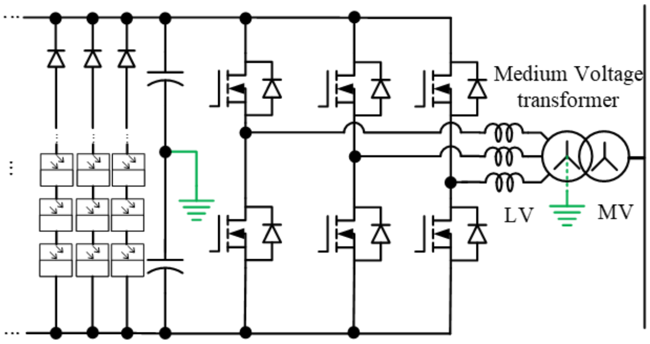


Figure 2-2 Traditional grid-tied medium voltage solar inverter system

Distribute Generator has been widely studied recently for new energy resources application such as photovoltaic(PV), wind and tidal energy. In medium voltage area, typical structure of a PV power plant system is shown as Figure 2-2. It consists of a three-phase 2L-NPC (or 3L-T-type) inverter, a three-phase medium-voltage transformer and plenty of PV modules. This structure is commercially used for decades and the power rate can reach megawatt. However, the efficiency is relatively low since only centralized maximum power point tracking (MPPT) control can be performed. Moreover, the bulky and heavy line-frequency transformer significantly increases the whole system cost, volume and weight. In order to solve this issue, multilevel modular converter (MMC) is proposed. MMC takes the advantage of adopting low voltage stress devices. By saving the bulky line-frequency transformer, both the weight and volume of the whole system have been greatly reduced. Moreover, every submodule of MMC can perform its own MPPT, which can realize relatively higher solar conversion efficiency than typical structure does. MMC can be divided into single-star and double-star structure, where single-star MMC converter is also named as Cascaded Multilevel Inverter (CMI). CMI system have been explored and evaluated in different applied fields such as static var generator (SVG), active power filter(APF) and motor drive area. Furthermore, with the development of wide bandgap devices, CMI system combined with low voltage stress, high switching speed as well as small size Gallium Nitride(GaN) devices attract more and more attention in recent years. For example, the GaN-EPC2021 from EPC corporation is an 80V/90A device with 2.2mΩ conduction resistance, and its die area is just 13.9mm2. By adopting these low voltage GaN devices, the CMI system with extremely high-power density can be realized.

In the light of CMI system, power sharing and communication within different sub-modules are two hot issues that should be addressed, which could be easily solved if the CMI system becomes centralized structure. Centralized structure requires a central calculation unit to burden all the calculation task and all sub-modules’ ADC data should be transferred to central unit. This central unit spreads out the PWM signals to every submodule after finishing all the calculation. As a result, it is very suitable for the case that all sub-modules are integrated into one PCB board. However, if the distance between two submodules become too far, such centralized structure will be more difficult to realize because at this time high-bandwidth communication tool must be adopted to synchronize all sub-modules’ phase. For example, Ref. [7] adapts high-bandwidth intraconverter communication system to transmit time critical control signals within different submodules. Under such circumstance, the hardware cost is much higher with relatively lower robustness. In order to solve these issues with central structure, different methods have been proposed, which mainly focus on the communication-independent solutions. In general, they can be divided into two categories based on whether the droop control is adopted. Droop control method originates from the synchronous generator that active power is controlled by adjusting synchronous generator’s frequency and reactive power is controlled by adjusting its output voltage. This control method has been successfully adopted in parallel-inverter system with communication part among different submodules being totally avoided. Ref. [13] applies the droop control concept into CMI system so that the communication part is totally saved, and it is also named as inverse droop control. Ref. [8]-[12] doesn’t adopt inverse droop control to synchronize the sub-modules’ phase, instead, each sub-module directly samples PCC voltage to synchronize its own phase. Although the communication can be avoided, the measurement circuits for PCC voltage are still required for each sub-module. Therefore, they are still communication-dependent systems since every sub-module should obtain PCC voltage information. Inverse droop control can further be divided into grid-tied system and island system. For grid-tied system, the main target is to manage all submodules’ active power and reactive power which are injected to the grid. In [20] and [22], each sub-module has the ability to inject any active power to power grid without grid voltage information, however, they must keep reactive power to 0 Var. In [21], all sub-modules must inject the same active power and reactive power to the power grid, where in this case both the active power as well as the reactive power among different sub-modules are not decoupled. In [23], all submodules must inject the same active power to the power grid while keep the reactive power under same proportion. Ref. [24] can realize the decoupled active power distribution among different submodules. However, the power distribution ratio of reactive power must be the same as the active power distribution ratio. Therefore, only active power is decoupled in this case. Moreover, Ref. [23]-[24] requires an additional module to sample the PCC voltage, which should be called weak communication-dependent system.

Different from grid-tied system, island inverter system requires CMI system to produce both active power and reactive power. It mainly focuses on how to control the PCC voltage as a stable value of 120V/60Hz. The total power injected to the PCC point depends on the load side. Figure 2.2 shows a CMI system with 3 sub-modules in series, with different sub-modules powered by different DC sources such as solar panels, lithium battery and so on. The power capacity of these DC sources may greatly differ from each other, which makes the management of active power and reactive power distribution among sub-modules of great significance. However, this fact is not demonstrated in the previous publications. Instead of power allocation, most of the research works assume that each module will output the same power. It could be even worse that the island system may suffers from unstable issues due to the existing two equilibrium points compared with grid-tied system. For example, in [13]-[14], the system is stable only under inductive load condition. Every sub-module can just output the same active power and reactive power respectively, where both active power and reactive power distribution cannot be decoupled. Ref. [15]-[17] mainly focus on solving the stability issues under different load characteristics, while the power distribution among different sub-modules is subject to certain limitations. Ref. [18]-[19] partially solve the power distribution issue, with the active power of different submodules can be arbitrarily distributed, while the proportion of reactive power distribution should be the same as that of active power. Detailed comparison of different CMI decoupling methods is listed in Table 2-1.

A fully decoupled control method of active and reactive power distribution for the single-phase CCM system is proposed in [30]. Compared with the existing control method, the proposed method in [30] could achieve the active power and reactive power distribution fully decoupled, which is not restrained, not equal, and completely decoupled within different submodules under the islanded application. By using this method, issues of multiple-equilibrium points under islanded mode are also eliminated regardless of load characteristics, and the communication among different submodules as well as PCC voltage sampling circuits can be avoided. Since the active power and reactive power distribution are fully decoupled by utilizing the proposed control method, the mismatch of active and reactive power capabilities among different submodules can be easily solved. Therefore, the proposed method can enable the CCM system to become a competitive candidate for islanded application. In this paper, more detailed analysis including the active and reactive power distribution range among different submodules, system hardware design, simulation results, experimental results and most importantly, the stability proof of the system with proposed control method is performed to further enhance the feasibility of the proposed control method in [30] and this paper.

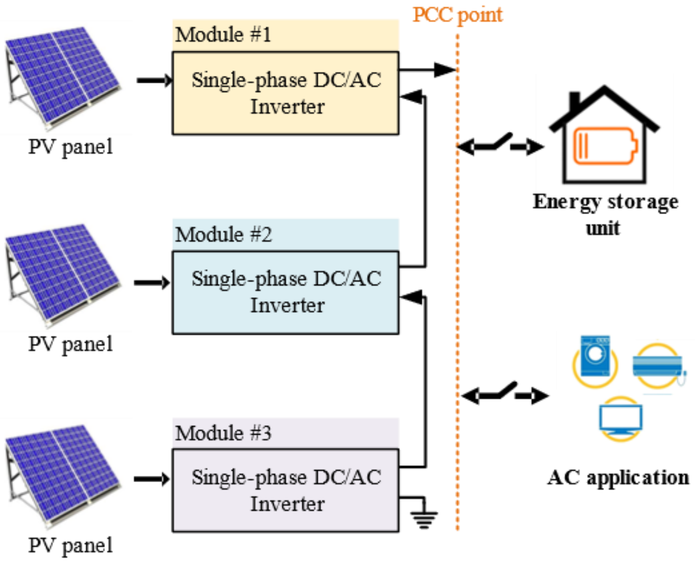


Figure 2-3 Single phase CCM with 3 submodules under islanded mode.

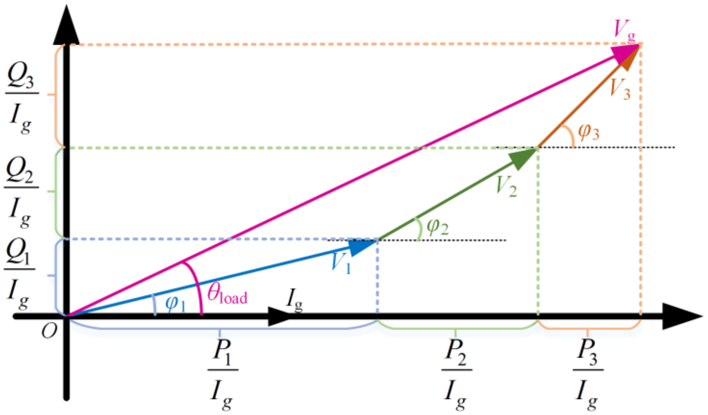


Figure 2-4 The relationship between output power and corresponding voltage

Table 2-1 Comparison within different control methods for CCM system

Ref.	No communication within submodules	Avoid sampling PCC voltage	Stable for all kinds of load	Active power distribution is decoupled	Reactive power distribution is decoupled	Grid-tied mode	Island Mode
[11]			✓	✓	✓		✓
[10], [12]-[17]	✓	All submodules are required	✓	✓	✓		✓
[17]-[18]	✓	✓					✓
[19]-[23]	✓	✓	✓				✓
[24],[25]	✓	✓	✓	✓		✓	
[25]	✓	✓	✓			✓	
[27]	✓	Only one submodule is required	✓			✓	
[28]	✓		✓	✓		✓	
Proposed Method	✓	✓	✓	✓	✓		✓

*'Power distribution is decoupled' means power can be arbitrarily distributed within different submodules

2.2 Proposed Control method

2.2.1 Derivation of Droop Control Method Based on Proposed Method (Q,φ-f, V)

The proposed control methods are not constrained by the number of submodules. However, in order to simplify the derivation, suppose a CCM system with three submodules in series, and their output voltages are expressed as $V_1e^{j\varphi_1}$, $V_2e^{j\varphi_2}$, $V_3e^{j\varphi_3}$ respectively, as is shown in Figure 2-4. The total output voltage is expressed as $V_{PCC}e^{j\theta_{load}}$. Furthermore, the active and reactive power generated by three submodules is P_1, P_2, P_3, and Q_1, Q_2, Q_3 respectively. After normalization, the active power and reactive power are described as P_{nom1}, P_{nom2}, P_{nom3} and Q_{nom1}, Q_{nom2}, Q_{nom3}. The basic derivation of the system is expressed in equation (2-1) to (2-5) as follows.

$$P_{nom1}:P_{nom2}:P_{nom3} = V_1\cos\varphi_1:V_2\cos\varphi_2:V_3\cos\varphi_3 = P_1:P_2:P_3 \tag{2-1}$$

$$Q_{nom1}:Q_{nom2}:Q_{nom3} = V_1\sin\varphi_1:V_2 sin\varphi_2:V_3 sin\varphi_3 = Q_1:Q_2:Q_3 \tag{2-2}$$

$$P_{nom1} + P_{nom2} + P_{nom3} = 1 \tag{2-3}$$

$$Q_{nom1} + Q_{nom2} + Q_{nom3} = 1 \tag{2-4}$$

$$V_1e^{j\varphi_1} + V_2e^{j\varphi_2} + V_3e^{j\varphi_3} = V_{PCC}e^{j\theta_{load}} \tag{2-5}$$

Solving (2-1)-(2-5) leads to (2-6)-(2-7)..

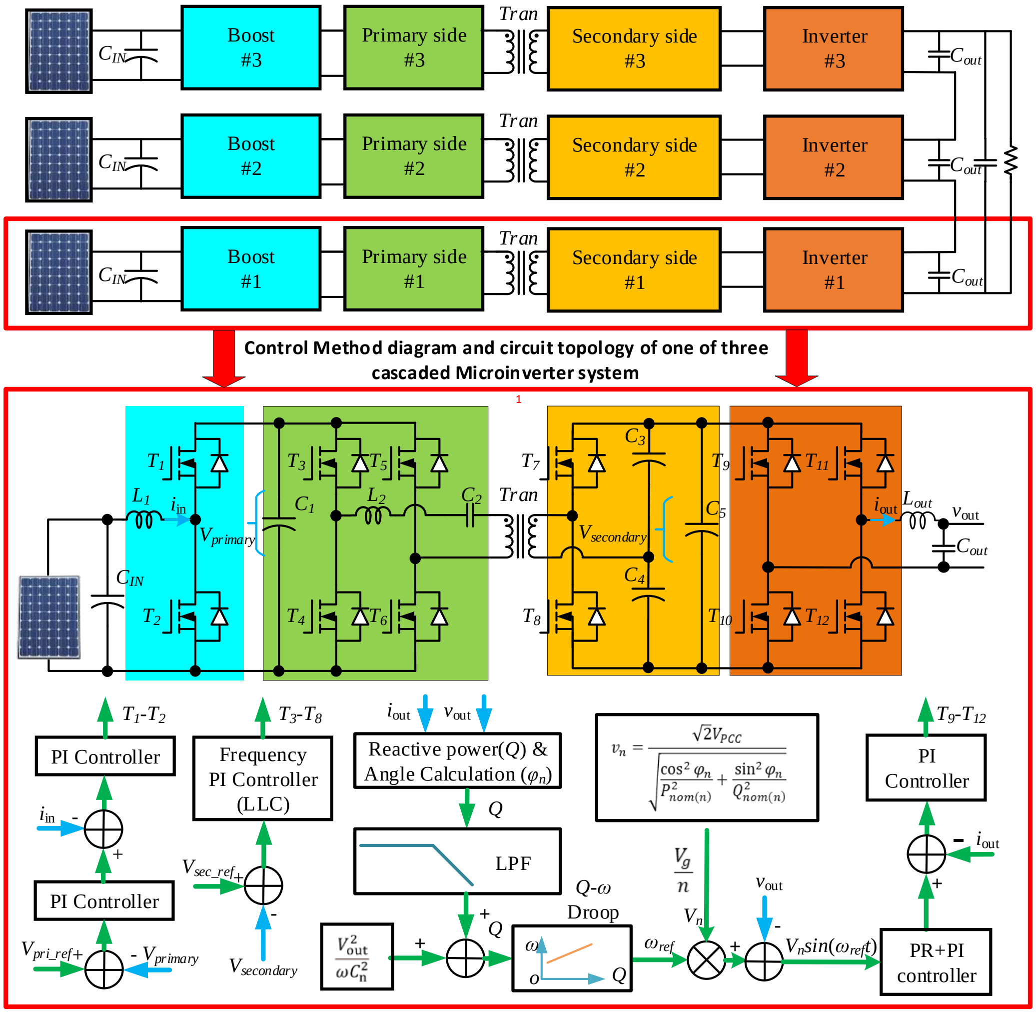


Figure 2-5 The proposed fully decoupled CCM system.

$$\frac{V_1\cos\varphi_1}{P_{nom1}} = \frac{V_2\cos\varphi_2}{P_{nom2}} = \frac{V_3\cos\varphi_3}{P_{nom3}} = V_{PCC}\cos(\theta_{load}) \tag{2-6}$$

$$\frac{V_1 sin\varphi_1}{Q_{nom1}} = \frac{V_2 sin\varphi_2}{Q_{nom2}} = \frac{V_3 sin\varphi_3}{Q_{nom3}} = V_{PCC}\sin(\theta_{load}) \tag{2-7}$$

$$k_1Q_1 = k_2Q_2 = k_3Q_3 = \Delta\omega \tag{2-8}$$

$$k_n = \frac{k_{droop}}{Q_{nom(n)}} \quad n \in \{1,2,3\} \tag{2-9}$$

$$V_n = \frac{V_{PCC}}{\sqrt{\frac{\cos^2\varphi_n}{P_{nom(n)}^2} + \frac{\sin^2\varphi_n}{Q_{nom(n)}^2}}} \quad n \in \{1,2,3\} \tag{2-10}$$

According to the droop control strategy which feedbacks reactive power and phase angle to adjust output frequency and output voltage (Q, φ-f, V), then (2-8) should be satisfied. Where k_1~ k_3 stands for three submodules' droop factor, is expressed in (2-9).

To satisfy the condition that the total output voltage is equal to V_{PCC}, and the active power distribution ratio is equal to P_{nom1}:P_{nom2}:P_{nom3}, each submodule's output voltage V_{n} is derived as (2-10).

Table 2-2 Parameters for ccm system's submodule

Symbol	Parameters	Value
$V_{\mathrm{PCC}}/f_{\mathrm{PCC}}$	PCC Voltage (RMS/frequency)	56.56V/60Hz
V_{in}	Input Voltage	20~30V
V_{Primary}	Primary Side DC link voltage	40V
$V_{\mathrm{secondary}}$	Secondary Side DC link voltage	40V
V_{n}	Output voltage for each subsmodule (RMS)	0~28V
L_1	Boost stage inductor	10μH/PCV-0-103-20L
L_2	LLC resonant inductor	2.55μH
T_{13}	High frequency transformer (Turn ratio)	2:1
L_{out}	Inverter stage output inductor	15μH/VER2923-153KL
C_{IN}	Boost stage input side capacitor.	44μF
C_{out}	Inverter stage output side capacitor	10μF
C_1	Boost stage output capacitor	44μF
C_2	Resonant capacitor	147nF
C_3~C_4	Secondary side capacitor	10uF
C_5		1.5mF
f_{s1}	Boost stage and inverter stage switching frequency	250kHz
f_{s2}	LLC stage frequency	230kHz~270kHz
T_1~T_{12}	Switching devices	EPC2021
P_1~P_3	Active power of each submodule	0~200W
Q_1~Q_3	Reactive power of each submodule	-100~100 Var
P_{nom1}~P_{nom3}	Standardized active power distribution ratio	0.2~0.4
Q_{nom1}~Q_{nom3}	Standardized reactive power distribution ratio	0.2~0.4
k_{iL}	Inverter stage current inner loop feedback factor	0.2
k_p, k_i	Inverter stage voltage outer PI loop	0.007954, 149.9
ω_o	Inverter stage voltage outer PR loop's resonant angular frequency	$377\times m$ $m\in\{1,3,5\}$
ω_{LPF}	Cutoff frequency of low pass filter	125.6 rad/s

2.3 Proposed Control Scheme Based on Proposed Control Law

Figure 2-5 illustrates the control scheme of the proposed fully decoupled control of active and reactive power distribution for CCM system. The boost stage adapts primary side voltage as the outer loop feedback variable and inductor current as the inner loop feedback variable. The LLC circuit feedbacks secondary side voltage to adjust the PWM frequency.

Regarding the inverter stage, the reactive power is calculated by sampling the submodule's output voltage and current. To calculate the output power angle, the classic digital PLL is adopted. Since the calculated reactive power contains the harmonic component, a digital LPF which is expressed in (2-11) is utilized to decrease the second-order harmonic component.

$$Q_{n(filter)} = \frac{\omega_{LPF}}{s + \omega_{LPF}} Q_n \tag{2-11}$$

The -3dB cutoff frequency of the LPF is set as 20Hz. Each inverter's angular frequency can be expressed in (2-11). (2-11) and the parameter k_n directly influences the system's dynamic response. The detailed analysis is shown in (2-12).

$$\omega_{ref} = \omega^* - Q_{n(filter)} \times k_n \tag{2-12}$$

Based on the calculation above, each submodule's output voltage reference can be expressed in (2-13), and the output voltage changes with its reactive power and power angle. Since each submodule's control scheme is independent of the other submodules', in this case, all the communication part has been totally saved. And the PCC voltage phase information is not needed anymore, which improves the robustness of the whole system and lowers the hardware cost. In addition, the active power and reactive power within different submodules can be distributed within a wide range. In summary, the power capacities of different submodules are not required to be equal anymore, which certainly improves the flexibility and applicability of the whole system.

$$v_n(t) = \frac{\sqrt{2}V_{PCC}}{\sqrt{\frac{\cos^2 \varphi_n}{P_{nom(n)}^2} + \frac{\sin^2 \varphi_n}{Q_{nom(n)}^2}}} \sin(\omega_{ref} t) \tag{2-13}$$

When $P_{\text{nom(n)}}$ is equal to $Q_{\text{nom(n)}}$, then (2-13) can be expressed in (2-14), where its RMS value is constant. Therefore, previous work can be treated as a special case that which active and reactive power distribution are equal.

$$v_n(t) = \sqrt{2}V_{PCC}P_{nom(n)} \sin(\omega_{ref} t) \,|_{P_{nom(n)}=Q_{nom(n)}} \tag{2-14}$$

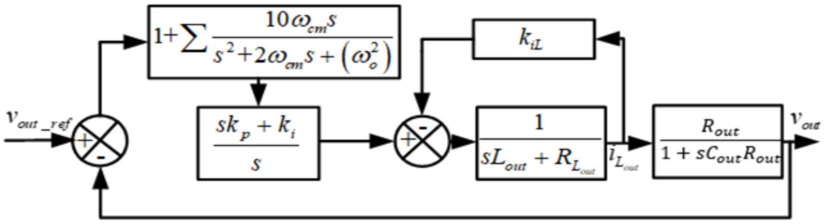


Figure 2-6 Double Loop of CCM system's submodule.

2.3.1 Design of Double Loop Compensator

Here, PR with PI controller is adapted to the output voltage loop, and P controller is adopted as the inner current loop. The inverter stage control block is shown in Figure 2-6. For typical double-loop control, the inner inductor current loop is usually adopted to suppress the resonant spike caused by the LC filter. Here, the LC filter will cause a 180° output voltage phase shift at its resonant frequency so that the system may be unstable, especially at light load. Each submodule's open-loop transfer function G_o before compensation is expressed as (2-15), Where k_{iL} is the inner loop feedback coefficient.

$$G_O = \frac{k_{iL}V_{secondary}}{s^2LC + sC(R_L + k_{iL}V_{dc} + \frac{L}{CR_{load}}) + \frac{R_{load} + k_{iL}V_{dc} + R_L}{R_{load}}} \tag{2-15}$$

The bode diagram that v_n^* to v_n is shown in (2-15). With the increase of the inner current loop's gain k_{iL}, the dc gain will rise accordingly. More importantly, the LC resonant spike is suppressed by the inner current loop so that the whole system becomes more stable. To further improve control accuracy, the PR+PI compensator is adopted to increase gain at line frequency.

Set k_{iL} and cutoff frequency as 0.2, and 300Hz respectively, and the zero of PI controller is set as 3kHz to avoid phase lag at the cutoff frequency. As a result, the PI compensator is expressed in (2-16)~(2-18).

$$G_O = \frac{k_{iL}V_{secondary}}{s^2LC + sC(R_L + k_{iL}V_{dc} + \frac{L}{CR_{load}}) + \frac{R_{load} + k_{iL}V_{dc} + R_L}{R_{load}}} \tag{2-16}$$

$$|G_{open}|\big|_{s=j2\pi\times 300} = |G_o G_{PI} G_{PR}| = 1 \tag{2-17}$$

$$\left|\frac{k_i}{sk_p}\right| |_{s=j2\pi\times 3000} = 1 \tag{2-18}$$

In order to improve the gain at the line and harmonic frequency, the Quasi-PR controller that resonant frequency at 50Hz, 150Hz, and 300Hz is adopted. Since PCC point frequency will change with power, ω_{cm} should be carefully designed. Assume that the PCC point frequency variation is 2%, then ω_{cm} should be equal to $2\pi f$×2%. The PR controller is expressed in (2-19). The specific parameters of the control loop are shown in Table 2-2. The open-loop bode diagram after compensation is shown in (2-20). The cutoff frequency is around 325Hz and the phase margin is 45˚, which meets the dynamic requirement.

$$G_{PR} = 1 + \sum_{m=1,3,5} \frac{2\times 5\omega_{cm}s}{s^2 + 2\omega_{cm}s + (2\pi\times 60m)^2} \quad \begin{cases} \omega_{cm} = 2\pi f \times \Delta f \\ m \in \{1,3,5\} \\ \Delta f = 2\pi f \times 2\% \end{cases} \tag{2-19}$$

$$\begin{aligned} k_1(I_{1out}V_1\sin\varphi_1 - \frac{V_1^2}{\omega C_{out}^2}) &= k_2(I_{2out}V_2\sin\varphi_2 - \frac{V_2^2}{\omega C_{out}^2}) \\ &= k_3(I_{3out}V_3\sin\varphi_3 - \frac{V_3^2}{\omega C_{out}^2}) = \Delta\omega \end{aligned} \tag{2-20}$$

The output power is calculated by the inductor current instead of PCC current and output voltage, which ignores the reactive power consumed by C_{out}. To further improve the calculated power precision, the reactive power consumed by output capacitor C_{out} should be compensated, where in this case equation (2-8) is replaced by (2-20)

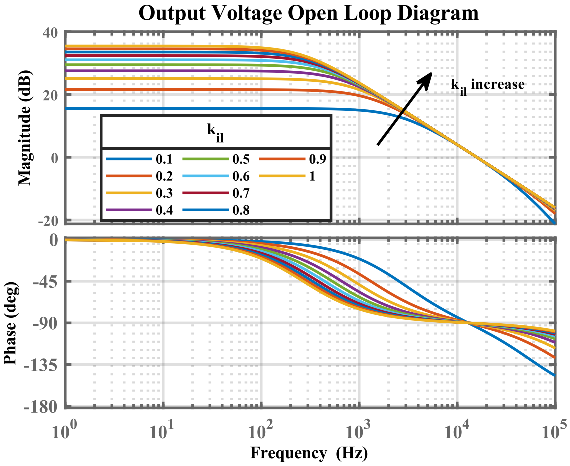


Figure 2-7 The open loop bode plot with inner current loop compensation

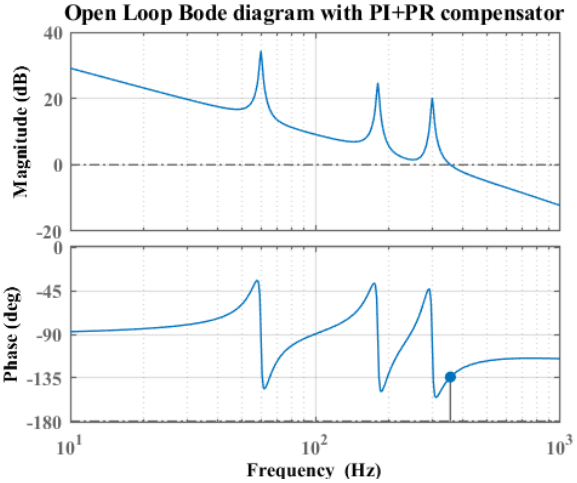


Figure 2-8 The open loop bode plot with PR+PI compensation

2.4 System Analysis

This section presents a detailed discussion on the active power and reactive power distribution range and descriptive analysis of system stability. Based on (2-1) and (2-2), phase angle and amplitude are expressed in (2-21) and (2-22) respectively.

$$\varphi_n = \tan^{-1}\left(\frac{Q_{nom(n)}}{P_{nom(n)}}\tan\theta_{load}\right) \quad n \in \{1,2,3\} \quad \varphi_n \in (-\frac{\pi}{2},\frac{\pi}{2}) \tag{2-21}$$

$$V_n = V_{PCC}\sqrt{(P_{nom(n)}cos(\theta_{load}))^2 + (Q_{nom(n)}sin(\theta_{load}))^2} \tag{2-22}$$

$$
\begin{aligned}
k_1(I_{1out}V_1\sin\varphi_1-\frac{V_1^2}{\omega C_{out}^2}) &= k_2(I_{2out}V_2\sin\varphi_2-\frac{V_2^2}{\omega C_{out}^2}) \\
&= k_3(I_{3out}V_3\sin\varphi_3-\frac{V_3^2}{\omega C_{out}^2}) = \Delta\omega
\end{aligned}
\tag{2-23}
$$

Each submodule's output power phase angle and its voltage amplitude are related to distribution ratio and load characteristics. Moreover, the sign of each submodule's output power angle φ_n is the same as load's, which indicates that there is no such a case that one submodule works at inductive-inverter mode while the other submodule works at capacitive-inverter mode. And the output power angle φ_n of different submodules' is decoupled. For n^{th} submodule, if the active power distribution ratio is equal to the reactive power distribution ratio ($P_{nom(n)}=Q_{nom(n)}$), then its output power angle is equal to the load angle ($\varphi_n=\theta_{load}$).

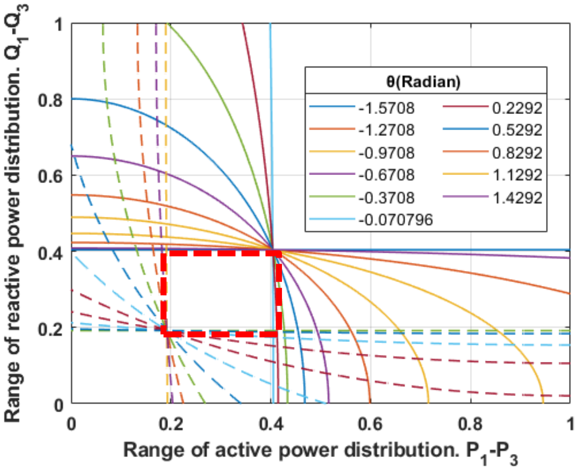


Figure 2-9 Power distribution ratio range when $V_{secondary}$ =40V & V_{PCC}=56.5V

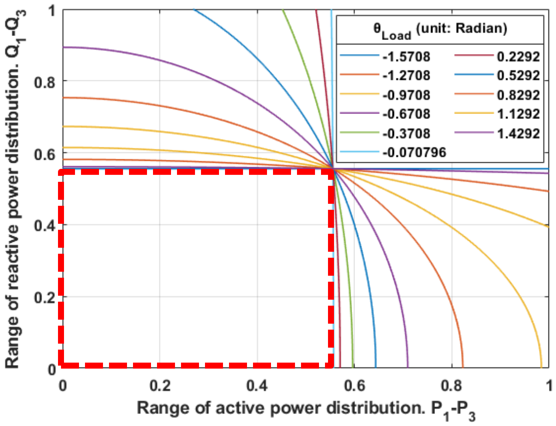


Figure 2-10 Power distribution ratio range when $V_{secondary}$ =55V & V_{PCC}=56.5V

Suppose that each submodule's secondary side DC voltage $V_{\text{secondary}}$ is same and its peak output voltage less than $V_{\text{secondary}}$ as is shown in (2-26). By substituting (2-26), then (2-27) should be satisfied.

$$V_n = V_{PCC}\sqrt{(P_{nom(n)}cos(\theta_{load}))^2 + (Q_{nom(n)}sin(\theta_{load}))^2} \tag{2-24}$$

$$\begin{aligned} k_1(I_{1out}V_1\sin\varphi_1 - \frac{V_1^2}{\omega C_{out}^2}) &= k_2(I_{2out}V_2\sin\varphi_2 - \frac{V_2^2}{\omega C_{out}^2}) \\ &= k_3(I_{3out}V_3\sin\varphi_3 - \frac{V_3^2}{\omega C_{out}^2}) = \Delta\omega \end{aligned} \tag{2-25}$$

$$\sqrt{2}V_n \le V_{secondary} \tag{2-26}$$

$$P_{nom(n)}^2 \cos^2\theta_{load} + Q_{nom(n)}^2 \sin^2\theta_{load} \le \frac{V_{secondary}}{2V_{pcc}^2} \tag{2-27}$$

$$\left|\sum_{k\neq n} \vec{V_k}\right|_{max} = \sqrt{2}(N-1)V_n \ge \sqrt{2}V_{PCC} - V_{secondary} \quad N = 3 \tag{2-28}$$

$$P_{nom(n)}^2 \cos^2\theta_{load} + Q_{nom(n)}^2 \sin^2\theta_{load} \ge (\frac{\sqrt{2}V_{PCC} - V_{sec}}{\sqrt{2}(N-1)V_{second}})^2 \tag{2-29}$$

Moreover, the sum of (N-1) submodule's maximum voltage should be satisfied with the boundary set in (2-28) to ensure the rest submodule's peak output voltage is less than $V_{\text{secondary}}$. Then (2-29) can be derived based on (2-28). If the dead time effect is considered, the maximum voltage utilization should be less than 1. Considering the inequality equation, Figure 2-9 and Figure 2-10 demonstrate the range of power distribution ratio under the condition that $V_{\text{secondary}}$ is 40V and 55V respectively. The area in the red dash line boxes are suitable for all the inductive, conductive, and resistive load conditions. $P_{\text{nom(n)}}$ and $Q_{\text{nom(n)}}$ of different submodules should be with in this region. For instance, when $V_{\text{secondary}}$ is set to 40V, all three submodules' active power and reactive power distribution ratio should be larger than 0.2 and less than 0.4. When $V_{\text{secondary}}$ increases, the area of power distribution ratio also enlarges as well. This conclusion is consistent with common sense: the higher $V_{\text{secondary}}$ is, the higher V_{out} can be realized. As a result, a higher power can be produced by the specific submodule.

2.5 Simulation and Experiment Verification

2.5.1 Simulation Verification

A simulation model of CMI system with three submodules in series is built with PLECS to verify the proposed methods, with the circuit configuration given in Figure 2-11. The key parameters are listed in Table 2-2. P_{nom1}, P_{nom2}, P_{nom3} and Q_{nom1}, Q_{nom2}, Q_{nom3}, are the power distribution setting ratio among three submodules.

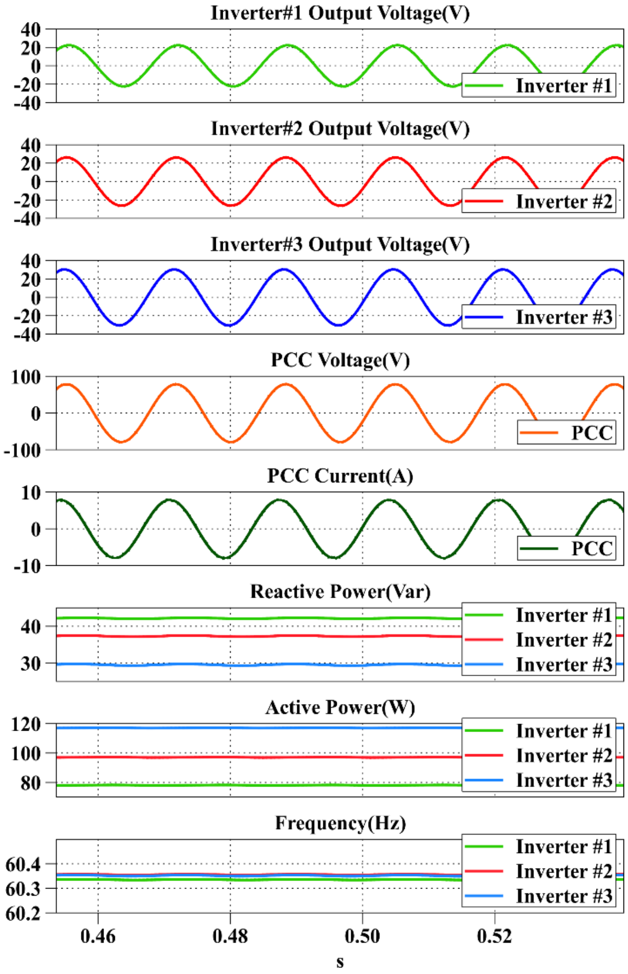


Figure 2-11 Simulation result at steady state

Figure 2-11 shows the simulation results of steady state under the condition that P_{nom1}:P_{nom2}:P_{nom3} is set as $\frac{0.8}{3}:\frac{1}{3}:\frac{1.2}{3}$, and Q_{nom1}:Q_{nom2}:Q_{nom3} is set as $\frac{1.2}{3}:\frac{1}{3}:\frac{0.8}{3}$, with the PCC voltage at 56.5V/60Hz. The total active power is set as 320W and the total reactive power is 100Var. It can be observed that the active power of submodule#1 to submodule#3 are perfectly controlled to be 78.0W, 96.9W, and 117.0W respectively and the reactive power of submodule#1 to submodule#3 to be 42.2Var, 37.4Var, and 29.6Var. The total active and reactive power of the simulation are 291.9W and 109.2Var respectively. The PCC voltage is around 55.29V/60.3Hz which is about 1.3V different from the setting value. The active power distribution ratio of the simulation is 0.805:1:1.207 and the reactive power distribution ratio of the simulation is 1.16:1:0.791 which is quite close to the setting value, which proves the proposed strategy has good accuracy and feasibility.

Figure 2-12 shows the simulation result that active power load switches back and forth between 0W and 320W while reactive power maintains to be 180Var. The active and reactive power distribution ratio of submodule#1 to submodule#3 are set as 0.8:1:1.2 and 1.2:1:0.8 respectively. The PCC voltage is set as 56.56V/60Hz. As is shown in Figure 2-12, at t_1, the active power switches from 0W to 320W. The PCC voltage can keep the same value while the output voltage of submodule#1 to submodule#3 changes accordingly. At t_2, the active power switches from 320W to 0W, and the PCC voltage still remains unchanged as well. This proves that the proposed control method can deal with sudden load change while achieving good active power distribution.

Figure 2-13 shows the simulation result that the reactive power load switches back and forth between 0Var and 180Var while the active power remains stable. The active and reactive power distribution ratio of submodule#1 to submodule#3 are set as 0.8:1:1.2 and 1.2:1:0.8 respectively. The PCC voltage is set as 56.56V/60Hz. At t_1, the reactive power switches from 180Var to 0Var, and the PCC voltage amplitude is immune to the change while the frequency gradually decreases to 60Hz. At t_2, the reactive power switches from 0Var to 180Var, and the PCC voltage amplitude also shows no influence while the frequency increases from 60Hz to 60.6Hz.

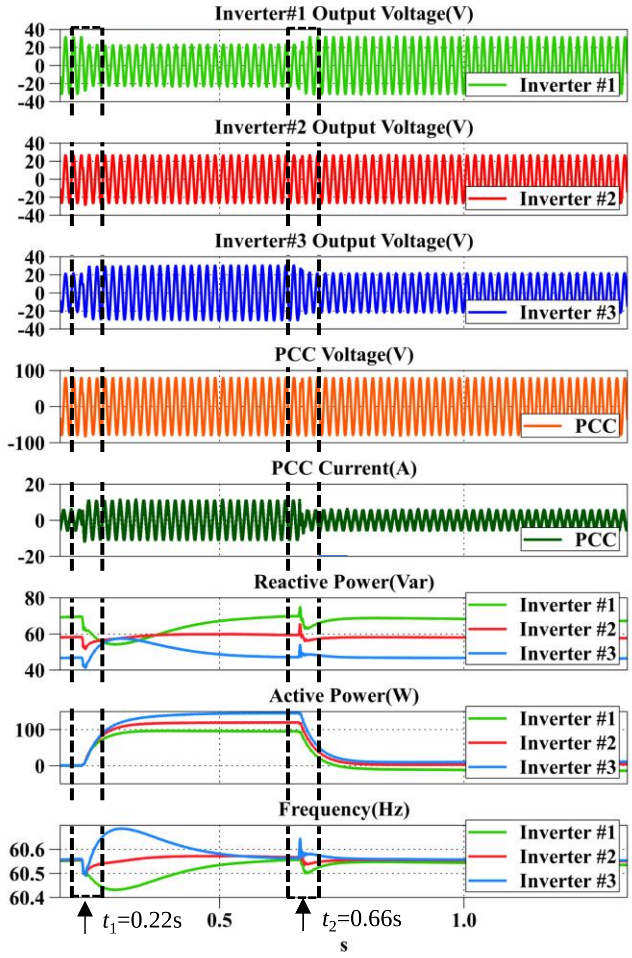
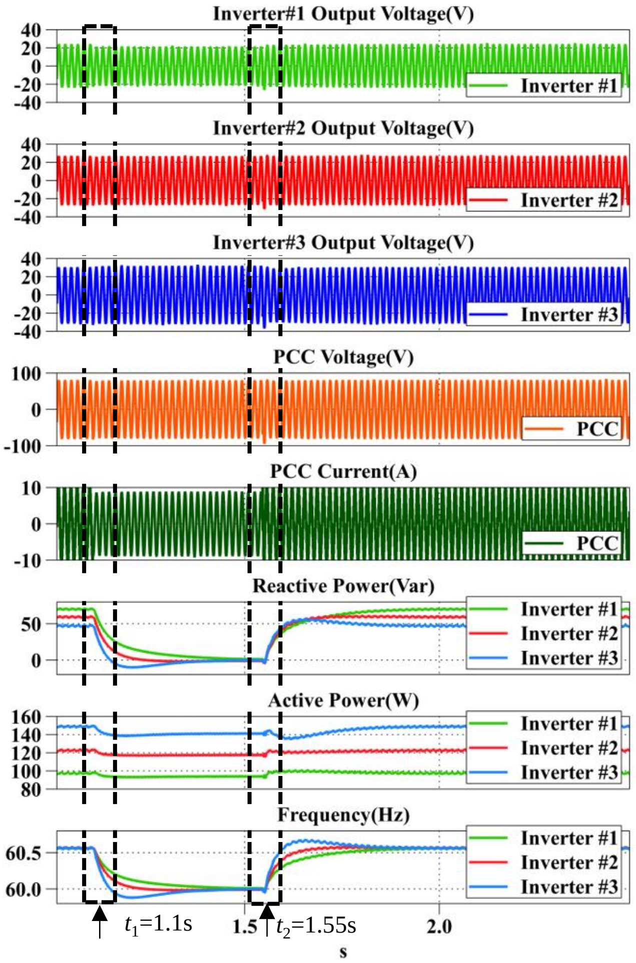


Figure 2-12 Simulation result for active power load switching back and forth

Figure 2-14 shows the dynamic simulation results when the power distribution ratio changes while the total output power and PCC voltage are kept the same. The total active and reactive power are set as 320W and 180Var respectively. Before t_1, the active and reactive power distribution ratio between submodule#1 to submodule#3 are set as 0.8:1:1.2 and 1.2:1:0.8 respectively. At t_1, both active and reactive power distribution ratios are switched to 1:1:1. At t_2, the active and reactive power distribution ratios become 0.8:1:1.2 simultaneously. Finally, the active and reactive power distribution ratio switches to 1.2:1:0.8 and 0.8:1:1.2 respectively. The PCC voltage is totally immune to the dynamic process during the whole power distribution ratio changes, which further illustrates the effectiveness of the proposed method.



Inverter#1 Output Voltage(V)

Inverter#2 Output Voltage(V)

Inverter#3 Output Voltage(V)

PCC Voltage(V)

PCC Current(A)

Reactive Power(Var)

Active Power(W)

Frequency(Hz)

Figure 2-13 Simulation result for reactive power load switching back and forth.

2.5.2 Experiment Result

The laboratory setup of CCM system with 3 submodules in series is shown in Figure 2-15. As we can see in this setup, each submodule contains a power board and a control board. The control board is formed with a sampling board and a control card with DSP28335. The specification of DC source and power load are 6260-80 and 63800 respectively from Chroma Corporation. All the waveforms are recorded by a 5 Series MSO oscilloscope from Tektronix Corporation. It should be mentioned that the active power, reactive power, and frequency shown in the experiment waveforms are calculated by math function of this oscilloscope. To filter out the second-order harmonic component of instantaneous calculated power, a low pass filter is added into the math function. The hardware parameters of each submodule are shown in Table 2-2.

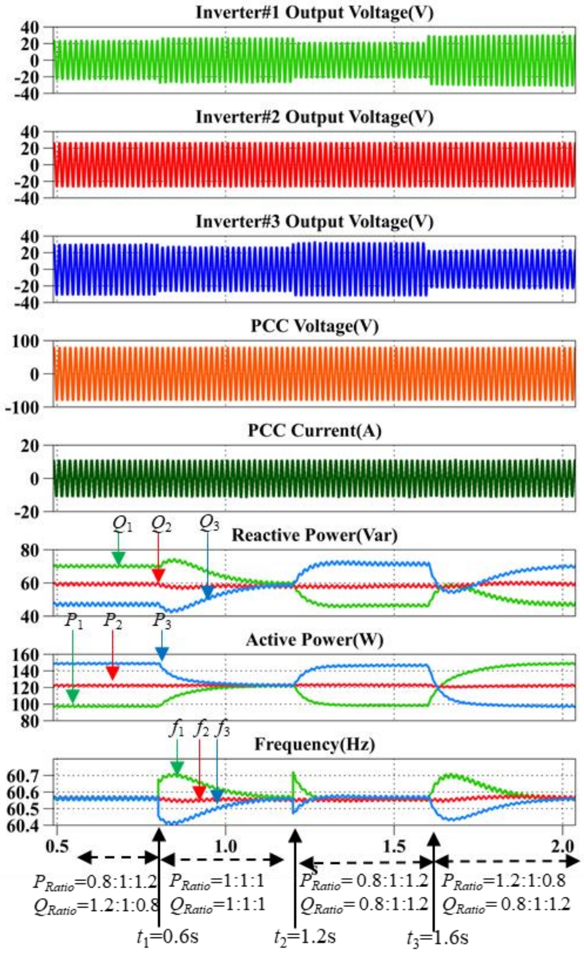


Figure 2-14 Dynamic result that the power distribution ratio changes.

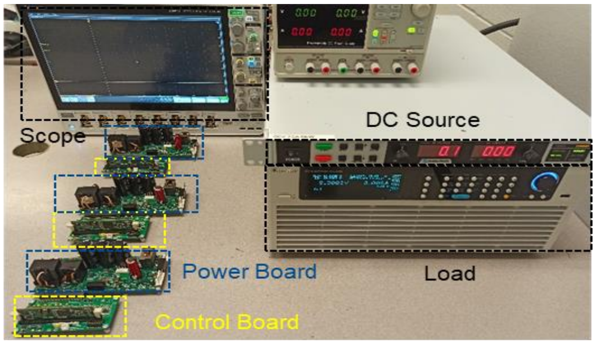


Figure 2-15 Laboratory setup for experimental verification.

Similar with simulations, Figure 2-15 shows the experiment results at steady state under the condition that P_{nom1}:P_{nom2}:P_{nom3} is set as $\frac{1.2}{3}:\frac{1}{3}:\frac{0.8}{3}$,and Q_{nom1}:Q_{nom2}:Q_{nom3} is also set as $\frac{1}{3}:\frac{1}{3}:\frac{1}{3}$. The experimental results show that the real power of submodule#1 to submodule#3 are 105.7W, 86.64W, 67.07W respectively. The power distribution ratio of active power is around 1.23:1:0.788, which shows a little difference with the setting value. The reactive power distribution ratio is also slightly different within submodules too. Despite a nominal 2% difference, I consider this variance acceptable, especially within the context of hundred-watt power levels. The PCC voltage is around 57.5V/60.5Hz, which is just 0.92V bias from the setting value. There are several reasons for the slight error between the experimental result and the setting value. On the one hand, the precision of current ADC data is not high enough with small submodule's inductor and large current ripple, which will introduce switching-frequency level noise into the ADC circuits. On the other hand, the H-bridge side current is sampled instead of the PCC side current, which will decrease the accuracy of power calculation.

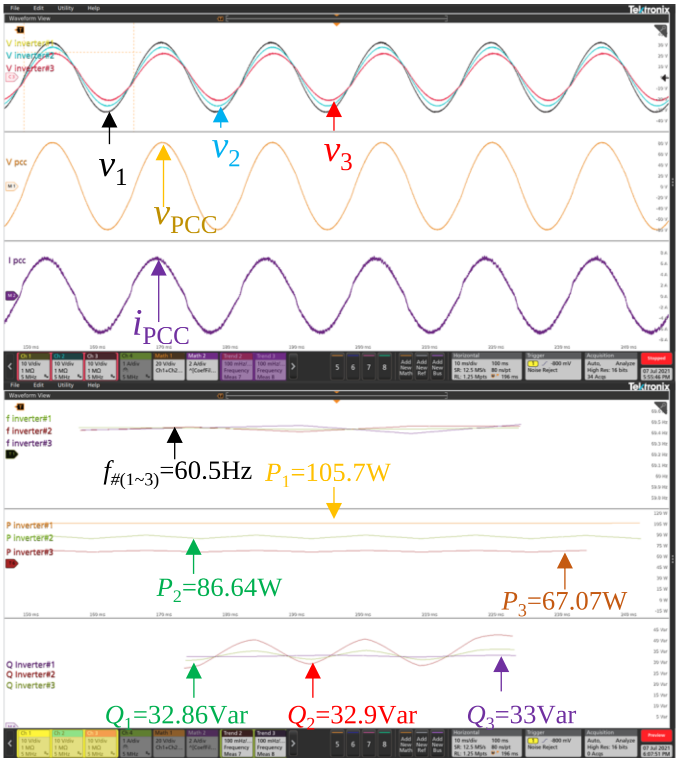


Figure 2-15 Experiment result at steady state under the condition that P_{nom1}:P_{nom2}:P_{nom3}=1.2:1:0.8 & Q_{nom1}:Q_{nom2}:Q_{nom3}=1:1:1

Figure 2-16 shows the experiment results when load switches from 260W/110Var to 130W/110Var and vice versa. Here, only active power is switched while reactive power is kept the same. The power distribution ratio of active power and reactive power are set as $\frac{1.2}{3}:\frac{1}{3}:\frac{0.8}{3}$ and $\frac{1}{3}:\frac{1}{3}:\frac{1}{3}$ respectively. At the steady state, the reactive power ratio is nearly the same all the time while the active power distribution ratio switches from 1.23:1:0.74 to 1.23:1:0.78. As can been observed in Figure 2-16, the PCC point voltage is not influenced at all during load switching, which proves that the PR controller can largely decrease the response time of the whole system. Since the PCC point frequency is only related to reactive power, the frequency also remains constant at the steady state around 60.45Hz. However, the angular frequency ω_n shakes during active power switching at t_1 and t_2, which is mainly caused by the calculation method of reactive power Q_n. According to Figure 2-16, the angular frequency change rate $\Delta\omega_{\underline{n}}/\Delta t$ is the output of the high pass filter and with the input to be reactive power Q_n. Therefore, the calculated reactive power Q_n will directly influence the dynamic response of ω_n.

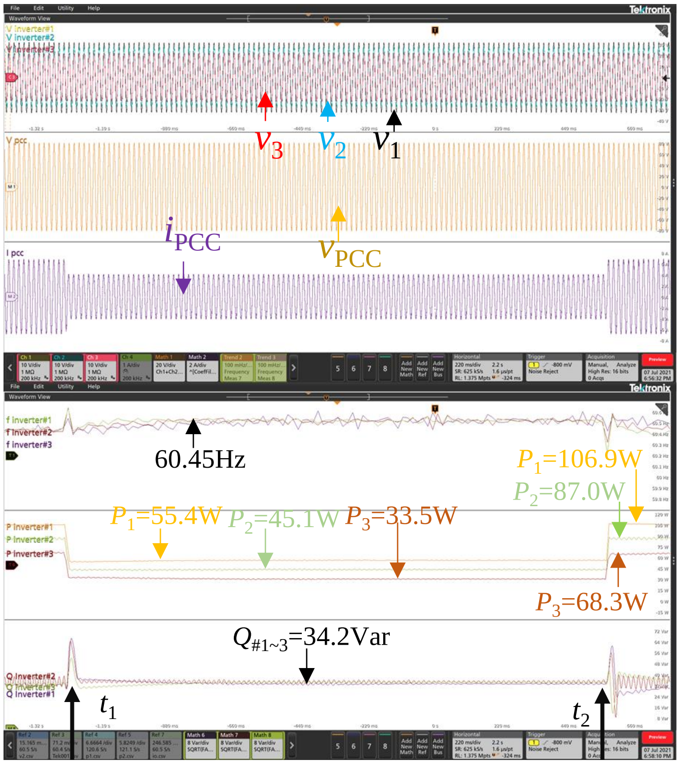


Figure 2-16 Experiment results when active power switches back and forth

Figure 2-17 shows the experimental waveforms when loading switches from 260W/110Var to 260W/46Var and vice versa. Only reactive power is switched while active the power is kept the same. The ratio of active power and reactive power are also set as $\frac{1.2}{3}:\frac{1}{3}:\frac{0.8}{3}$ and $\frac{1}{3}:\frac{1}{3}:\frac{1}{3}$ respectively. In addition, the PCC point voltage is also not influenced at all during load switching.

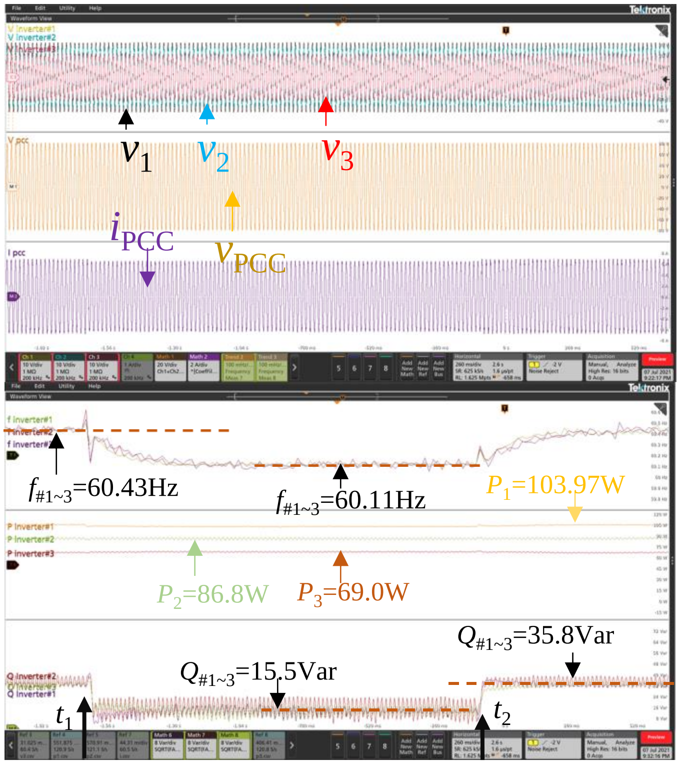


Figure 2-17 Experiment results when reactive power switches back and forth

Figure 2-18 shows the experiment results when the power distribution ratio switches. Before t_1, the active and reactive power distribution ratios are set as 1.2:1:0.8 and 0.8:1:1.2 respectively. At t_1, the active and reactive power distribution ratios are all switched to 1:1:1 simultaneously. Then the active power and reactive power distribution ratios switch to 0.8:1:1.2 and 1.2:1:0.8 respectively at t_2. Finally, the active power and reactive power distribution proportion are switched back to 1.2:1:0.8 and 0.8:1:1.2 respectively at t_3. The PCC point of voltage is immune to the distribution ratio change all the time, which is 56.5V/60.3Hz. All the above results clearly verifies the effectiveness of the proposed control method which can distribute the active and reactive power in a wide range and keep them totally decoupled and separated simultaneously.

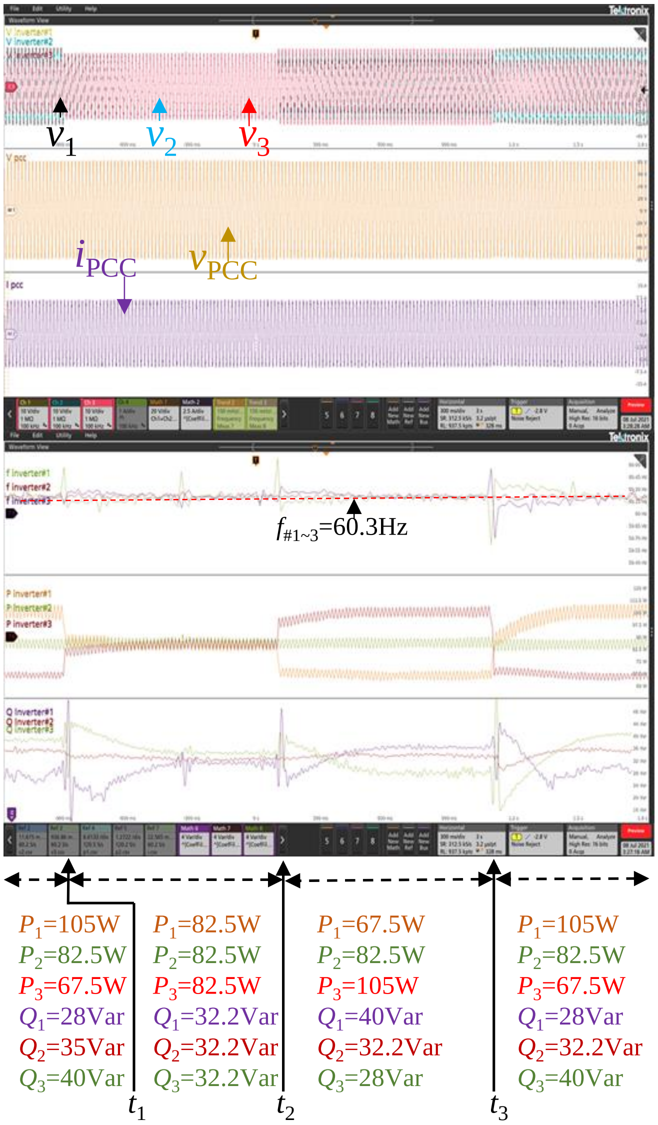


Figure 2-18 Experiment results when power distribution ratio switches

2.6 Conclusion

This chapter extends the study of the inverse droop control method that has been adopted in CCM system application under islanded mode. Although the previous work can successfully solve the multiple equilibrium points issue, the active power and reactive power distribution of different submodules have to be kept in a fixed ratio, i.e. the active and reactive power can't be arbitrarily distributed. In this chapter, the active and reactive power of the different submodules can be arbitrarily distributed in a wide range, which means the power distribution are fully decoupled. This paper also provides the boundary of the power distribution range and proves the stability of the whole system. Moreover, the feasibility of the proposed control method has been verified by the simulation results and hardware prototype experimental results.

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CHAPTER 3

A FAMLILY OF NOVEL DC-DC CONVERTER FOR DATA CENTER APPLICATION

3.1 Introduction

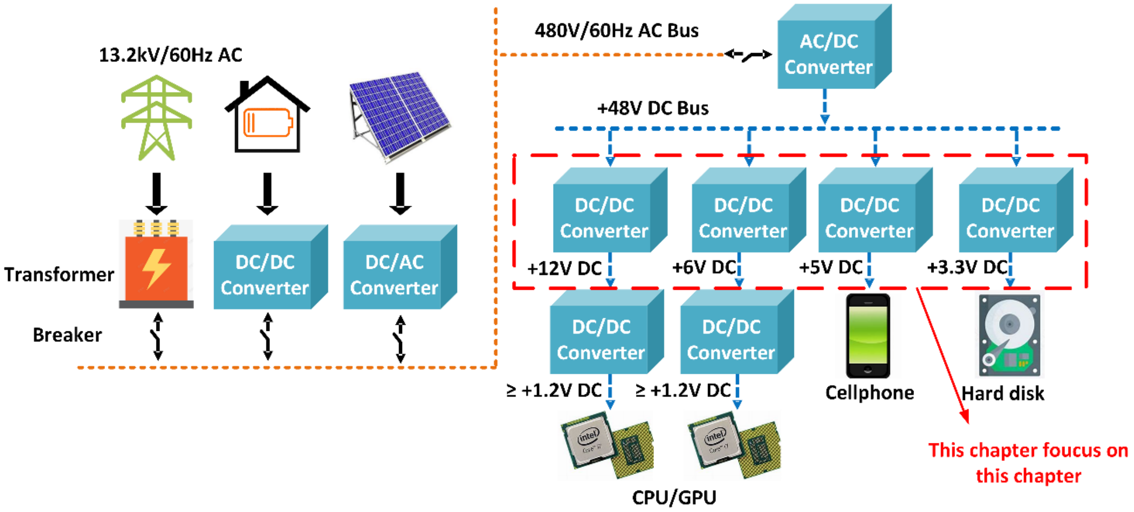


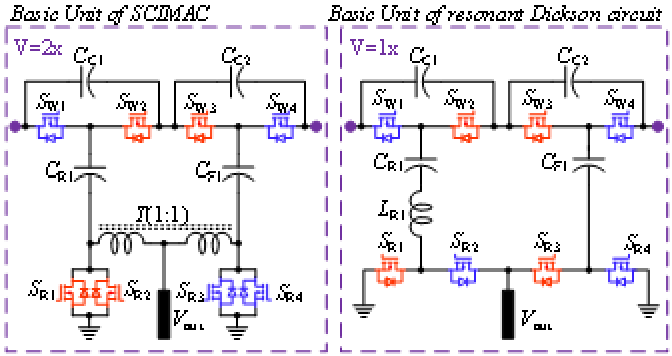
Figure 3-1 This chapter focuses on the Family of Matrix Autotransformer LLC Converter

Switched tank converter(STC) is a good candidate for low voltage application like Data Center application due to its high efficiency and power density [1]-[4], and it belongs to one kind of resonant switched capacitor converter(ReSC). STC is usually adopted as intermediate bus converter (IBC), i.e. 12V with very high efficiency, and there are also some other topologies that can realize nearly 99% power efficiency for 12V DC bus structure as well [5]-[7]. With the development of the Artificial Intelligence (AI) and machining learning, lower CPU voltage is highly required. Early in 2000, CPU with 1.8V on average can already realize high performance but now, it requires CPU with 0.8V to perform heavy computation task [8]. As a result, the IBC with 12V is not suitable anymore, instead, lower intermediate DC bus voltage is needed to decrease conversion ratio of the point of load(POL) stage and the whole system efficiency can be improved as a result [9]. On the other hand, LLC converter can also realize high efficiency and high conversion ratio [21]-[17]. The power efficiency of LLC converter is lower than STC or other ReSC converters in the light or medium load since the transformer’s core loss accounts a large part among the total power loss, while the power efficiency of LLC converter is higher in heavy load since the conduction loss dominates. As a result, there are two main trends which are divided into ReSC converters and LLC converters to develop the IBC for Data Center application. Moreover, there also appears a new method that merges both IBC stage and POL stage together [10]-[14], and the soft charging technology [15]-[16] is realized by the buck inductor in the POL stage. By this way, not only high efficiency and very high-power density can be realized, but also the current spike issue of switched capacitor converter can be overcome. On the other hand, the LLC converter with matrix transformer also tries to directly convert 48V to 1V in one stage[20].

Therefore, one idea that adopts autotransformer to merge the benefits of both LLC converter and ReSC has been proposed for the IBC of data center application. There are several reasons for the autotransformer-based converter solution: 1) Isolation is not necessary [2], so primary side windings of LLC converter can be removed to increase power efficiency; 2) The resistance of winding is lower than semiconductor devices. In other words, the total conduction loss of LLC converter is lower than ReSC converter’s in heavy load, and this is very important for high current application area since the conduction loss dominates. 3)The low figure of merit (FOM) devices can be adopted to increase the power efficiency. LLC converter requires higher FOM devices while the ReSC converter can adopt lower one. As a result, the autotransformer-based converter solution can further increase the power efficiency. Different kinds of autotransformers based LLC converters are proposed in [21], and the switch capacitor combined with autotransformer converters are proposed in [22]-[23]. However, the winding turns of the circuit are not the same, and it’s difficult to extend the conversion ratio unless more independent inductors are added in the circuit[24].

In this paper, a family of Switch Capacitor based Integrated Matrix Autotransformer LLC Converters(SCIMAC) is proposed. It takes the advantage of both LLC converter and STC: 1). The conduction loss of the transformer's primary side is saved. 2). Resonant inductors are integrated into the matrix autotransformer, so the conduction loss of the resonant inductors is also saved. 3). Low FOM devices are adopted due to the low voltage stress of the switches compared with LLC converter. 4). ZVS turning on can be realized by the magnetizing current in full load range. A 9x conversion ratio DC-DC prototype is built to show the feasibility of these proposed circuits. And the calculated power efficiency with 9x is up to 99% at 270W. Section II shows the family of the proposed circuits. Section III shows the simulation result. The prototype is in built to verify the feasibility of the proposed topology.

3.2 The Family of the SCIMAC



(A) The basic unit of SCIMAC (B) The basic unit of Dickson converter

Figure 3-2 The basic unit of SCIMAC and Dickson converter

Figure 3-2 shows the basic unit of the SCIMAC and resonant Dickson circuit. The C_{R1} means the resonant capacitor and the C_{F1} means the non-resonant capacitors which should be 10 times larger than resonant capacitor. The voltage stress of switches shown in Figure 3-2(A) is equal to $2\times V_{out}$, which can be named as 2x, and the voltage stress of switches shown in Figure 3-2 (B) is equal to V_{out}, which can be named as 1x. Moreover, the current RMS stress of all the switches shown in both Figure 3-2(A) and Figure 3-2(B) is input RMS current-I_{input}, which is named as 1x. However, the basic unit of SCIMAC can realize 4:1 while the basic unit of Dickson converter realizes 2:1. Therefore, if the high voltage side switches S_{w2} and S_{w3} in Figure 3-2 are merged together, the 4:1 STC converter is shown in Figure 3-3 while the 4:1 SCIMAC is shown in Figure 3-4.

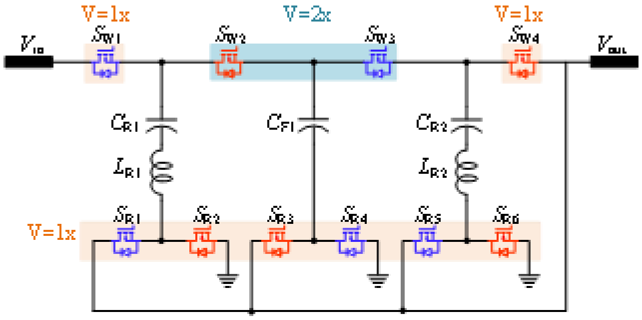


Figure 3-3 The 4:1 Dickson converter

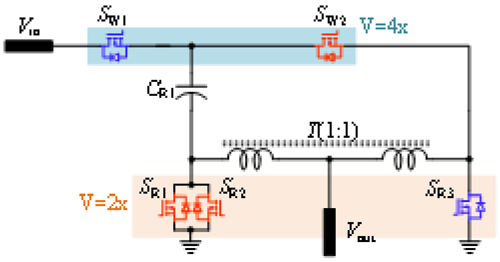


Figure 3-4 The 4:1 SCIMAC

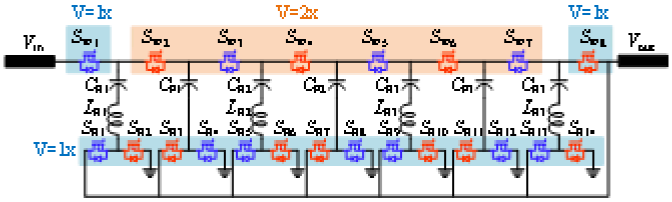


Figure 3-5 The 8:1 STC converter

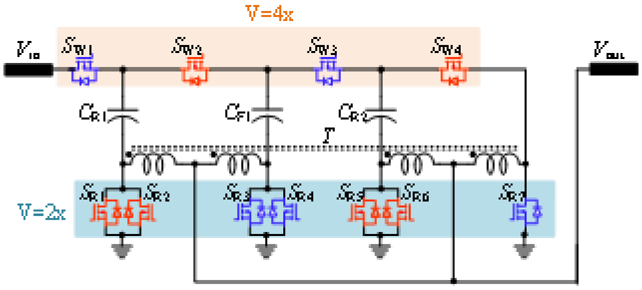


Figure 3-6 The 8:1 SCIMAC

For 8x conversion ratio, the STC converter is shown in Figure 3-5, the voltage stress of majority high voltage side switches is 2x while the voltage stress of low voltage side switches is 1x. The 8:1 SCIMAC is shown in Figure 3-6, the voltage stress of high voltage side switches is 4x while the voltage stress of low voltage side switches is 2x. Although both the two kinds of circuits can realize 8:1, the switches counts of SCIMAC are just half of the STC while the voltage stress is doubled.

Figure 3-7 shows the 16:1 SCIMAC, and all the windings are also just one turn. The voltage stress of both high voltage side switches and low voltage side switches are the same as 8:1 SCIMAC.

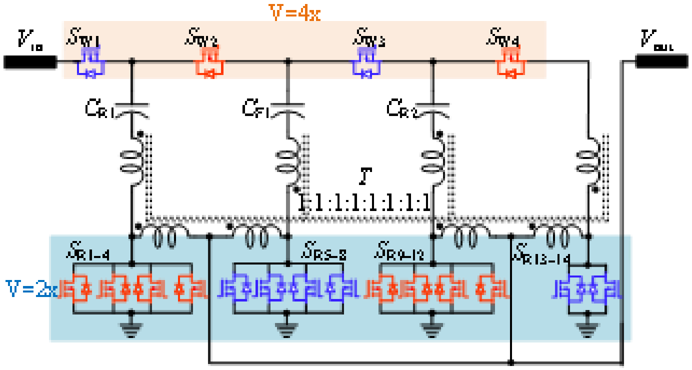


Figure 3-7 The 16:1 SCIMAC

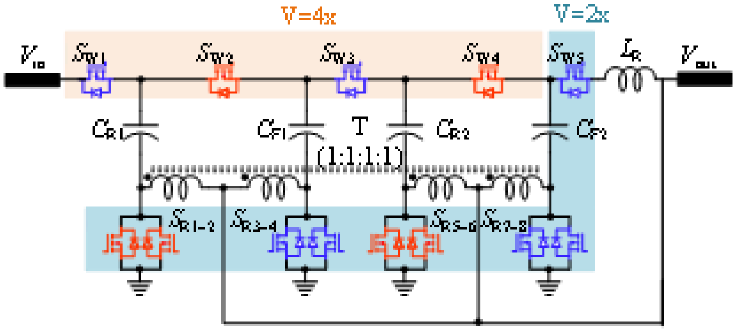


Figure 3-8 The 9:1 SCIMAC

For the conversion ratio as 4N can add more modules like Figure 3-6 does or more wingdings on the capacitor branch like Figure 3-7 does. For the converter that the conversion ratio is 4N+1, an additional independent L_R is required to make all the current loops realize soft switching which is shown in Figure 3-8. If the 17:1 is required, another basic unit of SCIMAC in Figure 3-2(A) is required to add into the circuit.

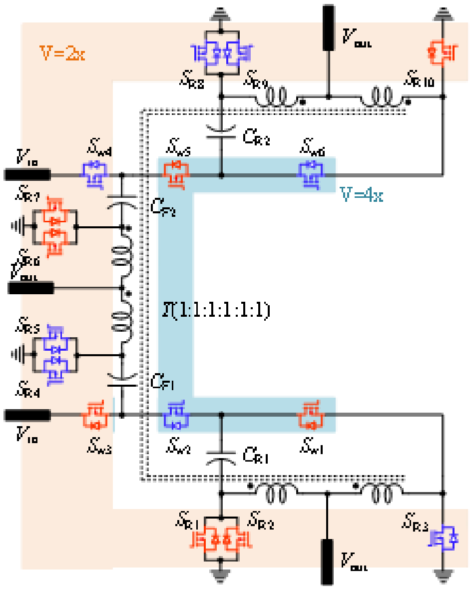


Figure 3-9 The 6:1 interleaved SCIMAC

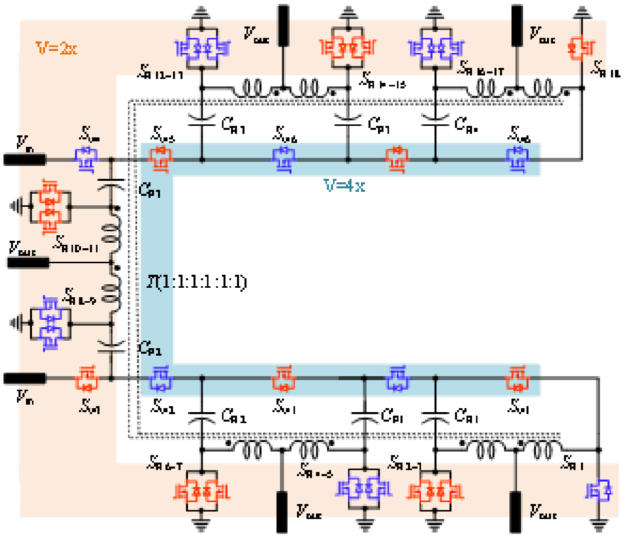


Figure 3-10 The 10:1 interleaved SCIMAC

For the converter that the conversion ratio is 4N+2, an interleaved SCIMAC converter is proposed which is shown in Figure 3-9 and Figure 3-10. For the converter that the conversion ratio is 4N+3, the circuit topology as Figure 3-11 can be adopted. It should be pointed out that all circuits descripted in this paper can realize ZCS switching. The converter that the conversion ratio is 4N+2 or 4N+3, the two-phase interleaved SCIMAC is required. Furthermore, the converter with the conversion ratio as 4N+1 or 4N+3 needs extra independent inductors which is labeled as L_R in the circuit. Moreover, all the windings of the transformer can be merged into one core, and the resonant inductors are also integrated into the core except the independent inductors L_R. The current stress of all the switches in this paper are the same, which is equal to input current RMS value. If higher conversion is needed, we just need to add the basic unit of SCIMAC in Figure 3-2(A) to the specific conversion ratio type. For example, for the converter with 4N+2 conversion ratio, one more basic unit of SCIMAC is added into the circuit when the 6:1 converter and 10:1 converter are compared.

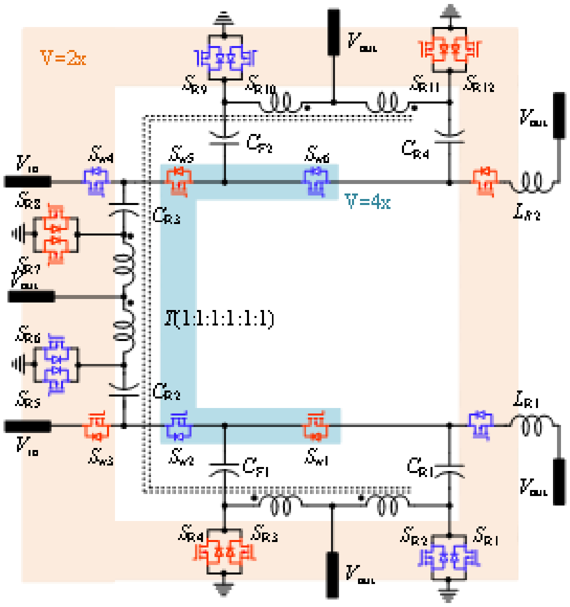


Figure 3-11 The 7:1 interleaved SCIMAC

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CHAPTER 4

A NOVEL 8X MATRIX AUTOTRANSFORMER SWITCHED CAPACTIOR DC-DC CONVERTER

4.1 Introduction

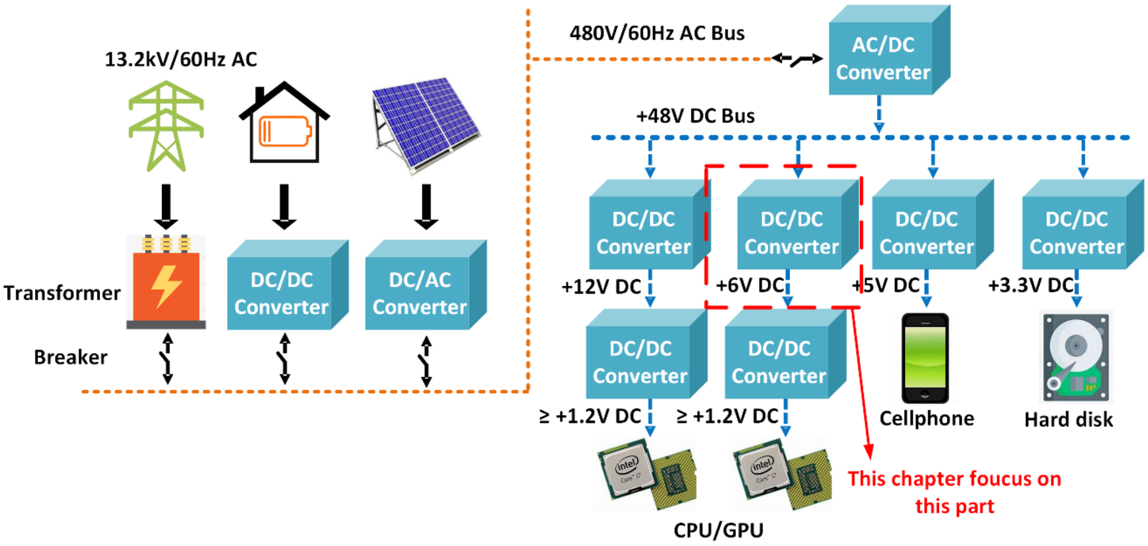

Figure 4-1 This chapter mainly focuses on the 8x MASC

With the development of artificial intelligence (AI), cloud computing, and mobile internet, a growing number of data-centers have been built all over the world[1]-[2]. Switched tank converter(STC) is a good candidate for Data Center application derived from Dickson converter due to the high efficiency and high power density [3]-[7], and it is usually adopted as intermediate bus converter. Moreover, there are many other resonant Dickson based switched capacitors that can realize very high performance [8]-[15]. However, the low voltage side of the Dickson based converter like STC utilizes full bridge rectifier with two switches conducting current simultaneously, which would cause high power loss under high-current, low-voltage application. And due to the limitation of the semiconductor technology on the low voltage devices, it is overkill to use the full bridge rectifier. On the other hand, the LLC converter that adopts transformer with current doubler circuit reduces the use of the semiconductor device by one [16]-[20], and only utilize one switch with doubled voltage stress to conduct the current. In order to utilize the benefits of the STC and the LLC converter together, this paper proposes the MASC which features at sharing the same high voltage side circuit of the STC and the same low voltage side circuit as LLC's. Different from the traditional LLC converter with an isolated transformer, the proposed MASC utilizes one autotransformer with only the secondary side windings similar to LLC's secondary side. Therefore, it further increases efficiency of the traditional STC.

4.2 THE Derivation of the Proposed MASC

Figure 4-2 shows the derivation of proposed converter from the STC. On the low voltage side, Figure 4-3 changes the full bridge to the current doubler circuits shown in Figure 4-3, which is the proposed 8x MASC. Taking the 8x(48V-6V), 300W,300kHz converter as an example, Figure 4-2 adopts 14 devices with voltage stress as 6V while Figure 4-3 adopts 7 devices with voltage stress as 12V on the low voltage side. Therefore, we should adopt blocking voltage of 10V or 15V devices for Figure 4-2 and adopt 20V or 25V blocking voltage devices for Figure 4-3. To clearly compare circuits shown in Figure 4-2 and Figure 4-3, a method called total semiconductor loss index (TSLI) is adopted [21]. The device's total gate charge Q_g as well as output capacitance C_{oss} is proportional to die area$Q_g = \beta A_{die}$, $C_{oss} = \alpha A_{die}$ and conduction resistance R_{ds} is inversely proportional to die area $R_{ds} = \xi / A_{die}$. β, α, ξ are only related to semiconductor's technology. Then TSLI can be expressed as $TSLI = (\frac{I_{RMS}^2 \cdot \xi}{A_{die}} + \beta A_{die} V_g f + \alpha A_{die} f V_{coss}^2) \times N / P_{IN}$, where I_{RMS} represents the RMS current through devices, V_g, P_{IN}, f , N are gate voltage, input power, frequency and total number of devices respectively. The TSLI of devices on the low side is shown in Figure 4-4. It can be obviously seen that circuit in Figure 4-3 realizes higher efficiency. Furthermore, all magnetic components including two transformers and inductors are merged into one core shown in Figure 4-7 and the specific core design isn't introduced here due to page limitation. By this method, the power density and efficiency can be further improved.

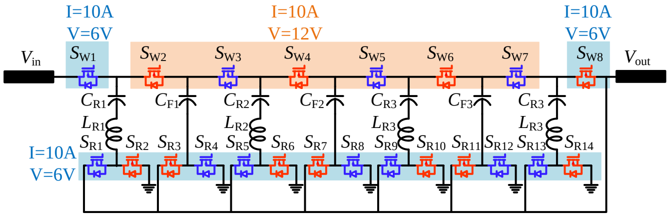

Figure 4-2 The 8x switched tank converter.

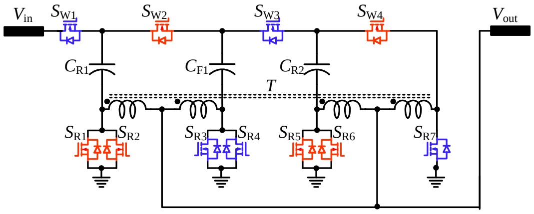

Figure 4-3 The proposed 8x MASC.

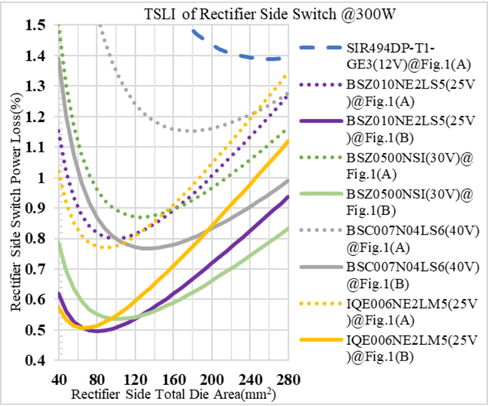

Figure 4-4 The TSLI of rectifier side switches.

4.3 Simulation and The Experimental Result

Figure 4-5 and Figure 4-6 show the current commutation loop of the MASC during two states. During state(A), the capacitors C_{R1} and C_{R2} are discharged while C_{F1} is charged, and vice versa for the state on Figure 4-6.

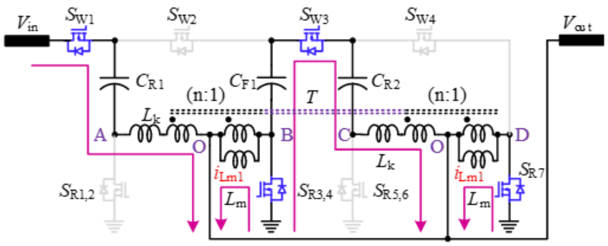

Figure 4-5 The current commutation when blue devices are on.

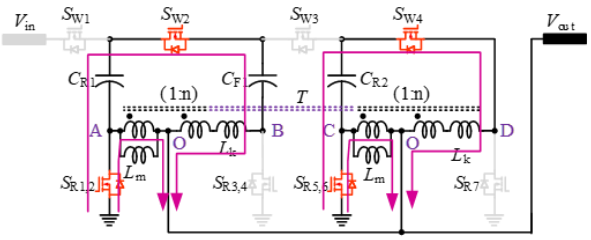

Figure 4-6 The current commutation when red devices are on.

Figure 4-8 shows the experimental result at heavy load-460W, and the voltage and current waveforms of the input and output port is shown in this figure. Figure 4-9 shows the current waveforms through capacitors C_{R1}~C_{R2} and C_{F1}, and the RMS current through the three capacitors is around 21.9A.

Table 4-1 The components for the proposed 8x MASC

V_{in}	46V~50V
V_{out}	5.75V~6.25V
P_{in}	500W
f	417kHz
C_{in}	22uF×6 (X7S,100V)-C5750X7S2A226M280KB
C_{out}	47uF×18(X5R,10V)-C4532X5R1A476M280KA
C_{F1}	22uF×3(X7R,50V)-C5750X7S2A226M280KB
C_{R1} & C_{R2}	1.4uF (U2J,50V)-C1812C145J5JLC7805
S_{R1}~S_{R7}	BSZ010NE2LS5ATMA1(25V,1mΩ)
S_{W1}~S_{W5}	BSC0500NSIATMA1(30V,1.3mΩ)
Core	ML95S@Hitachi Company

Figure 4-7 Prototype of the MASC and the core of the matrix autotransformer.

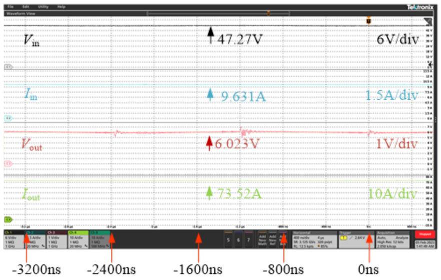

Figure 4-8 The current and voltage waveforms of the input and output.

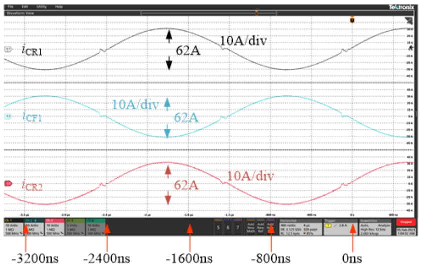

Figure 4-9 The current and voltage waveforms of the input and output.

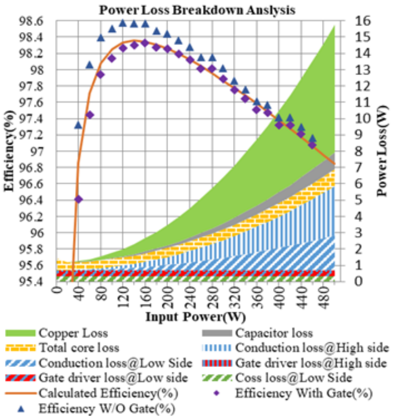

Figure 4-10 The efficiency analysis of 8x MASC.

Figure 4-10 shows the efficiency of the proposed MASC. The peak power efficiency is around 98.33% (gate driver loss included) at 160W, and it drops to 96.8%(gate driver loss included) at 500W. The power density of the proposed 8x MASC is 767.4W/in^3.

4.4 Conclusion

This chapter proposes a new circuit called MASC which can be derived from STC, and the reason that MASC can improve the power efficiency when compared with STC is explained from TSLI point of view. Moreover, the core that can integrated all inductors as well as transformers have been adopted. Both the simulation and experimental have been conducted to verify the feasibility of the proposed circuit.

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CHAPTER 5

THE MATRIX AUTOTRANSFORMER SWITCHED CAPACITOR DC-DC CONVERTER WITH PARTIAL POWER PROCESSING REGULATOR

5.1 Introduction

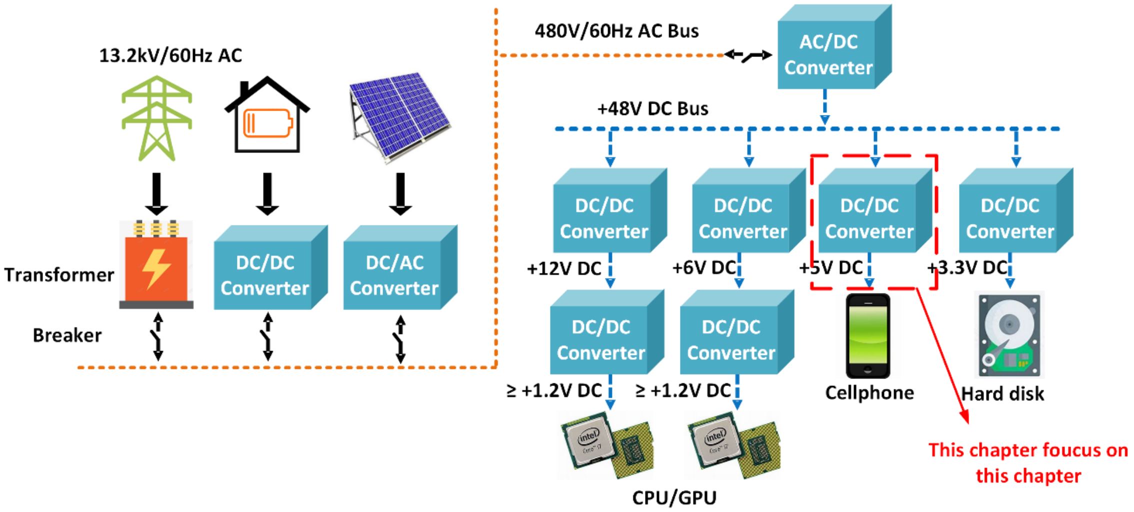


Figure 5-1 This chapter mainly focuses on the 48V to 5V partial power processing

This chapter focuses on the 48V to 5V partial power processing regulator which is shown on Figure 5-1. With the development of the Artificial Intelligence (AI), the power delivery system of data center gets more and more attention. Currently, a 48V typical data-center power system includes two stages: the first stage converts 48V DC bus to an intermediate DC bus voltage, i.e. 12V or 6V, and the second stage converts 12V or 6V to 1V~1.5V for chips. The 48V to 6V DC-DC converter for data center application has been studied in [1]–[5] and it can be mainly divided into LLC converter and resonant switched capacitor converter(ReSC). Moreover, the ReSC is very helpful for EMI attenuation [6]-[10] when compared with non-resonant switched capacitor converter. The power efficiency of the ReSC is far lower at heavy load than LLC converter in [1]–[3] since the current doubler circuit on LLC converter's secondary side only requires one switch conducted for its every current loop. Therefore, a new circuit called MASC shown in Figure 5-2 that merges current doubler circuit and switched capacitor circuit is adopted in this paper [11]. It features at using fewer switches on its low voltage side while adopting high figure of merit switches on its high voltage side, and the transformer's primary side windings can also be saved.

With respect to the partial power regulator circuit, sigma converter is proposed in [12] which is composed of LLC converter as well as buck converter. The LLC converter works at resonant frequency point to keep very high efficiency, while the buck converter works as regulation mode.

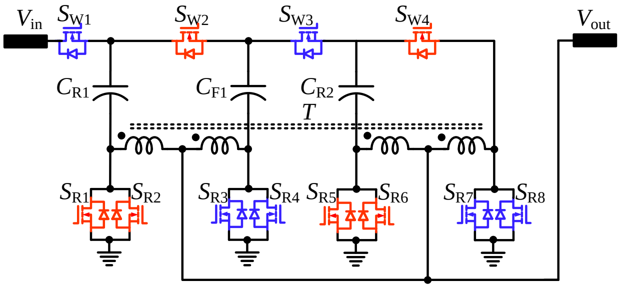


Figure 5-2 The 8x MASC converter

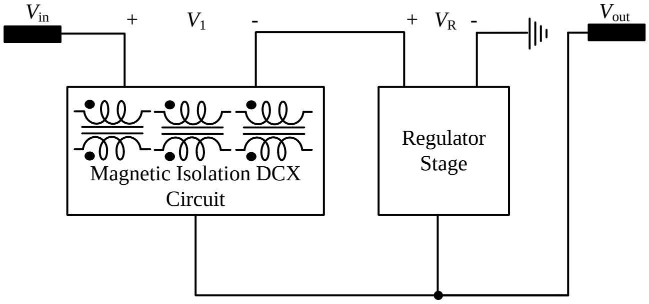


Figure 5-3 The circuit structure of sigma converter

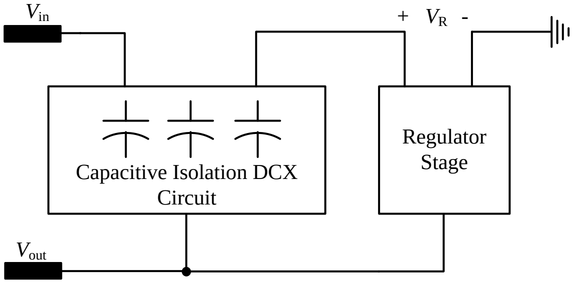


Figure 5-4 The circuit structure

On the other hand, paper [13] adopts the multilevel modular switched capacitor converter in series with regulated boost converter to realize inverter purpose [14]. Similarly, an 8x MASC converter as capacitive isolation DCX circuit and a buck converter as regulator is proposed shown in Figure 5-5. The 8x MASC works at resonant frequency point to keep very high efficiency, while the buck converter works under regulation mode.

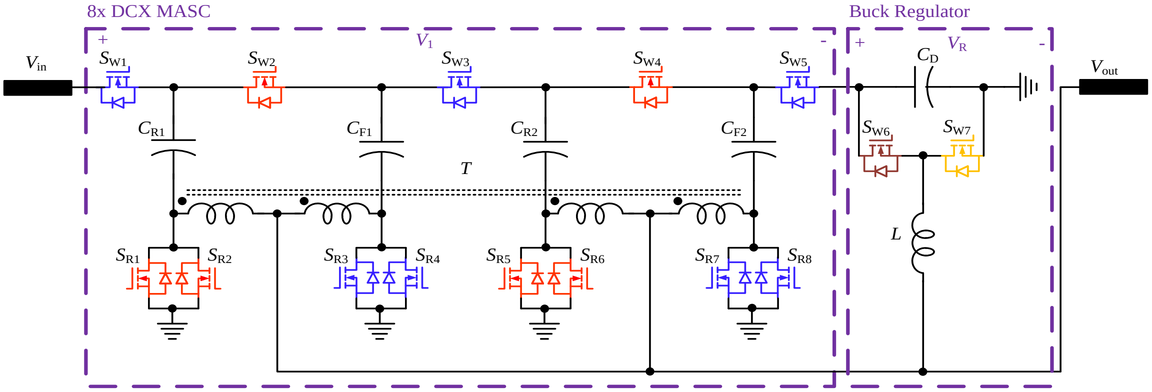


Figure 5-5 The proposed 8x MASC in series with buck regulator

5.2 The Working Principle of the 8X MASC with Buck Regulator

The derivation of the working principle of the 8x MASC is shown in this section. Assume input range is 45V~52V and the output voltage is 5V, then the high voltage side of 8x MASC V_1 in Figure 5-5 is 40V, and the high voltage side of buck regulator voltage V_R varies from 5V~12V which is depended on input voltage. The power processed by buck regulator is expressed as $P_{regulator}/P_{in}= V_R/V_{in}$, which changes from 11% to 23.1% accordingly. Suppose the duty cycle of switch S_{w6} is D, and the duty cycle of switch S_{w7} is (1-D). Then the power processed by 8x MASC to total power can be expressed in (5-1). Figure 5-6 shows the relationship between the power processed by 8x MASC and the input voltage. For example, when the input voltage is 48V, then around 83% power is processed by 8x MASC, while just 17% power is processed by buck regulator.

$$\frac{P_{MASC}}{P_{total}} = \frac{V_{in} - V_R}{V_{in}} = \frac{8V_{out}}{8V_{out} + \frac{V_{out}}{D}} = \frac{8D}{1 + 8D} \tag{5-1}$$

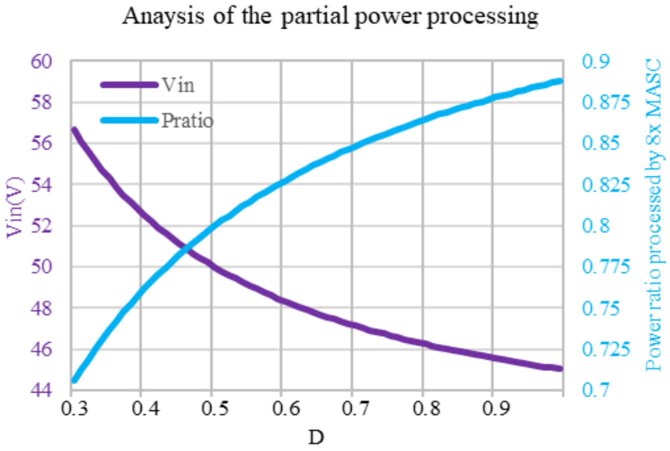


Figure 5-6 The power processed by 8x MASC with the change of input voltage

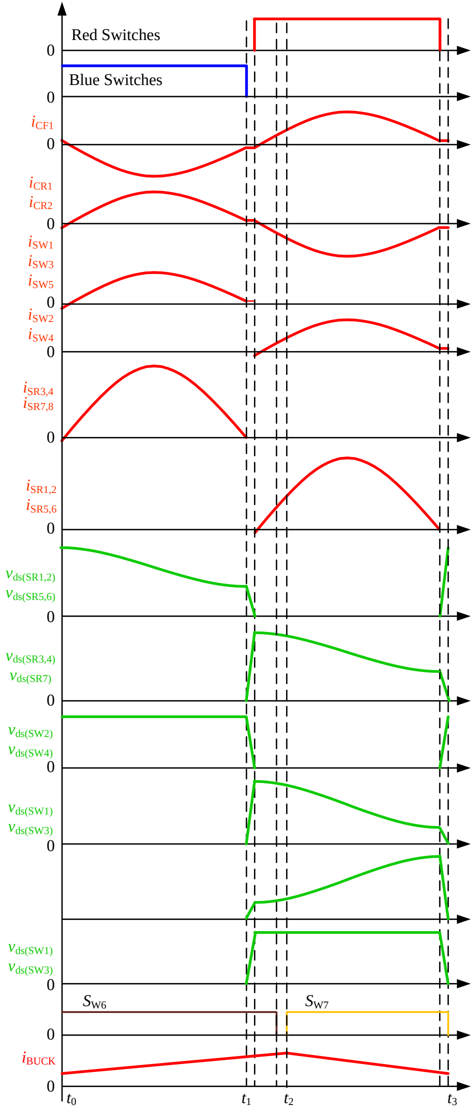
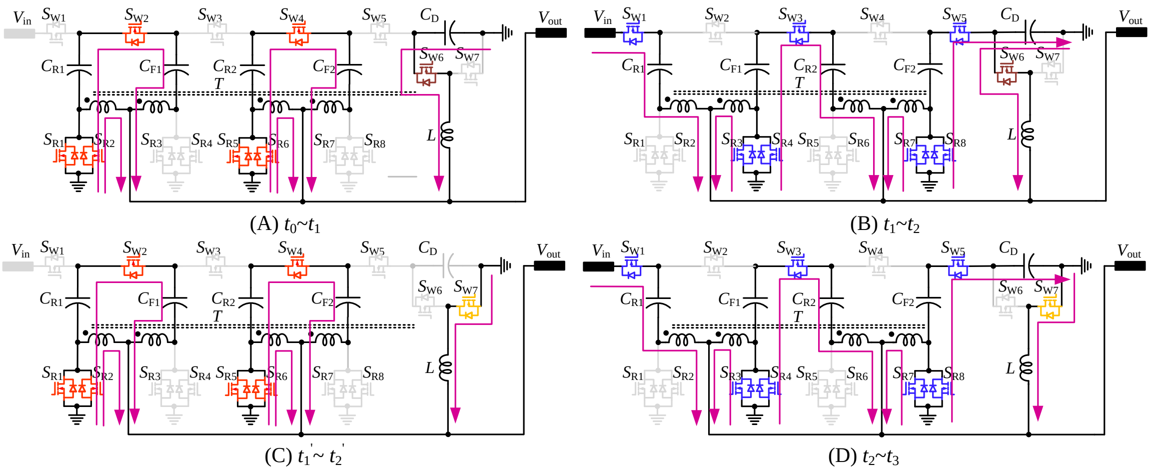


Figure 5-7 The working principal analysis during one period

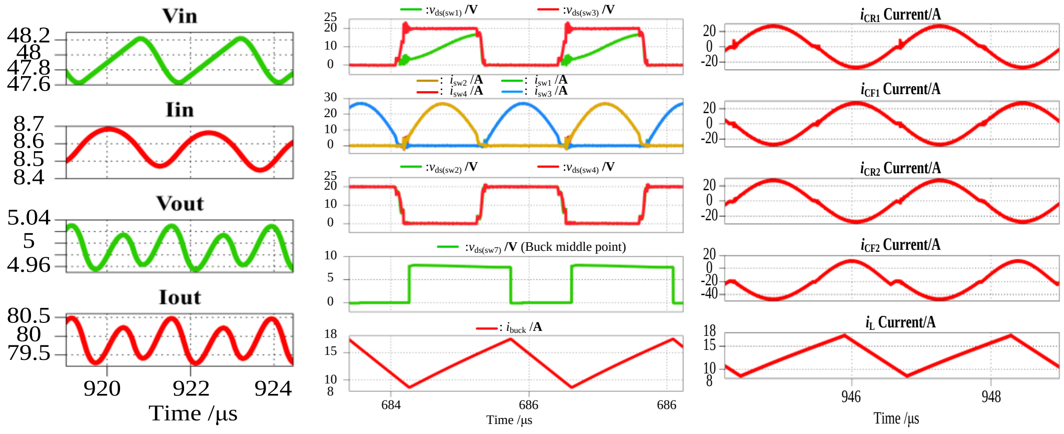


(A) t_0~t_1 (B) t_1~t_2

(C) t_1'~ t_2' (D) t_2~t_3

Figure 5-8 The circuit commutation loop of the 8x MASC with Buck Regulator

Figure 5-7 shows the working principal analysis during one period. For the 8x MASC, the switches duty cycle is always 50% if dead time is ignored. Figure 5-8 shows the circuit commutation loop of the proposed circuit. When the input voltage changes from 45V to 52V, the duty cycle D of switch S_{W6} changes from 1 to 0.416. Moreover, when the input voltage changes from 45V to 50V. The period t_0~t_1, t_1~t_2 and t_2~t_3 are expected. When the input voltage changes from 50V to 52V, the period t_0~t_1, t_1'~t_2' and t_2~t_3 are expected.



(A)Input and output voltage and current (B) High voltage side voltage and current (C) Low voltage side voltage and current

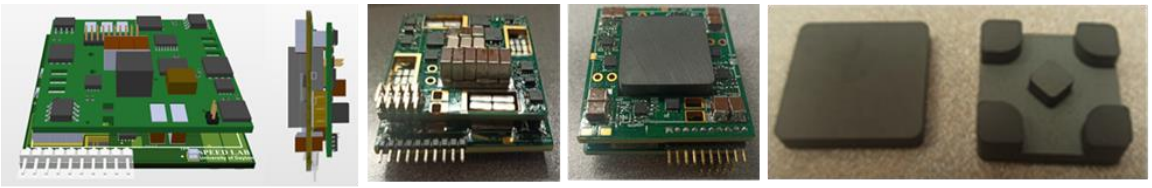
Figure 5-9 The simulation result of the 48V to 5V partial power DC-DC converter

Figure 5-9 shows the simulation waveforms at 400W. The input and output voltage as well as current are shown in Figure 5-9, the high voltage side devices' current and voltage are shown in Figure 5-9 (B), and the current through capacitors is shown in Figure 5-9 (C). For the 8x MASC, the high voltage side devices can achieve ZVS switching as LLC converter does and the low voltage side switches can realize ZCS.

Table 5-1 The hardware parameters of the prototype

C_{in}	**22uF×3 (X7S,100V) C5750X7S2A226M280KB**
C_{F1} & C_{F2}	22uF×2(X7R,50V) CGA9P3X7R1H226M250KB
C_D	47uF(X7R,25V) CGA9P3X7R1H226M250KB
S_{R1}~S_{R8}	(25V,1mΩ) BSZ010NE2LS5ATMA1
S_{W1}~S_{W5}	(40V,2.1mΩ) BSZ018N04LS6ATMA1
S_{W6}~S_{W7}	TDA21472
Gate Driver	9×1EDN7136GXTMA1
C_{out}	47uF×9(X5R,10V) C4532X5R1A476M280KA
C_{R1} & C_{R2}	1.4uF(U2J,50V) C1812C145J5JLC7805
L	470 nH XGL6060-471MEC
Magnetic Core	ML95S@Hitachi Company

Figure 5-10 shows the hardware building of the prototype. The 3D prototype is shown in Figure 5-10 (A), and the real prototype is shown in Figure 5-10 (B). The magnetic core for the matrix autotransformer is shown in Figure 5-10 (C), and the total size is 37mm×37mm×7.8mm. The prototype is composed with two boards, and one board is for the high voltage side components while the other board is for the low voltage side components. Table 5-1 shows the main hardware parameters of the prototype, the maximum power of the prototype is 500W and the switching frequency is 417kHz. The voltage stress of the low voltage side devices is 10V, and the 25V Mosfets are adopted. The voltage stress of the +-high voltage side devices is 20V, and the 40V Mosfets are adopted.



(A) 3D model (B) Prototype (C) Magnetic Core

Figure 5-10 The hardware building of the prototype

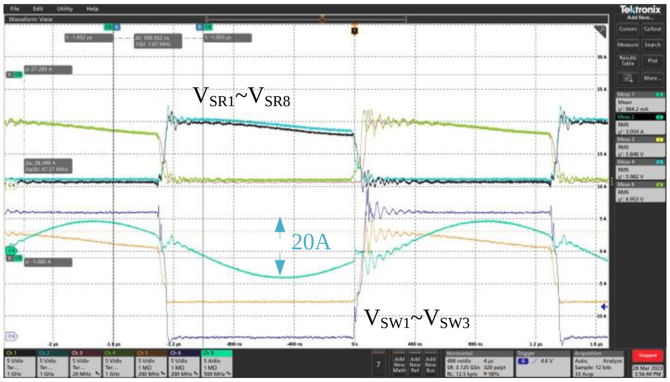


Figure 5-11 The experimental waveform of 8x MASC

Figure 5-11 shows the experimental results of the 8x MASC, and the 8x MASC works as unregulated stage to keep its high efficiency performance. The low voltage side switches voltage stress is 10V while the high voltage side switches is 20V.

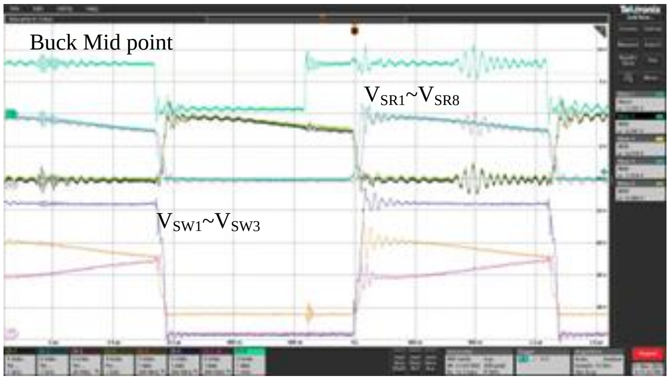


Figure 5-12 The experimental waveform of 8x MASC and buck voltage

Figure 5-12 shows the experimental waveform of unregulated 8x MASC and the middle point voltage of the regulated buck simultaneously. The input voltage is 48V, so the duty cycle of the switch S_{w6} is around 0.625.

Figure 5-13 shows the calculated power efficiency of the proposed circuit. The maximum calculated efficiency (gate driver loss is included) is around 97.75% and the efficiency under full load is around 95.8%. The conduction loss accounts a major part of the total loss and Figure 5-14 shows the test power efficiency. The maximum test power efficiency including gate driver loss is around 97.85% at 150W, and the power efficiency drops to 95.5% at 460W. The power density of the converter is 767.4W/in3.

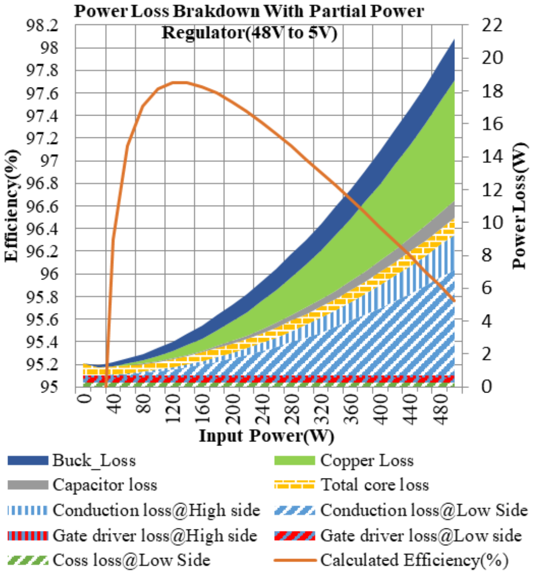


Figure 5-13 The calculated efficiency of the proposed circuit.

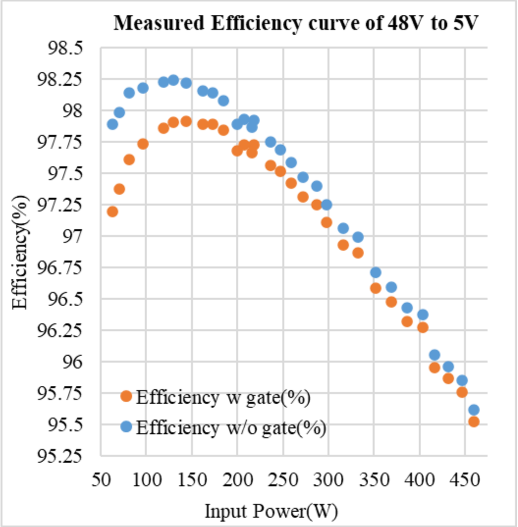


Figure 5-14 The experimental efficiency of the proposed circuit.

5.3 Conclusion

This chapter proposes a new converter based on matrix autotransformer switched capacitor converter(MASC). By adding a buck stage regulator as sigma converter does, the unregulated MASC can work at resonant switching frequency to keep the high efficiency since the soft switching is realized, and the buck can regulate the output voltage at a fixed value with relatively less power processed. The circuit working principle and simulation are conducted in this paper.

Moreover, a prototype of the proposed circuit shown in Figure 5-14 that converts 48V to 5V is built to verify the proposed circuit. The maximum power efficiency can be up to 97.75% at 150W.

5.4 References

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CHAPTER 6

A 15X MATRIX AUTOTRANSFORMER SWITCHED CAPACITOR DC-DC CONVERTER

6.1 Introduction

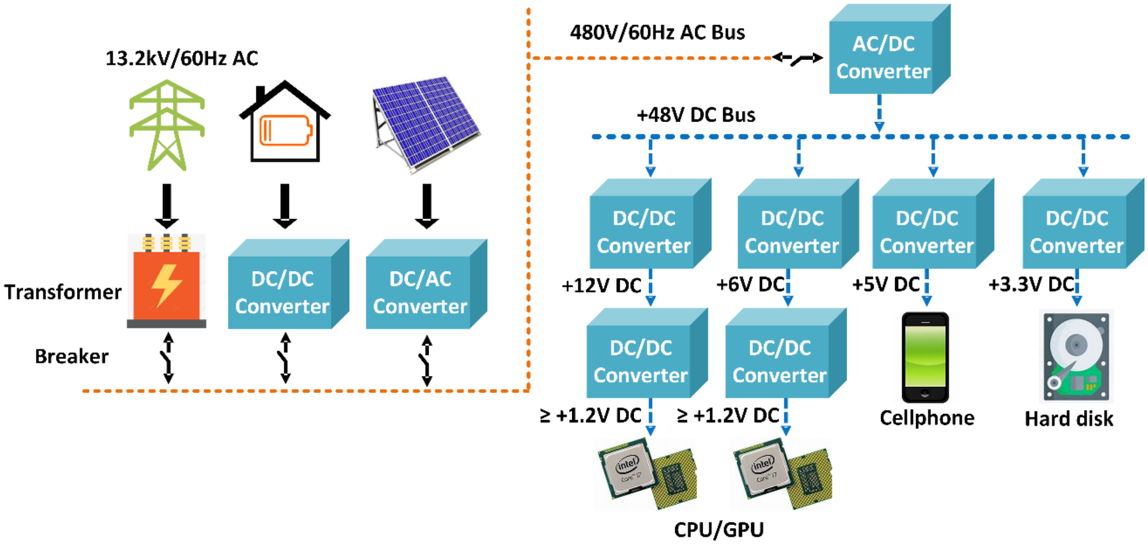

Figure 6-1 This chapter mainly focuses on the 15x MASC

Resonant switched capacitor converter is very widely studied as intermediate bus converter(IBC) for 48V to 12V application on the datacenter application area[1]–[5], and switched tank converter(STC)[6]–[9] is one kind of resonant switched capacitor converters that is commonly adopted among them due to its very high efficiency and power density. On the other hand, LLC converter in [10]–[13] is also very popular among these solutions. With the development of artificial intelligence (AI), the chips' voltage is becoming lower and lower and reference [14] points out that the power levels of AI accelerator CPU/GPUs are already exceeding 750-W with voltage as low as 0.75V. Therefore, the 12V DC bus seems not better than 6V or lower DC bus since it can decrease the conversion ratio of the second stage which is point of load stage (POL). One solution directly that converters 48V to 1V is proposed in [15]–[17].

In terms of the IBC that converts 48V to 6V or lower DC bus voltage, the STC seems not to be more attractive than LLC converter since the LLC can adopt current doubler circuits on its low voltage side, which reduces the devices counts by half. As a result, the conduction loss as well as gate drivers counts are also reduced. This is more obvious at heavy load. For example, the 48V to 6V LLC converter can achieve peak efficiency as 98.1% at 75A while keeping its full load efficiency above 97.6% at full load, which shows just 0.5% efficiency drops across full load range[10]. On the other hand, the isolation is not required on the 48V DC bus structure proposed by Google company[18], so the LLC can be further modified to non-isolated circuit to further decrease the power loss. Therefore, a new circuit structure called Matrix Autotransformer Switched Capacitor DC-DC converter (MASC) is proposed and explored [19], [20]. In the high voltage side, it adopts the low voltage stress with better performance as STC converter does, and in the low voltage side, it adopts current doubler circuit as LLC converter does. The proposed circuit can further increase the power efficiency when compared with LLC and STC. Moreover, the autotransformer can integrate the resonant inductor into it, which decreases the total size and the transformer copper loss like CLL converter does[21], [22]. This paper builds a 15x MASC which is one kind of circuit in [19]. The section II and III analyze the devices' power loss and transformer copper loss among the STC, LLC and MASC. Section IV and V shows the simulation and experimental results to verify the feasibility of the proposed circuit.

6.2 The Low Voltage Side Devices' Loss Comparison

This section firstly compares the low voltage side devices power loss of STC, LLC and MASC with 16x conversion ratio. Figure 6-2 shows the 16x STC, and there are 30 counts of devices on its low voltage side with their voltage and current stress as V_{out} and I_{in} respectively. Figure 6-3 shows the proposed 15x MASC, and there are 15 counts of devices on its low voltage side with their voltage and current stress as $2V_{out}$ and I_{in} respectively. Figure 6-3 shows the 16x LLC, and there are 16 counts of devices on its low voltage side with their voltage and current stress as $2V_{out}$ and I_{in} respectively. In order to compare the power loss of the low voltage side devices, a method called total semiconductor loss index(TSLI) in [8] is adopted for power loss evaluation. For a specific device, its gate driver charge Q_g and output capacitor C_{oss} are proportion to the die area A_{die} while its conduction resistance $R_{ds(on)}$ is inversely proportional to the die area A_{die}, which can be concluded as $Q_g=\alpha A_{die}$, $C_{oss}=\beta A_{die}$ and $R_{ds(on)}=\gamma/A_{die}$. Since the ZCS is achieved on low voltage side, so the C_{oss} loss, conduction loss and gate driver loss are calculated and expressed in (6-1).

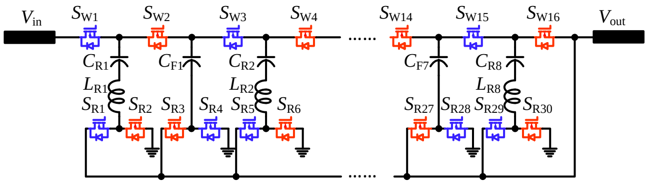

Figure 6-2 The circuit structure of 16x STC

$$Q_{n(filter)}=\frac{\omega_{LPF}}{s+\omega_{LPF}}Q_n \tag{6-1}$$

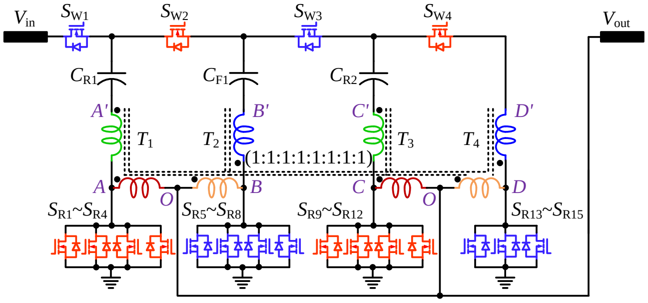

Figure 6-3 The proposed 15x MASC

In order to compare the devices' power loss, the characteristic of the devices should be firstly evaluated. Figure 6-5 shows the figure of merit(FOM) which is expressed as the product of the conduction resistor and gate driver charges, and the 25-V device IQE006NE2LM5 is adopted due to its good performance.

Figure 6-6 shows the power loss of the low voltage side devices, and it can be seen that the devices' power loss of both MASC and LLC is obviously lower than STC's since the current doubler circuit can decrease the counts of the low voltage side devices by half, while the RMS current through every device is the same.

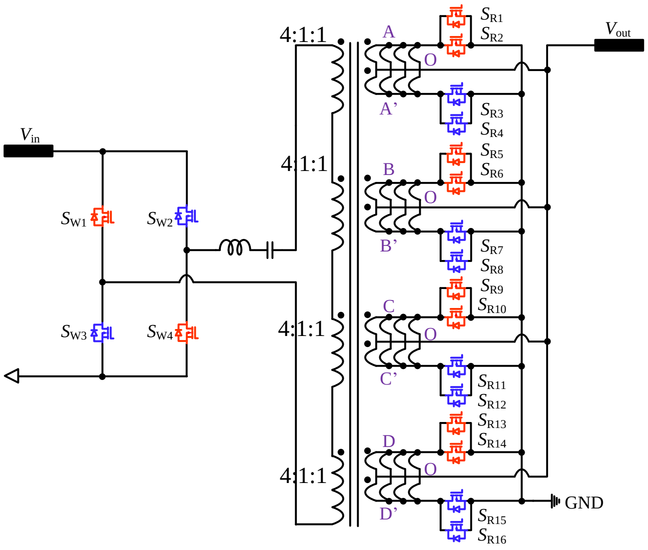

Figure 6-4 The 16x LLC

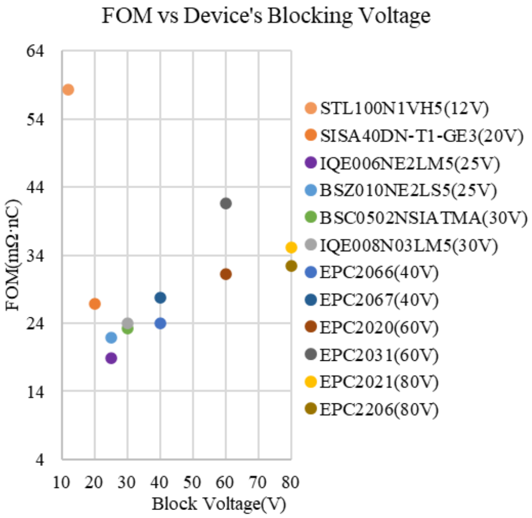

Figure 6-5 Figure of merit(FOM) of low voltage devices

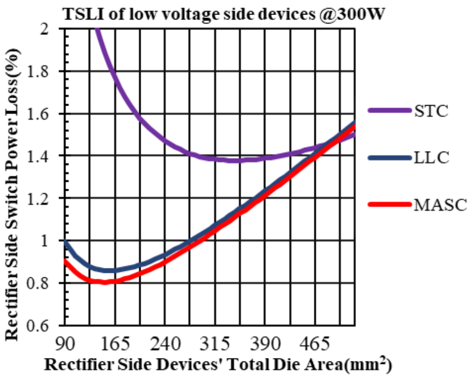

Figure 6-6 The TSLI comparison of the low voltage side devices

6.3 The Transformer Winding Loss Comparison Between the LLC and MASC

Figure 6-7 shows the current waveforms for the 15x MASC, and Figure 6-8 shows the auto-transformer's winding layout. Assume input voltage, output voltage, total copper height, copper width, power rating, copper resistance, perimeter for one turn as V_{in}, V_{out}, h, w, P, l, σ respectively. The winding loss of MASC's auto transformer can be expressed in (6-2), then the minimum power loss can be calculated as $20.95\left(\frac{\pi P}{V_{in}}\right)^2 \frac{\sigma l}{wh}$ when h_1=0.7h and h_2=0.3h.

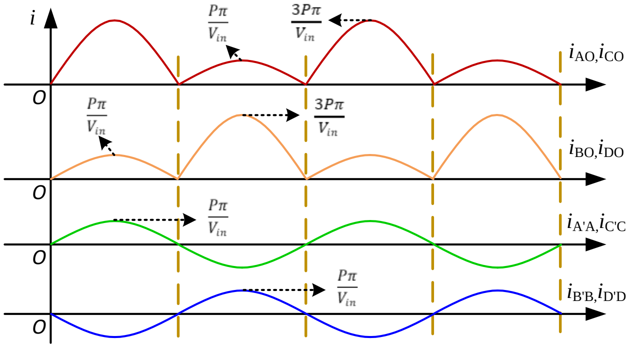

Figure 6-7 The current waveforms of the 15x MASC transformers

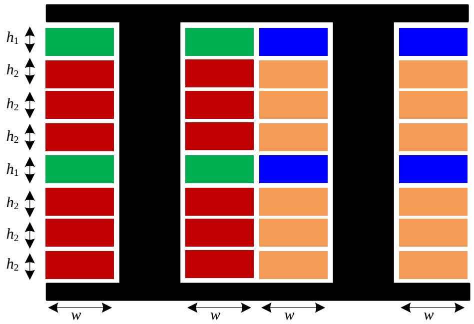

Figure 6-8 The current waveforms through the 15x MASC transformers

$$P_{MASC_{Winding}} = 4\left(I_{AO}^2 R_{AO} + I_{AA'}^2 R_{AA'}\right) = 4\left[\left(\frac{\sqrt{10}\pi P}{2V_{in}}\right)^2 \frac{\sigma l}{wh_1} + \left(\frac{\pi P}{\sqrt{2}V_{in}}\right)^2 \frac{\sigma l}{wh_2}\right] = \left(\frac{\pi P}{V_{in}}\right)^2 \frac{\sigma l}{w}\left(\frac{10}{h_1} + \frac{2}{h_2}\right) \tag{6-2}$$

Figure 6-9 The prototype and the magnetic core

Figure 6-10 shows the current waveforms for the 15x LLC, and Figure 6-11 shows the winding structure of the LLC converter. Likewise, the winding loss can be expressed in (6-3) under the condition that the core size is the same. The minimum winding loss of LLC's transformer can be calculated as $46.67\left(\frac{\pi P}{V_{in}}\right)^2 \frac{\sigma l}{wh}$, where h_p=0.43h and h_s=0.57h. Therefore, the minimum winding loss of MASC is just around 44.9% compared to LLC's if the magnetic core is the same shown in Figure 6-12.

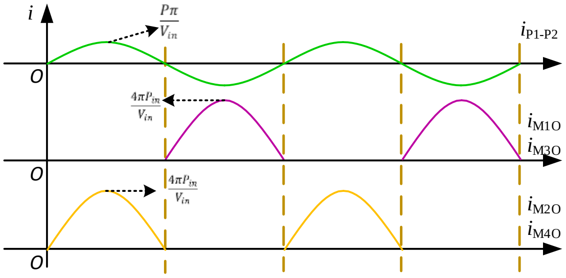

Figure 6-10 The current waveforms through the 15x LLC's transformers

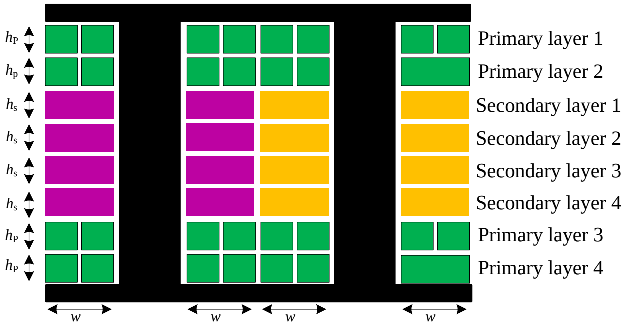

Figure 6-11 The 15x LLC's transformer winding structure

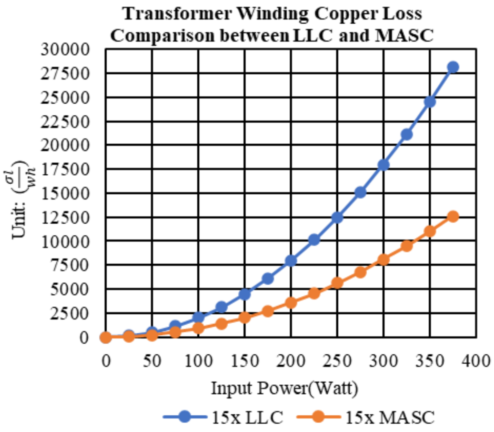

Figure 6-12 The transformer's winding loss comparison LLC and MASC

$$P_{LLC_{Winding}} = I_P^2 R_P + 8 I_{AO}^2 R_{AO} = \left(\frac{\pi P}{2\sqrt{2}V_{in}}\right)^2 \frac{16\sigma l}{\frac{h_p w}{4}} + 8\left(\frac{\pi P}{V_{in}}\right)^2 \frac{\sigma l}{\frac{w h_s}{2}}] = \left(\frac{\pi P}{V_{in}}\right)^2 \frac{\sigma l}{w}\left(\frac{8}{h_p} + \frac{16}{h_s}\right) \tag{6-3}$$

6.4 The Working Principle Analysis

The circuit working principle is shown in Figure 6-13 and Figure 6-14. When the blue devices are conducted, capacitors C_{R1} and C_{R2} are charged, and capacitors C_{F1} is discharged. When the red devices are conducted, capacitors C_{R1} and C_{R2} are discharged while C_{F1} is charged. The resonant frequency of the circuit is $1/\sqrt{C_R L_r}$. Figure 6-13 shows the equivalent model of the auto-transformer, and the detailed equation is expressed in (6-4).

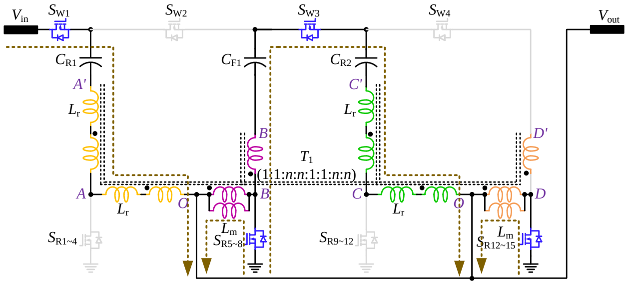

Figure 6-13 The current loop when blue devices are on

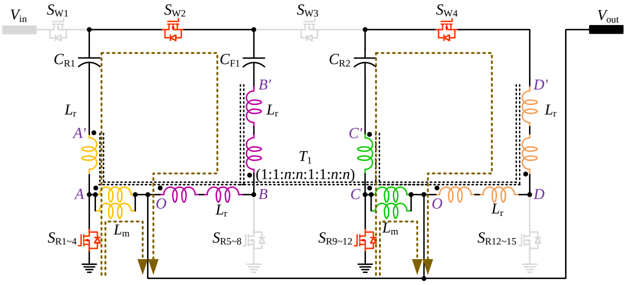

Figure 6-14 The current loop when red devices are on

$$\begin{cases} F_{A'A} + F_{AO} - \Phi_A \mathfrak{R}_S = F_{B'B} + F_{BO} - \Phi_B \mathfrak{R}_S = \Phi_B \mathfrak{R}_L \\ \Phi_A = \Phi_C ; \Phi_B = \Phi_D ; \Phi_L = 2\Phi_A + 2\Phi_B \end{cases} \tag{6-4}$$

$$\begin{cases} v_{BO} = -\dfrac{2\mathfrak{R}_L}{2\mathfrak{R}_L + \mathfrak{R}_s} v_{AO} + \dfrac{2}{2\mathfrak{R}_L + \mathfrak{R}_s} \dfrac{di_{BO}}{dt} \\ i_{AO} = \dfrac{6\mathfrak{R}_L + \mathfrak{R}_s}{2\mathfrak{R}_L + \mathfrak{R}_s} i_{BO} + \dfrac{4\mathfrak{R}_L \mathfrak{R}_s + \mathfrak{R}_s^2}{2\mathfrak{R}_L + \mathfrak{R}_s} \displaystyle\int v_{AO} dt \end{cases} \tag{6-5}$$

When red devices are conducted, then $F_{B'B} = F_{BO}$ and $F_{D'D} = F_{DO}$, then the (6-4) can be further expressed in (6-5). As a result, the resonant inductor, magnetizing inductor and turn ratio are expressed in (6-6), and the equivalent transformer model is shown in Figure 6-14. Likewise, the equivalent transformer model when blue devices are conducted is shown in Figure 6-17.

$$\begin{cases} L_r = \dfrac{2}{2\Re_L + \Re_s} \\ n = \dfrac{2\Re_L}{2\Re_L + \Re_s} \\ L_m = \dfrac{2\Re_L + \Re_s}{4\Re_L\Re_s + \Re_s^2} \end{cases} \tag{6-6}$$

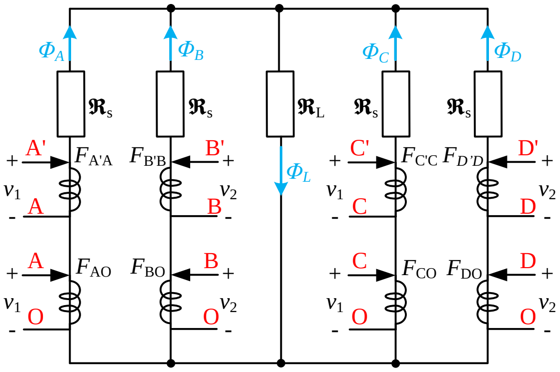

Figure 6-15 The magnetic core model of the matrix auto-transformer

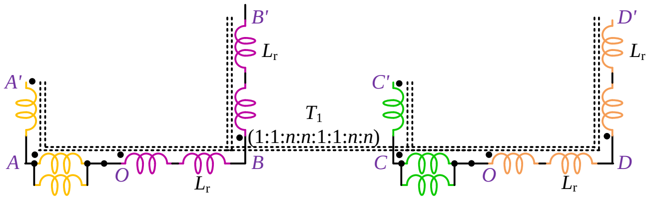

Figure 6-16 The equvilent magnetic core model when red devices are conducted

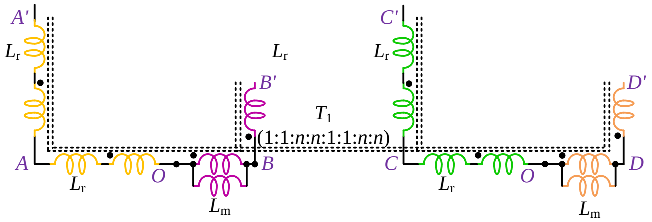

Figure 6-17 The equvilent magnetic core model when blue devices are conducted

6.5 The Simulation of 15x MASC

The simulation at full load is conducted by PLECS. Figure 6-18 shows the waveforms of the input and output ports.

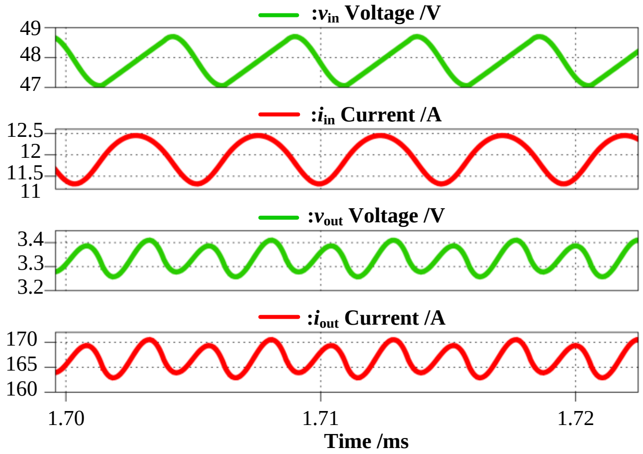

Figure 6-18 The simulation results of the input and output's current and voltage

Figure 6-19 shows the current through resonant and non-resonant capacitors.

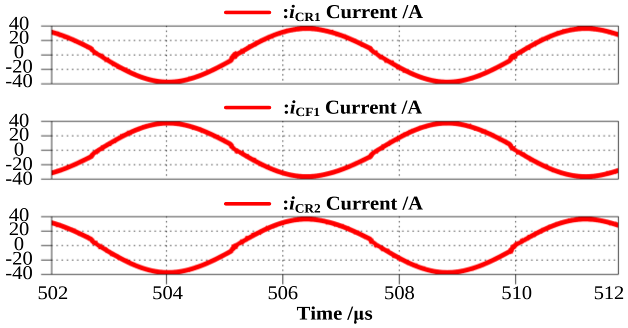

Figure 6-19 The simulation results of the capacitors' current

Figure 6-20 shows the low voltage side devices waveforms, and it can realize ZCS switching at resonant frequency like LLC converter does.

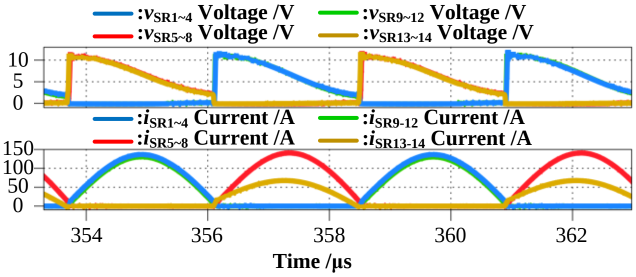

Figure 6-20 The low voltage side devices' waveforms

Figure 6-21 shows the high voltage side devices waveforms, and the ZVS switching is realized by the energy stored in the magnetizing inductor like LLC converter does.

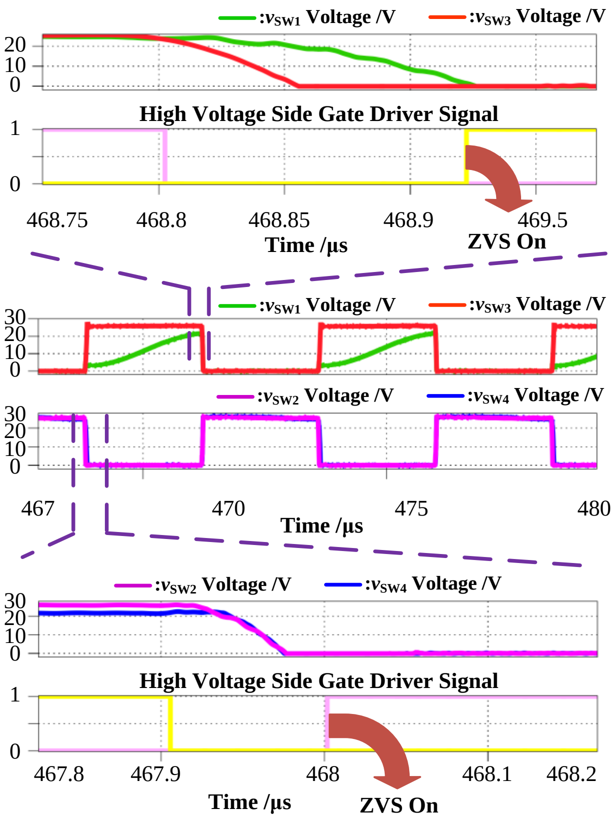

Figure 6-21 The high voltage side devices' waveforms

Figure 6-22 shows the magnetic flux of the matrix auto-transformer and the center cylinder works as resonant inductor, this is also the reason why its waveform is sinusoidal shape.

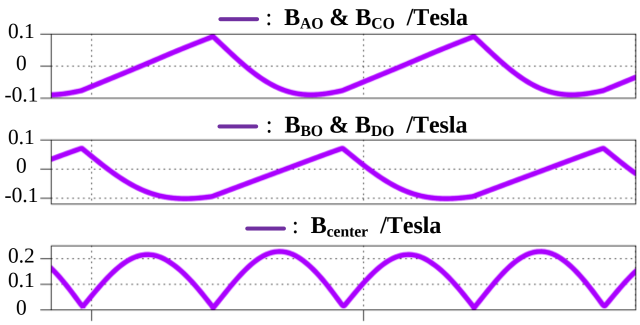

Figure 6-22 The magnetic flux of the matrix auto-transformer

6.6 The Experimental of the 15x MASC

The hardware parameters are shown in Table 6-1. The magnetic core is customized by Proterial company. The working frequency of the prototype is 230kHz with maximum power as 400W. The PWM signal is generated by DSP28379 from TI corporation. The load is 3206A-60-1000 from Chroma.

Table 6-1 The hardware parameters of the 15x MASC

V_{in}	46V~50V
V_{out}	3.06V~3.33V
P_{in}	400W
f	230kHz
C_{in}	22uF×6 (X7S,100V)-C5750X7S2A226M280KB
C_{out}	47uF×18(X5R,10V)-C4532X5R1A476M280KA
C_{F1}	22uF×3(X7R,50V)-C5750X7S2A226M280KB
C_{R1} & C_{R2}	1.4uF (U2J,50V)-C1812C145J5JLC7805
S_{R1}~S_{R15}	IQE006NE2LM5
S_{W1}~S_{W4}	BSC0500NSIATMA1(30V,1.3mΩ)
Gate Driver	13×1EDN7136GXTMA1
Core	ML95S@Hitachi Company

Figure 6-23 shows the experimental waveforms of the input port and output port at peak efficiency point(92W).

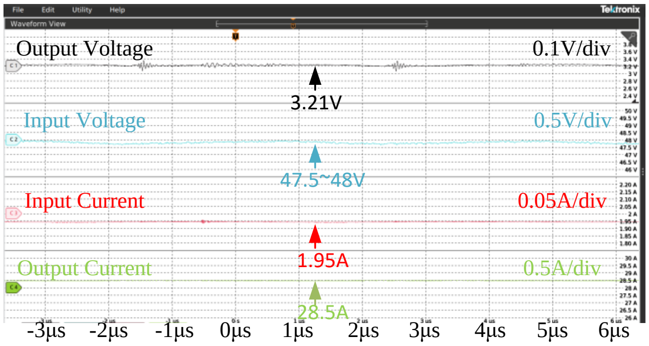

Figure 6-23 The experimental results of input and output's current and voltage

Figure 6-24 shows the devices voltage and capacitor current. The current waveforms is consistent with the simulation results which proves the feasibility of the proposed method.

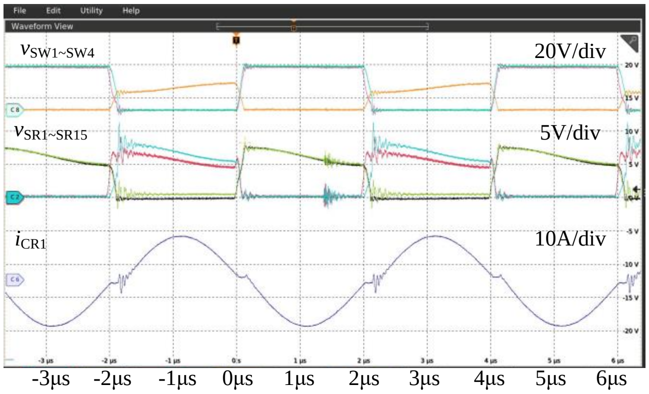

Figure 6-24 The devices voltage and capacitor current

Figure 6-24 shows the efficiency curve of the converter. The RMS value of the input voltage, input current, and the output voltage is measured by the 87-V Fluke digital voltage meter and output current is the data directly obtained from the scope of the electrical load. Moreover, the power for the gate driver chips is obtained from the scope of auxiliary power supply. The blue points in Figure 6-25 shows the measured efficiency without gate driver loss, and the maximum efficiency is 98.75% at 65W. The orange points shows the measured efficiency with auxiliary power (devices' gate power loss + gate driver chips' power loss), and the maximum efficiency can reach 97.6% at around 110W. The grey points shows the estimated efficiency when only the devices' gate power loss is considered.

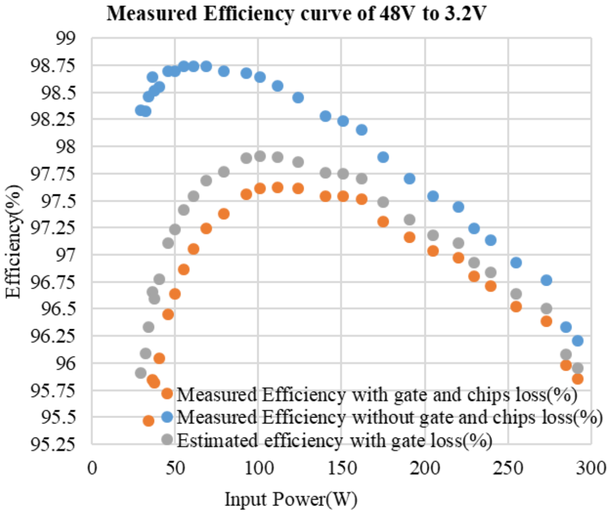

Figure 6-25 The efficiency curve of the 15x MASC prototype

6.7 References

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