ZIRCONIUM DOPING OF TANTALUM OXIDE FOR INCREASED VACANCY MOBILITY IN RESISTIVE SWITCHING BILAYER STRUCTURES

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ZIRCONIUM DOPING OF TANTALUM OXIDE FOR INCREASED VACANCY MOBILITY IN RESISTIVE SWITCHING BILAYER STRUCTURES

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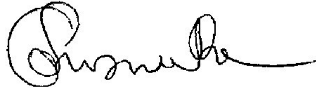

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ABSTRACT

ZIRCONIUM DOPING OF TANTALUM OXIDE FOR INCREASED VACANCY MOBILITY IN RESISTIVE SWITCHING BILAYER STRUCTURES

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Memristors are among the leading devices for non-volatile memory applications due to its in-memory computing capability, power efficiency and high endurance, as well as the speed at which memory states can be written. Tantalum oxide is currently one of the most promising materials in memristor design. Tantalum oxide based memristor devices operate via oxygen vacancy migration in the TaO_x layer forming a filament which then allows current flow once formed. Due to the migration of the vacancies through the material to form this chain, there is permanent structural damage to the device over the course of operation which eventually results in reduced performance of the devices and less change between the SET/RESET states. In this paper, we analyze the impact of zirconium doping concentrations on oxygen vacancy migration by studying the electric field required to induce switching in the devices and device endurance. We test the power efficiency and ON/OFF resistance ratios of numerous $TiN/TaO_x/Ta/TiN$ devices made with zirconium oxide doping layers. The results are then analyzed to understand the effects of the TaO_x/ZrO_2 bilayer structure and the impact on the total power efficiency and endurance of the devices. The devices did show increased conductivity but switching performance and endurance were reduced. TEM imaging was performed to determine the cause, but no definitive cause could be identified.

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LIST OF ABBREVIATIONS AND NOTATIONS

1R1R	One Resistor One Memristor in Series
1T1R	One Transistor One Memristor in Series
ALD	Atomic Layer Deposition
CC	Current Compliance
CMOS	Complementary Metal-Oxide-Semiconductor
C2C	Cycle-to-Cycle
D2D	Device-to-Device
DC	Direct Current
EDS	Energy-Dispersion Spectroscopy
HfO_2	Hafnium Oxide
HRS	High Resistance State
IRS	Intermediate Resistance State
LRS	Low Resistance State
MIM	Metal-Insulator-Metal
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
OCF	Oxygen Ion Conducting Filament
RRAM	Resistive Random-Access Memory
STEM	Scanning Transmission Electron Microscope
SMU	Precision Source Measurement Unit
Ta	Tantalum
Ta_2O_5 / TaOx	Tantalum Oxide
PDMAT	Pentakis(dimethylamino) Tantalum(V)
TDMAZ	Tetrakis(dimethylamino)Zirconium (IV)
V_o	Oxygen vacancy

WGFMU	Waveform Generator/Fast Measurement Unit
XPS	X-Ray Photoelectron Spectroscopy
Zr	Zirconium
ZrO_2	Zirconium Oxide

CHAPTER 1

INTRODUCTION

1.1 Thesis Structure

Chapter one summarizes memristor technology as a hopeful future technology that will revolutionize the semiconductor industry. Chapter two will review literature to establish the current state-of-the-art technologies, memristors' basic operation, structure, and implementations. Chapter three will cover the experimental processes used to design the memristor test structures, their layout, fabrication steps, characterization techniques, and optimization of these processes. Chapter four is an analysis of the electrical characteristics and results for the different compositional models used. Chapter 5 is a summary and discussion of this work and possible future work to be performed to further this area of study.

1.2 Research Area

The memristor has become one of the leading devices in the race for new and innovative computing technologies in the world of microelectronics since its discovery. As computational power has increased over time, so has the desire for better components and performance. Memristors show great promise in this regard with their very simple structure, low energy consumption, high switching speeds, and remarkable scalability.

Memristors gained their name from their very basic functionality. At a basic level, the memristor accomplishes one thing, it stores memory via a change in its resistance. This device, first theorized by Leon Chua in 1971, was not proven to exist until Hewlett-Packard Labs fabricated the first device successfully in 2008 [1]. Since 2008, the number of publications and articles on memristors has increased substantially. However, this technology has not been implemented into everyday technology because while the devices have many characteristics that make them desirable such as high switching speeds, scalability, low energy requirements, etc.

they lack the accuracy and durability required to make them predictable and able to be integrated into most modern systems. More research is needed to address these problems.

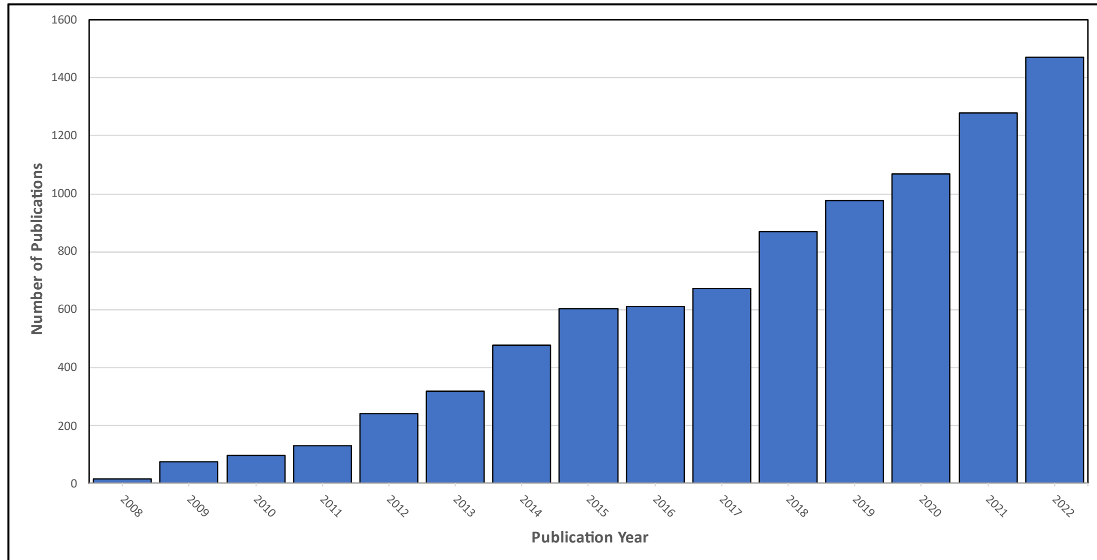

Figure 1.1: Number of publications per year pertaining to memristors since discovery in 2008 from Web of Science Core Database

1.3 What is a Memristor?

Memristors are very simple two terminal devices composed of a metal-insulator-metal (MIM) structure. Within this structure, the top electrode and bottom electrode are composed of metal layers while the insulating layer is the active switching layer of the device where most of the device's unique operation occurs. The devices studied in this thesis are redox-based oxygen ion conductive filament devices (OCF). The graph in Figure 1.2 shows the representative current-voltage (I-V) characteristics for a memristor. These devices switching behavior is reliant upon the voltage polarity to drive the state transitions. Unipolar and bipolar memristors do exist, however, they are temperature reliant and not electric field reliant like the devices in this work. Figure 1.2 also shows the behavior curve for such devices. All devices operate based on I-V hysteresis where the device transitions from a high resistance (OFF) state (HRS) to a low resistance (ON) state (LRS).

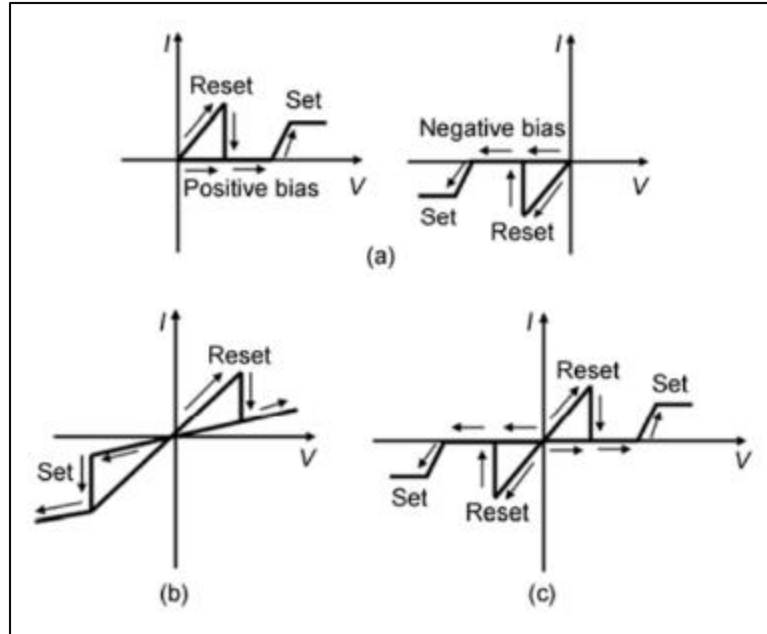

Figure 1.2: Current-voltage (I-V) behavior curves for (a) unipolar; (b) bipolar; (c) nonpolar memristor devices [2]

1.4 Memristor Uses

As we progress into an age of artificial intelligence and massive data transfers, the existing computational standards have not kept up with the incredible pace of and quantity of data processed by these new state-of-the-art technologies. The number of devices that can be fit onto a single integrated-circuit chip is increasingly limited by how small such devices can be made [3]. The energy requirements, processing speeds, thermal budget, and scale of these devices are now paramount to the future development of computational technologies. Memristors offer a unique solution to these problems in terms of data storage and neuromorphic computing due to the unique operation of these devices. By combining the memory and computational capability of a memristor into a circuit design, the required power consumption can be significantly reduced compared to existing transistor technology. Because memristors are passive circuit components, they do not require power to operate. Their memory values are stored once the current has passed

through the device making them ideal for both reducing thermal load and overall power cost of current architecture.

1.5 Research Overview

The aim of this research is to determine the optimal concentration of ZrO_2 doping in Ta_2O_5 OCF memristors. The goal is to reduce the device power consumption and increase cycle endurance of the existing Ta_2O_5 devices by introducing a Zr doping during fabrication. Existing HfO_2 memristors already use ZrO_2 doping layers in the fabrication of HZO memristors to accomplish this same task for transition-metal oxide memristors. The TaOx:Zr memristors underwent electrical characterization and X-ray photoelectron spectroscopy (XPS) to determine their behavior and composition.

CHAPTER 2

LITERATURE REVIEW

2.1 Existing Technologies

Modern semiconductor technology relies heavily upon the use of complementary metal-oxide semiconductor (CMOS) transistor technology. Until now, the growth of this technology has followed the expectations set forth by Moore's Law, which states the number of transistors in an integrated circuit will double every two years [4]. This model has been accurate until recently as we push the limits of current fabrication methods and scalability of CMOS technology.

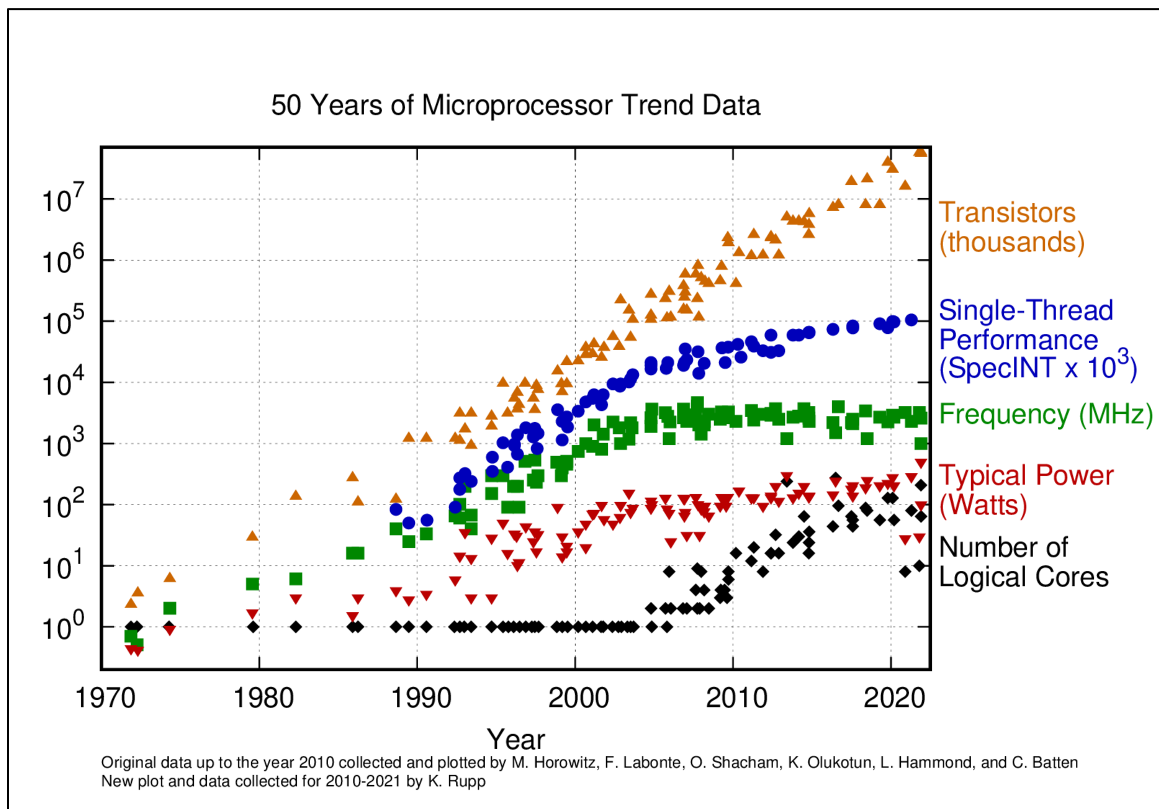

Figure 2.1: Collected data of microprocessor performance for the previous 50 years [5]

The technology to create smaller features has advanced significantly with the advent of several photolithography techniques. Such technologies as 193nm immersion (193i) lithography

and deep-ultraviolet (DUV) patterning have made it possible to draw impossibly small features and create ever smaller devices [6]. The issue, however, that we now face with these technologies, they are approaching their physical limits of operation. Now with devices reaching sizes of less than 10nm, the physics of such devices that we have observed until this point are changing as we approach the limits of their atomic structures and normal physical constants. Because of this, the existing technology for DRAM, SRAM, and Flash memories are having difficulty following Moore's Law.

2.2 The Memristor

The memristor, when it was proposed by Leon Chua, was described as the undiscovered fourth fundamental circuit element relating magnetic flux to electric charge.

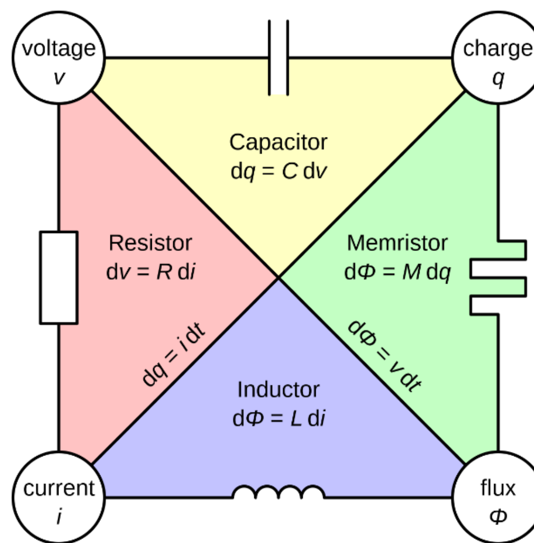

Figure 2.2: Diagram of the four fundamental circuit elements as proposed by Leon Chua [7]

Prior to HP Labs proving Chua's theory in 2008, there was no circuit element capable of relating magnetic flux to electric charge. This is important because while a memristor shares some similarities with both a capacitor and an inductor, it does not store energy. Rather, memristors are bound to a static non-volatile state until disrupted by a charge. Unlike a resistor, whose resistance value is static, memristors change their resistance state depending on how much

current is passed through the device. Since this resistance value is dependent upon the current, memristors have the unique ability to remember how much current has passed through them at any given point making them ideal for storing data with very little energy consumption or heat generation. While the most common device operation modes are either a high resistance state (HRS) or a low resistance state (LRS), they are capable of several intermediate resistance states (IRS) other than just the existing binary ON/OFF states. However, currently the ON/OFF binary state of a memristor makes it easily implementable into contemporary electronics which is desirable. This is not to say that the IRS is not a desirable state. In fact, many exciting prospects are targeting these states for analog device operation [9][10]. The potential to create new and improved circuit architecture for neuromorphic computing applications makes this technology very exciting. With the opportunity to create great breakthroughs in machine learning and create in-memory computing capabilities, this technology is continuously at the forefront of research. With how recent these discoveries are, the primary focus of most of this research is on understanding the operation of such devices and how their behavior is derived.

2.3 Types of Memristors

The characteristic hysteretic behavior of a memristor has been observed across many device types to date. Many of these devices can be seen illustrated in Figure 2.3 and Figure 2.4. Ionic migration such as the ones in this paper form or rupture a conductive filament of ionic defects to change the characteristics of the switching layer [12]. Phase change devices depend upon a classification of phase change materials to change the operation of the switching layer where the devices change from a crystalline to amorphous state and vice versa [13]. Spin Torque Transfer devices operate using the magnetic orientation of the magnetic tunnel junction and its spin-valve structure to determine the device state [14]. Ferroelectric devices use the unique properties of ferroelectric materials to produce spontaneous electric polarization as induced by an external electric field and is currently already in use for many non-volatile memories [15]. Intercalation devices operate based upon lithium-ion intercalation effect as it has been studied in

the anode material of different battery cells [16]. Lastly ionic trapping or electron trapping uses ionic gel or liquid to create a synaptic structure in which the concentration of gated or trapped electrons determines the state [17].

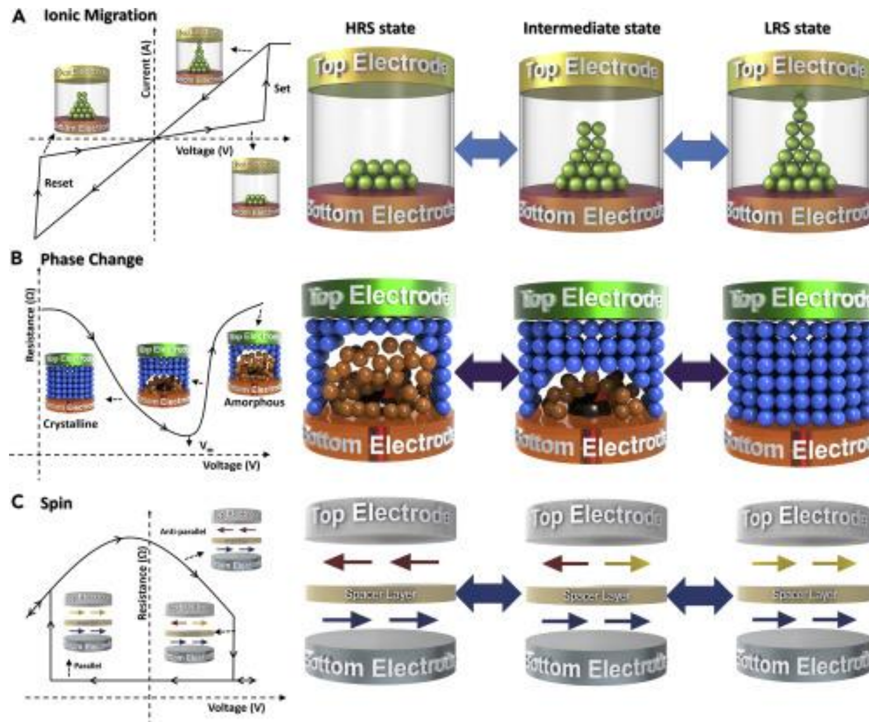

Figure 2.3: Diagram of memristive devices based on the mechanism of operation (a) Ionic Migration; (b) Phase Change; (c) Spin Torque Transfer [11]

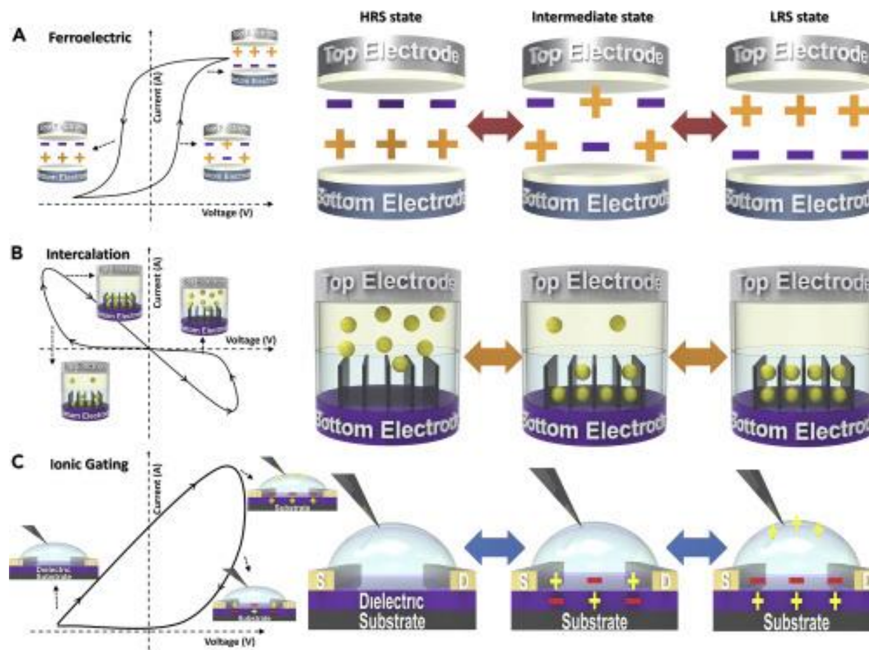

Figure 2.4 Diagram of memristive devices based on the mechanism of operation (a) Ferroelectric Domains; (b) Intercalation; (c) Ionic Gating [11]

2.4 Resistive Random-Access Memory

Among the many promising technologies one of the leading device types is the resistive switching type also referred to as ReRAM or RRAM. As can be seen in Figure 2.5, RRAM memristive structures outperform most if not all the other device types except in linearity. This is the reason for utilizing resistive switching devices for this study.

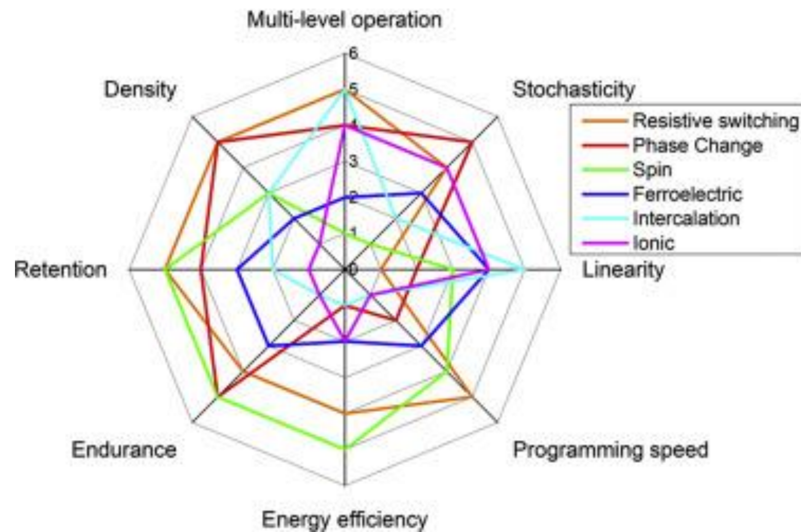

Figure 2.5: Comparison of desirable neuromorphic characteristics of memristor device types [11]

These devices come in many different varieties. The primary two types that people will address are valence change memories (VCM) and electrochemical metallization memories (ECM) [18]. An ECM is constructed of an insulating layer using an electrolyte or oxide connected to an active metal electrode such as Cu. The other electrode is an inert metal of usually Au, Pt, or W [19]. When positively biased cations form and migrate to the inert electrode creating an ionic conducting filament putting the device into the LRS. When the bias polarity switches, this conductive filament ruptures as the device enters the HRS. This process can be repeated such that bipolar switching characteristics can be observed in ECMs. By comparison, in VCMs, the switching layer is composed of a metal-oxide that when biased causes oxygen anion migration. These oxygen vacancies (V_o) form a conducting filament under the applied electric field. For VCMs to operate as intended, they must undergo an initial forming bias under which a higher-than-average voltage is applied to the device. This induces oxygen defects in the device to form and creates V_o in the active switching layer of the device as they migrate from the top electrode to the bottom electrode. Once this is done, the device will operate similarly to the ECM devices. A positive bias will facilitate the formation of a conducting filament putting the device into the LRS which then ruptures under negative bias forcing it back into the HRS.

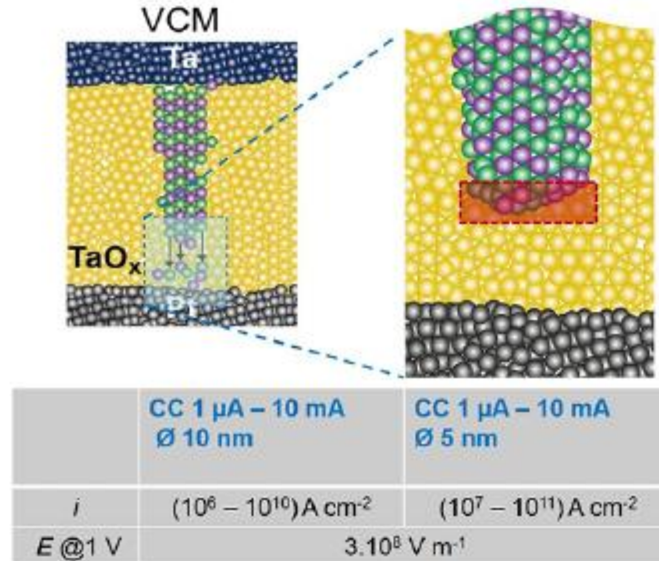

Figure 2.6: Diagram of a VCM model device [18]

2.4.1 VCM Structures

Many different VCM structures show great promise. Such examples that are actively being studied include hafnium oxide (HfO_2), tantalum oxide (Ta_2O_5), titanium dioxide (TiO2), and zirconium dioxide (ZrO2) [20][21][22][23]. Each of these devices in literature use a variety of different electrode materials that change their behavior so often finding the correct electrode material is paramount to optimizing performance. With the wide variety in electrode and metal-oxide materials available for VCM devices, it is not uncommon to see a great deal of device-to-device (D2D) variability. Among VCM materials, Ta_2O_5 is promising because of its excellent endurance, switching speed, and data retention time. This is partially due to TaOx having two stable phases in the form of Ta_2O_5 and TaO_2. A few studies also report on the doping of Ta_2O_5 with Zr to improve switching behavior which is the basis for this paper [24]. Certain devices also incorporate another metallic layer referred to as the oxygen exchange layer. This layer is located between the active switching layer and the top electrode and is responsible for acting as an ohmic electrode and oxygen ion reservoir. This layer helps induce a higher number of V_o making it easier to form a conducting filament within the switching layer. This increase in available V_o has

shown increases in device endurance, lower switching voltages, and lower initial forming voltages. This is attributed to the increase in V_o at the interface between the oxygen exchange layer and the oxide layer [12].

Table 1: Literature Review of different memristor device performance metrics

Device Structure	Insulator Thickness (nm)	Set Voltage (V)	Reset Voltage (V)	R_{OFF}/R_{ON}	Current Density (A/cm^2)	Reported Endurance	Ref
W/Ta_2O_5:Zr/W	10	2.3	-2.3	21.4	6		[23]
$Pt/Ta_2O_5/Ta$	10	0.7	-1.25	457	-	-	[24]
$TiN/Hf/HfO_x/TiN$	8	2	-1.5	10	-	10^6	[25]
$Pt/Ta_2O_5/TiN$	75	1.2	-1.2	-	333	-	[26]
Pd/Ta_2O_5-$Si/TaO_x/Pd$	5	1.5	-1.1	-	-	10^10	[27]
$Pt/HfO_2/Ti$	15	4.0	-5.0	10^4	-	-	[12]
$Pt/HfO_2/TaO_x/Ti$	18	1.5	-1.7	10	-	-	[12]
$TiN/Ti/HfO_x/TiN$	5	1.0	-1.5	100	-	10^7	[28]
W/HfO2/Ti/TiN	5	1.1	-1.4	-	-	-	[29]
$TiN/Ta_2O_5/Ta/TiN$	8	1.2	-1.2	333	10^6	-	Fig 4.2

2.5 Memristor Applications

2.5.1 Integration with Existing CMOS

Memristors, thanks to their incredibly simple metal-insulator-metal (MIM) structure, can be integrated easily into existing circuit structures. With existing CMOS architecture, the size of a device is key to keeping up with Moore's Law as mentioned in Chapter 2.1. Thankfully, since memristors are so simple, they do not occupy a large area in an integrated circuit. By simply having a memristor in series with a MOSFET transistor, the transistor acts as a current limiter for the memristor. This is important for two reasons. One, because of the operation of a memristor, the current passing through a memristor changes rapidly. On occasion, this rapid increase in current is outside of the time resolution scale of many analyzers and during the time where current is not being read, the memristor can experience a large spike in current that can damage both the memristor and other less robust components attached to it. Second, by limiting the current using a transistor you can define the current flow by adjusting the gate voltage. This means that you can define a preset number of memory states reliant upon the gate control of the transistor and achieve a great number of IRS states for the memristor. This means that a memristor can reliably be set to several non-binary states that are incredibly useful for computations and expands the number of operations a CPU could potentially perform.

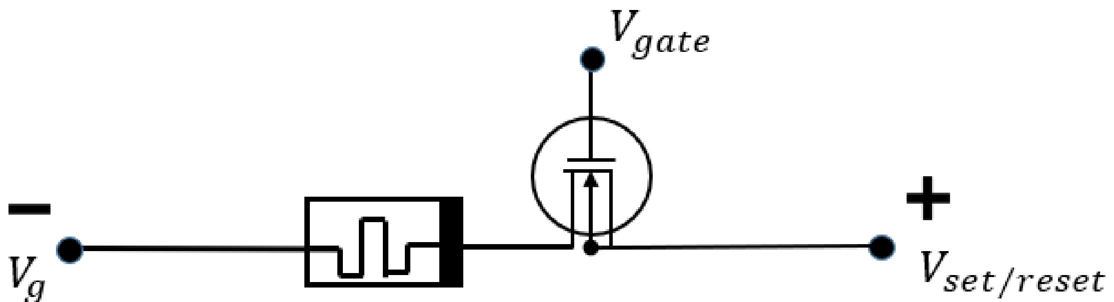

Figure 2.7: Example circuit diagram of memristor integration into with a transistor using one transistor and one memristor (1T1R)

2.5.2 Neuromorphic Computing & Neural Networks

Neuromorphic computing is the concept of replicating biological operations artificially using complex networks of electrical devices. This concept was essential to the development of AI technology we see today. With the growth of software like ChatGPT or control systems like Boston Dynamics, it is not difficult to see the rapid progress that these fields are making. In many areas, AI is being implemented as a tool to assist mankind in many applications. However, these processes take a lot of computational power and consume a lot of energy with current technologies. The existing memory and computational methods in use today follow von Neumann architecture. This has some key issues that are restricting further progress. All data must be stored independently from the computational structure, it is why modern computers have a separate CPU and RAM. This transfer of data between RAM and CPU and vice-versa takes time and energy which are negligible on a single operation basis but non-negligible on the scale of operations that modern CPUs perform. Modern CPUs perform 3.8 billion operations every second making a seemingly negligible delay and power cost large rather quickly. Many researchers theorize that memristors are the key to moving past von Neumann architecture [30]. The model difference between the two architectures can be seen in Figure 2.8. With the crossbar model shown, the input and output vectors of the different sections can be read into a neural network model. In this model, the current values can be read as weighted values in a decision matrix and be used to greatly increase the adaptability of the neural network [31].

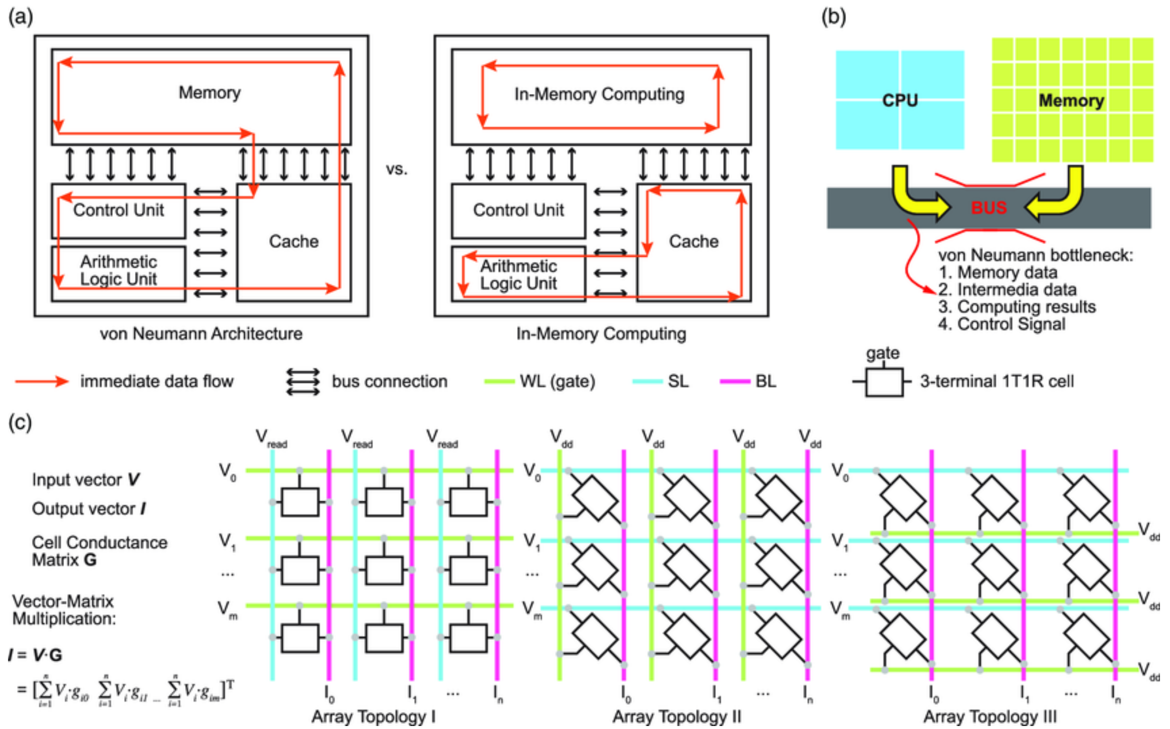

Figure 2.8: Diagram of (a) von Neumann vs In-Memory Computing models as they pertain to CPU operations and (b) the von Neumann bottleneck (c) RRAM matrix array [30]

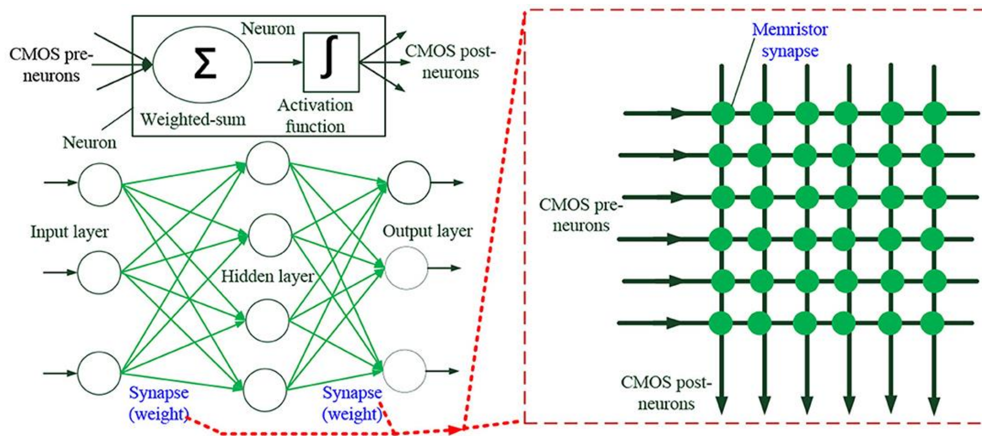

Figure 2.9: Neural Network modeling as a function of a memristor crossbar array [31]

2.6 Importance of ALD for Thin Films

As the scale of device layers continues to decrease the need for smooth and conformal interfaces has risen sharply. For example, assuming a growth like many of those in Table 1 where

the oxide or insulator thickness is 10 nm or less, a surface geometry defect of even ~1nm is incredibly destructive as it can account for 10% of the active layer of the device. To solve these problems we need smooth, clean substrates and even conformal growth layers to create a uniform device stack and interface. Atomic Layer Deposition (ALD) is instrumental in achieving this as it provides the ability to grow a single atomic monolayer at a time across the whole sample surface [32] [33]. This is achieved by using either plasma or water vapor mixed with a metal-organic precursor to react in a self-limiting reaction resulting in only a single layer of growth. Processes involving plasma are called Plasma Enhanced ALD (PE-ALD) and those using water are called Thermal ALD. ALD is also beneficial in that the processes often occur at lower temperatures than their chemical vapor deposition (CVD) counterparts or other such similar processes. This results in less structural change due to heating and thus less damage to the device. When films grown via ALD are studied using atomic force microscopy (AFM) to determine their topography, often the films have <1 nm RMS surface roughness factors [34]. This is essential when trying to characterize a memristor's behavior as any abnormal geometry or peaks at the interfaces can cause local field amplification effects around those features. This will cause filaments to form at these locations and can cause significant cycle-to-cycle (C2C) variations in devices. As can be seen in Figure 2.10, films grown via ALD are often incredibly uniform and very few peaks or geometric anomalies form because of the ALD growth process making it ideal for thin film devices such as memristors.

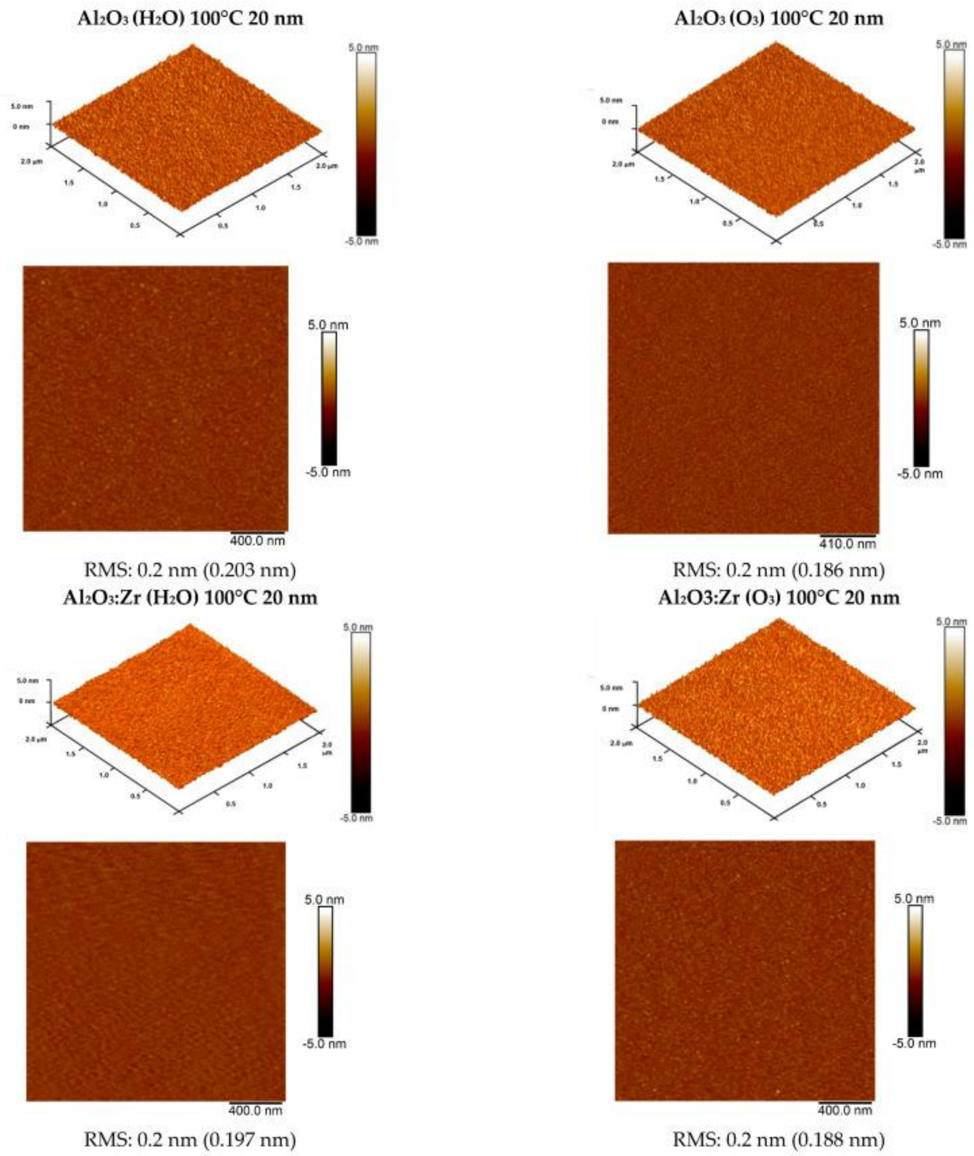

Figure 2.10: Al_2O_3 grown via (left) Thermal ALD; (right) PE-ALD with low RMS roughness (<0.5 nm) [33]

CHAPTER 3

EXPERIMENTAL METHODS

3.1 Fabrication Overview

Memristor devices were fabricated on highly resistive (>10k Ω.cm) <100> undoped 300 µm thick 2-inch diameter Si wafers for this study.

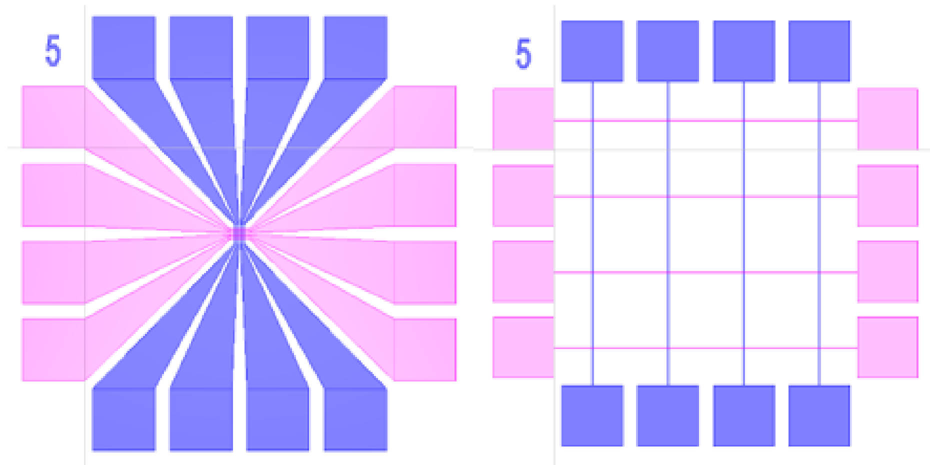

Figure 3.1: Diagram of fabricated devices in crossbar array with 5 µm x 5 µm square device regions. Top metal (blue); bottom metal (pink); intersects contain devices (16 count) for both bowtie (left) and grid (right)

The device geometry of samples used can be seen in Figure 3.1 above. These structures contain 16 devices located at the intersections between the top and bottom metal. Electrode contact regions were covered with a 60 nm protective layer of Ti and Pt following the top contact deposition to make sure that the tungsten probe needles did not damage them. An in-depth write up of the patterning and fabrication steps developed by Dr. Eunsung Shin and can be found in Appendix B.

3.1.1 Electrode Materials

The target for the top and bottom electrodes was 50 nm of conductive TiN. This proved to be one of the greater challenges throughout the project. Since we wanted to use the TiN for

both the top and bottom electrodes, we needed to deposit the material using methods that would not cause any unintended annealing effects or damage in the metal-oxide switching layers. Because of this, we explored many different methods of depositing a conductive TiN electrode at room temperature. Many of these methods involved sputtering from a TiN target on various systems and different sputtering chambers. In all cases where a TiN target was used, regardless of vacuum quality, plasma compositions, power used, every sample had resistivity values above the desired value. As such the final electrodes used for this study were all grown via reactive DC magnetron sputtering at 60 W from a Ti target in a room temperature deposition using a 10 sccm Ar/10 sccm N environment at 4 mTorr. The N plasma used when sputtering would react with the Ti target on impact such that the final deposited material was TiN. This resulted in a sufficiently conductive electrode from the desired material. This growth was done by Dr. John Jones of AFRL. Figure 3.2 shows the picture of the plume inside the chamber during the DC magnetron sputtering of TiN.

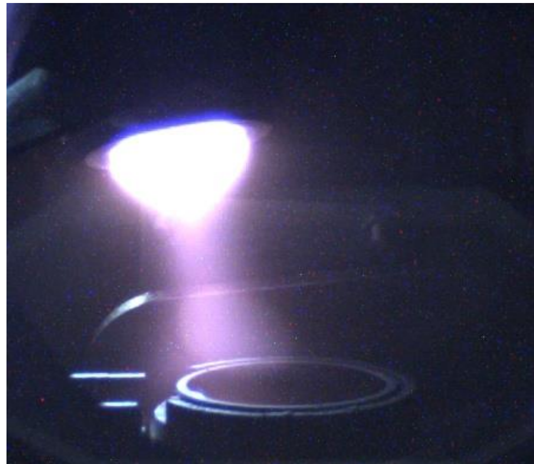

Figure 3.2: Image of TiN bottom electrode sputtering inside of chamber provided by Dr. John Jones

3.1.2 Metal-Oxide via ALD

The metal-oxide switching layer of the devices were grown via Thermal-ALD, shown in Figure 3.3. Using this ALD systme, we created a series of devices with varying Zr concentrations

as measured by the number of grown layers in a Ta_2O_5 and ZrO_2 bilayer structure. By doing this with the ALD we could very accurately control the number of monolayers of each material and their relative thickness. The Ta_2O_5 layers were deposited using the metal-organic precursor Pentakis (dimethylamino) tantalum(V) (PDMAT) and H_2O at 250 °C. The process flow for the deposition was an 80 sccm Ar gas flow to maintain the vacuum environment followed by 10 seconds of wait time. A 0.05 second pulse of H_2O followed by 5 seconds of wait time. A 0.25 second pulse of PDMAT and 5 seconds of wait time. The chamber is then purged, completing one cycle. The ZrO_2 layers were deposited using Tetrakis(dimethylamino)zirconium (IV) (TDMAZ). The process flow for the deposition was a 100 sccm Ar gas flow followed by 10 seconds of wait time. A 0.06s pulse of H_2O followed by 5 seconds of wait time. A 0.25 second pulse of TDMAZ followed by 5 seconds of wait time. Finally ending with a purge to complete one cycle. Both the Ta_2O_5 and ZrO_2 layers had an average growth-per-cycle (GPC) of ~1 Å/cycle. A series of devices with different Zr concentrations were grown with this technique. These devices' concentrations were measured as a function of (# of Ta_2O_5 layers: # of ZrO_2 layers / %expected Zr concentration). The concentrations were (1:1 / 50%), (9:6 / 40%), (12:3 / 20%), (12:2 / 14%), (6:1 / 14%).

Figure 3.3: Veeco Fiji G2 Plasma-Enhance ALD used for deposition.

3.1.3 Oxygen Exchange Layer

The oxygen exchange layer was deposited on top of the metal-oxide layer. This layer is a pure Ta metal layer. It is deposited via e-beam evaporation at a separate AFRL facility. This is an oxygen deficient layer that assists in the development of V_o during the formation of the conductive filament. Figure 3,4 shows the cross-sectional diagram of the device layers along with their thicknesses.

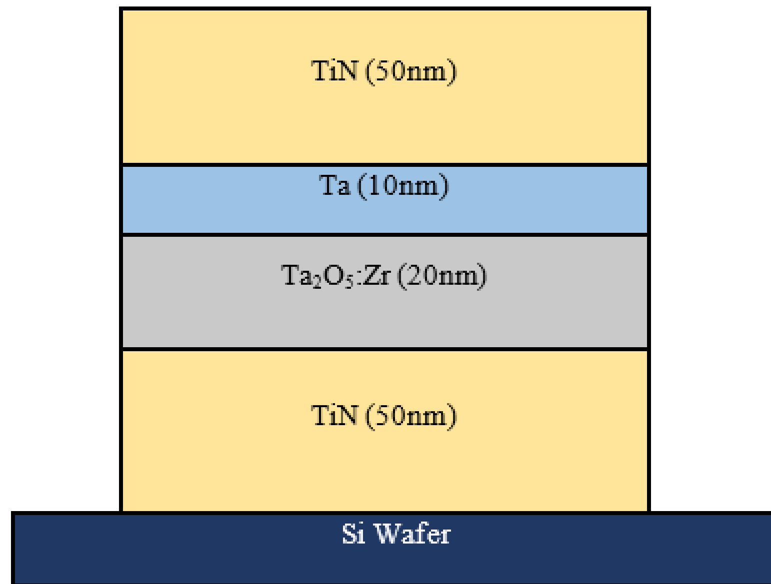

Figure 3.4: Cross-sectional diagram of device stack for Ta_2O_5:Zr memristors

3.2 Work with Undoped Ta_2O_5

In my previous work, many tests were conducted on undoped Ta_2O_5 memristors. These samples were provided by SUNY Polytechnic Institute in collaboration with AFRL. The devices used a very similar device stack with a series NMOS transistor. The thickness of the Ta_2O_5 layer was ~8 nm and the Ta oxygen exchange layer was ~8 nm as well. This was confirmed via scanning transmission electron microscope (STEM) energy dispersive spectroscopy (EDS) done by Dr. Krishnamoorthy Mahalingam. Testing on these devices was done using a series of different gate voltage (V_g) values. These values were in the range of V_g = [1.0, 1.2, 1.4, 1.6, 1.8]

V. An initial forming sweep was applied from 0 V to 3.5 V for all devices. Each device was then tested on a SET/RESET cycle with RESET pulses/sweeps reaching -1.2 V and SET pulses/sweeps reaching 1.2 V. This data is included as part of Table 1 and will also be addressed in the results section for comparison. For these samples a current compliance was not set as the 1T1R configuration utilizes the transistor as a current limiter.

3.3 Electrical Characterization

Measurements for this experiment were done using a MicroXact probe station and Keysight B1500A Semiconductor Analyzer, shown in Figure 3.5. The B1500A unit had two B1530A Waveform Generator/Fast Measurement Units (WGFMU) and three B1517A High Resolution Source/Measurement Unit (HRSMU) modules installed.

Figure 3.5: MicroXact probe station (left) and Keysight B1500A (right)

All samples were tested with an initial current compliance of 0.5 mA. An initial 3.5 V formation voltage was applied and increased by 0.5 V for every failed formation or until devices showed signs of non-memristive behavior. A DC sweep was then performed with a SET voltage of 1.2 V

and a RESET of -1.2 V. If devices failed to switch the values for SET and RESET were adjusted to ±1.5 V and increased in 0.5 V increments until switching occurred in each respective cycle. Current compliance was also adjusted in increments of 0.5 mA to account for D2D variability. The final values for all tests were ~8 V SET pulses with -8 V RESET pulses. Two samples required ±15 V to show switching behavior. All samples were tested with a final current compliance of 2 mA. One sample tested at 2 mA showed signs of damage due to excessive conductivity in the HRS. This sample, though tested at 2 mA as well, was reduced to 1 mA for the final tests. All samples were tested with ramping values until behavior was shown. No tests exceeded 2 mA or 15 V. The time scale in Figure 3.6 is typically in seconds for a full cycle of measurement.

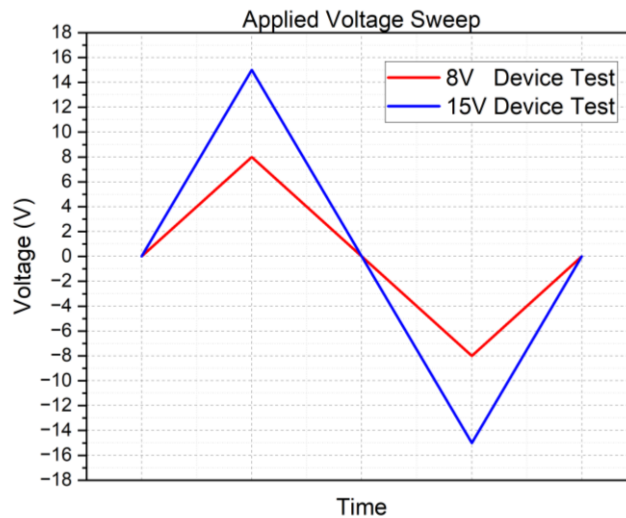

Figure 3.6: SET/RESET Applied Voltage Sweep/Pulses

3.4 STEM and EDS

To analyze the behavior due to device structure, STEM and EDS sample preparation and characterization were completed by Cindy Bowers at AFRL. Samples were prepared using a focused ion beam using a Ga source.

CHAPTER 4

RESULTS

4.1 Undoped Ta_2O5 Samples

4.1.1 Electrical Data

The undoped devices provided by SUNY Polytechnic Institute are used as a baseline for what the expected device stack should behave. Since they share the same material structure, they are comparable devices. These devices are in a 1T1R configuration with an NMOS transistor.

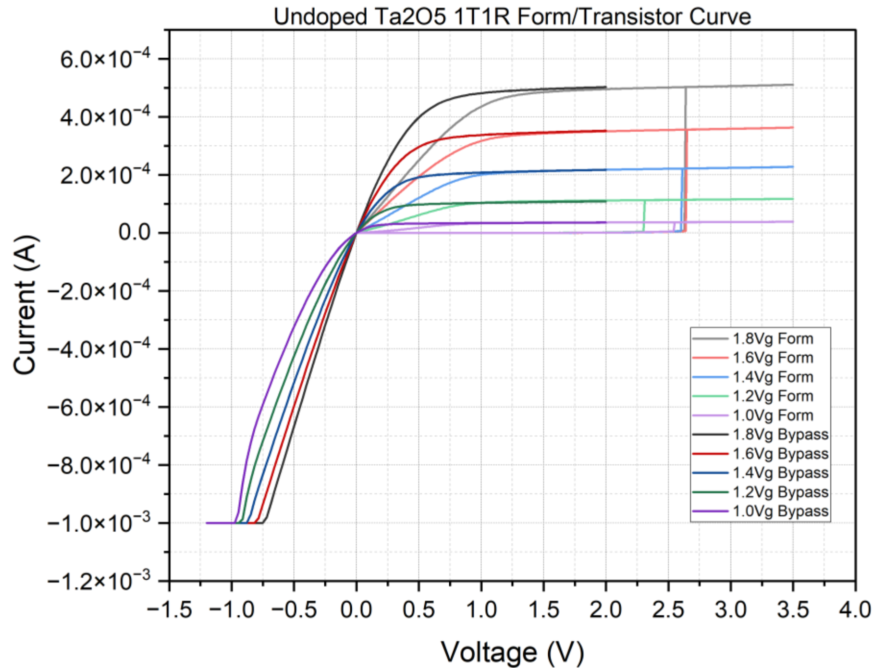

Figure 4.1: Transistor characteristic I-V and 1T1R formation I-V

Figure 4.1 shows the curves for five different gate voltages in a 1T1R configuration device and when the memristor is bypassed to give just the transistor behavior independently. This contributed greatly to the overall device endurance. This in conjunction with the low SET/RESET voltages contributed greatly to the overall D2D and C2C performance by limiting the amount that

the current could spike after conductive filament formation. The HRS values were in the range of ~100k Ω while the LRS values reached ~2500 Ω. Devices tested at the other Vg values are listed under Appendix A.

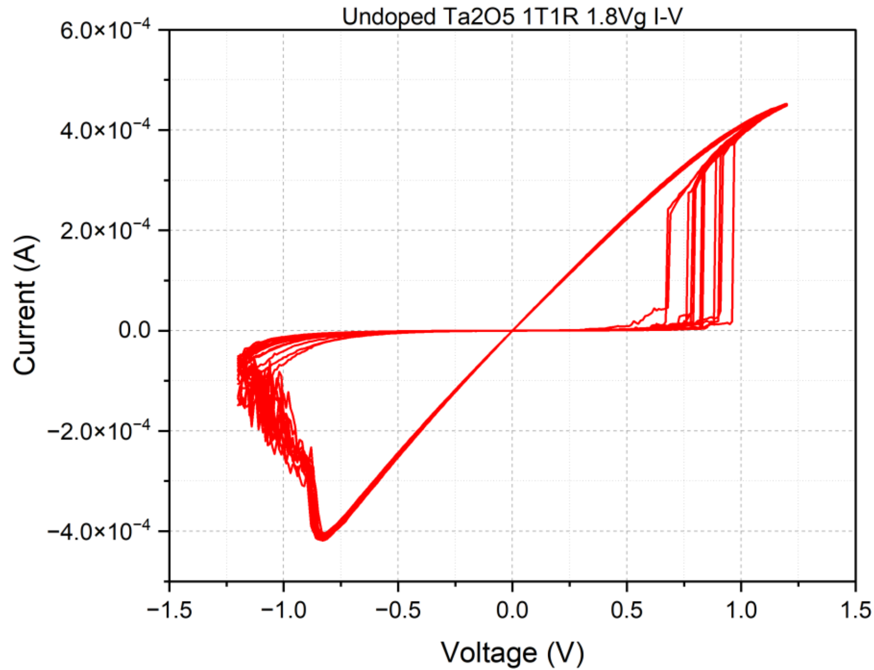

Figure 4.2: Undoped TaOx 1T1R Linear I-V data at 1.8Vg

Figure 4.2 shows just the 1.8 V gate voltage I-V characteristics of the undoped SUNY provided sample. According to the figure, the devices followed the current compliance values set using the transistor gate voltage seen in Figure 4.1. These devices SET at approximately +0.6 V to +0.8 V and RESET at approximately -0.9 V to -1.2 V as seen in Figure 4.2. The exact behavior for these devices at their highest tested current compliance is listed in Table 1. The HRS values were low to begin with allowing for a very low current compliance to be set.

The overall performance of these devices is used as a reference for which to compare the doped devices. Important differences between these and the doped devices include the 1T1R configuration. The transistor used for the samples in Figure 4.1 are made as part of the device

structure and different from standard breadboard transistors and therefore the transistor behavior curves of these devices cannot be matched with any external device we could incorporate. The device region is also smaller. The device area of the undoped samples is in the range of 0.1 μm by 0.1 μm. This contributes to the resistivity of the material and therefore the resistance values observed.

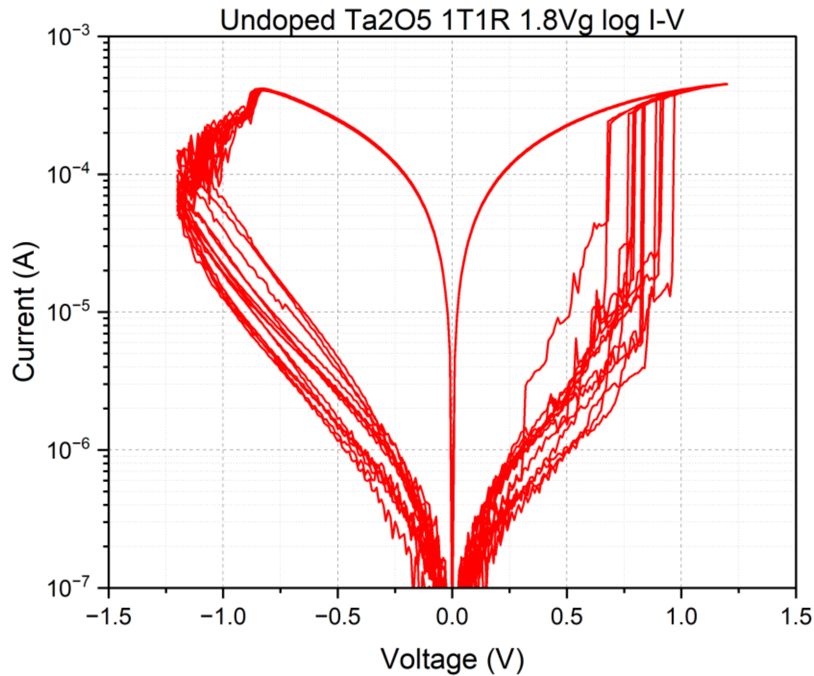

Figure 4.3: Undoped TaOx 1T1R Logarithmic I-V data at 1.8Vg

Figure 4.3 shows a logarithmic scaling of the same data contained in Figure 4.2.

4.1.2 STEM and EDS Data

To ensure that the device is undamaged and is of the expected composition they are imaged and analyzed using STEM and EDS analysis. The structure shows the expected TiN electrodes and Ta_2O_5 switching layer with accompanying Ta oxygen exchange layer. There are trace oxygen amounts in the exchange layer and electrodes which are expected as Ti reacts

readily with O to for TiO_2. The Ta layer is also designed to increase the amount of oxygen vacancies (V_o) by taking in oxygen atoms from the oxide layer. The structure shown in Figures 4.4 to 4.6 are exactly as expected.

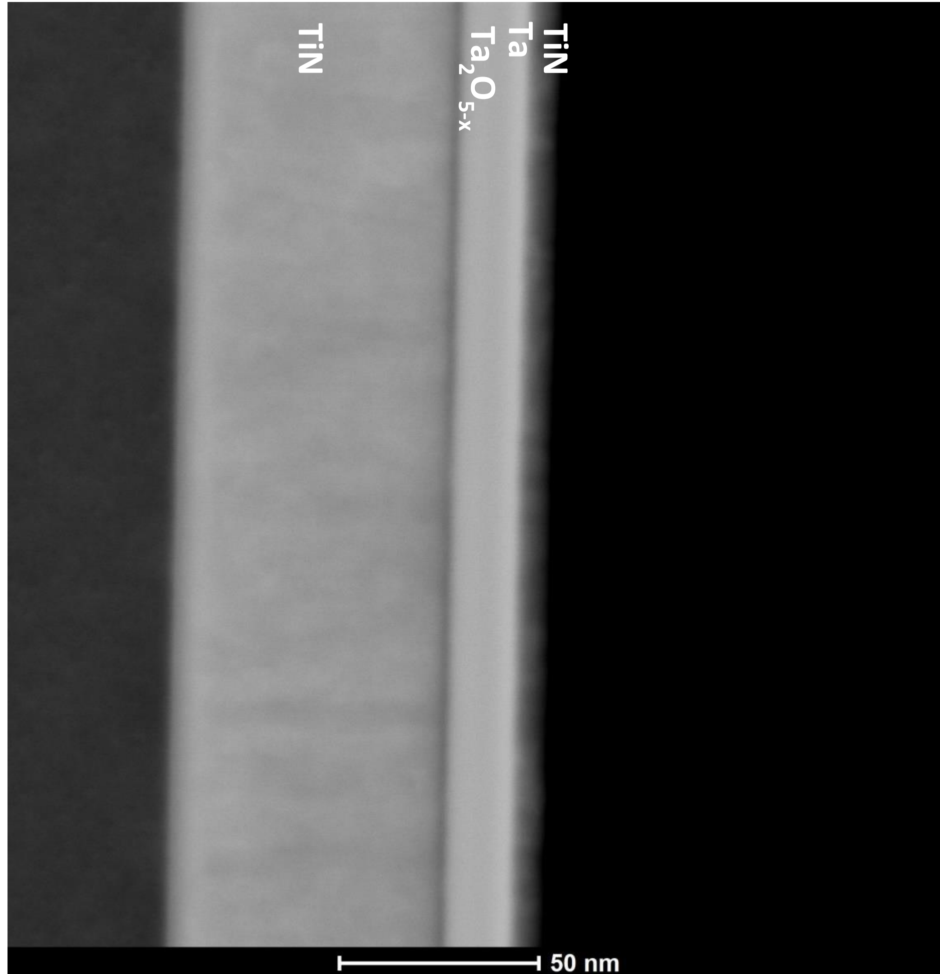

Figure 4.4: STEM image of the undoped device cross section

In Figure 4.5 the relative regions where the Ti, Ta, and O peaks are located can be seen as a color spectrum. The layers' thickness can be confirmed as ~8 nm. Figure 4.6 shows the relative concentrations based on their locations in the sample. The TiN contacts and the Ta_2O_5 and Ta oxygen exchange layers can all be identified by the relative intensity and peaks of each curve. The locations are as expected starting from the bottom TiN electrode on the left to the top

electrode on the right of the curve and images. Devices show no signs of damage and indicate the expected diffusion of oxygen into the exchange layer to create V_o in the device.

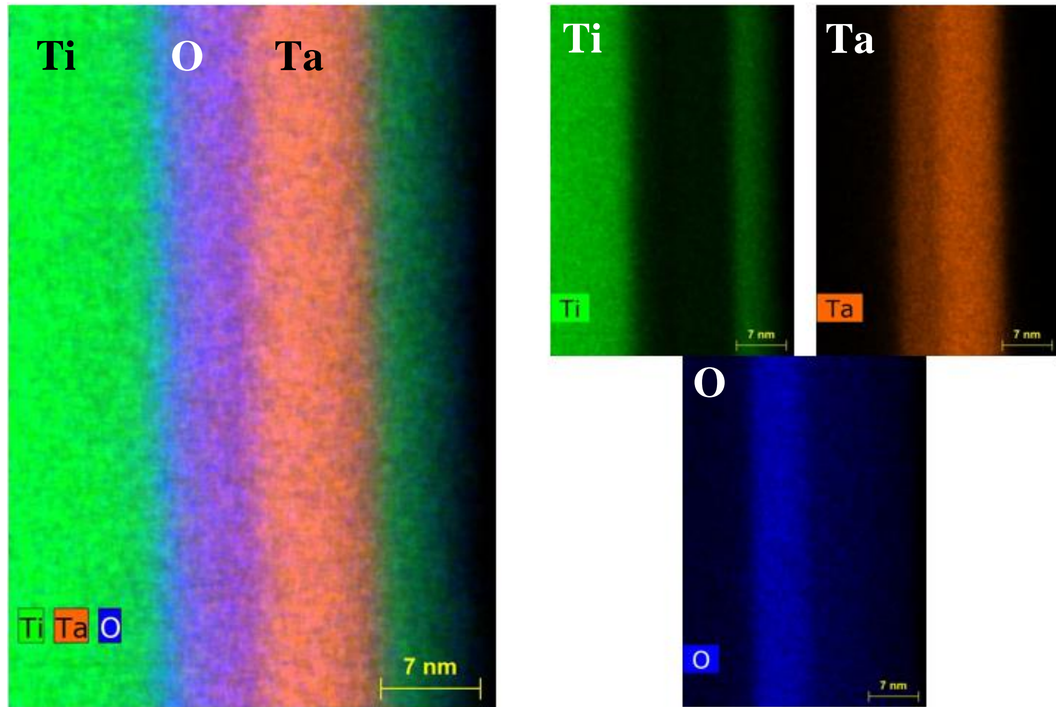

Figure 4.5: EDS overlay of STEM undoped device cross section for Ti, O, and Ta

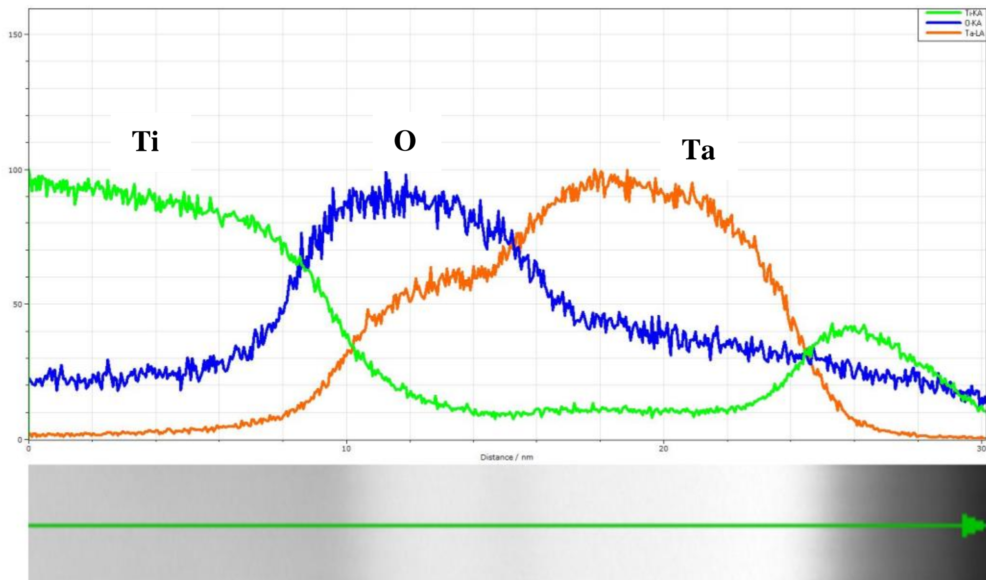

Figure 4.6: Elemental Line Profiles EDS for relative concentrations by area in STEM image

4.2 Doped Ta_2O5 Samples

4.2.1 Electrical Data

As a proof of concept some initial devices at a TaOx:Zr (12:3 / 20%) were fabricated using SUNY Polytechnic Institute one memristor and one resistor series (1R1R) devices. Other concentrations were made as well at (1:1 / 50%) and (9:6 / 40%). Only the concentration 20% devices managed to have any switching behavior. A sample diagram of a 1R1R configuration can be seen in Figure 4.7 below.

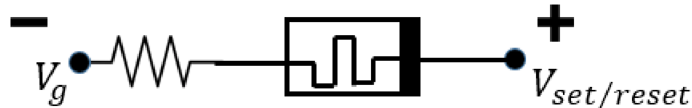

Figure 4.7: Sample 1R1R configuration diagram

The 1R1R configuration used several different series resistance values to test the doped films. Resistances used included 1000 Ω, 2000 Ω, 3000 Ω, 5000 Ω, 10k Ω, and 15k Ω.

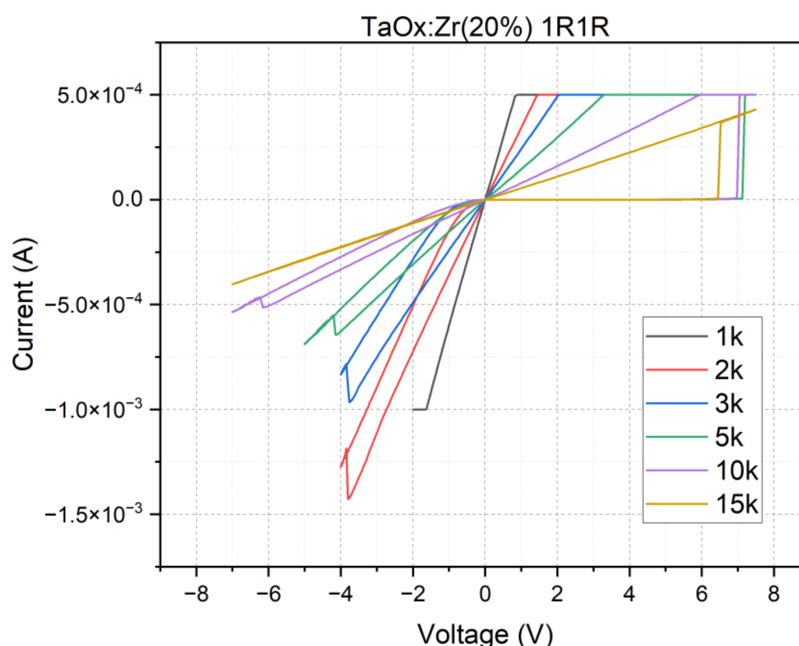

Figure 4.8: Linear I-V analysis for 1R1R doped device proof of concept

Curves shown in Figures 4.8 and 4.9 are of the first formation at +7 V and the RESET curves at varying voltages relative to each resistance. The current compliance for these devices was held at a constant 500 µA for the formation and adjusted for the RESET sweeps. No successful RESET was achieved for the 1k and 15k resistances due to either excessive voltage or current requirements. In general, these devices had much higher formation and switching voltages relative to the undoped samples. The device-to-device (D2D) variability of these devices also made it difficult to achieve a successful dataset from which to derive any results. Many of the devices that did form at these voltages failed to RESET to a low enough voltage that a consequent SET sweep could be applied. The endurance as a result was much lower overall for these tests but switching behavior was shown and thus further devices at the relative concentrations were fabricated to verify the results.

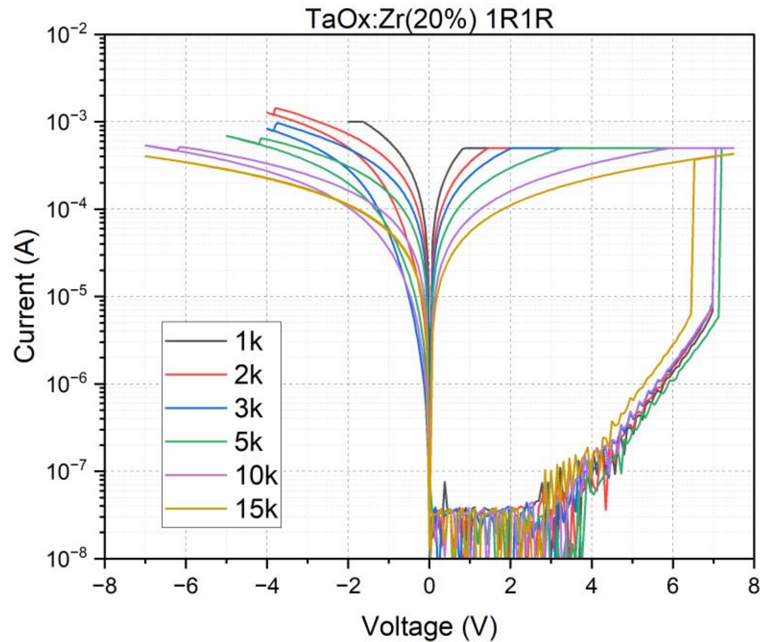

Figure 4.9: Logarithmic I-V analysis for 1R1R doped device proof of concept

The fabricated devices for this study included numerous samples of the relative TaOx:Zr concentrations listed. These include (1:1 / 50%), (9:6 / 40%), (12:3 / 20%), (12:2 / 14%), and (6:1 / 14%) samples. Of these concentrations, the (1:1) samples showed no successfully tested devices and many of the other concentrations have unrepresented also due to a lack of useful extracted data. Device areas are measured at 5 µm by 5 µm. Most samples did not show a separate formation curve from their standard SET/RESET curve. As such, the voltages used for all samples that showed successful behavior were ±8 V for the SET/RESET sweeps. The exact details for the applied bias voltage can be found in Figure 3.6. These large voltages are likely due to the much lower HRS resistance values observed. The observed low resistance of all states is also the cause for increased current compliance on the doped samples. Without increasing the current compliance, the voltage applied to the devices would peak before any switching behavior could be observed. All linear data sets are colored such that the first cycle through the last cycle

can be identified. This is because the devices, though they started with switching behavior, slowly started to show pinched hysteresis loops and a decay in their switching properties. Testing was considered concluded once a device had repeated the same pinched hysteresis with no change in resistance for three consecutive tests. The logarithmic scales are normally included in many memristor papers as an easy way to visualize the difference between the HRS and LRS. In these examples, the logarithmic curves highlight the lack of a useful HRS necessary to force devices into LRS. Most devices showed conductive behavior immediately and did not have a large R_{OFF}/R_{ON} value. All values derived from these datasets can be found in Table 2.

Samples 182 through 185 show very little difference in their behavior relative to each other. Sample 186 shows a great difference in behavior despite undergoing the same fabrication and having the same layer composition as samples 184 and 185. This behavior is not explainable except as D2D variability. One possibility could be the variability in the electrode conductivity because of the trial and error in TiN deposition, however, these samples were all grown within 24 hours of one another on the same system under identical conditions.

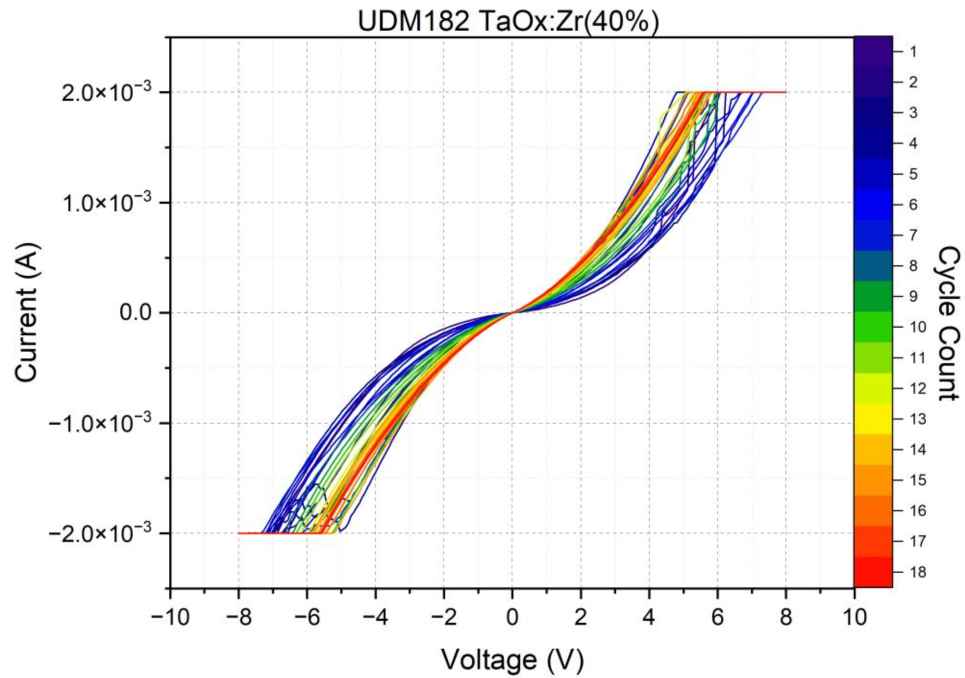

Figure 4.10: Linear I-V of Sample 182 (9:6)

As can be seen in Figure 4.10, the I-V curves of sample 182 show signs of the hysteresis loop pinching off within just a few cycles. The color bar indicates the cycle count of the device and the changes observed between each cycle to indicate cycle-to-cycle variability. The curves shown in Figure 4.11 are identical to the data contained in Figure 4.10 but with a logarithmic scale for current. This was to visually separate the low and high resistance states but as can be seen the HRS current values were too high to distinguish between them. The process is repeated for each of the samples.

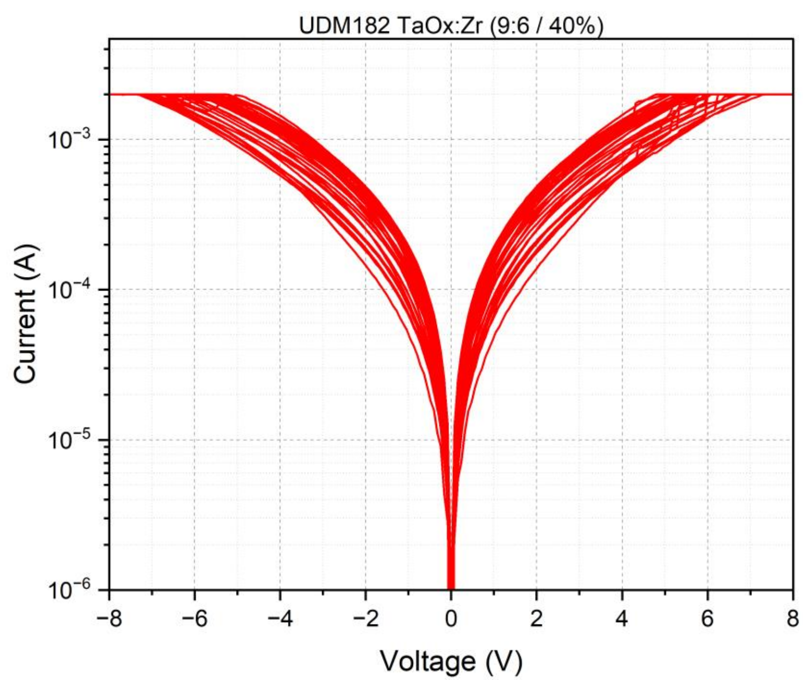

Figure 4.11: Logarithmic I-V of Sample 182 (9:6)

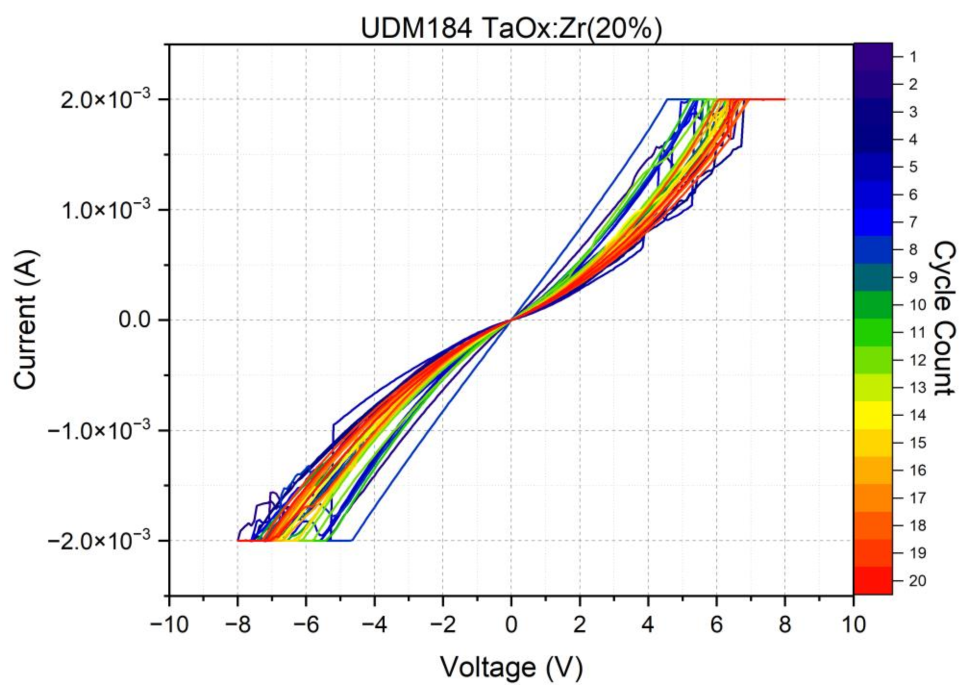

Figure 4.12: Linear I-V of Sample 184 (12:3)

Figure 4.12 shows the same pinching observed in the previous sample. Both have a low initial resistance before forming and SET. Figure 4.13 shows the logarithmic I-V for the same data contained in Figure 4.12.

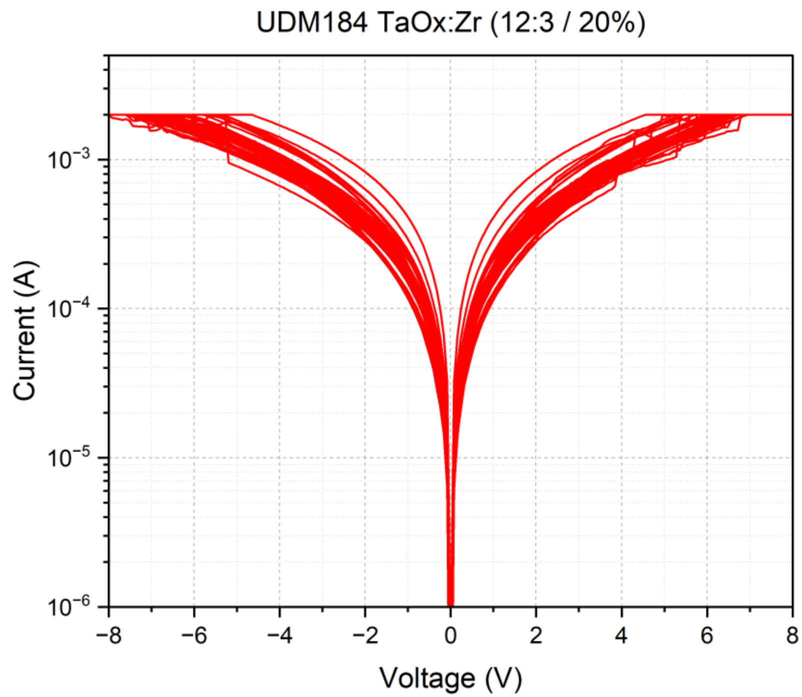

Figure 4.13: Logarithmic I-V of Sample 184 (12:3)

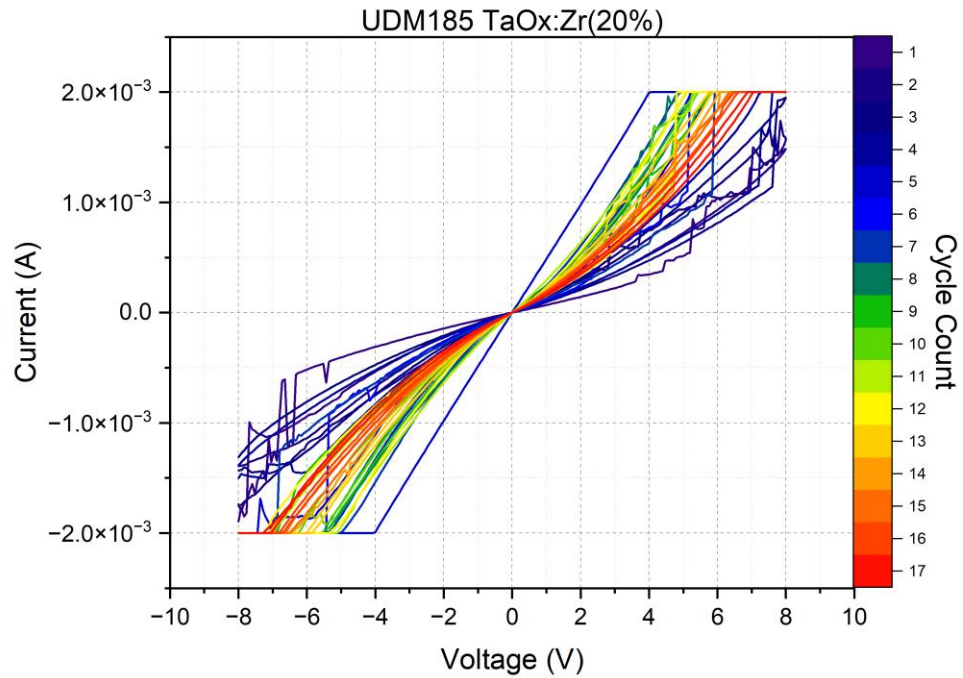

Figure 4.14: Linear I-V of Sample 185 (12:3)

The behavior shown in Figure 4.14 for sample 185 is much like the behavior shown in previous figures. The low number of cycles and quick pinch off of the hysteresis loops seems indicative of low oxygen vacancy mobility. Figure 4.15 shows the same data contained in Figure 4.14 on a log-scale. The same behavior shows up again in Figure 4.16 and Figure 4.17 showing the same behavior in sample 186.

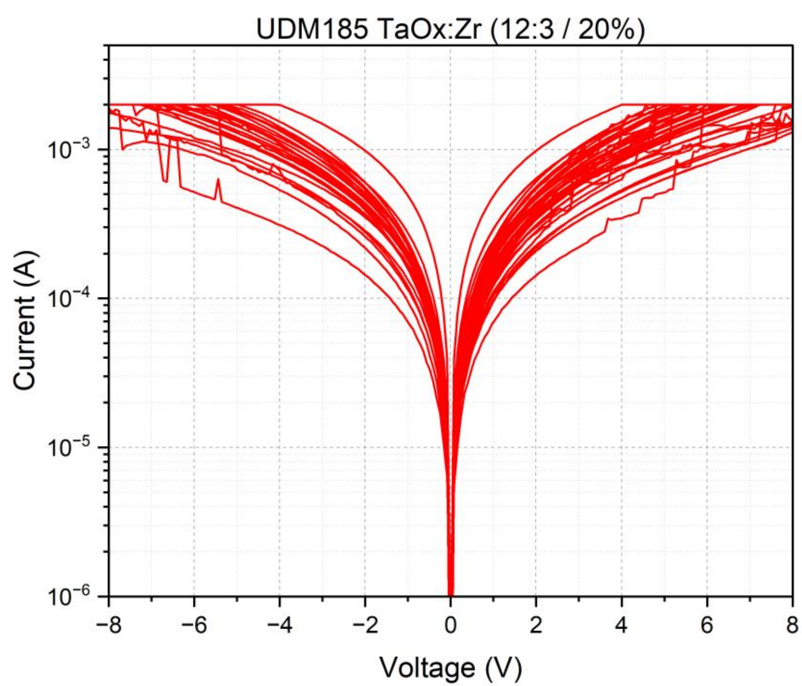

Figure 4.15: Logarithmic I-V of Sample 185 (12:3)

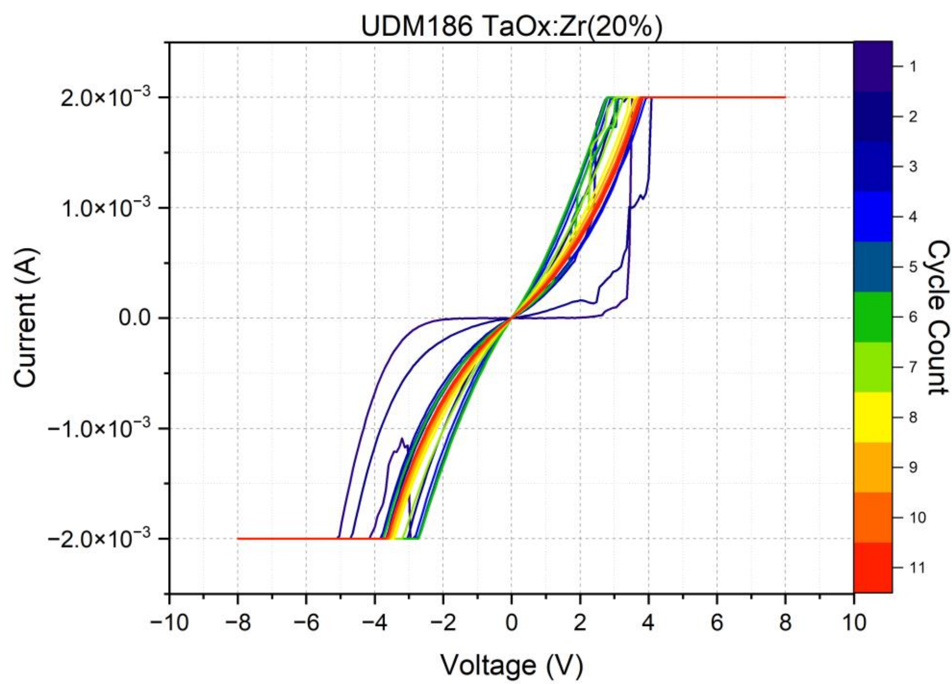

Figure 4.16: Linear I-V of Sample 186 (12:3)

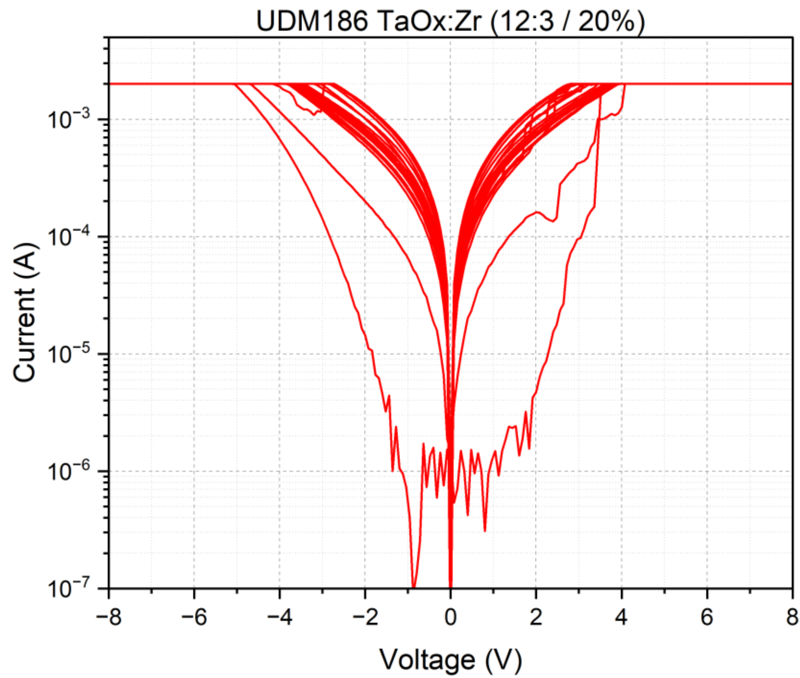

Figure 4.17: Logarithmic I-V of Sample 186 (12:3)

Samples 201 and 202 showed much higher required voltages and current to achieve switching. In the case of sample 201, the current compliance required increased to 10mA and switching only occurred one time at cycle 4. In cycles 1 through 3 the device showed near behavior more like a diode than what is expected of a memristor. When the curve for cycles 1 to 3 of Figure 4.19 are inverted. They mimic very closely the example of diode behavior shown in Figure 4.18. This leads me to believe that there is some issue with structure of the devices or if not the physical geometry of the devices, then the composition of the devices. The diode like behavior exhibited was not unique to sample 201 but was present on various devices across all the samples to varying degrees. Sample 202 showed the worst results of all devices requiring both ±15 V to show any switching as well as an increase in the current compliance to 20 mA.

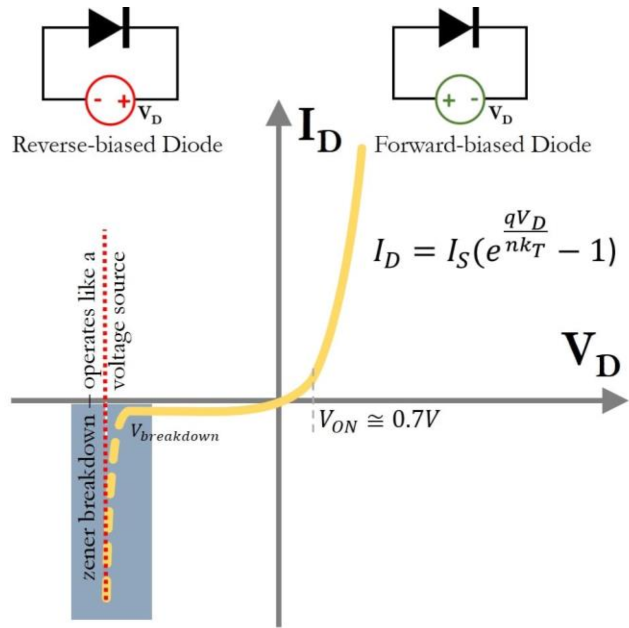

Figure 4.18: Example diode I-V curve for comparison [35]

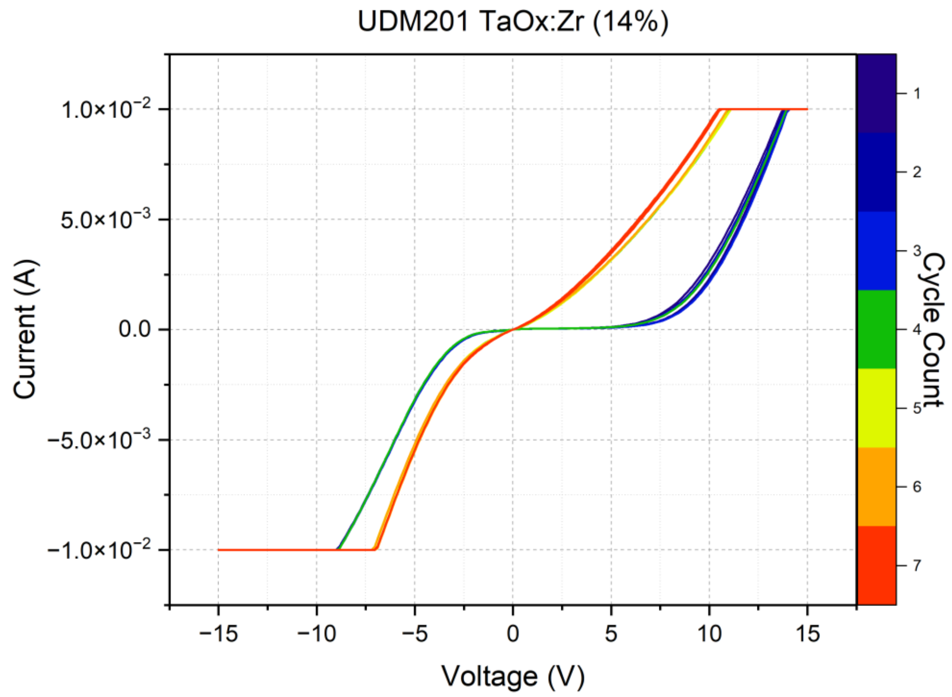

Figure 4.19: Linear I-V of Sample 201 (12:2)

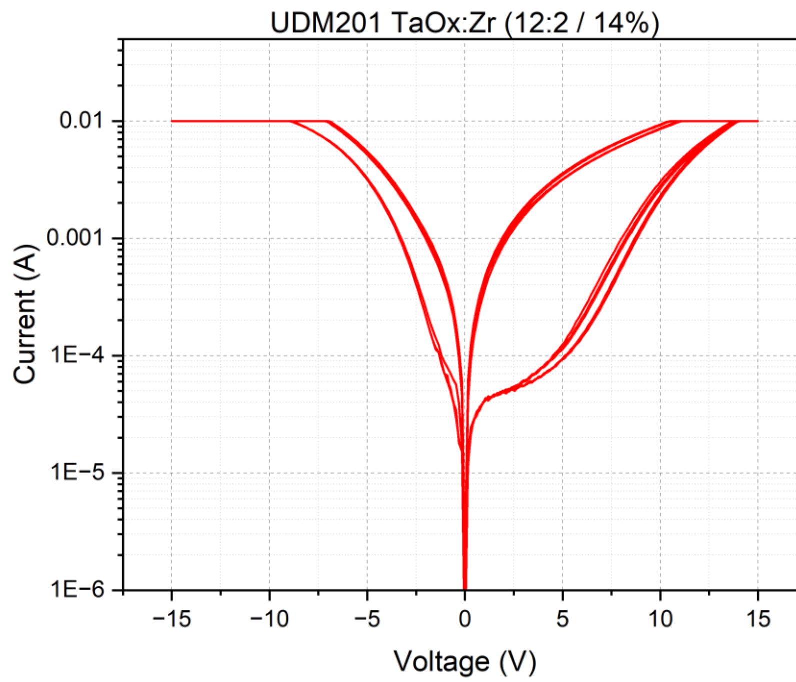

Figure 4.20: Logarithmic I-V of Sample 201 (12:2)

Figure 4.20 is the logarithmic current scaling of the data in Figure 4.19.

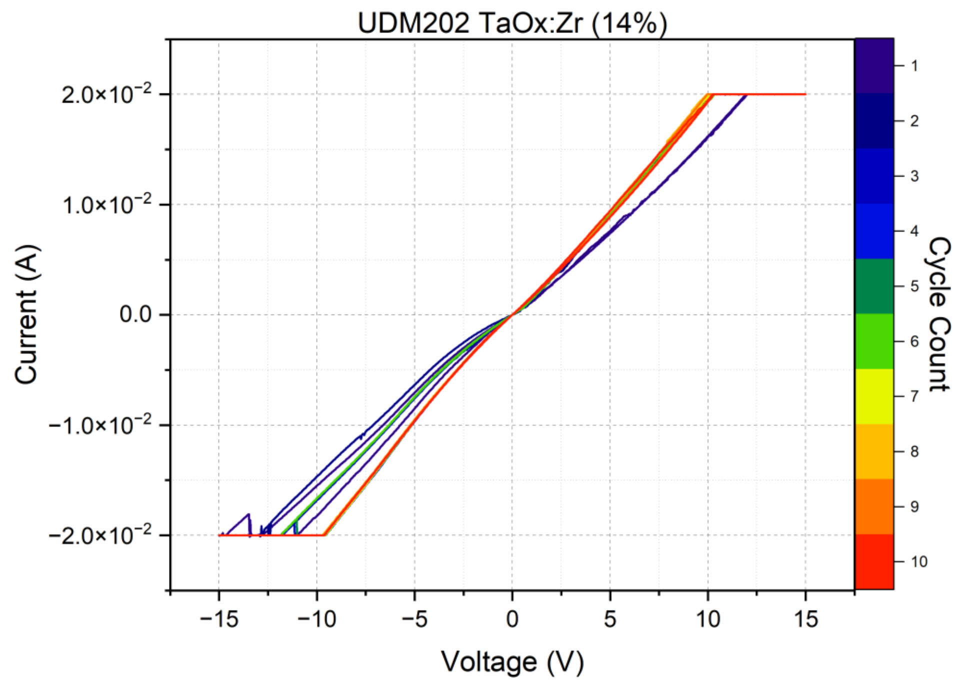

Figure 4.21: Linear I-V of Sample 202 (6:1)

Figure 4.21 shows the I-V characteristics of sample 202. This sample has the same ratio of Ta_2O_5 to Zr seen in sample 201 but the layers were grown in thinner overall groups. Figure 4.22 shows the logarithmic form of the data in Figure 4.21.

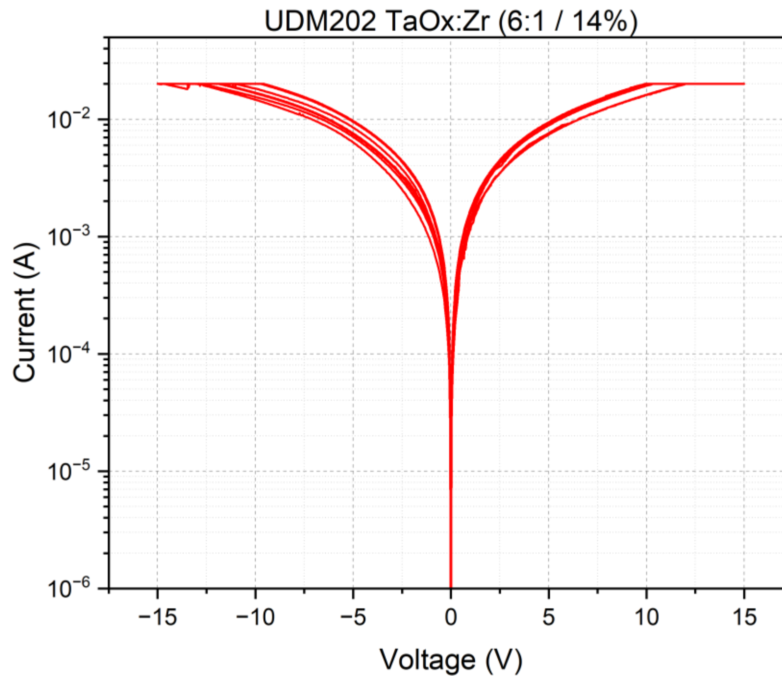

Figure 4.22: Logarithmic I-V of Sample 202 (6:1)

Compared to other reported results on Ta_2O_5 and Zr devices, these results were less than satisfactory. While the conductivity did increase with the introduction of Zr doping layers. The overall performance of these devices decreased in nearly all other useful metrics. Device endurance, switching voltage, current compliance levels, ON/OFF ratios, number of potential intermediate states, device-to-device and cycle-to-cycle variability all decreased rather significantly. C2C variability was often so poor that during cycles where the devices were supposed to transition from HRS to LRS and vice versa, they would exhibit the opposite behavior either becoming less resistive when entering the HRS or more resistive in the LRS. Many devices simply did not switch at all. With the number of samples created for this study it leads me to believe that there is some problem with either the fabrication process of the devices or some other such variable which was not accounted for.

Table 2. Cumulative Results of Doped Ta_2O_5 Testing and Analysis

Resistance @ SET/RESET	UDM182 (9:6) (40%)	UDM184 (12:3) (20%)	UDM185 (12:3) (20%)	UDM186 (12:3) (20%)	UDM201 (12:2) (14%)	UDM202 (6:1) (14%)
LRS μ	3605 Ω	3927 Ω	3969Ω	2167 Ω	23925 Ω	566 Ω
LRS σ	736 Ω	538 Ω	1313 Ω	564 Ω	27956 Ω	38 Ω
LRS σ^2	542703 Ω	290334 Ω	1.7+E6 Ω	318646 Ω	7.8+E8 Ω	1506 Ω
LRS Max	5393 Ω @ 6th cycle	4792 Ω @ 3rd cycle	7490 Ω @ 1st cycle	3054 Ω @ 3rd cycle	54053 Ω @ 3rd cycle	676 Ω @ 1st cycle
LRS Min	2741 Ω @ 4th cycle	2944 Ω @ 11th cycle	2599 Ω @ 7th cycle	1518 Ω @ 6th cycle	1414 Ω @ 6th cycle	547 Ω @ 3rd cycle
HRS μ	485024 Ω	4348 Ω	5222 Ω	15826 Ω	6358 Ω	624 Ω
HRS σ	1314 Ω	826 Ω	2530 Ω	40803 Ω	41681 Ω	94 Ω
HRS σ^2	1.7+E6Ω	682684 Ω	6.4+E6 Ω	1.7+E9 Ω	1.7+E7 Ω	8869 Ω
HRS Max	6945 Ω @ 4th cycle	6014 Ω @ 5th cycle	12846 Ω @ 1st cycle	138677 Ω @ 1st cycle	9721 Ω @ 1st cycle	785 Ω @ 2nd cycle
HRS Min	3281 Ω @ 17th cycle	2358 Ω @ 8th cycle	2009 Ω @ 5th cycle	2263 Ω @ 8th cycle	1794 Ω @ 7th cycle	519 Ω @ 10th cycle
Average Cycle #	19	19	13	15	6	~10 Likely not reliable
R_{OFF}/R_{ON}	~134	~1.1	~1.3	~7.3	-	-

4.2.2 TEM and EDS Data

Due to the overall failure of the devices, it was concluded that further compositional and structural analysis was needed to diagnose the issue. Due to time constraints, the best and worst devices were selected in attempts to analyze any differences that could contribute to the large variability in behavior. Samples 186 and 202 were selected and subject to STEM and EDS analysis to identify an issue with either sample. As can be seen in Figure 4.23, there was not any apparent damage to the device layers. The significant carbon presence in the C presence spectra is due to the addition of a carbon cap during TEM sample prep. Of note however, was the significant Zr signature in the oxygen exchange layer. The Ta oxygen exchange layer was grown independently from the TaOx:Zr layers. This is evidence of Zr diffusion into the exchange layer. This could be contributing to some of the observed behavior.

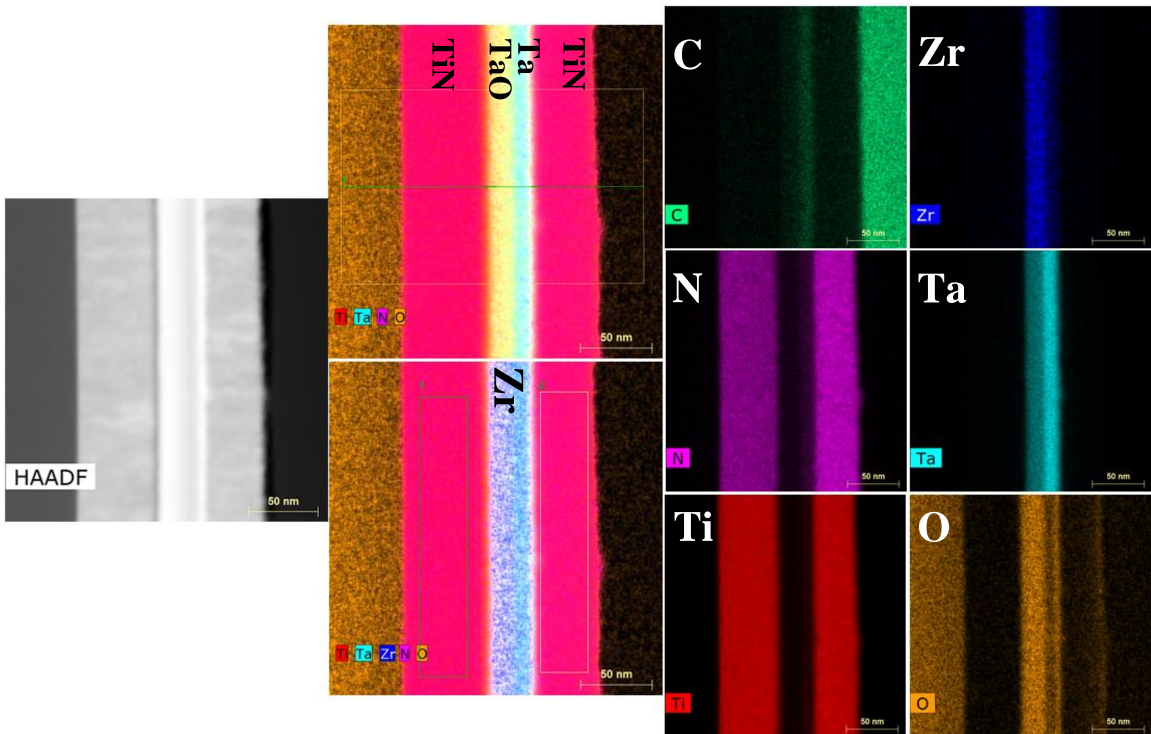

Figure 4.23: TEM and EDS images of sample 186

This can be confirmed with the elemental line EDS analysis in Figure 4.24. Of note in Figure 4.24 as well is the significant oxygen presence at the top electrode interface at approximately point

number 600. This could either be due to the exchange layer functioning as intended and transporting or creating V_o in the switching layer by absorbing oxygen atoms or it could be a remnant from the conductive filament formation rupturing that could not be repaired. Another possibility is that during the time between the deposition of the exchange layer and the top electrode, exposure to atmosphere caused a contaminant oxide layer to form.

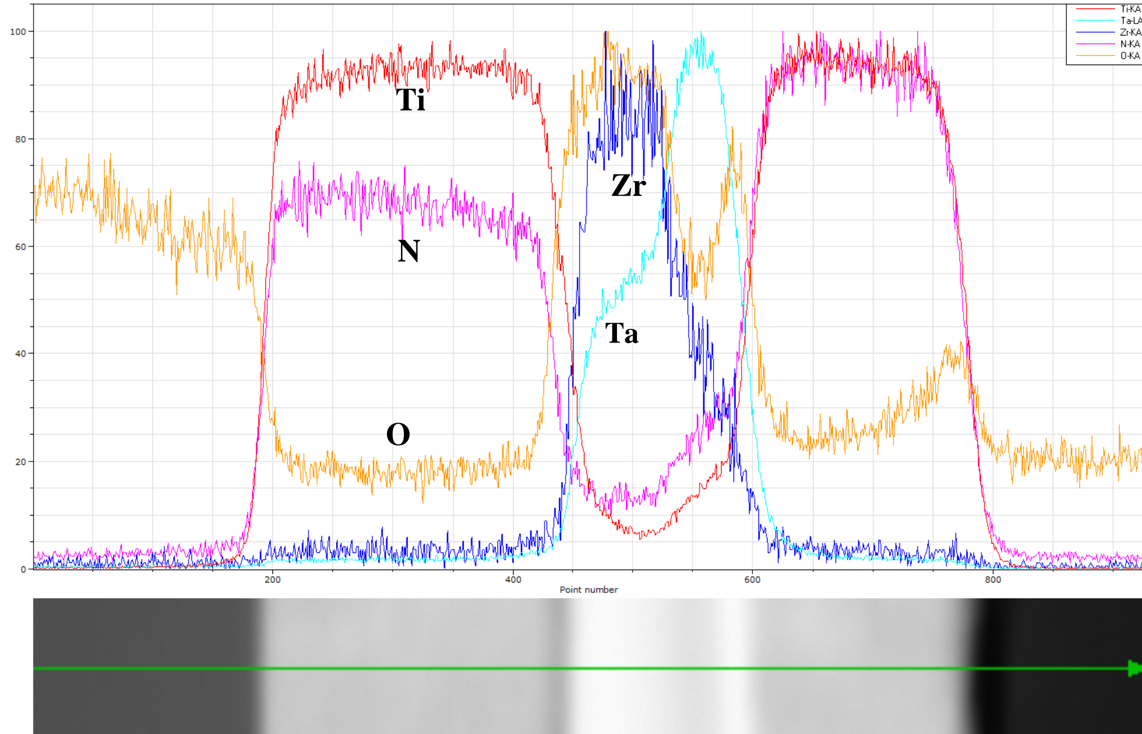

Figure 4.24: EDS Elemental Line Spectra of sample 186

Many of the problems mentioned with respect to sample 186 also apply to the STEM and EDS of sample 202. There is evidence of Zr diffusion in the oxygen exchange layer and a noticeable oxide layer presence at the top electrode interface but no noticeable damage to the structure otherwise. This can be seen in Figure 4.25 where the same Zr spectrum coloration is in the oxygen exchange layer. The bottom electrode also has a much higher oxygen concentration in the EDS spectra showing that some of the high voltage behavior could be in part due to the development of TiO_2 during electrode deposition which was the cause of much headache and

reasoning behind so much of the optimization of the TiN deposition process leading into this experiment. Otherwise, there appears to be no noticeable difference between the two samples seen in the TEM and EDS analysis.

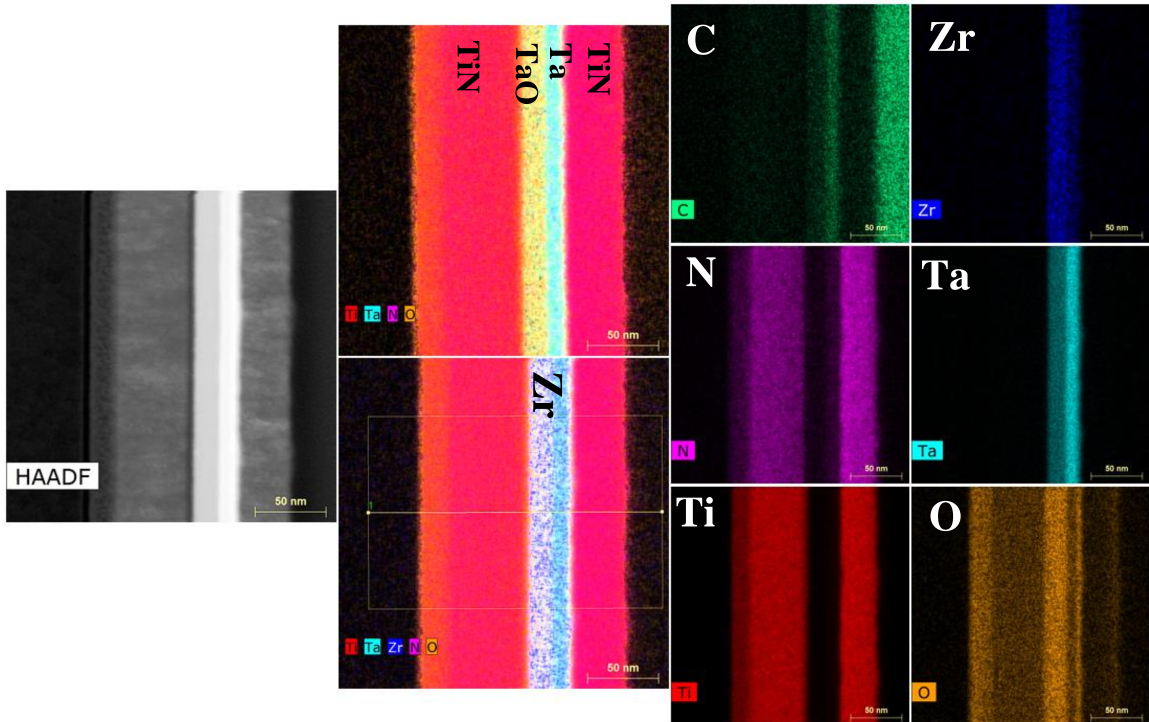

Figure 4.25: TEM and EDS images of sample 202

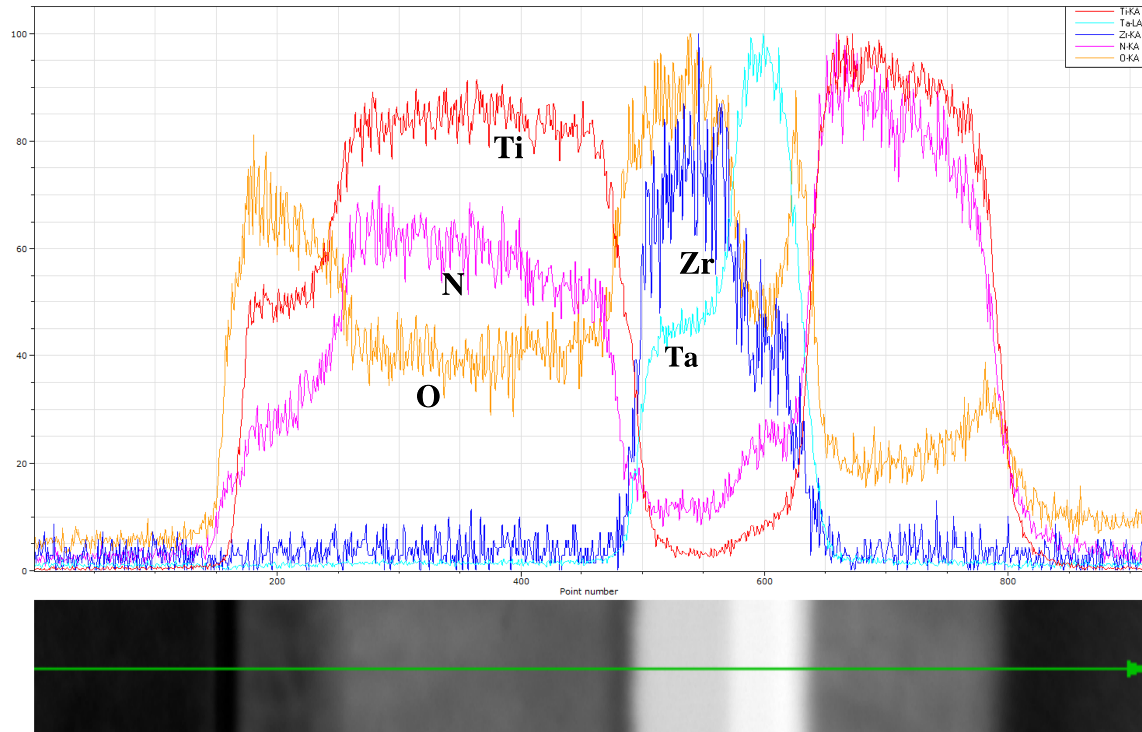

Figure 4.26: EDS Elemental Line Spectra of sample 202

The elemental line spectra shown in Figure 4.26 also confirms the presence of Zr in the Ta oxygen exchange layer. A relatively large spike in the O spectra at the top electrode interface confirms oxide formation in the Ta layer. The analysis, while helpful, ultimately did not conclude why the performance of the devices was so poor. Further testing on the devices would be necessary to reach a conclusion as to the cause of error and will be conducted in further studies.

CHAPTER 5

CONCLUSION

5.1 Summary

In this thesis, the concentration of Zr in Ta_2O_5 memristor devices grown by ALD was varied to determine the effect of the ZrO_2 in the bilayer structure. The theory put forth was that the Zr doping layers would increase device conductivity and oxygen vacancy mobility through the switching layer. A literature review of memristors as a technology helped establish the baseline for developing the material system used for this thesis. Then using several techniques including ALD, DC magnetron reactive sputtering, and e-beam evaporation the doped samples were fabricated. Extensive electrical characterization, SEM and TEM imaging were used to analyze the behavior of the devices and their operation. This included basic voltage sweeps using a B1500A Semiconductor Analyzer, EDS via TEM and general compositional analysis. It also covered some previous work done on undoped samples provided by SUNY Polytechnic Institute to use as a reference when measured on the same instruments using the same techniques. These devices showed stable switching and performance as expected from a Ta_2O_5 device and served as a good reference. The doped devices, however, showed very unreliable switching, higher voltage and current requirements, low endurance, rapid state decay into a pinched hysteresis, and evidence of significant levels of Zr diffusion into the exchange layers.

Based on the information contained within this study my preliminary conclusions are that the increase in conductivity seen with the introduction of Zr into the active layer may eliminate the need for oxygen vacancies to form a conductive filament to facilitate current flow. This would mean a reduction in the overall switching performance as the devices rely on conductive filament formation to store their state. Another possibility is that the increased device size and geometry could be leading to the unforeseen large increase in initial conductivity resulting in the same problem. Alternatively, the Zr diffusion into the oxygen exchange layer could have caused a

reduction in available oxygen vacancies causing the device to never form properly. However, there is not enough data to conclude that this is the case currently. Preliminary results with a 1T1R configuration with the doped devices show better control over higher voltage current fluctuations but show no change in the SET/RESET or forming voltage nor the overall power efficiency. In conclusion, further work and study is needed to determine the failure method. These devices may offer great insight into the operational failure and electrochemical operation of doped TaOx in future studies and provide useful information for a better design of the memristive devices.

5.2 Future Work

In continuing this research, a new set of devices with smaller device areas should be constructed to increase the resistance of the device in response to the increased conductivity due to the Zr dopant in TaOx. Introduction of a 1T1R structure for the devices to limit damage would also be useful to provide stable performance. Ultimately, the goal would be to identify the cause of failure in the devices to improve performance. The end goal of the research is reliable switching operation with high endurance to achieve excellent neuromorphic computing capability for integration with modern CMOS technologies.

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APPENDIX A

Undoped Ta_2O_5 Electrical Data

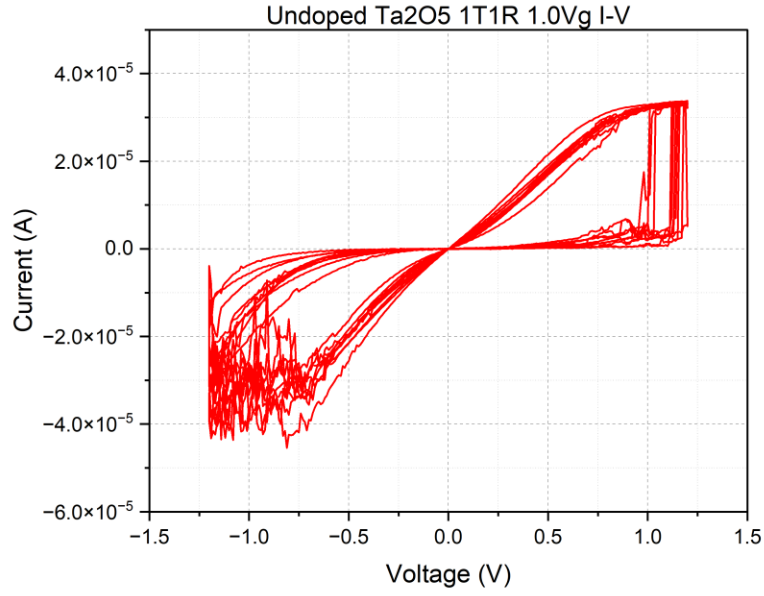

Figure A.1 Undoped TaOx 1T1R Linear I-V data at 1.0Vg

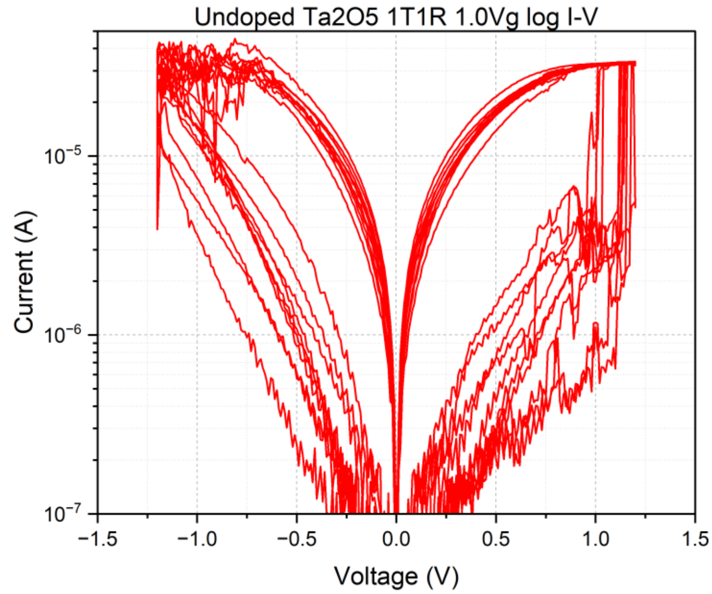

Figure A.2 Undoped TaOx 1T1R Logarithmic I-V data at 1.0Vg

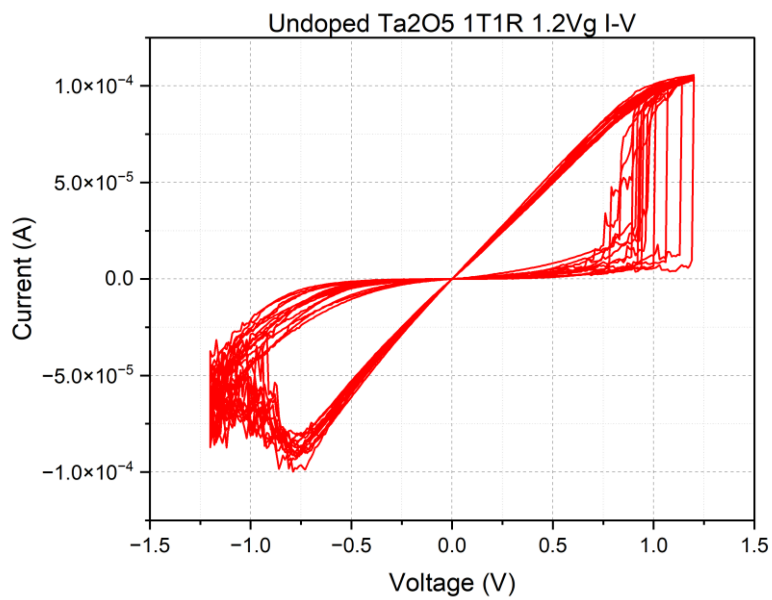

Figure A.3 Undoped TaOx 1T1R Linear I-V data at 1.2Vg

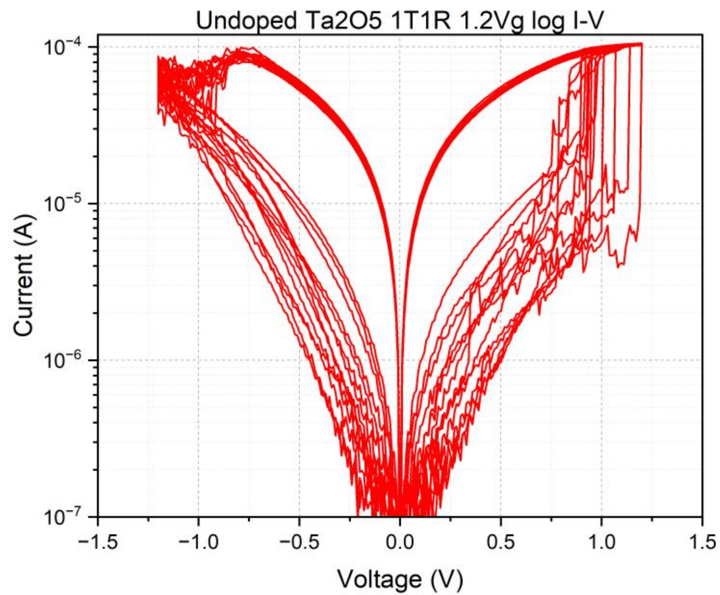

Figure A.4 Undoped TaOx 1T1R Logarithmic I-V data at 1.2Vg

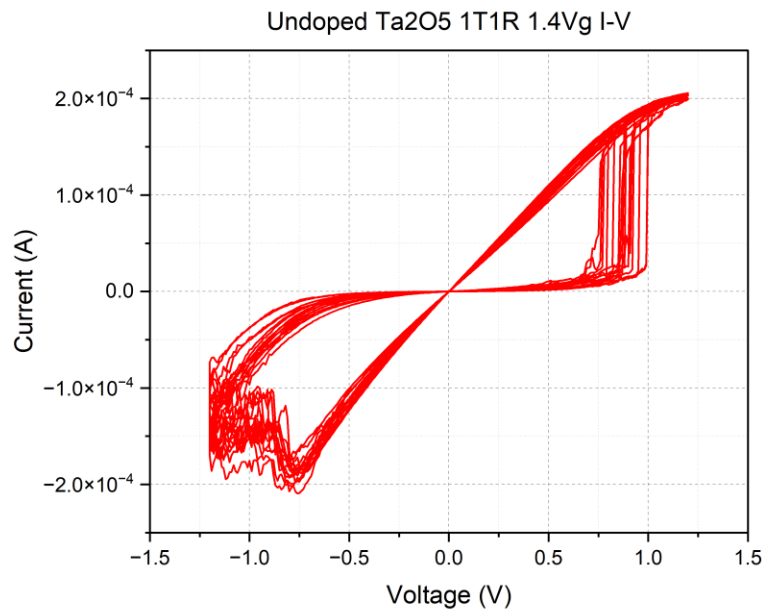

Figure A.5 Undoped TaOx 1T1R Linear I-V data at 1.4Vg

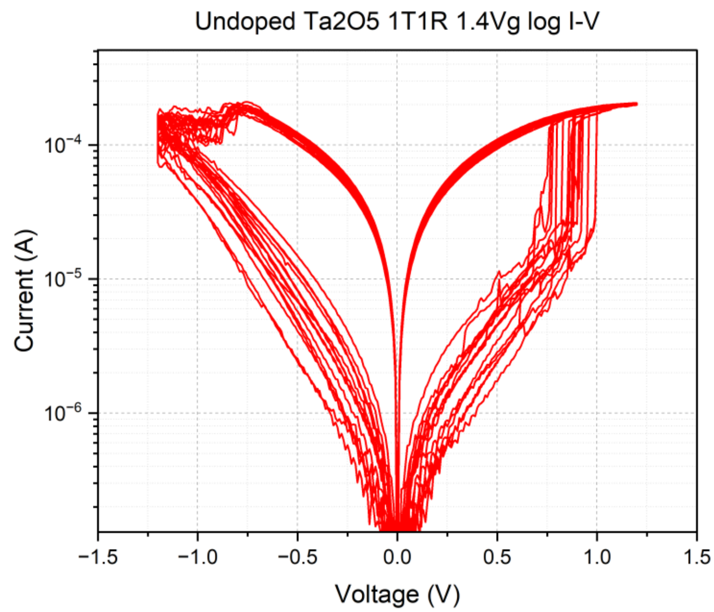

Figure A.6 Undoped TaOx 1T1R Logarithmic I-V data at 1.4Vg

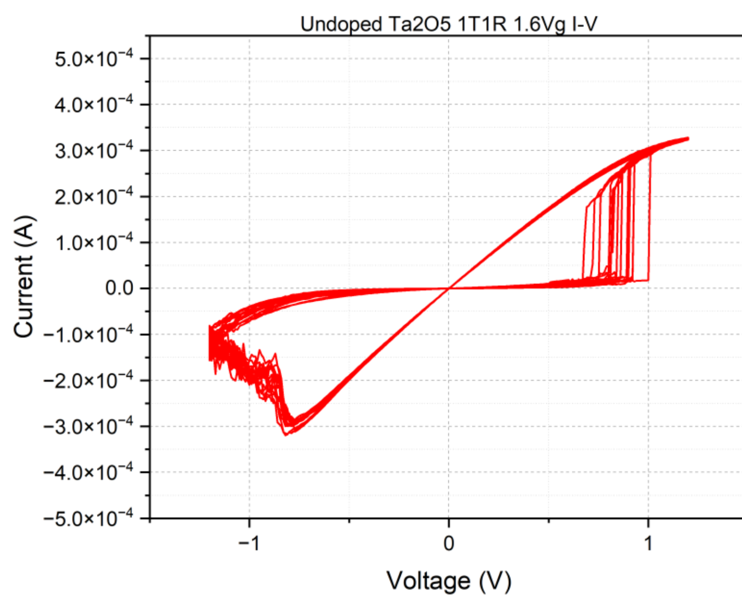

Figure A.7 Undoped TaOx 1T1R Linear I-V data at 1.6Vg

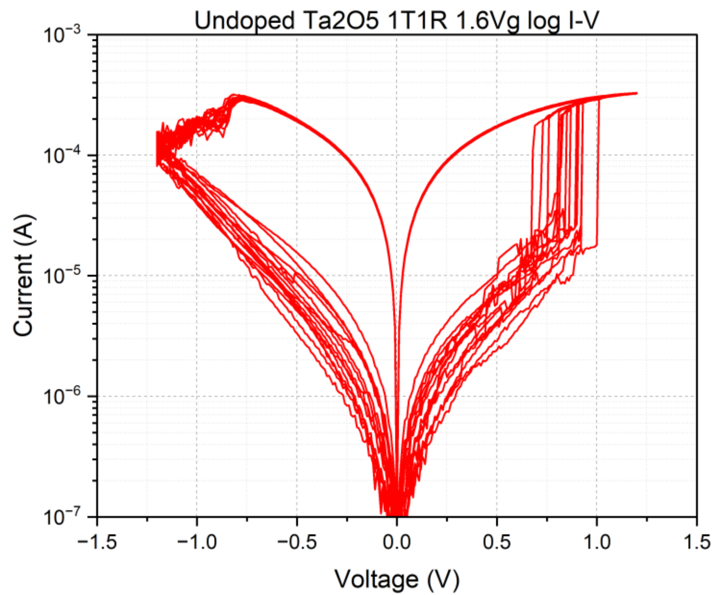

Figure A.8 Undoped TaOx 1T1R Logarithmic I-V data at 1.6Vg

APPENDIX B

Details of the Fabrication Processes Developed

The procedure begins with surface degreasing of a fresh 300 μm thick, 2-inch diameter, highly resistive (undoped) Si wafer by using cleaning step A. The cleaning step A is performed at 500 RPM, and it consists of Acetone gun spray, Acetone bottle spray, Isopropanol bottle spray, and N_2 blow drying for 15 seconds each. After that, dehydration bake process is conducted at 110 °C for 75 seconds. A layer of 50 nm thick TiN layer is deposited by magnetron sputter deposition process at room temperature from a Ti sputter target under Argon plus Nitrogen pressures. Next, a negative photolithography process is conducted to open specific area on the wafer surface for the TiN ICP etch process. A layer of photoresist NR9-1000PY is coated on the wafer at 4000 RPM. The spinning duration and the ramping speed of this process are set to 30 seconds and 400 RPM. Then, the wafer is baked at 112 °C for 120 seconds. After that, the wafer is exposed to a UV light source (365 - 405 nm, 10 mW/cm ^{2}) through Mask14 Bottom Metal mask for 15 seconds. For this NR9-1000PY process, a post exposure bake process is required for 60 seconds at 112 °C. After the post exposure bake, the wafer is soaked and developed in a fresh RD6 solution for 15 seconds, and then, rinsed three times in an automatic DI water rinse tank. After drying the wafer, the wafer is inspected under the optical microscope and cleaned in the O_2 plasma asher for 4 minutes. Then, the TiN ICP etch process is carried out. After that, the photoresist NR9-1000PY is cleaned by the cleaning step A, and then, further cleaning in the O_2 plasma asher is carried out for 4 minutes with a 200 W of RF power.

After the TiN bottom metal patterning process, a 10\50 nm thick Ti\Pt bottom metal pad protecting layer is achieved for protecting the bottom TiN probing pad structures during another TiN etch process for pattering the top TiN electrode structures. A layer of photoresist SF-11 is then coated on the wafer at 4000 RPM. The spinning duration and the ramping speed of this

process are also set to 30 seconds and 400 RPM. Next process is SF-11 bake of the wafer at 250 °C for 120 seconds. After the SF-11 bake process, a layer of photoresist S1813 is coated on the wafer at 4000 RPM. The spinning duration and the ramping speed are same with the SF-11 process. Then, 1813 bake process is conducted at 110 °C for 75 seconds. After that, the wafer is exposed to the UV light source through Bottom Metal Pad mask for 6 seconds. Next process is developing of S1813, and it is carried out with a mixed solution of 351:DI water (1:5). The solution is sprayed onto the spinning (50 RPM) wafer three times during total 50 seconds of total developing time. Then, the wafer is rinsed with a DI water spray and dried with a N_2 blower. After drying process, the photoresist S1813 patterns are visually inspected under the optical microscope to ensure the quality of the patterns all over the wafer. After that, the wafer is exposed to a DUV light source (16 mW/cm 2) for 320 seconds. For developing SF-11, the wafer is soaked in a fresh 101A developer for 100 seconds, and then, rinsed three times in the automatic DI water rinse tank. After drying the wafer by using the N_2 blower, the bottom metal pad patterns are inspected under the optical microscope again. Once satisfied patterns are acquired, possible residue of the photoresist on the patterns is cleaned in an O_2 plasma asher for 4 minutes. Then, the bottom metal pad layer deposition is conducted by E-beam evaporation process. After the deposition, a metal lift off process and a photoresist removal process are carried out. First, the sample wafer is soaked in a fresh Acetone for 5 minutes, and then, the cleaning step A is performed for removing unwanted metal layer and the photoresist S1813 from the wafer surface. When the metal thin film is completely removed from unwanted surface area, the sample wafer is soaked in a fresh 1165 solution at 90 °C for 4 minutes for removing the photoresist SF-11 completely. After that, the wafer is rinsed three times in the automatic DI water rinse tank. After drying the wafer, the bottom metal pad patterns are inspected under the optical microscope again. Once satisfied patterns are acquired, possible residue of the photoresist on the wafer surface is cleaned in the O 2 plasma asher for 4 minutes.

Next step is the depositions of TaOx and Ta thin film layers. Those are performed by ALD and e-beam evaporation processes. After that, a layer of S1813 is coated, baked, exposed through Mask14 Oxide Etch mask, and then, developed. After drying the wafer, the wafer is inspected under the optical microscope and cleaned in the O_2 plasma asher for 4 minutes again. Then, Ta/TaOx ICP etch process is performed, and then, the cleaning step A is performed for removing the S1813 photoresist. After drying the wafer, the thin film patterns on the wafer are inspected under the optical microscope and cleaned in the O_2 plasma asher for 4 minutes again.

Next step is the top TiN layer deposition and pattering. Another layer of 50 nm thick TiN is sputter deposited, and then, another NR9-1000PY lithography process is carried out for etching the top TiN layer from unwanted surface area of the wafer. Once the NR9-1000PY lithography process is done with Mask14 Top Metal mask, another TiN ICP etch process is carried out, and then, the photoresist NR9-1000PY is cleaned by the cleaning step A. Then, the fabrication procedure is finished, and the TiN – TaOx\Ta - TiN based memristor structures on the wafer are ready to be characterized.