DESIGN OF POWER-SCALABLE GALLIUM NITRIDE CLASS E POWER AMPLIFIERS

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DESIGN OF POWER-SCALABLE GALLIUM NITRIDE CLASS E POWER AMPLIFIERS

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ABSTRACT

DESIGN OF POWER-SCALABLE GALLIUM NITRIDE CLASS E POWER AMPLIFIERS

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The need for high power, highly efficient, multi-band and multi-mode radio frequency (RF) and microwave power amplifiers in the commercial and defense wireless industries continues to drive the research and development of gallium nitride (GaN) devices and their implementation in the receiver and transmitter lineups of modern microwave systems. Unlike silicon (Si) or gallium arsenide (GaAs), GaN is a direct wide bandgap semiconductor that permits usage in high voltage and therefore high power applications. Additionally, the increased saturation velocity of GaN allows for operation well into the super high frequency (SHF) portion of the RF spectrum. For the power amplifier designer, active devices utilizing GaN will exhibit power densities almost an order of magnitude greater than comparably sized GaAs devices and almost two orders of magnitude greater than Si devices. Not only does this mean an overall size reduction of an amplifier for a given output power, but it allows GaN to replace specialized components such as the traveling-wave tube (TWT) and other circuits once deemed impossible to realize using solid-state electronics. Designs utilizing GaN in amplifiers, switches, mixers, etc., are able to meet the continually shrinking size, increased power, stringent thermal, and cost requirements of a modern microwave system.

There are two relatively straight forward methods used to investigate the intrinsic power scaling properties of a GaN high-electron-mobility transistor (HEMTs) configured as a common source amplifier. The first method involves sweeping the applied drain to source voltage bias and the second method involves scaling the physical size of the transistor. The prior method can be used to evaluate fixed sized transistors while the latter method requires an understanding of the obtainable power density for a given device technology prior to fabrication. Since the power density is also a function of the drain to source voltage bias, an initial iterative component of the design cycle may be required to fully characterize the device technology. If a scalable nonlinear device model is available to the designer, the harmonic balance simulator in most computer aided design (CAD) tools can be used to evaluate device parameters such as the maximum output power and power added efficiency (PAE) using large signal load pull simulations.

The circuits presented in this thesis address two power amplifier design approaches commonly used in industry. The first approach utilizes commercially available bare die GaN transistors that can be wire-bonded to matching circuitry on a printed circuit board (PCB). This technique is known as hybrid packaging. The second approach utilizes a fully integrated design or monolithic microwave integrated circuit (MMIC) and the process design kit (PDK) used to design, simulate and layout the power amplifier circuitry before submission to a foundry for fabrication. In both cases, the nonlinear transistor models are used to investigate the power scalability of class E mode GaN power amplifiers and the techniques used to implement such circuits. The design, results, and challenges of each approach are discussed and future work is presented.

To the scientists, mathematicians and engineers who came before us, for we truly stand on the shoulders of giants.

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I would like to thank Dr. Guru Subramanyam, my undergraduate and graduate advisor, for all the support he has given me since my first semester at the University of Dayton in the fall of 2008. If it were not for his desire to see me succeed in every academic and professional endeavor I have undertaken, I would not have pursued an advanced degree in electrical engineering. He graciously welcomed me into his microwave engineering group as a graduate student after providing me with a solid foundation in microelectronics as an undergraduate. I cannot thank him enough for everything that he has done for me and the University of Dayton.

I am thankful for all of my family and friends; past and present, who have helped me become the person I am today. It takes a caring individual to have a genuine interest in another's obsession with electronics. Likewise, thank you to all of my professors who have encouraged me to go beyond the classroom and apply what I have learned. Additionally, I would like to thank all of my former coworkers and mentors while employed as an intern and co-op student; the practical work experience gained under your supervision has been an invaluable asset and a driving force for my future.

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CHAPTER I

INTRODUCTION

1.1 Background

The enduring need for higher power and highly efficient radio frequency (RF) and microwave power amplifiers for use in the receiver and transmitter lineups of base stations, cellular handsets, and defense related applications continues to drive the research and development of new semiconductor materials and transceiver architectures capable of meeting the stringent spectral requirements of multi-band and multi-mode communications systems. A new trend of spectral aggregation for wireless standards such as long term evolution (LTE) has forced handset manufactures to design RF front-ends capable of tuning across wide portions of the usable RF spectrum. Likewise, legacy wireless standards still in use today force the requirement of backwards compatibility either in the low or high bands of the service provider's licensed frequency spectrum. Traditional technologies such as laterally diffused metal oxide semiconductor (LDMOS) and gallium arsenide (GaAs) have dominated the commercial and defense power amplifier markets due to their maturity and therefore relatively low implementation cost; however, both suffer from either physical limitations in terms of maximum usable frequency and/or low power density [2]. A potential solution to satisfy the simultaneous requirements of high frequency and power is the application of microwave circuitry utilizing gallium nitride (GaN).

Gallium nitride is a direct wide bandgap semiconductor with a high saturation velocity and voltage breakdown [3]. Not only are GaN devices capable of operating well past the super high frequency (SHF) portion of the RF spectrum, commonly denoted from 3 GHz to 30 GHz, but the high power density of GaN has enabled its use in applications involving radar, satellite communications, telemetry, etc., that were once deemed impractical or unreliable for solid-state electronics [4, 5]. The low carrier scattering of GaN also makes it an ideal semiconductor for applications requiring low noise amplification [6, 7, 8]. When paired with GaN's high voltage breakdown, low noise amplifiers (LNAs) utilizing GaN may not even require a dedicated limiter stage traditionally used to protect the LNA from close proximity transmitters [9]. Likewise, the large voltage swings necessary to support the switched mode class E power amplifier can be comfortably accommodated in designs utilizing GaN [10]. The tunable and reconfigurability aspect of modern RF front-ends is also an important subject concerning GaN. Research into the usage of GaN based high power RF switches and varactors provide further opportunities for GaN to supplant LDMOS and GaAs altogether in one monolithic microwave integrated circuit (MMIC) solution.

1.2 Power Scaling

There are two relatively straight forward processes used to investigate the intrinsic power scaling properties of GaN. The first involves adjusting the drain to source voltage bias and the second involves changing the physical size of the transistor. The drain bias scaling technique is used if the transistor can operate over a wide range of supply voltages. For a common source GaN power amplifier, it has been shown that by increasing the drain bias from 30V to 40V for a fixed device periphery, the power density will increase by approximately 2W/mm [11]. Alternatively, if a design can accommodate a larger transistor, the increased device size will result in a higher output power for a fixed power density [12]. In both cases, the maximum output power is obtained using large signal load pull techniques for a given set of swept load and source impedances in order to account

for the device parasitics [10, 13]. If wide band and high efficiency operation are also desired, novel techniques such as parallel unit cell loading of a GaN transistor with a bondwire transformer have been demonstrated [14]. The usage of GaN in more complex power amplifier architectures, such as a reconfigurable Doherty for high efficiency operation, is also possible [15]. The Doherty configuration has demonstrated efficiencies greater than 50% at the peak output power level as well as in the 6 dB back-off condition. In any case, it is up to the designer to select the technique appropriate based on the system specifications.

A summary of the results obtained from researched techniques used to implement power scalable GaN PAs is shown below in Table 1.1.

Table 1.1: Researched GaN Power Scaling Techniques

Method	Power [W]	PAE [%]	Bandwidth	Packaging
Drain Bias Scaling [11]	5 - 7	50 - 57	16%	MMIC
Device Periphery Scaling [12]	79 - 145	74	-	Hybrid
Parallel Bondwire Transformer [14]	44 - 72	60 - 69	39%	Hybrid
Reconfigurable Doherty [15]	4 - 16	50	45%	Hybrid

1.3 Scope

The main objective of this thesis is to develop an integrated microwave power amplifier capable of electronically adjusting the output power while maintaining high efficiency class E mode operation. In order to accomplish this goal, initial research into the reactive power splitter/combiner circuitry, which is commonly used to combine parallel transistors, is performed [2, 13, 16, 17, 19]. From this research, it is proposed to integrate high power series-shunt microwave switches at the split ports of the combiner in order to effectively isolated the input and output of each parallel stage when a power device is turned off. The dc and RF isolation is necessary so that the optimized input

and output matching networks, which have been designed for the class E mode, are minimally impacted by the parasitic nature of an inactive device and its matching networks. In addition, a tunable high pass matching network is proposed to correct the mismatch at the output ports of the combiners and is electronically tuned based on the number of active parallel power stages. However, the proposed combiner techniques can also be implemented for other operating modes and is not restricted to class E amplifiers. It is expected that the overall output power of the reconfigurable amplifier will scale with the number of active devices while maintaining the desired power added efficiency.

The MMIC approach allows for the integration of GaN microwave switches and the novel reactive combiner technique described above. Additionally, PCB hybrid packaged amplifier circuits using commercially available bare die GaN transistors, fixed distributed matching and combining networks are designed and simulated to demonstrate the intrinsic power scaling nature of the selected gallium nitride foundry process. A total of six class E mode PCB power amplifiers are designed, simulated, and laid out on a selected microwave substrate. Three of the amplifier circuits investigate the power scaling of the selected GaN foundry process by progressively doubling the unit cell size. The other three circuits incorporate the use of Wilkinson power splitters to combine smaller unit cells to produce an effective device periphery of an single larger device.

1.4 Outline

A brief discussion of semiconductor device materials and system level challenges associated with RF and microwave power amplifier design is presented in chapter 1. An introduction to GaN device technology is also presented as well as its role in high power applications. Chapter 2 documents the design approach used to develop hybrid packaged and MMIC class E mode power amplifiers using discrete and integrated circuitry. The hybrid packaging design is detailed in chapter 3 and the reconfigurable MMIC power amplifier is documented in chapter 4. Chapters 5 and 6 present the

simulation results of the hybrid and MMIC designs, respectively. Finally, chapter 7 concludes with a discussion of the GaN technology utilized including the benefits and disadvantages of each design approach as well as recommendations for future work regarding the integrated reconfigurable power scaling architecture.

CHAPTER II

CLASS E AMPLIFIER DESIGN TECHNIQUES

2.1 Switch Mode Power Amplifiers

The performance demands and specifications placed on the high power output stage of modern wireless communications systems have been a driving force behind the advancements in new semiconductor materials and the circuit design techniques used to improve amplifier linearity. The need for highly linear operation arises from the utilization of complex amplitude modulation formats, e.g. Long-Term Evolution (LTE), designed to improve spectral agility and data transfer rates. A traditional design approach such as the omnipotent class AB amplifier has long provided a compromise between linearity and power added efficiency (PAE). The class AB amplifier is able to closely match the linear performance of a class A amplifier while exhibiting PAEs greater than 65% [2]. However, this metric assumes that the input drive is large enough to push the amplifier into compression, typically referred to as the 1 dB compression point (P1dB), and therefore is either a sinusoidal input or a signal with a constant envelope. While the device is in compression, the transistor is no longer operating in the small signal or linear region of operation and produces a considerable amount of undesired harmonic content. For wireless standards that apply some form of amplitude modulation scheme with high peak to average power ratios (PAPR), the linearity requirement of the amplifier typically dictates the obtainable efficiency of a given design and it is not uncommon to operate the amplifier in 10 dB back off or greater with average PAEs of less than 20% [2]. It is clear that an

efficient alternative to the class AB amplifier is needed in order to reduce wasted power in the form of heat and therefore cost in cooling base stations as well as extending the battery life of subscriber handsets. The introduction of gallium nitride with its ability to withstand high drain to source voltage swings and high output power density has allowed amplifier designers to explore architectures that were otherwise overly complicated or unreliable using other semiconductor technologies.

The switch mode class E amplifier has traditionally been used in lower frequency designs where the transistor is biased in the pinched off state and turned on using only the time varying nature of the large signal input. An ideal switch is 100% efficient since the voltage and current at the output of the common source device are orthogonal with each other, meaning there is no voltage and current overlap resulting in power being dissipated by the device, i.e., out of phase voltage and current square waves. Additionally, since the transistor must be pushed into deep compression to have it completely turned on or off, the class E mode amplifier also requires a harmonic matching network capable of ensuring that no harmonic currents are delivered to the load that would otherwise detract from the overall efficiency of the amplifier [13]. This is done by presenting an open circuit to the harmonics, typically the second and third harmonics, at the output of the device. In reality, the drain to source capacitance of the device plays a role in this harmonic matching network and effectively sets the upper frequency limit of the amplifier as well as how efficiently the device will perform, typically no greater than 80 to 85% [2]. The class E mode amplifier is a combination of not only correctly biasing the device and maintaining that bias, but a waveform engineering problem inherent to switch mode amplifier design. It is clear that modulation schemes with a constant envelope will have no problem of taking advantage of the improved efficiency of the class E mode, but the amplifier cannot natively support amplitude modulated waveforms that require high degrees of linearity. Other techniques such as digital pre-distortion (DPD) and/or envelope tracking; a power supply modulation scheme used to obtain linear performance of the amplifier, must be implemented

as well [18]. This added complexity can either be realized using a fully integrated approach or through the use of hybrid packaged designs.

The maximum obtainable output power as well as large signal gain of the class E mode will not exceed that obtainable from the class AB mode; however, the PAE of the class E mode will greatly exceed that of the class AB mode [2]. Since device selection for use in a class E mode amplifier is typically based on performance specifications of the device biased in the class AB mode, it is up to the designer to select an appropriately sized device for the given application. However, if complex power supply modulation schemes such as envelop tracking are unnecessary for the application since a constant envelope modulation format is being used, another approach may be necessary in order to obtain maximum efficiency for multiple output power levels. The power scaling nature of the device is an important parameter that must be understood by the designer in order to obtain the maximum performance from a selected device process. The two techniques explored in this thesis involve scaling the output power of an amplifier by either combining smaller low power transistors to obtain the desired output power or to scale up the device periphery in order to achieve the same goal. However, in both cases, any input power level other than one used to obtain the rated output power for a given operating efficiency is going to result in less than optimal PAE since the amplifier is not operating in the designed class E conditions.

The general circuit block diagram of a power amplifier is shown below in Figure 2.1.

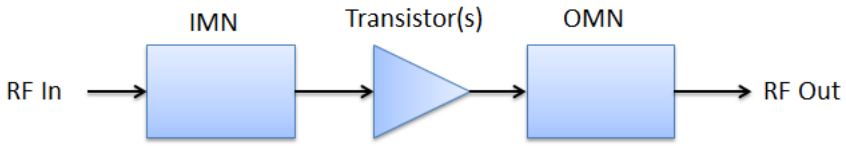

Figure 2.1: Generic PA block diagram

As shown in Figure 2.1 above, the most basic power amplifier consists of a transistor, an output matching network (OMN), an input matching network (IMN), and within those matching networks the biasing circuitry for the transistor. Traditionally, this is a fixed design for a specific range of frequencies and performance specifications. However, the integration of RF switches has allowed for the implementation of tunable designs that are capable of supporting wide bandwidths and operating conditions, all of which are necessary for the multiband nature of commercial and defense wireless networks.

In order to investigate the power scaling of gallium nitride in an integrated class E mode amplifier, a new architecture for a power scalable design is presented below in Figure 2.2.

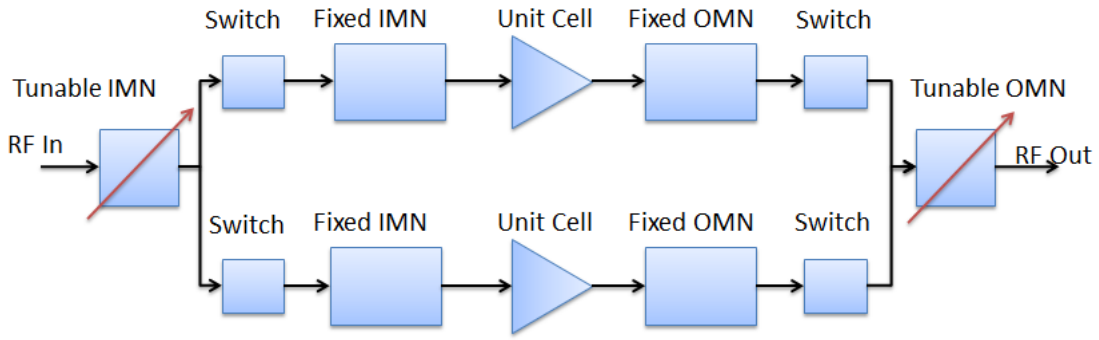

Figure 2.2: Scalable PA block diagram

As shown in Figure 2.2 above, the incorporation of high power gallium nitride switches at the input and output of identical parallel configured power amplifiers is proposed. In order to maintain the desired class E fundamental and harmonic loading of each transistor, the parallel amplifiers must have a minimal impact on each other when one device is either turned on or off. This is accomplished through the utilization of a reactive single pole double throw (SPDT) like combiner on the input and output of the combined amplifiers to provide isolation between each stage. An additional tunable matching network must also be incorporated at the combined port of the power

combiners in order to correct the impedance mismatch presented to the matching networks based on the state of the amplifier. It is expected that the output power of the amplifier will change by 3 dB (a factor of 2) based on how many transistor are active. This technique effectively changes the overall device periphery of the power amplifier in a controlled manner while maintaining the desired PAE for a given multiple of the output power. While the integrated design in this thesis only implements two parallel stages, it is possible to extend this architecture to as many stages as necessary and is only limited by the physical size restrictions placed on the integrated circuit as well as the ability to route separate paths for the drain and gate bias of each power transistor and the gate control for each switch. Ideally, integrated GaN based logic would accompany the power amplifier to control the state of the switches and the biasing of each power transistor.

A traditional technique used to combine parallel devices is also explored using commercially available bare die GaN transistors that can be wire bonded to a printed circuit board to form progressively larger single stage power amplifiers. Each single stage is then combined using a distributed Wilkinson power splitter/combiners at their respective inputs and outputs. This approach is common in industry; however, two smaller devices with an effective overall device periphery are compared to a single larger device of the same periphery and the challenges involved in designing the matching networks for the class E mode are investigated. The integrated and hybrid packaged power amplifiers are designed in the same manner through the utilization of the available nonlinear simulation models provided by the manufacturer. However, the integrated design is realized using on-chip microstrip spiral inductors and metal-insulator-metal capacitors whereas the hybrid packaged designs have their active devices wire bonded to a printed circuit board where surface mount capacitors and microstrip stub matching is employed to form the matching and biasing networks. Each approach offers insight into the challenges of class E mode power design and their limitations.

2.2 Load Pull Characterization

The technique used in this thesis to determine the optimal load and source reflection coefficients presented to the output and input of the device that are necessary to obtain the maximum PAE in the class E bias is called load pull characterization [2, 13]. While dynamic load line techniques will work well for some devices, the packaging and device parasitics play a very important role in determining what the load and source reflection coefficients should be since these parasitics are inherently part of the overall matching network. Most common RF and microwave computer aided design tools include a harmonic balance simulator that operates in the frequency domain to simulate the nonlinear behavior of an accurately modeled active device. If the transistor was a truly linear device, classical simulators such as SPICE would suffice. After selecting the desired operating point, input RF drive level, and fundamental frequency, the load pull is configured to sweep either the fundamental or harmonic load reflection coefficients over a selected region of the Smith chart until enough data is collected to generate constant contours of power, PAE, gain, etc. The load pull results are often used to determine what load or source reflection coefficient offers the best compromised between the desired operating specifications. As mentioned, this process can be performed both on the output and input of the transistor; however, not at the same time. It is common to first select an arbitrary input reflection coefficient and then perform the load pull on the output of the device. Once the first pass produces an optimum load impedance, the source is then conjugately matched to the input impedance presented by the device when it is loaded with the desired output reflection coefficients. The load pull is an iterative process and may require multiple fundamental and harmonic sweeps to produce a realizable matching network.

Load pull characterization is unlike the conjugate matching technique used for small signal designs, because an output conjugate match is not obtained from this procedure since the device is not operating under small-signal conditions. The load pull simulation must occur at each frequency

of interest or at least over a set of frequencies within the desired band of operation. Since this thesis is only concerned with a single frequency, only one set of load pull contours is obtained for each class E amplifier. Once the output and input reflection coefficients are obtained from the load and source pull data, matching networks are designed to present these reflection coefficients to the device. Since the matching networks consist of only passive linear elements, traditional S-parameter techniques are used to design and optimize each matching circuit until the reflection coefficients of interest adequately represent the results obtained from the load pull characterization of the device. Almost every microwave measurement setup in use today is terminated using a 50 Ohm system, so the output and input matching networks are designed using 50 Ohm terminations; however, this may not be appropriate if a non-50 Ohm driver or pre-driver amplifier stage precedes the input of the final amplifier. In reality, a broadband 50 Ohm load is not practical and often unobtainable due to the unpredictable nature of the operating environment, i.e., any power amplifier connected to an antenna.

2.3 Small-Signal Considerations

The S-parameters of the amplifier are important for calculating small-signal stability; therefore, the device needs to operate in a region where it is conducting. The typical solution is to bias the device in the class AB mode of operation and reduce the input RF drive level so that it does not exceed 0 dBm (1mW) in order for the linear, small-signal amplifier approximations to produce meaningful results. For the devices presented in this thesis, the necessary drain current density for the class AB mode ranges from approximately 50mA/mm to 100mA/mm based on the device periphery. Obviously, the stability of the transistor is dependent on the frequency of operation and most importantly the device's bias conditions, which will change with input drive level, temperature, supply voltages, etc., so it is necessary to ensure stability of the device for all possible operating conditions. While the load geometric stability factor is used to evaluate whether or not the device is unconditionally

stable at the fundamental, second, and third harmonics in this thesis, other techniques such as the Nyquist stability criterion are recommended to fully evaluate the stability of the amplifier [19].

2.4 Device Selection

For the hybrid packaged approach, three different size transistors are selected for evaluation and used in the design of single stage power amplifiers. The device peripheries of the commercially available bare die GaN transistors are 1.25mm, 2.5mm, and 5mm, respectively. Each larger transistor is double the size of the periphery of the preceding smaller device, allowing for the design of parallel stage power amplifiers of the same overall device periphery, e.g., two 1.25mm transistors are combined using Wilkinson power combiners and evaluated against a single 2.5mm device power stage. A total of six hybrid packaged amplifier circuits are designed and simulated, i.e., three single stage amplifiers using each different size transistor, two circuits using the 1.25mm device to create an overall periphery of 2.5mm and 5mm, and one circuit using two 2.5mm devices to create an overall periphery of 5mm. The three designated output power levels of each design are 5W, 10W, and 20W, respectively.

The reconfigurable MMIC amplifier utilizes two 0.6mm power transistors which are structurally similar to the devices utilized in the hybrid packaged designs. Since the designer has control over the dimensions of the transistor utilized in an integrated design, the 0.6mm device is selected so that it can be compared with the larger bare die 1.25mm device in the same manner as with the hybrid designs. The integrated amplifier is designed so that a single device produces an output power of approximately 2.5W and 5W when both devices are active.

CHAPTER III

HYBRID PACKAGING DESIGN APPROACH

3.1 Transistor IV Curves

The simulation setup for measuring the IV characteristics of the 1.25mm GaN bare die transistor is shown below in Figure 3.1.

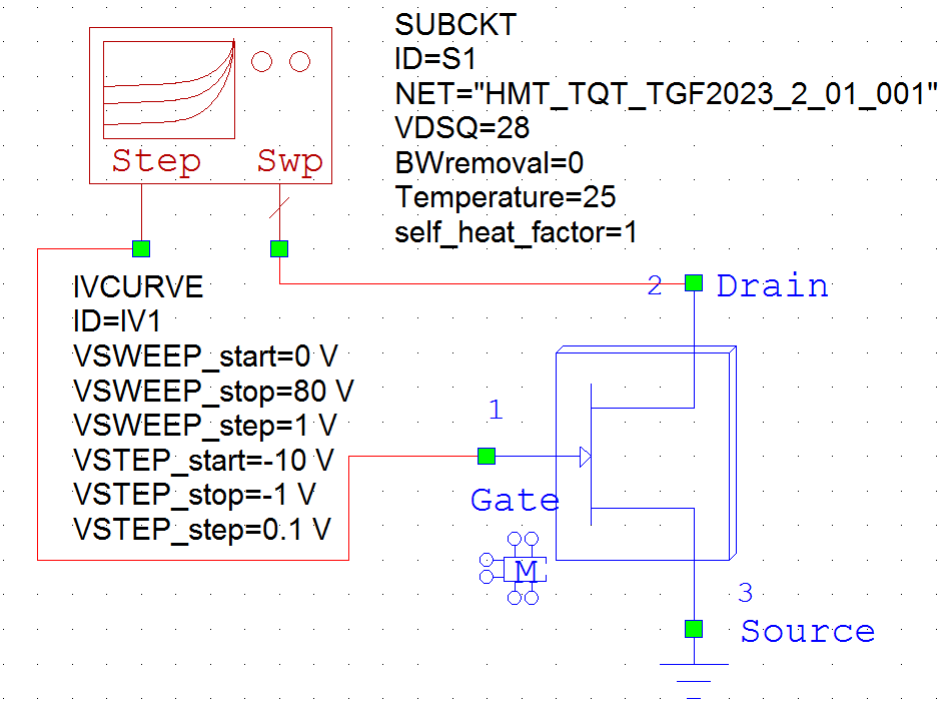

Figure 3.1: Bare die (1.25mm) DC sweep schematic [1]

As shown above in Figure 3.1, the drain to source voltage (Vds) is swept from 0V to 80V while the gate to source voltage (Vgs) is stepped from -10V to -1V in tenth of a voltage increments. The selected GaN process produces FETs that are depletion mode devices, which means the device is normally on with a Vgs of 0V. In order to fully turn the device off, a negative Vgs of -5 or more must be applied.

The IV characteristics of the 1.25mm bare die transistor are shown below in Figure 3.2.

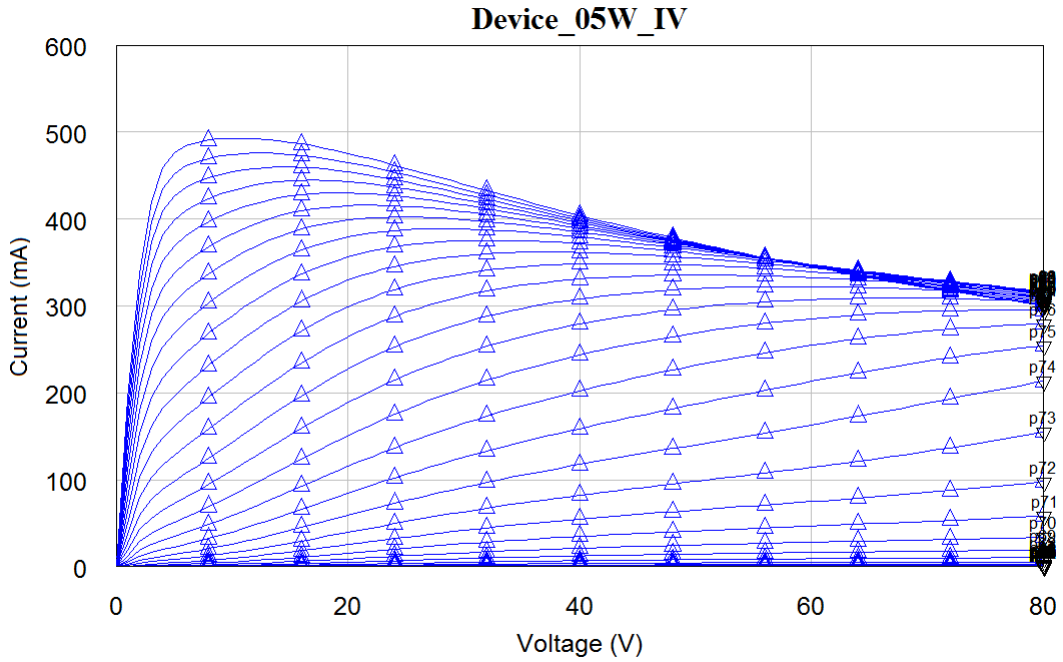

Figure 3.2: Bare die (1.25mm) IV curves [1]

As shown above in Figure 3.2, the saturation current of the device is greater than 500mA. Since the class E mode of operation is desired, Vgs is set to around the pinch-off voltage of approximately -4V and Vds is set to 30V in order for the nonlinear simulation model to accurately perform under

large signal conditions. Since GaN technology has a high breakdown voltage, it is not uncommon for GaN FET amplifiers to have drain supply voltages in excess of 50V.

A similar configuration is used for the 2.5mm bare die transistor and the IV measurement schematic is shown below in Figure 3.3.

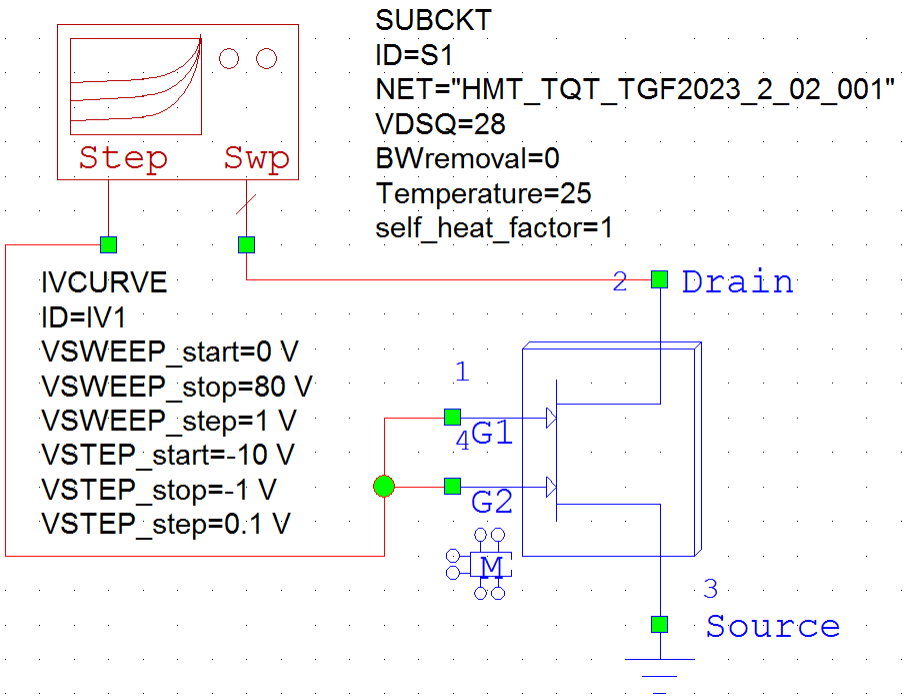

Figure 3.3: Bare die (2.5mm) DC sweep schematic [1]

As shown in Figure 3.3 above, the transistor is characterized over the same range of terminal voltages in order to compare transistors fabricated using the same foundry process.

The IV characteristics of the 2.5mm bare die transistor are shown below in Figure 3.4.

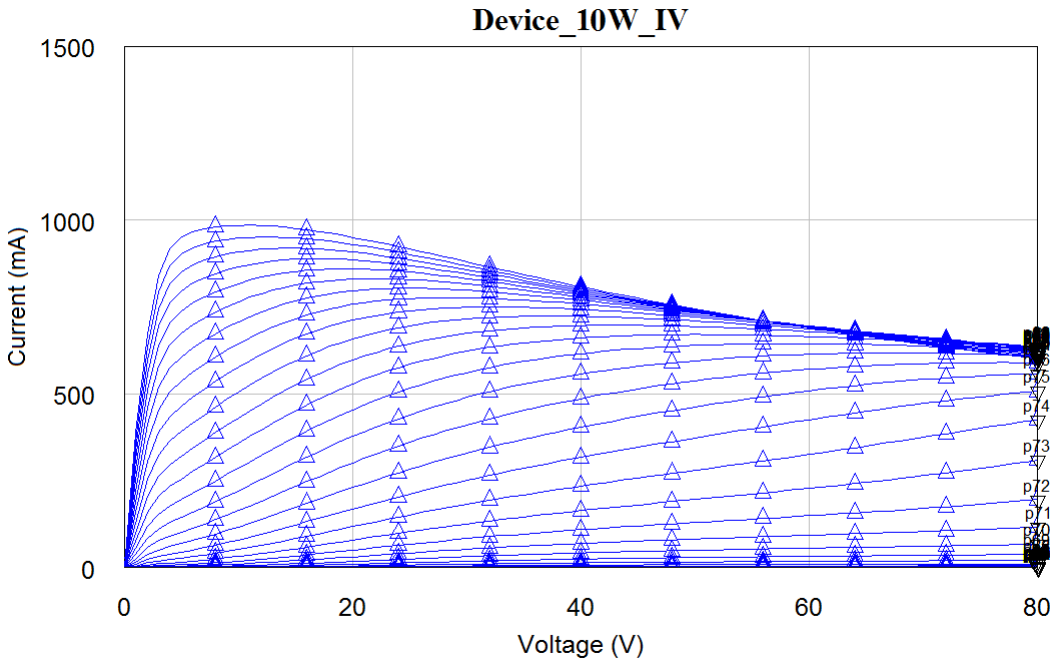

Figure 3.4: Bare die (2.5mm) IV curves [1]

As shown above in Figure 3.4, the saturation current of the device is greater than 1A. Again, since the class E mode of operation is desired, Vgs is set to around the pinch-off voltage of approximately -4V and Vds is set to 30V.

Finally, the same configuration is used for the 5mm bare die transistor and the IV measurement schematic is shown below in Figure 3.5.

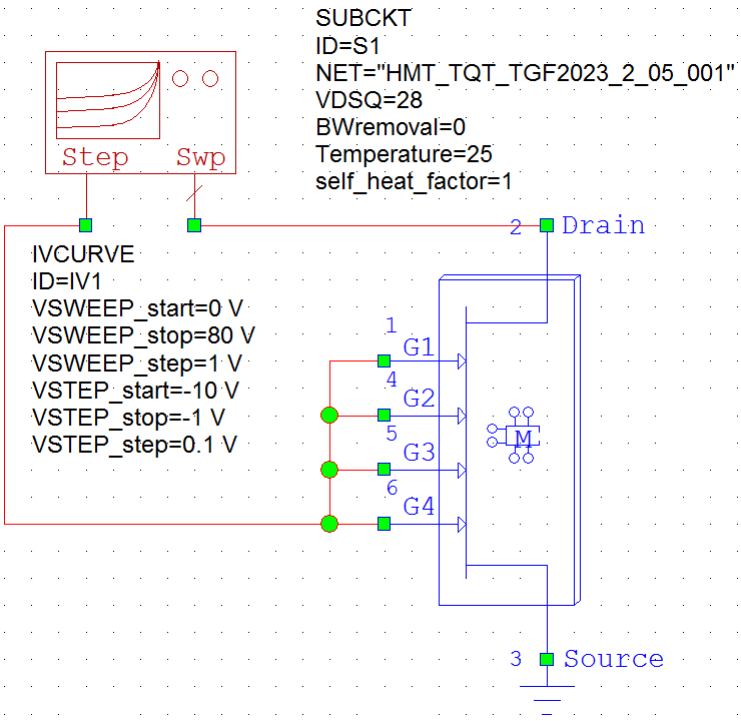

Figure 3.5: Bare die (5mm) DC sweep schematic [1]

As shown in Figure 3.5 above, the transistor is characterized over the same range of terminal voltages in order to compare transistors fabricated using the same foundry process.

The IV characteristics of the 5mm bare die transistor are shown below in Figure 3.6.

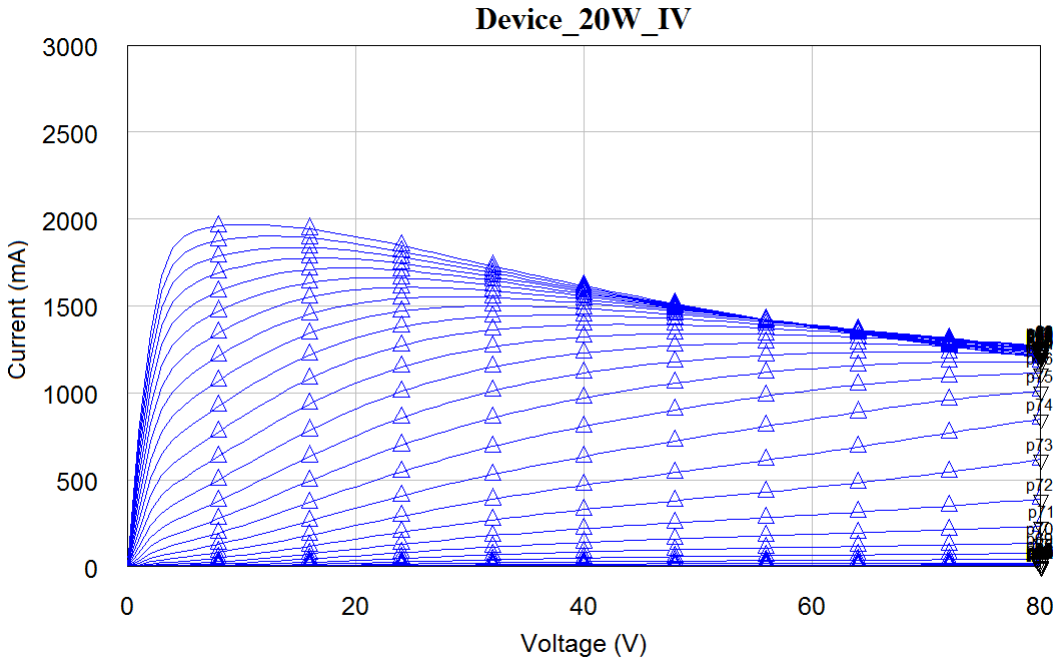

Figure 3.6: Bare die (5mm) IV curves [1]

As shown above in Figure 3.6, the saturation current of the device is greater than 2A. It is clear that as the device periphery is scaled by a factor of two, the saturation current is also scaled by a factor of two. Again, since the class E mode of operation is desired, Vgs is set to around the pinch-off voltage of approximately -4V and Vds is set to 30V. From these results, it is expected that the maximum obtainable output power of each device will scale with the periphery of the device.

3.2 Transistor Stability

For the 1.25mm device biased in the class AB mode condition described in Section 2.3, the schematic used to evaluate the geometric stability factor (Mu1) is shown below in Figure 3.7.

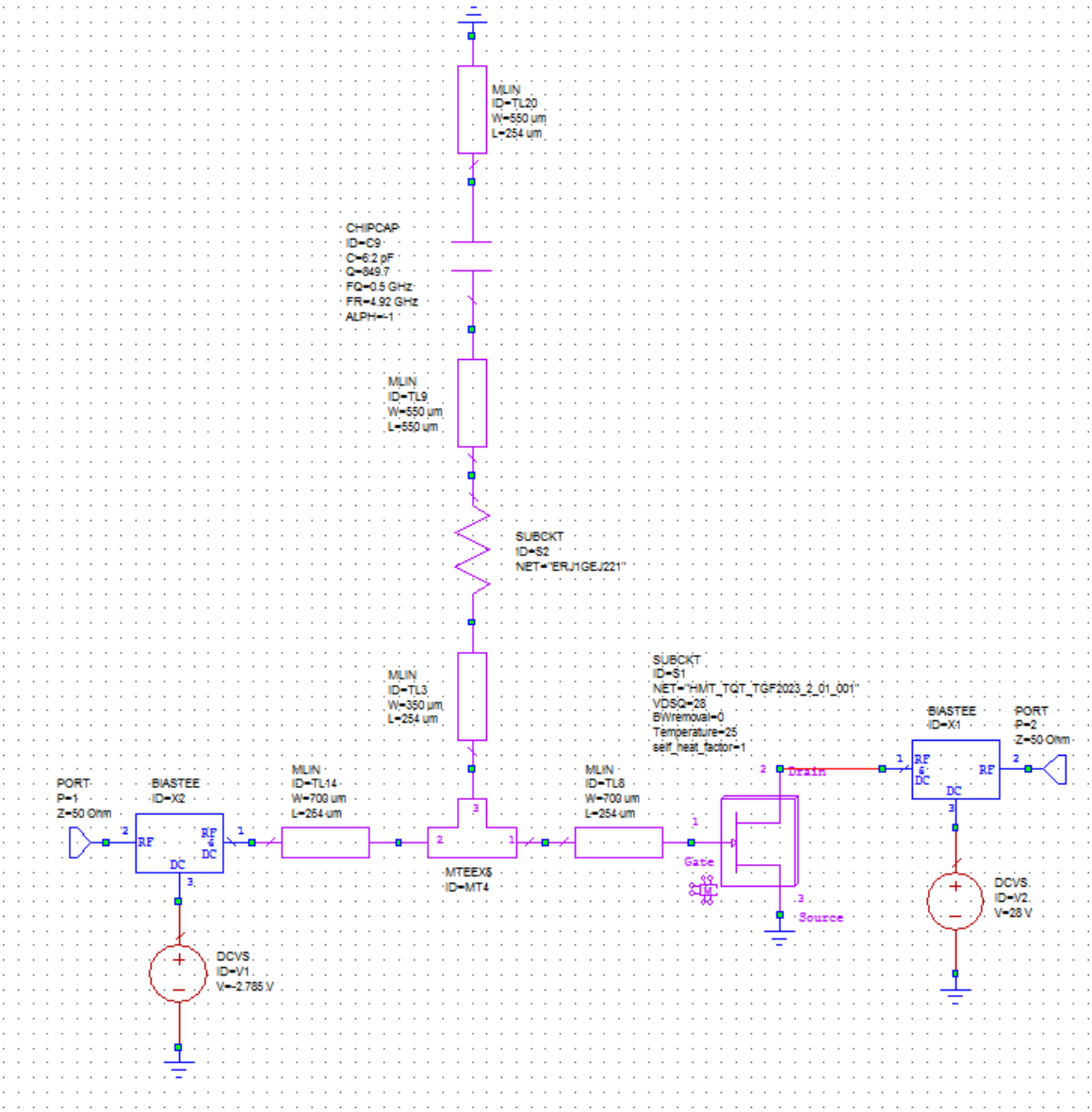

Figure 3.7: Bare die (1.25mm) stability schematic [1]

As shown above in Figure 3.7, a shunt-series combination of a resistor and capacitor are connected close to the gate of the transistor.

For the 1.25mm device biased in the described class AB mode condition, the geometric stability factor (Mu1) is shown below in Figure 3.8.

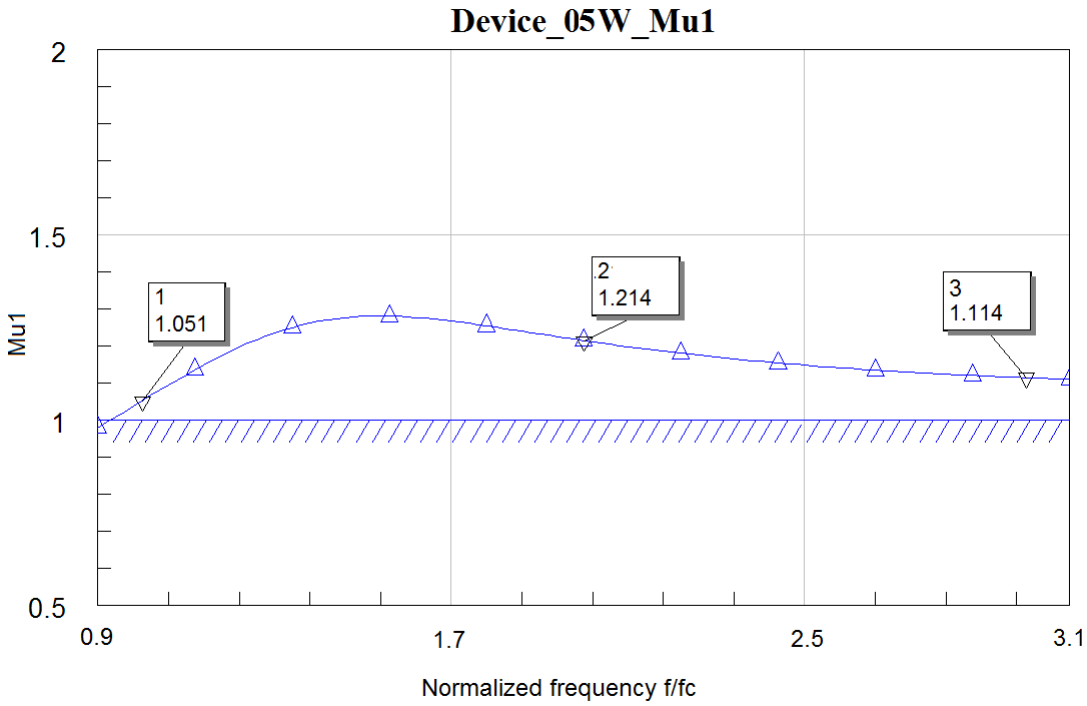

Figure 3.8: Bare die (1.25mm) geometric stability evaluation [1]

As shown above in Figure 3.8, the device is unconditionally stable at the design frequency as well as the second and third harmonics.

A similar stability network is used for the 2.5mm bare die transistor and is shown below in Figure 3.9.

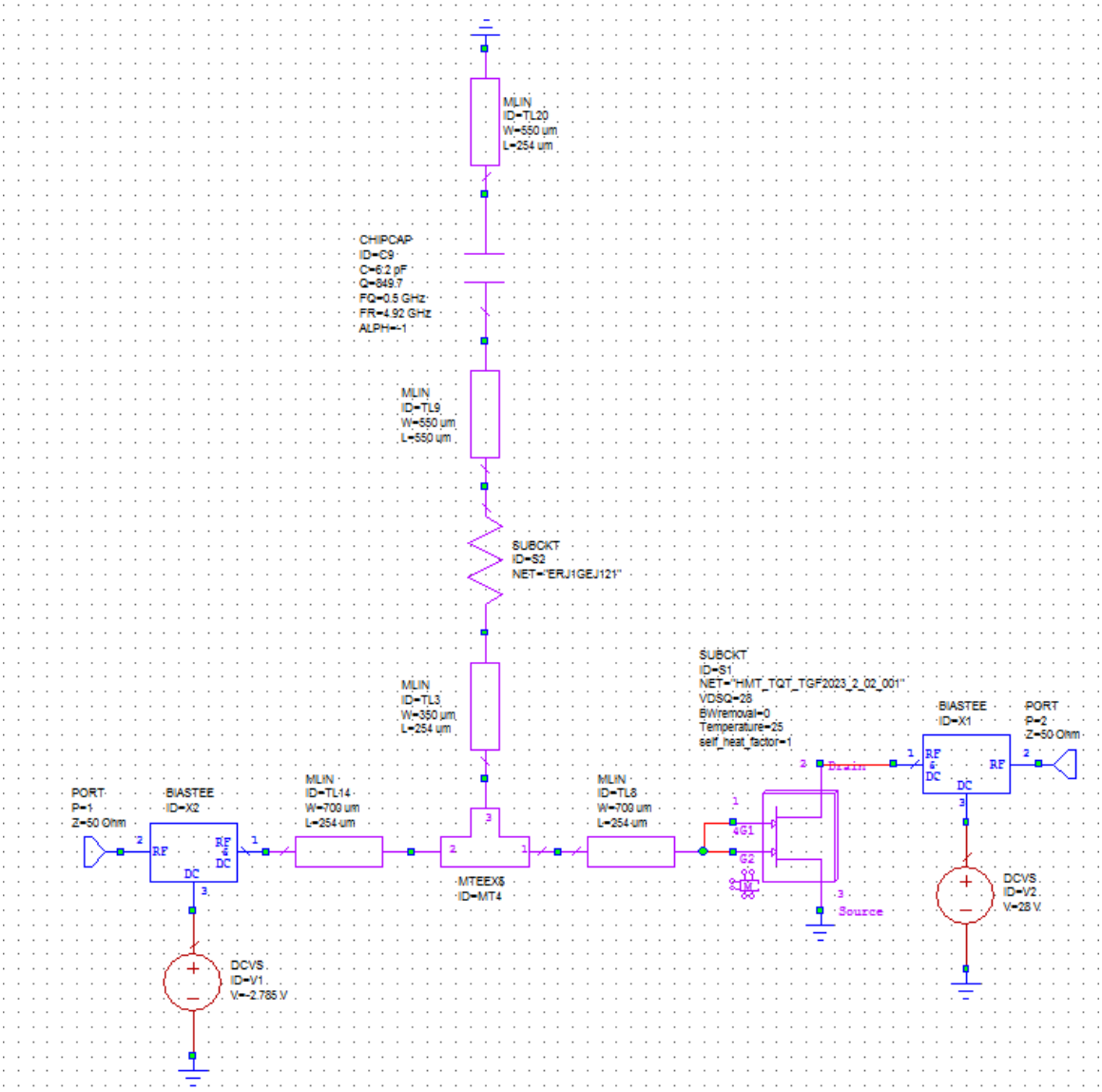

Figure 3.9: Bare die (2.5mm) stability schematic [1]

As shown above in Figure 3.9, a shunt-series combination of a resistor and capacitor are connected close to the gate of the transistor.

For the 2.5mm device biased in the described class AB mode condition, the geometric stability factor (Mu1) is shown below in Figure 3.10.

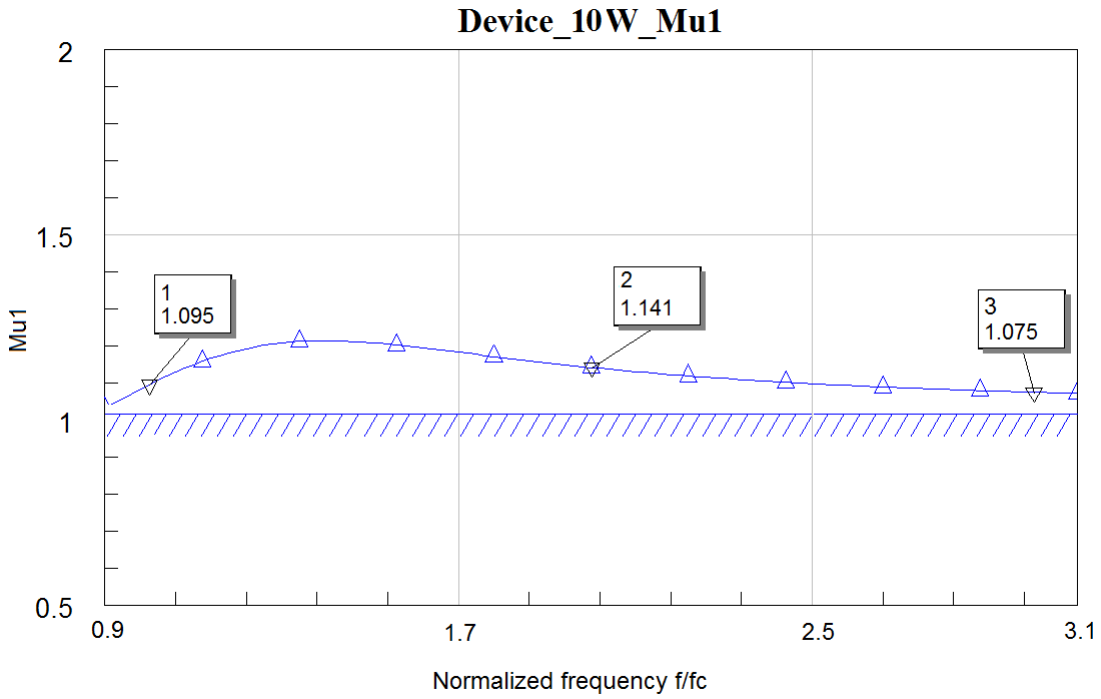

Figure 3.10: Bare die (2.5mm) geometric stability evaluation [1]

As shown above in Figure 3.10, the device is unconditionally stable at the design frequency as well as the second and third harmonics.

Finally, the same configuration of the stability network is used for the 5mm bare die transistor and is shown below in Figure 3.11.

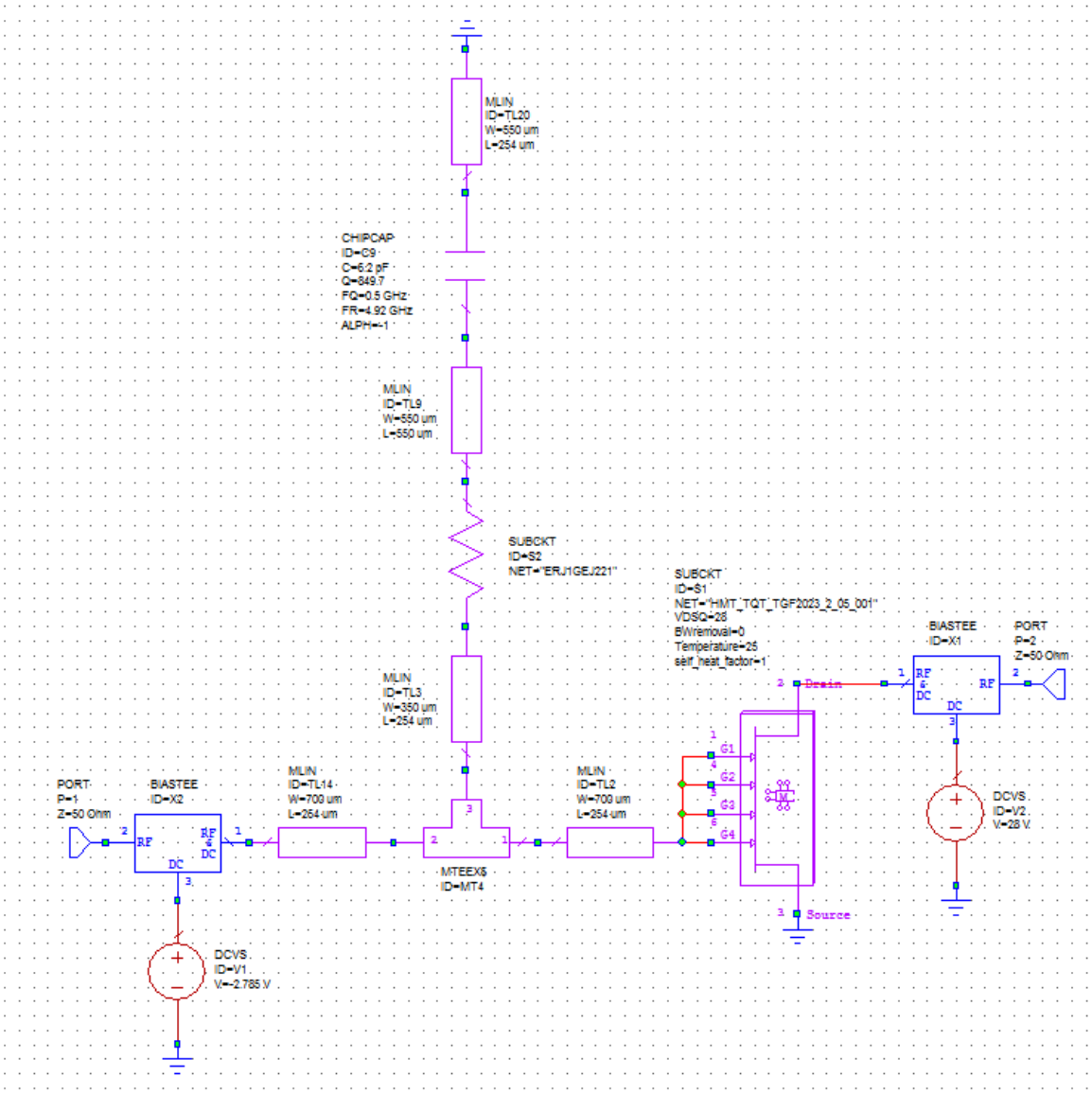

Figure 3.11: Bare die (5mm) stability schematic [1]

As shown above in Figure 3.11, a shunt-series combination of a resistor and capacitor are connected close to the gate of the transistor.

For the 5mm device biased in the described class AB mode condition, the geometric stability factor (Mu1) is shown below in Figure 3.12.

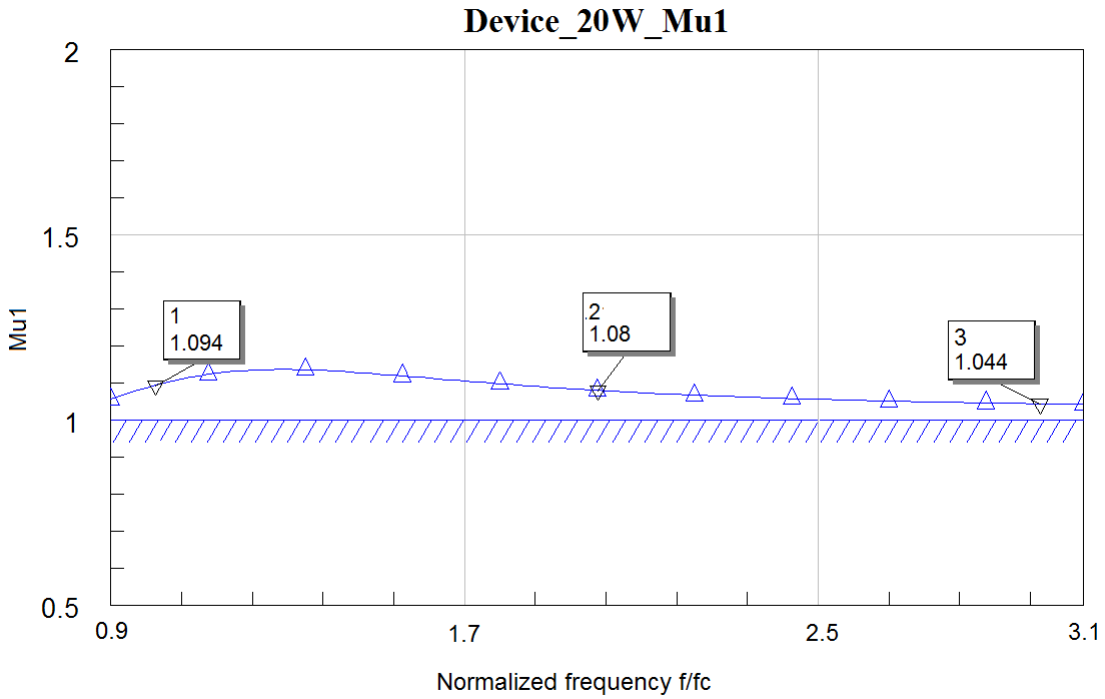

Figure 3.12: Bare die (5mm) geometric stability evaluation [1]

As shown above in Figure 3.12, the device is unconditionally stable at the design frequency as well as the second and third harmonics.

The transistors used in this thesis have a significant amount of gain at lower frequencies and therefore low frequency stability is of concern once the circuits are fabricated. The stabilizing network used in the hybrid designs becomes part of the input matching network and is as close to the gate of the transistor as possible. Other techniques are available to stabilize the transistor; however, since the output power of these amplifiers is significantly higher than the input power, techniques such as shunt resistors on the output or resistive feedback are undesired due to their dissipative effect on the power added efficiency of the amplifier. The common technique used in

high power amplifier design is to incorporate a lossy input matching network while minimizing losses on the output [19].

3.3 Transistor Load Pulls

The load pull contours of the 1.25mm device, including the effects of the bond wires, are shown below in Figure 3.13.

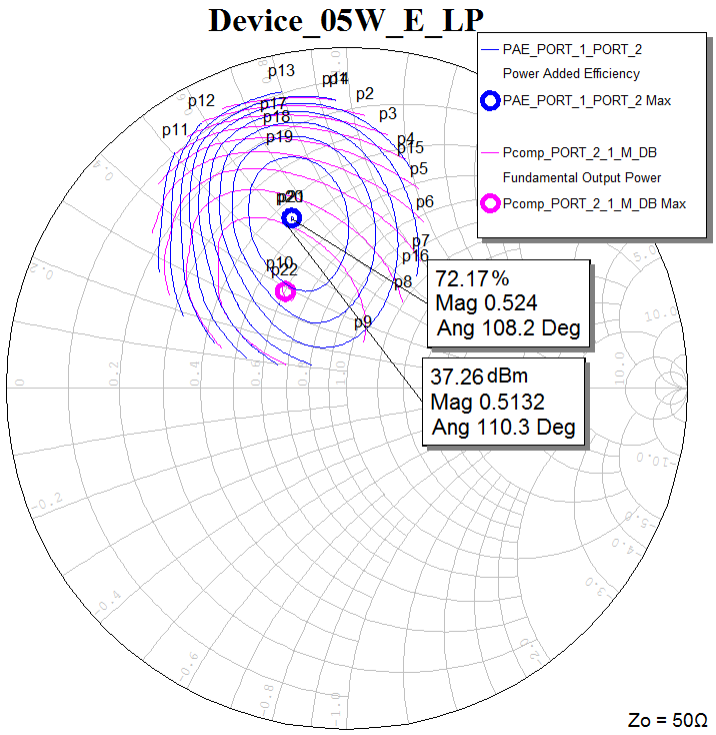

Figure 3.13: Bare die (1.25mm) class E load pull [1]

As shown above in Figure 3.13, the peak power added efficiency is approximately 72.2% with an output power of 37.3dBm (approx. 5W). Since a highly efficiency PA is desired, the fundamental load impedance is selected based on this maximum obtainable power added efficiency. The identified reflection coefficients on the load pull contours are then used to design the fundamental and

harmonic matching networks. It should be noted that the load pull tuners in the simulation environment assume lossless matching networks and therefore represent the best possible results. It is clear that any realizable lossy circuit element will detract from the circuit's overall performance.

The load pull contours of the 2.5mm device, including the effects of the bond wires, are shown below in Figure 3.14.

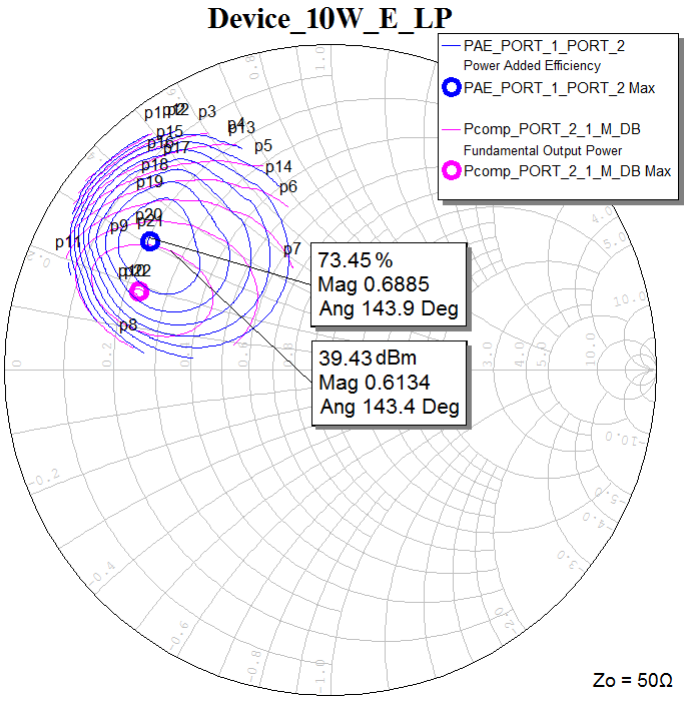

Figure 3.14: Bare die (2.5mm) class E load pull [1]

As shown above in Figure 3.14, the maximum obtainable power efficiency is approximately 73.5% with an output power of 39.4dBm (approx. 10W).

The load pull contours of the 5mm device, including the effects of the bond wires, are shown below in Figure 3.15.

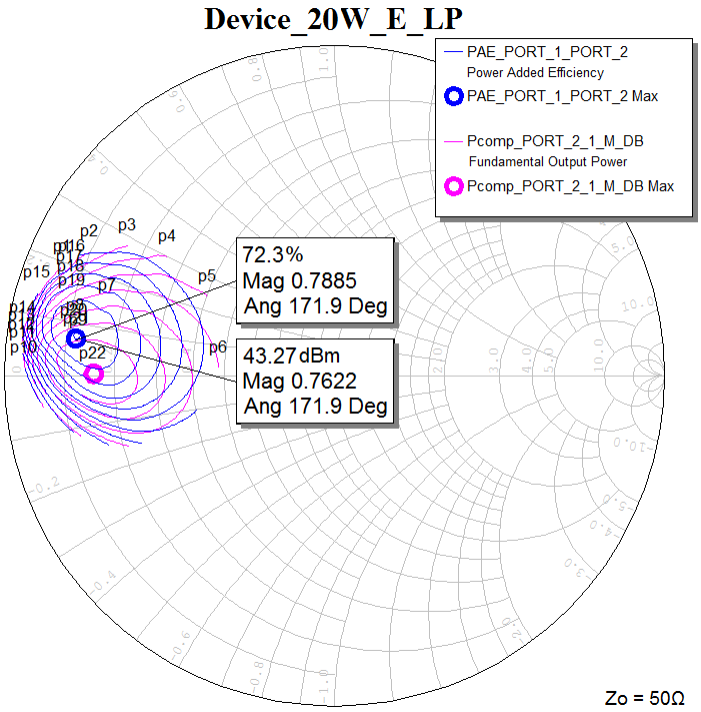

Figure 3.15: Bare die (5mm) class E load pull [1]

As shown above in Figure 3.15, the maximum obtainable power efficiency is approximately 72.3% with an output power of 43.3dBm (approx. 20W).

3.4 Microwave Substrate Laminate

The TMM4 substrate selected for the hybrid packaged designs is available from Rogers Corporation. The substrate definition used in the design of the matching networks and simulations is shown below in Figure 3.16.

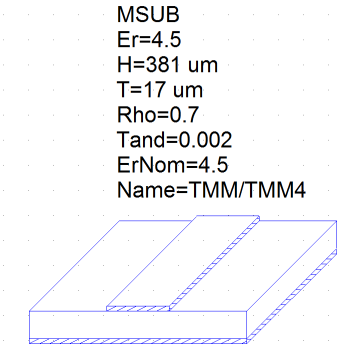

Figure 3.16: Rogers Corporation TMM4 substrate definition

As shown in Figure 3.16, the selected substrate has a reasonably low dielectric constant and loss tangent, allowing for the design of low loss distributed matching networks within a relatively small area.

3.5 Wilkinson Power Splitter/Combiner

In order to combine multiple power amplifier stages in parallel to form a higher output power, a low-loss power combining/splitter network must be implemented both on the input and output of the amplifying stages. A number of widely available circuits have been successfully implemented for such a purpose with varying degrees of complexity; however, one of the most popular and easy to implement designs is known as the Wilkinson power splitter/combiner [13]. Unlike the traditional reactive combiner approach, which is to simply split the input or output feeds into separate transmission paths, the Wilkinson presents the desired impedance to each of its ports while providing path isolation between the split ports. The major benefit of this in-phase design is an inherent fail-over protection mechanism should one amplifier shutdown or become inoperable [13]. Unlike the two-way reactive combiner, isolation on the order of 20dB or more is possible with the Wilkinson compared to the 3dB of isolation inherent in a reactive combiner/splitter. The Wilkinson

accomplishes this through the addition of a balancing resistor placed across the single-ended output ports. This resistor will dissipate power lost due to an amplitude or phase imbalance between each port. For a 50 Ohm Wilkinson, each split or combined path is formed using a quarter wavelength of transmission line (microstrip) at the design frequency with a characteristic impedance of 70.7 Ohms, which is the geometric mean between 50 and 100 Ohms.

The schematic of the designed Wilkinson is shown below in Figure 3.17.

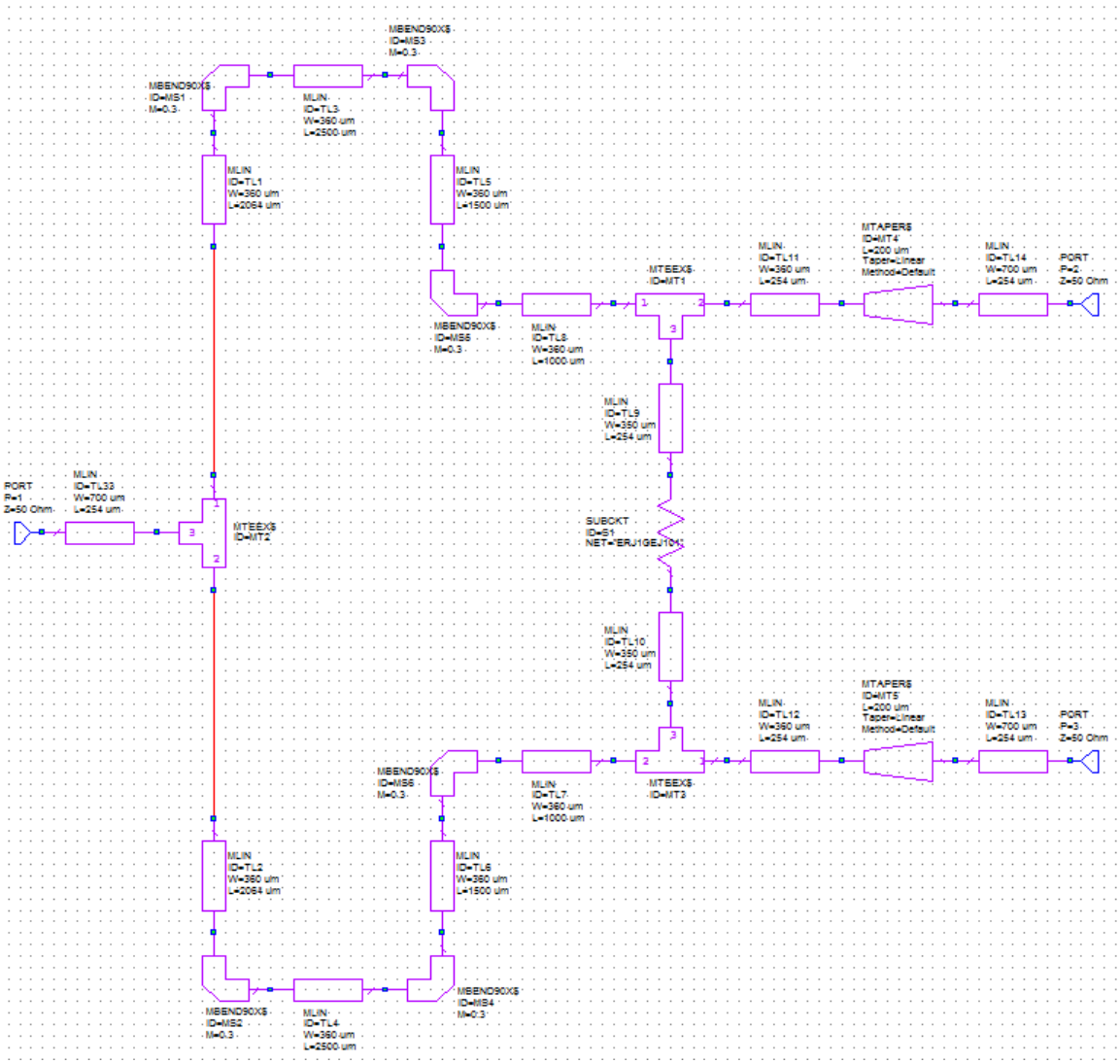

Figure 3.17: Distributed Wilkinson schematic

The Wilkinson shown in Figure 3.17 above is presented in such a way that it closely represents the final layout of the circuit, which is shown below in Figure 3.18.

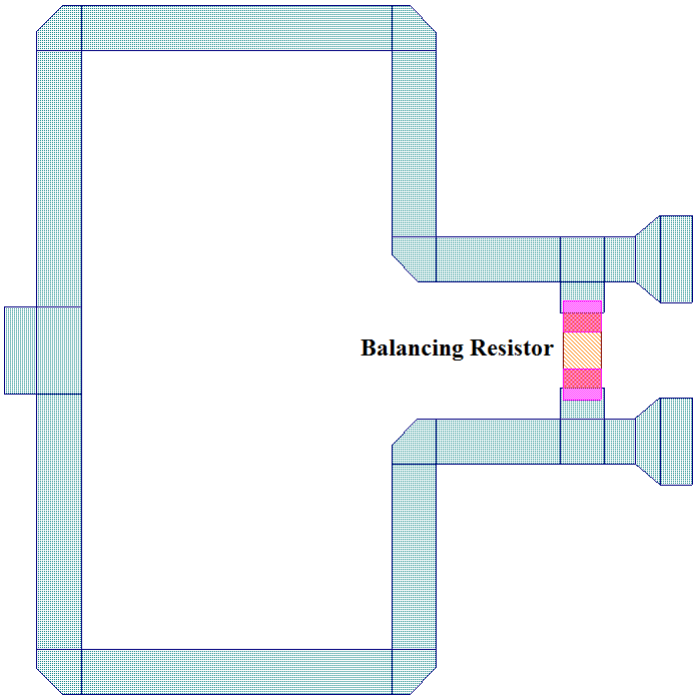

Figure 3.18: Distributed Wilkinson layout

As shown in Figure 3.18 above, the overall footprint of the Wilkinson is reduced by meandering the quarter-wave transformers that form each RF path. All of the combined PA circuits presented in the hybrid packaging approach utilize this Wilkinson on the input and output of the 50 Ohm matching networks.

3.6 Gate and Drain Bias Networks

In order to apply the correct bias for both the drain and gate of each transistor, a shunt short circuited quarter-wave stub is designed and implemented. The shunt short circuited quarter-wave

stub presents a low admittance at the design frequency as well as to the odd harmonics and a high admittance to the even harmonics. Since the class E mode requires open harmonic terminations for high efficiency operation, the bias networks are placed near the 50 Ohm point of the fundamental input and output matching networks.

The gate and drain bias network is shown below in Figure 3.19.

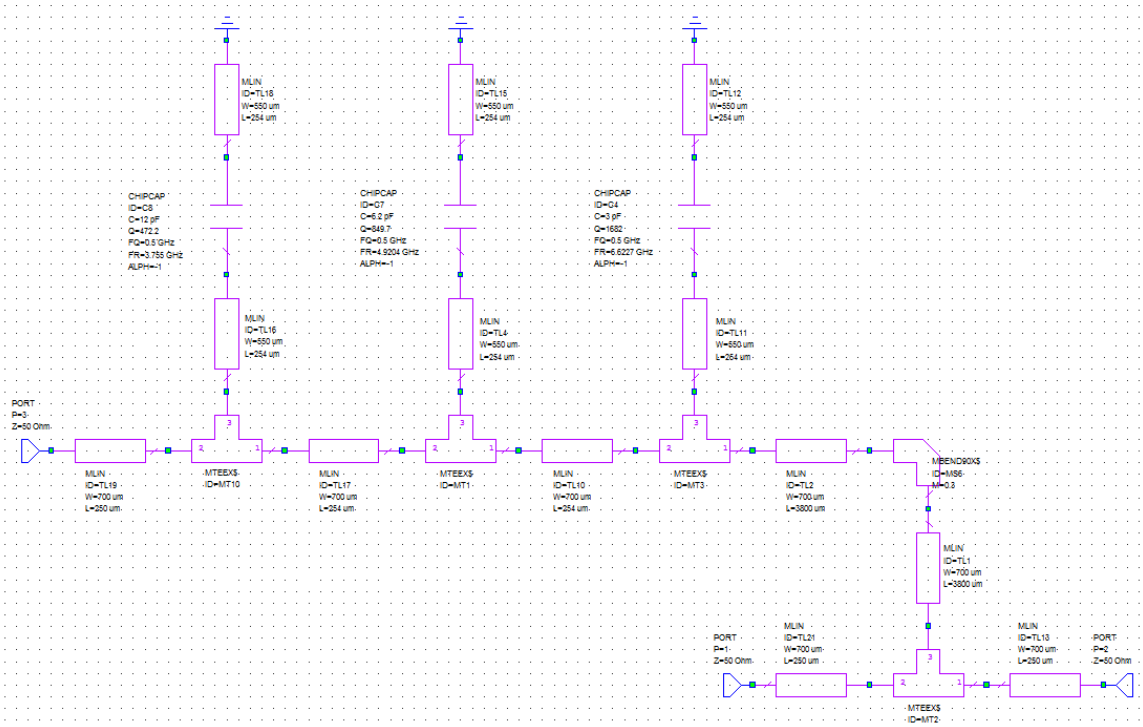

Figure 3.19: Gate and drain bias network schematic

As shown in Figure 3.19 above, bypass capacitors are utilized near the dc feed point in order to filter out any additional high frequency content that may be present.

The layout of the bias network shown in Figure 3.19 is shown below in Figure 3.20.

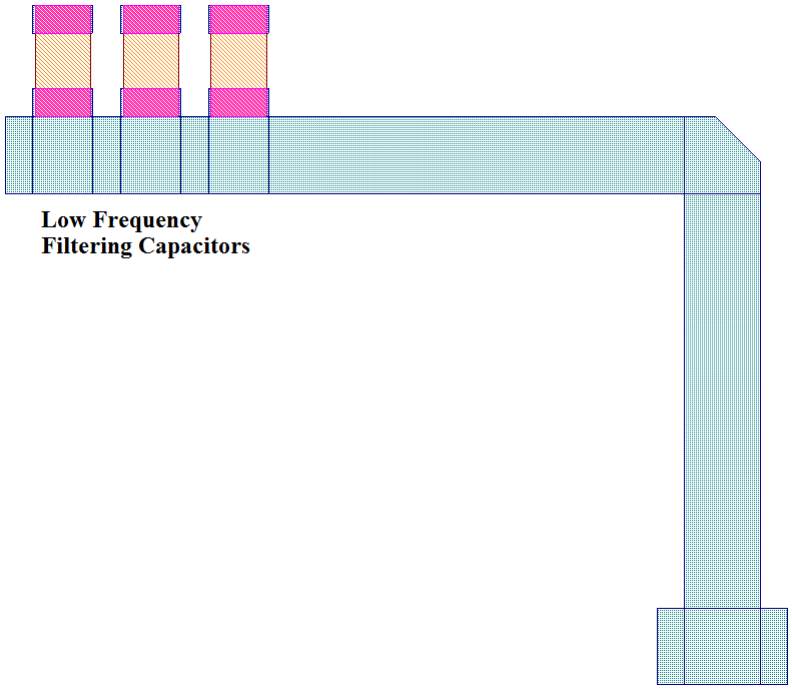

Figure 3.20: Gate and drain bias network layout

As shown in Figure 3.20 above, the foot print of the bias network is minimized by introducing a bend in the quarter-wave transformer.

3.7 Single Transistor Input and Output Matching

Since the matching networks consists of distributed linear elements, it is possible to use an S-parameter matching technique to tune the network so that it presents the desired reflection coefficients (S11) to the output of the transistor. This is done by using variables in the simulation environment to tune the length of the matching stubs until an acceptable match at the fundamental and harmonics is obtained. Each matching network consists of a stub resonant at the second and third harmonic with the highest order being the closest to the terminals of the device and a series-shunt low pass microstrip transmission line configuration for matching the fundamental. It is

apparent that the harmonic matching will impact the behavior of the fundamental match, so observing the response of the overall matching network at the fundamental and harmonics is the easiest approach to satisfy the results of the load pull for each device shown in Section 3.3.

The reflection coefficients of the designed output matching network for the 1.25mm device is shown below in Figure 3.21.

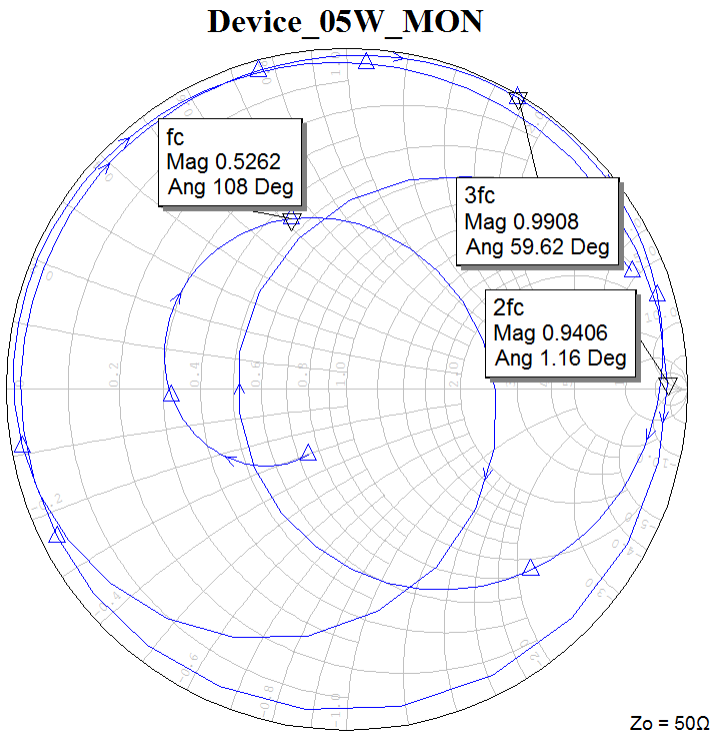

Figure 3.21: Output matching network for 5W amplifier using 1.25mm device

As shown in Figure 3.21, the performance of the output matching network for the 1.25mm device resembles the desired performance based on the results of the load pull shown in Figure 3.13. However, the matching network uses realizable components and losses will affect the performance of the amplifier.

The reflection coefficient of the designed input matching network for the 1.25mm device is shown below in Figure 3.22.

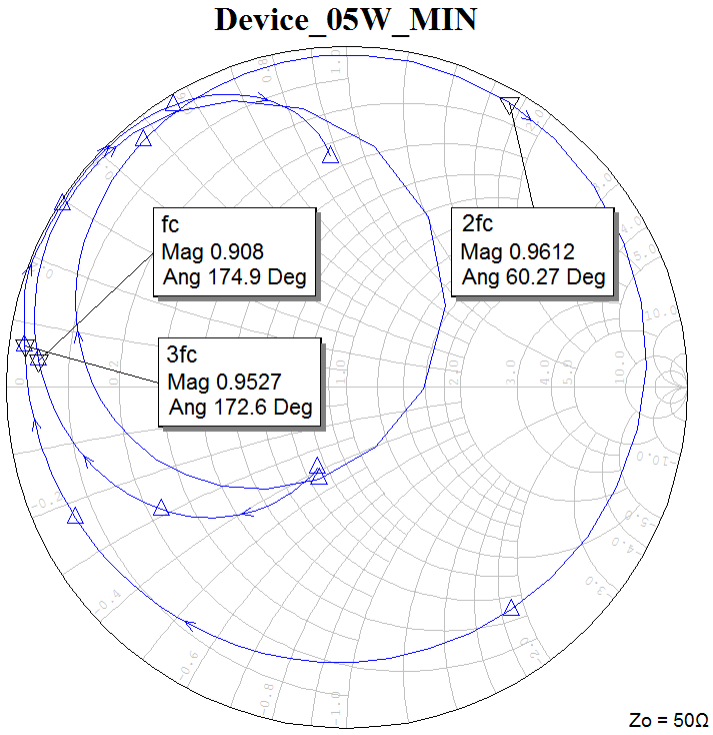

Figure 3.22: Input matching network for 5W amplifier using 1.25mm device

As shown in Figure 3.22 above, the input matching network of the device is designed in a similar manner used to develop the correct response of the output matching network; however, the input is conjugately matched based on the desired fundamental and harmonic loading presented to the output of transistor. Harmonic tuning stubs are also introduced on the input to further improve the efficiency of the power amplifier.

The reflection coefficients of the designed output matching network for the 2.5mm device is shown below in Figure 3.23.

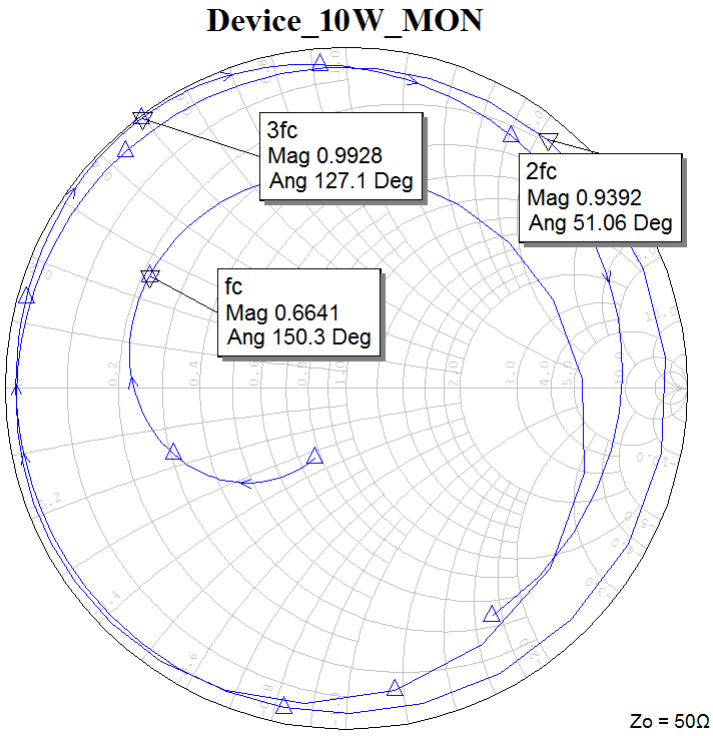

Figure 3.23: Output matching network for 10W amplifier using 2.5mm device

As shown in Figure 3.23, the performance of the output matching network for the 2.5mm device resembles the desired performance based on the results of the load pull shown in Figure 3.14.

The reflection coefficient of the designed input matching network for the 2.5mm device is shown below in Figure 3.24.

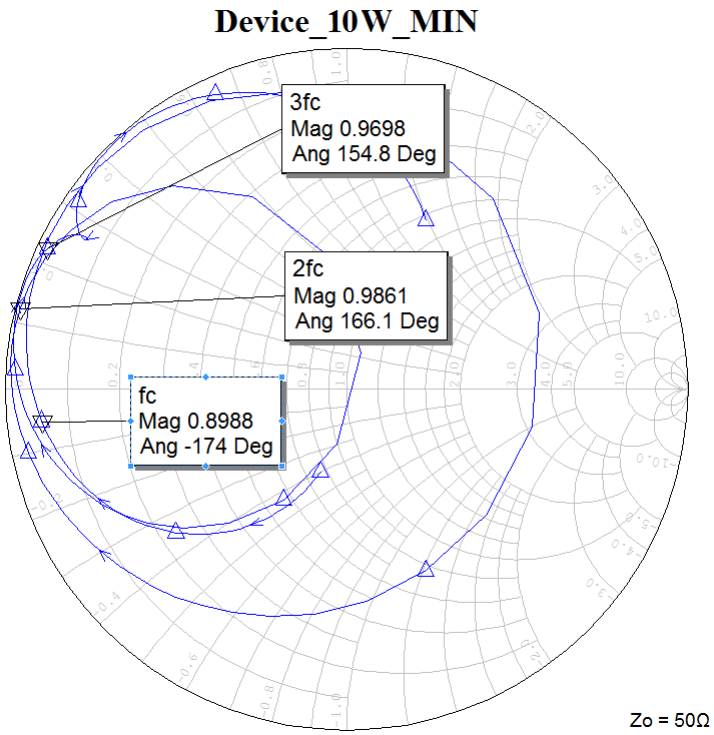

Figure 3.24: Input matching network for 10W amplifier using 2.5mm device

As shown in Figure 3.24 above, the input matching network of the device is designed in a similar manner used to develop the correct response of the output matching network.

The reflection coefficients of the designed output matching network for the 5mm device is shown below in Figure 3.25.

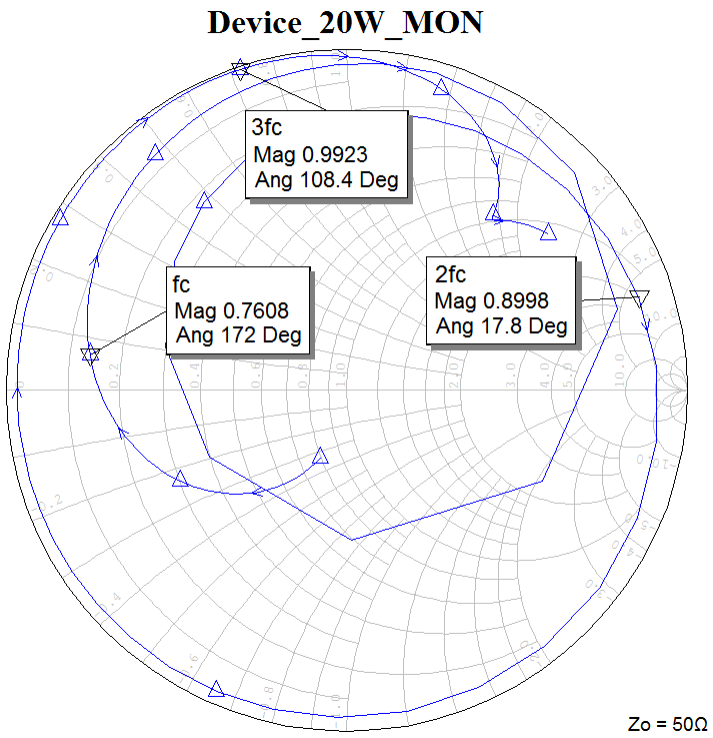

Figure 3.25: Output matching network for 20W amplifier using 5mm device

As shown in Figure 3.25, the performance of the output matching network for the 5mm device resembles the desired performance based on the results of the load pull shown in Figure 3.15.

The reflection coefficient of the designed input matching network for the 5mm device is shown below in Figure 3.26.

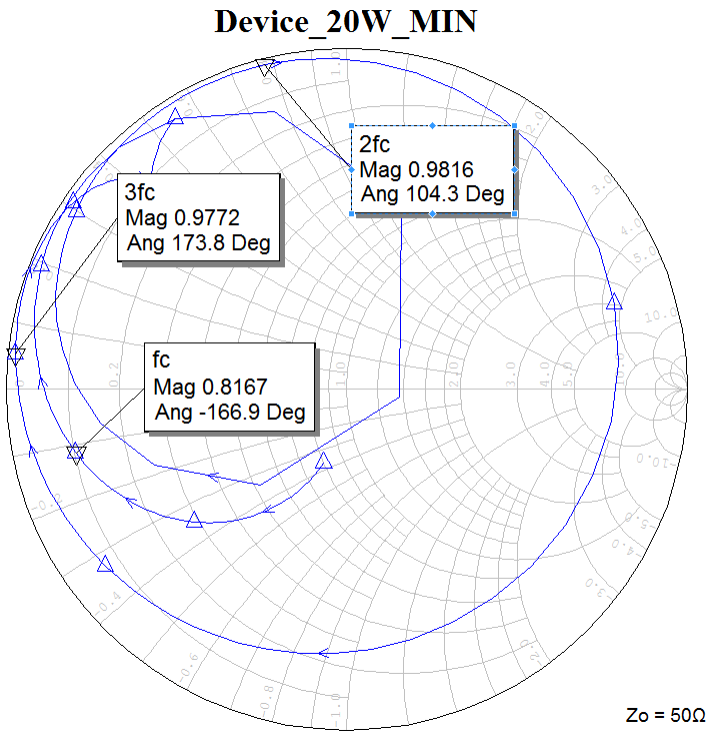

Figure 3.26: Input matching network for 20W amplifier using 5mm device

As shown in Figure 3.26 above, the input matching network of the device is designed in a similar manner used to develop the correct response of the output matching network. In each case, the output and input matching networks must be optimized in order to compensate for any losses or non-ideal behavior introduced by utilizing real components.

3.8 Single Transistor Power Amplifiers

Once each single device input and output matching network is designed and optimized, the individual subcircuits can be connected and laid out to form the overall power amplifier.

The single transistor 5W power amplifier schematic is shown below in Figure 3.27.

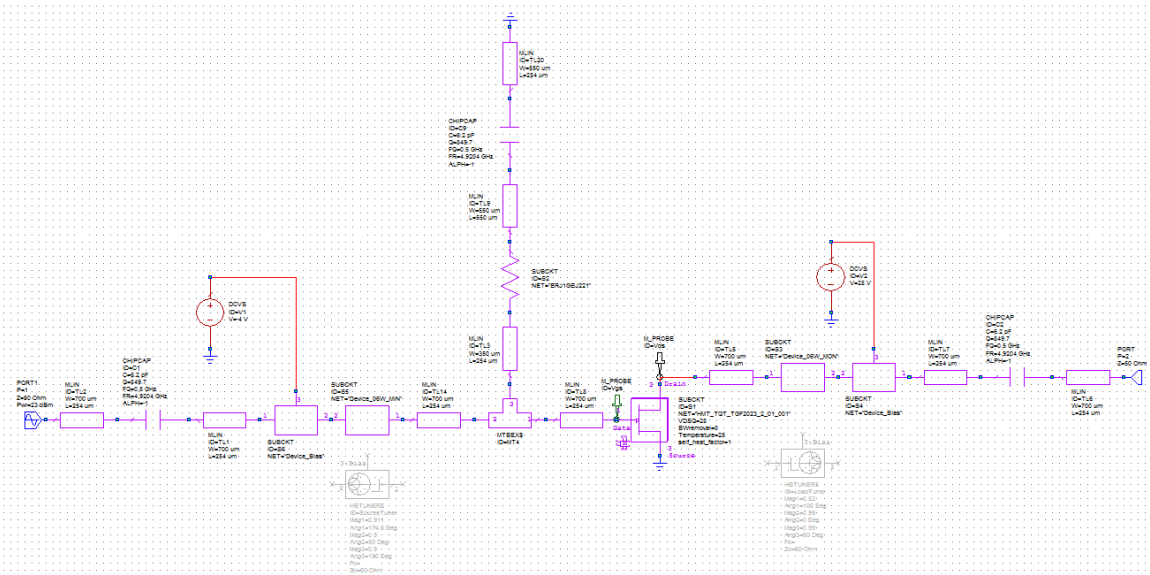

Figure 3.27: Single transistor (1.25mm) 5W power amplifier circuit schematic [1]

As shown in Figure 3.27 above, each subcircuit is contained within its own subblock and therefore simplifies the overall circuit schematic and allows for ease of optimization and layout.

The layout of the 5W single device amplifier schematic shown in Figure 3.27 above is shown in Figure 3.28 below.

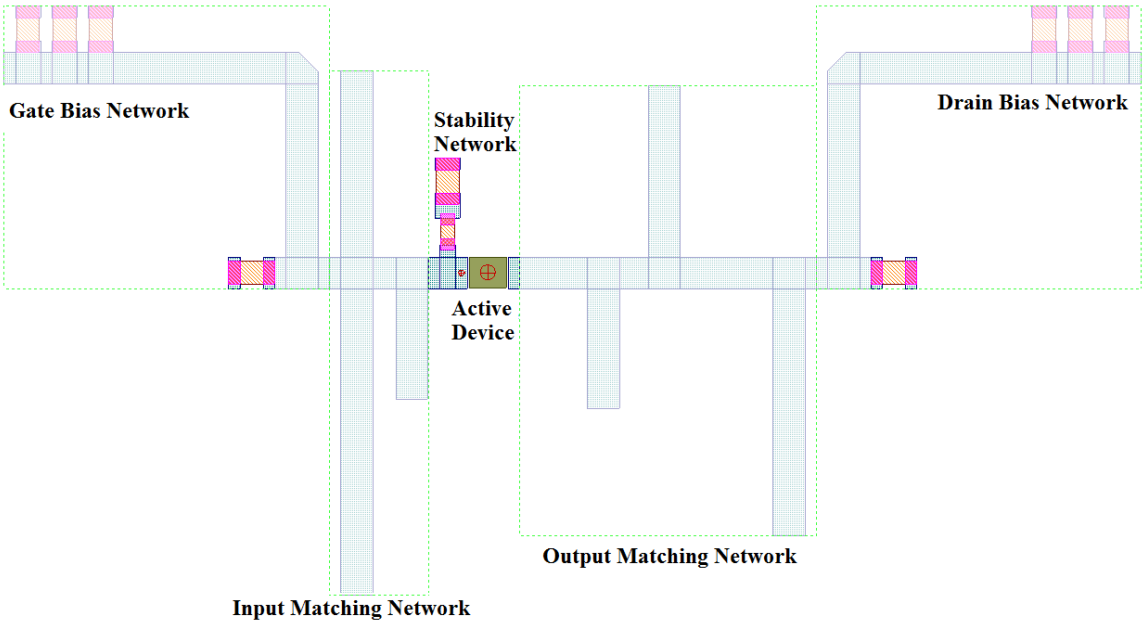

Figure 3.28: Single transistor (1.25mm) 5W power amplifier circuit layout [1]

As shown in Figure 3.28 above, each layout of the identified subcircuits, namely the matching and bias networks, forms the overall layout of the amplifier with the addition of the stability network and input and output dc blocking capacitors.

The single transistor 10W power amplifier schematic is shown below in Figure 3.29.

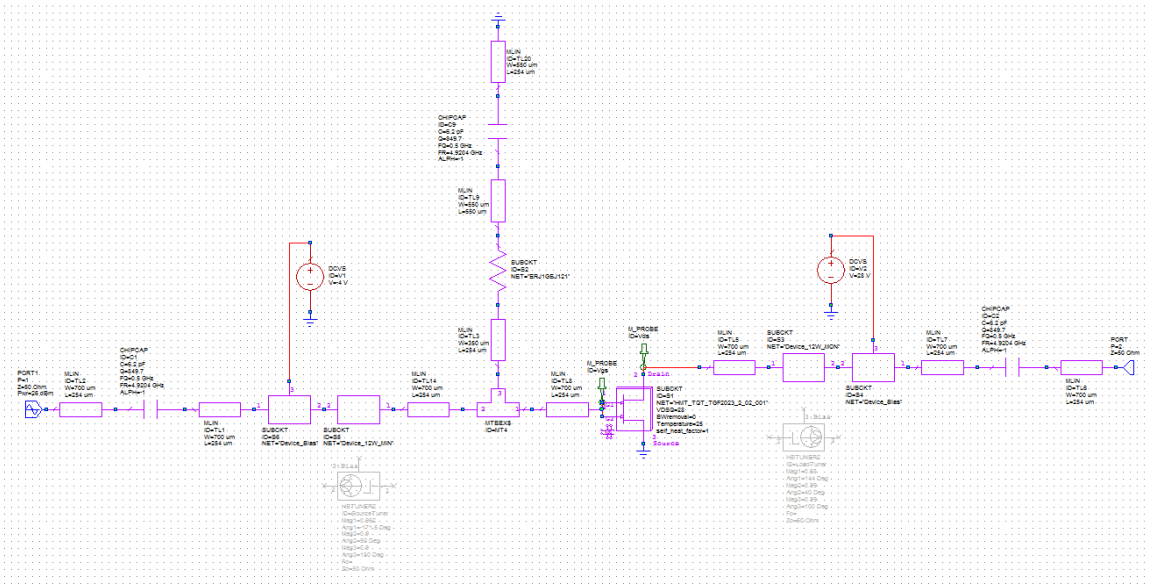

Figure 3.29: Single transistor (2.5mm) 10W power amplifier circuit schematic [1]

As shown in Figure 3.29 above, each subcircuit is again contained within its own subblock and therefore simplifies the overall circuit schematic and allows for ease of optimization and layout.

The layout of the 10W single device amplifier schematic shown in Figure 3.29 above is shown in Figure 3.30 below.

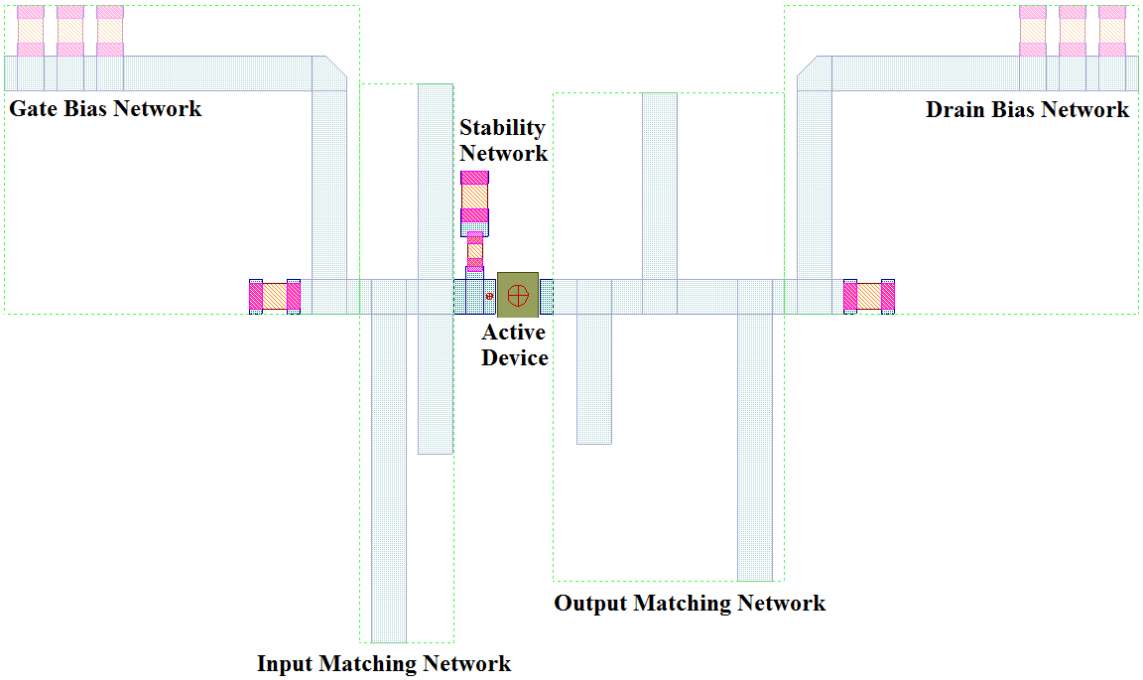

Figure 3.30: Single transistor (2.5mm) 10W power amplifier circuit layout [1]

As shown in Figure 3.30 above, each layout of the identified subcircuits, namely the matching and bias networks, forms the overall layout of the amplifier with the addition of the stability network and input and output dc blocking capacitors.

Finally, the single transistor 20W power amplifier schematic is shown below in Figure 3.31.

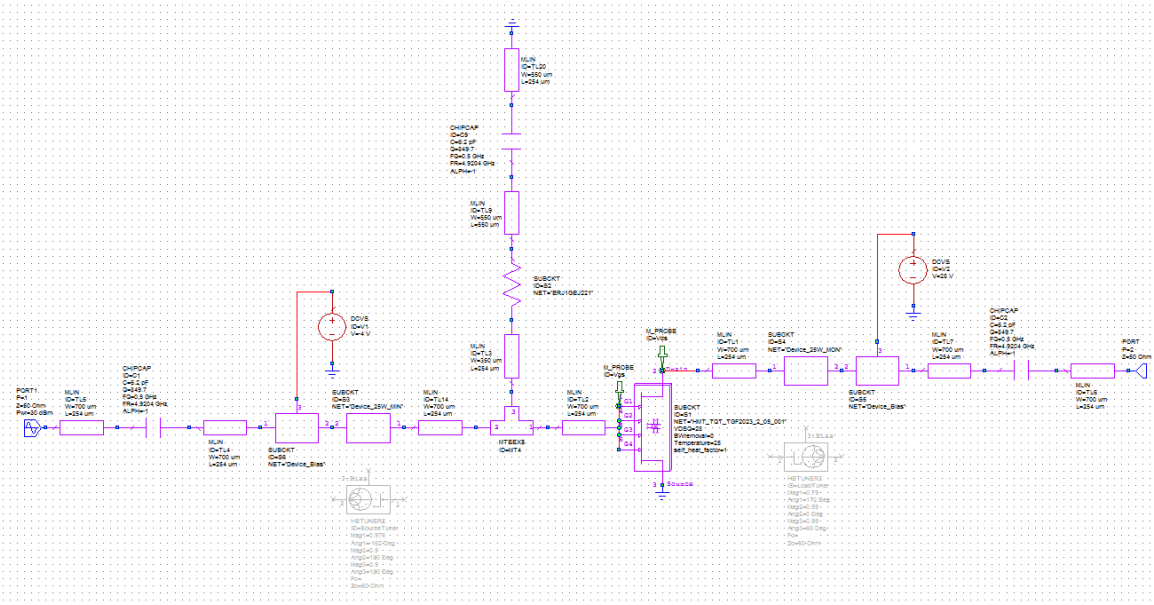

Figure 3.31: Single transistor (5mm) 20W power amplifier circuit schematic [1]

As shown in Figure 3.31 above, each subcircuit is contained within its own subblock and therefore simplifies the overall circuit schematic and allows for ease of optimization and layout.

The layout of the 20W single device amplifier schematic shown in Figure 3.31 above is shown in Figure 3.32 below.

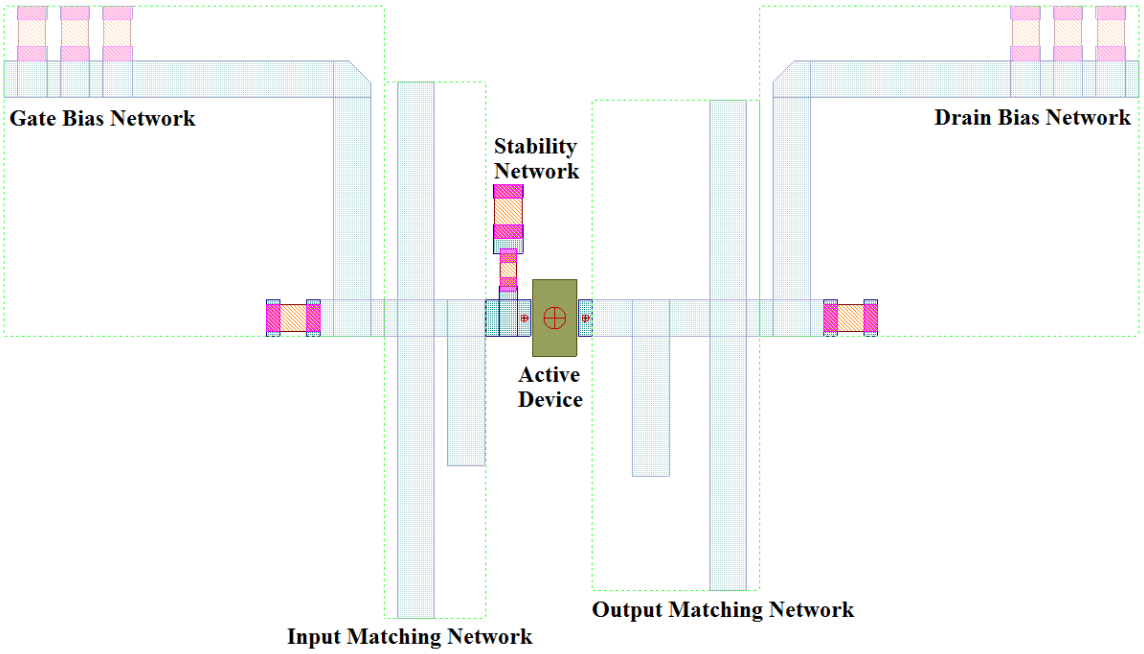

Figure 3.32: Single transistor (5mm) 20W power amplifier circuit layout [1]

As shown in Figure 3.32 above, each layout of the identified subcircuits, namely the matching and bias networks, forms the overall layout of the amplifier with the addition of the stability network and input and output dc blocking capacitors.

3.9 Parallel Transistor Power Amplifiers

Since each single device power amplifier is matched for a 50 Ohm system, it is possible to incorporate the use of the designed Wilkinson power splitter/combiner to increase the overall effective device periphery to scale the output power with the number of active devices accordingly.

The schematic of a 10W power amplifier using two 5W single device power amplifiers is shown in Figure 3.33 below.

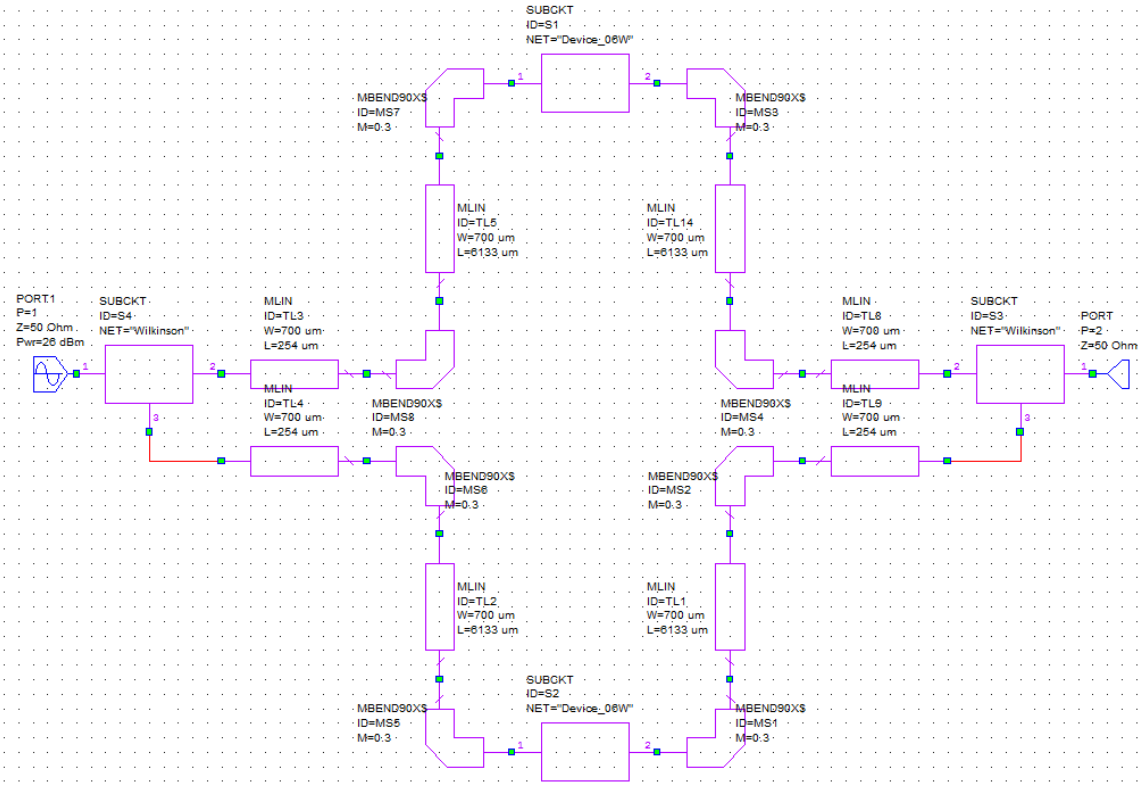

Figure 3.33: Parallel 5W circuits to obtain 10W power amplifier schematic [1]

Using the same modular subcircuit design technique, the layout of the schematic shown in Figure 3.33 above is shown in Figure 3.34 below.

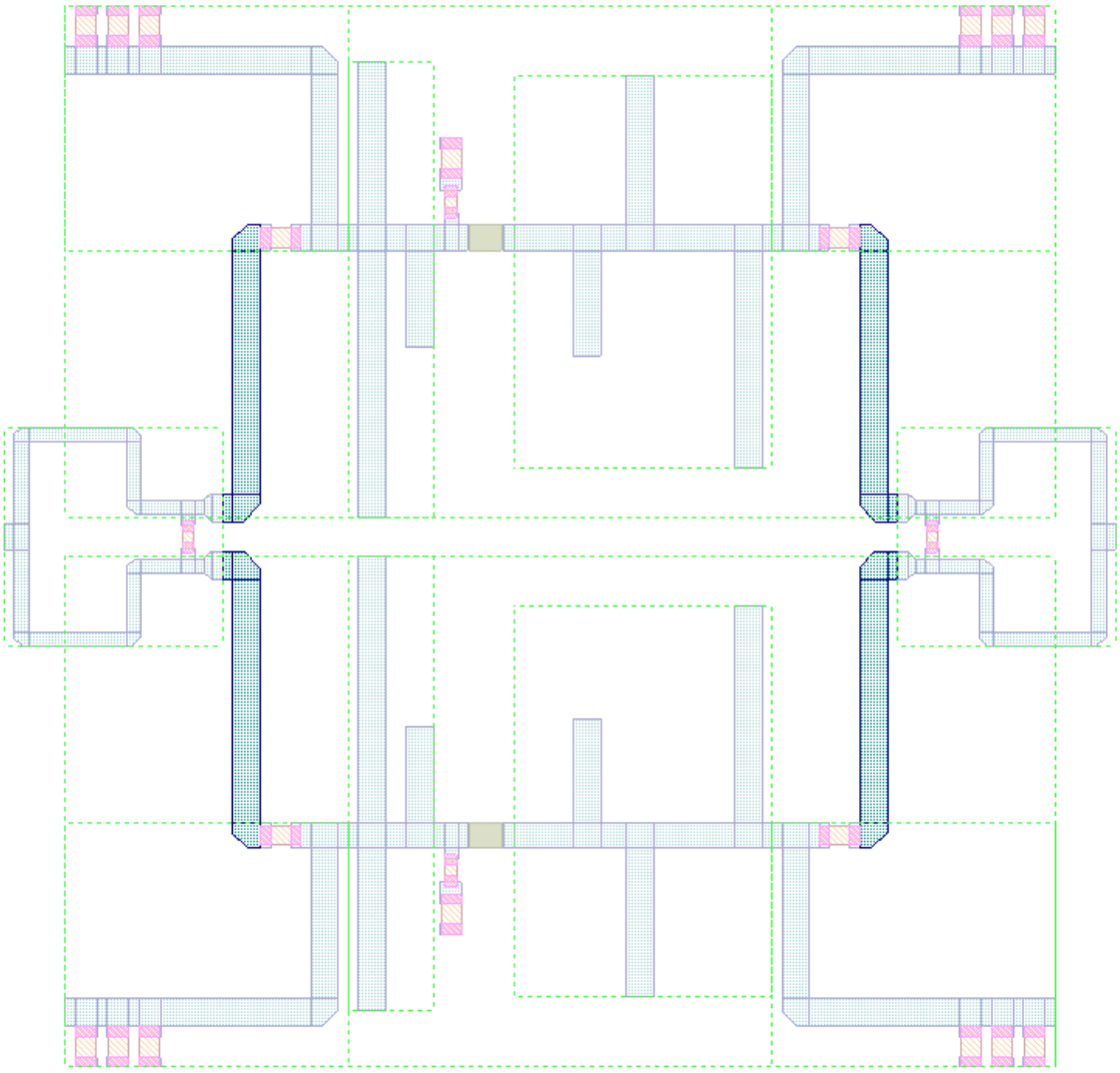

Figure 3.34: Parallel 5W circuits to obtain 10W power amplifier layout [1]

As shown in Figure 3.34 above, the Wilkinson circuitry is incorporated with additional RF routing introduced to accommodate the interconnects between the input and output of the amplifier.

The schematic of a 20W power amplifier using four 5W single device power amplifiers is shown in Figure 3.35 below.

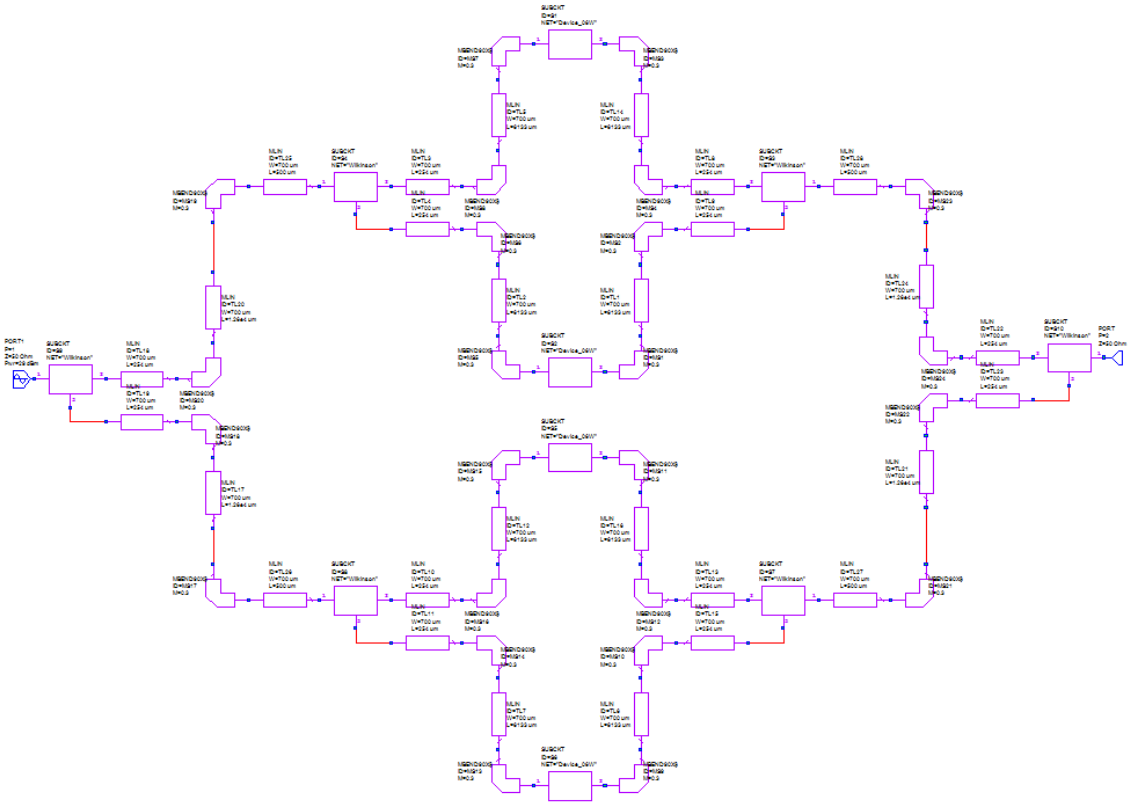

Figure 3.35: Parallel 5W circuits to obtain 20W power amplifier schematic [1]

Using the same modular subcircuit design technique, the layout of the schematic shown in Figure 3.35 above is shown in Figure 3.36 below.

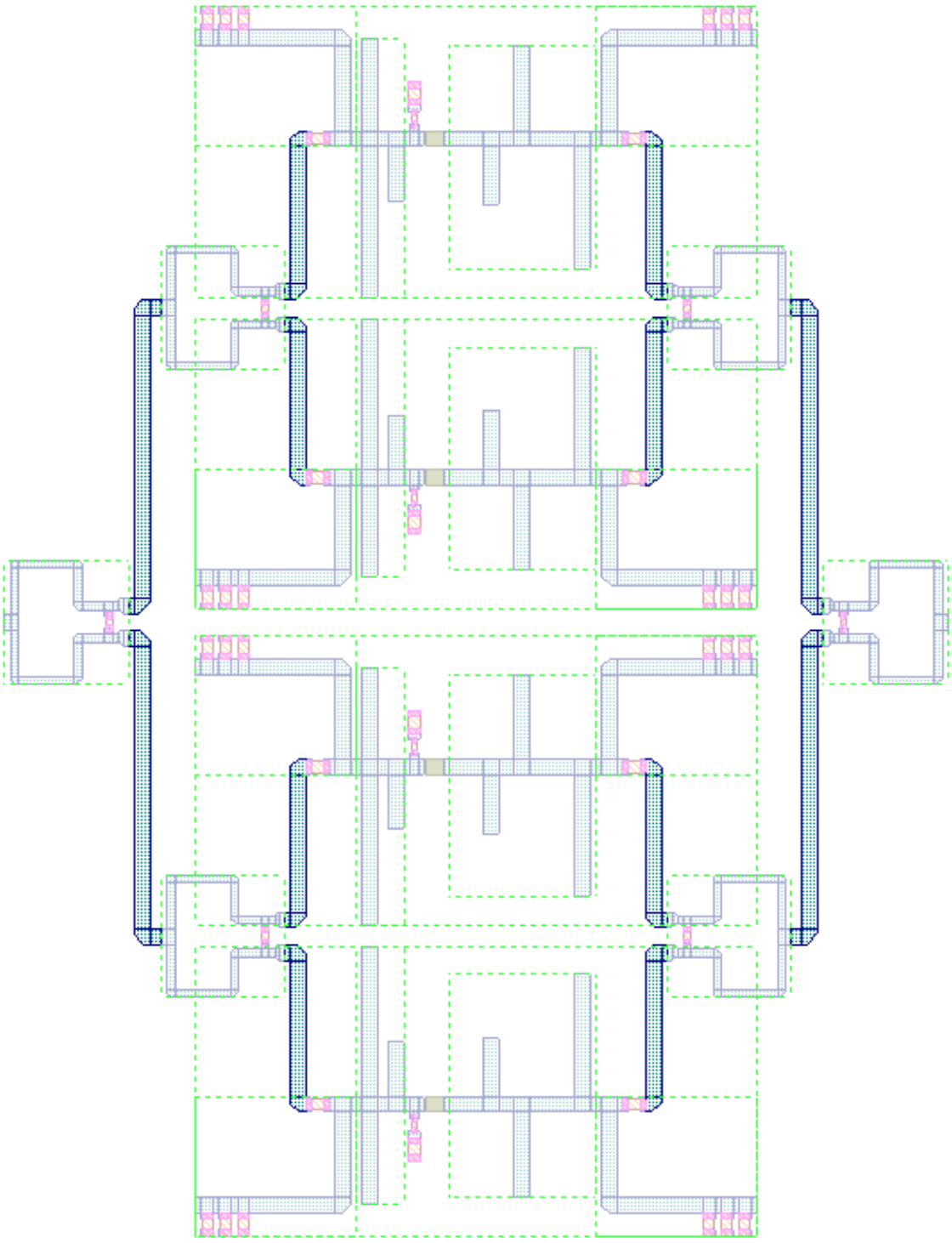

Figure 3.36: Parallel 5W circuits to obtain 20W power amplifier layout [1]

As shown in Figure 3.36 above, the additional Wilkinson circuitry is incorporated with RF routing introduced to accommodate the interconnects between the input and output of the amplifier.

The schematic of a 20W power amplifier using two 10W single device power amplifiers is shown in Figure 3.37 below.

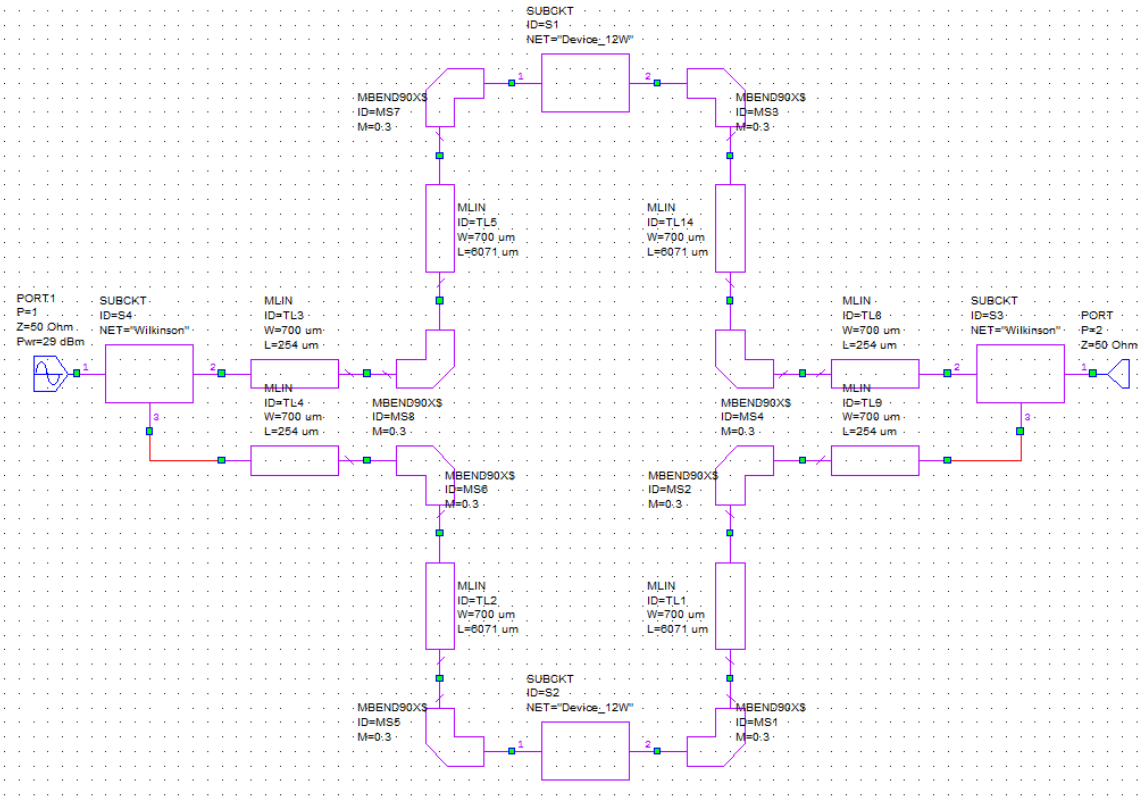

Figure 3.37: Parallel 10W circuits to obtain 20W power amplifier schematic [1]

Using the same modular subcircuit design technique, the layout of the schematic shown in Figure 3.37 above is shown in Figure 3.38 below.

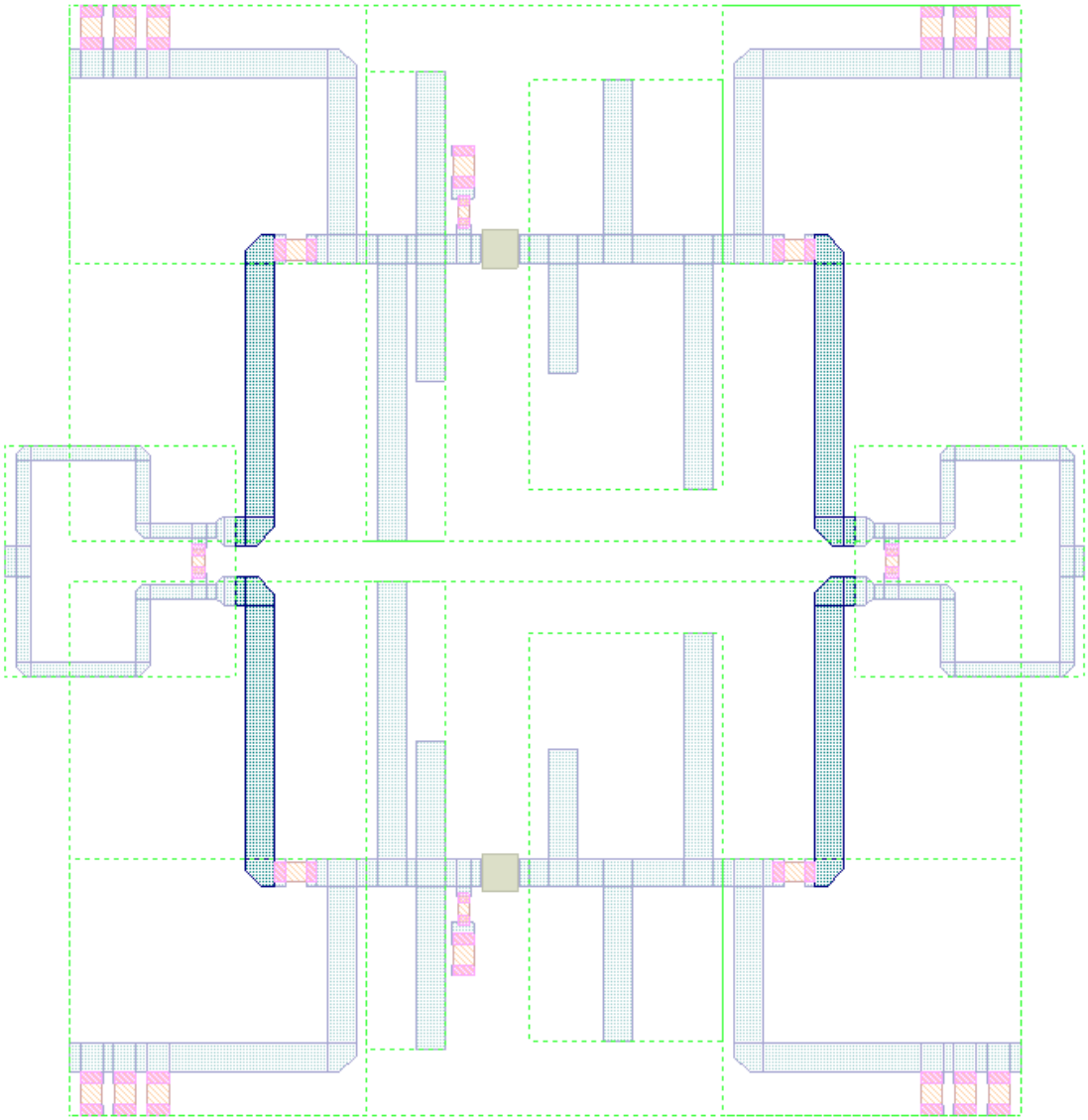

Figure 3.38: Parallel 10W circuits to obtain 20W power amplifier layout [1]

As shown in Figure 3.38 above, the Wilkinson circuitry is incorporated with additional RF routing introduced to accommodate the interconnects between the input and output of the amplifier.

CHAPTER IV

MMIC DESIGN APPROACH

4.1 Transistor IV Curves

The IV characteristics of the selected 600µm MMIC transistor are shown below in Figure 4.1.

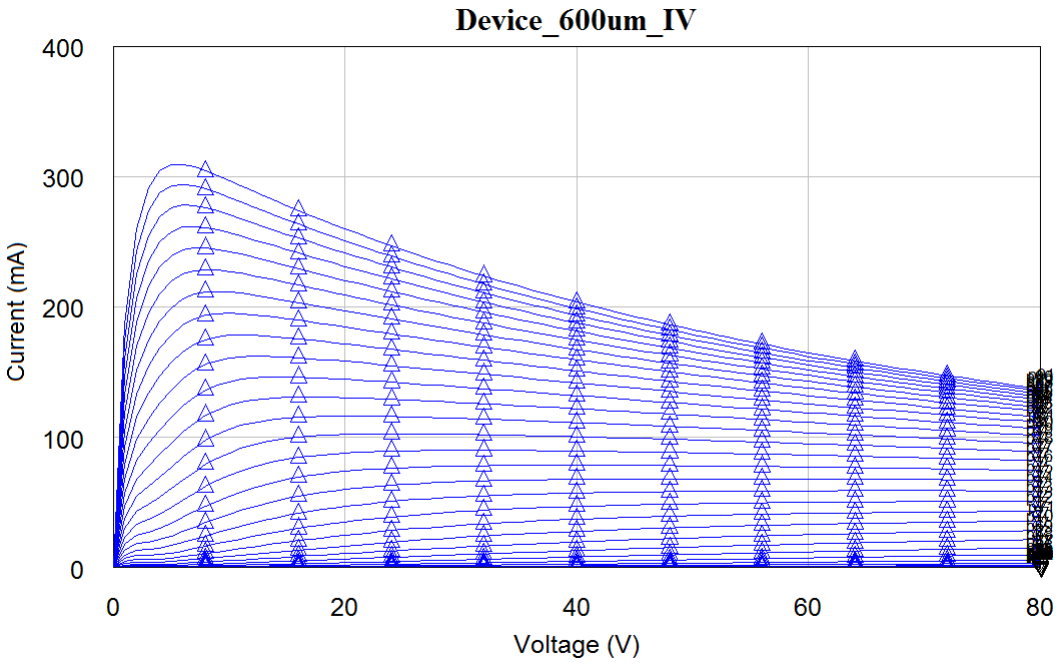

Figure 4.1: MMIC (0.6mm) transistor IV curves

As shown in Figure 4.1 above, the scalable nonlinear transistor model includes the effect of self heating and its impact of the saturation current of the device. The observed hill in the IV curves is characteristic of this effect. For this measurement, the drain to source voltage (Vds) is swept from 0V to 80V while the gate to source voltage (Vgs) is stepped from -5V to -1V in tenth of a voltage increments. This GaN process produces FETs that are depletion mode devices, meaning the device is normally on with a Vgs of 0V. Since the class E mode of operation is desired, Vgs is set to around the pinch-off voltage of approximately -4V and Vds is set to 30V.

4.2 Transistor Stability

For the 0.6mm device biased in the class AB mode condition described in Section 2.3, the geometric stability factor (Mu1) is shown below in Figure 4.2.

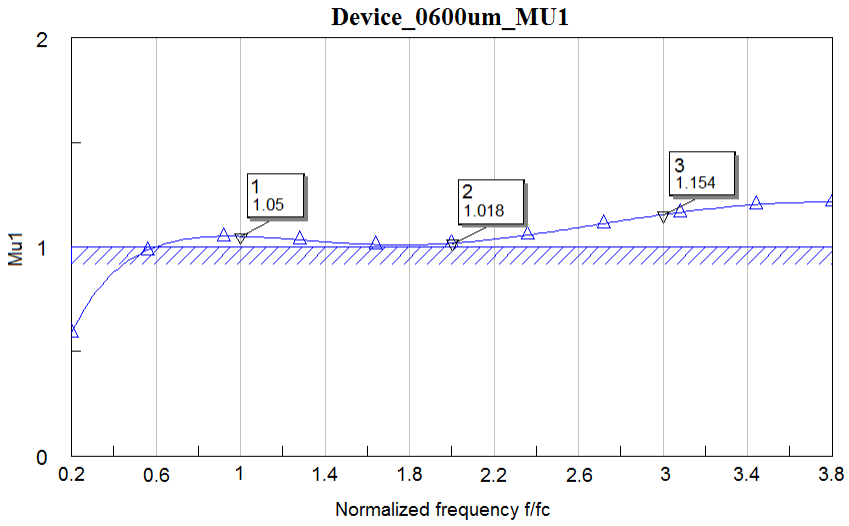

Figure 4.2: MMIC transistor (0.6mm) geometric stability evaluation

As shown in Figure 4.2 above the geometric stability factor is above 1, meaning that the amplifier is unconditionally stable at the design frequency and at the second and third harmonics. The stabilizing network used in the MMIC design is part of the input matching network closest to the gate of the transistor described in Section 4.4. It consists of a simple parallel RC filter that passes the dc bias at a high enough impedance at low frequencies while presenting a low impedance to the operating frequency and the respective harmonics. Other techniques are available to stabilize the transistor and are briefly described in Section 3.2.

4.3 Transistor Load Pull

The load pull contours for the 0.6mm MMIC device are shown below in Figure 4.3.

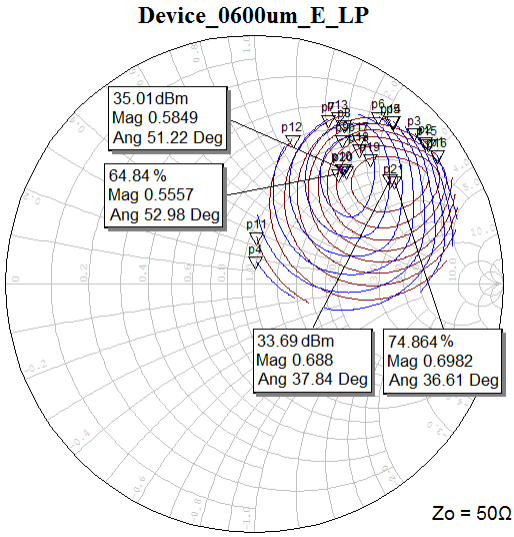

Figure 4.3: MMIC transistor (0.6mm) class E load pull

As shown above in Figure 4.3, the maximum obtainable output power for the selected class E bias conditions is approximately 35dBm (approx. 3W) with a power added efficiency of 65%. Likewise, the peak power added efficiency is approximately 75% with an output power of 33.7dBm

(approx. 2.5W). Since a highly efficiency PA is desired, the fundamental load impedance is selected based on this maximum obtainable power added efficiency. The identified reflection coefficients on the load pull contours are then used to design the fundamental and harmonic matching networks. It should be noted that the load pull tuners in the simulation environment assume lossless matching networks and therefore represent the best possible results. It is clear that any realizable lossy circuit element will detract from the circuit's overall performance.

4.4 Single 2.5W MMIC Power Amplifier

The schematic of the output matching network of the single transistor 2.5W MMIC power amplifier is shown below in Figure 4.4.

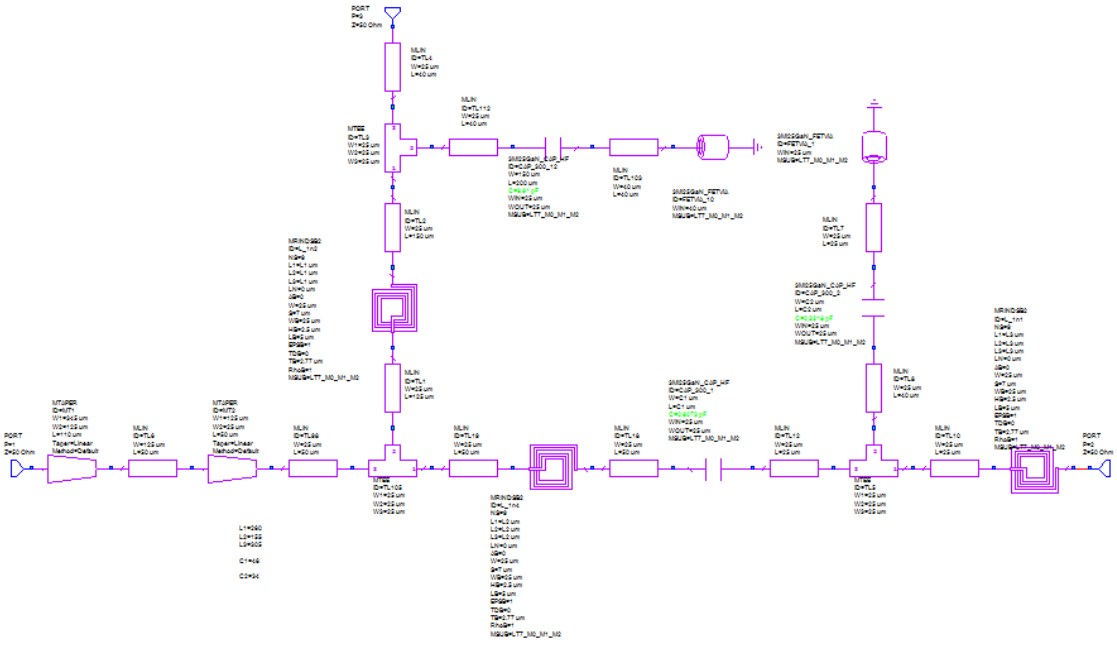

Figure 4.4: Output matching network for 2.5W MMIC amplifier using 0.6mm device

As shown above in Figure 4.4, the matching network consists of microstrip transmission lines, spiral inductors and metal-insulator-metal (MIM) capacitors. This schematic is representative of the final layout of the matching network and its performance is evaluated based on the fundamental and harmonic reflection coefficients presented to the drain of the transistor. Notice that the selected architecture allows for the dc drain bias to pass through the shunt inductor of the matching network. Unlike a typical PC board design, establishing a high inductance RF path to form the dc bias network on a MMIC is difficult to realize without sacrificing space for a quarter-wave stub. Instead, using the match as part of the bias is necessary.

Since the matching network consists of linear elements, it is possible to use an S-parameter matching technique to tune the network so that it presents the desired reflection coefficient (S11) to the output of the transistor. This is done by using variables in the simulation environment to tune the values of the spiral inductors and MIM capacitors until an acceptable match is obtained. The input reflect coefficient of the output matching network is shown in Figure 4.5 below.

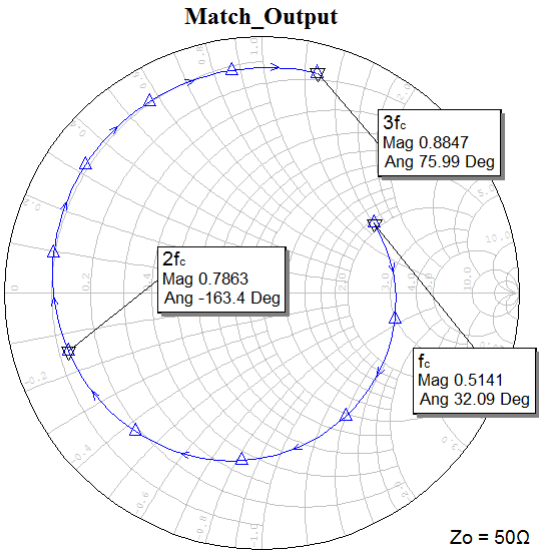

Figure 4.5: Output matching network for 2.5W MMIC amplifier using 0.6mm device

As shown above in Figure 4.5, the output matching network presents a fundamental load reflection coefficient that is close to the desired reflection coefficient obtained from the load pull in Figure 4.3. The discrepancy between the two is primary due to the fact that the load pull simulation presents harmonic terminations that are ideally open for the class E mode, a condition hard to simultaneously realize with a realizable matching network. Most importantly, the angle of the individual reflection coefficients has the most significant impact on the performance of the matching network. The obtained reflection coefficients, while not exactly the correct loading for the ideal class E mode, are suitable for high efficiency operation and actually satisfy another high efficiency class of operation called inverse class F [13].

Like with the output matching network, the input matching network is designed in a similar manner. In this case, the input matching network is matched to the input impedance of the transistor at the fundamental frequency when the desired fundamental and harmonic load impedances are presented to the output of the transistor. The schematic of the input matching network of the single transistor 2.5W MMIC power amplifier is shown below in Figure 4.6.

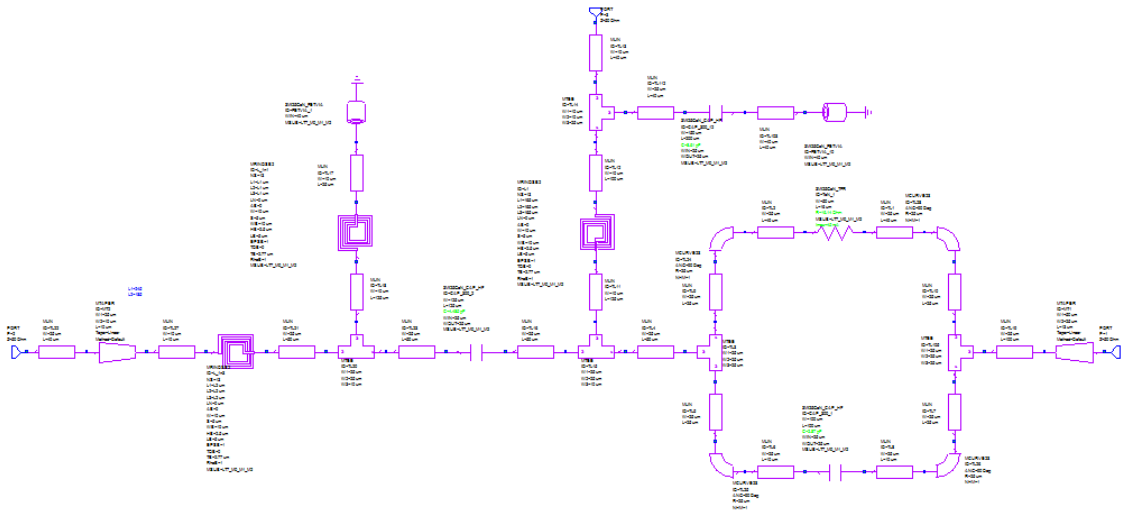

Figure 4.6: Input matching network for 2.5W MMIC amplifier using 0.6mm device

As shown above in Figure 4.6, the matching network consists of microstrip transmission lines, spiral inductors and metal-insulator-metal (MIM) capacitors. This schematic is representative of the final layout of the matching network and its performance is evaluated based on the fundamental and harmonic reflection coefficients presented to the gate of the transistor. Notice that the stability network described in Section 4.2 is part of the input matching network as well as the dc gate bias.

Since the matching network consists of linear elements, it is again possible to use an S-parameter matching technique to tune the network so that it presents the desired reflection coefficient (S22) to the input of the transistor. This is done by using variables in the simulation environment to tune the values of the spiral inductors and MIM capacitors until an acceptable match is obtained. The output reflect coefficient of the input matching network is shown in Figure 4.7 below.

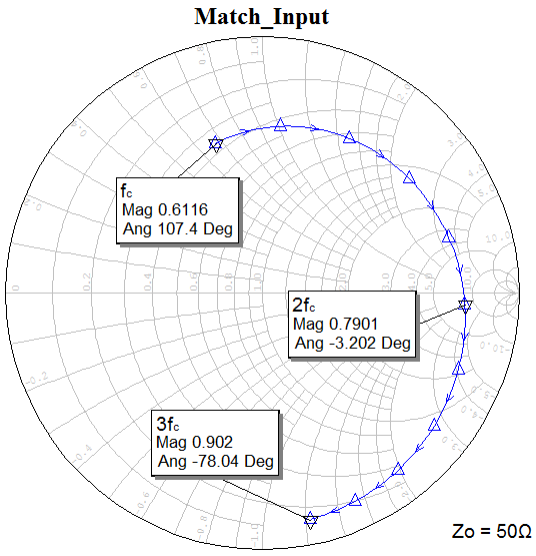

Figure 4.7: Input matching network for 2.5W MMIC amplifier using 0.6mm device

The input and output matching networks are used as sub-circuits to form the larger overall amplifier circuit. Not only does this allow for ease of optimization, but each sub-circuit can be

laid out on an individual basis. The overall schematic of the single transistor 2.5W MMIC power amplifier is shown below in Figure 4.8.

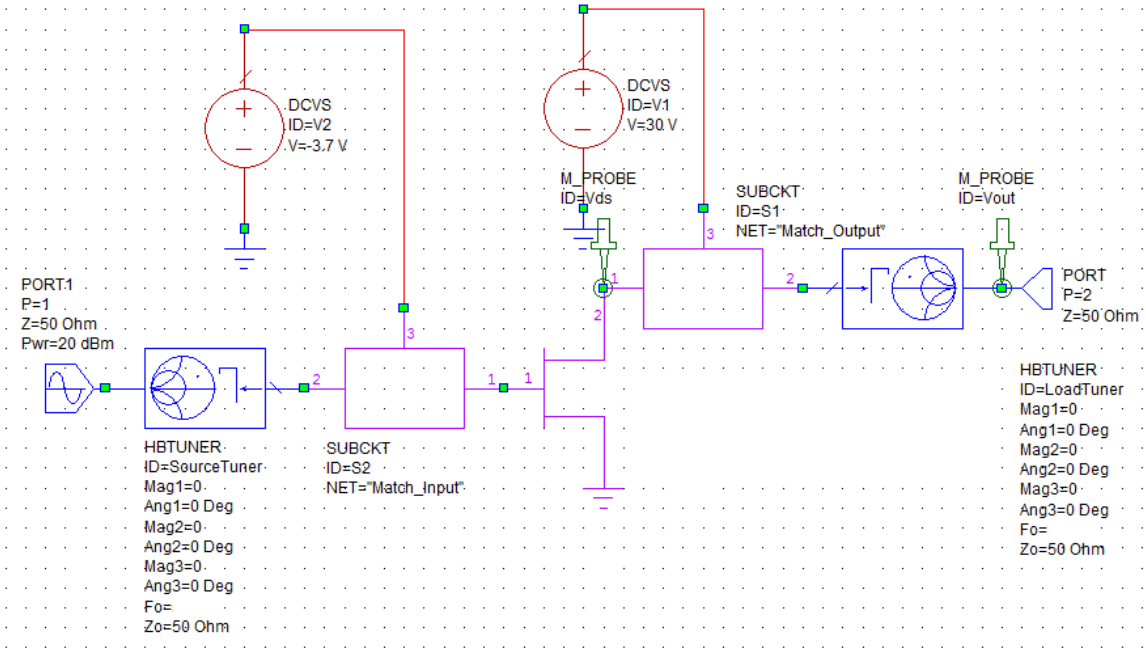

Figure 4.8: MMIC 2.5W power amplifier circuit schematic

From the schematic shown in Figure 4.8 above, the layout of each cell can be generated based on the schematic components. In order to ease the design effort of the layout, the arrangement of the components in the schematic closely represents the placement in the layout. This approach will reduce the amount of time spent on optimizing the circuit as well as resolving any design rule errors that may be triggered due to incorrect placement. The obtained layout is shown in Figure 4.9 below.

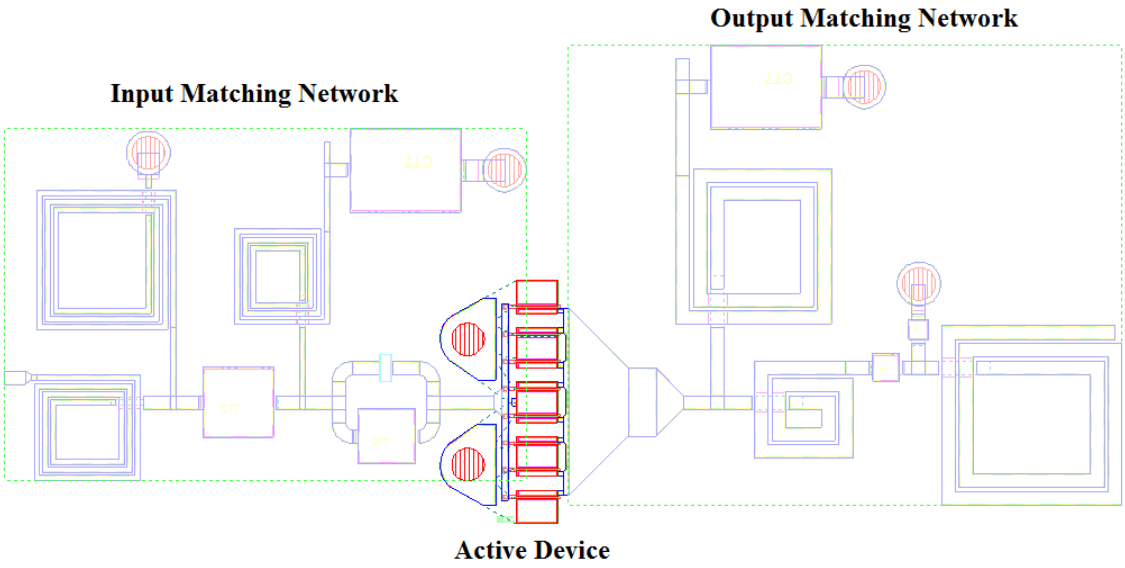

Figure 4.9: MMIC 2.5W power amplifier circuit layout

As shown in Figure 4.9 above, each matching network is contained within its own cell and forms the larger overall circuit.

4.5 Microwave SPDT Switch

In order to provide adequate isolation and bias control of each power transistor when combining smaller transistors to form a high power amplifier, a series-shunt single pole double throw (SPDT) microwave switch is implemented using GaN transistors. The on state resistance of the transistor dictates how much power is lost as heat while the device is conducting. Likewise, the off state capacitance of the transistor dictates how much shunt capacitive reactance is presented to the, in this case, the input and output matching networks while the device is turned off. In order to increase the isolation between input and output paths of the switch while the device is turned off, a grounded shunt path is enabled in order to bring any stray RF across the channel of the off series FET to ground. The schematic of the SPDT switch is shown below in Figure 4.10.

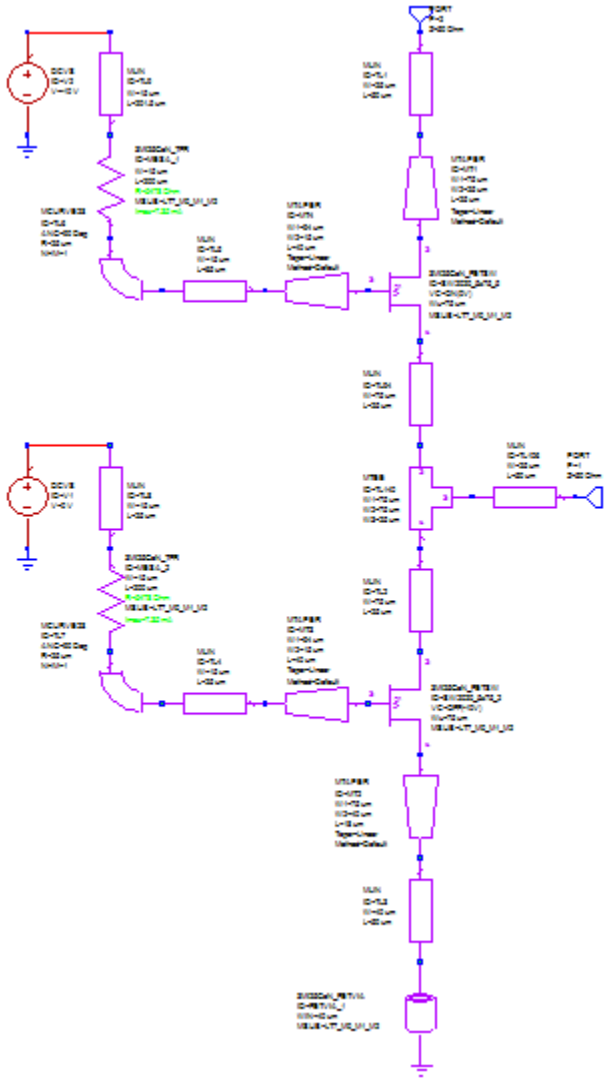

Figure 4.10: MMIC SPDT switch schematic

As shown in Figure 4.10, the switches are modeled as depletion mode devices characterized by foundry measured S-parameters that are dependent on the gate bias of the transistor. A gate to source voltage of 0 V would allow the device to be the fully conducting state. Based on the IV analysis of the nonlinear FET modeled use for the power transistor, a Vgs of less than -5V should be enough to turned the switch completely off. Since only S-parameters are available to evaluate

the performance of the switch, a Vgs of -10V and greater is selected in order to ensure the device remains off when the large signal RF is applied.

The basic layout of the SPDT switch is shown below in Figure 4.11.

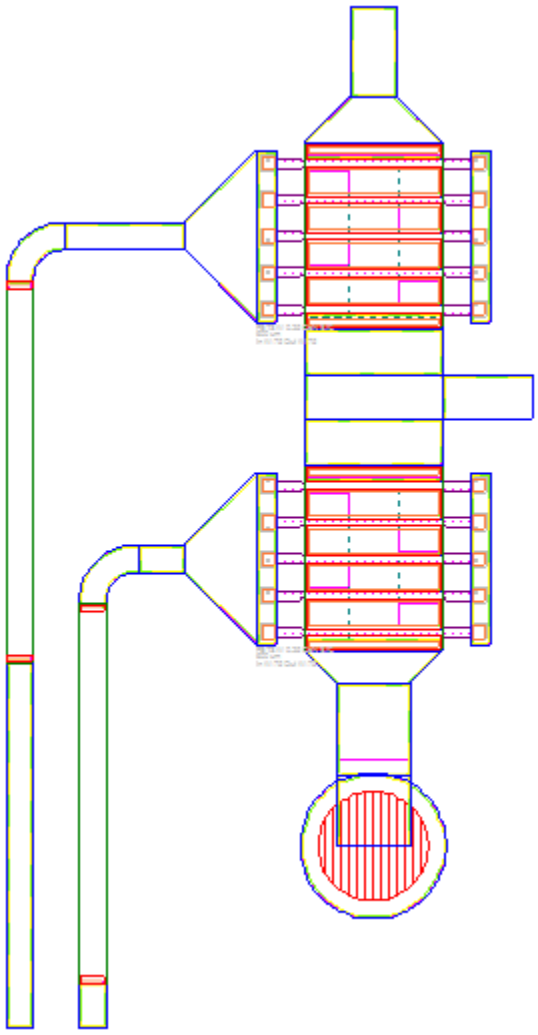

Figure 4.11: MMIC SPDT switch layout

As shown above in Figure 4.11, the size of the transistor is relatively large in order to minimize the on state resistance while introducing a minimal off state capacitance.

4.6 Combined Impedance Selector

In addition to requiring isolation between each parallel amplifying stage, a tunable combined output matching network is necessary to correct the impedance mismatch present while one device is disabled and the other enabled and vice versa. Since a high power and tunable series inductor is difficult to realize, a high pass matching network is designed that allows the effective shunt inductance to be changed based on the state of switched shunt capacitor. In one state, the capacitor is disconnected from the circuit and the inductor is fully participating the impedance transformation from 50 Ohm to approximately 25 Ohm at the design frequency. In the other state, the inductor is resonated out by the use of the shunt capacitor, presenting a low admittance path at the design frequency. This schematic of the impedance selector is shown below in Figure 4.12.

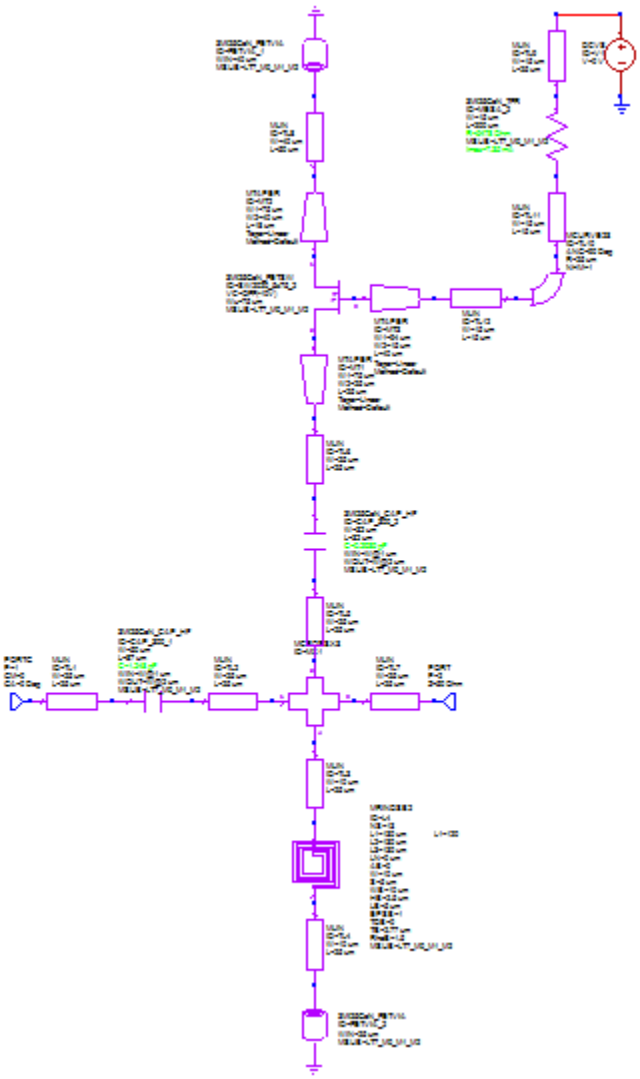

Figure 4.12: Combined impedance selector schematic

As shown in Figure 4.12 above, the tunable matching network utilizes the same FET switch used in the SPDT structure in Section 4.5, a spiral inductor and MIM capacitors. When the shunt capacitor of the match is turned off, the off state capacitance of the FET will effectively form a circuit with two series connected capacitors, that is, the capacitor resonated with inductor and the

parasitic capacitance of the FET. Since the off state capacitance of the FET is very small, the parasitic effect of the overall shunt capacitance will be minimized. The basic layout of the impedance selector is shown below in Figure 4.13.

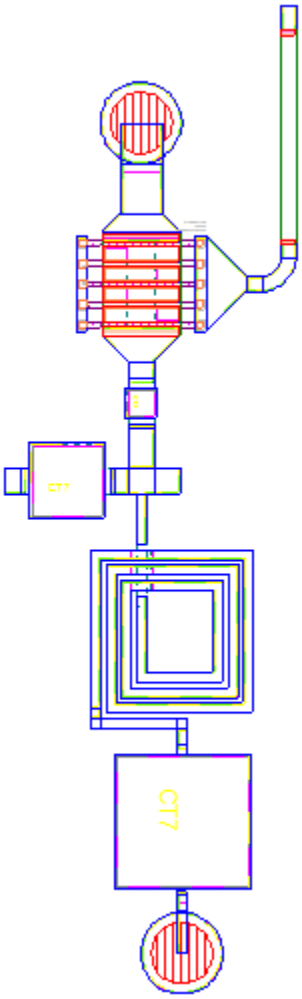

Figure 4.13: Combined impedance selector layout

As shown in Figure 4.13 above, the layout of the impedance selector is dominated by the presence of the shunt switch. While a smaller switch is possible to implement, further research and

evaluation of different size switches and their associated effects in high power RF circuits is necessary.

4.7 Reconfigurable MMIC Power Amplifier

Combining the sub-circuits shown in Sections 4.4 through 4.6, the schematic of the parallel stage and reconfigurable 5W MMIC power amplifier is shown below in Figure 4.14.

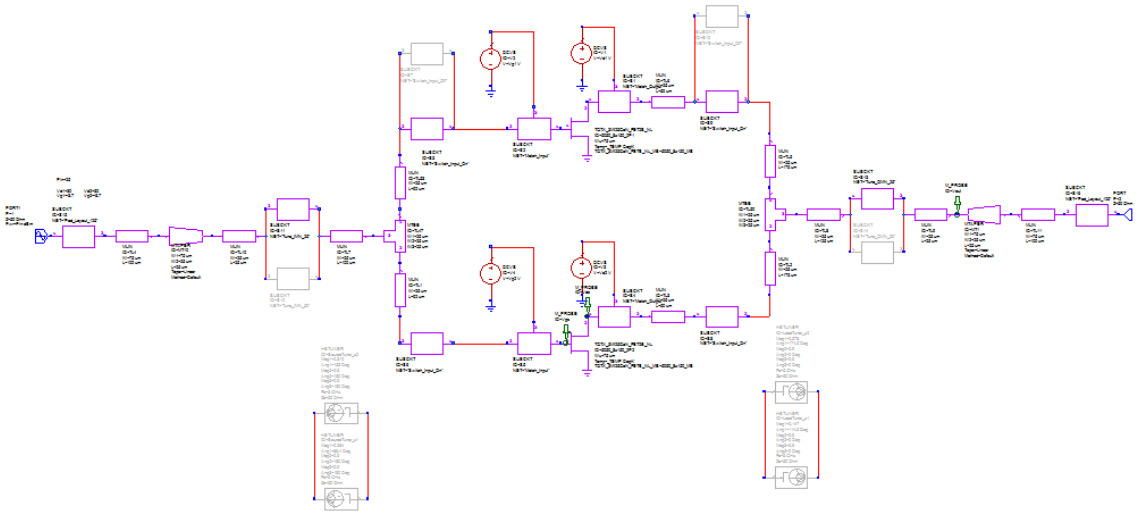

Figure 4.14: Reconfigurable MMIC power amplifier circuit schematic

As shown above in Figure 4.14, the amplifier consists of two identical 2.5W matched transistor stages with SPDT switches at the input and output, which are then combined with the impedance selector at the overall input and output of the amplifier. Each sub-circuit is optimized by using the large signal measurements available in the selected CAD tool. Since the layout of the circuit, namely the sub-circuit interconnects, affect the overall circuit performance, it is necessary to account for the layout in the design procedure using an iterative process. While it may seem counter productive to layout an unfinished circuit during the design and optimization stage, it will allow the final circuit

to be relatively DRC clean if the foundry design rules are observed from the very beginning of the design cycle. Additionally, having a mental picture of the what the final circuit may look like will assist in establishing overall space requirements as well as identifying any potential geometry problems early on. The layout of the reconfigurable power amplifier in Figure 4.14 is shown below in Figure 4.15.

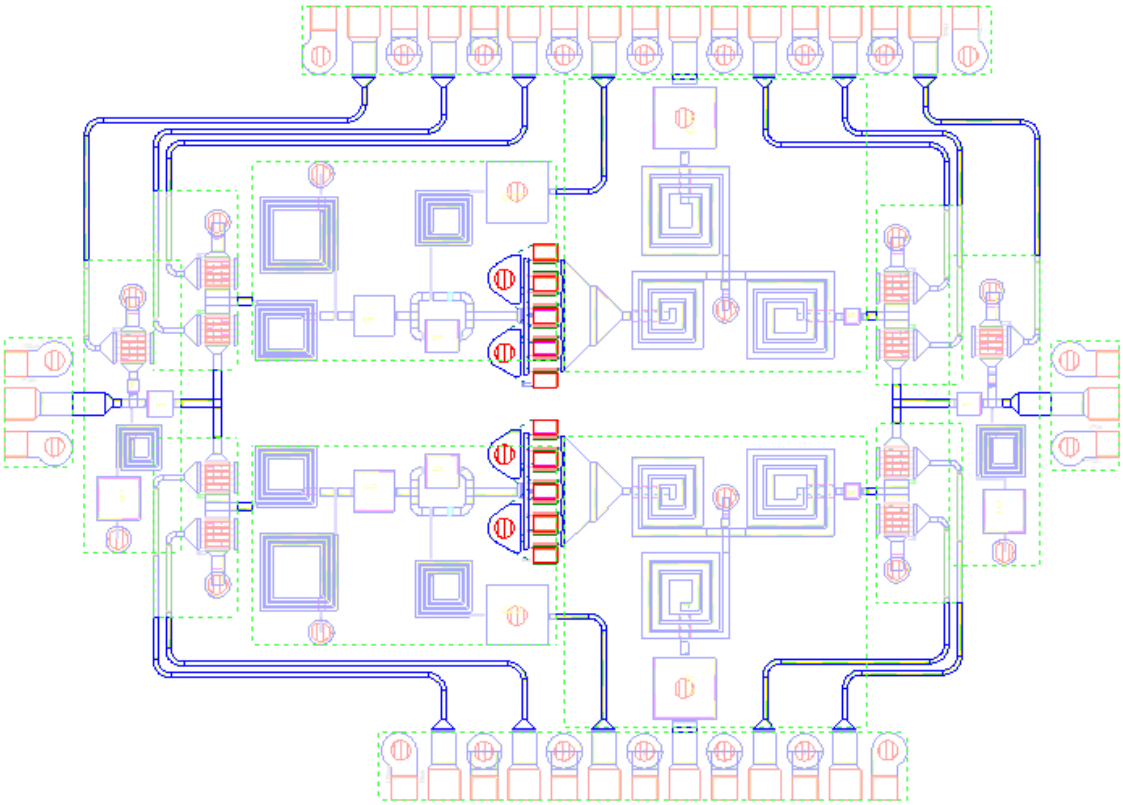

Figure 4.15: Reconfigurable MMIC power amplifier circuit layout

By splitting up each sub-circuit into its own block, the overall schematic shown in Figure 4.14 can be used both for simulation and generating the layout in Figure 4.15 above, which can greatly simplify and streamline the overall design process.

CHAPTER V

HYBRID PACKAGING SIMULATION AND RESULTS

5.1 Wilkinson Power Splitter/Combiner

The simulated small-signal S-parameter evaluation of the designed Wilkinson power splitter/combiner used in the hybrid packaged power amplifiers is shown below in Figure 5.1.

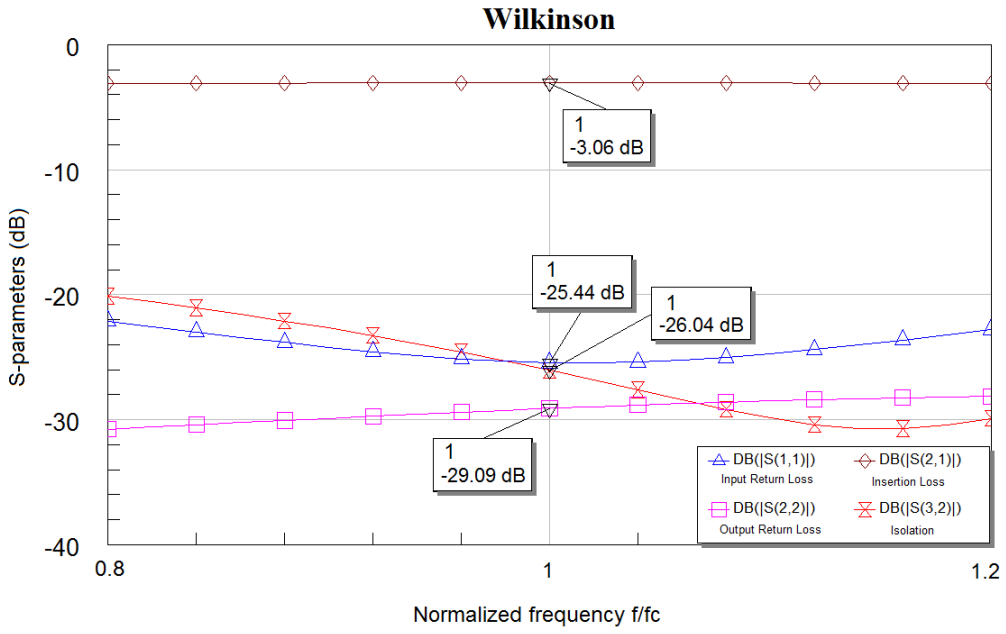

Figure 5.1: Distributed Wilkinson S-parameters

As shown above in Figure 5.1, the Wilkinson introduces an insertion loss of approximately 0.06 dB more than the inherent 3 dB insertion loss characteristic of an ideal 2-way power splitter. Additionally, the RF isolation between the output ports is approximately 26 dB at the center frequency. Finally, the return loss presented at each port is greater than 20 dB across a 20% bandwidth. Both output/split ports are electrically symmetrical and therefore only one set of S-parameters are shown to characterize the 50 Ohm terminated input and output ports.

5.2 Gate and Drain Bias Networks

The simulated small-signal S-parameter performance of the gate and drain dc bias networks is shown below in Figure 5.2.

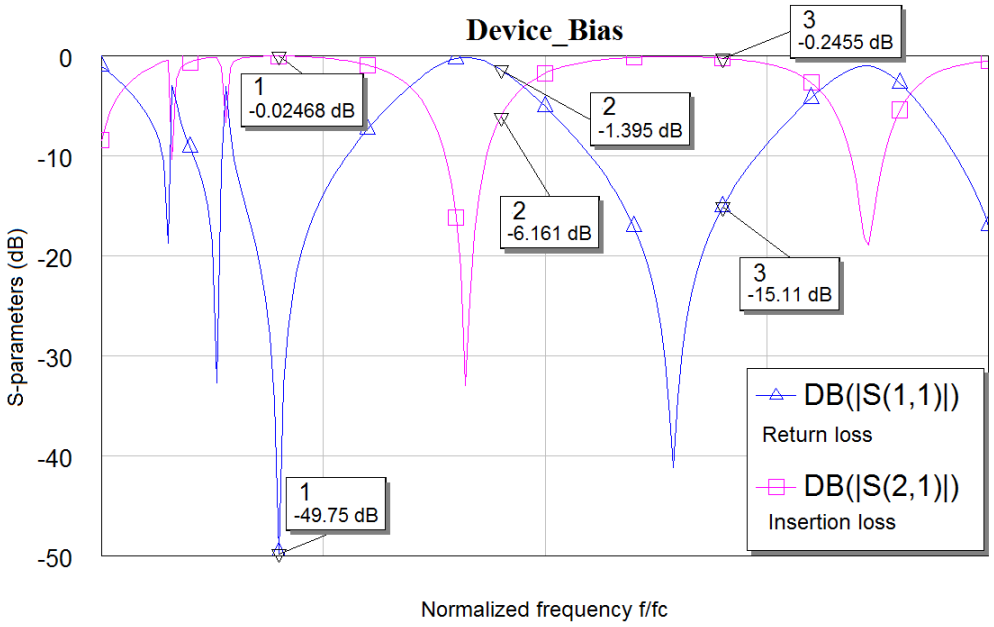

Figure 5.2: Gate and drain bias network S-parameters

As shown above in Figure 5.2, the quarter-wave stub bias network has a minimal impact on the input and output matching networks at the design frequency, fc. The bias network introduces an additional insertion loss of approximately 0.03 dB and presents an input return loss of about 50 dB. Since the quarter-wave stub is a periodic structure, performance at the second and third harmonics of the design frequency is critical. However, because the matching networks of the designed amplifiers explicitly set the load and source reflection coefficients at the second and thirds harmonics before the inclusion of the bias networks, the impact of the bias network on the harmonic terminations can be safely ignored. Notice that the behavior of the network response below the design frequency is due to the self resonance of the vendor modeled bypass capacitors.

5.3 Single Transistor Power Amplifiers

The simulated large signal performance of a single transistor 5W power amplifier is shown below in Figure 5.3.

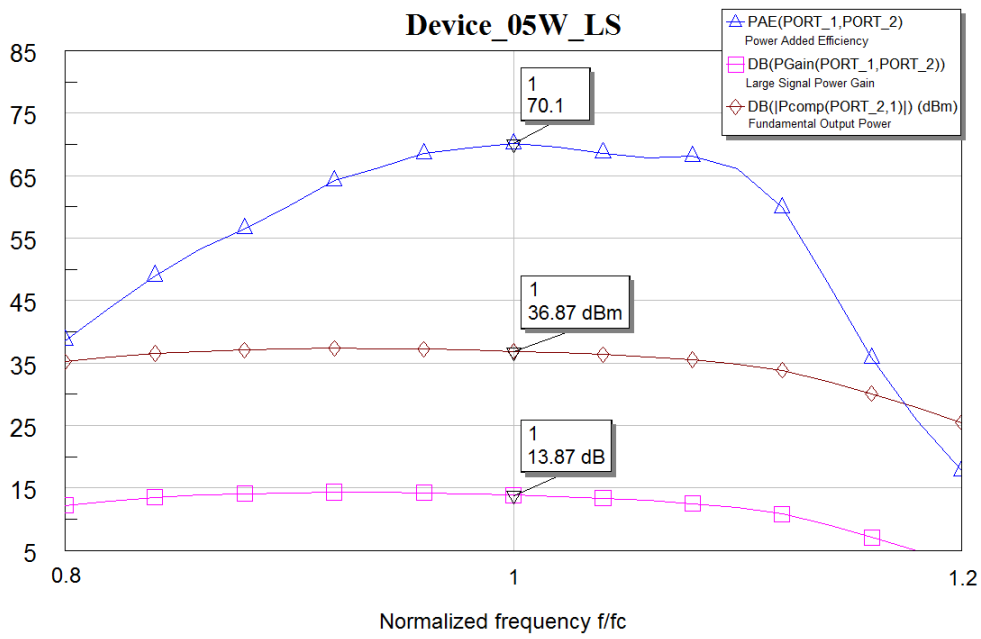

Figure 5.3: Single transistor 5W power amplifier circuit large signal performance [1]

As shown above in Figure 5.3, the single transistor power amplifier delivers approximately 5W of output power with a power added efficiency of 70% and a large signal gain of approximately 14 dB at the design frequency. This circuit is used as the foundation of the combined transistor power amplifier circuits utilizing multiples of the same 1.25mm active device.

The simulated time domain voltage and current waveforms at the drain of the single transistor 5W power amplifier is shown below in Figure 5.4.

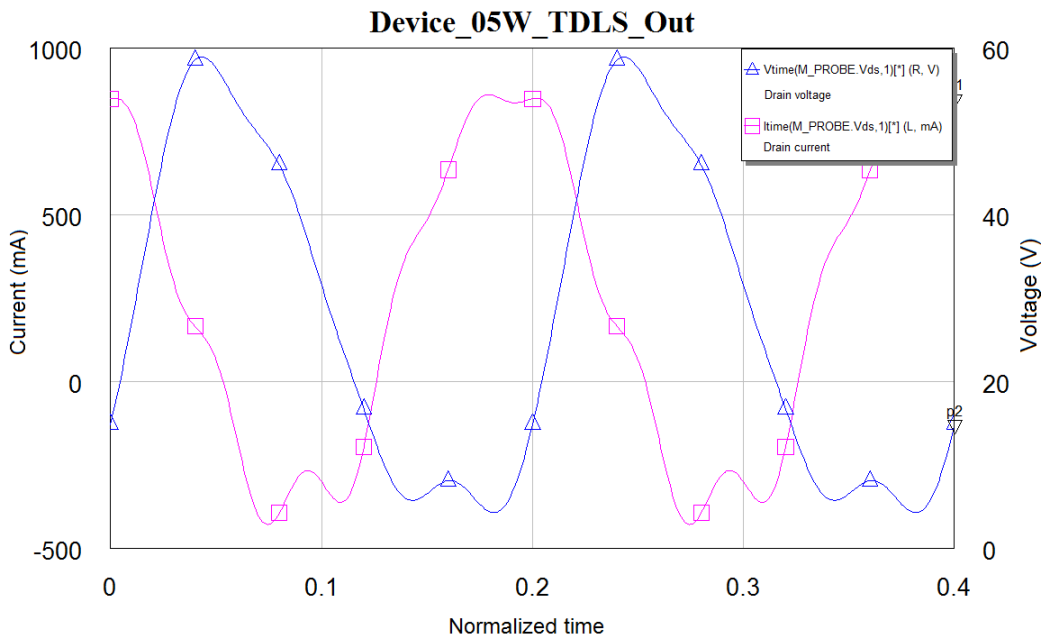

Figure 5.4: Single transistor 5W power amplifier circuit large signal voltage and current [1]

As shown above in Figure 5.4, the voltage and current waveforms are approximately in quadrature with each other and resemble that of a low-pass filtered square-wave. The physical characteristics of the real transistor and lossy matching networks account for this less than ideal switching behavior that would have otherwise been expected from a class E mode power amplifier [13].

The simulated large signal performance of a single transistor 10W power amplifier is shown below in Figure 5.5.

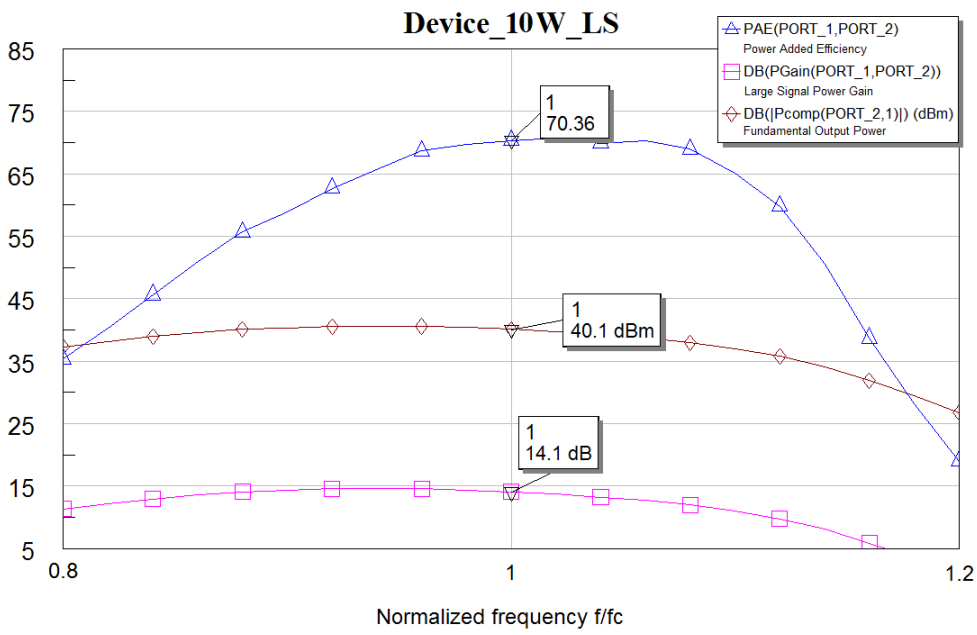

Figure 5.5: Single transistor 10W power amplifier circuit large signal performance [1]

As shown above in Figure 5.5, the single transistor power amplifier delivers approximately 10W of output power with a power added efficiency of 70% and a large signal gain of approximately 14 dB at the design frequency. This circuit is used as the foundation of the combined transistor power amplifier circuits utilizing multiples of the same 2.5mm 10W active device.

The simulated time domain voltage and current waveforms at the drain of the single transistor 10W power amplifier is shown below in Figure 5.6.

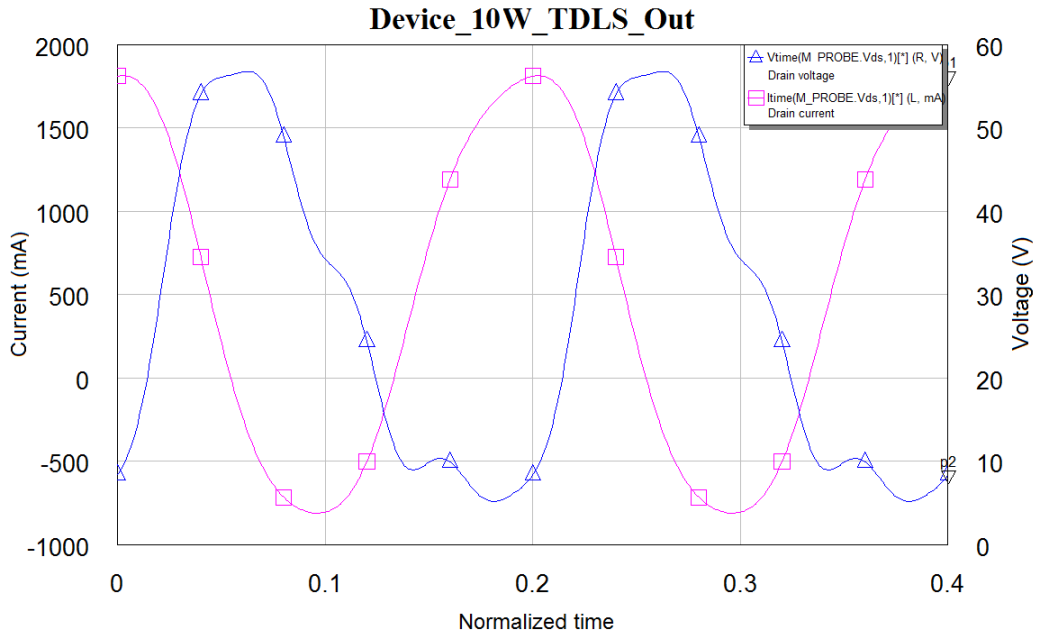

Figure 5.6: Single transistor 10W power amplifier circuit large signal voltage and current [1]

As shown above in Figure 5.6, the voltage and current waveforms are again approximately in quadrature with each other and resemble that of a low-pass filtered square-wave. The physical characteristics of the real transistor and lossy matching networks account for this less than ideal switching behavior that would have otherwise been expected from a class E mode power amplifier [13].

The simulated large signal performance of a single transistor 20W power amplifier is shown below in Figure 5.7.

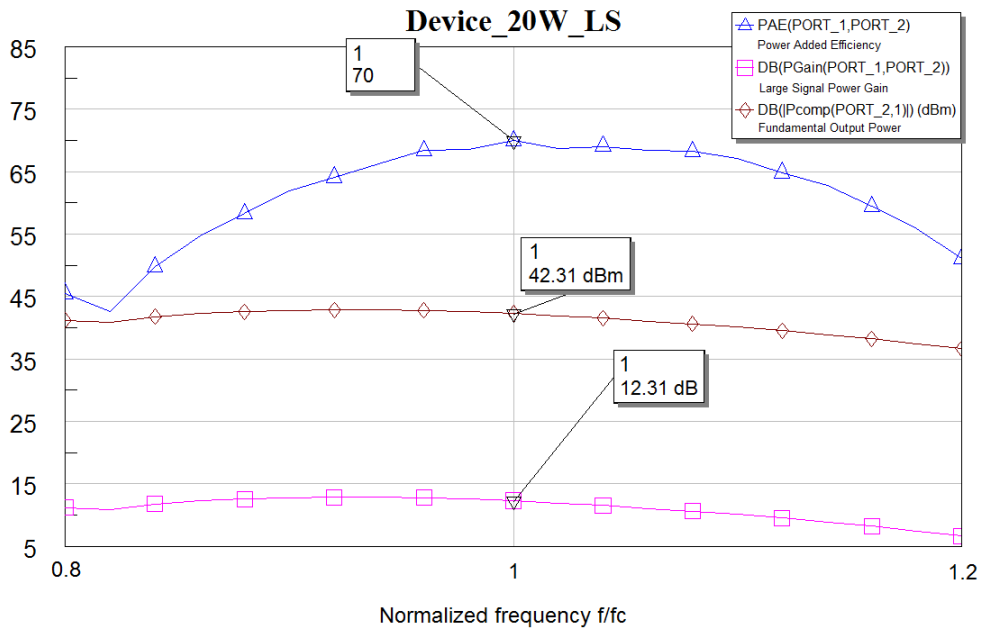

Figure 5.7: Single transistor 20W power amplifier circuit large signal performance [1]

As shown above in Figure 5.7, the single transistor power amplifier delivers approximately 17W of output power with a power added efficiency of 70% and a large signal gain of approximately 12 dB at the design frequency. This circuit implements the largest active device periphery (5mm) in this thesis and is used for comparison between combining multiple smaller active devices to obtain the same large signal performance.

The simulated time domain voltage and current waveforms at the drain of the single transistor 20W power amplifier is shown below in Figure 5.8.

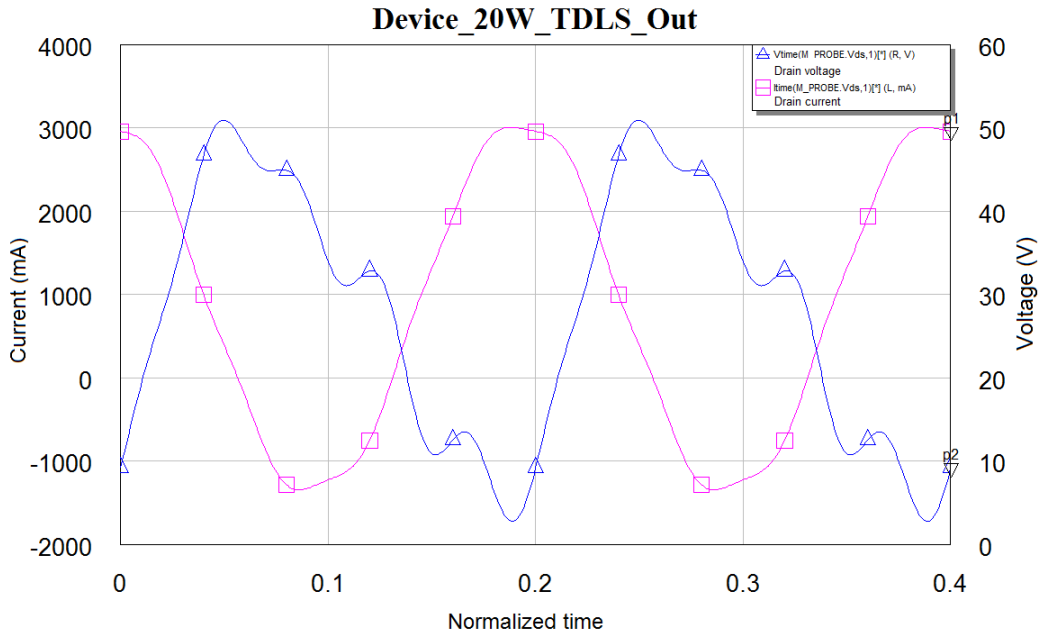

Figure 5.8: Single transistor 20W power amplifier circuit large signal voltage and current [1]

As shown above in Figure 5.8, the voltage and current waveforms are again approximately in quadrature with each other and resemble that of a low-pass filtered square-wave. The physical characteristics of the real transistor and lossy matching networks account for this less than ideal switching behavior that would have otherwise been expected from a class E mode power amplifier [13].

5.4 Parallel Transistor Power Amplifiers

The simulated large signal performance of two parallel 5W power amplifier circuits using a Wilkinson to obtain a 10W power amplifier is shown below in Figure 5.9.

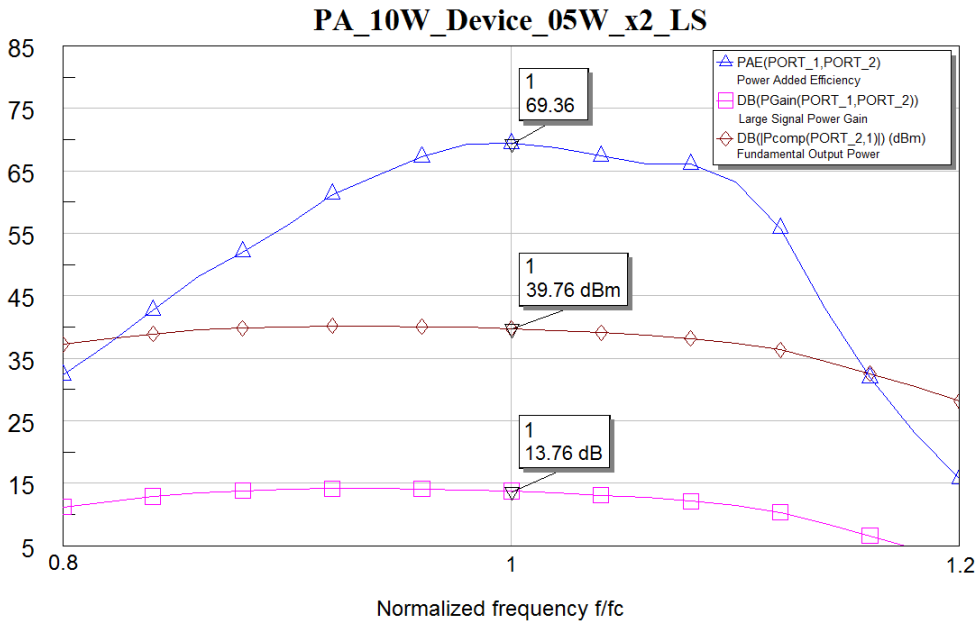

Figure 5.9: Parallel 5W circuits to obtain 10W power amplifier large signal performance [1]

As shown above in Figure 5.9, the two parallel 5W power amplifier circuits deliver approximately 10W of output power with a power added efficiency of 70% and a large signal gain of approximately 14 dB at the design frequency.

The simulated large signal performance of four parallel 5W power amplifier circuits using a Wilkinson to obtain a 20W power amplifier is shown below in Figure 5.10.

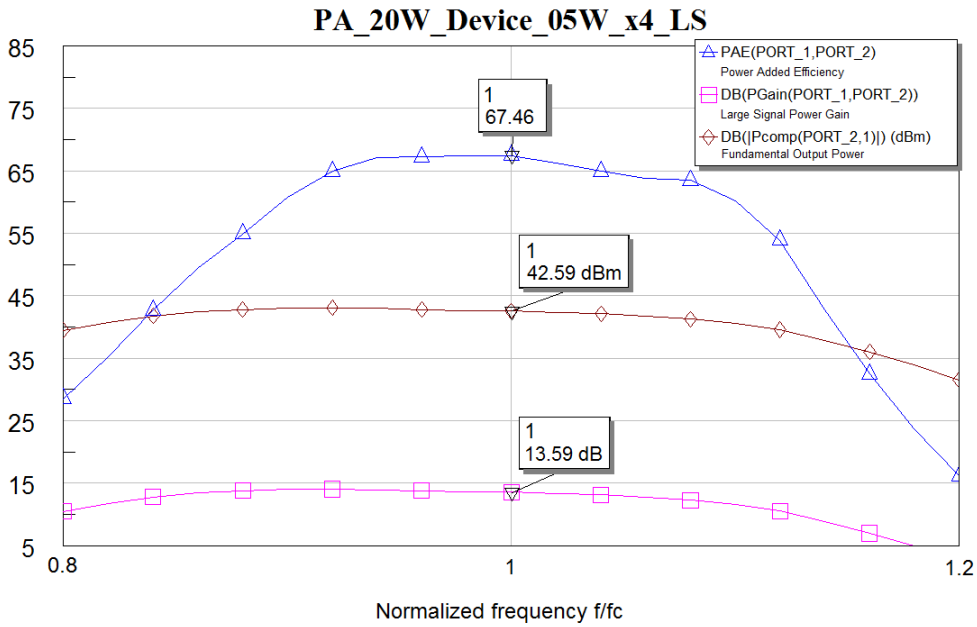

Figure 5.10: Parallel 5W circuits to obtain 20W power amplifier large signal performance [1]

As shown above in Figure 5.10, the four parallel 5W power amplifier circuits deliver approximately 20W of output power with a power added efficiency of 70% and a large signal gain of approximately 14 dB at the design frequency.

The simulated large signal performance of two parallel 10W power amplifier circuits using a Wilkinson to obtain a 20W power amplifier is shown below in Figure 5.11.

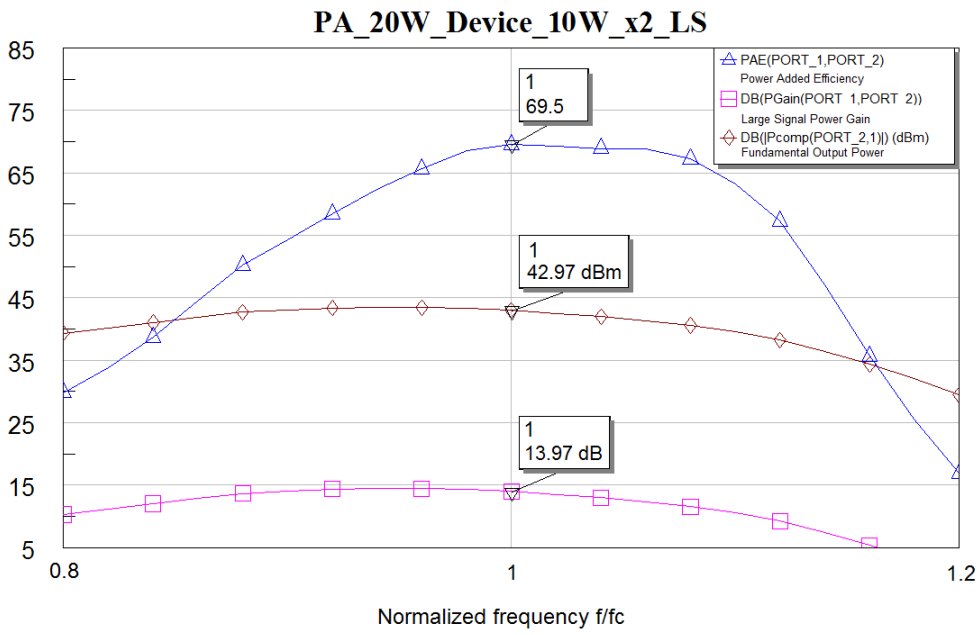

Figure 5.11: Parallel 10W circuits to obtain 20W power amplifier large signal performance [1]

As shown above in Figure 5.11, the two parallel 10W power amplifier circuits deliver approximately 20W of output power with a power added efficiency of 70% and a large signal gain of approximately 14 dB at the design frequency.

The results of these simulations show that the output power of the amplifier does scale with the size and number of transistors utilized in the design. The slight reduction in power added efficiency and output power in the parallel stage amplifiers when compared with their equivalent single stage amplifier is the result of additional insertion and mismatch losses introduced by the Wilkinson. The option to design the amplifier with smaller parallel transistors instead of a single larger device will depend on the cost and size restrictions of the system; however, if each single stage is carefully designed, it is possible to easily combine them using either a Wilkinson or other power

splitter/combiner circuitry. A summary of the simulated performance obtained from the designed hybrid packaged GaN class E power amplifiers is shown below in Table 5.1.

Table 5.1: Hybrid Packaged GaN Power Amplifier Summary

Device Size [mm]	Active Devices [#]	Power [W]	PAE [%]	Gain [dB]
1.25	1	4.86	70.1%	13.87
2.5	1	10.23	70.36%	14.1
1.25	2	9.46	69.36%	13.76
5	1	17.02	70%	12.31
2.5	2	19.81	69.5%	13.97
1.25	4	18.15	67.46%	13.59

CHAPTER VI

MMIC SIMULATION AND RESULTS

6.1 Single 2.5W Power Amplifier

The simulated large signal performance of a single transistor 2.5W integrated power amplifier is shown below in Figure 6.1.

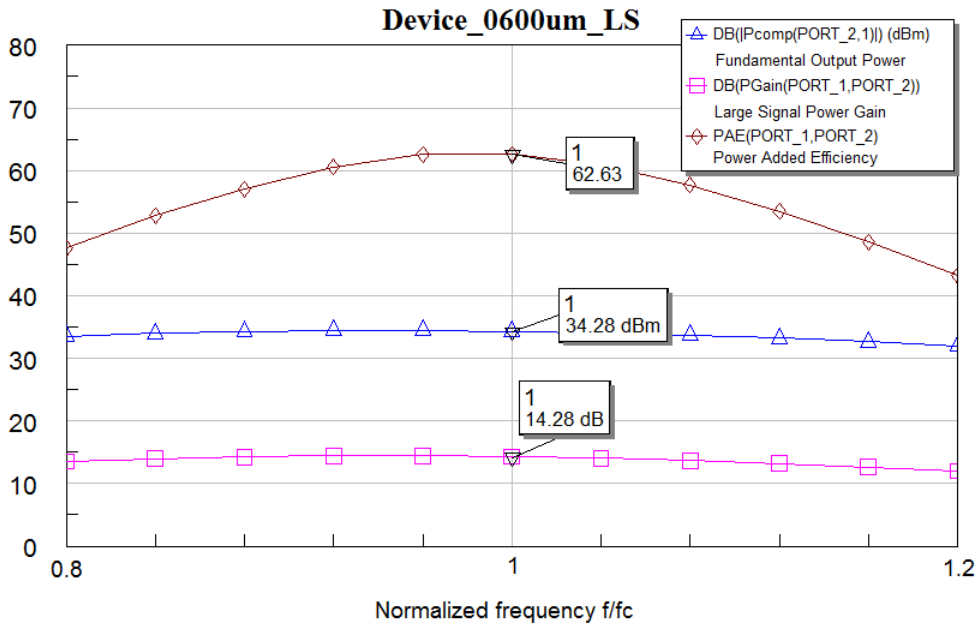

Figure 6.1: MMIC 2.5W power amplifier circuit large signal performance

As shown above in Figure 6.1, the single transistor power amplifier delivers approximately 2.5W of output power with a power added efficiency of 62% and a gain of approximately 14 dB at the design frequency. This circuit is used as the foundation of the reconfigurable MMIC power amplifier circuit that combines two 0.6mm active devices.

The simulated large signal input reflection coefficient of the single transistor 2.5W power amplifier is shown below in Figure 6.2.

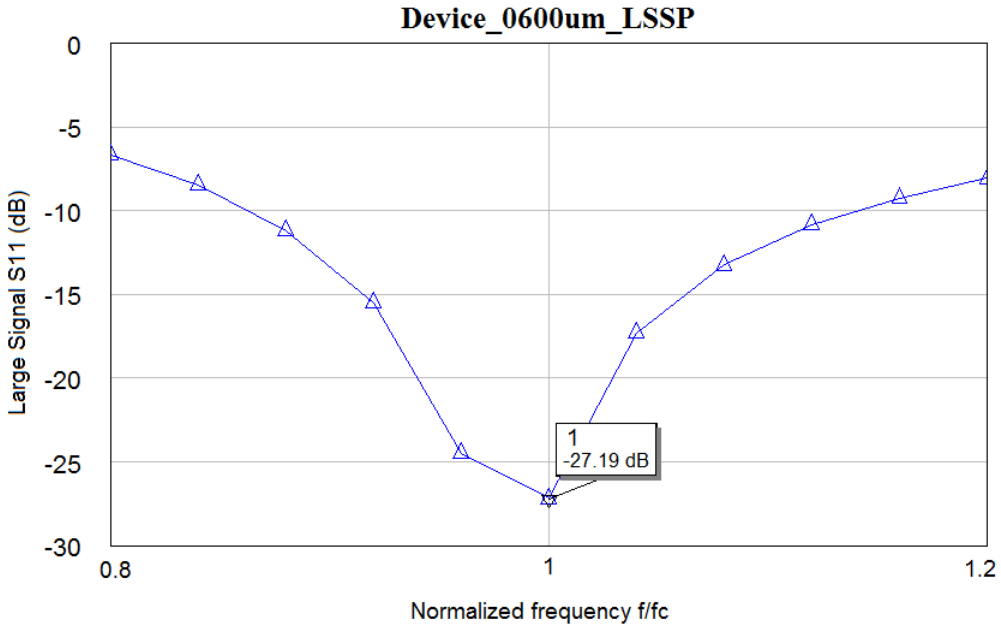

Figure 6.2: MMIC 2.5W power amplifier circuit large signal S11

As shown above in Figure 6.2, the single transistor power amplifier is well matched at the design frequency with a return loss of approximately 27 dB.

6.2 Microwave SPDT Switch

The simulated small signal performance of the designed microwave SPDT switch is shown below in Figure 6.3.

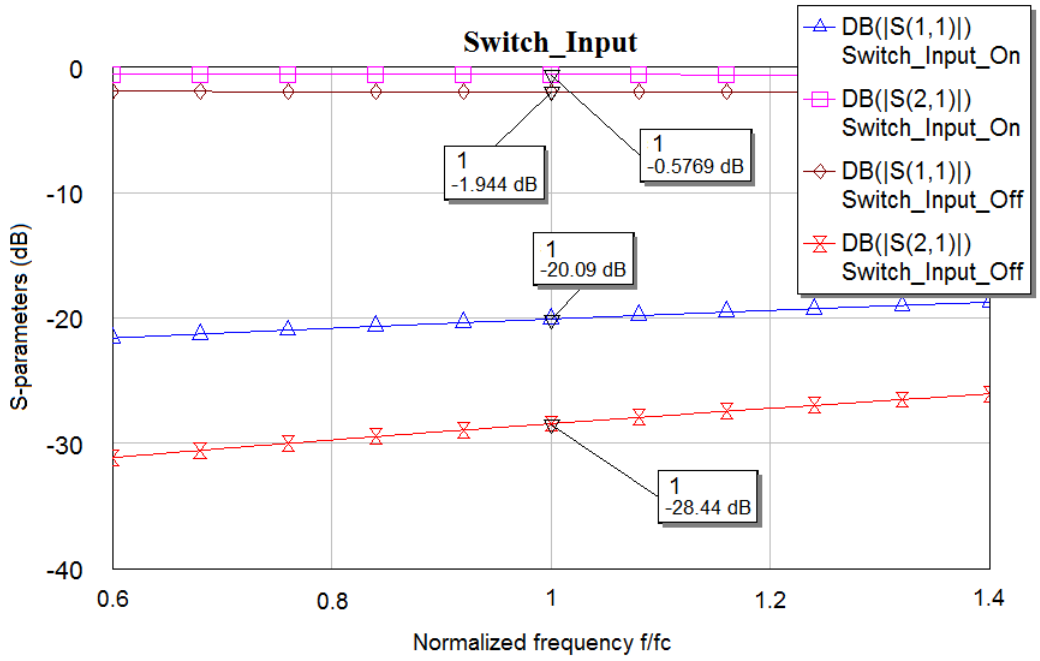

Figure 6.3: MMIC SPDT switch S-parameters

As shown above in Figure 6.3, the switch has an insertion loss of approximately 0.6 dB in the on state and approximately 28 dB of isolation in the off state. Additionally, the switch presents a return loss of approximately 20 dB in the on state.

6.3 Combined Impedance Selector

The simulated small signal performance of the combined output impedance selector in the 50 Ohm state is shown below in Figure 6.4.

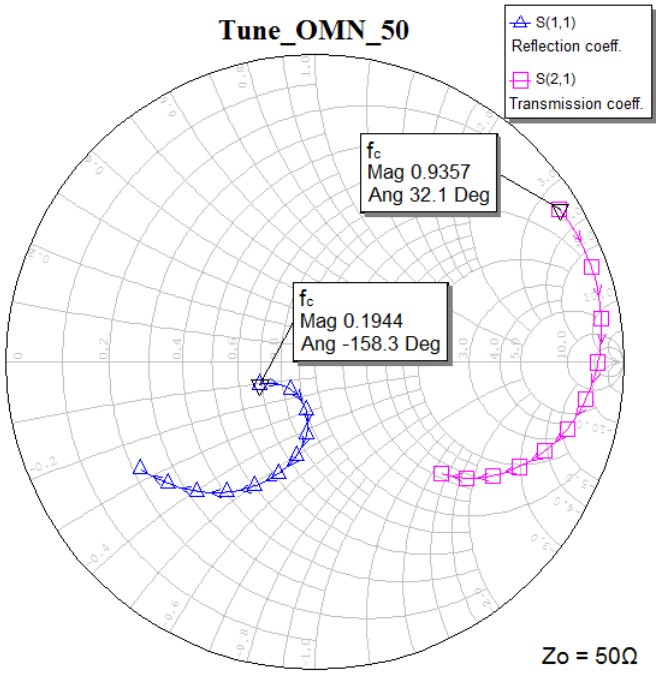

Figure 6.4: Combined output impedance selector 50 Ohm

As shown above in Figure 6.4, the output impedance selector circuitry presents a 50 Ohm match with a VSWR of less than 2:1.

The simulated small signal performance of the combined output impedance selector in the 25 Ohm state is shown below in Figure 6.5.

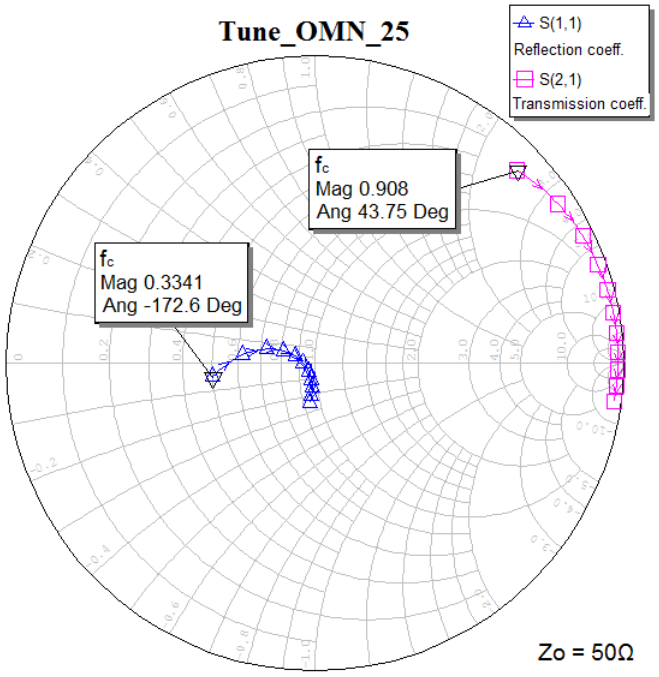

Figure 6.5: Combined output impedance selector 25 Ohm

As shown above in Figure 6.5, the output impedance selector circuitry presents a 25 Ohm match with a VSWR of less than 2:1.

The simulated small signal performance of the combined input impedance selector in the 50 Ohm state is shown below in Figure 6.6.

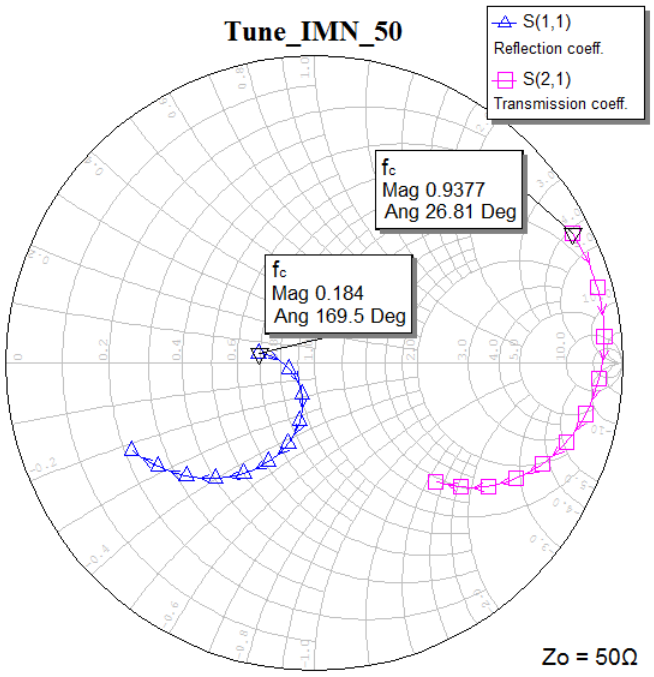

Figure 6.6: Combined input impedance selector 50 Ohm

As shown above in Figure 6.6, the input impedance selector circuitry presents a 50 Ohm match with a VSWR of less than 2:1.

The simulated small signal performance of the combined input impedance selector in the 25 Ohm state is shown below in Figure 6.7.

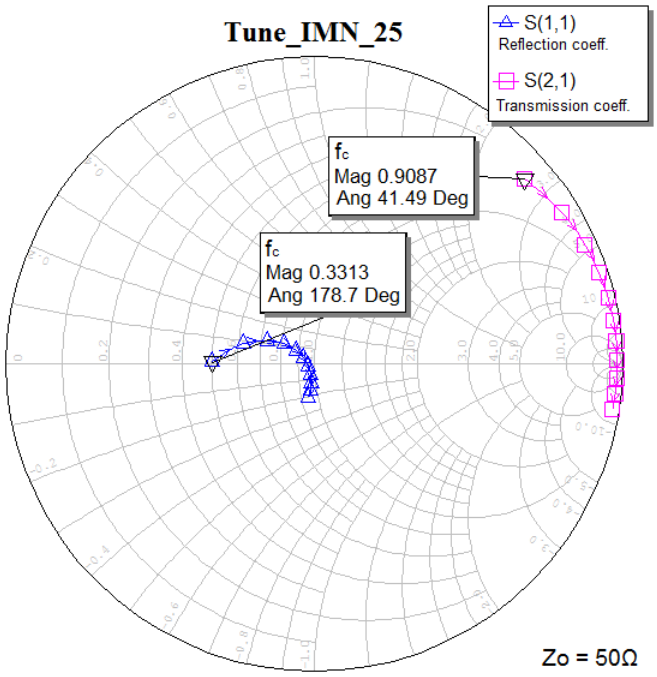

Figure 6.7: Combined input impedance selector 25 Ohm

As shown above in Figure 6.7, the input impedance selector circuitry presents a 25 Ohm match with a VSWR of less than 2:1.

6.4 Reconfigurable MMIC Power Amplifier - Single Device On

The simulated large signal performance of the reconfigurable MMIC power amplifier with a single power transistor active is shown below in Figure 6.8.

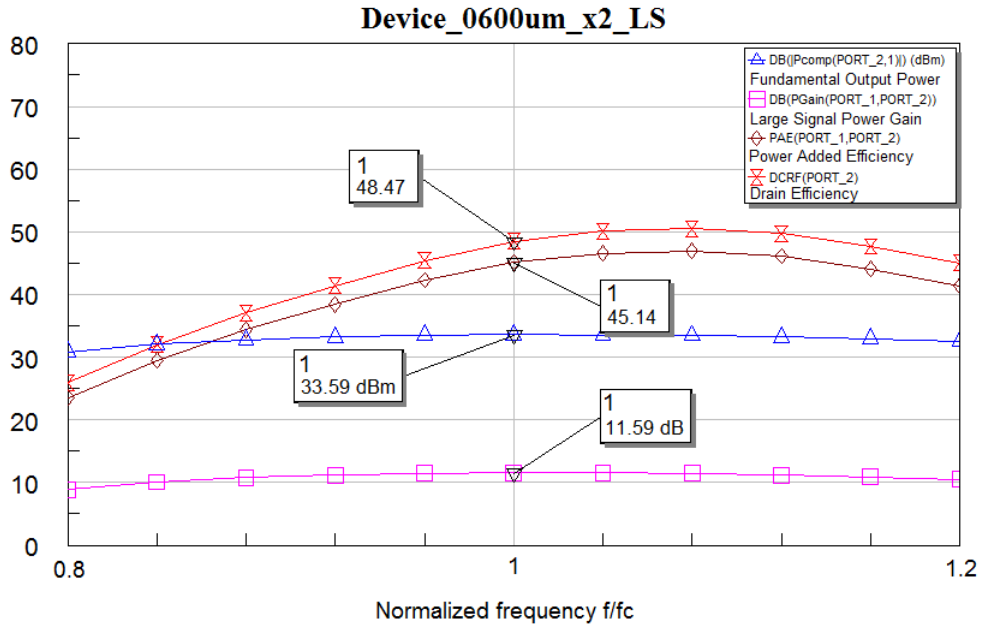

Figure 6.8: Reconfigurable MMIC power amplifier large signal performance

As shown above in Figure 6.8, the single operating device delivers an output power of approximately 2.5W with a power added efficiency of approximately 45% with a gain of 12 dB.

The simulated large signal input reflection coefficient of the single power transistor active is shown below in Figure 6.9.

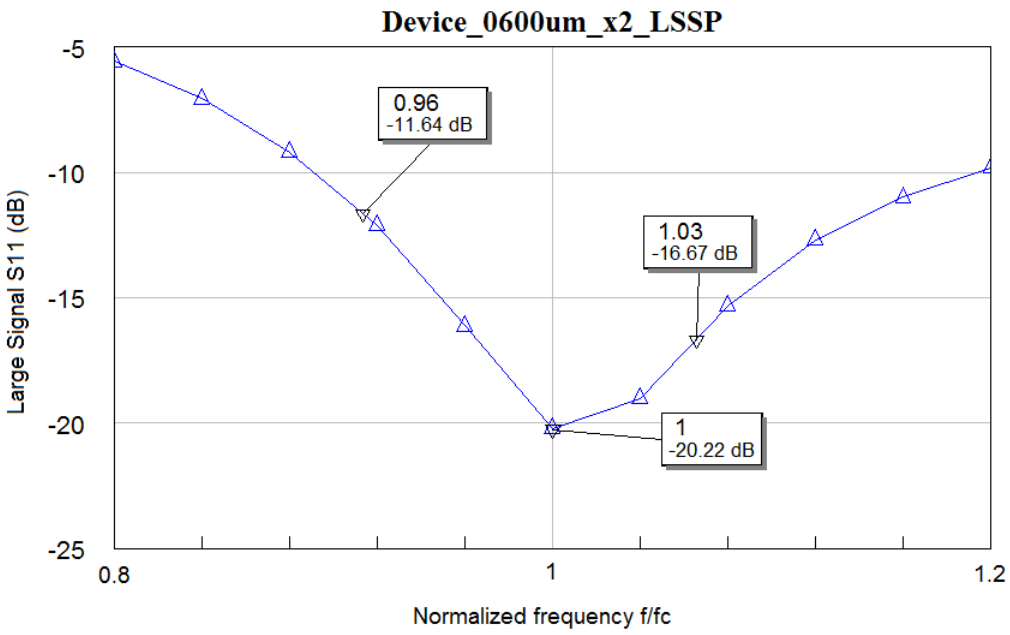

Figure 6.9: Reconfigurable MMIC power amplifier large signal S11

As shown above in Figure 6.9, the single power transistor active is well matched at the design frequency with a return loss of approximately 20 dB.

The simulated time domain voltage and current waveforms at the drain of a single transistor is shown below in Figure 6.10.

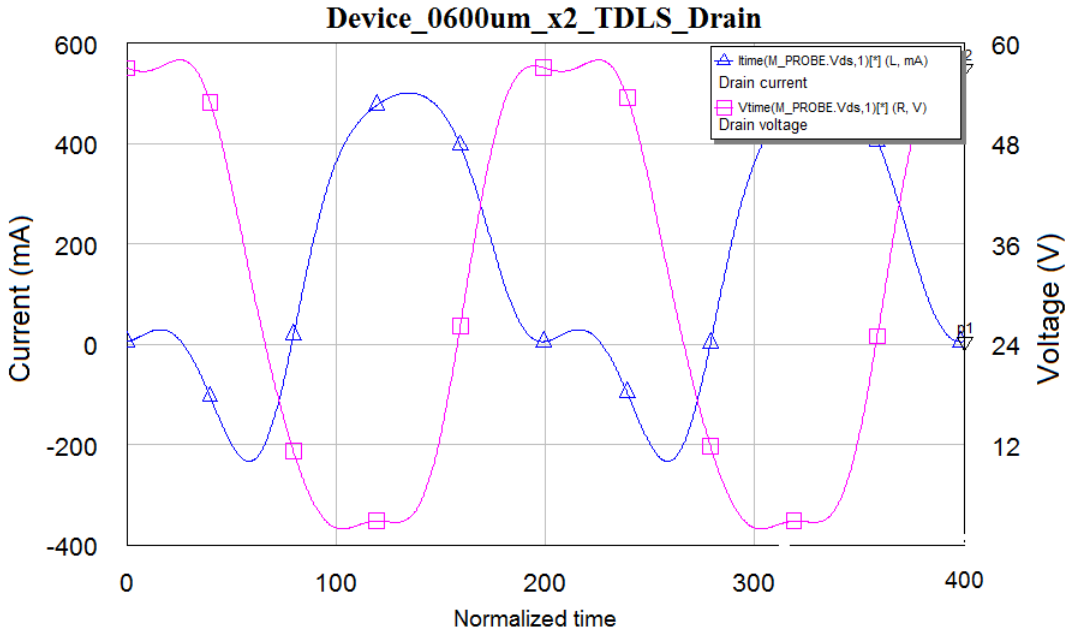

Figure 6.10: Reconfigurable MMIC power amplifier large signal voltage and current

As shown above in Figure 6.10, the voltage and current waveforms are approximately in quadrature with each other and resemble that of a low-pass filtered square-wave. The physical characteristics of the real transistor and lossy matching networks account for this less than ideal switching behavior that would have otherwise been expected from a class E mode power amplifier [13].

The simulated small signal performance of the reconfigurable MMIC power amplifier with a single power transistor active is shown below in Figure 6.11.

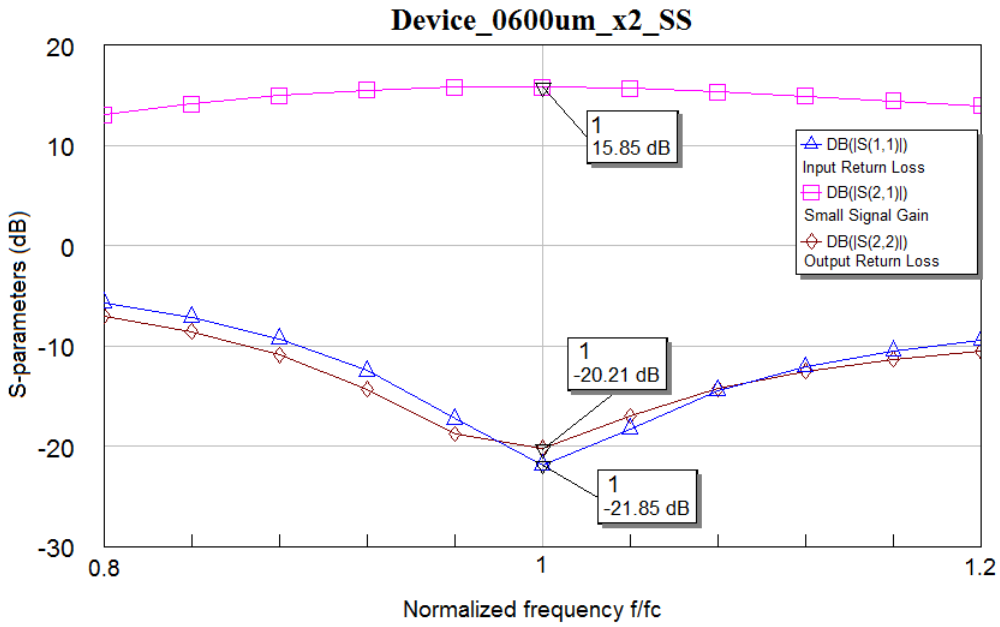

Figure 6.11: Reconfigurable MMIC power amplifier small signal performance

As shown above in Figure 6.11, the small signal gain of the reconfigurable MMIC power amplifier with one active device enabled is approximately 16 dB. Additionally, the input and output matching networks are well matched at the design frequency with a return loss of approximately 20 dB.

6.5 Reconfigurable MMIC Power Amplifier - Both Devices On

The simulated large signal performance of the reconfigurable MMIC power amplifier with both power transistors active is shown below in Figure 6.12.

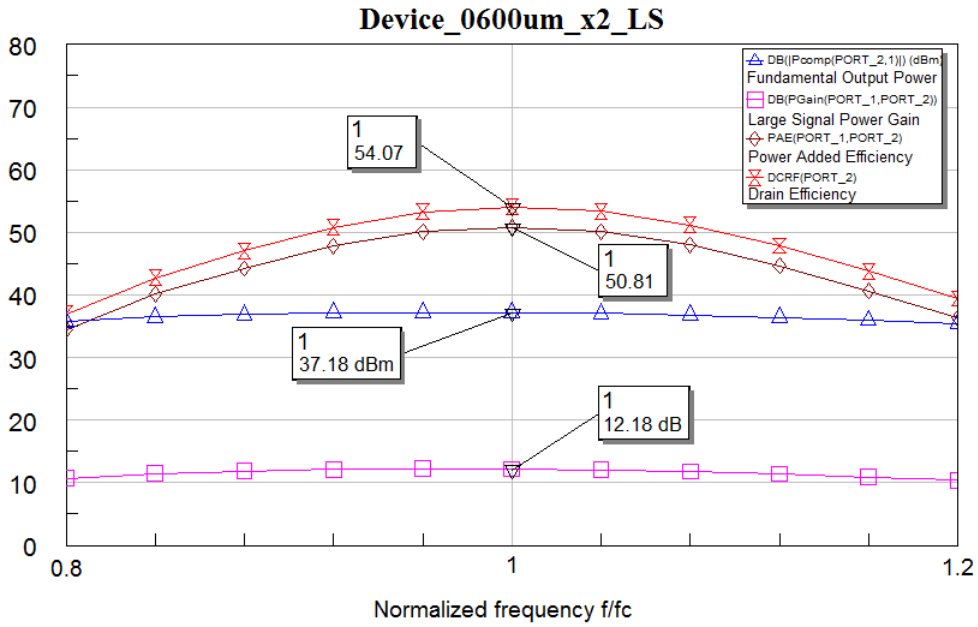

Figure 6.12: Reconfigurable MMIC power amplifier large signal performance

As shown above in Figure 6.12, both active devices deliver an output power of approximately 5W with a power added efficiency of approximately 50% with a gain of 12 dB.

The simulated large signal input reflection coefficient of both power transistors active is shown below in Figure 6.13.

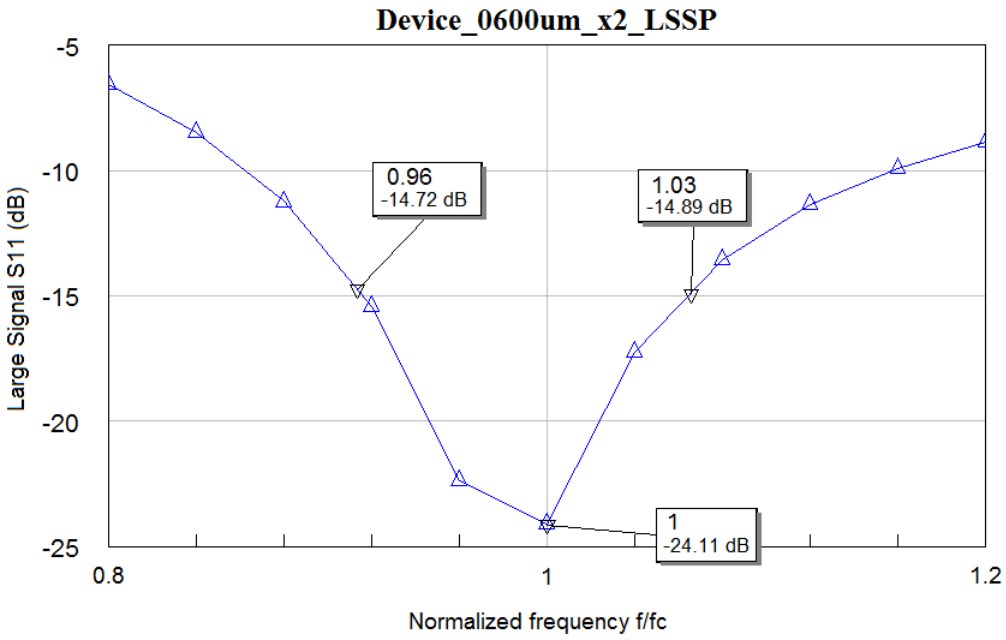

Figure 6.13: Reconfigurable MMIC power amplifier large signal S11

As shown above in Figure 6.13, the circuit is well matched at the design frequency when both power transistors are active with a return loss of approximately 24 dB.

The simulated time domain voltage and current waveforms at the drain of a single transistor is shown below in Figure 6.14.

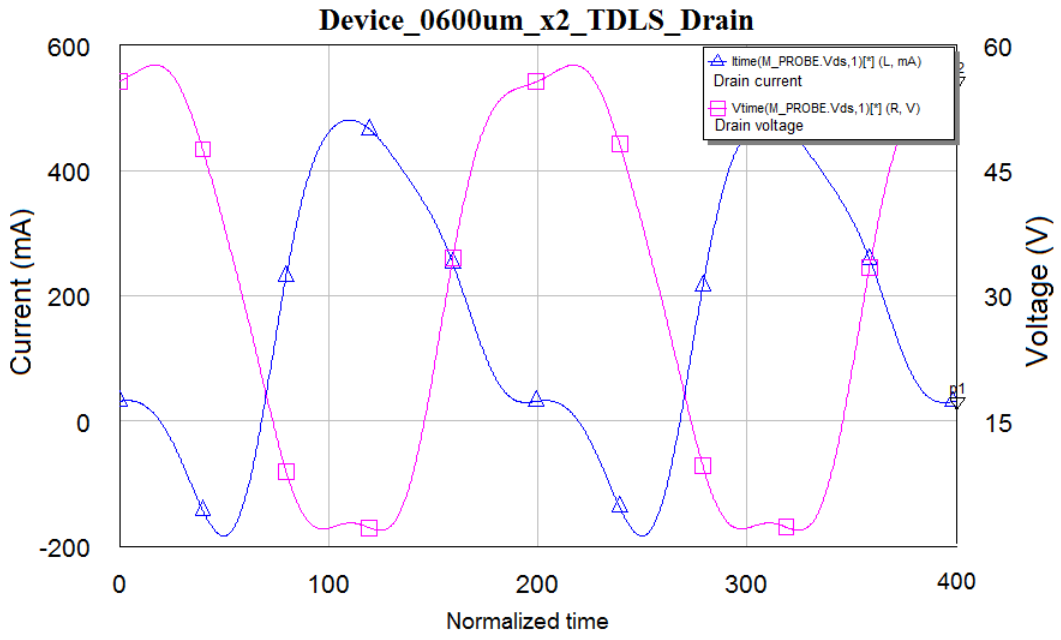

Figure 6.14: Reconfigurable MMIC power amplifier large signal voltage and current

As shown above in Figure 6.14, the voltage and current waveforms are approximately in quadrature with each other and resemble that of a low-pass filtered square-wave.

The simulated small signal performance of the reconfigurable MMIC power amplifier with both power transistors active is shown below in Figure 6.15.

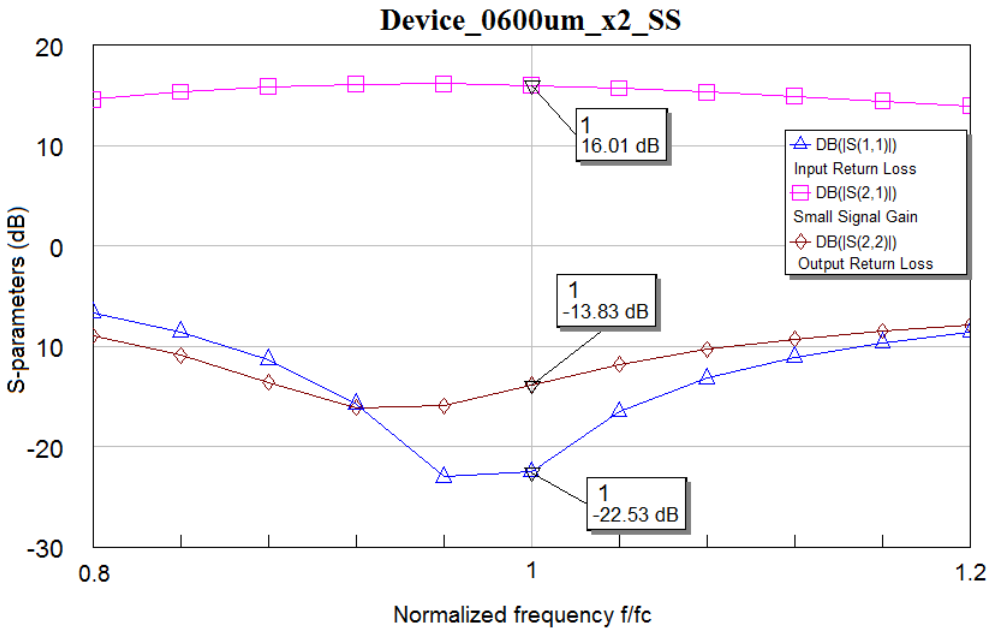

Figure 6.15: Reconfigurable MMIC power amplifier small signal performance

As shown above in Figure 6.15, the small signal gain of the reconfigurable MMIC power amplifier with both active devices enabled is approximately 16 dB. Additionally, the input and output matching networks are well matched at the design frequency with a return loss of approximately 20 dB and 14 dB, respectively.

The results of these simulations show that the output power of the amplifier does scale with the size and number of transistors utilized in the design. Additionally, the switch-combiner input and output network effectively provided isolates each device so that one can be turned off without adversely affecting the desired loading on a signal transistor as shown in Figures 6.10 and 6.14. The reduction in power added efficiency and output power in the parallel stage amplifiers when compared with their equivalent single stage amplifier is the result of the lossy spiral inductor matching

networks. A summary of the simulated performance obtained from the designed integrated GaN class E power amplifiers is shown below in Table 6.1.

Table 6.1: Integrated GaN Power Amplifier Summary

Device Size [mm]	Active Devices [#]	Power [W]	PAE [%]	Gain [dB]	Comments
0.6	1	2.67	62.63%	14.28	Fixed stage
0.6	1	2.28	45.14%	11.59	Reconfigurable
0.6	2	5.22	50.81%	12.18	Reconfigurable

CHAPTER VII

CONCLUSIONS AND RECOMMENDATIONS

7.1 Conclusions

The use of GaN as a viable replacement for GaAs and other traditionally utilized semiconductor materials in high power and high frequency applications continues to drive the development of novel circuit architectures capable of balancing the multitude of ever conflicting requirements placed on modern wireless systems. The academic and commercial sectors continue to redefine the cutting edge of solid state engineering as the proliferation of research in GaN based technology is a testament to its potential future. Not only does GaN satisfy high output power requirements, but it is permitting the use of circuitry such as the ideally 100% efficient switched class E mode power amplifier to operate well into the tens of gigahertz [4, 5]. While the demand for small footprint and high power amplifiers for applications involving radar, telemetry, and satellite communications is currently the primary force behind GaN research and development, it is only a matter of time before GaN makes a worldwide appearance in the commercial wireless industry. New technological developments such as enhancement-mode GaN FETs place the technology one step closer into the hands of the consumer [20]. As GaN foundry processes continue to improve, it can be expected to observe GaN power densities in excess of 30W/mm [21]. For the power amplifier designer, this opens the doors to a multitude of possible design choices such as incorporating a number of fixed power amplifiers for different operating bands to be integrated on a single chip or an architecture

capable of tuning across all bands of interest using electronically reconfigurable components while maintaining performance specifications such as output power and efficiency. Since GaN is capable of operating at very high voltages, microwave switches on the output of the power amplifier are feasible, meaning the flexibility of the input and output matching networks have significantly increased and are only restricted by the design specifications.

The hybrid packaging designs presented in this thesis show that it is possible to utilize a rapid PCB prototyping approach for high efficiency GaN based power amplifier design. As expected, the obtainable output power of each device is progressively doubled as the overall gate periphery is effectively doubled. However, it is shown that instead of doubling the transistor's individual size, if one is to create an amplifier with multiple devices in parallel, the same effect can be obtained with the added benefit of the inherent failover mechanism provided by the Wilkinson combiner network. While the Wilkinson power splitter/combiner was used in these designs, a balanced amplifier design can be implemented using quadrature couplers in place of the Wilkinson circuitry. The reconfigurable MMIC power amplifier design incorporates the use of high power switches to form a reactive SPDT-like input and output combiner network. When both amplifying devices are turned on, a traditional reactive combiner is formed. When one device is turned off, the switches provide isolation between the parallel branches in order to maintain the desired class E loading on each transistor. It is shown that this approach allows the output power to scale by a factor of two while maintaining approximately the same power added efficiency and large signal gain in each case. The addition of the tunable matching circuitry is necessary to fix the impedance mismatch at the combined ports based on the state of the amplifier; 25 Ohms to 50 Ohms when both amplifiers are operating and an approximate 50 Ohm pass-through when only one amplifier is operational. Like the hybrid approach, this design has the added benefit of an inherent failover mechanism as well as providing isolation when one device is turned off.

The hybrid and MMIC approach both have their advantages and disadvantages. For the class E mode, it is necessary to present the correct harmonic terminations to the transistor in order to obtain a reasonable efficiency and output power. These harmonic terminations are difficult to accurately realize and their performance is narrow-band by nature. In the hybrid design, the fundamental and harmonic terminations are realized using open circuited microstrip stubs that form the fully distributed matching networks; however, the die and bond wire parasitics become part of the match and their effect is difficult to predict without the use of an accurate nonlinear model. Likewise, tuning the parasitic drain to source capacitance of the packaged device is unobtainable after the introduction of the bond wire. For the MMIC approach, the matching networks are realized using spiral inductors and MIM capacitors. The low quality factor of these components present challenges at the second and third harmonics, especially the spiral inductors that require wider traces to handle the higher output power of the device. This results in lossy matching networks and therefore less than desired power added efficiency. In both cases, the power scalability of single and parallel transistors is readily observable.

7.2 Recommendations

All of the amplifier circuits presented in this thesis are designed to operate at the same fixed frequency; however, the need for wideband operation is also frequently desired. The techniques used to accomplish this goal are fundamentally similar to the integrated reconfigurable power matching technique presented in this thesis. After all, filter design, broad-banding, phase and impedance matching are all different views of the same theory. With the incorporation of frequency agile matching networks utilizing switches or varactors, one is able to realize the potential possibilities of a fully integrated and reconfigurable GaN based power amplifier. Additionally, future work involving the integration of frequency agile matching networks is possible using the power scaling architecture presented in this thesis. However, the current integrated design approach can be used

for applications that require the ability to adjust the final output power while maintaining high efficiency operation for frequency or phase modulated signals. By selecting an appropriately sized device for the lowest output power and then scaling up with additional parallel devices to obtain the highest desired output power, a design capable of device level control can form a robust RF front-end for any software defined and multipurpose wireless system.

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