A SELF-SUSTAINED MINIATURIZED MICROFLUIDIC-CMOS PLATFORM FOR BROADBAND DIELECTRIC SPECTROSCOPY

by

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for any proprietary material contained therein.

This dissertation is dedicated to
my parents and my love
for their love, patience and support

MAHIN SORORIAN, HESHMAT BAKHSHIANI

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A Self-Sustained Miniaturized Microfluidic-CMOS Platform for Broadband Dielectric Spectroscopy

Abstract

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This project has developed two integrated microsystems fabricated in a 0.35-µm two-poly four-metal RF CMOS process for miniaturized broadband dielectric spectroscopy. In particular, first, a broadband sensor interface IC as part of a miniaturized measurement platform for MHz-to-GHz dielectric spectroscopy has been developed. The IC measures frequency-dependent S21 magnitude and phase of a microfluidic dielectric sensor fabricated in a thick gold-on-glass microfabrication process and loaded with a material-under-test (MUT). The sensor interfaced with the IC is fully capable of differentiating among deionized (DI) water, phosphate buffered saline (PBS), ethanol and methanol in tests conducted at four different excitation frequencies of 50 MHz, 500 MHz, 1 GHz and 3 GHz. Further, dielectric readings of ethanol from the sensor interfaced with the IC at five excitation frequencies in the range of 50 MHz to 2 GHz are in excellent agreement (error < 1%) with those from using a vector network analyzer (VNA) as the sensor readout.

Next, a self-sustained, miniaturized, microfluidic-CMOS platform for palmtop dielectric spectroscopy has been developed. The platform incorporates a parallel-plate capacitive sensor with a three-dimensional gap, floating electrode, and microfluidic channel for sample delivery, as well as a fully integrated transceiver for broadband dielectric spectroscopy. The IC applies a single-tone sinusoidal RF excitation signal in a frequency range of ~ 9MHz to 2.433GHz to the MUT-loaded sensor, and measures the sensor transmission characteristics in the voltage domain via an amplitude/phase measurement utilizing broadband frequency response analysis (bFRA) to extract the MUT complex permittivity with microliter sample volumes. Complex dielectric readings of PBS from the platform at six excitation frequencies in the range of 50 MHz to 2.4 GHz are in excellent agreement (RMS error <1.5% for 0.5 to 2.4 GHz) with those from a reference measurement by an Agilent 85070E dielectric probe kit interfaced with a VNA.

Finally, an autonomous self-sustained palmtop platform, incorporating the microfluidic-CMOS platform, ADC, power supply unit, Wi-Fi module, and a Raspberry Pi computing module has been developed. The palmtop platform is capable of accurately measuring the real and imaginary parts of MUT complex permittivity from ~ 9MHz to 2.433GHz in less than 5s, enabling rapid, high-throughput, and low-cost measurements with a self-sustained, portable platform that can pave the way for translating dielectric spectroscopy from the lab bench to the field or the bedside.

Chapter 1

Introduction

1.1 Motivation

Quantitative measurement of the complex dielectric permittivity of a material versus frequency (i.e., dielectric spectroscopy, or DS) is a powerful monitoring technique [1.1] that extracts key information on molecular characteristics of the material-under-test (MUT) via its interactions with electromagnetic waves in a broad frequency range. DS is used as a label-free, nondestructive, real-time and fully electrical monitoring modality for myriad applications including chemical analysis of oil in the petroleum industry [1.2]-[1.3], soil moisture monitoring in agriculture [1.4]-[1.5], fermentation monitoring during the production of alcoholic beverages [1.6], food quality/safety monitoring [1.7] and drug development in the pharmaceutical industry [1.8]. DS is also used in the biomedical field as to study the interaction of radio-frequency (RF)/microwave electromagnetic waves with biological or biochemical samples requiring minimal sample preparation [1.9].

In the late 20th century, the interaction of biological samples with electromagnetic waves has been investigated by Schwan [1.10]-[1.11] demonstrating the frequency-dependent behavior which translates into relaxations of the complex relative permittivity. These dispersion regions are related to the different polarization phenomena as described in Fig 1.1. The first dispersion region, named α dispersion occurring in Hz – kHz frequency range, is associated with ionic relaxation. The β dispersion in MHz frequency range is related to polarization of the cellular membrane with the capacitive cell membrane charging as well as the dipole polarization. By increasing the frequency to δ dispersion region, the capacitive barrier of the cell membrane will be crossed and waves will penetrate into the cells leading to the enhanced interaction of electromagnetic waves with biological matter due to the dipole polarization and molecular reorientation dynamics. Further increase in frequency to several GHz –THz (γ dispersion) would lead to atomic polarization which is observed when the nucleus of the atom reorients in response to the electric field. Fig 1.1 also shows the frequency bands of dielectric dispersion for various biomaterials. In general, larger molecules such as DNA or RNA exhibit their relaxation characteristics at excitation frequencies in Hz-to-kHz range (α-dispersion), whereas smaller molecules such as proteins, lipids or amino acids exhibit their response at higher frequencies in MHz-to-GHz range within β, δ and γ dispersion regions. Above ~10 GHz, the response is primarily dominated by the relaxation characteristics of free water molecules.

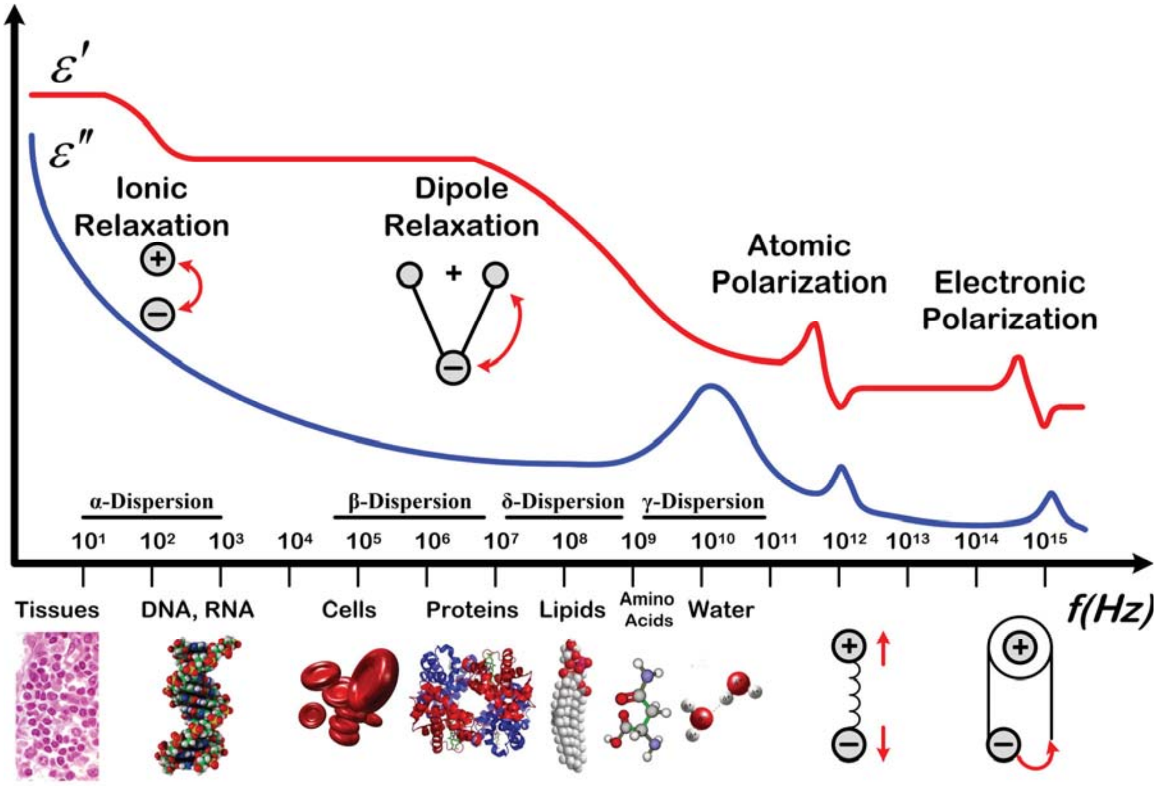

Figure 1.1: The conceptual illustration of relative dielectric constant versus the frequency with related polarization mechanisms in biological matter along with frequency bands of dielectric dispersion for biomaterials.

The relaxation characteristics of various biomaterials such as human blood [1.12], spinal fluid [1.13], breast tissue [1.14] and skin [1.15], [1.16] have been studied using DS for applications in disease detection and clinical diagnosis. In particular, DS coupled with optical reflection has been used for noninvasive glucose monitoring in Type I diabetic patients [1.17], [1.18]. DS is also a powerful tool in proteomics for the study of molecular dynamics and protein interactions such as the hinge-bending motion of immunoglobulin G [1.19], dynamical processes of the water-protein interface for ribonuclease A [1.20] and dipole moment as well as hydrodynamic radius of avidin and biotin-bound avidin [1.21]. Nonetheless, DS is still largely under-investigated as an analytical tool in scientific research or clinical settings due to the dearth of an autonomous, small-sized, low-power and portable instrument that is conducive to conducting rapid, high-throughput and low-cost measurements. The ultimate goal in this work is hence to realize a miniature, autonomous, integrated measurement platform capable of rapidly capturing the dielectric relaxation characteristics of biomolecules of an aqueous solution in a wide frequency range from MHz to GHz with applications ranging from proteomics for high-throughput study of protein structure and function to measurements of receptor-ligand interactions in drug screening, changes in membrane protein configuration during cell signaling or macro-level study of the whole blood permittivity with application in blood coagulation studies.

1.2 Commercial DS Instruments and Techniques

Fig 1.2 shows the different techniques and commercial instruments that perform broadband dielectric spectroscopy over different frequency ranges from 10^{-6} to 10^{15} Hz. Time domain dielectric spectroscopy (TDDS) is a dominant technique for low frequency range dielectric spectroscopy (10^{-6} to 10^{3} Hz). TDDS is based on transmission line theory in the time domain [1.22]. A rapidly increasing voltage step is applied to the line and recorded, along with the reflected voltage, returned from the sample and delayed by the cable propagation time. As long as the line is homogeneous the shape of this pulse will not change. But, in the case of heterogeneity in the line (the inserted sample) signal is partly reflected from the air-sample interface and partly passes through it. Dielectric measurements are made along a coaxial transmission line with the sample mounted in a sample cell that terminates the line. The advantage of this technique is that the entire frequency spectrum is captured at once, thus it is fast and eliminates drift and distortion between frequencies. However, this technique requires a high resolution ADC that can sample at least at the Nyquist rate of the targeted DS bandwidth. Thus, this technique is usually limited to the low frequencies (<MHz) which realization of the required ADC is practical. Frequency response analysis (FRA) and auto balance bridges are two other methods conventionally used for the low frequency DS measurements (<100MHz). These methods perform the measurement at single frequencies. As a result, performing dielectric spectroscopy over a wide frequency range requires frequency sweep by the measurement system which could potentially takes more time compared to TDDS.

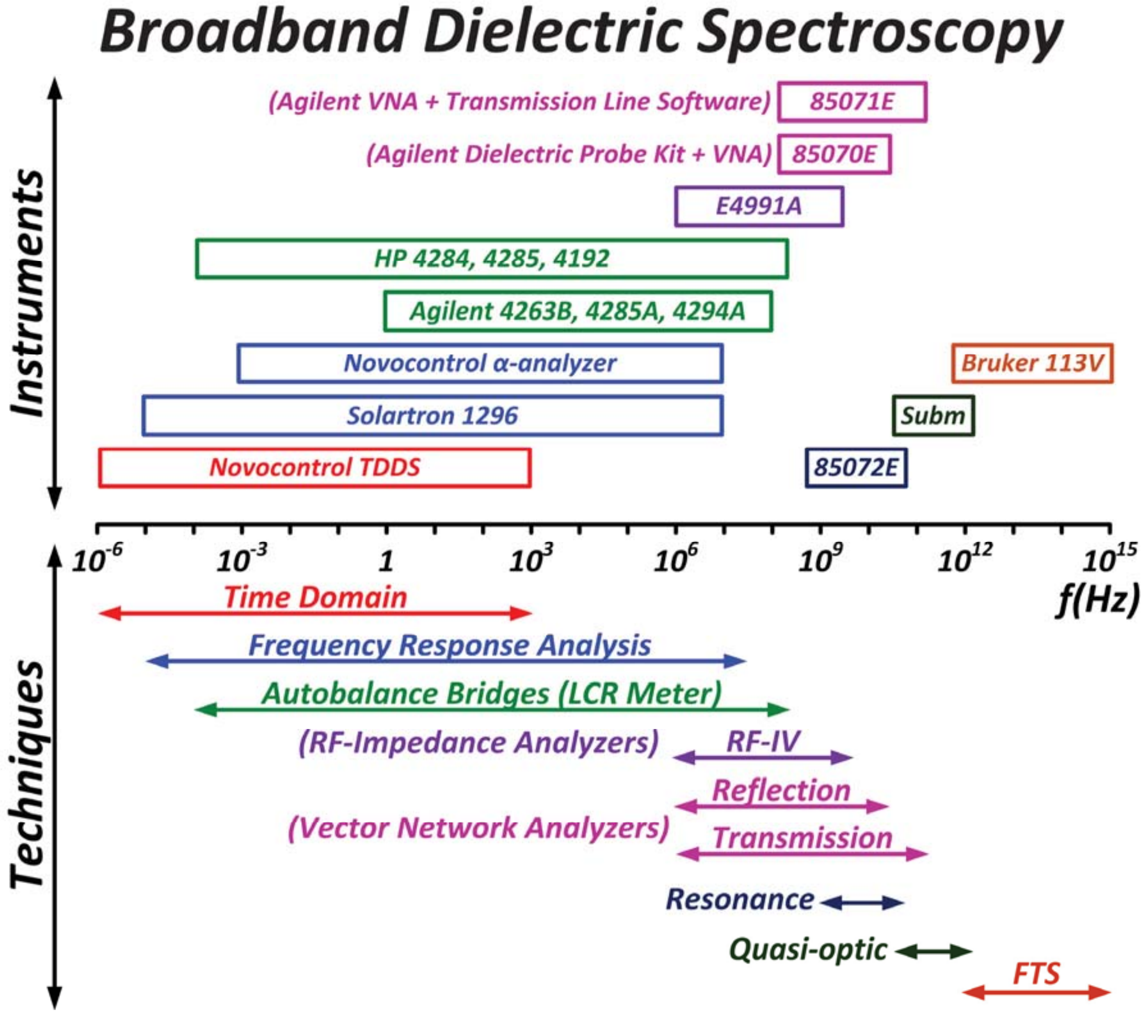

Figure 1.2: Commercially available instruments and techniques for broadband dielectric spectroscopy.

Conventionally in MHz – GHz frequency range, bench-top instruments including commercially available dielectric probes (e.g., *Agilent* 85070E dielectric probe kit) that are interfaced with a vector network analyzer (VNA) are used. These bench-top measurement setups measure the MUT permittivity based on different techniques including resonance (e.g., *Agilent* 85072E), transmission (e.g., *Agilent* 85071E), or reflection (e.g., *Agilent* 85070E) technique. In resonant technique, MUT sample affects the center frequency (f) and quality factor (Q) of the resonant cavity which is a high Q structures that resonate at certain frequencies. From the measured f and Q parameters, the complex permittivity (ε_r) of the material can be calculated at a single frequency. As shown in Fig 1.3, the transmission technique involves placing the MUT sample inside a portion of an enclosed transmission line which is usually a section of rectangular waveguide or coaxial airline. Then the transmitted signal (S_{21}) is measured by the VNA and the designated software extracts the permittivity from the S_{21} measurement. In the reflection technique, the MUT permittivity is measured by immersing the probe into the MUT sample. The fields at the probe end fringe into the material and change as they come into contact with the MUT. The reflected signal (S_{11}) then can be measured by the VNA and related to ε_r by the probe kit software runs on a home-based computer as shown in Figure 3. These bench-top measurement setups achieve a very wide bandwidth from MHz to 10’s of GHz. However, they are often bulky and expensive. Further, they require a large sample volume on the order of 10’s to 100’s of mL. Thus is not suitable for most DS applications that require extremely small sample volumes on the order of μL or less. Therefore, development of a low-power, portable, miniaturized, and self-sustained platform with μL sample volume for conducting DS measurements to replace the conventional expensive, bulky benchtop equipment is highly motivated and can ultimately pave the way for translating DS measurements from the lab bench to the field or to the bedside.

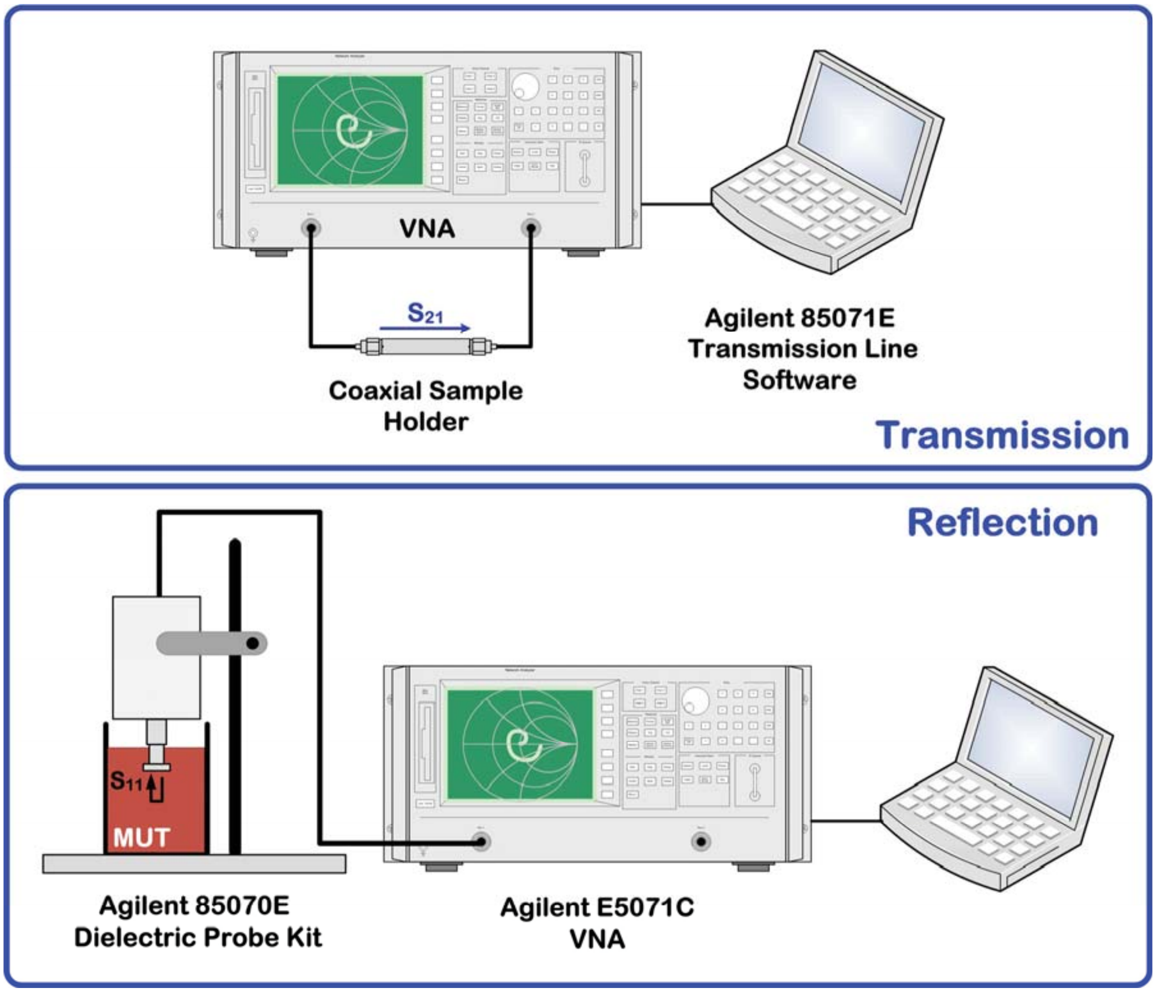

Figure 1.3: Commercially available DS setup for MHz-GHz dielectric spectroscopy.

1.3 Previous Work

Recent advances in integrated microsystem technology for biomolecular detection have paved the way for the development of such sensing instruments based on the miniaturization of the measurement platform in a single-chip CMOS IC. Specifically, the nuclear magnetic resonance (NMR) platform has been miniaturized by integrating the RF generator and receiver on a single chip [1.23], [1.24] and later by integrating the detection coil with the RF transceiver on a single chip to create a truly hand-held instrument [1.25] that achieves 150× more spin-mass sensitivity and >1,000× reduction in volume and weight compared to state-of-the art commercial benchtop systems. Another such example is a CMOS electrochemical impedance spectroscopy (EIS) microarray with an operation frequency range up to 10 kHz [1.26] or 50 MHz [1.27] developed to detect a small impedance change when a target protein binds to a functionalized on-chip electrode. Other examples include a CMOS IC-based magnetic-relaxation detector for micro-bead labels [1.28], CMOS IC-based platforms for DNA analysis [1.29]-[1.31] and a lab-on-chip (LOC) for bioluminescence detection [1.32].

However, despite the broad range of applications for DS and the recent advances in integrated microsystem technology, there has been little effort focused on developing a standalone microsystem dedicated to DS studies in the past. First efforts on miniaturizing DS systems focused on developing miniaturized DS sensors by combining a coplanar waveguide (CPW) and a microfluidic channel for delivery of the MUT [1.33]-[1.37]. As compared to commercial DS systems requiring bulk-solution measurements, these sensors need only a small liquid volume (µL to nL) confined to their microfluidic channel. However, they still require an expensive microwave probe station to contact the sensor at the wafer level and a bulky benchtop vector network analyzer (VNA) to perform two-port S-parameter measurements for dielectric extraction.

More recently, there has been several works focused on developing a standalone miniaturized platform for dielectric spectroscopy to enable low-cost, integrated platforms that can operate on aqueous samples in the microliter range [1.38]-[1.48].These works are mainly based on two different methods. The first method is based upon measuring the oscillation frequency shift caused by the MUT, when the MUT-loaded sensor acts as a capacitive element in a sensing VCO [1.40]-[1.44]. In [1.41], Helmy and colleagues have reported one of the first miniaturized DS systems that incorporates an on-chip interdigitated capacitor in the LC tank of a VCO placed within a synthesizer loop as shown in Fig 1.4. Due to the limited tuning range of the LC VCO, this work is only suitable for GHz-range operation (7–9GHz). Furthermore, it can only measure the real part of complex permittivity of the MUT.

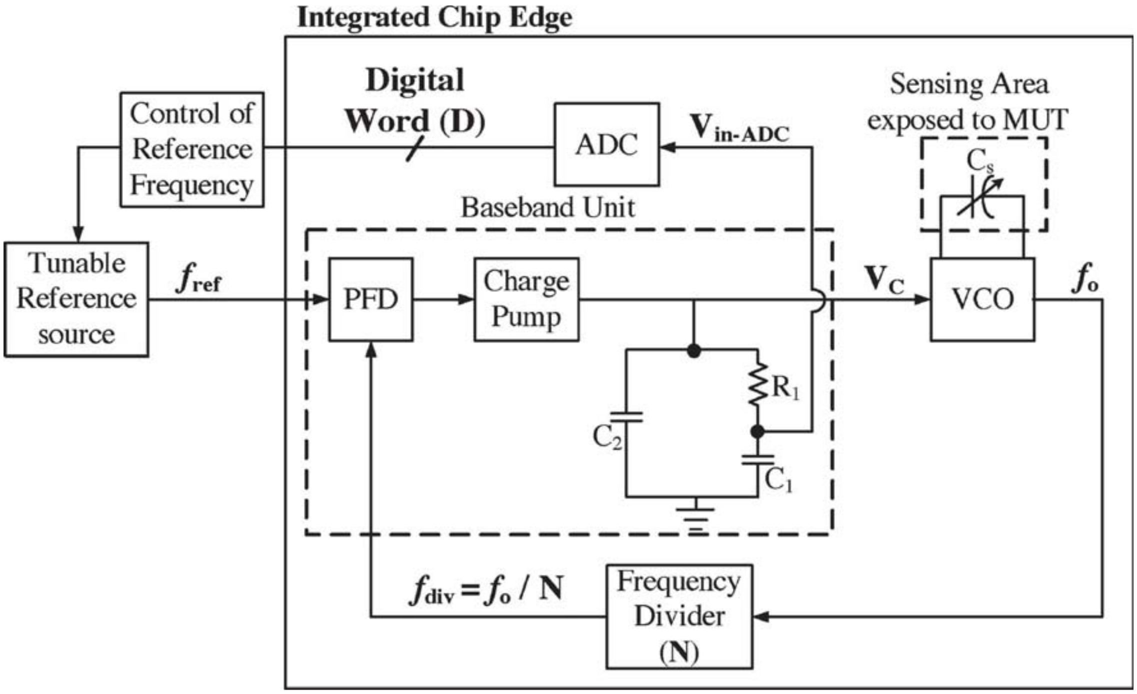

Figure 1.4: Block diagram of the dielectric sensor basic read-out circuitry based on a frequency synthesizer loop and an ADC [1.41].

More recently in [1.43], Elhadidy has combined the oscillation-frequency-shift method with an amplitude-locked loop circuit in order to measure both real and imaginary parts of MUT permittivity, using a 3-stage ring-oscillator-based VCO as shown in Fig 1.5. A wider tuning range for the ring VCO allows an operation frequency from 700MHz to 6GHz in this work. However, at the same time, the higher phase noise of the ring VCO requires a 300ms measurement time at each operation frequency point for averaging in order to reduce the error induced by phase noise of the VCO. Moreover, the operation frequency range is MUT dependent in a way that the maximum frequency is limited by the maximum VCO/PLL operating frequency with highest MUT permittivity (e.g., Water) and the minimum frequency is limited by the minimum VCO/PLL operating frequency of the VCO/PLL with lowest MUT permittivity (e.g., Air).

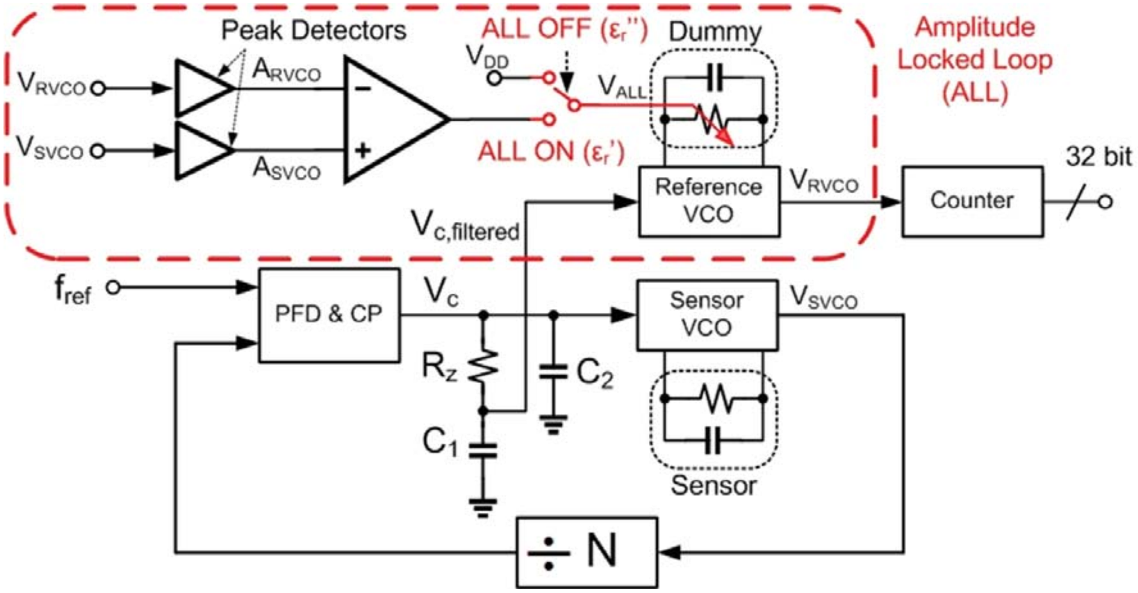

Figure 1.5: Block diagram of the broadband PLL-based complex dielectric spectroscopy system [1.43].

The second method utilized by miniaturized DS systems is based upon measuring the amplitude and phase of a single-tone sinusoidal RF excitation signal after it is transmitted through the MUT-loaded sensor [1.46]-[1.48] as shown in Fig 1.6. In [1.47] – [1.48], integration of on-chip sensors and RF receiver front-ends is achieved to enable both real and imaginary permittivity detection over 1 – 50GHz, and 620MHz – 10GHz frequency range, respectively. However, utilization of zero-IF receiver in [1.48], decreased the system resolution because of the inherent harmonic and low frequency noises problem in zero-IF architecture. In addition, neither work is self-sustained as they require external signal generation for LO and RF signals with bulky benchtop equipment.

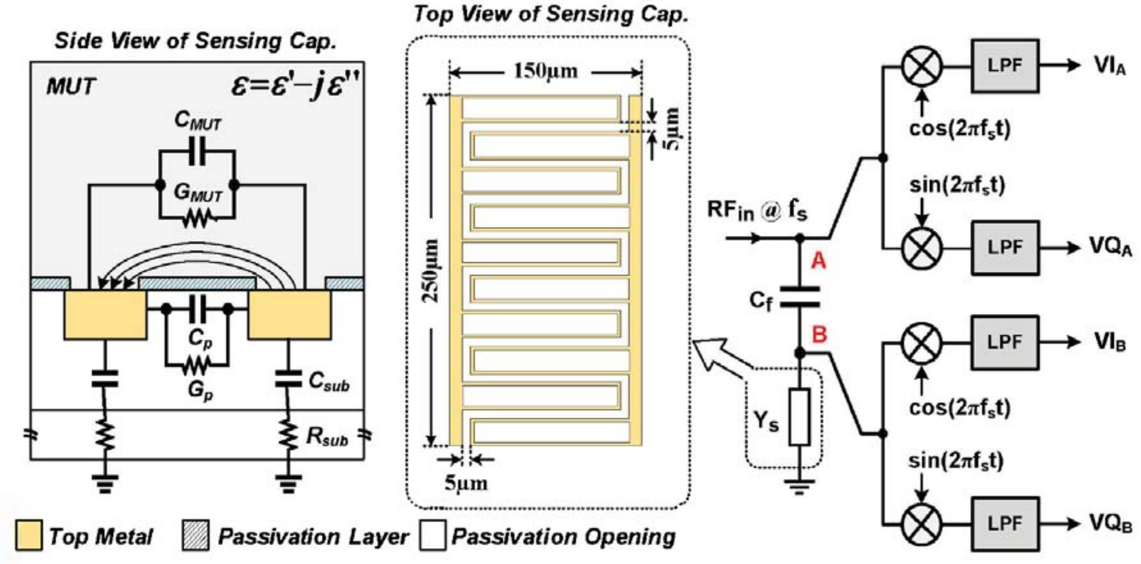

Figure 1.6: Sensing capacitor and a conceptual block diagram of the complex dielectric spectroscopy system based on amplitude/phase measurement [1.48].

1.4 Proposed Research

The ultimate goal of this Ph.D. research work is hence to realize a self-sustained miniaturized, autonomous, palmtop platform capable of rapidly capturing the dielectric relaxation characteristics of material under test (MUT) in a wide frequency range from MHz to GHz. The palmtop DS platform will incorporate a parallel-plate capacitive sensor with a three dimensional gap, floating electrode, and microfluidic channel for sample delivery, as well as a fully integrated transceiver IC as conceptually shown in Fig 1.7.

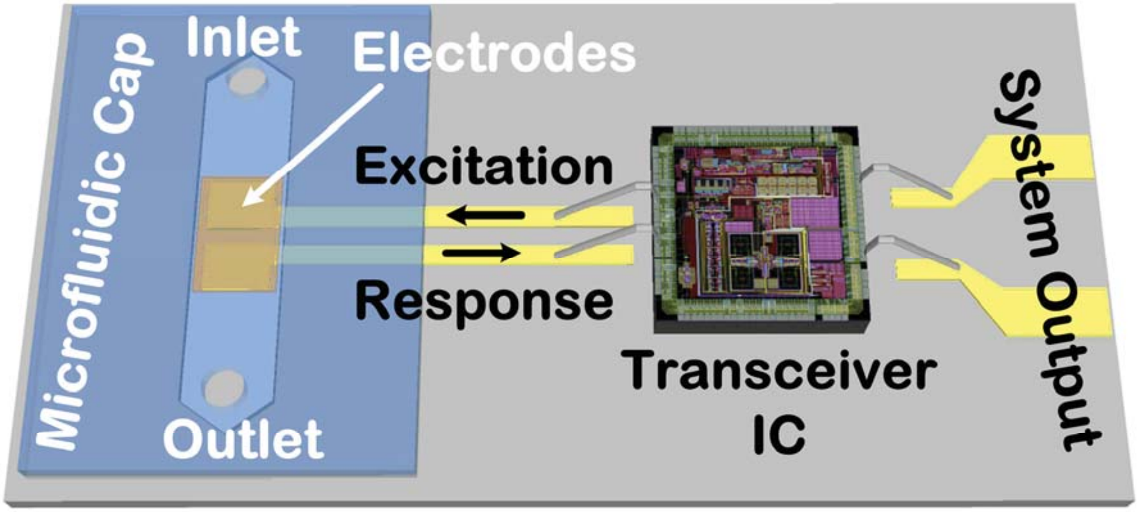

Figure 1.7: Conceptual illustration of a miniaturized measurement platform for dielectric spectroscopy.

In particular, in the first phase, a Gen-1 sensor interface IC (Receiver IC) is developed for measuring the wideband transmission characteristic of the MUT-loaded sensor in the voltage domain, employing a broadband frequency response analysis (bFRA) method [1.49]-[1.51]. In this phase, the IC is interfaced with Gen-1 microfluidic dielectric sensor [1.52] in order to measure the real part of complex permittivity of different organic chemicals. The micro fabricated sensor architecture is based on a micro strip line with a centered gap as its parallel-plate capacitive sensing area. The Gen-1 interface IC only has readout capability and does not provide the sensor excitation signal. Therefore it is not yet self-sustained as it needs two benchtop signal generators to generate the required RF and LO signals.

Next, in the second phase, a fully integrated transceiver IC [1.53] is developed incorporating a receiver (RX), which utilizes broadband frequency response analysis method as well as a transmitter (TX) to generate the RF excitation signal for the sensor, and the LO signals for the RX in MHz-GHz frequency range in order to enable a self-sustained operation for platform portability. In this phase, the transceiver IC is interfaced with Gen-2 microfluidic DS sensor in order to measure both the real and imaginary part of complex permittivity of the MUT. The proposed sensor is based on a parallel-plate capacitive structure with a floating electrode integrated into a microfluidic cap that delivers the MUT to the sensing area [1.54].

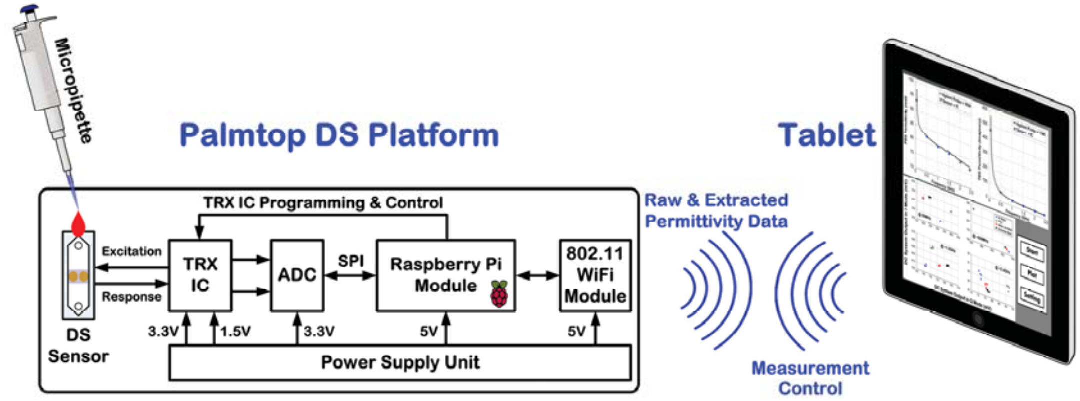

Figure 1.8: Illustration of palmtop dielectric spectroscopy (DS) platform architecture along with its measurement setup.

Finally, as shown in Fig1.8, in the third phase, the palmtop DS platform is developed in order to enable rapid, high-throughput, and low-cost measurements. In this truly portable system that is small enough to fit on the palm of a hand, a Raspberry Pi module is interfaced with the transceiver IC as a low-cost embedded computing platform to run the sensor calibration algorithm online, wirelessly connect with a handheld tablet to transfer the data for plotting and storage, as well as wirelessly program the transceiver IC from the tablet. In particular, this capability facilitates an automated frequency sweep from MHz to GHz, resulting in a short measurement time (<5 seconds) for the entire frequency range. In this phase, a python program is developed to automatically program the transceiver IC for each excitation frequency, capture the data from the commercial

ADC via SPI port, run the sensor calibration algorithm to extract the MUT's real and imaginary permittivity information from the IC measurement and plot the extracted permittivity information on the tablet. Table 1.1 summarizes target performance metrics and for the proposed miniaturized platform in this research.

The remainder of this thesis presents a detailed report on the design, development, and performance characterization of these platforms as organized in the following chapters:

- Chapter 2 presents the Gen-1 sensor interface IC (RX only) for miniaturized dielectric spectroscopy. The system and circuit design procedure for MHz-GHz miniaturized DS platform is described and measured results from benchtop electrical characterization, and from experiments with *Gen-1 Sensor + IC* are presented.
- Chapter 3 reports the Gen-2 sensor interface IC (fully integrated TRX IC) developed for palmtop dielectric spectroscopy platform. The detailed transmitter system and circuit design is described and measured results from benchtop electrical characterization, and from experiments with Gen-2 Sensor + IC are presented.
- Chapter 4 Presents the palmtop DS platform developed for MHz-GHz dielectric spectroscopy. The detail hardware design procedure as well as DS measurement/calibration algorithm implementation is described. Finally, measured result from experiments with different MUT samples performed by palmtop platform is presented.

- Chapter 5 draws final conclusions and highlights the major contributions of this research, as well as identifies further research opportunities in this field.

Table 1.1: Summary of Target Performance Characteristics

TOTAL SYSTEM PERFORMANCE CHARACTERISTICS	
Functionality	Measurement of dielectric permittivity
Methodology	Amplitude/phase measurement
MUT Sample Volume	< 10µL
Power Supply	Analog: 1.5 V Digital: 3.3 V
Self-Sustainability	Yes
Operation Frequency	10MHz – 2.4GHz
Permittivity Type	ε_r' , ε_r''
RMS Permittivity Error	< 2%
Technology	AMS 0.35µm CMOS
Total Power Consumption	< 100 mW
RECEIVER (RX) CHARACTERISTICS	
Methodology	Broadband FRA
IF Frequency	1MHz
Minimum Detectable Signal	< -100 dBm
Peak SNR	> 75 dB
Power Consumption	< 10 mW
Scan Rate (14b resolution)	> 900 s^{-1}
Calibration Capability	Gain/Phase/Temperature
TRANSMITTER (TX) CHARACTERISTICS	
RF Excitation Frequency	10MHz – 2.4GHz
RF – LO Frequency Offset	1MHz
RF Excitation Frequency Resolution	32 MHz
LO Spur Rejection	> 50 dBc
LO Phase Noise (1MHz Offset Freq.)	< -105 dBc
RF Spur Rejection	> 35 dBc
Power Consumption	< 90 mW
Synthesizer Type	Integer-N with Constant Loop Gain
VCO Type	LC QVCO with constant K_{vco}
Other Functionality	RF Excitation Amplitude Tunability Autonomous Sweep Capability

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Chapter 2

Gen-1 Sensor Interface IC for MHz to GHz Dielectric Spectroscopy

This Chapter describes a broadband sensor interface IC as part of a miniaturized measurement platform for MHz-to-GHz dielectric spectroscopy. Developed in 0.35 μm 2P/4M RF CMOS, the IC measures frequency-dependent S_{21} magnitude and phase of a microfluidic dielectric sensor fabricated in a thick gold-on-glass microfabrication process and loaded with a material-under-test (MUT). The IC architecture implements a broadband frequency response analysis (bFRA) method by first down-converting the sensor response signal from the RF excitation frequency to an intermediate frequency (IF) of 1 MHz using a low-noise amplifier (LNA) and active mixer, followed by down-converting the IF signal to dc using a coherent detector employing IF amplification stages with programmable gain, a passive mixer driven by in-phase (I) and quadrature-phase (Q) signals and an active-RC lowpass filter (LPF). The sensor interfaced with the IC is fully capable of differentiating among deionized (DI) water, phosphate buffered saline (PBS), ethanol and methanol in tests conducted at four different excitation frequencies of 50

MHz, 500 MHz, 1 GHz and 3 GHz. Further, dielectric readings of ethanol from the sensor interfaced with the IC at five excitation frequencies in the range of 50 MHz to 2 GHz are in excellent agreement (error < 1%) with those from using a vector network analyzer (VNA) as the sensor readout. A bulk-solution reference measurement by an Agilent 85070E dielectric probe kit interfaced with a VNA is also performed to verify proof-of-concept feasibility in conducting MHz-to-GHz dielectric spectroscopy with a miniaturized measurement platform using μL-sample volumes.

The rest of this chapter is organized as follows. Section 2.1 describes the principles of the bFRA technique and presents the corresponding system architecture for the IC [2.1]-[2.2]. Section 2.2 discusses the circuit architecture of the major building blocks within the Gen-1 interface IC, and Section 2.3 presents electrical benchtop characterization results from a prototype fabricated in 0.35 μm RF CMOS as well as measurement results from the IC interfaced with the Gen-1 dielectric sensor [2.3]. Finally, Section 2.4 draws some conclusions from this work.

2.1 Operation Principles and System Implementation

Figure 2.1 illustrates the principles of the bFRA method. The sensor is excited with a single-tone sinusoidal signal, $A_0 \sin(\omega_{RF} t)$, at a user-set RF excitation frequency of ω_{RF}. Next, the sensor response signal to this input excitation, $A_1 \sin(\omega_{RF} t + \phi)$, is multiplied with another single-tone sinusoidal signal at a frequency of $(\omega_{RF} - \omega_{IF})$, where ω_{IF} is an intermediate frequency. Therefore, the output of the first multiplier stage can be expressed as:

$$V_{OUT,Mult1} = A_1 \sin(\omega_{RF} t + \phi) \times \sin((\omega_{RF} - \omega_{IF})t) = \frac{A_1}{2}\left[\cos(\omega_{IF} t + \phi) - \cos((2\omega_{RF} - \omega_{IF})t + \phi)\right]. \quad (2.1)$$

In the in-phase (*I*) and quadrature-phase (*Q*) branches, this signal will be multiplied with another single-tone sinusoidal signal at ω_{IF} and its quadrature-phase version, respectively. Therefore, the output of the second and third multiplier stages can be expressed as:

$$\begin{aligned}
&V_{OUT,Mult2} = \frac{A_1}{2}\left[\cos(\omega_{IF} t + \phi) - \cos((2\omega_{RF} - \omega_{IF})t + \phi)\right] \times \sin(\omega_{IF} t) = \\
&\frac{A_1}{4}[\sin(2\omega_{IF} t + \phi) - \sin(\phi) - \sin(2\omega_{RF} t + \phi) + \sin(2(\omega_{RF} - \omega_{IF})t + \phi)] \\
&V_{OUT,Mult3} = \frac{A_1}{2}\left[\cos(\omega_{IF} t + \phi) - \cos((2\omega_{RF} - \omega_{IF})t + \phi)\right] \times \cos(\omega_{IF} t) = \\
&\frac{A_1}{4}[\cos(2\omega_{IF} t + \phi) + \cos(\phi) - \cos(2\omega_{RF} t + \phi) - \cos(2(\omega_{RF} - \omega_{IF})t + \phi)].
\end{aligned} \quad (2.2)$$

Finally, the two output signals are lowpass filtered to retain their dc component and remove all other frequency components, which results in $V_{OUT,\ I}$ and $V_{OUT,\ Q}$ to be $-\frac{A_1}{4}\sin(\phi)$ and $\frac{A_1}{4}\cos(\phi)$, respectively. Since the RF excitation amplitude, A_0, can also be directly measured in a calibration procedure without the sensor in place (in that case, $V_{OUT,\ Q}$ will be equal to $\frac{A_0}{4}$) and therefore known, it can be seen that the two dc components are essentially proportional to the imaginary (real) part of sensor S_{21} in *I* (*Q*) mode of operation. The dielectric permittivity of the MUT loaded onto the sensor can then be extracted from the S_{21} measurement using a sensor calibration algorithm that runs offline on a personal computer (PC).

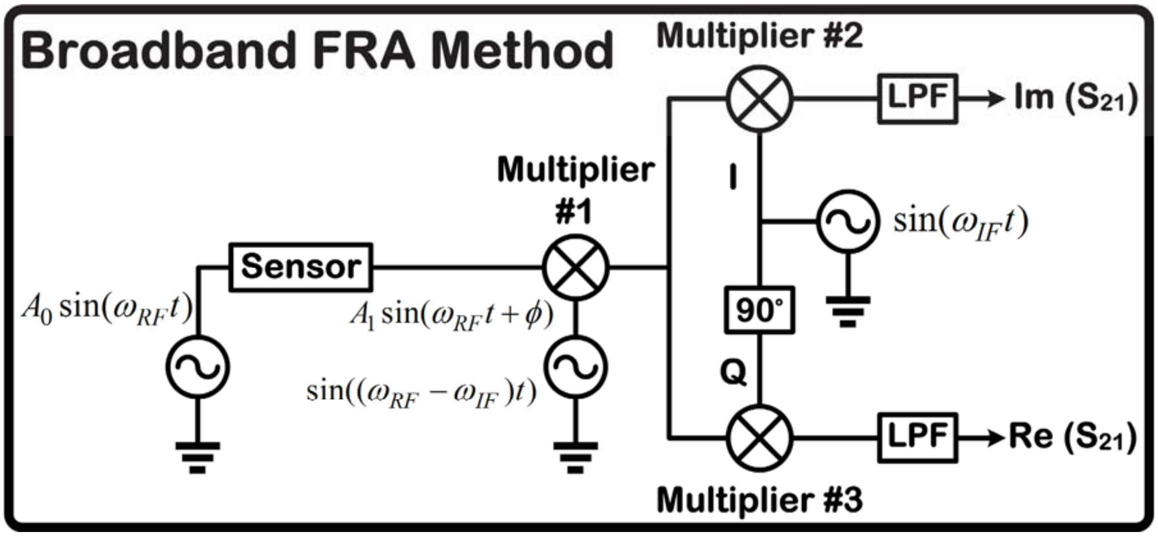

Figure 2.1: Broadband frequency response analysis (bFRA) method.

Figure 2.2 shows the system architecture of the sensor interface IC and an illustration of the experimental setup used in this work. The operation principle is that a sinusoidal excitation signal drives a microfluidic dielectric sensor based on a microstrip line with a centered gap as its parallel-plate capacitive sensing area [2.3]. As the MUT passes through this gap, the through-impedance of the sensor changes based on the dielectric permittivity of the liquid. The large through-impedance of the capacitive sensor dominates its series impedance, making it feasible to determine the impedance, and hence the liquid permittivity, using only an S_{21} measurement.

The interface IC is therefore designed to accurately measure the transmission characteristics (i.e., S_{21} magnitude and phase) of the loaded sensor using the bFRA method as previously described. Specifically, the sensor response signal at the RF excitation frequency is first down-converted to an IF frequency of 1 MHz using a low-noise amplifier (LNA) and a double-balanced, differential, Gilbert-cell, active mixer. The 1-MHz IF signal is next down-converted to dc using a coherent detector, employing a passive highpass filter (HPF), two variable-gain amplifiers (VGAs), a passive mixer driven by *I/Q* signals and a lowpass filter (LPF) to extract the dc component of the system output.

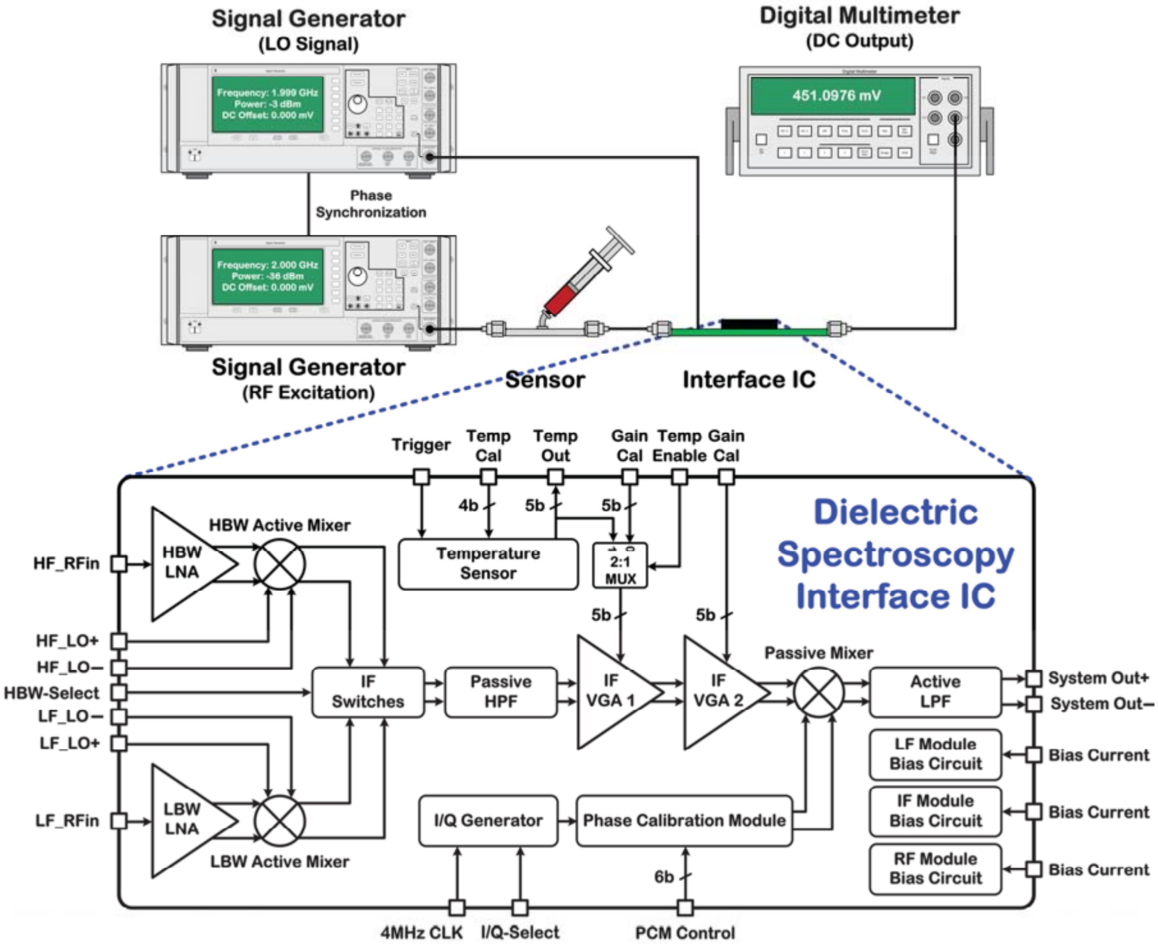

Figure 2.2: System architecture of the dielectric spectroscopy interface IC (Gen-1) and an illustration of the experimental setup.

As seen in Fig. 2.2, the system architecture incorporates two parallel paths at the front-end for processing the sensor response signal. The low-bandwidth (LBW) and high-bandwidth (HBW) paths are used for the excitation frequency range of ~10 to 200 MHz and ~200 MHz to 3 GHz, respectively. Controlled by an external bit (*HBW-Select*), the IF Switches block routes the appropriate RF module output to the input of the coherent detector for the second down-conversion step. Since the two RF modules have separate power supplies, they can be turned on and off independently. This feature allows the user to save power by using the LBW RF module only, in case the study does not require high excitation frequencies. The IF Switches block has relaxed design constraints, since it is placed *after* the active mixers and operates only statically.

The IF frequency of 1 MHz is high enough to minimize the impact of flicker noise and dc offset on the sensor response signal at the active mixer output, relaxing the design constraints of the front-end LNA and mixer. At the same time, the IF frequency is low enough to allow low-power design of the IF VGAs in the coherent detector circuitry.

After down-converting the sensor response signal to 1 MHz, a passive HPF removes the dc offset (and low-frequency noise) at the active mixer output, preventing the dc offset from saturating the subsequent VGAs. The gain of each VGA can be adjusted using an external 5b code (*Gain Cal*) to overcome the decrease of RF conversion gain versus frequency in the RF modules. Further, the gain of the first VGA can also be adjusted by the 5b digital output of an on-chip temperature sensor to compensate for the decrease of total system gain versus temperature in 0 to 60°C. This mode can be activated by an external bit (*Temp Enable*) that controls a 2:1 multiplexer for routing the appropriate 5b code to the first VGA for gain adjustment. The amplified/filtered IF signal is next down-converted to dc via a passive mixer and a LPF. The 1-MHz, square-wave, *I*/*Q* signals for the passive mixer are first derived by a digital *I*/*Q* generator from an external 4-MHz clock and then phase-adjusted using a phase calibration module (PCM) before they drive the passive mixer.

2.2 Integrated Circuit Implementation

In this section, we present the circuit architectures of the main building blocks of the sensor interface IC, including those in the HBW RF, IF and low-frequency (LF) modules. All analog and digital circuitry are powered from 1.5 and 3.3 V, respectively.

Figure 2.3 depicts the architecture of the HBW RF module. The HBW LNA has an inductorless, wideband, common-gate–common-source (CG-CS) architecture with a single-ended input matched to ~50 Ω [2.4], employing local feedback for G_m-boosting and a differential output that allows differential signaling throughout the rest of the system for canceling common-mode noise and even harmonics. Transistors $M_{2,3}$ implement a local feedback mechanism that boosts gm_1 by a factor of $(gm_2 + gm_3)/gm_4$, which in turn allows reducing the bias current of M_1 (600 µA) for low-power operation and increasing its resistive load (450 Ω) for enhanced gain. Similarly, current steering by M_3 (1.4 mA) also allows reducing the bias current of M_4 (1.2 mA) and hence increasing its resistive load. The bias currents of $M_{2,3}$ are set by tunable voltages $V_{b2,3}$, which allows controlling the gm_1-boosting factor and hence the LNA input impedance. The LBW LNA employs the same CG-CS architecture as that of the HBW LNA, but based on a *pMOS* CG transistor instead to reduce the low-frequency noise and with lower bias currents due to the reduced bandwidth (3-dB bandwidth of 197 MHz). Two capacitors (250 fF) in parallel with the resistive loads further reduce the out-of-band high-frequency noise.

Each LNA is designed to target equal gain in the CG and CS paths for a balanced differential output. However, a gain mismatch would practically lead to incomplete cancellation of the even-order harmonics at the LNA output. Our IF-based readout architecture (as compared to e.g. a direct-conversion receiver) is not too sensitive to these even-order harmonics, because the corresponding down-converted signal components would not overlap with the IF of 1 MHz where the information is located after mixing. Additionally, these down-converted signal components would be further filtered by the IF VGAs before reaching the passive mixer. Finally, the 1-MHz, square-wave, differential, local oscillation (LO) signal of the double-balanced passive mixer does not contain even-order harmonics, minimizing the possibility of these down converted signal components to translate into dc at the system output, even if they reach the passive mixer.

The HBW active mixer is a standard, double-balanced, Gilbert cell with resistive loads and source-degenerated RF input transistors (using two resistors) for enhanced linearity. The bias current of the mixer (325 μA), which is controlled by the external V_{Bias}, is set to be low enough to reduce the power consumption, while meeting the design constraints related to mixer bandwidth, linearity and noise figure. The low bias current also allows using relatively large resistive loads (3 kΩ) at the output for increased conversion gain without adding extra *1/f* noise. The LBW active mixer employs an identical architecture, but with lower bias current (165 μA) due to the reduced bandwidth and without resistive source degeneration. To maintain enhanced linearity, the sizing of the RF input transistors is reduced instead. The ensuing reduction in the conversion gain is compensated by further increasing the resistive loads (8 kΩ) afforded by the lower bias current resulting in higher voltage headroom available at the output.

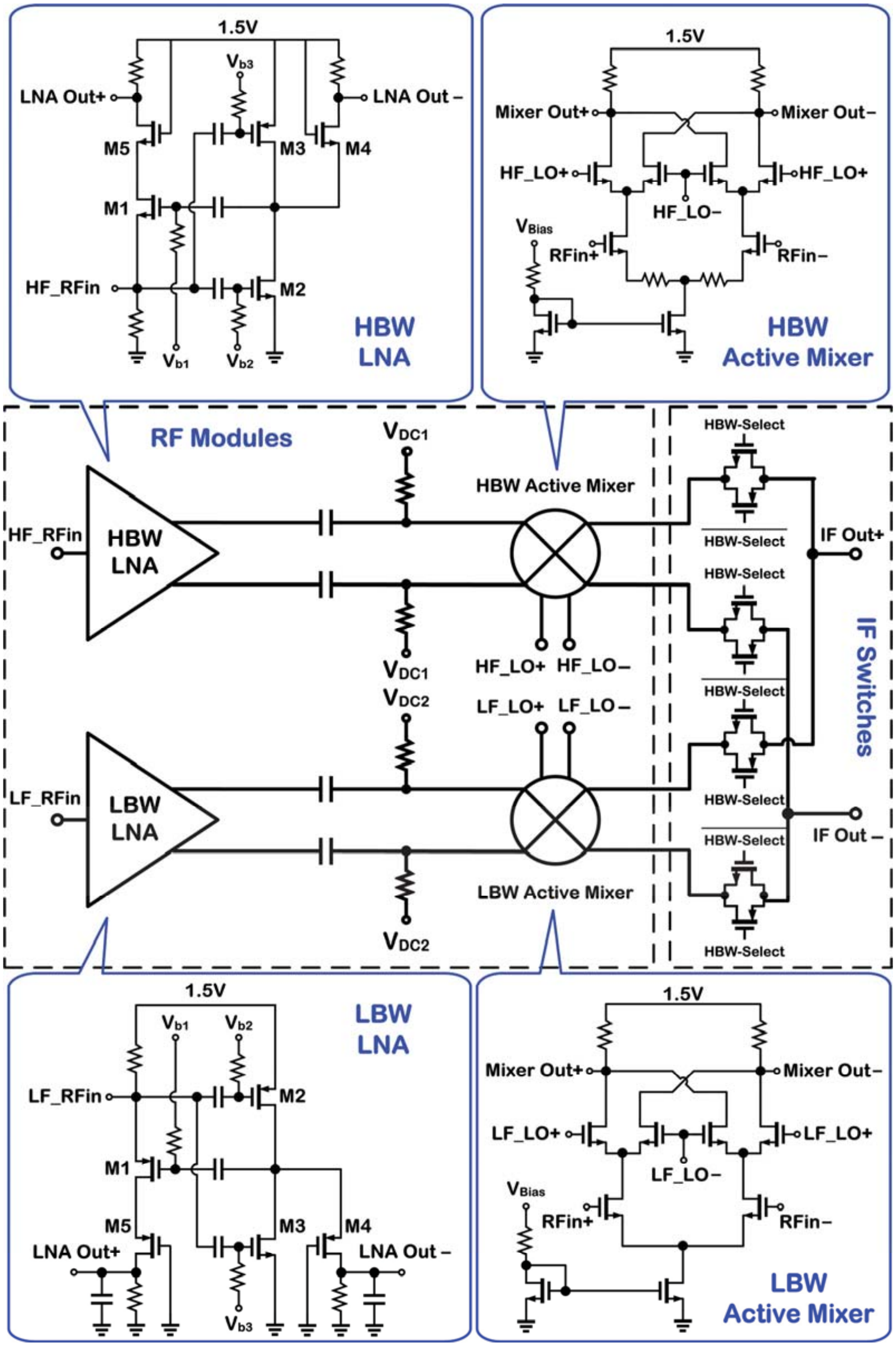

Figure 2.3: Circuit architecture of the RF module in Gen-1 Interface IC.

Figure 2.4 shows the circuit architecture of the IF module, comprising two 5b-programmable VGAs with each gain stage based on a differential-input differential-output op-amp with resistive feedback. The op-amp employs a two-stage, telescopic, folded-cascode architecture with common-mode feedback, featuring a high open-loop gain (132.4 dB) for enhanced linearity and accurate gain in closed-loop mode, rail-to-rail input/output dynamic range and a unity-gain bandwidth of 34 MHz (selected to be > 10× higher than the 1-MHz IF) for optimized power consumption and operation speed. A series resistor (5 kΩ)-capacitor (1 pF) combination is used for stabilizing the op-amp. The properly sized transmission gates in parallel with the five feedback resistors in each gain stage are driven by digital control signals at 3.3 V for negligible ON resistance (compared to the LSB feedback resistor) for enhanced linearity in gain variation.

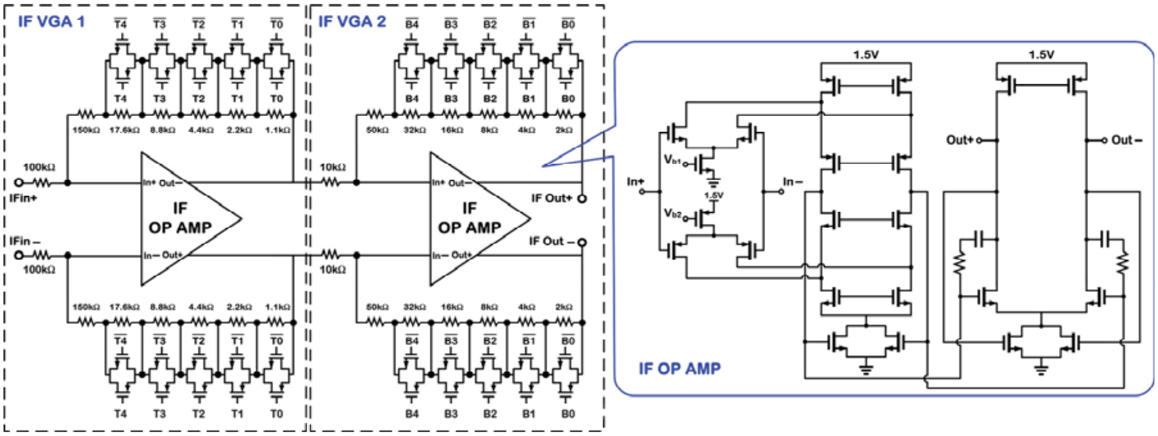

Figure 2.4: Circuit architecture of the two VGAs in the IF module of Gen-1 Interface IC.

As shown in Fig. 2.5, a low-power, low-area, digital circuit is used to generate the 1-MHz, square-wave, I and Q signals from a 4-MHz external reference clock by frequency division using two DFFs and an XOR function of the two DFF outputs, respectively. An external control bit (I/Q-Select) determines which signal is selected to drive the passive mixer. Given the path delay experienced by the sensor response signal at each excitation frequency, the PCM circuitry adds appropriate time delay in the range of 0.8 to 50 ns to the I/Q signals (same delay for both signals to preserve their 90° phase shift) before they drive the passive mixer. The PCM circuitry consists of four programmable delay cells, each incorporating 6 binary-weighted metal-insulator-metal (MiM) capacitors at the output of an inverter. The delay can be varied digitally using an external 6b code (PCM Control) that controls the operation of six properly sized transmission gates in series with the load capacitors. A second inverter is used to sharpen up the delayed signal before it drives the next programmable delay cell. To mitigate the effect of parasitic capacitance, the transmission gates are connected to the bottom plate of the load capacitors, while the top plate is connected to the output node. Also, instead of one programmable delay cell with large load capacitors, four identical delay cells with smaller capacitors are used for better capacitor matching with careful layout and thus enhanced linearity in delay variation. The last programmable delay cell drives an output buffer that generates the differential local oscillation (LO) signals for the passive mixer.

As described in the following sections, the timing operation of the SoC must ensure that electrical stimulation would not temporally overlap with voltammetry in order to minimize the possibility of large stimulus artifacts interfering with FSCV current recordings. However, proper timing management is still not enough to allow *combined* electrical stimulation and FSCV sensing using a single-chip device.

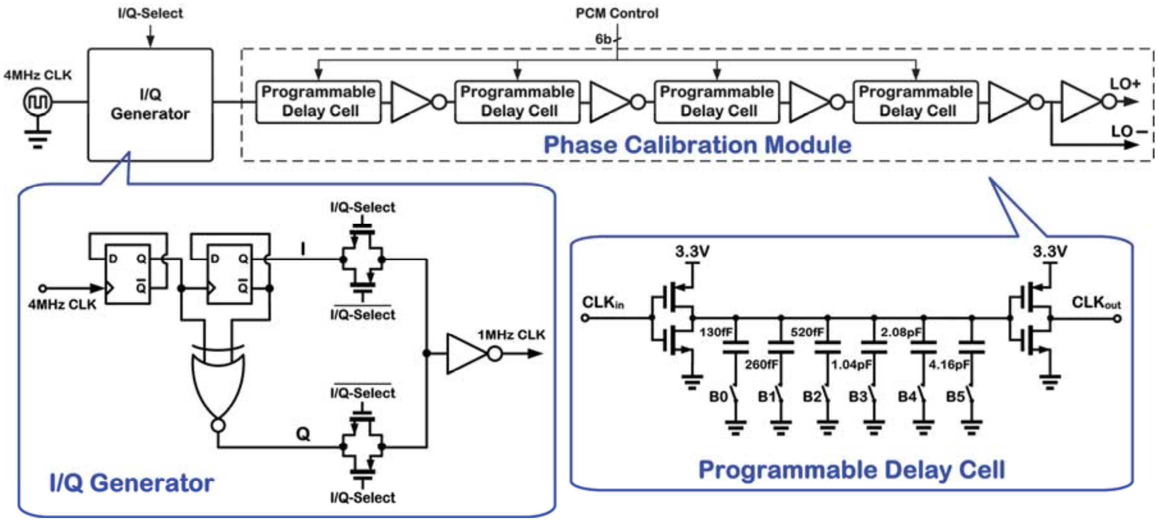

Figure 2.5: Circuit architecture of the digital I/Q generator and PCM circuitry in the LF module.

Figure 2.6 shows the circuit architecture of the passive mixer and the 1st-order active-RC LPF in the LF module. The passive mixer, employing four identical transmission gates as its switches, is a double-balanced Gilbert cell with reduced dc offset and low-frequency noise at its output compared to an active counterpart. The double-balanced architecture also attenuates the 1-MHz LO feed-through at the output, relaxing the design constraints of the LPF. The LF op-amp of the LPF has an identical architecture to that of the IF op-amp, but with much lower unity-gain bandwidth (1.97 MHz), and hence consumes less power. Using two external capacitors (10 nF), the 3-dB bandwidth of the LPF is ~1.48 kHz for a tradeoff between the total measurement time of the system for each excitation frequency (affected by the settling time of the LPF output) and noise bandwidth as well as filter attenuation at 1 MHz (IF/LO feed-through) and 2 MHz (up-converted IF) at the passive mixer output. The externally tunable bias voltages, $V_{CM1,2}$, are used to cancel out the dc offset of the LPF output.

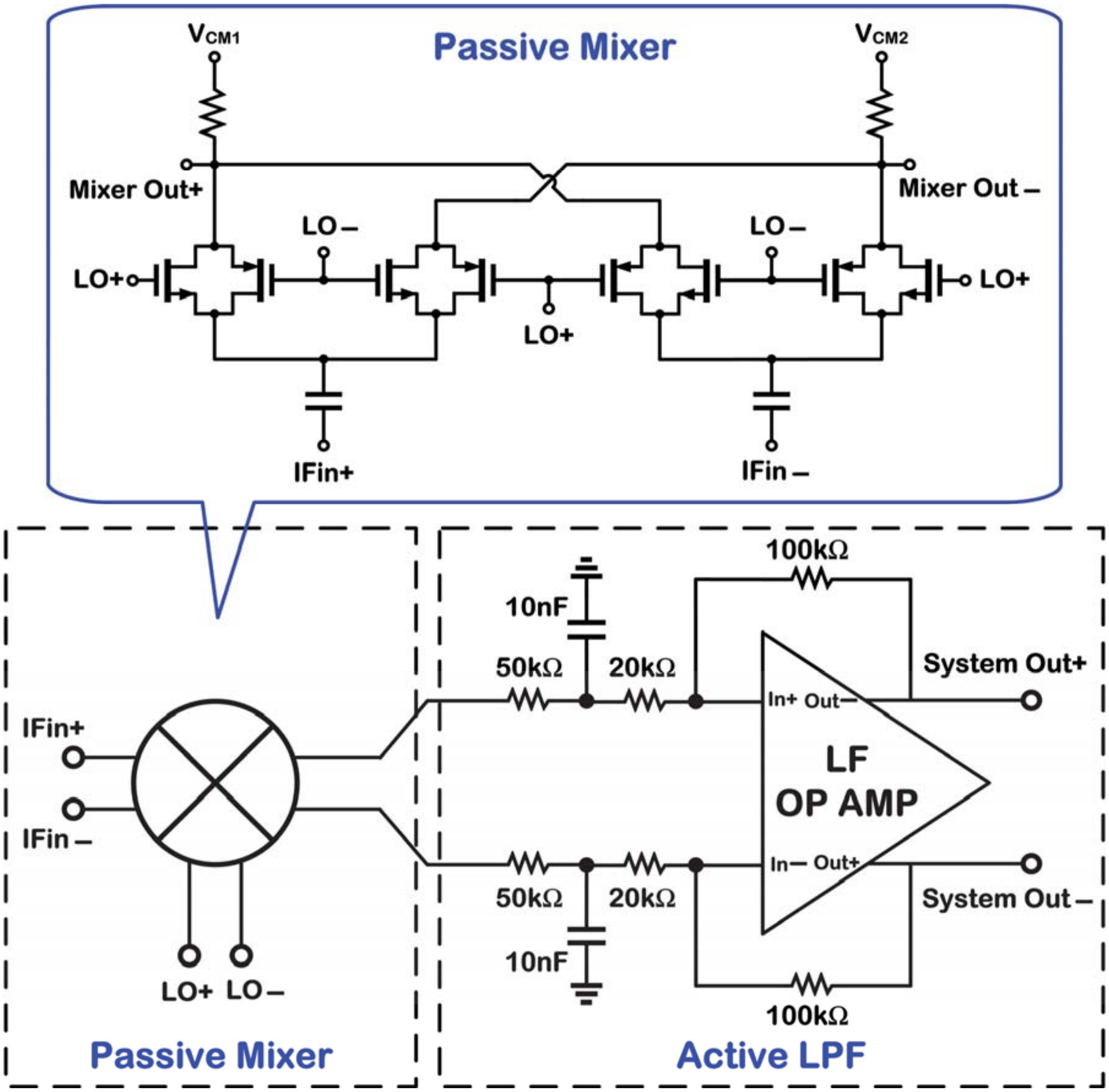

Figure 2.6: Circuit architecture of the passive mixer and active LPF in the LF module.

2.3 Measurement Results

A prototype chip was fabricated in AMS 0.35 µm 2P/4M RF CMOS, measuring 3 mm × 3 mm including the bonding pads. Fig 2.7 shows a microphotograph of the fabricated chip. This section presents the measurement results from electrical characterization of the IC as well as from DS studies using the IC interfaced with the microfluidic dielectric sensor from [2.3]. All measurements were performed using the

HBW RF module of the IC unless stated otherwise. Fig 2.8 shows a photograph of the custom Printed Circuit Board (PCB), showing the chip housed in a Quad Flat No-leads (QFN) package and transmission lines for feeding the RF and LO signal to the chip.

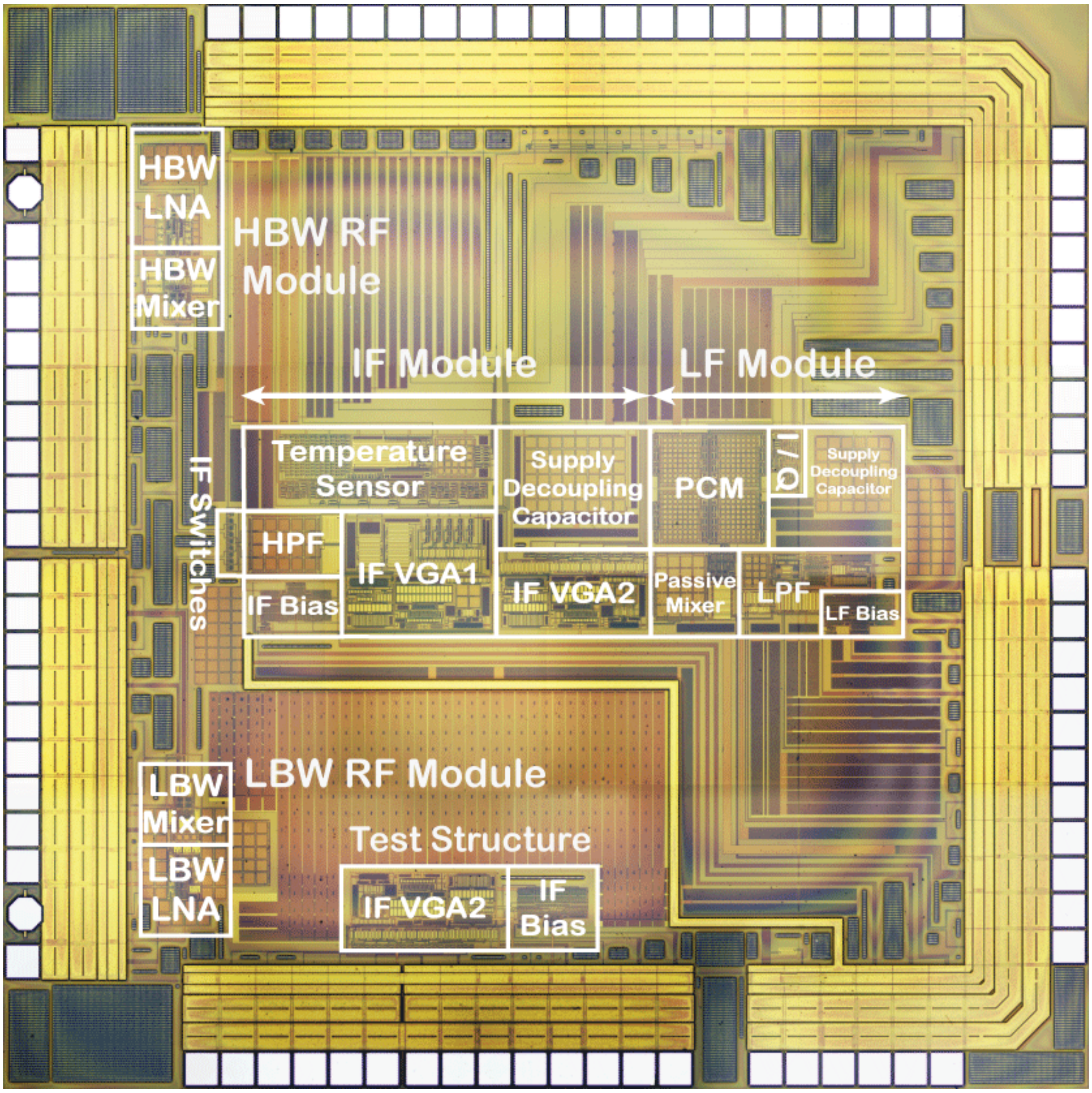

Figure 2.7: Die micrograph of the 3 mm × 3 mm Gen-1 interface IC fabricated in AMS 0.35 µm 2P/4M RF CMOS.

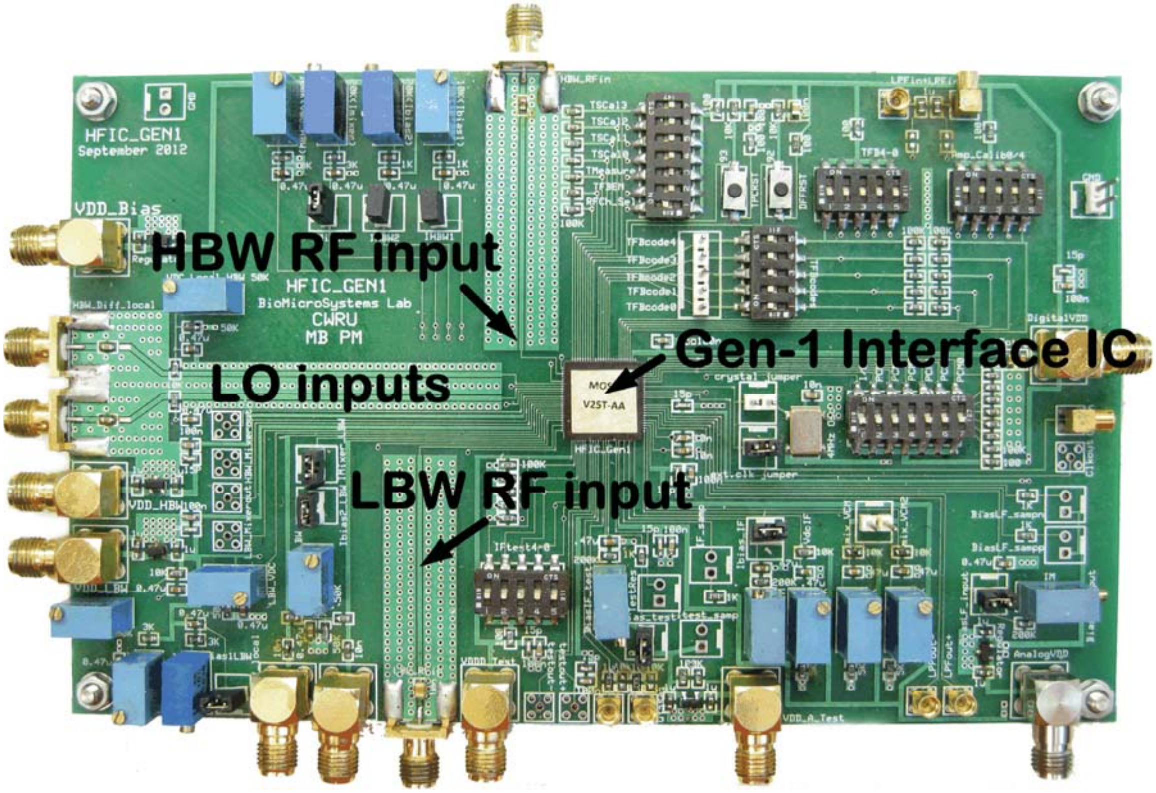

Figure 2.8: photograph of the Gen-1 interface IC custom PCB for dielectric spectroscopy.

2.3.1 Electrical Characterization

The top plots in Fig. 2.9 depict the measured conversion gain of the HBW RF module (i.e., HBW LNA + active mixer) versus the RF and IF frequencies. For both measurements, the RF input power was set to be -40 dBm, and the RF input frequency was fixed at 1 GHz for the second measurement. As seen on the left plot, the conversion gain was 28.2 dB at 200 MHz and decreased to 9.9 dB at 2.8 GHz. This reduction in conversion gain versus the RF frequency was compensated to a large degree by a gain increase in the IF module via gain calibration. As seen on the right plot, the measured 3-dB bandwidth was ~6 MHz, providing a gain of 24.2 dB at 1 MHz and attenuating higher-frequency noise components and harmonics at the IF output.

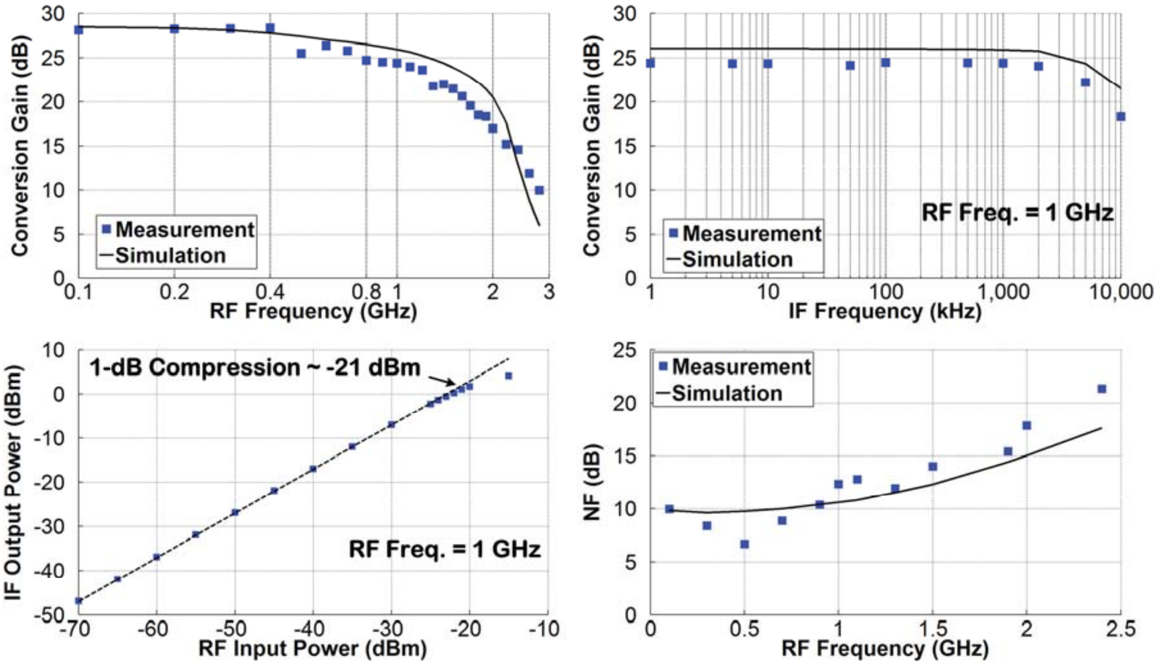

Figure 2.9: Measured results from the HBW RF module. Top – Conversion gain vs. RF frequency (left) and IF frequency (right). Bottom – Linearity (left) and noise figure (right) characterization.

The bottom plots in Fig. 2.9 depict the measured linearity and noise performances of the HBW RF module. With the RF signal at 1 GHz, the 1-dB compression point was -21 dBm, showing that the HBW RF module was highly linear with an RF input power less than -31 dBm (backing off by 10 dB from the 1-dB compression point). The minimum double-side-band noise figure (NF) of the HBW RF module was measured to be 6.7 dB at 500 MHz and increased to 17.8 dB at 2 GHz. This increase was primarily due to the decrease of the LNA gain versus frequency, allowing the mixer to contribute more to the input noise. The power consumption of the HBW RF module was measured to be 7.1 mW from 1.5 V including the bias circuitry.

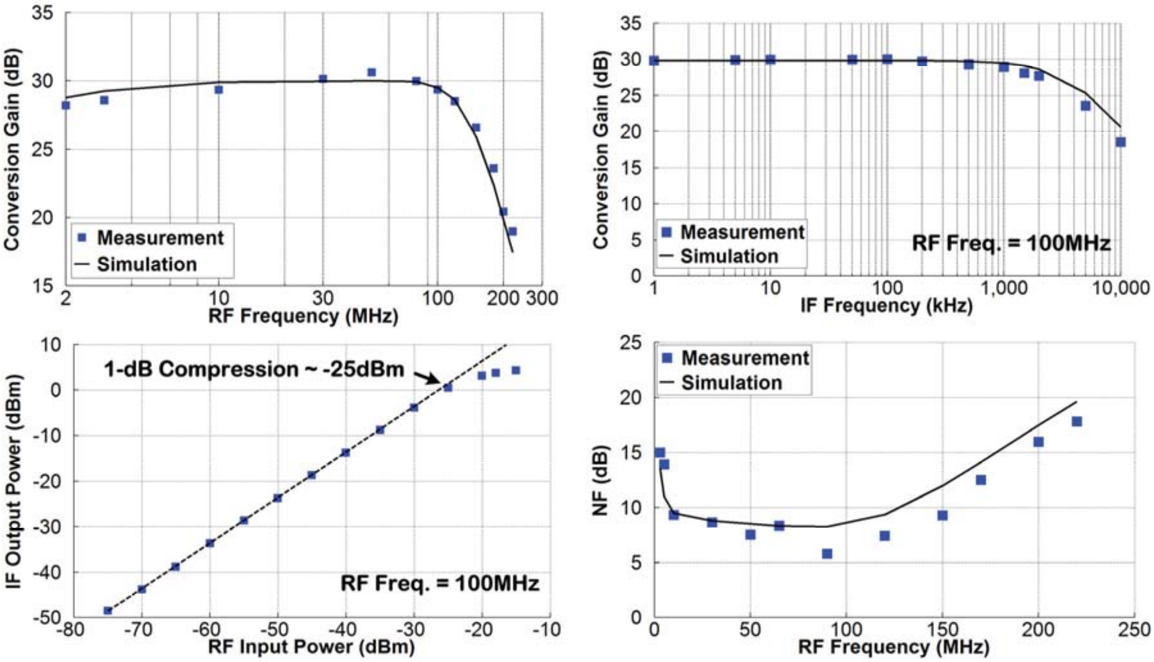

Figure 2.10: Measured results from the LBW RF module. Top – Conversion gain versus RF frequency (left) and IF frequency (right). Bottom – Linearity (left) and noise figure (right) characterization.

The top plots in Fig. 2.10 depict the measured conversion gain of the LBW RF module (i.e., LBW LNA + active mixer) versus the RF and IF frequencies. As seen in the left plot, the conversion gain was 29.3dB at 10MHz and decreased to 20.4dB at 200MHz. The bottom plots in Fig. 2.10 depict the measured linearity and noise performances of the LBW RF module. With the RF signal at 100MHz frequency, the 1-dB compression point was -25dBm, showing that the LBW RF module was highly linear with an RF input power less than -35dBm (backing off by 10dB from the 1-dB compression point).

The top left plot in Fig. 2.11 depicts the measured gain of the IF VGA versus frequency, when the gain calibration code was set to zero (i.e., minimum VGA gain). The gain was measured to be 14.6dB at 1MHz with 3dB bandwidth of 8.3MHz. At 1MHz, the gain exhibited a very linear response versus the 5b calibration code. As stated previously, the LPF exhibited a measured 3dB bandwidth of 1.48kHz. As seen in the bottom right plot, the phase calibration module (PCM) also exhibited a very linear response versus the 6b calibration code, with a maximum delay of 50ns in steps of 0.8ns.

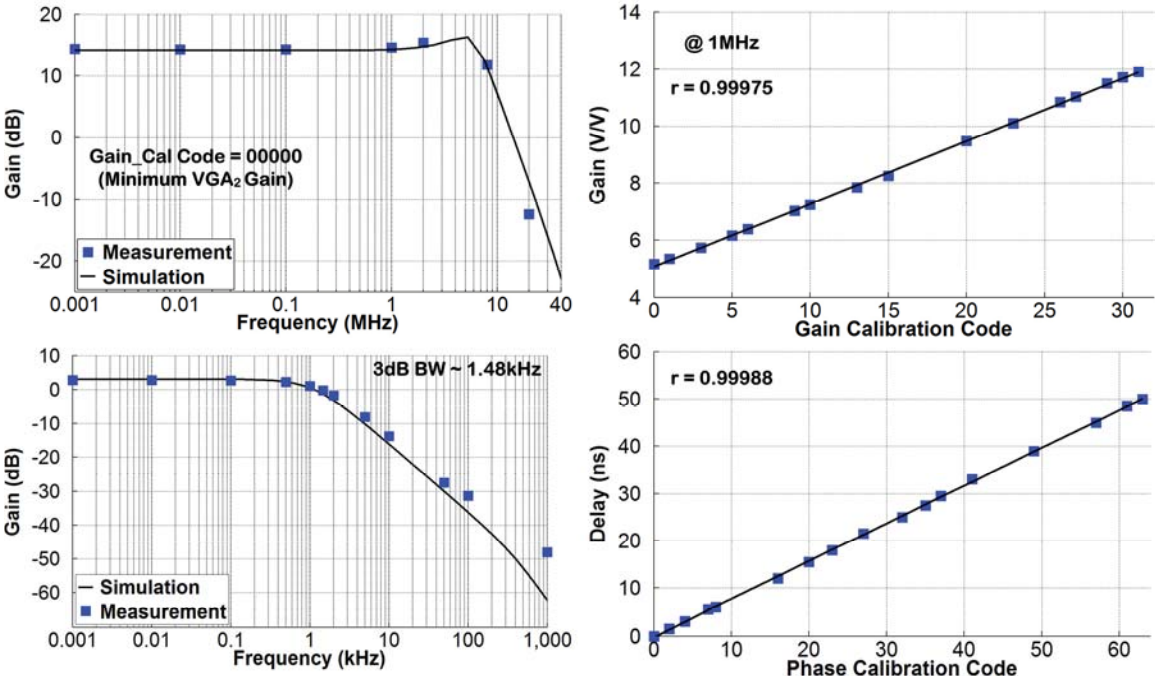

Figure 2.11: Measured results from the IF and low-frequency (LF) modules Top – IF VGA2 gain versus frequency (left) and calibration code (right). Bottom – LPF frequency response (left) and PCM characterization (right).

Figure 2.12 depicts the dc system output versus the RF input phase from 0 to 360° with the RF input amplitude and frequency set to 1 mV and 3 GHz, respectively. As can be seen, after phase calibration by the PCM to remove any phase offset (calibration code of 011111 for f_{RF} of 3 GHz), the dc system outputs in I and Q modes were proportional to $\sin(\phi)$ and $\cos(\phi)$, respectively, as predicted in Section 2.1, demonstrating correct functionality of the interface IC.

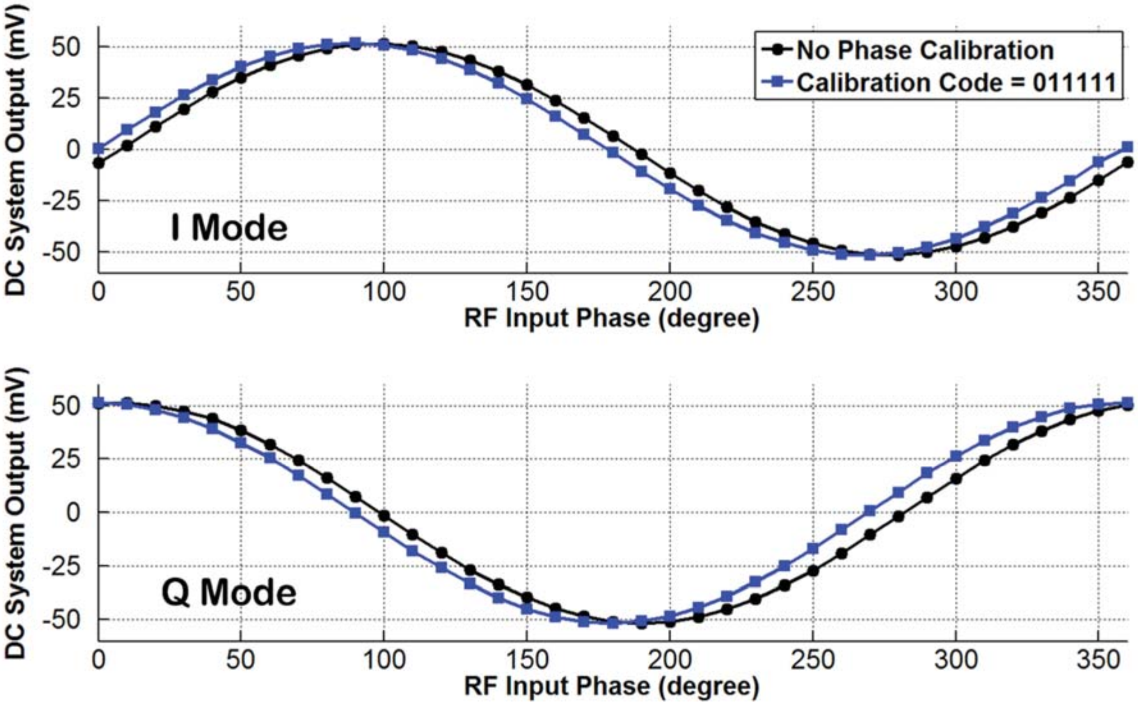

Figure 2.12: Measured dc system output *vs.* RF input phase in *I* (top) and *Q* (bottom) mode of operation. The RF input amplitude and frequency were 1 mV and 3 GHz, respectively.

In the absence of an on-die calibration loop to automatically set the gain of the IF VGAs, one-time gain calibration was performed manually. Specifically, at a given RF excitation frequency (e.g., 1 GHz), a phase calibration was first performed using the PCM to ensure that the dc system output in *Q* mode would be proportional to $\cos(\varphi)$. Next, the RF signal at 1 GHz and with fixed amplitude was directly applied to the input of the IC. Setting the RF input phase to 0 and operating the system in *Q* mode would result in the dc system output to be proportional to the total system gain. Next, the 5b control word (*Gain Cal*) for IF gain calibration was adjusted to match the dc system output at 1 GHz to that obtained with a lower excitation frequency (e.g., 300 MHz in Fig. 15). This calibration procedure was then repeated for all other RF excitation frequencies to obtain the requisite 5b control words.

As seen in the right plot in Fig. 2.13, the gain calibration in the IF module yielded a constant total system gain of 200 V/V for each RF excitation frequency. The gain calibration could not be done for frequencies >1.8 GHz, because the corresponding conversion gain drop I the HBW RF module was higher than the maximum available gain in the IF VGAs. Therefore for subsequent measurements at such frequencies, the total system gain needed to be measure every time prior to the S_{21} measurement. This limitation can easily be addressed in the future b providing higher gain values in the IF module.

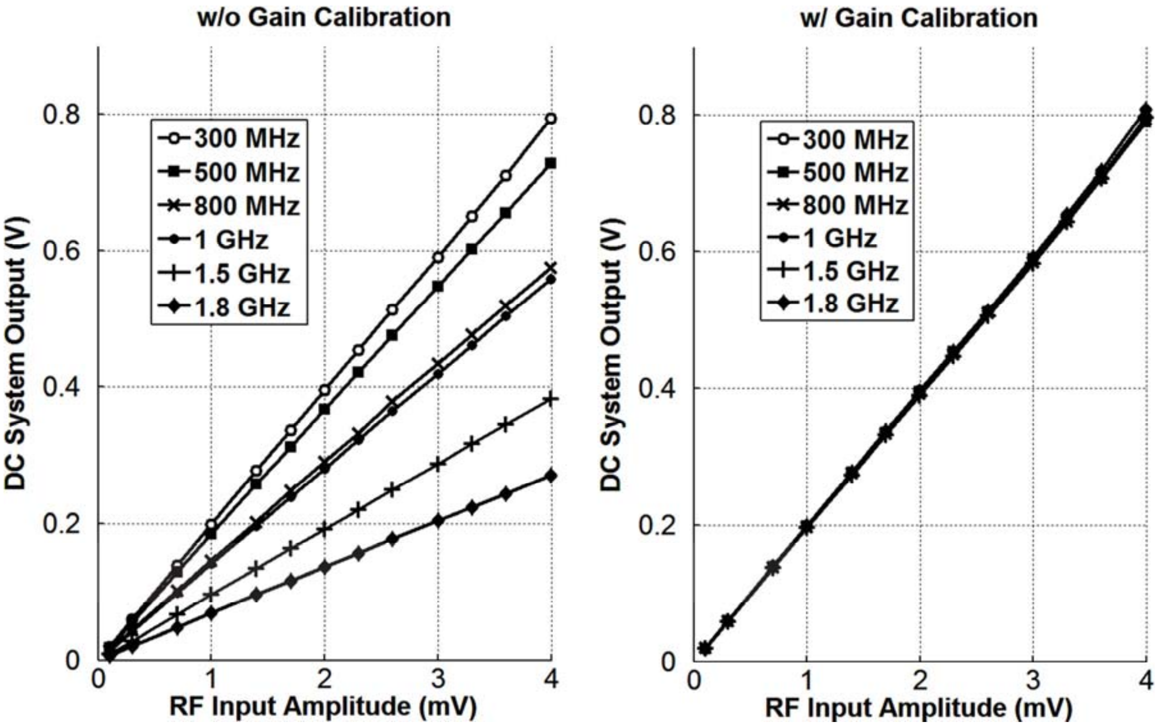

Figure 2.13: Measured dc system output vs. RF input amplitude for six different RF input frequencies without (left) and with (right) gain calibration in the IF module.

The top plots in Fig. 2.14 depict the dc system output versus the RF input phase from 0 to 360° with the RF input amplitude and frequency set to 1mV and 100MHz, respectively. As can be seen, after phase calibration by the PCM (calibration code of

100010) to remove any phase offset, the dc system output in I and Q modes was proportional to $\sin(\varphi)$ and $\cos(\varphi)$, respectively. The bottom plots in Fig. 2.14 show the dc system output in Q mode versus the RF input amplitude for five different RF input frequencies from 10 to 200MHz. In the left plot, no gain calibration was performed in the IF module, and hence the total system gain (i.e., from RF to dc) varied with the RF excitation frequency due to conversion gain variability in the LBW RF module. This limitation was addressed in the right plot via gain calibration in the IF module to yield a constant total system gain of 150V/V at each RF excitation frequency.

Finally, Fig. 2.15 depicts the measured signal-to-noise ratio (SNR) at the system output versus the RF input power for three different RF excitation frequencies of 50 MHz (using the LBW RF module), 1 GHz and 3 GHz. The peak SNR was measured to be >83 dB at 50 MHz and 1 GHz at an RF input power of -39.1 and -36 dBm, respectively. For a given RF input power, the SNR dropped by ~20 dB from 1 to 3 GHz due to the decreased total system gain and increased output noise level. Nonetheless, a peak SNR of 78.2 dB was still achieved at 3 GHz at an increased RF input power of -22.4 dBm. Any further increase in the RF input power would saturate the output voltage of the IF gain stages, resulting in distortion of the otherwise sinusoidal IF signal and leading to a decrease in the signal power at 1 MHz that propagates all the way to the system output and degrades the output SNR.

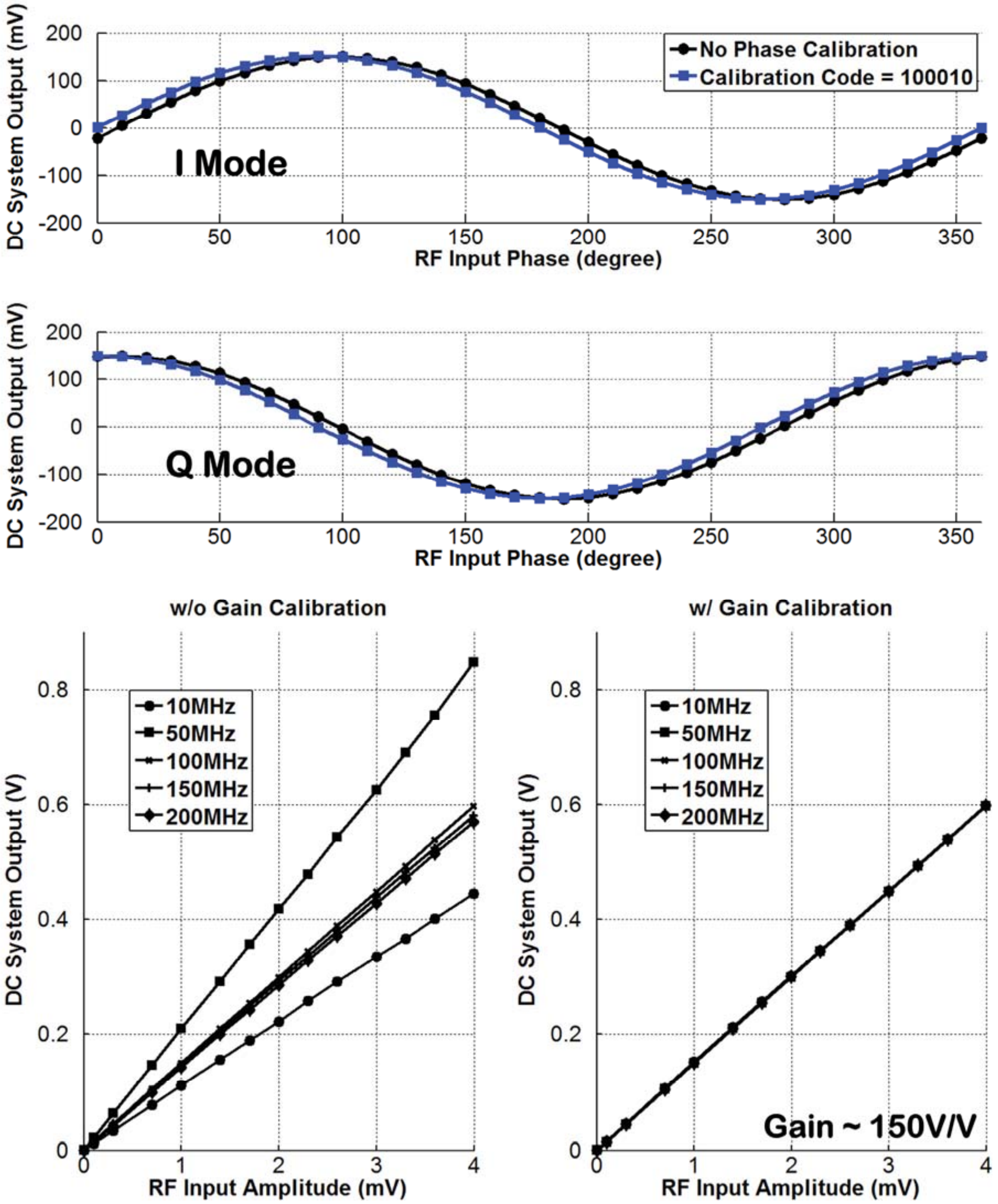

Figure 2.14: Top – Measured dc system output versus RF input phase in I/Q modes of operation. Bottom – Measured dc system output versus RF input amplitude for five different RF excitation frequencies without (left) and with (right) gain calibration in the IF module.

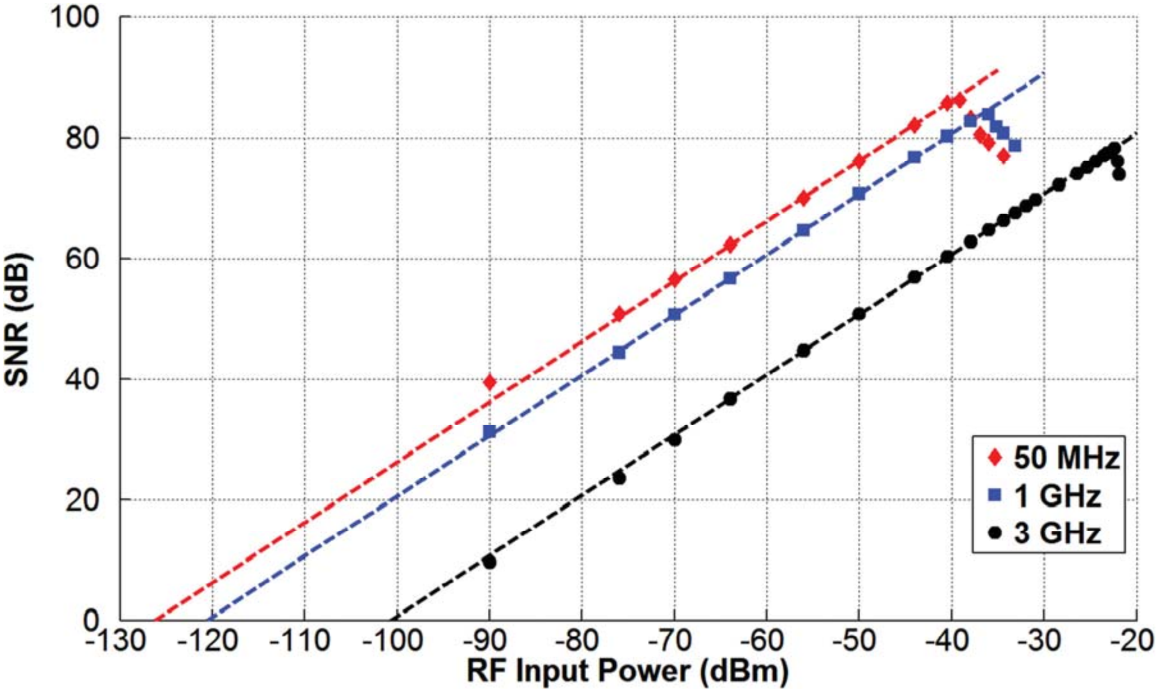

Figure 2.15: Measured SNR at the system output vs. RF input power for three different RF input frequencies of 50 MHz, 1 GHz and 3 GHz.

2.3.2 Voltage-Based Wideband Measurement Using Gen-1 Interface IC

Expensive, benchtop vector network analyzers (VNAs) are routinely used in radio-frequency integrated circuit (RFIC) design to characterize a variety of RF components and subsystems. More recently, benchtop VNAs are also used in material characterization, dielectric spectroscopy, and impedance spectroscopy, with a wide range of potential applications including petroleum analysis, food quality and safety monitoring, as well as structural biology. The VNA typically provides information on reflection or transmission characteristics of the device-under-test (DUT) by measuring the S_{11} or S_{21} parameter of the DUT, respectively.

On the other hand, RF/microwave biomedical sensors and systems are increasingly garnering attention for emerging applications such as noninvasive blood glucose measurements in point-of-care diagnostics [2.5], cancerous cell detection [2.6], and remote, noncontact vital sign monitoring [2.7]. These applications would benefit from a miniaturized, low-power, low-cost, and portable realization of the read-out electronics to replace the expensive, bulky VNA equipment.

To that end, Hofmann et al. have reported a 3-band, 2-port VNA for biomedical concentration measurements [2.8]. Designed for measuring aqueous glucose solutions, the system can operate at 6.6, 19.7, and 32.4GHz with a 10% bandwidth. More recently, Nehring et al. have also reported an integrated microwave VNA for biomedical sensor read-out applications [2.9]. Realized using a low-cost silicon-germanium technology, the system can conduct reflection-based measurements from 17 to 21GHz, but cannot perform any transmission-based characterization. Furthermore, neither of these works is capable of extending the frequency range of operation down to the MHz range.

This section presents wideband measurement of the transmission characteristics of a device-under-test (DUT) in the voltage domain using the Gen-1 Interface IC (RX IC). The receiver IC employs a broadband frequency response analysis methodology in order to measure the amplitude and phase of an RF excitation signal applied to the input port of the DUT and received at its output port. Utilizing three different test impedances as DUTs, the receiver IC can measure the transmission characteristics of each DUT, as quantified via its S_{21} parameter, over a wide frequency range from 10MHz to 3GHz [2.10]. The S_{21} readings of the IC are also in excellent agreement with reference measurements conducted by a benchtop vector network analyzer (VNA). This work can ultimately enable the miniaturization of read-out electronics in sensing platforms that rely upon the measurement of transmission characteristics of a DUT.

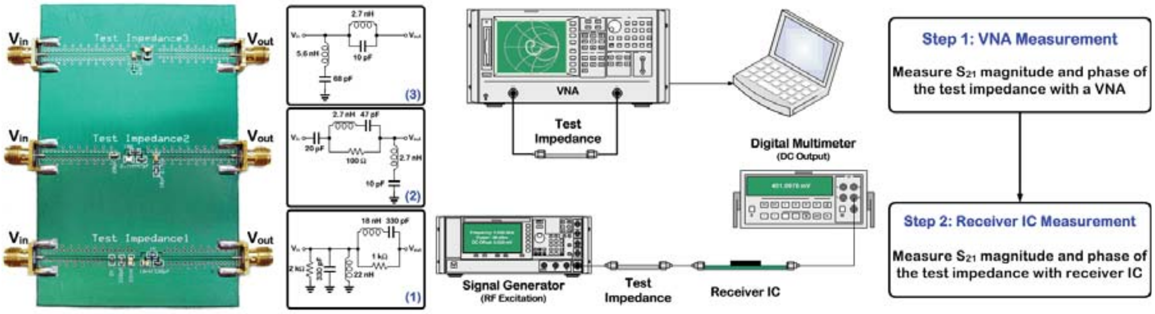

Figure 2.16: Photograph and circuit schematic of three test impedances along with illustration of the procedure to measure their S_{21} parameter.

To showcase the utility of the integrated receiver IC in measuring transmission characteristics in the form of S21 parameter, three test impedances were designed, fabricated on a printed-circuit board (PCB), and interfaced with a benchtop VNA as well as the receiver IC, as shown in Fig. 2.16. A second signal generator (not shown) that was synchronized in phase with the RF signal generator was used to provide the local oscillation (LO) signal for the IC with a 1-MHz frequency offset from the RF excitation frequency. VNA measurements were performed in 10MHz to 3GHz, whereas IC measurements were done at 19 distinct excitation frequencies using both the LBW and HBW RF modules. As can be seen in Fig. 2.17, the S21 magnitude and phase readings by the IC closely matched those by the VNA for all three test impedances. The error between the two measurements was primarily attributed to any impedance mismatch (versus 50Ω) at the input of the IC, as well as any loss or phase shift added by connectors and short cables used to interface the test impedances with the signal generator and the IC.

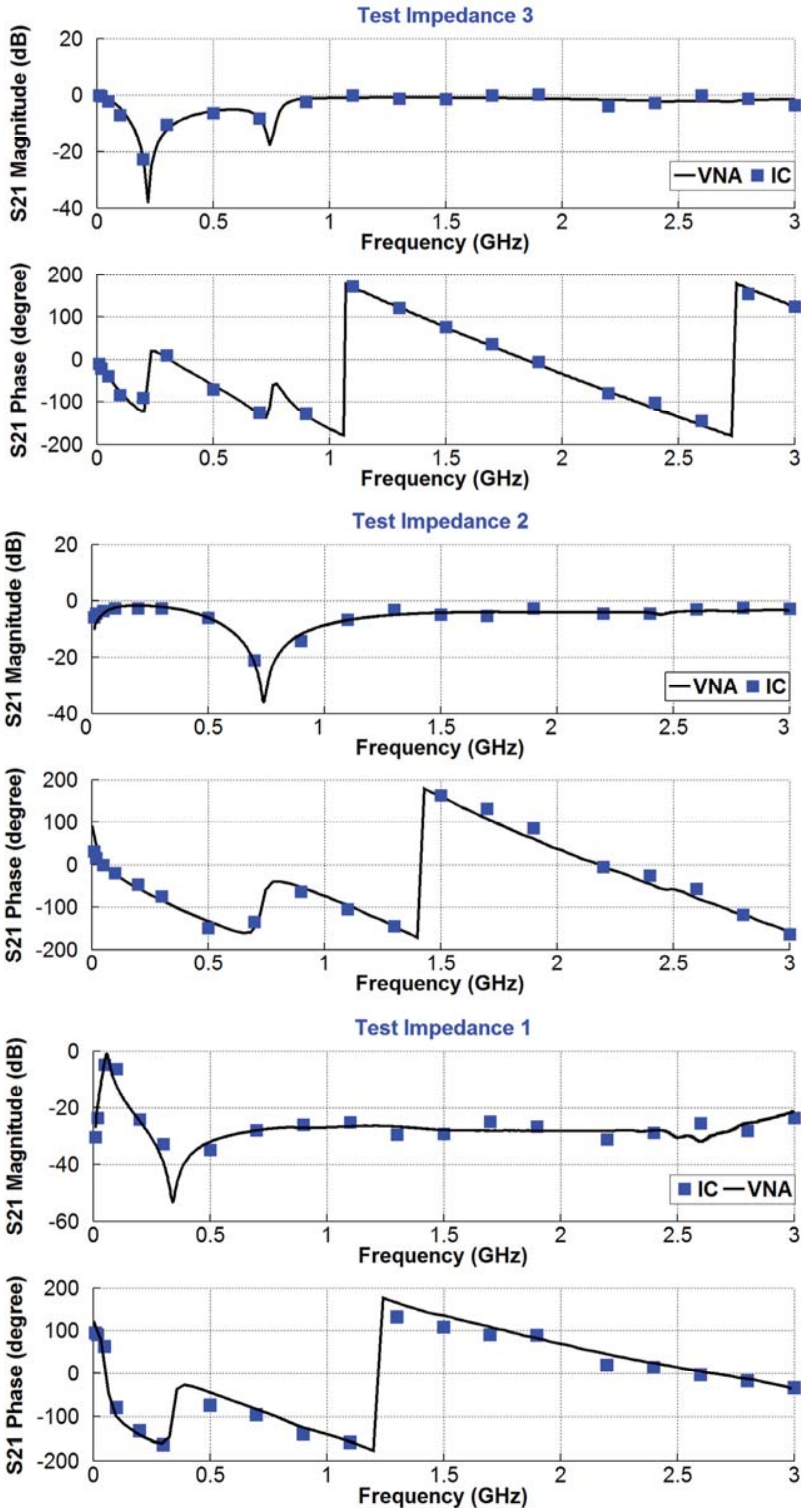

Figure 2.17: S_{21} magnitude and phase of the three test impedances versus frequency measured by a benchtop VNA and the receiver IC.

2.3.3 Gen-1 Dielectric Sensor + Interface IC Experiments

In this section, the Gen-1 Interface IC was interfaced with the microfluidic dielectric sensor from [2.3], and various experiments were performed. The ultimate goal was to extract the frequency-dependent dielectric permittivity of an MUT from “sensor + IC” measurements and thereby demonstrate proof-of-concept feasibility in miniaturization of the DS platform. As previously stated in Section II.A, this necessitated to also develop a sensor calibration algorithm that ran offline on a PC as described in further detail below.

Figure 2.18 shows the measured dc system output in *I* mode versus that in *Q* mode at 50 MHz (using the LBW RF module), 500 MHz, 1 GHz and 3 GHz, when the sensor was loaded with deionized (DI) water, phosphate buffered saline (PBS), ethanol and methanol as the MUT. Our miniaturized measurement platform was fully capable of differentiating among the four MUTs. Interestingly, although PBS and DI water had very similar responses at 3 GHz (this is not entirely unexpected given that PBS is primarily water-based and that the dielectric relaxation characteristics of water molecules would dominate the response at sufficiently high excitation frequencies), they had very different responses at 50 MHz, indicating that conducting these measurements in MHz-to-GHz range can indeed yield additional information.

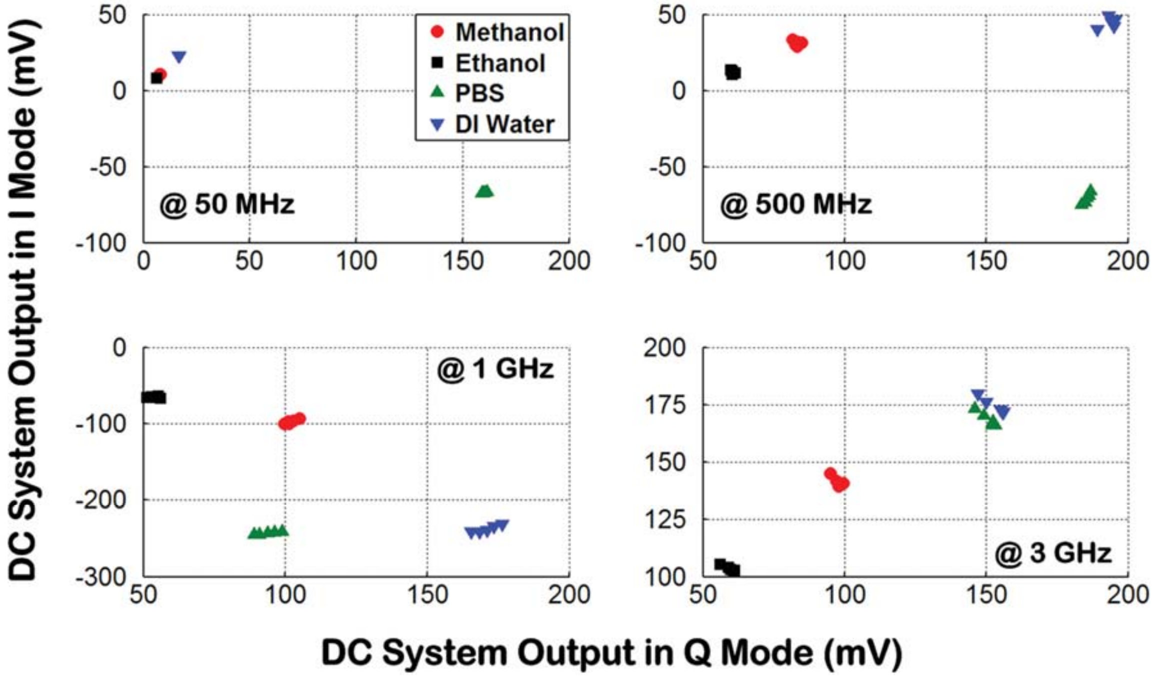

Figure 2.18: Measured dc system output in I/Q modes at 0.05, 0.5, 1 and 3 GHz with the DS sensor loaded with DI water, PBS, ethanol and methanol as the MUT.

As shown in Figure 2.19, In order to show the functionality of the interface IC in dielectric spectroscopy, the IC was interfaced with the DS sensor to extract the frequency-dependent dielectric permittivity of organic chemicals. This measurement was done in 3 steps. In step 1, the permittivity of the bulk-solution MUT was measured using an Agilent dielectric probe kit and VNA as reference measurement. In step 2, the S_{21} magnitude and phase of the DS sensor loaded with the MUT was measured by VNA as another reference measurement. In step 3, the S_{21} magnitude and phase of the DS sensor loaded with the MUT was measured by the interface IC, instead of a VNA. Comparison of results from steps 2 and 3 can demonstrate the feasibility of sensor read-out miniaturization for S_{21} measurement, whereas comparison of results from steps 1 and 3 can demonstrate the feasibility of miniaturization of the entire DS system.

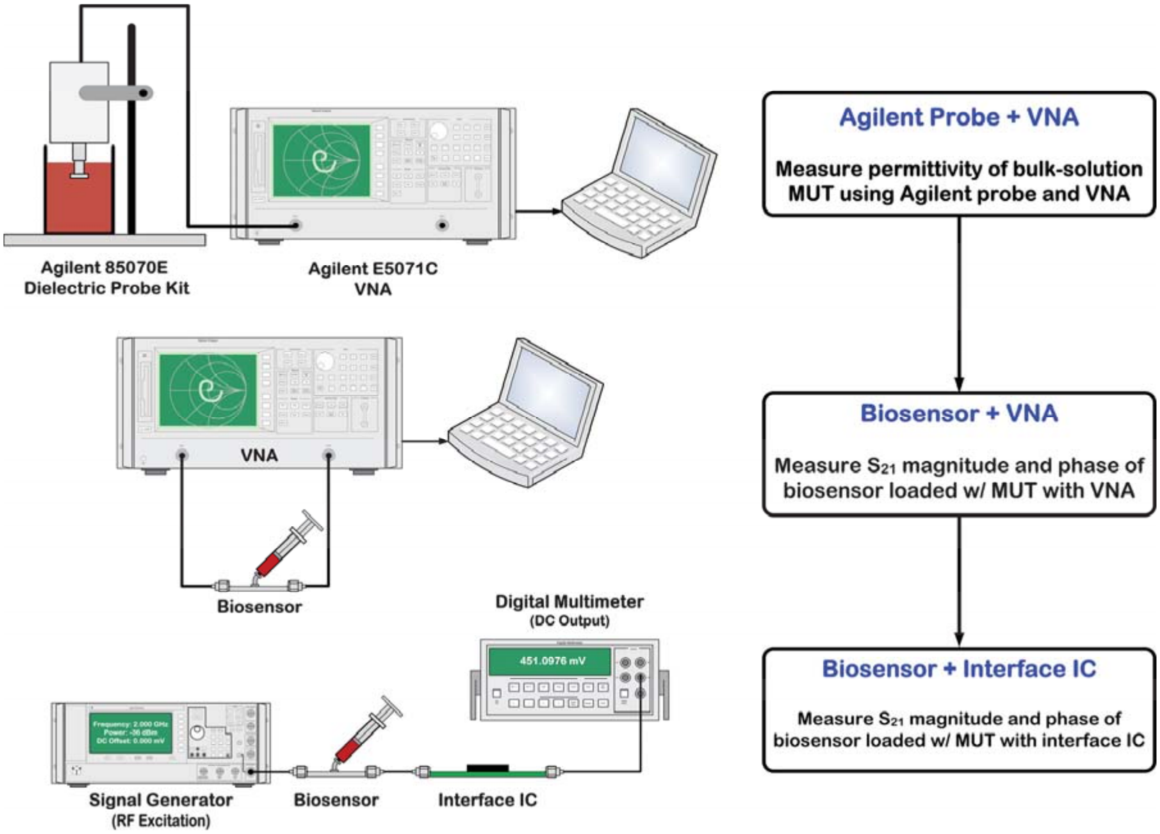

Figure 2.19: Illustration of experimental procedure for dielectric spectroscopy using Gen-1 interface IC.

Figure 2.20 depicts the measured S_{21} magnitude and phase of the sensor loaded with ethanol as the MUT and interfaced with a VNA (solid line, 14 MHz to 3 GHz) as well as the IC (blue square). The IC measurements were done at seven distinct excitation frequencies from 50 MHz (using the LBW RF module) to 3 GHz. As can be seen, the IC readings closely matched those of the VNA after a 1-point calibration to remove constant offset errors in magnitude and phase at each excitation frequency.

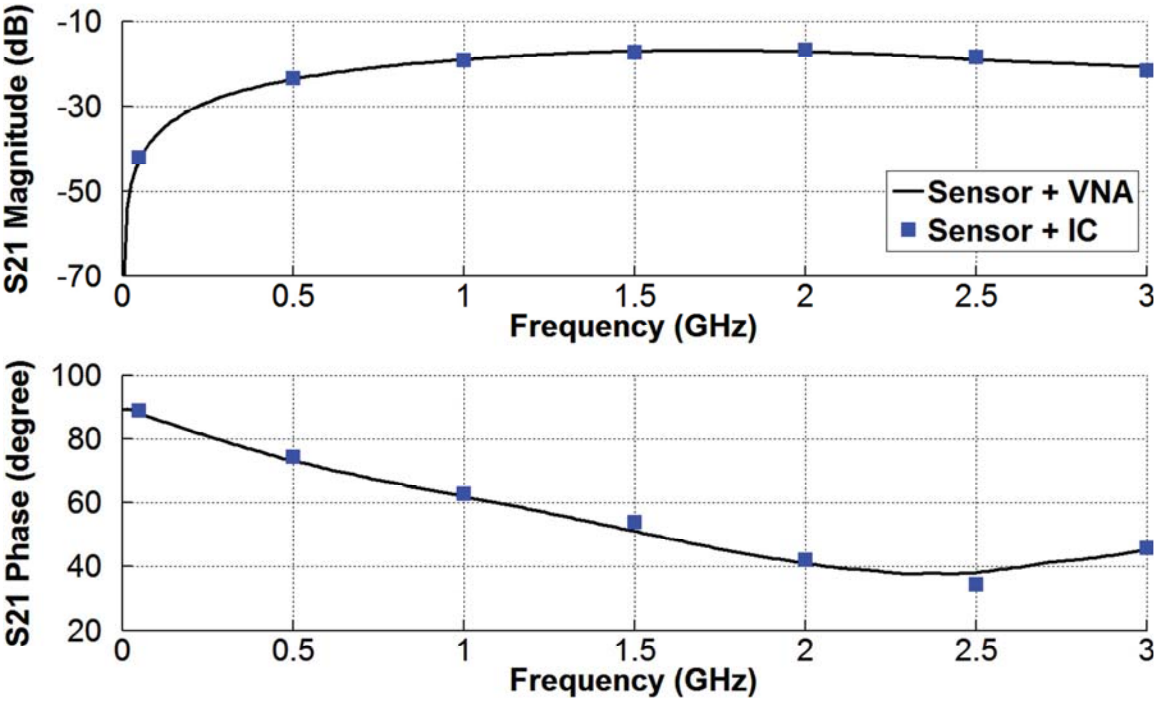

Figure 2.20: Measured S_{21} magnitude and phase vs. frequency of the DS sensor loaded with ethanol as the MUT.

A 5-point calibration procedure was developed to relate the measured S21 characteristics of the sensor to the real part of the complex dielectric permittivity (ε'_r) of the MUT. This procedure was based on a nonlinear fit of the sensor S21 characteristics loaded with reference calibration materials with known permittivity and needed to be performed only once prior to the actual measurement involving an MUT. A flowchart of the calibration procedure is shown on the left in Fig. 2.21. Reference materials were chosen to accurately characterize the sensor with low-frequency dielectric constants ($\varepsilon'_{r,LF}$) from 1 to 48. Specifically, air ($\varepsilon'_{r,LF} = 1$), dichloromethane ($\varepsilon'_{r,LF} = 10$), isopropyl alcohol($\varepsilon'_{r,LF} = 21$), methanol ($\varepsilon'_{r,LF} = 35$) and dimethyl sulfoxide ($\varepsilon'_{r,LF} = 48$) were chosen as reference calibration points. Each material was first characterized with a commercial dielectric probe kit (*Agilent* 85070E) to obtain a reference permittivity versus frequency as shown in top right of Figure 2.21. The calibration material was then loaded onto the sensor, and the S_{21} magnitude and phase of the sensor were measured with the IC at seven distinct excitation frequencies from 50 MHz to 3 GHz as shown in bottom right of Fig. 2.21. A relationship between ε'_r and S21 was then found by fitting ε'_r of the reference materials to a 3rd-order polynomial function of $x = \mathrm{Im}(S_{21}) + \beta \times \mathrm{Re}(S_{21})$ using the following equation:

$$\varepsilon'_r = p_1 \times x^3 + p_2 \times x^2 + p_3 \times x + p_4, \tag{3}$$

where $p_{1\text{-}4}$ are the fit parameters, $\mathrm{Re}(S_{21})$ and $\mathrm{Im}(S_{21})$ are the real and imaginary parts of the measured S_{21} of the loaded sensor, respectively, and β is a parameter that relates the S_{21} characteristics to the permittivity. The parameters $p_{1\text{-}4}$ were found using the least-squares method to fit the 3rd-order function to the five calibration points. To complete the calibration procedure, the unknown β factor was then found by sweeping it to obtain an optimal β that minimized the error of the least-squares fit. This procedure to find an optimal β was repeated for each RF excitation frequency set by the user for the experiment.

Figure 2.22 depicts the frequency-dependent ε'_r of ethanol extracted from the S21 measurements of the sensor interfaced with both a VNA and the IC, employing the calibration algorithm described above. Only raw S21 measurements by the IC (i.e., without 1-point calibration) were used to extract ε'_r in this step. As can be seen, dielectric readings of the "sensor + IC" showed excellent agreement with those of the "sensor + VNA", with an error < 1% up to 2 GHz. The increase in error above 2 GHz (e.g., 8.7% at 2.5 GHz) was primarily because of the increased input noise level of the IC due to the reduction in conversion gain of the HBW RF module, as well as the sensitivity of the sensor calibration algorithm to the measured S21 data when extracting small values of dielectric permittivity. Further, a bulk-solution reference measurement with *Agilent* 85070E dielectric probe kit interfaced with a VNA was also performed (solid line in Fig. 25), verifying proof-of-concept feasibility in conducting MHz-to-GHz dielectric spectroscopy with a miniaturized measurement platform using μL-sample volumes (3 μL in this case).

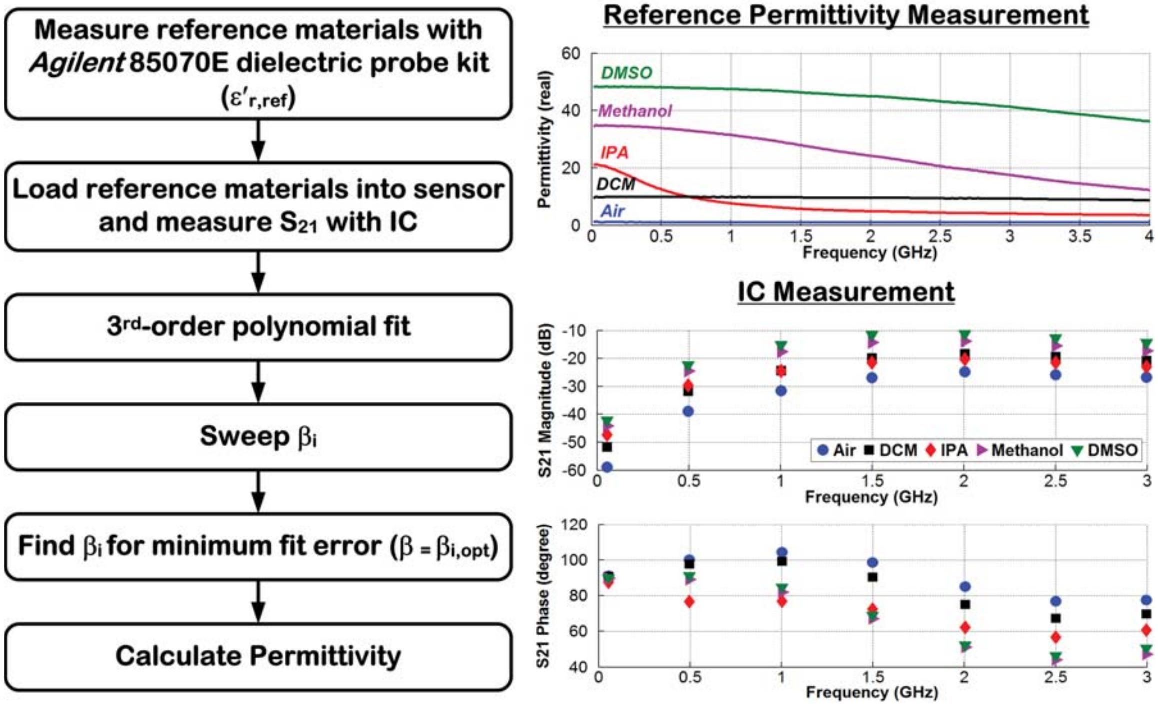

Figure 2.21: DS sensor calibration procedure to extract dielectric permittivity information from S_{21} measurements of the DS sensor by the IC.

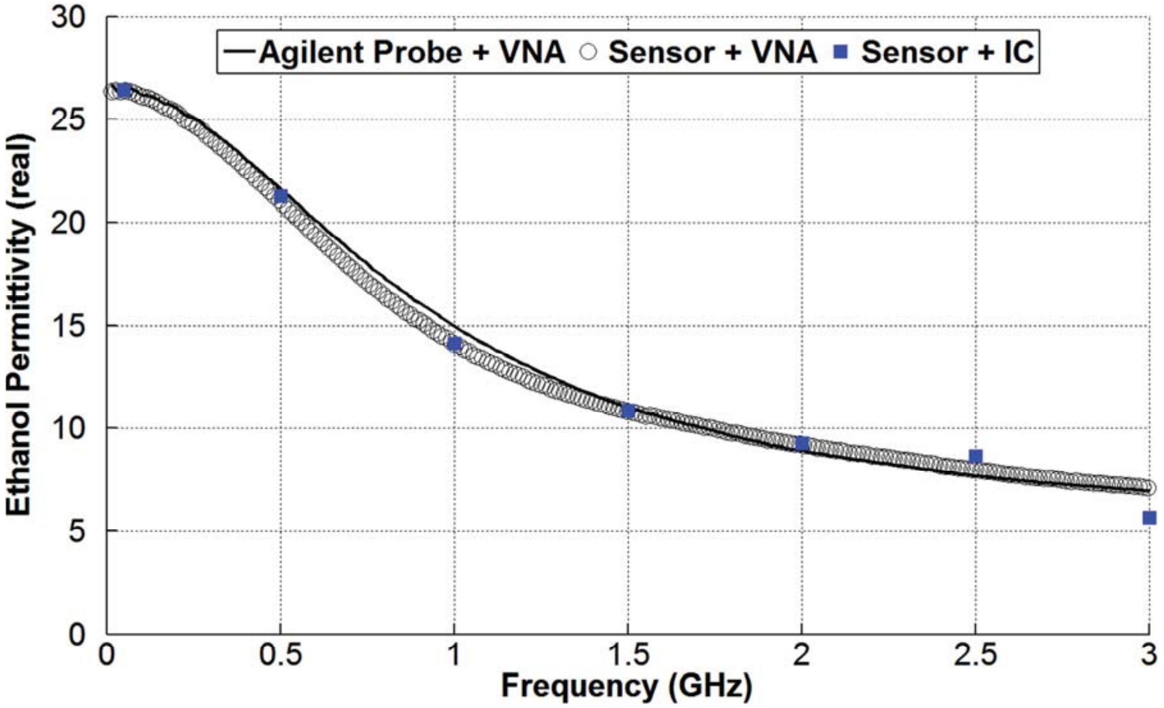

Figure 2.22: Real part of complex relative dielectric permittivity (ε'_r) vs. frequency for ethanol extracted from S21 measurements of the DS sensor. Solid line depicts the measured curve with an *Agilent* 85070E dielectric probe kit.

Table 2.1 summarizes the measured performance of the IC, and Table 2.2 compares the IC functionality and its measured performance with that in recent published works.

Table 2.1: Summary of Measured Performance Characteristics for Gen-1 IC

<table>
<tr><th colspan="5"><i>RF Module</i></th><th colspan="4"><i>LPF (LF Module)</i></th></tr>
<tr><td></td><td colspan="2"><i>HBW</i></td><td colspan="2"><i>LBW</i></td><td>DC Gain</td><td colspan="3">2.7 dB</td></tr>
<tr><td>Power Consumption</td><td colspan="2">7.1 mW</td><td colspan="2">2.1 mW</td><td>Power Consumption</td><td colspan="3">30 µW</td></tr>
<tr><td rowspan="2">RF Conversion Gain</td><td>0.5 GHz</td><td>1 GHz</td><td>10 MHz</td><td>100 MHz</td><td>3-dB Bandwidth</td><td colspan="3">1.48 kHz</td></tr>
<tr><td>25.5 dB</td><td>24.4 dB</td><td>26.5 dB</td><td>26.7 dB</td><td>Attenuation</td><td colspan="3">48.1 dB (@ 1 MHz)
50.9 dB (@ 2 MHz)</td></tr>
<tr><td rowspan="2">Noise Figure</td><td rowspan="2">6.7 dB</td><td rowspan="2">12.3 dB</td><td rowspan="2">9.3 dB</td><td rowspan="2">6.2 dB</td><td colspan="4"><i>PCM (LF Module)</i></td></tr>
<tr><td>Delay Range</td><td colspan="3">0.8–50 ns</td></tr>
<tr><td rowspan="2">1-dB Compression Point</td><td colspan="2" rowspan="2">-21 dBm
@ 1 GHz</td><td colspan="2" rowspan="2">-25 dBm
@ 100 MHz</td><td>Number of Steps</td><td colspan="3">64</td></tr>
<tr><td colspan="4"><i>Total System</i></td></tr>
<tr><td rowspan="2">Minimum Detectable Signal</td><td colspan="2" rowspan="2">-126.6 dBm
@ 1 GHz</td><td colspan="2" rowspan="2">-132.7 dBm
@ 100 MHz</td><td></td><td colspan="2"><i>HBW</i></td><td><i>LBW</i></td></tr>
<tr><td>Power Consumption</td><td colspan="2">9 mW</td><td>4 mW</td></tr>
<tr><td>Dynamic Range</td><td colspan="2">95.6 dB
@ 1 GHz</td><td colspan="2">97.7 dB
@ 100 MHz</td><td>Operation Freq.</td><td colspan="2">0.2–3 GHz</td><td>10–200 MHz</td></tr>
<tr><td colspan="5"><i>VGA 2 (IF Module)</i></td><td>Scan Rate</td><td colspan="3">958.7 s^{-1} (14b resolution)</td></tr>
<tr><td>Power Consumption</td><td colspan="4">310 µW</td><td>Total Gain (after gain cal.)</td><td colspan="2">46 dB
(0.2–1.8 GHz)</td><td>43.5 dB
(10–200 MHz)</td></tr>
<tr><td rowspan="2">Gain @ 1 MHz</td><td colspan="4" rowspan="2">14.6–21.9 dB</td><td rowspan="2">RMS Input Noise (BW = 12.8 kHz)</td><td>1 GHz</td><td>3 GHz</td><td>50 MHz</td></tr>
<tr><td>208.7 nV</td><td>2.06 µV</td><td>109.5 nV</td></tr>
<tr><td>Number of Steps</td><td colspan="4">32</td><td>Peak SNR</td><td>83.8 dB</td><td>78.2 dB</td><td>86.2 dB</td></tr>
<tr><td>3-dB Bandwidth</td><td colspan="4">4.2–8.3 MHz</td><td>Minimum Detectable Signal</td><td>-120.6 dBm</td><td>-100.7 dBm</td><td>-126.2 dBm</td></tr>
</table>

Table 2.2: Comparison of Gen-1 IC Functionality and Measured Performance

	This Work	**[2.11]**	**[2.12]**	**[2.13]**	**[2.14]**	**[2.15]**
Functionality	Measurement of dielectric permittivity					
Methodology	Amplitude/phase	CBCM	Phase shift	Oscillation freq. shift	Amplitude/phase	Amplitude/phase
Sensor Type	µfabricated center-gapped µstrip line	On-chip interdigitated	TTD cell	On-chip interdigitated	On-chip CPW t-line	Planar interdigitated
Frequency	MHz–GHz	DC only	GHz only	GHz only	GHz only	MHz–GHz
Permittivity Range	1–30	1–30	3–20	1–30	1–5	1–30
Permittivity Error	< 1% (0.05–2 GHz)	< 6%	< 4% (1–8 GHz)	< 3.5% (7–9 GHz)	< 1% (@ 20 GHz)	< 1.5% (0.5–3 GHz)
Total Power Consumption	4 mW (LBW RF) 9 mW (HBW RF)	-	-	16.5 mW	114 mW	-
Area	3 × 3 mm^2	-	36 × 45 mm^2	2.5 × 2.5 mm^2	2 × 0.6 mm^2	100 × 65 mm^2
Integration	0.35 µm RF CMOS	0.18 µm CMOS	No (PCB)	90 nm CMOS	65 nm CMOS	No (PCB)
Publication	JSSC’14	TBCAS’07	T-MTT’12	JSSC’12	IMS’13	T-MTT’13

2.4 Conclusion

Quantitative measurement of the complex dielectric permittivity of a material versus frequency (i.e., dielectric spectroscopy, or DS) is a label-free, non-destructive, real-time and fully electrical monitoring technique for investigating molecular structure and dynamics of materials using electromagnetic fields. Despite having potential for a broad range of biomedical and industrial applications, DS is still under-investigated as an analytical tool, primarily due to a dearth of small-sized, low-power and autonomous instruments for rapid broadband capturing of the relaxation times in a wide range of samples without requiring specialized measurement setups and large sample volumes. To that end, this paper reported on a broadband interface IC that measured the S21 magnitude and phase of a microfluidic sensor fabricated in a thick gold-on glass microfabrication process to realize a miniaturized measurement platform for MHz-to-GHz DS. The sensor interfaced with the IC was fully capable of differentiating among DI water, PBS, ethanol and methanol in tests conducted at 50 MHz, 500 MHz, 1 GHz and 3 GHz. Further, dielectric readings of ethanol from the sensor interfaced with the IC at five excitation frequencies in the range of 50 MHz to 2 GHz were in excellent agreement with those from using a VNA as the sensor readout.

The Gen-1 sensor calibration procedure is unable to accurately extract the imaginary part of the complex permittivity (ε_r'') from the sensor S_{21} measurements, because the voltage at the sensor output is primarily contributed by ε_r'. This in turn is because the imaginary part of the permittivity for all the organic chemicals that we have used as reference materials and MUT is always less than (or at most equal to) the real component. Further, the sensor output voltage is highly susceptible to the complex parasitic impedance contributed by the output transmission line, wire bond, PCB trace, SMA connector and cable used to interface the sensor PCB with the IC; thus Gen-1 sensor-IC interfacing strategy is not conducive to accurately detect the relatively small signal contributed by ε_r''. The next generation DS sensor is focused on reducing the complex parasitic impedance at the sensor output by developing an integrated microsystem in which the sensor is directly sit on the IC PCB, thereby enabling a more straightforward calibration algorithm and more accurate estimation of ε_r''. The next-generation IC will also incorporate frequency-synthesizer circuitry to generate the excitation signal for the sensor, allowing the user to either pre-select specific frequency points at which to conduct an experiment or sweep the excitation frequency over a specific range.

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Chapter 3

A Microfluidic-CMOS Platform with 3D Capacitive Sensor and Fully Integrated Transceiver IC for Palmtop Dielectric Spectroscopy

As described in Chapter 2, we have previously reported on the design, fabrication and measured results of the Gen-1 sensor interface IC [3.1]-[3.3] that measures the voltage transmission characteristics of a microfluidic dielectric sensor [3.4] loaded with an MUT. However, that work only featured receiver (RX) circuitry and did not have the capability of signal generation for sensor excitation as well as the LO signals for the receiver. Moreover, it only extracted the real part of permittivity due to limitations in the dielectric sensor and interfacing strategy between the sensor and RX IC. In this chapter, we present a self-sustained, miniaturized, microfluidic-CMOS platform for palmtop dielectric spectroscopy that incorporates a parallel-plate capacitive sensor [3.5] with a three-dimensional gap, floating electrode, and microfluidic channel for sample delivery, as well as a fully integrated transceiver IC [3.6] for broadband dielectric spectroscopy. The transceiver IC applies a single-tone sinusoidal RF excitation signal with MHz-to-

GHz tuning capability to the MUT-loaded sensor, and measures the sensor transmission characteristics in the voltage domain via an amplitude/phase measurement utilizing broadband frequency response analysis (bFRA) to extract the MUT complex permittivity with microliter sample volumes. The IC architecture incorporates a receiver, with similar architecture to Gen-1 interface IC to measure the amplitude/phase of the sensor response signal in MHz to GHz frequency range. It also implements a transmitter to generate the RF excitation signal for the sensor, as well as the LO signals for the receiver in a frequency range of 9.75MHz to 2.432GHz. The presented platform is fully capable of differentiating among deionized (DI) water, phosphate buffered saline (PBS), Miller Lite beer and Guinness beer in tests conducted at four different excitation frequencies in the range of 50 MHz to 2.4 GHz. Further, complex dielectric readings of PBS from the platform at six excitation frequencies in the range of 50 MHz to 2.4 GHz are in excellent agreement (RMS error <1.5% for 0.5 to 2.4 GHz) with those from a reference measurement by an Agilent 85070E dielectric probe kit interfaced with a VNA, demonstrating proof-of-concept feasibility in conducting MHz-to-GHz dielectric spectroscopy with a self-sustained palmtop platform using μL-sample volumes.

The rest of this chapter is organized as follow. Section 3.1 describes the principles of the measurement methodology and compares it to the conventional lock-in architecture. The corresponding system architecture of the transceiver IC is also presented in section 3.1. Section 3.2 discusses the circuit architecture of the major building blocks within the Transmitter part, and Section 3.3 presents electrical benchtop characterization results from a prototype fabricated in 0.35 μm RF CMOS as well as measurement results from the IC interfaced with the Gen-2 dielectric sensor [3.5]. Finally, Section 3.4 draws some conclusions from this work.

3.1 System Implementation

3.1.1 Broadband FRA Method vs. Conventional Lock-in Architecture

The main difference between bFRA method and conventional lock-in architecture is that the former uses a low IF architecture while the latter uses zero IF architecture to process the sensor response signal. In bFRA method as described in chapter 2, the sensor is excited by a single-tone sinusoidal signal, $A_0 \sin(\omega_{RF} t)$, at the desired RF frequency of ω_{RF}. Assuming that the sensor response is $A_1 \sin(\omega_{RF} t + \phi)$, the first multiplier will down-convert this signal to the IF frequency. In *I* mode of operation, this signal will be multiplied by the sinusoidal LO signal at the IF frequency, and then a lowpass filter will separate the dc component of the output from other higher-frequency terms. Therefore, the output of *I* mode is proportional to $A_1 \sin(\phi)$. In *Q* mode of operation, the IF signal will be multiplied by the quadrature-phase LO signal at the IF frequency and the dc output will be then proportional to $A_1 \cos(\phi)$. Thus, performing measurements in *I/Q* modes can measure the amplitude and phase of the sensor response signal.

The difference between bFRA method and conventional lock-in architecture in terms of noise and harmonics are shown in Fig. 3.1 and Fig. 3.2, respectively. As shown in Fig. 3.1, in the conventional lock-in architecture, the LO frequency is the same as the RF excitation frequency and therefore there is no intermediate frequency. As a result, the low frequency noises and the DC offset at the output of the mixer overlaps with the down-converted signal resulting in lower signal to noise ratio (SNR) at the output. On the other hand, in bFRA method, the first mixer down-convert the signal to the IF frequency without any overlap between low frequency noises and DC offset of the mixer output. Therefore, the following high pass filter could eliminate low frequency noises and DC offset to achieve better noise performance in the system while passing the IF signal to IF VGA stages for amplification before being down-converted by the second mixer. Note that the VGA low frequency noise and DC offset is still at different frequency compared to the IF signal and therefore not degrading the SNR. The IF signal at the input port of the second mixer is well-amplified, therefore there is no need for extra gain in second mixer and this mixer can be implemented in passive fashion with lower low frequency noises and DC offset. Therefore the SNR degradation due to the second mixer is negligible comparing to the conventional lock-in architecture. Note also the low frequency noises and DC offset of the IF VGA stages is now up-converted to IF frequency and will be filtered out by the low pass filter.

Fig. 3.2 describes the harmonic effect in both lock-in and bFRA architecture. In the conventional lock-in architecture, the fundamental LO frequency is at the same RF excitation frequency. Therefore, the mixing terms of LO and LNA output harmonics could be at DC, f_{RF}, 2 f_{RF}, etc. This means that the mixing terms of same order harmonics could be down-converted to the DC where the actual signal is down-converted results in SNR degradation due to the harmonics especially in lower RF excitation frequency in which the higher order harmonics could potentially be in the LNA bandwidth. On the other hand, in bFRA architecture, the LO frequency has a constant offset, $f_{IF,}$ regarding to the RF excitation frequency, $f_{RF.}$ Therefore the mixing terms of LO_1 and LNA output will be down-converted to $3f_{IF}$, $5f_{IF}$, etc. assuming that the LO signals are differential and have only odd harmonics. As can be seen there is no frequency overlap between the IF signal and harmonic mixing terms. Thus the harmonic mixing terms could be potentially filtered or attenuated by either the IF VGA inherent bandwidth or an additional band-pass filter on IF frequency. As a result, the remained higher order harmonics at the input of the second mixer is much smaller compared to the IF signal, making less degradation to the SNR at the system output. Thus, with careful consideration in bFRA architecture, this architecture could have better performance in terms of noise and harmonics compared to the conventional lock-in architecture. Another advantage of bFRA architecture to conventional lock-in architecture is precise *I/Q* LO generation in fixed IF frequency instead of precise I/Q generation in variable RF frequency which is quit challenging for broadband frequency range leading to have additional error in measurement due to the phase/amplitude mismatch between *I/Q* LO signals. However, the potential drawback of bFRA architecture could be the complexity of the system compared to lock-in architecture, especially in single tone RF and LO signal generation at two different frequencies with constant offset of f_{IF}. In the following section, the innovative signal generation technique for bFRA method is presented in order to reduce the system complexity and die area while maintaining the signal requirements in a wide frequency range of MHz to GHz.

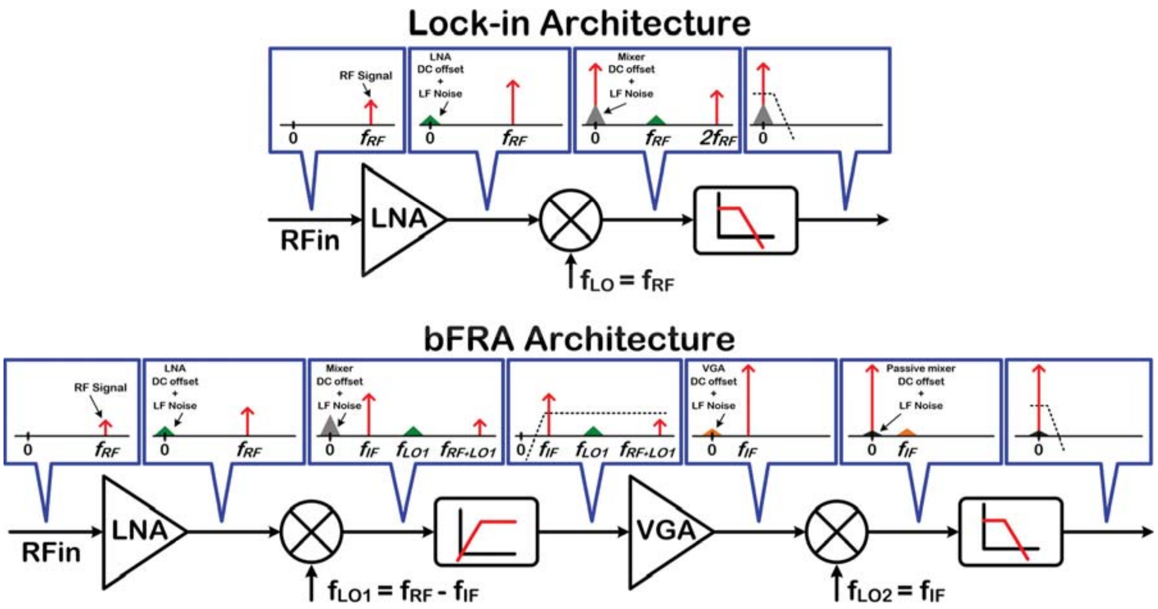

Figure 3.1: Signal flow and noise analysis for bFRA and Lock-in architectures.

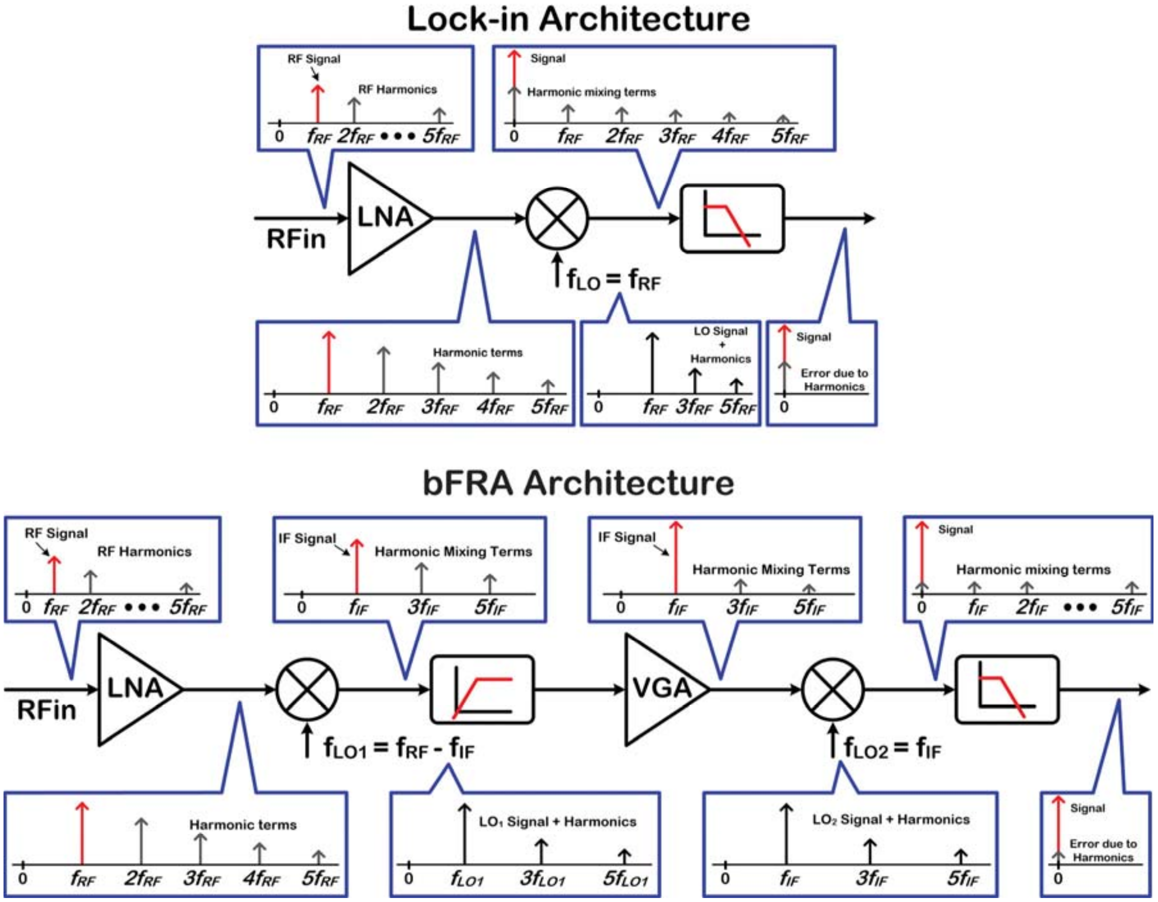

Figure 3.2: Harmonic analysis for Lock-in and bFRA architectures.

3.1.2 Platform Operation Principle

Fig. 3.3 conceptually illustrates the proposed self-sustained miniaturized DS platform that incorporates a microfabricated parallel-plate capacitive sensor with a 3D-gap, floating electrode and microfluidic channel for sample delivery, as well as a fully integrated transceiver IC. The proposed sensor is based on a parallel-plate capacitive structure with a floating electrode integrated into a microfluidic cap that delivers the MUT to the sensing area. Two planar sensing electrodes (0.6×0.6mm^2) are separated from a floating electrode (1.2×2.8mm^2) through a microfluidic channel with a height of 250um to form a three-dimensional, series-connected, capacitive sensing area with 9μL volume. A surface coating (1.5μm Parylene-N) prevents direct contact between the MUT and metal electrodes. As the MUT passes through the sensing area, the impedance (and hence voltage-transmission characteristics) of the sensor changes based on ε_r of the MUT. The transceiver IC is therefore designed to excite the sensor with a single-tone sinusoidal signal at a user-set RF excitation frequency of ω_{RF} and accurately measure the transmission characteristics of the loaded sensor using the bFRA method. The ε_r of the MUT is then extracted from the IC measurements of the sensor using a 6-point sensor calibration algorithm that runs either offline on a computer or online on low-cost embedded platforms such as the Raspberry Pi.

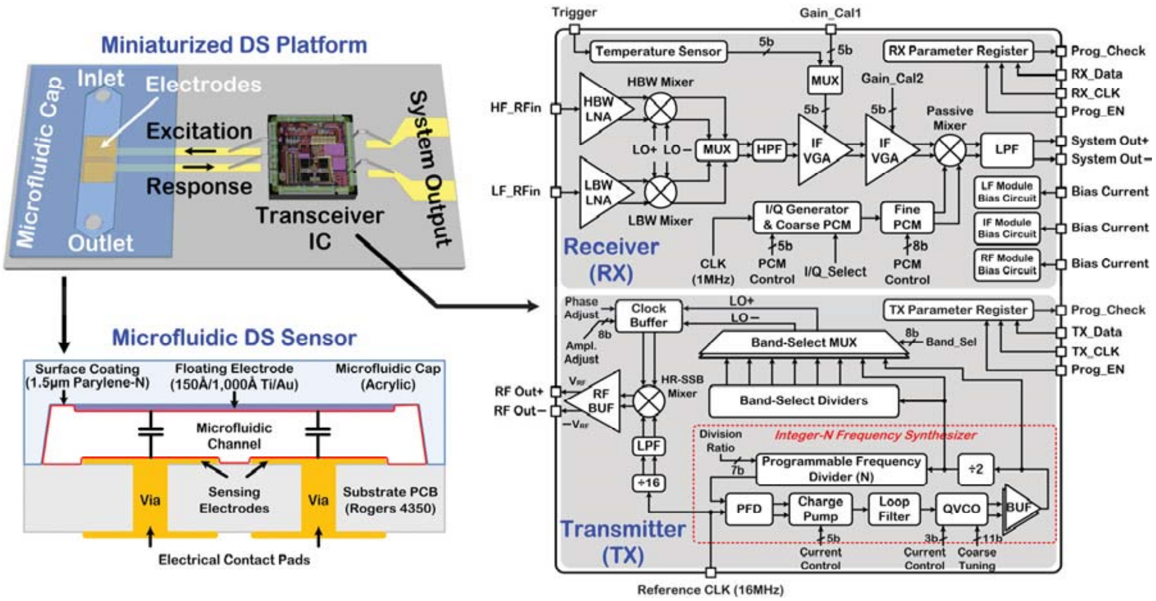

Figure 3.3: Conceptual illustration of a miniaturized measurement platform for dielectric spectroscopy as well as a cross-sectional view of the Gen-2 DS sensor and transceiver IC system architecture.

3.1.3 Transceiver IC System Architecture

As seen in Fig. 3.3 The IC architecture incorporates a RX, which utilizes broadband frequency response analysis to process the sensor response signal by first down-converting it from the RF excitation frequency to an IF of 1MHz using an LNA and active mixer, followed by down-converting the IF signal to dc using a coherent detector employing a passive HPF, two IF VGAs, a passive mixer driven by phase-calibrated I/Q signals (1MHz) and an active-RC LPF. To enable a self-sustained operation for platform portability, the IC architecture also incorporates a TX to generate the RF excitation signal for the sensor, as well as the LO signals for the RX in a frequency range of 9.75MHz to 2.432GHz.

The TX core is an integer-N frequency synthesizer operating from 1.248 to 2.432GHz, which integrates a PFD, current-programmable charge pump, loop filter, dual

GM-mode QVCO and buffer, high-frequency divide-by-2 block and programmable frequency divider with a ratio (N) from 39 to 76. The synthesizer is designed with a constant loop gain K ($\propto K_{VCO} \times I_{cp}/N$) by keeping a nearly constant VCO gain factor (K_{VCO}) and varying the charge pump current (I_{CP}) in proportion to the programmable N. This ensures stability and consistency in settling time and phase noise of the synthesizer over the entire operation frequency range. As shown in Fig. 3.4 for the transmitter frequency planning strategy, the synthesizer output directly constitutes Band 1 of the LO signal. In order to generate lower LO frequencies from 9.75MHz to 1.248GHz (that is Band 2 to Band 8), seven band-select frequency divide-by-2 blocks are used in the TX architecture, in conjunction with a wideband MUX to route the differential LO signal (I/Q) to both the RX circuitry and a programmable clock buffer. The RF excitation signal for the sensor is generated by mixing the differential LO signal (after clock buffer) with an 8-phase 1MHz signal (generated by an all-digital frequency divide-by-16 block from 16MHz external reference clock) using a harmonic-rejection SSB (HR-SSB) mixer.

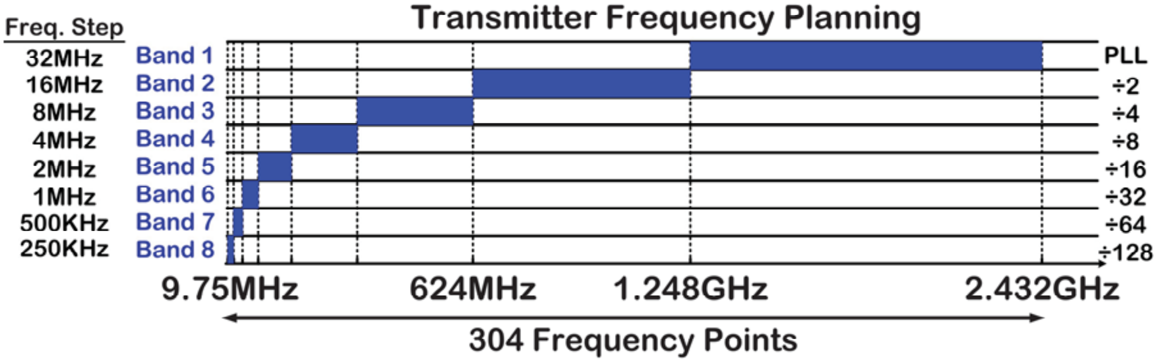

Figure 3.4: Illustration of transmitter frequency planning.

Fig. 3.5 illustrates the potential SNR degradation issue that can happen due to the 3rd- and 5th-harmonic mixing terms in RF excitation signal generation. Assuming the RF excitation signal has two mixing terms at $f_{LO}+3f_{IF}$ (3^{rd} Harmonic mixing term) and $f_{LO}-5f_{IF}$ (5^{th} Harmonic mixing term), these additional terms can be mixed with f_{LO} and down-converted to $3f_{IF}$ and $5f_{IF}$.These terms then potentially can mixed with 3^{rd} and 5^{th} order harmonics of the second LO and down-converted to DC, degrading the output SNR. In order to prevent this issue, the HR-SSB mixer rejects the image sideband as well as 3rd- and 5th-harmonic mixing terms by >35dBc, resulting in a nearly single-tone RF excitation signal for the DS sensor. The clock buffer corrects any amplitude/phase mismatch between I/Q LO signals, enhancing HR-SSB mixer performance. Further, the current-programmable clock buffer and HR-SSB mixer allow for tunability in RF excitation amplitude ($\pm V_{RF}$) to ensure that the sensor response signal lie within the input DR of the RX, given a target range for ε_r of the MUT and the desired RF excitation frequency.

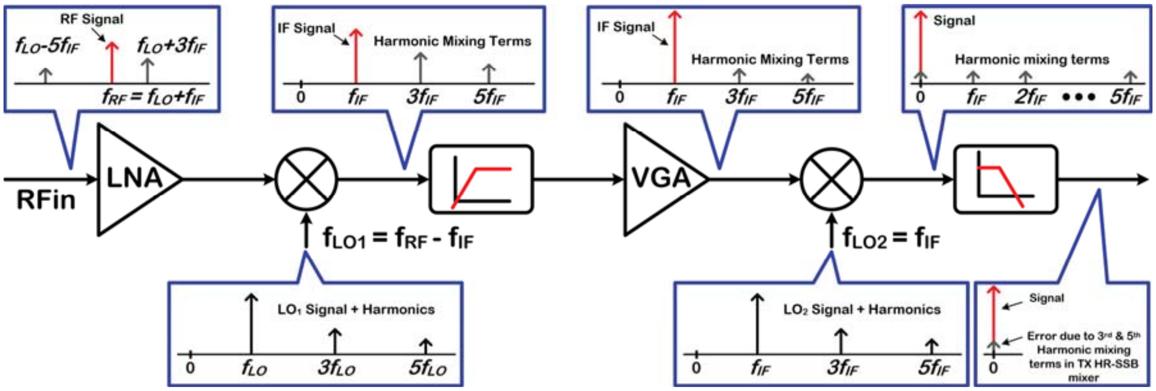

Figure 3.5: Effect of 3^{rd} and 5^{th} harmonic mixing terms in RF excitation signal on RX output SNR.

3.2 Integrated Circuit Implementation

In this section, we present the circuit architectures of the main building blocks of the Transmitter. All analog and digital circuitry are powered from 1.5 and 3.3 V, respectively. We have previously described detailed information about the circuit architecture and performance characterization of the receiver in chapter 2.

3.2.1 3rd-order Type-II Integer-N Frequency Synthesizer

Fig. 3.6 depicts the block diagram of the third-order type-II integer-N frequency synthesizer along with design parameters for each block shown in table 3.1. The PLL loop bandwidth is an important parameter that affects the PLL phase-noise variation and loop stability. Thus, having constant loop bandwidth is important to ensure PLL performance over the entire frequency range. In third or higher order loops, the loop gain *K* is often used to model the low-pass corner of the closed-loop PLL transfer function. The open-loop transfer function of a PLL with general low-pass filter $H_{LPF}(s)$ can be described as

$$H(s) = \frac{I_{CP}K_{VCO}}{2\pi Ns}H_{LPF}(s) \tag{3.1}$$

where I_{cp} is the charge pump current, K_{vco} is the VCO gain factor and N is the frequency division ratio. For a third-order PLL, the low-pass filter transfer function can be expressed as [3.6]

$$H_{LPF}(s) = R_1C_1\left(1+\frac{1}{R_1C_1s}\right)\frac{1}{R_1C_1C_2s+C_1+C_2} \tag{3.2}$$

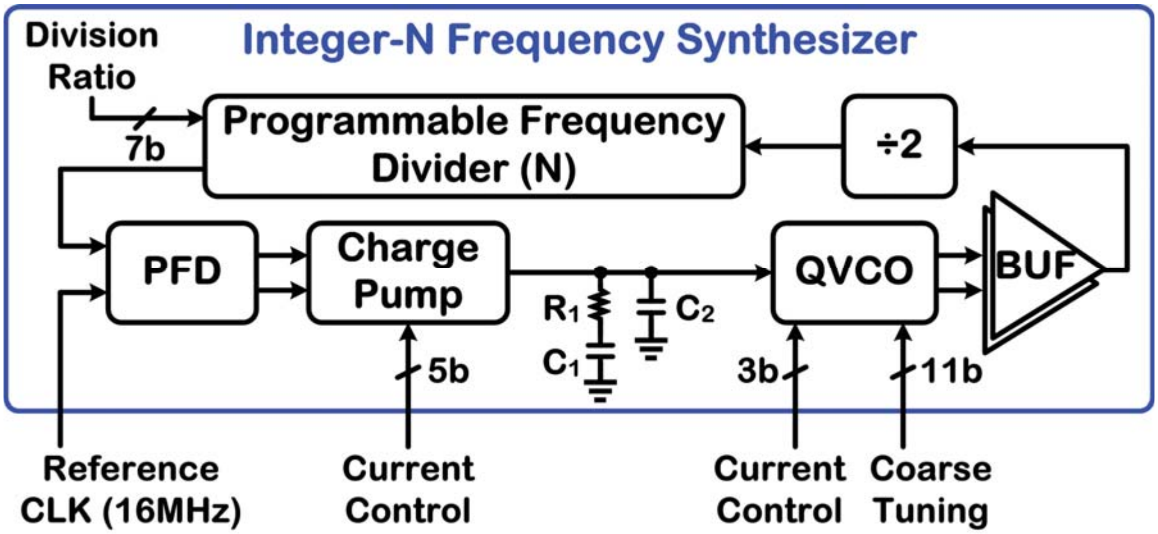

Figure 3.6: The 3rd-order type-II Integer-N frequency synthesizer architecture.

Table 3.1: Design Parameters of the 3rd-order Type-II Integer-N Frequency Synthesizer

Output Frequency Range (f_{out})	1.248 – 2.432 GHz
Reference Frequency (f_{ref})	16 MHz
Frequency Division Ratio (N)	39 – 76
Loop Bandwidth / Phase Margin	500 kHz / 64°
Charge Pump Current (I_{CP})	50 – 100 µA
Loop Filter Components	R_1 = 14 kΩ C_1 = 9.9 pF C_2 = 0.54 pF
VCO Gain (K_{VCO})	35 MHz/V

Therefore the open-loop transfer function of the third-order Type-II PLL can be rewritten as:

$$\begin{aligned} H(s) &= \frac{I_{CP}K_{VCO}R_1C_1}{2\pi Ns}\left(1+\frac{1}{R_1C_1s}\right)\frac{\frac{1}{C_1+C_2}}{\frac{R_1C_1C_2s}{C_1+C_2}+1} \\ &= \frac{I_{CP}K_{VCO}R_1}{2\pi N}\frac{C_1}{C_1+C_2}\frac{1}{s}\left(1+\frac{1}{R_1C_1s}\right)\frac{1}{\frac{R_1C_1C_2s}{C_1+C_2}+1} \end{aligned} \tag{3.3}$$

Thus, the loop gain K can be described as

$$K = \frac{I_{CP} K_{VCO} R_1}{2\pi N} \frac{C_1}{C_1 + C_2} \tag{3.4}$$

Therefore the constant loop gain can be achieved without changing the pole and zero positions and by keeping the VCO gain K_{VCO} and I_{CP}/N constant. Thus The frequency synthesizer is designed to operate from 1.248 to 2.432GHz with a constant loop gain, by keeping a nearly constant VCO gain factor of 35MHz/V and varying the charge pump current from 50 to 100uA in proportion to the programmable frequency division ratio, N, in the range of 39 to 76. Furthermore, the loop bandwidth of 500kHz as well as loop damping ratio close to one are designed based on the Gardner's stability conditions to ensure loop stability. The synthesizer reference frequency and frequency step is 16MHz and 32MHz respectively. The difference between these two frequencies is due to the high-frequency divide-by-2 block in the PLL which is implemented before the programmable frequency divider block in order to relax the bandwidth requirement for that block resulting in lower power consumption in programmable frequency divider. Note that for the DS application, permittivity variation over frequency is smooth and this frequency resolution is enough to capture the dielectric spectrum of the MUT. Also Note that the frequency resolution is 32MHz/$2^{(N-1)}$ where N is the selected band in the transmitter (e.g. 250kHz for band8).

3.2.2 Wideband *Dual-G_m* Mode Quadrature VCO

Recent wireless communication markets have demanded a transceiver that supports multiband and multimode standard in one chip. Such a wideband operation requires a voltage-controlled oscillator (VCO) with extremely wideband tuning range. Since each standard emphasizes different aspects of performance in local oscillating (LO) signals, such as phase noise, spurious tones, and power budget, an optimal design for wideband VCOs becomes challenging. Moreover, wireless communication techniques are currently employed not only in cellular devices but also in several new applications such as biochips, identifications, and miniaturized broadband dielectric spectroscopy. For these applications, wide tuning range (more than an octave) as well as the power efficiency is an important design issue. In addition, transceiver architectures like direct conversion or low IF architecture requires quadrature signals for RF signal generation or I/Q demodulation. Hence, developing a QVCO with wide tuning range and low phase noise at minimum power consumption is important for these applications [3.7].

Conventionally, ring-based VCO is considered for the wide tuning range applications [3.8]. However, to reach the stringent phase noise specifications for today's cellular applications, most transceivers use *LC*-VCOs, although its frequency tuning range is limited. Many works have been reported on expanding the tuning range of *LC*-VCOs utilizing different techniques. In [3.9]–[3.11], inductor switching technique is utilized, but it can suffer from quality factor (Q-factor) degradation as well as the increased silicon area. A more common method utilizes digitally switched capacitor bank in the *LC* tank [3.12]. However, the challenge is to overcome the tradeoff between minimum oscillation frequency which is restricted by the start-up gain of the active core and maximum oscillation frequency which is limited by the parasitic capacitance of its active core and capacitor banks. [3.13] adopted a core-switching technique to the NMOS-type VCO, however, small series switches were placed between the cores could be detrimental to the quality factor (Q-factor) and phase noise. Moreover, as the tuning range is increased, the large variation of the VCO gain (K_{VCO}) across the whole tuning range creates problems for optimal and stable PLL design that needs to be considered in the design.

This section presents a wideband NMOS-type *LC*-VCO with switchable active core transistors, 3b-programmable core current, pseudo-exponential capacitor banks and quadrature output. Programmability on active core transistor size and core current provides more than an octave tuning range as well as power optimization regarding to the target phase noise. Moreover, the QVCO coupling current is also programmable, featuring tunability in QVCO phase noise and phase error. The VCO also employs pseudo-exponential capacitor bank structure [3.14] with both coarse and fine tuning to overcome the large variation of the K_{VCO} across the whole tuning range.

3.2.2.1 Frequency-Range Analysis of A *Dual-G_m* Mode LC-VCO

Fig. 3.7 depicts an NMOS-type cross-coupled LC-VCO with switchable active core. In this architecture, VCO has two modes of operation. In *Low-G_m* mode, active core switches are open and therefore, M_{m2} cross-coupled transistors are off. In this case, the overall G_m of the active core is the same as a typical NMOS LC-VCO as

$$G_{m,Low} = g_{mm1} = \sqrt{2\mu_n C_{ox} \frac{W_{mm1}}{L_{mm1}} \frac{I_{ss}}{2}} \qquad (3.5)$$

where μ_n, C_{ox}, W_{mm1}/L_{mm1}, and I_{ss} are the mobility of electrons, the gate-oxide capacitance, the aspect ratio of M_{mm1}, and the bias current of the VCO, respectively.

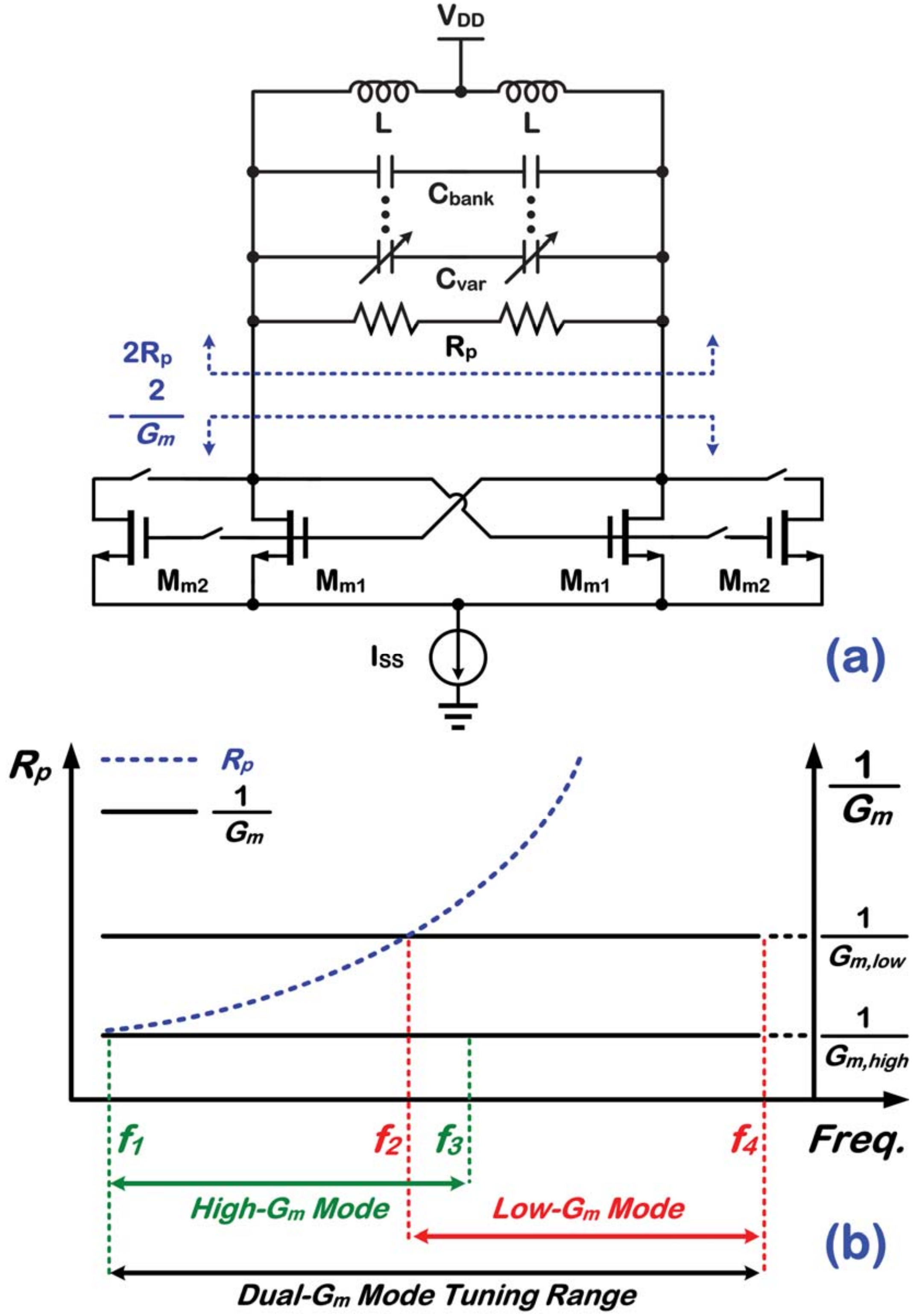

Figure 3.7: (a) Dual-G_m mode LC-VCO architecture. (b) Frequency tuning range according to different modes of operation in Dual-G_m mode VCO.

In *High-G_m* mode, active core switches are closed and therefore, M_{m2} cross-coupled transistors are in parallel with M_{m1} transistors. In this case, the overall G_m is represented as

$$G_{m,High} = g_{mm1} + g_{mm2} \tag{3.6}$$

$$= \sqrt{2\mu_n C_{ox} \frac{W_{mm1}}{L_{mm1}} \frac{I_{ss}}{2} \cdot (1+\beta)}, \quad \beta = \frac{W_{mm2}/L_{mm2}}{W_{mm1}/L_{mm1}}$$

where W_{mm2}/L_{mm2} is the aspect ratio of M_{m2} transistors. As can be seen in (3.6), the overall transconductance in *High-G_m* mode is increased by $\sqrt{1+\beta}$ compared to *Low-G_m* mode [3.13]. In order to have a sustainable oscillation, the active core of the VCO needs to compensate for the energy loss in the *LC* tank. In Fig. 3.7, the lossy component of each *LC* tank is modeled as a parallel resistor R_p. Therefore, the start-up condition of the *LC*-VCO can be determined as

$$R_p > \frac{1}{G_m} \tag{3.7}$$

R_p is mainly determined by the Q-factor of the inductor Q_L, assuming it is generally much lower than the Q-factor of other components. Therefore, R_p can be determined as

$$R_p = L\omega Q_L = \frac{L^2\omega^2}{R_s} \tag{3.8}$$

where R_s is the parasitic series resistance of the inductor. As illustrated in Fig. 3.7, the dotted line represents the quadratic relation of R_p to the oscillation frequency according to (3.8). As the oscillation frequency decreases, R_p decreases, resulting in more stringent start-up condition at lower side of tuning range. Therefore, the lower boundary of tuning range can be determined from the start-up condition (3.7) as

$$f_{osc,low} = \frac{1}{2\pi}\sqrt{\frac{R_s}{G_m L^2}} \tag{3.9}$$

Thus, from the equation (3.6) in the *High-G_m* mode of operation, the minimum oscillation frequency f_1 can be lowered by the factor of $\sqrt{1+\beta}$ for the same core current.

In general, the upper boundary of oscillation frequency is restricted by the parasitic capacitance of the *LC* tank and active core which can be determined as

$$f_{osc,high} = \frac{1}{2\pi\sqrt{L.(C_{gs} + 4C_{gd} + C_{bank,\min} + C_{\mathrm{var},\min})}} \tag{3.10}$$

where C_{gs} and C_{gd} are the parasitic gate-source and gate-drain capacitance of the core transistors, respectively. Thus, in the *High-G_m* mode, the large parasitic capacitance from the core transistors limits the maximum oscillation frequency to f_3 in Fig. 3.7. In order to increase the maximum oscillation frequency from f_3 to f_4, the size of the core transistors is minimized to lower the parasitic capacitance by switching off the M_{m2} transistors. Therefore, *Low-G_m* mode of operation extends the frequency range from f_3 to f_4. However, the lower boundary is limited to f_2 due to the start-up condition in (3.7). Thus, the combination of two modes results in an overall frequency tuning range of f_1 – f_4. In order to avoid the frequency gap between two modes of operation, β needs to be optimized in a way that f_2 is sufficiently smaller than f_3, considering process-voltage-temperature variations.

3.2.2.2 Tuning Sensitivity Analysis of a Wideband VCO

The conventional way to achieve wide tuning range and low tuning sensitivity at the same time is to use a binary-weighted switched-capacitor array bank while keeping the varactor size small in the *LC* tank. However, when the tuning range becomes wider, large variations happens in the coarse tuning (f_{step}) and fine tuning (K_{vco}) across the tuning range where f_{step} and K_{VCO} is defined as

$$K_{VCO} = \frac{\partial f_{osc}}{\partial V_{control}} = \frac{\partial f_{osc}}{\partial C} \cdot \frac{\partial C}{\partial V_{control}}, \qquad f_{step/code} = \frac{\partial f_{osc}}{\partial n} \tag{3.11}$$

in which *n* is the capacitor bank code. In [3.14], these variations for binary-weighted capacitor banks were quantified as

$$\frac{K_{VCO,\max}}{K_{VCO,\min}} = \frac{f_{step/code,\max}}{f_{step/code,\min}} = \left(\frac{f_{osc,\max}}{f_{osc,\min}} \right)^3 \tag{3.12}$$

According to (3.12), an octave tuning range would result in eight times variation in K_{VCO} and f_{step}. These large variations are not desirable for PLL employing the VCO and may cause instability or phase noise inconsistency.

The VCO oscillation frequency is determined by a simple relationship of $1/2\pi\sqrt{LC}$. In order to obtain linear coarse tuning characteristics, the pseudo exponential capacitor bank structure was previously proposed by [3.14]. In this structure, the total capacitance of capacitor bank mimics an exponential form of n^{-2}, in order to compensate the square root dependence of the VCO oscillation frequency on the total capacitance. The proposed VCO in this brief also employs this technique to reduce the variation of K_{VCO} and f_{step} across the tuning range.

3.2.2.3 Proposed VCO Circuit Architecture

Fig. 3.8 shows the proposed wideband *dual-G_m* mode *LC*-QVCO which employs three different capacitor banks and varactors to mimic the pseudo-exponential capacitor bank structure with both coarse and fine tuning to feature a nearly constant VCO gain factor of 35MHz/V. The VCO features a dual G_m-mode architecture for switching in cross-coupled transistors, M_{m2} ($3\times M_{m1}$), to overcome a tradeoff between VCO minimum frequency limited by the startup gain of its active core and VCO maximum frequency impacted by parasitic capacitances of the active core. Two identical VCOs are anti-phase coupled to generate in phase and quadrature phase differential signals. The bias current of coupling transistors M_c are 3b-programmable and designed to be 25% of the core current in order to maintain the tradeoff between phase noise and phase error in QVCOs.

Fig.3.8 also illustrates the pseudo exponential capacitor bank structure as well as core current and core size versus capacitor bank code. In order to mimic the exponential dependence of capacitor banks to capacitor bank code *n*, The VCO tuning range is divided to four sub-sections. Each capacitor bank has the binary weighted structure but with different unit capacitor size. The unit capacitors for four sub-bands are {100fF, 220fF, 320fF, 390fF}. In order to maintain the constant K_{vco} across the tuning range, three different size varactors are implemented in the VCO as well. As shown in Fig. 3.8, In sub-band 1, varactor C_{v2} (390fF) is switched in to the tank. In sub-band 2, varactors C_{v1} and C_{v2} are simultaneously in the *LC* tank (980fF). In sub-band 3 C_{v1} and C_{v2} are switched off and varactor C_{v3} (1.4pF) is switched in and finally in sub-band 4 all the varactors are switched in to the *LC* tank (2.38 pF). To minimize the cap bank switches effect on the *LC* tank Q-factor degradation, the switch sizes are scaled up in proportional to the capacitor size, resulting in constant Q factor for the capacitors. However this would increase the parasitic capacitance due to switches, limiting the maximum oscillation frequency. Therefore, switch sizes are optimized to maintain the tradeoff between Q-factor and parasitic capacitance. In addition, all the switches use 3.3V logic in order to minimize the on-resistance.

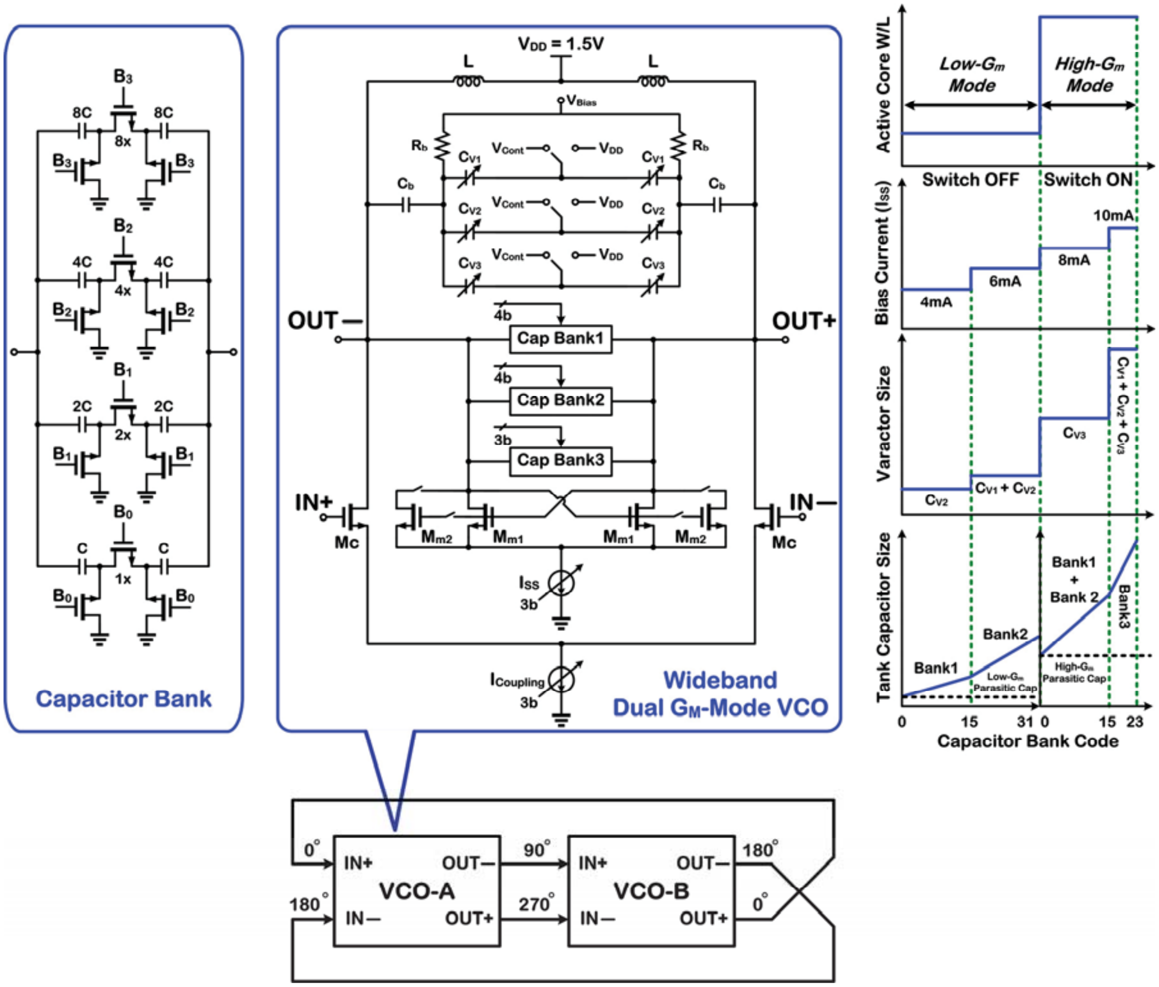

Figure 3.8: Circuit architecture of wideband dual Gm-mode QVCO.

According to the target oscillation frequency, the proposed VCO can switch between *Low-G*$_m$ mode and *High-G*$_m$ mode. In the *low-G*$_m$ mode of operation, the transmission-gate switches are open, therefore, only M_{m1} cross coupled transistors with lower parasitic capacitance are connected to the *LC* tank, resulting in the higher maximum oscillation frequency. By increasing the cap bank code from 0 to 31 in the *low-*G_m mode, the oscillation frequency as well as the quality factor will decrease as determined in (4), resulting in lower amplitude of oscillation, higher phase noise and finally VCO start-up issue. To avoid these issues, 3b-programmable core current source of the VCO features core current tuning capability, optimizing between power consumption and phase noise requirement. As shown in Fig. 3.8, the core current increased from 4mA in sub-section 1 to 6mA in sub-section 2 to maintain the phase noise requirement and further overcome the degradation of the *LC*-tank Q factor at lower frequencies. In the high-G_m mode of operation, M_{m2} cross coupled transistors (3×M_{m1}) are switched in to the active core, resulting in 2×G_m in the same bias current. In order to cover the frequency tuning range without any frequency gap between *low-*G_m and *high-*G_m modes, the capbank1 and 2 will be switched off from *LC* tank at code 0 in *High-*G_m mode. In this case, the inductance L only sees the parasitic capacitance of the capacitor banks, varactors, and active core transistors M_{m2} and M_{m1}. This ensures the 300MHz overlap frequency between the two modes to tolerate the PVT variations. In sub-section3, capbank1 and capbank2 are simultaneously switched in (from code 0 to code 15) to mimic the pseudo-exponential fashion without adding additional cap bank for this sub-section, resulting in reduced active area and parasitic capacitance. Starting the sub-section 4, the VCO bias current is also increased from 8mA to 10mA in order to avoid the decrease in oscillation amplitude and maintain the phase noise requirement by further increase the active core transconductance.

3.2.3 Other PLL Blocks

Fig. 3.9 depicts the circuit architecture of phase frequency detector (PFD) and programmable charge pump. A tri-state PFD is implemented in the PLL with a 500 ps delay, provided by inverter chain to mitigate the PFD dead zone issue. The timing mismatch of the PFD output signals (Q_A and Q_B signals) is minimized by proper design and layout as well as adding transmission gate in *Down* pulse path to replicate the delay of the inverter in *Up* pulse path. The programmable charge pump utilizes a 5bit current DAC to provide the user-programmable charge pump current, I_{CP}, in the range of 50uA to 127.5uA with 2.5uA step which is controlled by CP0 to CP4 control bits. A rail-to-rail opamp is also implemented to utilize a servo loop to suppress the effect of channel-length modulation between current mirror transistors by making V_R to follow V_C, resulting in better matching between the current mirrors in the upper and lower branch and decrease the mismatch between the charge pump sink and source currents.

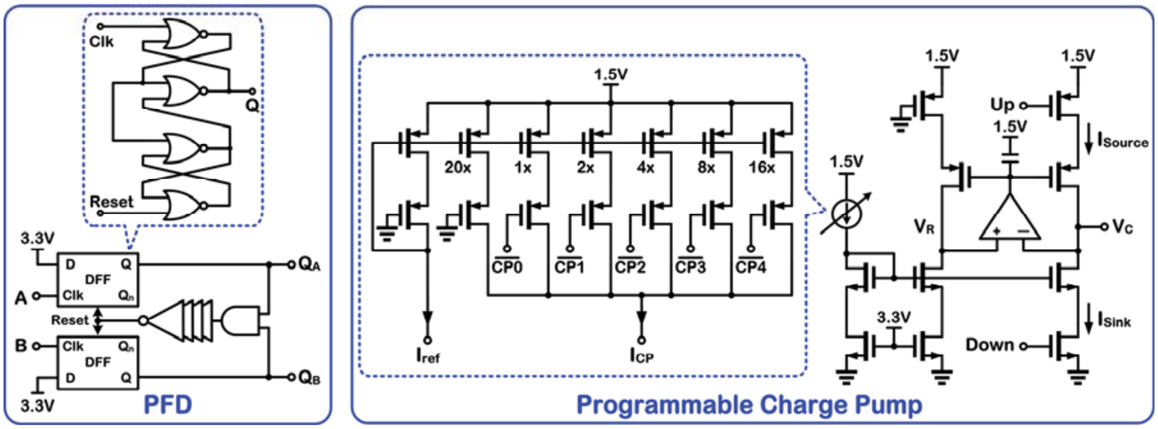

Figure 3.9: Circuit architecture of PFD and programmable charge pump.

Fig. 3.10 depicts the wide-range programmable integer frequency divider based on modular programmable prescaler architecture [3.15]. The divider consists of a cascade of 6 divide-by-2/3 cells. This architecture achieves the advantage of local feedback loops between adjacent cells which allows for power optimization regarding to the delay requirements of each loop. Moreover, the divider exploits a hybrid CMOS/CML style in order to further optimize the power consumption. The nominal voltage swing is set to 500 mV in the CML Logic cells. A 2/3 divider cell divided the frequency of the input signal by 2 or by 3, and outputs the divided clock signal to the next cell in the chain. The Mod_{in} signal becomes active once in a division cycle. At that moment, the state of the control bit P is checked, and if P = 1, the divide-by-2/3 cell swallows one extra period of the input signal resulting in division by 3. If P= 0, the cell stays in division by 2 mode. Since M divide-by-2/3 cells provide division ratios from 2^M to $2^{M+1}-1$, 6 divide by-2/3 cells are implemented to cover a 64–127 range for *N* controlled by P_0–P_5 bits. Moreover, by shunting out the last divide-by-2/3 cell (using an additional control bit P_6) the first 5 divide by-2/3 cells are used to cover ratios from 32 to 63. Therefore, the programmable division ratio *N* can cover the wide range of 32 to 127 which encompass the required range for the synthesizer (39-76).

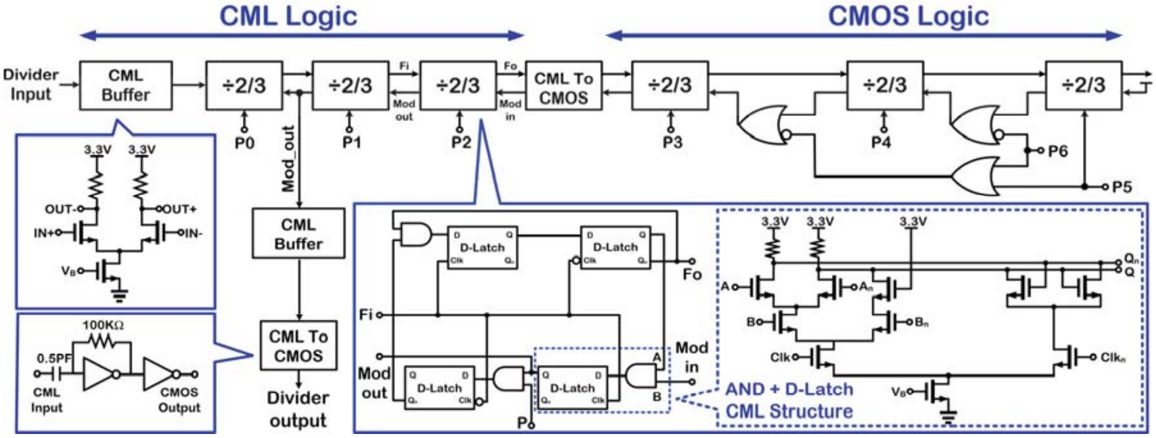

Figure 3.10: Circuit architecture of modular programmable prescaler frequency divider.

3.2.4 Band-Select Frequency Dividers

Fig. 3.11 depict the circuit architecture of the chain of seven CML band-select frequency dividers for generating the LO signal in Band 2 to Band 8 from the output of the frequency synthesizer (that is, Band 1). Each divider block is followed by a CML buffer stage in order to reduce the capacitive loading effect and maintain the required dc level for the next divider block. The quadrature outputs are connected to a replica divider to improve *I/Q* signal matching. Each divider block consists of 2 CML D flip-flops with feedback. As signal flows through the divider chain from left to right, the bandwidth requirement of each divider block is relaxed by a factor of 2. Therefore, the value of the resistive load, R_L, is doubled, and the corresponding tail current is halved to reduce the power consumption while satisfying the bandwidth requirement for each divider block.

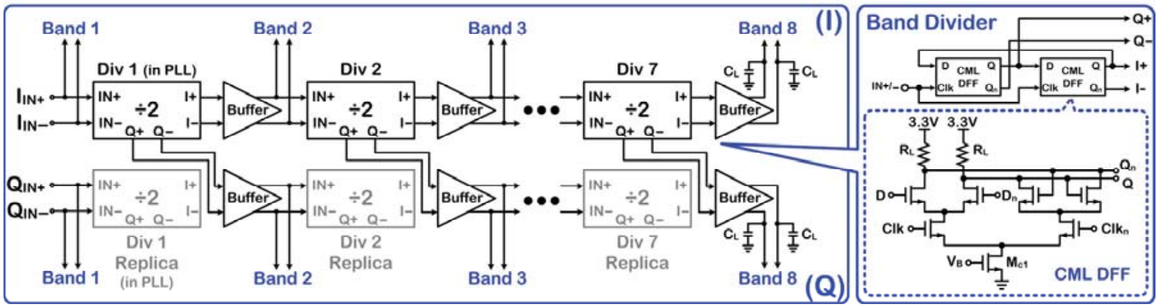

Figure 3.11: Circuit architecture of the chain of seven CML band-select frequency dividers for generating the LO signal in Band 2 to Band 8 from the output of the frequency synthesizer.

3.2.5 RF Signal Generation

Fig. 3.12 shows the circuit architecture of the HR-SSB mixer, band-select MUX, clock buffer and frequency divide-by-16 block. The wideband MUX routes one of the 8 *I/Q* LO signal bands using common-gate switching stages for enhanced signal isolation and suppression of harmonic mixing in HR-SSB mixer. The resistive load is utilized to maintain the broadband operation of MUX as well as saving areas comparing to the switchable LC tanks. Tail currents of each differential stage as well as the sizing of differential stage transistors are optimized to maintain the required bandwidth of each stage as well as the constant transconductance for all 8 differential stages resulting in constant gain for all bands.

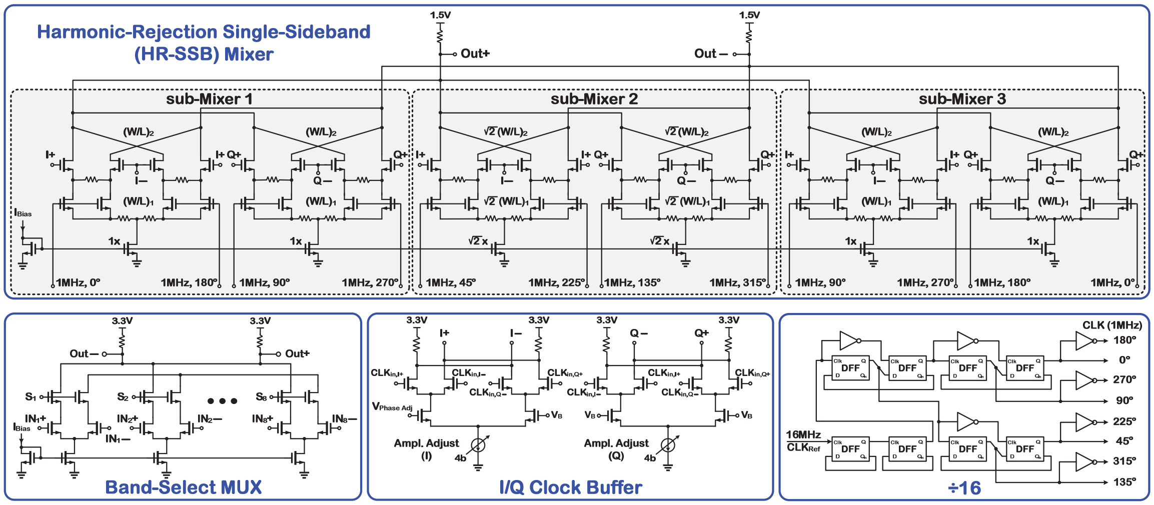

Figure 3.12: Circuit architecture of HR-SSB mixer, band-select multiplexer, programmable I/Q clock buffer and all-digital frequency divide-by-16 block.

To generate the quadrature LO inputs required for HR-SSB mixer, anti-phase-coupled quadrature VCO is incorporated. However, this commonly used topology inevitably introduces finite phase and gain errors due to the device mismatches and routing asymmetries. Such imperfections result in sidebands in the SSB mixer output degrading the RF excitation signal spectrum. In order to overcome this issue, an interpolating clock buffer with adjustable gain and phase is employed here to counterbalance the *I/Q* amplitude and phase mismatches. The clock buffer uses two identical stages driven by selected *I/Q* LO signals to generate two *I/Q* LO outputs with phases of 45° and 135°. Any phase error between the *I/Q* LO outputs in the range of ±45°

is compensated via *VPhase Adj* by steering the tail current and altering weighting factors of the two inputs. Any amplitude error is also corrected by adjusting the 4b-programmable current of the two stages. An 8-phase 1MHz signal is generated by an all-digital frequency divide-by-16 block from an external reference clock at 16MHz.To further suppress the 3rd and 5th order harmonics of the 1MHz signal, The 8-phase 1MHz signals are passively low pass filtered before to the HR-SSB mixer.

The HR-SSB mixer incorporates three SSB sub-mixers with a common resistive load to sum the output current signal in sub-mixer #2 with that from sub-mixers #1 and #3 with relative phase shifts of ±45° and scaling of $\sqrt{2}$. This is implemented by scaling the transconductance of the sub-mixer #2. The tail currents of SSB-sub mixers are tunable by changing the reference current, I_{bias}, making it possible to tune the amplitude of mixer output signal. The performance of each SSB sub-mixer is heavily influenced by the mismatches between the two input paths as well as the nonlinearities in the SSB mixer itself. While the mismatches create image sidebands, the nonlinearities produce spurs all over the spectrum due to cross-products of the input harmonics. In order to overcome the nonlinearity problem, each SSB sub-mixer has resistive source-degeneration at both input ports to further enhance linearity. Here, R1–R4 linearize the LO port switches with no voltage headroom consumption, splitting the RF port into 8 Transistors. These transistors also get degenerated by R5-R8 to further improve the mixer linearity. The harmonic rejection ratio for the HR-SSB mixer depends on the amplitude and phase matching of the input signals as well as the gain matching of the SSB sub-mixers and can be derived as [3.16]

$$HRM_3 \approx \frac{1}{9}\frac{2\Delta^2 + 2(3\theta)^2}{\left(2\sqrt{2}\right)^2}$$

$$HRM_5 \approx \frac{1}{25}\frac{2\Delta^2 + 2(5\theta)^2}{\left(2\sqrt{2}\right)^2}$$

where Δ and θ are the gain and phase mismatch, respectively. Based on that, 35dB of rejection requires less than1-degree phase error and 1% gain error which can be provided by programmable clock buffer calibration.

3.3 Measurement Results

A prototype chip was fabricated in AMS 0.35 μm 2P/4M RF CMOS, measuring 3.3 mm × 3.3 mm including the bonding pads. Fig. 3.13 shows a photograph of the miniaturized platform and a close-up view of its sensor prototype along with a microphotograph of the fabricated chip. This section presents the measurement results from electrical characterization of the IC as well as from DS studies using the IC interfaced with a microfabricated parallel-plate 3D capacitive sensor from [3.5].

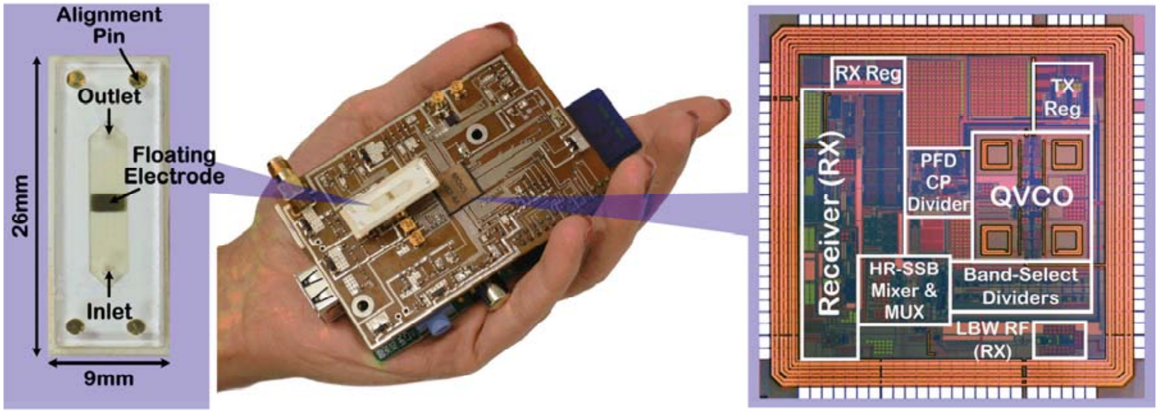

Figure 3.13: Photograph of the microfluidic-CMOS platform along with its microfabricated microfluidic sensor prototype and die micrograph of the transceiver IC.

3.3.1 Electrical Characterization

Fig. 3.14 shows the measured VCO frequency tuning range in *Low-G_m* mode, when the core switches are open, and in *High-G_m* mode, when the secondary core is switched in. The maximum achievable frequency range when all the capacitor banks are off is 2.455GHz. The VCO in High-G_m mode ranged from 1.232 to 1.975GHz. In this mode, the lower boundary is extended more than 440MHz due to the increased start-up gain, resulting in more than an octave overall tuning range which is critical for LO signal generation using division techniques.

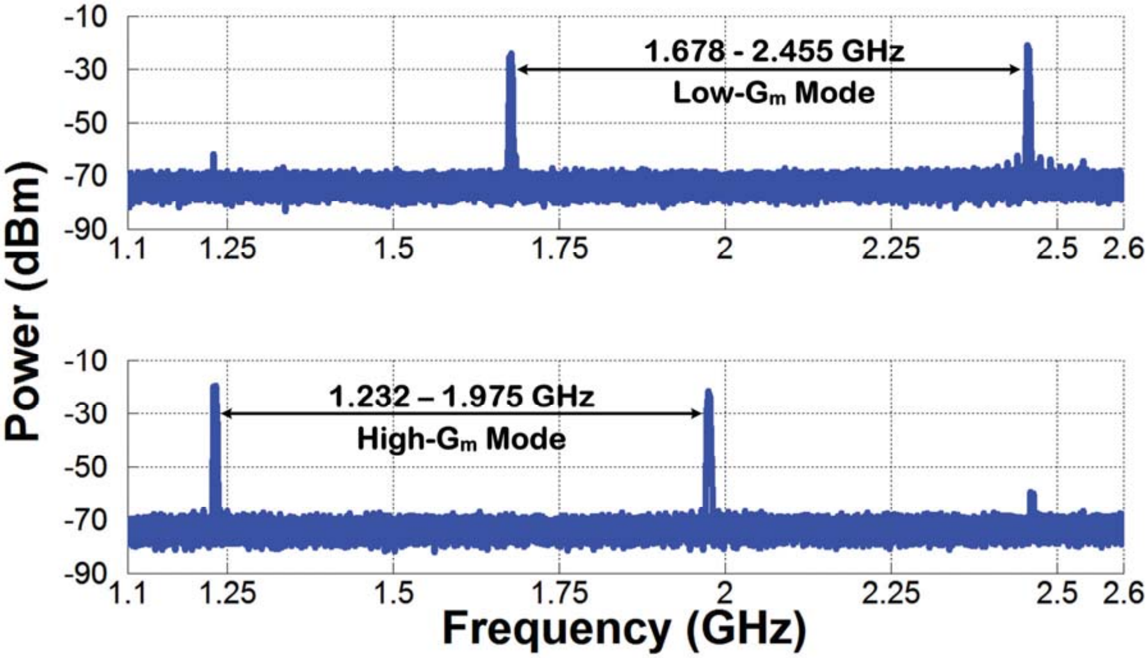

Figure 3.14: Measured VCO frequency tuning range in Low-Gm and High-Gm mode.

Fig. 3.15 shows the measured tuning characteristics of the VCO in both modes. As can be seen, there is no blind zone between *f-V* curves and the overlap between two modes is ~300MHz in order to cover the PVT variation.

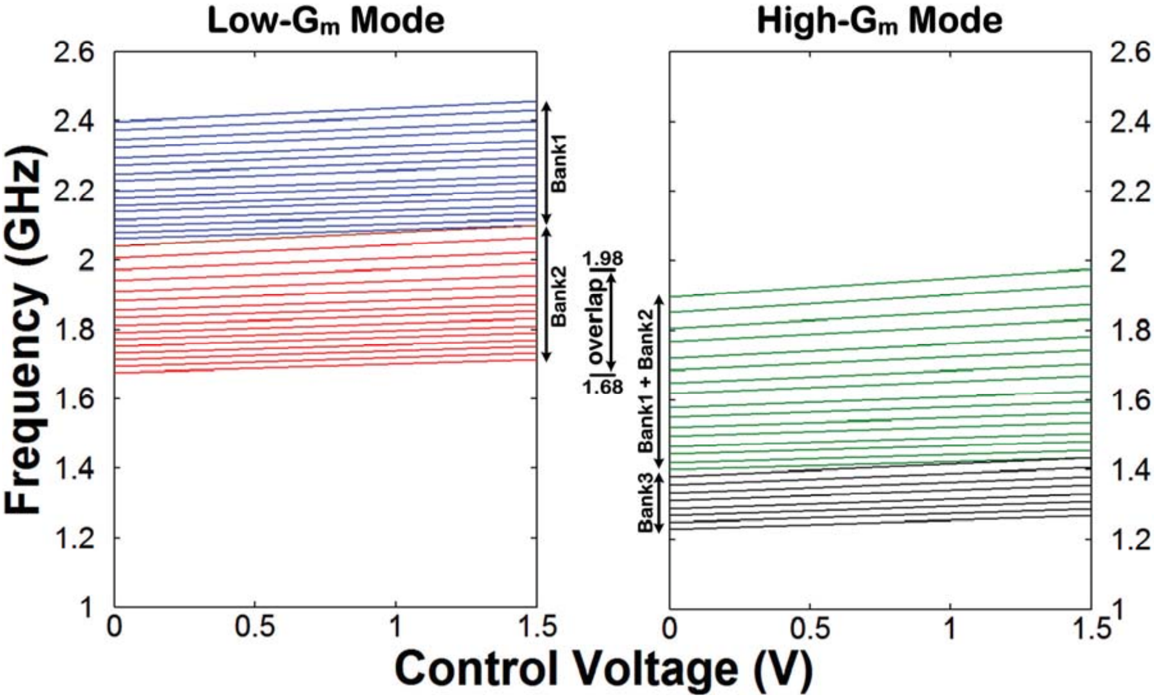

Figure 3.15: Measured tuning characteristics of Dual-Gm mode VCO.

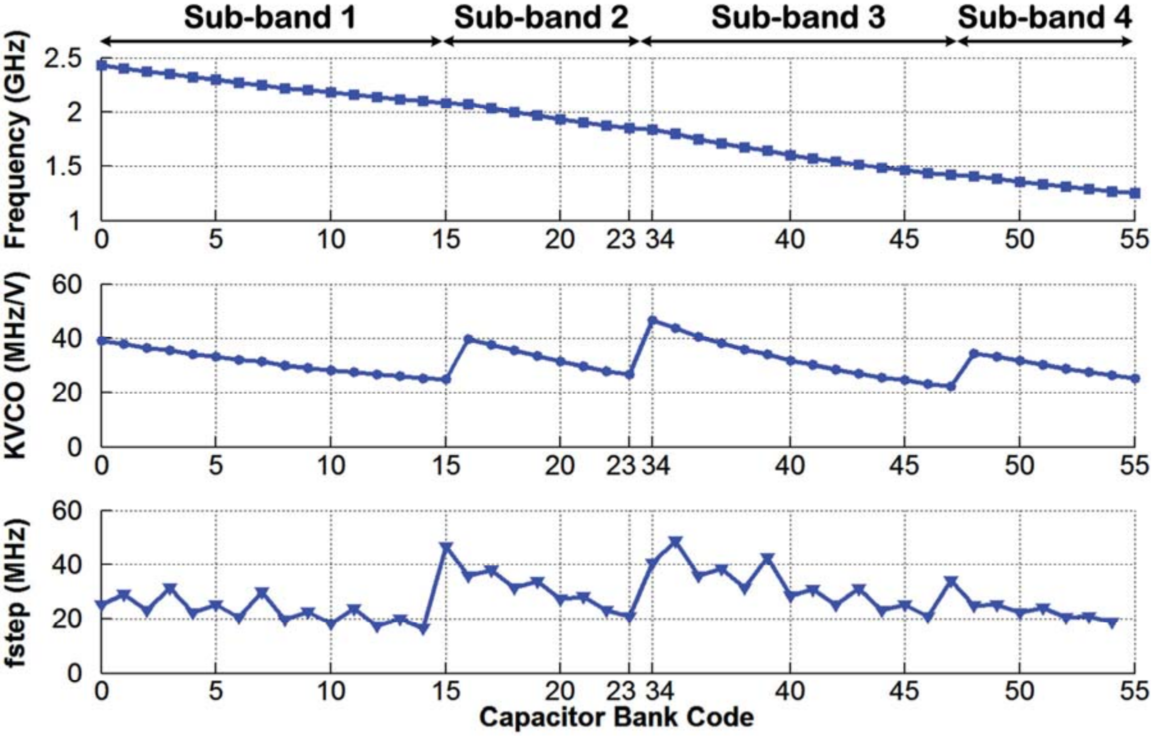

Figure 3.16: Measured frequency tuning characteristic of VCO at a fixed V_C = 0.75 V, frequency step (f_{step}) and VCO gain (K_{VCO}) versus capacitor bank code.

Fig. 3.16 depicts the measured plots for the VCO oscillation frequency, K_{vco} , and f_{step} versus the capacitor bank code. The measured K_{vco} and f_{step} vary between 22.4 – 46.6MHz/V and 16.5 – 46.5MHz, respectively, which reduced from 8 times variation for an octave tuning range in conventional VCO architecture to about 2 times (×4 variation reduction).

Fig. 3.17 shows the measured phase noise at maximum and minimum VCO oscillation frequency. The measured phase noise at offset frequency of 1MHz is -121.5dBc/Hz and -119.5 dBc/Hz at 2.455GHz and 1.232GHz, respectively.

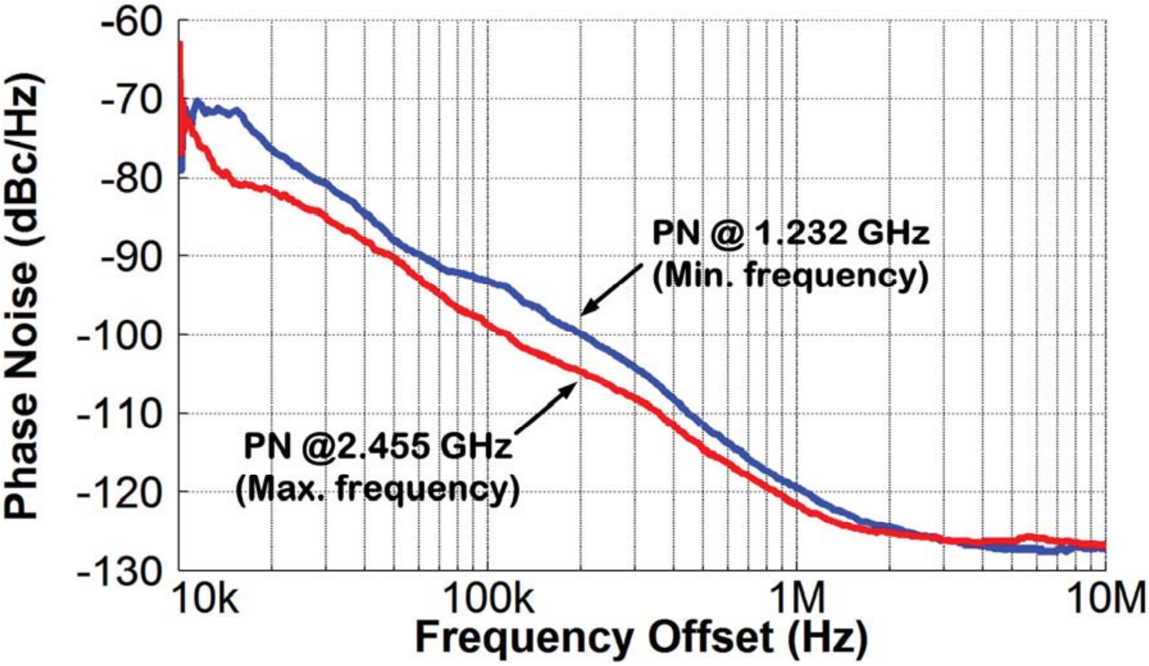

Figure 3.17: Measured VCO phase noise at maximum & minimum oscillation frequency.

Table 3.2 compares the proposed *dual*-G_m mode VCO with other recent reconfigurable LC-VCOs.

Table 3.2: Comparison with Reconfigurable *LC*-VCOs

	This Work	[3.13]	[3.14]	[3.17]	[3.18]
Process	0.35μm CMOS	65nm CMOS	0.18μm CMOS	65nm CMOS	65nm CMOS
Topology	NMOS Core-G_m Switching	NMOS Core Switching	NMOS	NMOS Core Switching	NMOS/CMOS Core Switching
FTR Range (Hz)	66.3% 1.232 – 2.455G	41.1% 3.36 – 5.1G	66.7% 0.924 – 1.85G	40% 3.0 – 4.5G	32.2% 6.5 – 9G
PN (dBc/Hz) @ $\Delta f/f_{osc}$	-121.5 @ 1M/2.455G	-123.1 @ 1M/4.21G	-127.1 @ 1M/1.752G	-137.5 @ 3M/3.3G	-129.3 @ 1M/3.9G
P_{DC} (mW)	6 - 15	8.7	10.8	15	9
FOMT*	197.9	198.4	197.9	198.5	195.7

* $FOMT = -PN(f_{offset}) + 20\log\frac{f_{osc}}{f_{offset}} - 10\log\frac{P_{DC}}{1mW} + 20\log\frac{FTR}{10}$

Figure 3.18 shows the measured frequency spectrum of the LO signals for the maximum and minimum frequency of all seven bands generated by the transmitter. As can be seen, the measured LO frequency range is 9.75MHz – 2.432GHz. The frequency step is 32MHz in band1 and divides by 2 in each following bands, leading to 250kHz frequency resolution in band8. Therefore the LO signal generated by transmitter can cover the entire frequency range with 304 frequency points (38 frequency points in each band).

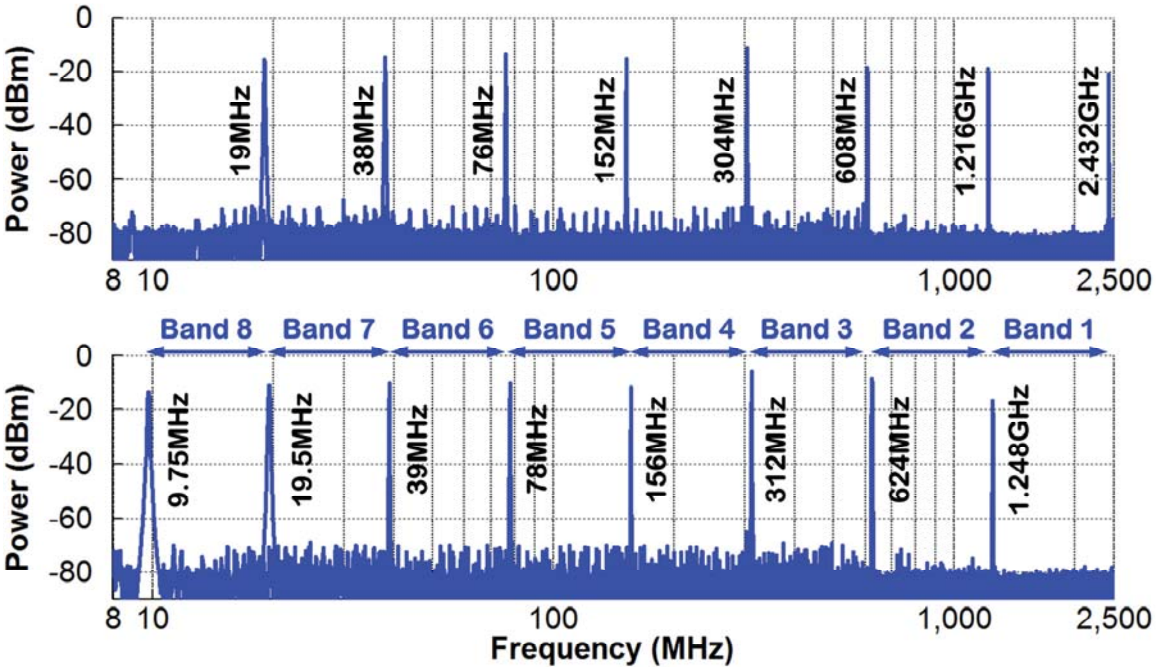

Figure 3.18: Measured frequency spectrum of the LO signals for the maximum and minimum frequency of all seven bands generated by the transmitter.

The left plots in Fig. 3.19 depict the measured frequency spectrum of the LO and RF signals, for the maximum sensor excitation frequency generated by the transmitter. In this case, the PLL is locked at its maximum operation frequency of 2.432GHz, and Band 1 is selected to generate an LO signal at the same frequency. The measured LO spur rejection at 16MHz offset (reference frequency) was 51dBc. The HR-SSB mixer generated the RF excitation signal at 2.433GHz and rejected the image sideband as well as 3rd- and 5th-harmonic mixing terms by 35.3, 47.3, and 36.8dBc respectively. The right plot shows the same measurement for the minimum sensor excitation frequency of 8.75MHz in which the PLL is locked at its minimum operation frequency of 1.248GHz and Band 8 is selected to generate an LO signal at 9.75MHz. In this case, the HR-SSB mixer was able to reject the image sideband as well as 3rd- and 5th-harmonic mixing terms by 53.7, 42.8, and 38.3dBc respectively. The measured LO phase noise for maximum and minimum LO frequency was -107dBc/Hz at 1MHz and 10 kHz offsets, respectively.

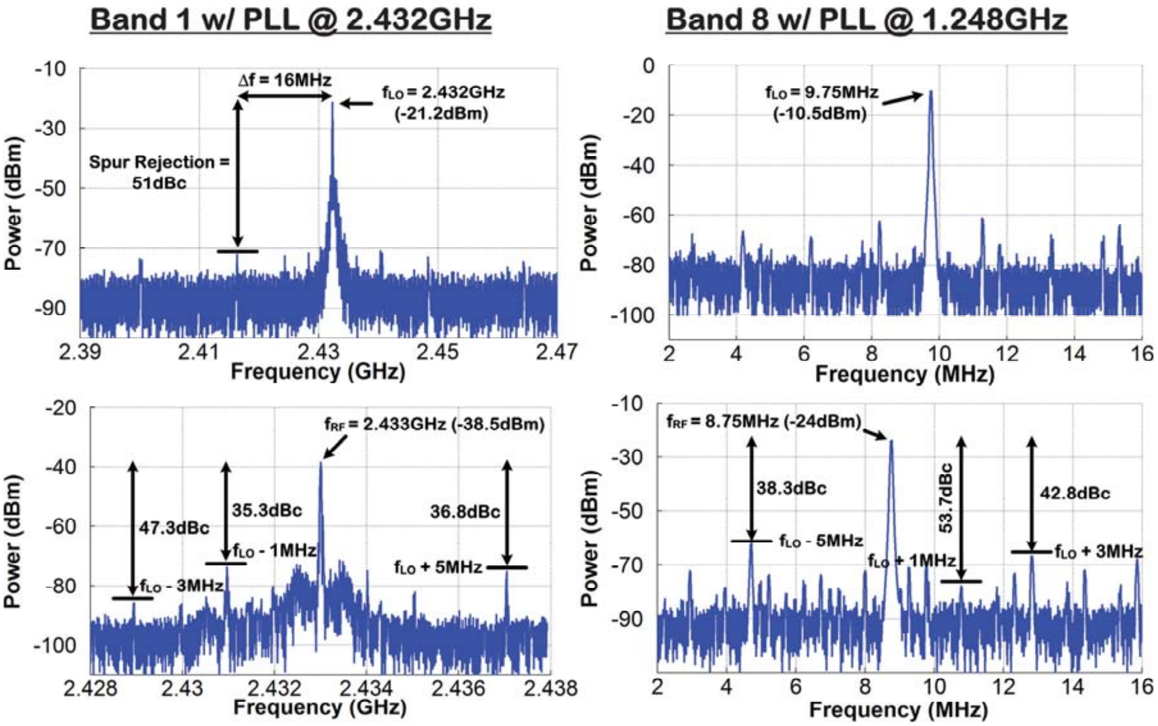

Figure 3.19: Measured frequency spectrum of the LO and RF signals for maximum (left) and minimum (right) sensor excitation frequencies generated by the TX.

Figure 3.20 shows the measured dc receiver output versus the RF input phase in both *I* and *Q* modes of system operation. The RF input power and frequency were -40dBm and 2.433GHz, respectively. In order to enable a phase sweep, the RF signal was applied to the receiver from an external signal generator, whereas the LO signal was generated on-chip by the transmitter and synchronized with the RF signal generator via the 16MHz external reference clock. As can be seen, after phase calibration by the PCM to remove any phase offset (calibration code of 00001 11001011 for f_{RF} of 2.433 GHz), the dc receiver outputs in *I* and *Q* modes were proportional to $\sin(\varphi)$ and $\cos(\phi)$, respectively, as discussed in Section II.A, demonstrating correct functionality of the receiver part while using on-chip generated LO signals.

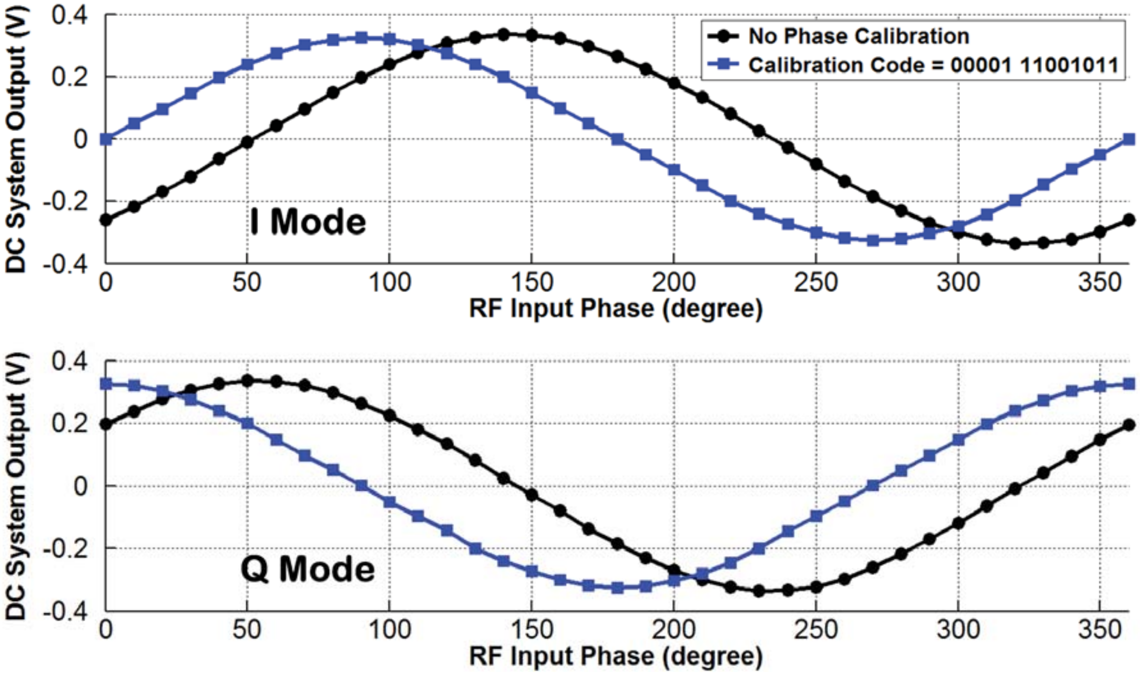

Figure 3.20: Measured dc system output vs. RF input phase in I (top) and Q (bottom) mode of operation. The RF input power and frequency were -40dBm and 2.433GHz, respectively. In order to enable a phase sweep, the RF signal was applied to the RX from an external signal generator, whereas the LO signal was generated on-chip by the TX and synchronized with the RF signal generator via the 16MHz external reference clock.

Figure 3.21 depicts the measured phase-noise at frequency offsets of 100 kHz and 1 MHz for six different PLL oscillation frequencies ranging from 1.248 to 2.432 GHz. The phase-noise curves have a flat characteristic across the entire frequency range. The variation is less than 2 dB in 100kHz offset frequency and 1 dB in 1MHz offset. It is also shown that the closed loop has an average 3-dB bandwidth of 391 kHz and the bandwidth variation is less than 13%.

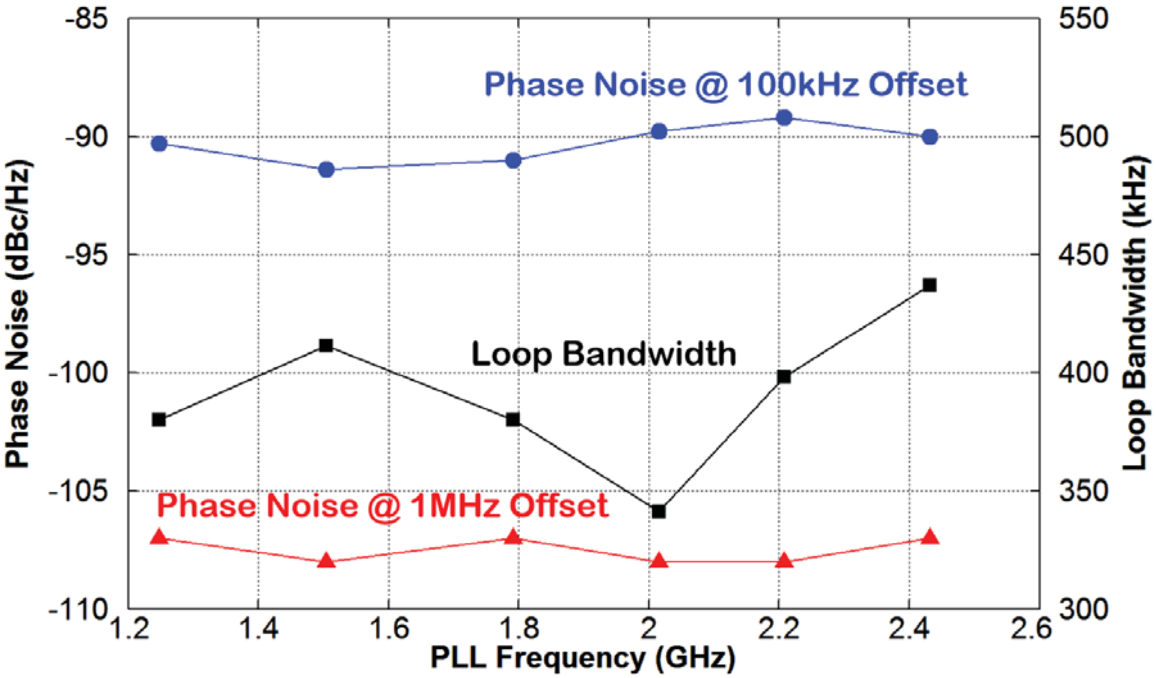

Figure 3.21: Measured phase-noise at frequency offsets of 100 kHz and 1 MHz for six different PLL oscillation frequencies ranging from 1.248 to 2.432 GHz along with measured 3dB closed-loop bandwidth.

Figure 3.22 shows the output spectra of RF excitation signal at 2.433GHz generated by HR-SSB mixer with and without clock buffer calibration. As can be seen, regarding to *I/Q* finite phase and amplitude error caused by device mismatches and routing asymmetries, the HR-SSB mixer attenuates the image sideband by 12dBc. However, after phase and amplitude calibration being performed by the clock buffer, the HR-SSB mixer attenuates the image sideband by 50.2dBc. Therefore, clock buffer calibration improved the image sideband rejection by more than 38.2 dB at 2.433 GHz RF excitation frequency.

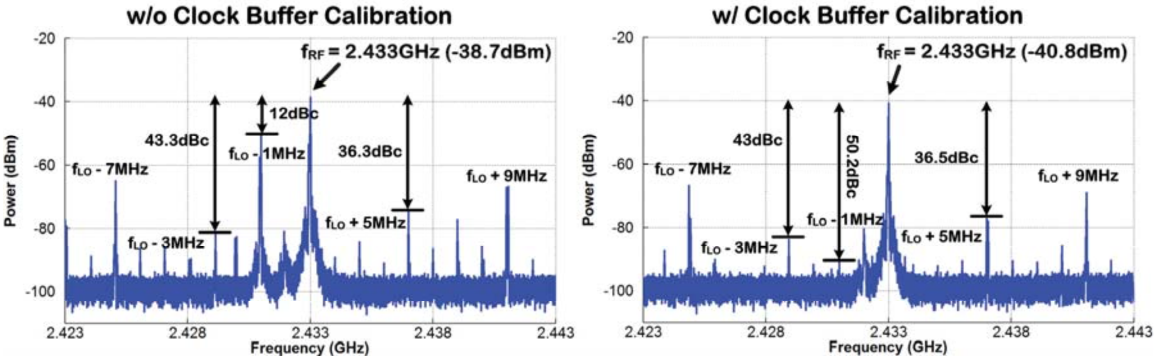

Figure 3.22: The measured output spectra of RF excitation signal at 2.433GHz generated by HR-SSB mixer with and without clock buffer calibration.

3.3.2 DS Sensor + Transceiver IC

The Transceiver IC was interfaced with the microfluidic three dimensional capacitive sensor from [3.5], and various experiments were performed. The ultimate goal was to extract the frequency-dependent complex dielectric permittivity of water-based solutions and thereby demonstrate proof-of-concept feasibility in miniaturization of the self-sustained broadband dielectric spectroscopy platform.

Figure 3.23 shows the measured output power of RF excitation signal generated by the TRX IC as well as the input referred power at the receiver input port for six different RF excitation frequencies from 50MHz to 2.433GHz when the DS sensor is loaded with DI water as a MUT. Fig 3.23 also shows the S21 magnitude of the DI water in the sensor channel versus frequency measured by VNA in order to show the attenuation over the channel for different RF excitation frequency. As can be seen, the RF excitation power for each excitation frequency is tuned (-20.4dBm @ 10MHz, -38.5dBm @ 2.433GHz) to ensure that the sensor response signal lie within the input DR of the RX

(RX maximum input power = -31dBm for HBW, -35dBm for LBW [3.3]), given a target range for ε_r of the MUT and the desired RF excitation frequency.

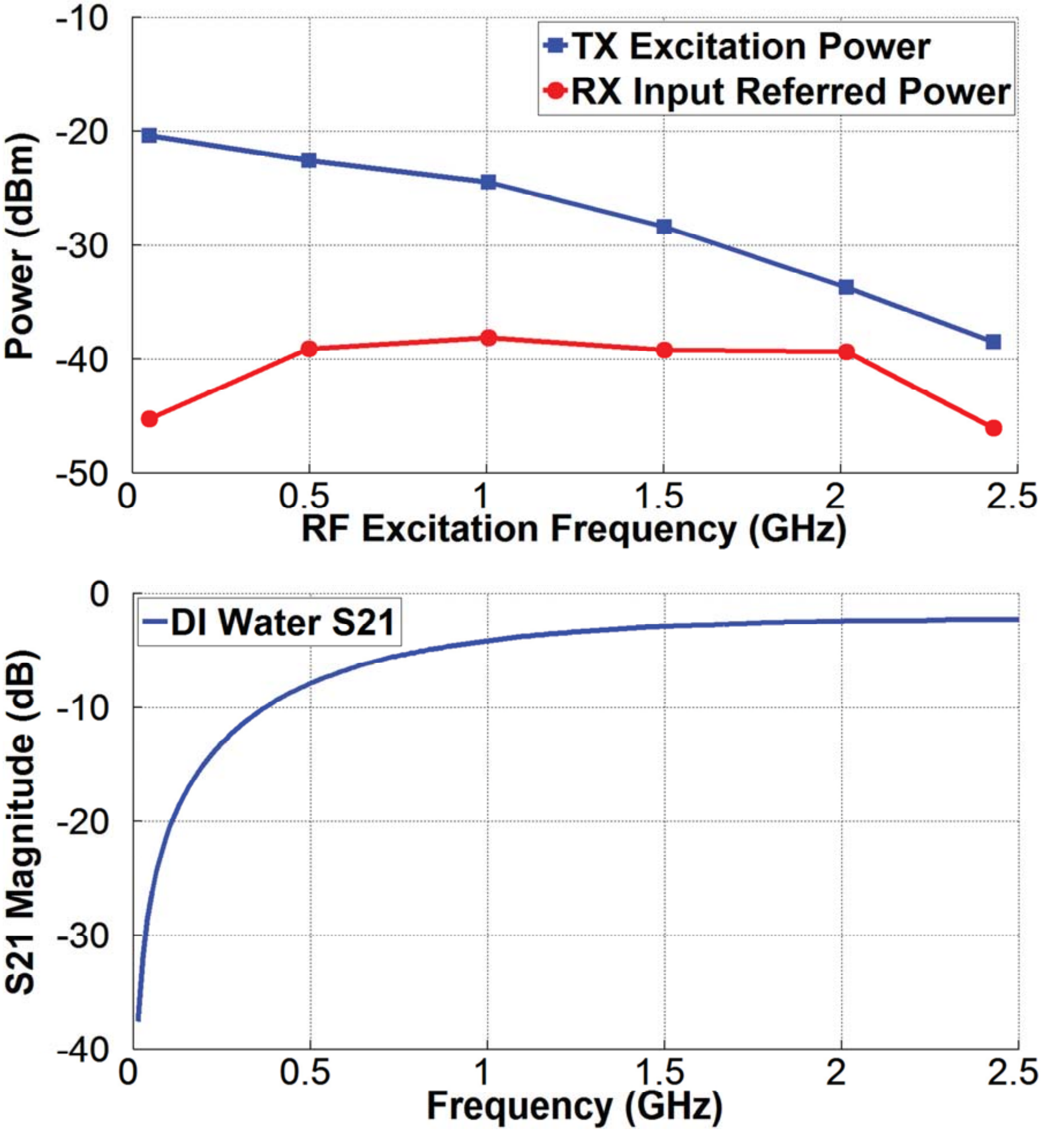

Figure 3.23: The measured TX output power and RX input referred power versus RF excitation frequency along with measured S_{21} magnitude of the DS sensor's channel when it is loaded with DI water and measured with VNA.

Figure 3.24 shows the measured dc receiver output in *I* mode versus that in *Q* mode at RF excitation frequencies of ~ 50MHz, 500MHz, 1.5GHz and 2.4GHz, with the sensor loaded with DI water, phosphate-buffered saline (PBS), Miller Lite beer and Guinness beer as four primarily-water-based MUTs. Since dielectric relaxation characteristics of water molecules would dominate the response at sufficiently high excitation frequencies, the MUT responses were much closer to each other at 2.4GHz (compared to 50MHz), as evident by the much smaller DR of X-Y axis. Nonetheless, the miniaturized DS platform was fully capable of differentiating among the four MUTs at all frequencies. Note also how the response from Miller Lite beer, as compared to darker Guinness beer, was always closer to that of DI water at elevated excitation frequencies.

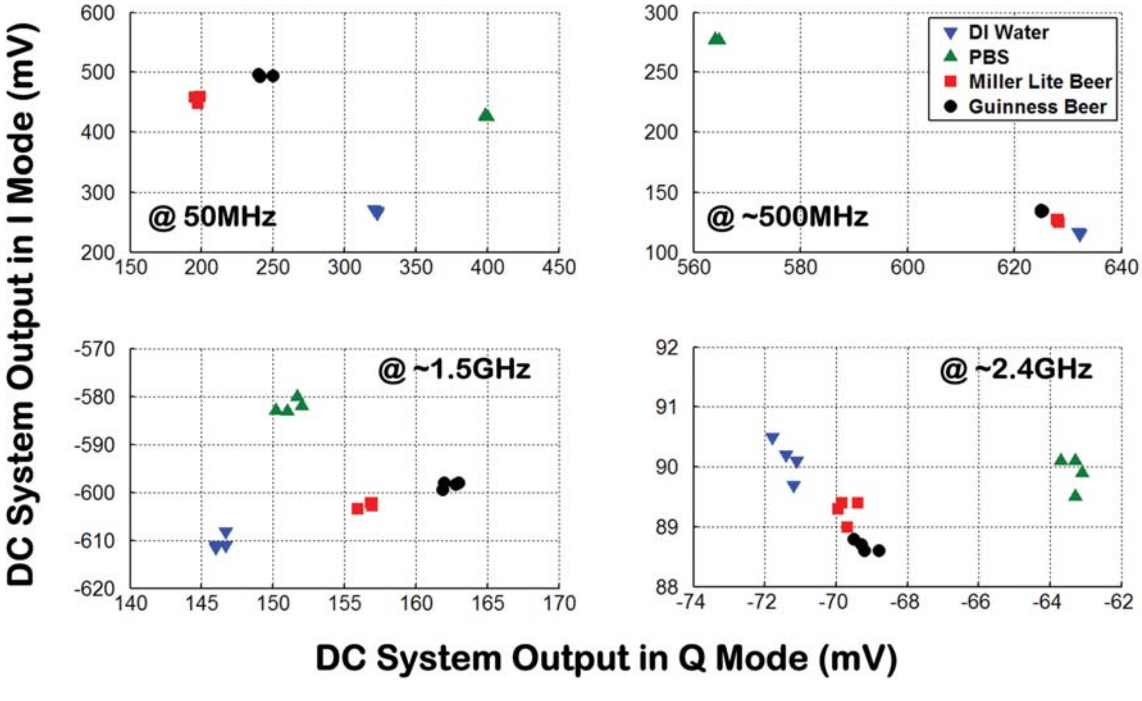

Figure 3.24: Measured dc system output in I/Q modes at ~ 50MHz, 500MHz, 1.5GHz and 2.4GHz with the sensor loaded with DI water, PBS, Miller Lite beer and Guinness beer as four primarily-water-based MUTs.

In order to verify the functionality of the proposed platform in extracting the frequency-dependent, complex permittivity of an MUT, a 3-step measurement procedure was developed as shown in Fig. 3.25. In step 1, the permittivity of the bulk-solution MUT was measured using an Agilent dielectric probe kit interfaced with a VNA as reference measurement for comparison purposes. In step 2, the amplitude/phase measurement was done on the MUT-loaded DS sensor using the transceiver IC as previously described. In step 3, a 6-point sensor calibration algorithm was run offline on a home-based computer to extract the MUT complex permittivity from the raw data recorded in step 2. Finally, a comparison of results from steps 1 and 3 would determine the error in permittivity measurement by the platform versus the reference measurement to establish proof-of-concept feasibility in DS system miniaturization. Figure 3.25 also shows the flow chart of the sensor calibration algorithm developed for PBS-based MUTs as an example. Six reference solutions consisting of PBS+2.5% Ethanol, PBS+5% Ethanol, PBS+10% Ethanol, PBS+2.5% Methanol, PBS+5% Methanol, and PBS+10% Methanol were used to calibrate the sensor in a multistep procedure. First, the permittivity of these six reference solutions was measured using an Agilent dielectric probe kit. Next, the reference solutions were loaded into the sensor interfaced with the transceiver IC, and the dc receiver outputs in I and Q modes of system operation were measured. A 1st -order polynomial fit was then used to relate the real part of permittivity information to Q-mode measurement results, and the imaginary part of permittivity to I-mode measurement results. The right figure is an example of such plots at 1GHz for the six reference solutions where the red dashed line shows a linear fit to the calibration data. Once the coefficients have been determined, the permittivity function can be used for any other

PBS-based MUT to extract the complex permittivity information from the corresponding voltage measurements.

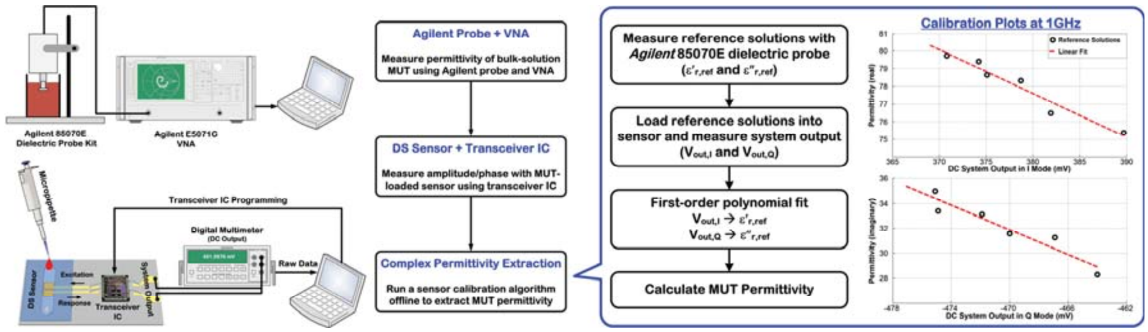

Figure 3.25: Illustration of the experimental setup for extracting the frequency-dependent, complex permittivity of an MUT along with the six-point sensor calibration procedure to extract dielectric permittivity information from IC measurements.

Figure 3.26 depicts the frequency-dependent real and imaginary parts of complex permittivity for PBS as the MUT at six RF excitation frequencies from 50MHz to ~2.4GHz. These data were extracted from voltage measurements of the sensor by the IC using a 6-point sensor calibration algorithm described before. Compared to bulk-solution reference measurements with a benchtop Agilent probe and VNA, dielectric readings of the platform showed an overall rms error of 1.7% (real) and 7.2% (imaginary), with the errors reducing to 0.7% and 1.5%, respectively, between 500MHz and 2.4GHz, demonstrating feasibility of conducting MHz-to-GHz DS measurements with a self-sustained fully miniaturized platform using μL-sample volumes.

Table 3.3 summarizes the measured performance of the IC (TX part), and Table 3.4 compares the IC functionality and its measured performance with that in recent published works.

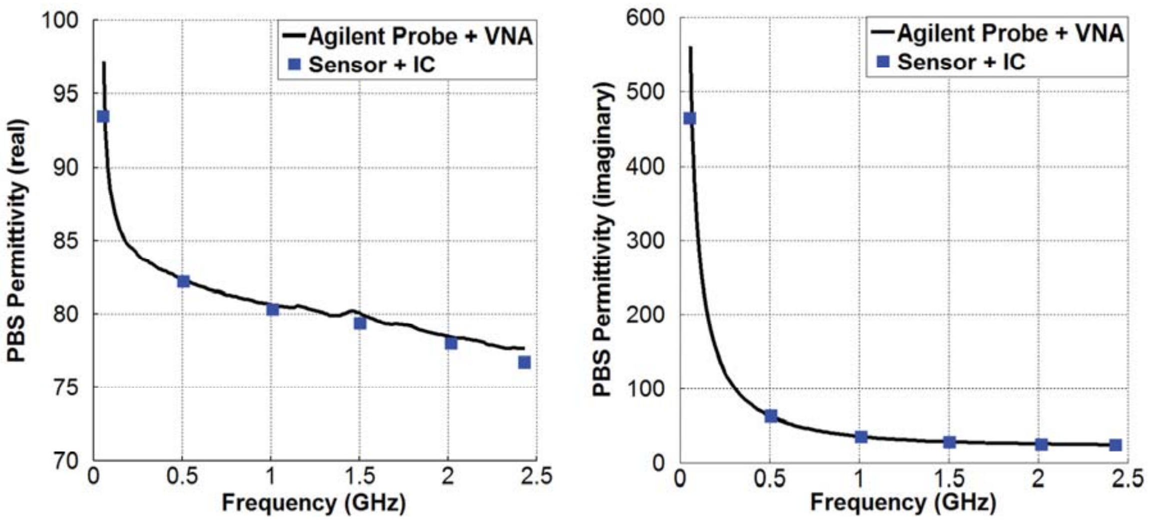

Figure 3.26: Real and imaginary parts of complex relative dielectric permittivity vs. frequency for PBS extracted from voltage measurements of the sensor by the IC after excitation at 6 different frequency points from 50MHz to ~2.4GHz. Solid line depicts the measured curve with an Agilent 85070E dielectric probe interfaced with a VNA as a reference measurement from a benchtop setup.

Table 3.3: Summary of IC Performance (TX Part)

QVCO				***Frequency Synthesizer***	
Topology	NMOS Core-G_m Switching			Frequency Range	1.248 – 2.432GHz
Tuning Range	***High - G_m***	***Low - G_m***		Frequency Step	32 MHz
	1.232 – 1.975GHz	1.678 – 2.455GHz		Loop Bandwidth	341 – 437 kHz
Programmability	***Coarse***	***Fine***	***Tail Current***	Phase Noise	-107 dBc/Hz @ 1MHz offset For 1.248 & 2.432GHz
	11 bits	3 bits	4 bits		
Kvco	22.4 – 46.6MHz/V			Spur Rejection	>51dBc @ 16MHz offset
$f_{step\ per\ code}$	16.5 – 46.5MHz			***HR-SSB Mixer***	
Power Consumption	***VCO***	***QVCO + Buffers***		Image Rejection	>50dBc (w/ Clock Buffer Calibration)
	6 – 15 mW	22 – 45 mW		Harmonic Rejection	>35dBc (for 3rd and 5th Harmonic)
Charge Pump				Power Consumption	1.5 – 2.5 mW
Programmability	5 bits			***Total Transmitter***	
Current Range	50 – 127.5 μA			LO Frequency Range	9.75MHz – 2.432GHz
Current Step	2.5 μA			RF-LO Offset	1 MHz
Programmable Frequency Divider				Frequency Points	304
Topology	Modular Programmable Prescaler			RF Output Power	-38.5dBm @2.433GHz -20.4dBm @10MHz
Division Ratio	32 – 127			Supply Voltage	1.5 V (Analog) 3.3V (Digital)
Power Consumption	20 mW			Power Consumption	57 – 85 mW

Table 3.4: Comparison of IC Functionality and Measured Performance

	This Work	**[3.3]**	**[3.19]**	**[3.20]**	**[3.21]**	**[3.22]**
Functionality	Measurement of dielectric permittivity					Capacitive sensing for flow cytometry
Methodology	Amplitude/phase	Amplitude/phase	Oscillation frequency shift + ALL	Amplitude/phase	Oscillation frequency shift	Oscillation frequency shift
Self-Sustainability	Yes	No (RX only)	Yes	No (external excitation)	Yes	Yes
Sensor Type	µfabricated 3D capacitor	µfabricated center-gapped µstrip line	On-chip 2D capacitor	On-chip interdigitated capacitor	On-chip interdigitated capacitor	On-chip coplanar electrodes
Operation Freq.	9MHz – 2.4GHz	10MHz – 3GHz	0.7 – 6GHz	0.62 – 10GHz	7 – 9GHz	6.5/11/17.5/30GHz
Permittivity Type	ε_r', ε_r''	ε_r'	ε_r', ε_r''	ε_r', ε_r''	ε_r'	ε_r'
Permittivity Range	1 – 94 (ε_r') 0 – 465 (ε_r'')	1 – 48	1 – 30 (ε_r') 0 – 14 (ε_r'')	1 – 48 (ε_r') 0 – 20 (ε_r'')	1 – 30	1 – 60
RMS Permittivity Error	< 0.7% (ε_r') < 1.5% (ε_r'') (0.5 – 2.4GHz)	< 6.4% (0.5 – 2.5GHz)	< 3.7%** (0.7 – 6GHz)	< 1%* (0.62 – 10GHz)	< 3.5%** (7 – 9GHz)	-
Total Power Consumption	61 – 94mW	4 – 9mW (RX only)	69 – 140mW	65 – 72mW (w/o freq. synthesizer)	16.5mW	65 – 75mW (4 channels)
Die Size	3.3 × 3.3mm^2	3 × 3mm^2	2.5 × 2.5mm^2	3 × 3mm^2	2.5 × 2.5mm^2	-
Technology	0.35µm RF CMOS	0.35µm RF CMOS	0.18µm CMOS	0.18µm CMOS	90nm CMOS	65nm CMOS

3.4 Conclusion

Quantitative measurement of the complex relative dielectric permittivity of a material versus frequency (i.e., dielectric spectroscopy, or DS) is a label-free, nondestructive, real-time and fully electrical monitoring technique for investigating molecular structure and dynamics of materials using electromagnetic fields. Despite having potential for a broad range of biomedical and industrial applications, DS is still under-investigated as an analytical tool, primarily due to a dearth of small-size, low-power and autonomous instruments for rapid, broadband capturing of the relaxation times in a wide range of samples, without requiring specialized measurement setups and large sample volumes. To that end, this chapter described a self-sustained dielectric spectroscopy platform which incorporates a microfluidic capacitive sensor with 3D-gap, floating electrode, and microfluidic channel for sample delivery, as well as a fully integrated transceiver IC for MHz-to-GHz dielectric spectroscopy. The presented platform is fully capable of differentiating among deionized (DI) water, phosphate buffered saline (PBS), Miller Lite beer and Guinness beer in tests conducted at four different excitation frequencies in the range of 50 MHz to 2.4 GHz. Further, complex dielectric readings of PBS from the platform at six excitation frequencies in the range of 50 MHz to 2.4 GHz are in excellent agreement (RMS error <0.7% (ε') and <1.5% (ε'') for 0.5 to 2.4 GHz) with those from a reference measurement by an Agilent 85070E dielectric probe kit interfaced with a VNA. The unique features of the proposed dielectric spectroscopy (DS) platform, namely, extraction of complex dielectric permittivity information from transmission-based characteristics of the sensor only, as well as associated IC development for simultaneous sensor excitation and measurement of its transmission characteristics have obviated the need for any external, large, benchtop equipment and resulted in the development of a platform that is small enough to be carried on the palm of a hand, ultimately paving the way for translating DS measurements from the lab bench to the field or to the bedside.

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Chapter 4

A Palmtop Platform for MHz-GHz Dielectric Spectroscopy

This paper describes an autonomous self-sustained palmtop measurement platform for dielectric spectroscopy (DS) which incorporates a microfluidic DS sensor, a fully integrated transceiver IC for MHz-to-GHz dielectric spectroscopy, as well as a Raspberry pi module as a low-cost embedded computing platform. With the dimension of 10cm × 6.5cm × 5.2cm, the proposed palmtop platform is capable of accurately measuring the real and imaginary part of material under test (MUT) complex permittivity from 9MHz to 2.433GHz by programming the IC to generate a single-tone sinusoidal RF excitation signal with MHz-to-GHz tuning capability to the sensor loaded with MUT, and measures the sensor transmission characteristics in the voltage domain. The Raspberry pi module is then capable of extracting the MUT permittivity from the IC measurement by running the sensor calibration algorithm and plotting the data on a handheld device wirelessly. The presented platform is fully capable of differentiating among deionized (DI) water, Lemonade, Red wine and Vodka as four primarily-water-based MUTs in tests conducted at four different excitation frequencies in the range of 34 MHz to 2.176 GHz.

Further, complex dielectric readings of DI water + different concentration of Ethanol from the platform at 32 excitation frequencies in the range of 10 MHz to 2.433 GHz are in excellent agreement (RMS error <0.4% for real part over the entire frequency range and <1.7% for imaginary part over 0.5 to 2.433GHz) with those from a reference measurement by an *Agilent* 85070E dielectric probe kit interfaced with a VNA, demonstrating proof-of-concept feasibility in conducting MHz-to-GHz dielectric spectroscopy with a self-sustained palmtop platform using μL-sample volumes.

The rest of this chapter is organized as follows. Section 4.1 describes the system architecture of the proposed platform as well as the principles of the measurement methodology Section 4.2 discusses the DS measurement and sensor calibration algorithm implementation, and Section 4.3 presents measurement results from experiments with the self-sustained palmtop DS platform. Finally, Section 4.4 draws some conclusions from this work.

4.1 System Implementation

Figure 4.1 depicts the system architecture of the proposed palmtop DS platform as well as the illustration of the experimental setup. The palmtop platform incorporates a three-dimensional, parallel-plate capacitive sensor embedded in a microfluidic channel [4.1] and a fully integrated transceiver IC (TRX IC) [4.2] for sensor excitation and measurement of the sensor response signal as described in chapter 3. The differential system output signal from TRX IC is then digitized by a 16bit commercial ADC IC and transferred to the Raspberry Pi module through SPI interface. The palmtop platform also incorporates a power supply unit to provide required supply voltages for different modules as well as a 802.11 WiFi module for data communication with a handheld device. The palmtop platform only requires a single 5V power supply with standard Micro-USB connector to operate. The detailed principle operation of DS sensor + Transceiver IC is described in chapter 3. Therefore, in this section, we focus on the detailed description of other blocks in the palmtop platform as well as the implemented algorithms for the self-sustained autonomous operation of the platform.

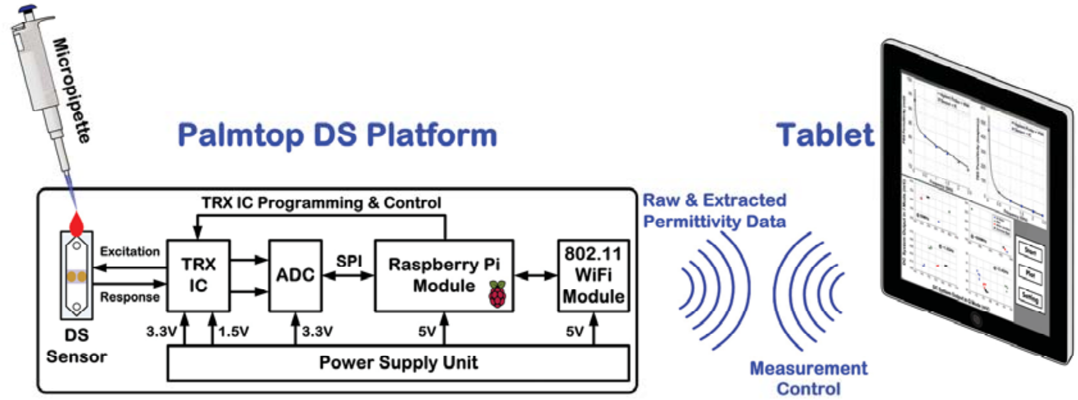

Figure 4.1: System architecture of the proposed palmtop DS platform along with its measurement setup.

4.1.1 DS Sensor + Transceiver IC

As described in detail in chapter 3, the DS sensor is based on a parallel-plate capacitive structure with a floating electrode integrated into a microfluidic cap that delivers the MUT to the sensing area [4.1]. As the MUT passes through the sensing area, the impedance (and hence voltage-transmission characteristics) of the sensor changes based on ε_r of the MUT. The transceiver IC is therefore designed to excite the sensor with a single-tone sinusoidal signal at a user-set RF excitation frequency of ω_{RF} and accurately measure the transmission characteristics of the loaded sensor via amplitude/phase measurement [4.2]. The TRX IC also incorporates SPI interface for programming RX/TX blocks which allows programming the measurement frequency as well as different IC calibrations by the Raspberry Pi module. The ε_r of the MUT is then extracted from the digitized IC measurements of the sensor using a 6-point sensor calibration algorithm that runs online on the Raspberry Pi as a low-cost embedded platforms.

4.1.2 ADC

The palmtop platform incorporates ADS8861 commercial 16bit 1-MSPS Serial interface ADC IC to digitize the differential DC system output signal from the TRX IC. The ADC has a differential input with ±2.5V swing and works with 3.3V power supply. In order to send out the digitized data to Raspberry Pi module, the SPI interface with 1 MHz clock frequency is used. For each ADC readout, Raspberry Pi actives the ADC CONVST bit (conversion time enable pin) and after 5μs delay, reads 16 serial bits of the data. The reference voltage for ADC is 2.5V and it is generated by the power supply unit.

4.1.3 Raspberry Pi Module

The Raspberry Pi is a credit-card sized computer with 39.29g weight based on Broadcom BCM2835 SoC, which includes an ARM1176JZF-S 700 MHz processor, VideoCore IV GPU, and 512 Megabytes of RAM. It relies on SD card for booting and long-term storage and runs Linux kernel based operating system called Raspbian. The palmtop DS platform leverages the Raspberry Pi Model B 512MB RAM model with two USB ports and a 10/100 Ethernet controller for wired network connection. In addition, HDMI plug, generic USB keyboards, and mice are compatible in case the user prefers not to use a remote handheld device to access the palmtop platform. The Raspberry Pi module also feature 26 pins of general purpose input/output (GPIO) along the edge of the board which interfaces the Raspberry Pi board to TRX IC, ADC IC, and power supply unit via 2×13 header in palmtop platform. DS measurement and calibration algorithms are implemented in python language running on Raspberry Pi module. The user can access to the Raspberry Pi module, either through the wired/wireless network or by directly connecting keyboard and monitor to the Raspberry Pi.

4.1.4 802.11 WiFi Module

In order to provide the wireless access to the palmtop platform, a Miniature WiFi 802.11 module with 150Mbps data rate is employed. The WiFi module is based on RTI8192 chipset with USB2 host interface which connects to one of the Raspberry Pi USB ports. The handheld device (e.g., tablet) can access to the Raspberry Pi module graphical user interface (GUI) through the wireless network using *VNC viewer* remote IP program. The WiFi module can be turned on and off by the Raspberry Pi module. In order to eliminate the WiFi signal interference (2.412 – 2.462 GHz) with the DS measurement around 2.4 GHz, the WiFi module will be disabled by the DS measurement program during the measurement time (~ 1s) automatically. After the measurement being done, the Raspberry Pi module automatically enables the WiFi module to reconnect with the handheld device for data transfer and control.

4.1.5 Power Supply Unit

The palmtop platform only needs a 5V supply voltage with standard Micro-USB connector in the bottom layer PCB. The Raspberry Pi module as well as the WiFi module use 5V voltage directly as a supply voltage. In order to provide different supply voltages for other blocks, the middle layer PCB incorporates two types of commercial voltage regulator ICs. Two AP1713 commercial ICs are used to provide 3.3V supply voltage for TRXIC (digital supply voltage) as well as ADC IC from 5V input voltage with 300mA maximum output current. Separate 3.3V supplies are used to eliminate digital noise coupling between TRX and ADC ICs. In addition, AP7313 commercial IC is to provide 1.5V analog supply voltage from 5V input voltage with 150mA maximum output current. AP7333 commercial IC is also used in conjunction with proper decoupling capacitors to provide 2.5V reference voltage for ADC IC.

Fig. 4.2 depicts the three PCB layers of the palmtop DS platform prototype incorporating DS sensors on top layer, TRX IC, ADC IC, and power supply unit on middle layer, and Raspberry Pi module along with WiFi dongle on bottom layer.

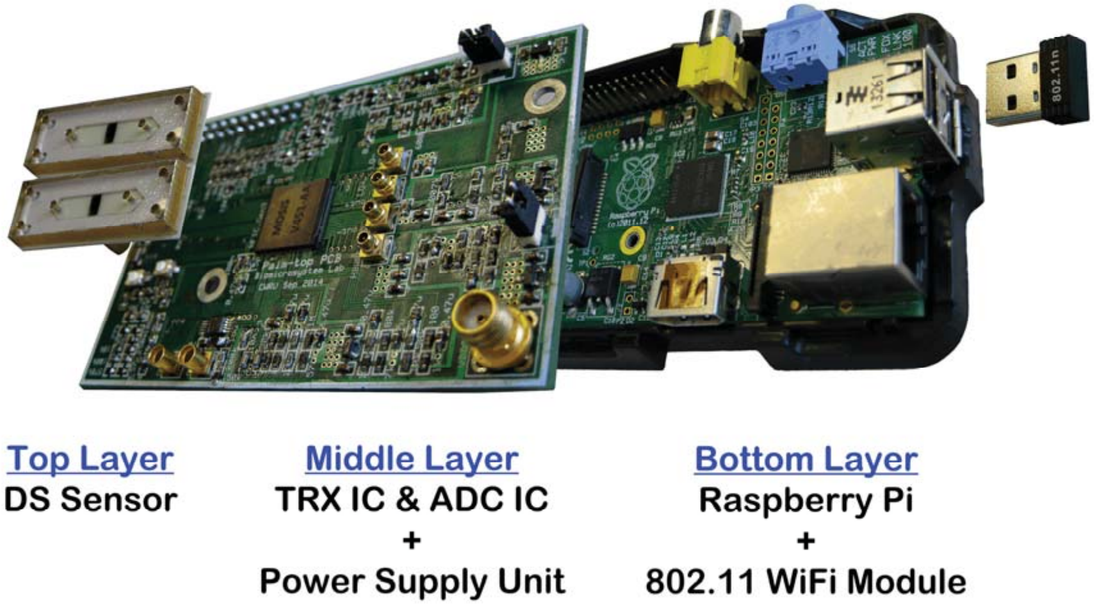

Figure 4.2: Illustration of palmtop DS platform implementation incorporating DS sensors on top layer, TRX IC, ADC IC, and power supply unit on middle layer, and Raspberry Pi module along with WiFi dongle on bottom layer.

4.2 Calibration and Measurement Algorithms Implementation

In this section, we present the algorithms implemented in Raspberry Pi module to perform the DS measurement as well as the sensor calibration algorithm.

4.2.1 DS Measurement Algorithm

Fig. 4.3 illustrates the flowchart of DS measurement algorithm implemented in Python language in the Raspberry pi module. The algorithm has three main modules including *I/Q* measurement, permittivity calculation, and plotting the data. The DS measurement algorithm can be run wirelessly from the tablet on the Raspberry Pi module. The algorithm first initializes the Raspberry Pi GPIO pins as well as the SPI port in order to communicate with TRX and ADC ICs. As a next step, the LookUpHex.txt file will be opened. This file contains the table of measurement frequency points which is set by user to perform the DS measurement as well as the TRX IC programming data for each measurement frequency. The algorithm is then starts from the first measurement frequency point and programs the TRX IC. Figure 4.4 shows the timing diagram for TRX IC programming as well as the timing for the measurement module. The TRX IC will is programmed using SPI port through SCLK and SDATA pins. The SPI clock is set to 1MHz in initialization phase. The TRX IC has five program registers that needs to be programmed for each measurement frequency. Each program register has a *Prog_Enable* bit that needs to be high in order to enable programming. The first two registers (R1 and R2) belong to the receiver part (RX). During the first 15 cycles of programming, the first register sets the parameter for temperature and gain calibration as well as the HBW/LBW RF module selection. The second register is being programmed in 17 cycles to set the phase calibration parameters. The last three registers (R3, R4, and R5) set the transmitter parameters for VCO, PLL, and Band-select multiplexer + clock buffer, respectively. The total IC programming time for each measurement frequency is 90µs. After TRX IC programming, the algorithm sets *I/Q_Select* pin of TRX IC to 1 in order to set the TRX IC in *I* mode of operation. The time constant (τ) for the LPF at the TRX IC output is 675µs. Therefore the minimum required settling time for the TRX IC output for 16 bits resolution is 11.09 τ (~7.5ms). Therefore a 10ms delay is implemented in order to wait for the transmitter to be locked as well as the system output to be settled. After the delay, the Raspberry Pi enables the ADC and reads the ADC output through SPI port. During the ADC readout mode, Raspberry Pi module reads 100 samples taken by ADC from DC system output in 10ms. Then the Raspberry Pi set *I/Q_Select* bit to 0 resulting in TRX IC *Q* mode of operation. The same ADC readout procedure is repeated for this mode. Therefore, for each measurement frequency, the TRX DC system output is sampled by ADC for 20ms and the total time required for a single frequency measurement is 40.09ms. The ADC data is then written to Dataout.txt file in Raspberry pi SD card and it can be retrieved by the handheld device. The measurement module will be repeated for all the measurement frequencies in the LookUpHex.txt table.

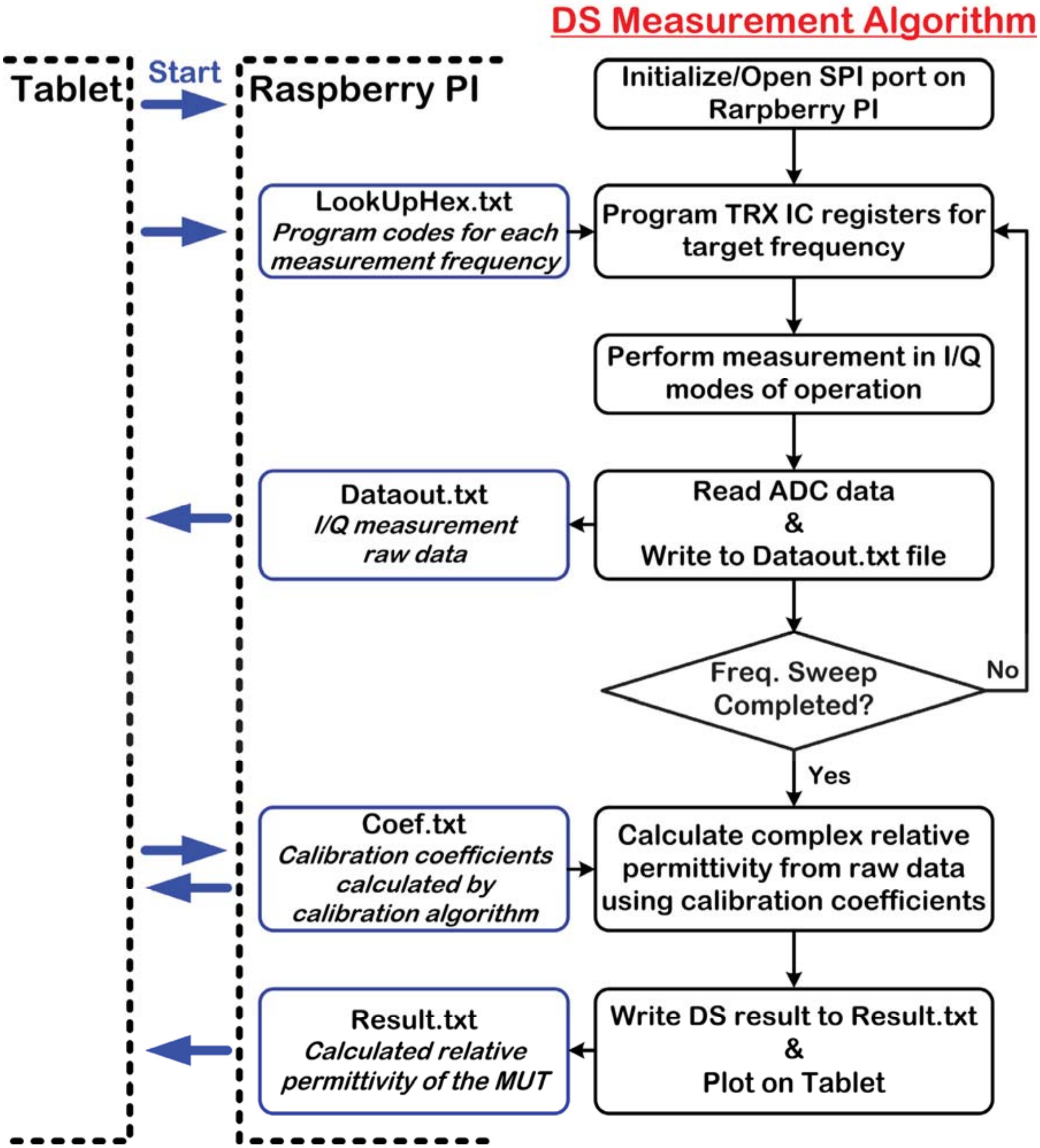

Figure 4.3: DS measurement algorithm flowchart implemented in Raspberry Pi module.

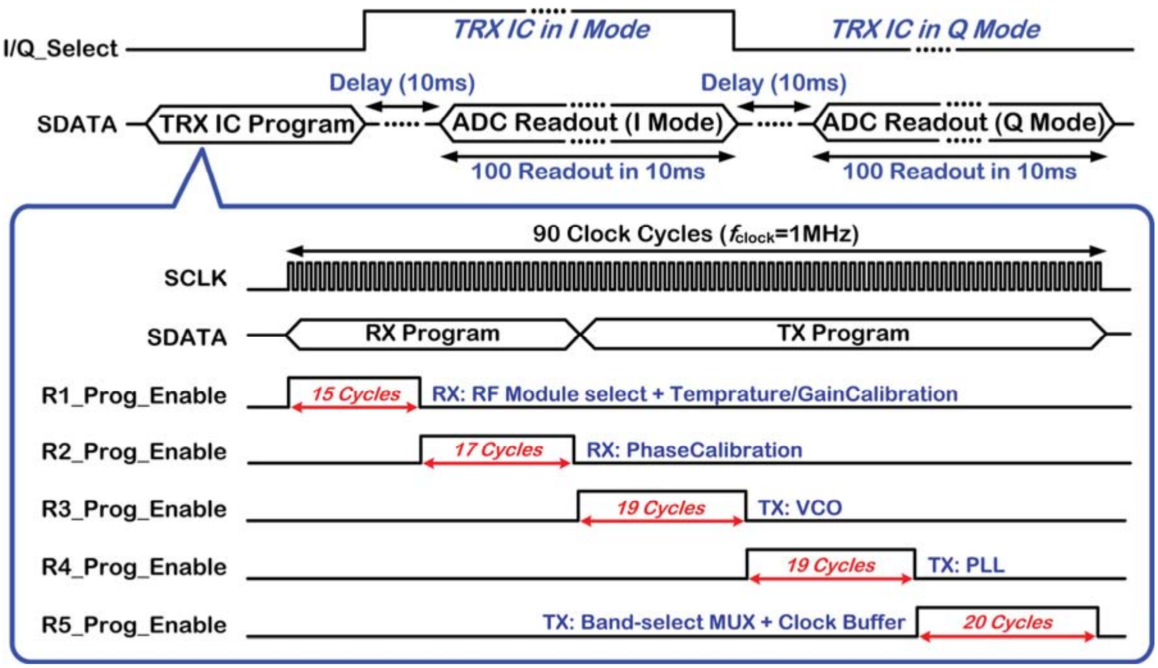

Figure 4.4: Timing diagram for TRX IC programming as well as single frequency measurement by measurement algorithm.

In the permittivity calculation module, the measurement raw data is used to calculate the *complex* relative permittivity of the MUT based on the calibration coefficients in the Coef.txt file stored in the Raspberry Pi SD card. This coefficient has been calculated by the Raspberry Pi by running the Sensor Calibration Algorithm which will be described in section 4.2.2. After permittivity calculation for each measurement frequency, the permittivity data will be saved in Result.txt file. Then, the algorithm plots the real and imaginary permittivity versus frequency using *matplotlib* python plotting library. For the comparison purposes, the DS measurement algorithm is also capable to calculate the permittivity RMS error with respect to the MUT reference permittivity (measured by the commercial dielectric probe) if that data is stored in the Raspberry Pi SD card.

4.2.2 Sensor Calibration Algorithm

Fig. 4.5 depicts the sensor calibration algorithm implemented in Raspberry Pi module to calculate the calibration coefficients required for complex permittivity calculation. Six reference solutions consisting of DI Water, DI Water + 5% Ethanol, DI Water + 10% Ethanol, DI Water + 5% IPA, DI Water + 10% IPA, DI Water + 20% IPA were used to calibrate the sensor. First, the permittivity of these reference solutions was measured using a commercial DS system (VNA + 85070E *Agilent* dielectric probe kit).These reference data is then stored in the Probe_data.txt file in the Raspberry Pi SD card. Next, the sensor calibration algorithm will be run on the Raspberry Pi from the handheld device by the user. First, each reference solutions will be loaded to DS sensor by the user and the *I/Q* measurement for all the frequencies listed in *LookUpHex.txt* will be performed by the palmtop platform and stored in *Calibration_data.txt* file. After performing these measurements, the algorithm normalized the raw data ($V_{out,I}$ and $V_{out,Q}$) with respect to the DI water raw data. A 1st -order polynomial fit was then used by the algorithm to relate the real part of permittivity information ($\varepsilon'_{r,ref}$) to Q-mode normalized measurement results ($V_{out,Q,Normalized}$), and the imaginary part of permittivity ($\varepsilon''_{r,ref}$) to I-mode normalized measurement results ($V_{out,I,Normalized}$). Once the coefficients have been determined for each measurement frequency, they will be stored in *Coef.txt* file to be used for any other Water-based MUT to extract the complex permittivity information from the corresponding voltage measurements.

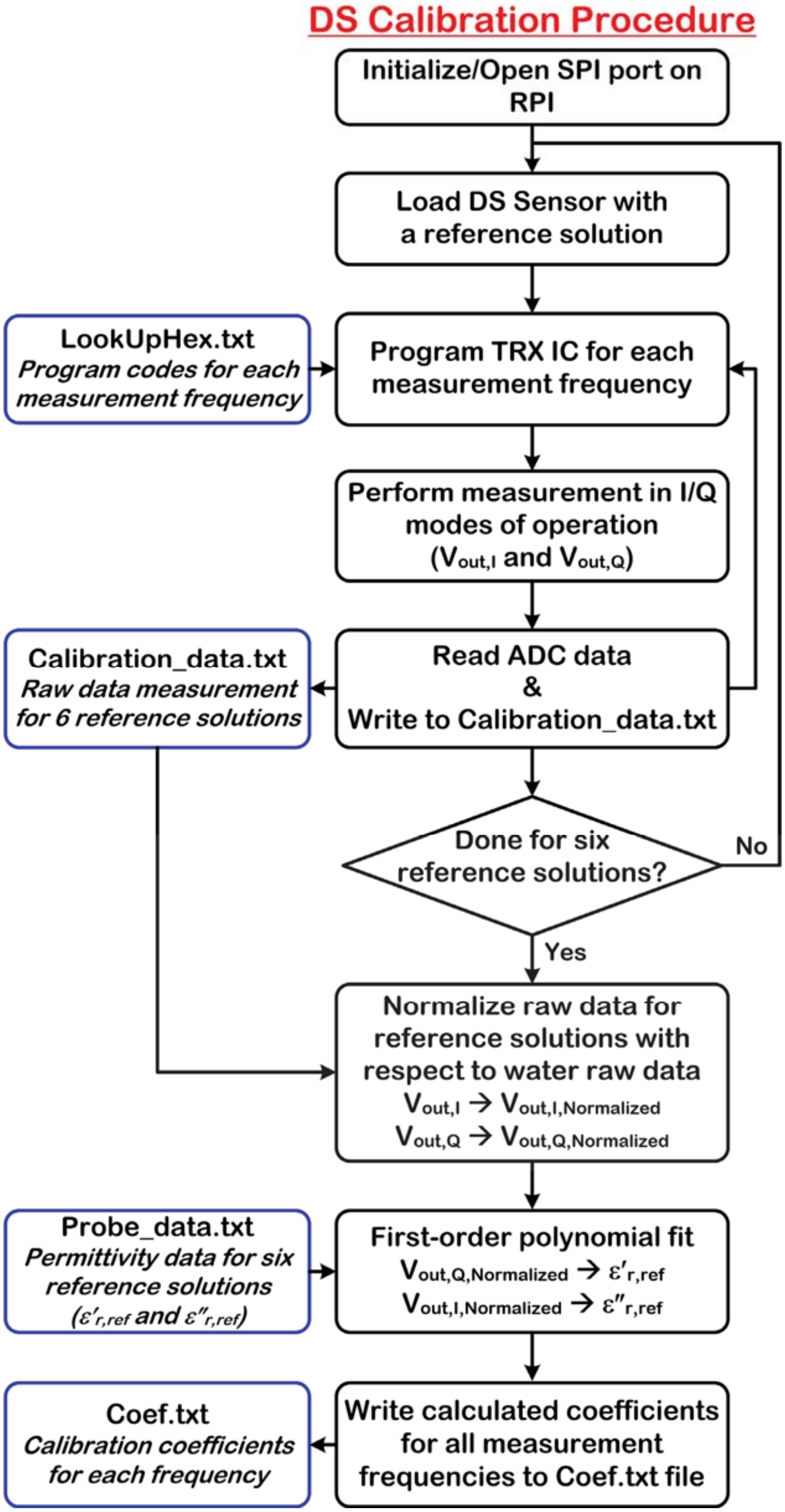

Figure 4.5: Sensor calibration algorithm flowchart implemented on Raspberry Pi Module.

4.3 Measurement Results

This section presents the measurement results from DS studies using the palmtop DS platform interfaced with different aqueous solutions. Figure 4.6 shows a photograph of the palmtop DS platform along with its measurement setup including a micropipette for MUT sample delivery as well as a tablet for measurement control as well as data retrieval. The prototype dimension is 10cm (length) × 6.5cm (width) × 5.2cm (height).

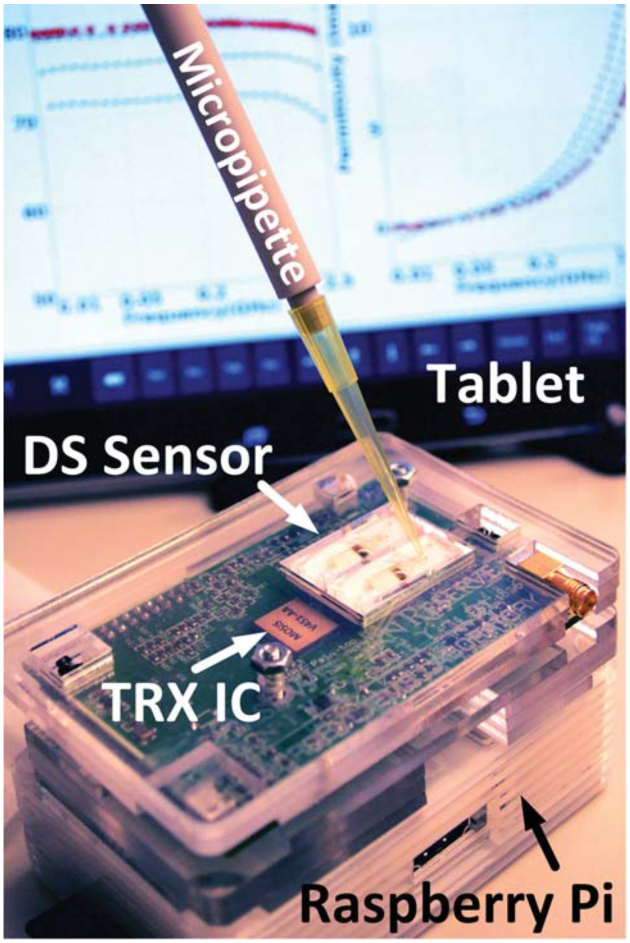

Figure 4.6: Photograph of a palmtop DS platform prototype along with its measurement setup incorporating a micropipette for sample delivery as well as a tablet for measurement control and data retrieval.

Figure 4.7 shows the ADC readout versus time when the DS sensor is loaded with DI water and Palmtop platform performs the measurement at 32 different RF excitation frequencies from 10MHz to 2.433GHz. As described before in section II.A, at each measurement frequency, the ADC IC takes 200 samples of the TRX system output in 20ms (100 samples in 10ms for each mode of operation). The total ADC sampling time and measurement time for this measurement is then 660ms, and 1.3s respectively.

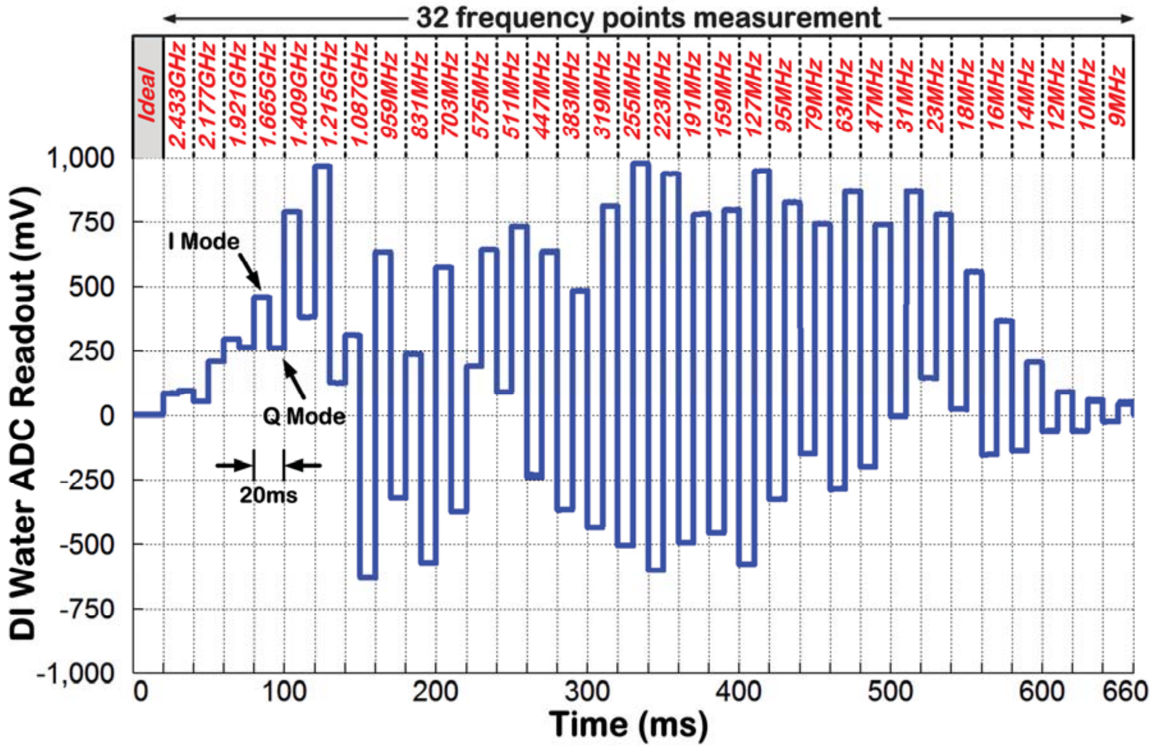

Figure 4.7: ADC readout versus time when the DS sensor is loaded with DI water and Palmtop platform performs the measurement at 32 different RF excitation frequencies from 10MHz to 2.433GHz.

Figure 4.8 shows the digitized TRX IC dc system output in *I* mode versus that in *Q* mode measured by the palmtop platform at RF excitation frequencies of ~ 33MHz, 487MHz, 1.087GHz and 2.177GHz (50 measurements for each MUT), with the DS sensor loaded with DI water, Lemonade , Red Wine and Vodka as four primarily-water-based MUTs. Since dielectric relaxation characteristics of water molecules would dominate the response at sufficiently high excitation frequencies, the MUT responses were much closer to each other at 2.177GHz (compared to 33MHz), as evident by the much smaller DR of X-Y axis. Nonetheless, the palmtop DS platform was fully capable of differentiating among the four MUTs at all frequencies. Note also how the response from Lemonade (non-alcoholic), as compared to Red Wine and Vodka (alcoholic beverages), was always closer to that of DI water.

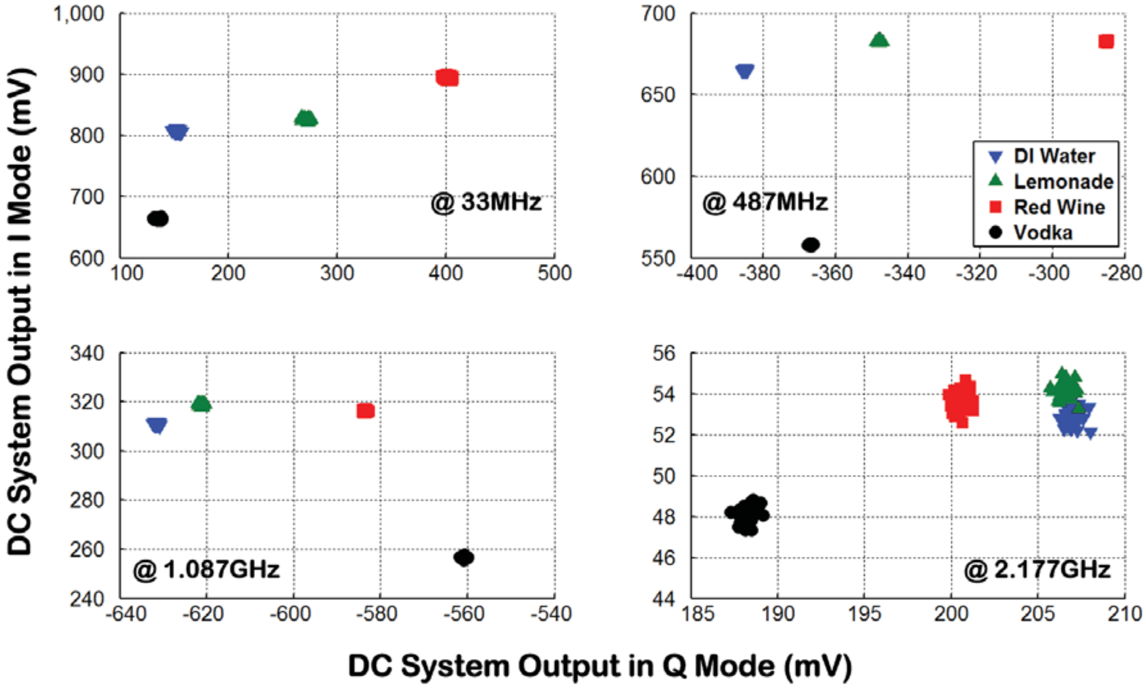

Figure 4.8: DC system output in I mode versus that in Q mode at RF excitation frequencies of ~ 33MHz, 487MHz, 1.087GHz and 2.177GHz (50 measurements for each MUT) measured by palmtop DS platform, with the DS sensor loaded with DI water, Lemonade , Red Wine and Vodka as four primarily-water-based MUTs.

Figure 4.9 depicts the calibration plots at 1.087GHz and 2.433GHz from the sensor calibration algorithm. As can be seen, the real/imaginary part of permittivity has a linear relation with normalized TRXIC DC system output in *Q/I* modes. The red dashed line is the linear fit calculated by the calibration algorithm to be used for permittivity calculation in DS measurements.

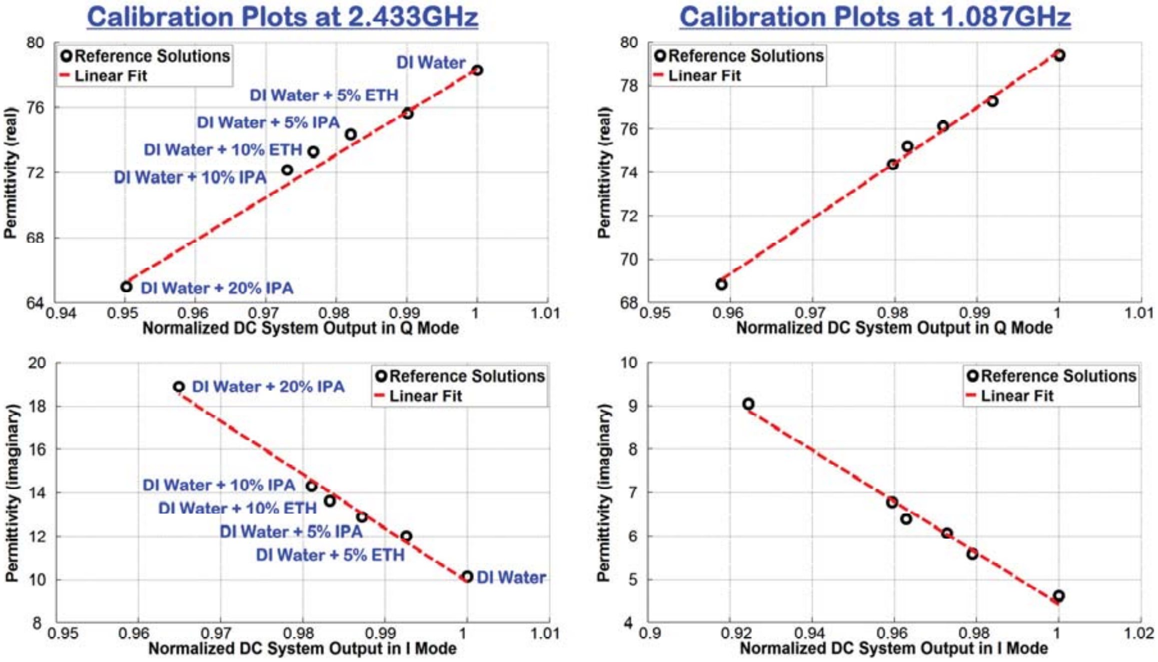

Figure 4.9: Calibration plots at 1.087GHz and 2.433GHz RF excitation frequencies for six reference solutions including DI Water, DI Water + 5% Ethanol, DI Water + 10% Ethanol, DI Water + 5% IPA, DI Water + 10% IPA, and DI Water + 20% IPA calculated by the sensor calibration algorithm implemented on Raspberry Pi module.

Figure 4.10 shows the frequency-dependent real and imaginary parts of complex permittivity for four different mixture solutions of DI water and Ethanol as the MUT measured by the palmtop DS platform at 32 RF excitation frequencies from 10MHz to 2.433GHz. The DS measurement algorithm were extracted these permittivity data automatically after the *I/Q* voltage measurements using calibration coefficients that calculated by the sensor calibration algorithm described before. Compared to bulk-solution reference measurements with a benchtop Agilent probe and VNA, dielectric readings of the platform showed an overall rms error of 0.4%

(real) over the entire frequency range and 1.7% (imaginary) between 500MHz and 2.433GHz. The RMS error for imaginary part is calculated from 500MHz to 2.433GHz mainly because below 500MHz the imaginary part of permittivity for the measured MUTs is very small. Therefore small difference between the palmtop platform measurement and reference measurement results in a large relative error. Note also how the palmtop DS platform could capture different relaxation characteristics of the MUT as the percentage of ethanol in the DI water mixture was gradually increased.

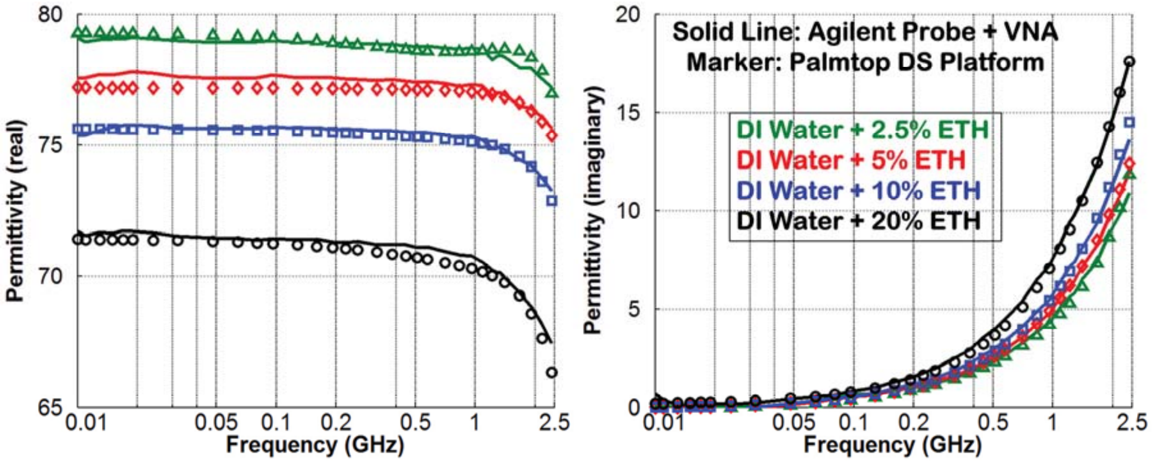

Figure 4.10: Real and imaginary parts of complex relative dielectric permittivity vs. frequency for four different mixture solutions of DI water and Ethanol extracted online by the palmtop DS platform from voltage measurements of the sensor by the TRX IC after excitation at 32 different frequency points from 10MHz to 2.433GHz. Solid line depicts the measured curve with an Agilent 85070E dielectric probe interfaced with a VNA as a reference measurement from a benchtop setup.

Finally Figure 4.11 depicts the frequency-dependent real and imaginary parts of complex permittivity for Vodka (40% Alcohol) as the MUT measured by the palmtop DS platform at 32 RF excitation frequencies from 10MHz to 2.433GHz. Compared to bulk-solution reference measurements with a benchtop Agilent probe and VNA, dielectric readings of the platform showed an overall rms error of 0.27% (real) over the entire frequency range and 4% (imaginary) between 500MHz and 2.433GHz, demonstrating feasibility of conducting MHz-to-GHz DS measurements with a self-sustained portable palmtop platform using μL-sample volumes. In particular, embedding all required modules for DS measurement including DS sensor, TRX IC and Raspberry Pi embedded computing platform in a single portable instrument facilitates an automated broadband dielectric spectroscopy from MHz to GHz with an overall measurement time of less than 5s.

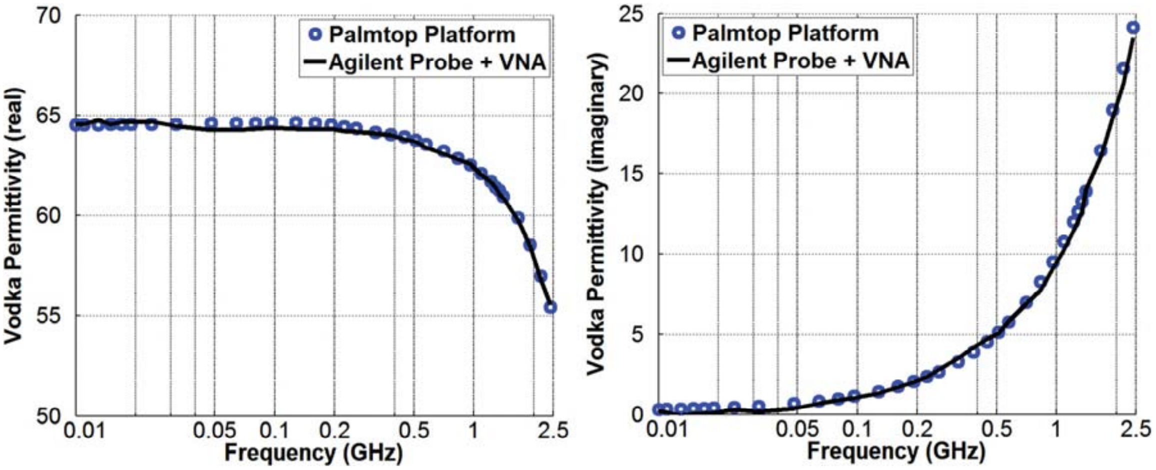

Figure 4.11: Real and imaginary parts of complex relative dielectric permittivity vs. frequency for Vodka (40% alcohol) extracted online by the palmtop DS platform from voltage measurements of the sensor by the TRX IC after excitation at 32 different frequency points from 10MHz to 2.433GHz.

4.4 Conclusion

This an autonomous self-sustained palmtop measurement platform for dielectric spectroscopy (DS) which incorporates a microfluidic DS sensor, a fully integrated transceiver IC for MHz-to-GHz dielectric spectroscopy, as well as a Raspberry pi module as a low-cost embedded computing platform. The presented platform is fully capable of differentiating among deionized (DI) water, Lemonade, Red Wine and Vodka in tests conducted at four different excitation frequencies in the range of 33 MHz to 2.177 GHz. Further, complex dielectric readings of four different mixture solutions of DI water and Ethanol as well as Vodka from the platform at 32 excitation frequencies in the range of 10 MHz to 2.433 GHz are in excellent agreement (RMS error <0.4% (real) for entire frequency range and <4% (imaginary) for 0.5 to 2.4 GHz) with those from a reference measurement by an Agilent 85070E dielectric probe kit interfaced with a VNA. The unique features of the proposed palmtop dielectric spectroscopy (DS) platform, namely, online extraction of complex dielectric permittivity information from transmission-based characteristics of the sensor only by the embedded computing platform, as well as associated IC development for simultaneous sensor excitation and measurement of its transmission characteristics have obviated the need for any external, large, benchtop equipment and resulted in the development of a first self-sustained platform that is small enough to be carried on the palm of a hand, ultimately paving the way for translating DS measurements from the lab bench to the field or to the bedside.

4.5 References for Chapter 4

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Chapter 5

Conclusions, Contributions, and Future Work

Quantitative measurement of the complex relative dielectric permittivity of a material versus frequency (i.e., dielectric spectroscopy, or DS) is a label-free, nondestructive, real-time and fully electrical monitoring technique for investigating molecular structure and dynamics of materials using electromagnetic fields. Despite having potential for a broad range of biomedical and industrial applications [2-9], DS is still under-investigated as an analytical tool, primarily due to a dearth of small-size, low-power and autonomous instruments for rapid, broadband capturing of the relaxation times in a wide range of samples, without requiring specialized measurement setups and large sample volumes.

The ultimate goal of this Ph.D. research work is to realize a self-sustained miniaturized, autonomous, palmtop platform that *for the first time* capable of autonomously and rapidly capturing the dielectric relaxation characteristics of material under test (MUT) in a wide frequency range from MHz to GHz. This has been accomplished in a three-phased approach. In Phase I, a Gen-1 sensor interface IC (Receiver IC) is developed for measuring the wideband transmission characteristic of the MUT-loaded sensor in the voltage domain. The Gen-1 interface IC only has readout capability and does not provide the sensor excitation signal. Therefore it is not yet self-sustained as it needs two benchtop signal generators to generate the required RF and LO signals. Next, in the second phase, a fully integrated transceiver IC is developed incorporating a receiver (RX), which utilizes broadband frequency response analysis method as well as a transmitter (TX) to generate the RF excitation signal for the sensor, amd the LO signals for the RX in MHz-GHz frequency range in order to enable a self-sustained operation for platform portability. Finally, in the third phase, the palmtop DS platform is developed in order to enable rapid, high-throughput, and low-cost measurements. In this truly portable system that is small enough to fit on the palm of a hand, a Raspberry Pi module is interfaced with the transceiver IC as a low-cost embedded computing platform to run the sensor calibration algorithm online, wirelessly connect with a handheld tablet to transfer the data for plotting and storage, as well as wirelessly program the transceiver IC from the tablet. In particular, this capability facilitates an automated frequency sweep from MHz to GHz, resulting in a short measurement time (<5 seconds) for the entire frequency range.

5.1 Contributions

The major contributions of this research work to the field of biomedical microsystems are listed as follows

5.1.1 Design and Theory

- Introduce broadband frequency response analysis method (bFRA) to the field of on-chip analog signal processing in integrated circuit and microsystem design.
- Introduce an area-efficient low-power signal generation method for bFRA transceivers.
- Obtain a fundamental knowledge of the complex permittivity extraction methods from transmission characteristics to enable *real-time* complex permittivity extraction on the palmtop platform.
- Introduce a DS measurement and calibration algorithm for the palmtop platform to the field of integrated circuit and microsystem design for performing accurate broadband dielectric spectroscopy measurement on palmtop DS platform.
- Introduce the *first* self-sustained autonomous palmtop DS platform to the realm of broadband dielectric spectroscopy.

5.1.2 Development and Assembly

- Develop a sensor interface IC (RX only) which utilizes the broadband FRA method to measures the sensor transmission characteristics in the voltage domain via an amplitude/phase measurement.
- Develop a microfluidic-CMOS platform that incorporates a three-dimensional, parallel-plate capacitive sensor embedded in a microfluidic channel, as well as a fully integrated transceiver IC for sensor excitation and measurement of the sensor response signal.

- Develop a self-sustained palmtop DS platform incorporating the microfluidic-CMOS platform, ADC, power supply unit, Wi-Fi module, and a Raspberry Pi computing module to enable rapid, high-throughput, and low-cost DS measurement on the field or bedside.

5.1.3 Testing and Characterization

- Thorough benchtop testing and electrical performance characterization of the developed microsystems.
- Characterization of *Sensor + IC* platforms using different organic chemicals.
- Demonstration of classification between different organic chemicals and aqueous solutions using *Sensor + IC* platforms.
- Demonstration of functionality of the developed platforms in dielectric spectroscopy by extracting frequency-dependent dielectric permittivity of different aqueous solutions and organic chemicals.
- First ever autonomous, real-time, MHz-GHz complex permittivity extraction of different aqueous solutions with μL sample volume using the developed self-sustained palmtop platform.

5.2 Limitations and Future Work

5.2.1 Single Chip Integration of the Platform

One future direction for this project is to further integrate the proposed developed palmtop DS platform to a single chip in order to achieve higher level of integration and smaller size while simultaneously reduce the potential obstacles of interfacing different modules. In particular, integrating the microfluidic DS sensor on the surface of the chip could potentially reduce the sensor-IC interface parasitic components and reduce the platform calibration complexity. Integrating a DSP unit in the same chip also eliminates the need for a Raspberry pi module which can significantly reduce the overall size and power consumption of the platform. In addition, integration of voltage regulators and ADC will reduce the PCB size and lead to smaller platform which can be placed for example in a pipe for oil industry application or can be implemented under the skin for future potential applications.

5.2.2 Automatic Frequency/Gain/Phase Calibration for TRX IC

Another potential future direction of this work is to implement an automatic frequency/gain/phase calibration algorithm for TRX IC to extract the calibration codes for receiver and transmitter before the actual measurement to compensate for the effect of temperature drift over the time. In the developed platform, the calibration codes for the transmitter and receiver are first extracted by the user manually for each excitation frequency and written to the lookup table in the Raspberry pi. However, these codes may need to be changed for different ambient and temperatures over a long periods of time. Implementing an automated calibration algorithm can reduce the calibration time, in particular for extracting the TX/RX calibration codes at each excitation frequency.

5.2.3 Wider Frequency Range for Dielectric Spectroscopy

Another potential future direction of this work is to increase the frequency range for dielectric spectroscopy. As described in Chapter 1, broadband dielectric spectroscopy has a wide frequency of interest from 10^{-6} to 10^{15} Hz with different applications. Focusing on biomedical applications, extending the bandwidth from 10MHz-2.5GHz to Hz-10GHz could add more information about the MUT's electrolyte (Hz – 100KHz) as well as smaller molecules in the sample (GHz range). The upper limit of the frequency range could be extended using sub-micron technologies for IC fabrication. For the lower limit, as described in chapter one, time domain dielectric spectroscopy method (TDDS) can be implemented as a third receiver channel to process the sensor response from Hz-MHz frequency range.

5.2.4 Multi-Channel Sensor Architecture

Another potential future direction of this work is to redesign the DS sensor in a way to have a shared microfluidic channel with two or more sensing areas as described in Fig 5.1. As described in chapter 4, the developed palmtop platform has two signal paths in the receiver (LBW and HBW) and therefore utilizes two DS sensors. Replacing those sensors with a dual channel microfluidic sensor can avoid an extra sensor loading by the user as well as any measurement errors due to the two different samples in the sensors.

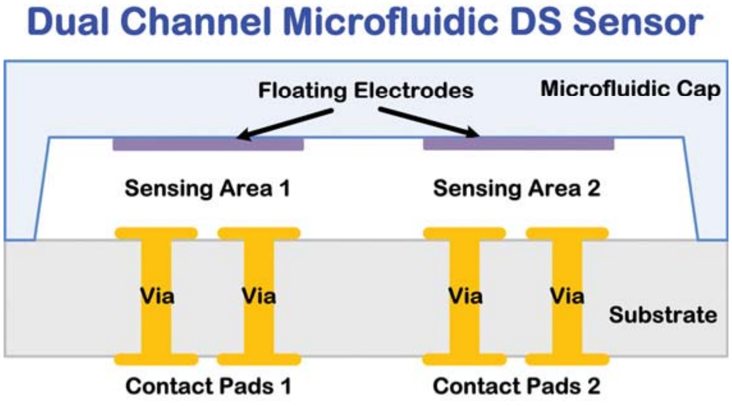

Figure 5.1: Illustration of the dual channel microfluidic DS sensor design.

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