WIRELESS, IMPLANTABLE MICROSYSTEM FOR CHRONIC BLADDER PRESSURE MONITORING

by

STEVE JOSEPH ARMAND MAJERUS

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Dissertation Adviser: Dr. Steven L. Garverick

Acting Adviser: Dr. Swarup Bhunia

Department of Electrical Engineering and Computer Science

CASE WESTERN RESERVE UNIVERSITY

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CASE WESTERN RESERVE UNIVERSITY

SCHOOL OF GRADUATE STUDIES

We hereby approve the thesis/dissertation of

STEVE JOSEPH ARMAND MAJERUS

candidate for the degree of Doctor of Philosophy *.

Committee Chair

Swarup Bhunia

Committee Member

Margot Damaser

Committee Member

Pedram Mohseni

Committee Member

Christian Zorman

Date of Defense

March 17th 2014

*We also certify that written approval has been obtained

for any proprietary material contained therein.

To the memory of Dr. Steven L. Garverick

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WIRELESS, IMPLANTABLE MICROSYSTEM FOR CHRONIC BLADDER PRESSURE MONITORING

Abstract

by

STEVE JOSEPH ARMAND MAJERUS

This work describes the design and testing of a wireless implantable bladder pressure sensor suitable for chronic implantation in humans. The sensor was designed to fulfill the unmet need for a chronic bladder pressure sensing device in urological fields such as urodynamics for diagnosis and neuromodulation for bladder control. Neuromodulation would particularly benefit from a wireless bladder pressure sensor providing real-time pressure feedback to an implanted stimulator, resulting in greater bladder capacity while using less power. The pressure sensing system consists of an implantable microsystem, an external RF receiver, and a wireless battery charger. The implant is small enough to be cystoscopically implanted within the bladder wall, where it is securely held and shielded from the urine stream, protecting both the device and the patient.

The implantable microsystem consists of a custom application-specific integrated circuit (ASIC), pressure transducer, rechargeable battery, and wireless telemetry and recharging antennas. Because the battery capacity is extremely limited, the ASIC was designed using an ultra-low-power methodology in which power is dynamically allocated to instrumentation and telemetry circuits by a power management unit. A low-power regulator and clock oscillator set the minimum current draw at 7.5 μA and instrumentation circuitry is operated at low duty cycles to transmit 100-Hz pressure samples while consuming 74 μA. An adaptive transmission activity detector determines the minimum telemetry rate to limit broadcast of unimportant samples.

Measured results indicated that the power management circuits produced an average system current of 16 μA while reducing the number of transmitted samples by more than 95% with typical bladder pressure signals. The wireless telemetry range of the system was measured to be 35 cm with a bit-error-rate of 10^{-3}, and the battery was wirelessly recharged at distances up to 20 cm.

A novel biocompatible packaging method consisting of a silicone-nylon mesh membrane and a compliant silicone gel was developed to protect the sensor from water ingress while only reducing the sensor sensitivity by 5%. Dynamic offset removal circuitry extended the system dynamic range to 2,900 cm H_2O but limited the sensor AC accuracy to 3.7 cm H_2O over a frequency range of 0.002 – 50 Hz. The DC accuracy of the sensor was measured to be approximately 2.6 cm H_2O (0.9% full-scale). Functionality of wired prototypes was confirmed in feline and canine animal models, and wireless prototypes were implanted in a female calf large-animal model. Measured *in vivo* pressure recordings of bladder contractions correlated well with reference catheters (r =0.893–0.994).

CHAPTER 1

INTRODUCTION

1.1 Motivation

Chronic bladder pressure monitoring is required in urodynamics to diagnose disease and to facilitate neuromodulation for bladder control and rehabilitation. Urology researchers rely on catheters for the vast majority of state of the art bladder pressure measurements. While catheters have been improved by MEMS sensors and packaging, the shortcomings of catheterization remain. Catheters can successfully be used in acute applications but problems arise when catheters are used chronically. In chronic applications, catheterization presents risks to the patient (infection, stone formation), limits patient mobility, and reduces the patient's quality of life.

The use of catheters in urodynamics is also limited because symptomatic bladder leakage is often irreproducible in a static clinical setting [1]. Some bladder symptoms might be induced through ambulation or other motional tasks, and clinicians must rely on patient reporting of these symptoms [2]. Even if a diagnosis is made, long-term confirmation of the correctness and efficacy of treatment is difficult due to the lack of chronic, tether-free bladder pressure sensors.

Recently, neuromodulation has emerged as an important urological pursuit, especially as it can effectively arrest reflex bladder contractions and overactive bladder activity in patients [3, 4]. Existing functional electrical stimulation (FES) systems, including the Medtronic Interstim® system, operate in an open-loop fashion by constantly stimulating a set of nerves. The main

drawback of such devices is patient habituation to constant stimulation. As the effectiveness wanes, frequent doctor visits are required to adjust stimulation parameters.

Closed-loop, or conditional, stimulation is only activated when the bladder state demands it and is more effective than continuous stimulation, leading to increased bladder capacity [5] while using less overall electrical power [6]. Currently, conditional stimulation has only been used for acute research purposes using catheter-based systems since an implantable chronic bladder pressure sensor is unavailable.

Both urodynamics and neuromodulation would be enhanced by a wireless, implanted bladder pressure sensor that could send real-time bladder pressure telemetry to an external receiver. Such a device would enable clinicians to properly diagnosis and monitor bladder disease in real-world environments. Moreover, the telemetry could be sent directly to another implanted device, such as a modern neurostimulator. The devices could be chronically implanted, permitting closed-loop control of bladder dysfunction. Finally, the pressure sensing implant could find application in a broader set of fields, for example gastroenterology and gynecology.

1.2 Examination of Existing Wireless Pressure Sensors

While a few published examples of implantable pressure sensors date back to the 1960s [7], there has been renewed interest in the field in the past decade. A summary of published implantable pressure sensors is shown in Table 1-1. The existing published work has been mostly focused on measuring vascular, cranial, or ocular pressure using devices which are passive or powered by radio-frequency (RF) electromagnetic fields. Devices intended to measure pressure in the bladder, gastro-intestinal tract, or other deep organs are typically designed for acute use, meaning they operate for a period of several days before being forcibly or naturally explanted. Generally, RF-powered devices are not suitable for applications requiring an implantation depth

(minimum distance from outer surface of skin to implant) greater than about 10 cm, due to practical and regulatory limitations.

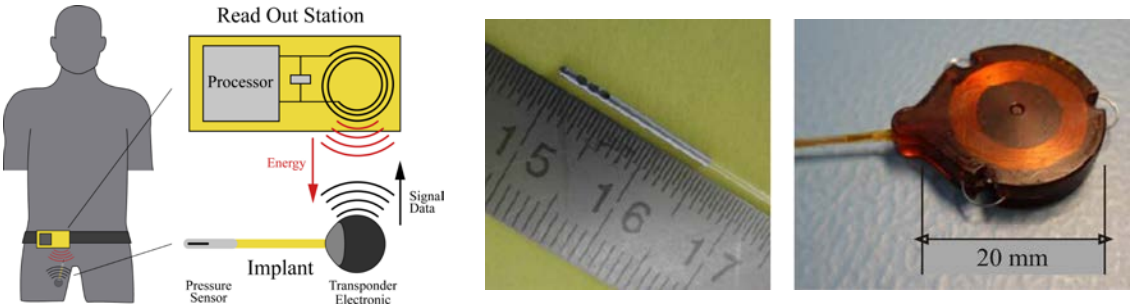
TABLE 1-1. SUMMARY OF EXISTING IMPLANTABLE PRESSURE SENSORS.

Ref.	Application Area	Size (mm x mm x mm)	Current Draw (μA)	Power Source	Lifespan per charge (days)	Wireless Telemetry	Transmit Distance (cm)	Sample Rate (Hz)	Resolution
[8]	Urology	13.6 x 2 disc	1000	Wired	N/A	None	wired	Continuous	mV output
[9]	Ocular	3.2 x 1.5 x 0.5	0	Passive	N/A	250 MHz Phase Dip	0.6	Continuous	7 bit
[10]	Cardio-vascular	220 x 20 x 4	150	RF	N/A	133 kHz LSK	10	30	8 bit
[11]	Cranial	13 x 4.5 cylinder	1000	RF	N/A	27.12 MHz LSK	3	< 1	8 bit
[12]	Cardio-vascular	10 x 5 mm cylinder	*	RF	N/A	434 MHZ FM	3	Continuous	6 bit (est.)
[13]	Cardio-vascular	15 x 19 x 6	*	RF	N/A	13.56 MHz LSK	*	*	*
[14]	Cranial	6 x 28 x 2	1200	RF	N/A	4 MHz LSK	0.45	40	*
[15]	Cardio-vascular	12 x 6 x 0.2	113	RF	N/A	4 MHz LSK	4	*	6 bit
[16]	Cardio-vascular	9 x 2 x 7	150	RF	N/A	433 MHz FSK	2	2000	8 bit
[17]	Urology	29 x 7 x 6	610	RF	N/A	132 kHz LSK	8.5	10	9 bit
[18]	Cardio-vascular	20 x 2.6 cylinder	150	RF	N/A	6.78 MHz LSK	3	10	6 bit
[19]	Urology	6.5 x 18 cylinder	166	Primary Cell	3 (planned)	planned	3 (planned)	*	*
[20]	Urology	25 mm sphere	417	Primary Cell	14	434 MHz FSK	100	0.003	6 bit
[21]	Urology	40 x 5 mm cylinder	77	Primary Cell	7	None	NA	2	5 bit
[22]	Gastro-intestinal	27 x 19 x 19	535	Primary Cell	2.3	434 MHz ASK	500	25	10 bit
[23]	Ocular	30 x 4 x 0.3	0.0045	Capaci-tor	1	2.4 GHz OOK	10	0.003	7 bit
[24]	Neurology	25 x 3.15 cylinder	33	Second-ary Cell	4.2	400-460 MHz QPSK	10	90	4 bit

**parameter not listed in publication*

One notable example of an RF-powered vascular pressure monitor is described by Cleven et al. [10], and represents the culmination of over one decade of work. This system consists of a thin, micro-tip catheter bonded to a transponder unit, as shown in Figure 1-1. The micro-tip catheter contains a monolithic pressure sensor and application-specific integrated circuit (ASIC). The catheter resides in the femoral artery while the transponder unit is implanted subcutaneously to allow for RF powering. The system can be as far as 10 cm from the external unit,

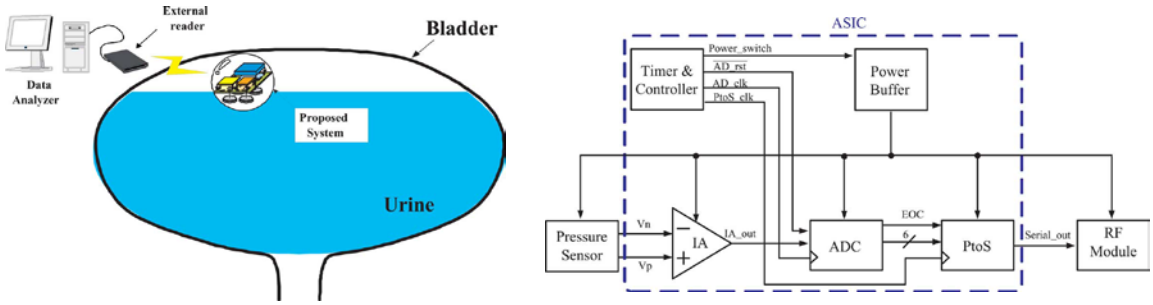
which provides RF power at 133 kHz and receives load-shift keyed (LSK) reverse telemetry from the implanted transponder. The system achieves 8-bit resolution at a sample rate of 30 Hz, and is suitable for chronic applications, provided the external transceiver provides constant power.



(a) (b)

Figure 1-1. Details of implantable microsystem to monitor blood pressure: (a) schematic overview of entire system, and (b) detailed photograph of implantable device (from [10]).

Another system, reported by Wang et. al. [20] is a fairly small, battery-powered device which can measure lumen (internal) bladder pressure. This system is designed to implement ambulatory and cost-effective acute cystometry to diagnose bladder dysfunction. The concept system consists of an ASIC, pressure sensor, and RF module, which are integrated with coin cell batteries onto a substrate and packaged in a buoyant sphere, as conceptualized in Figure 1-2. The implant would ultimately measure 25 mm in diameter and the batteries would power the system for 14 days before they are depleted. The sensing dynamic range is 6 bits and the RF transmitter can send telemetry as far as 1 m. Low average power consumption is achieved through a very low duty cycle of only one sample per 5 minutes (3 mHz).



(a) (b)

Figure 1-2. Details of implantable system to monitor bladder lumen pressure: (a) schematic overview of entire system, and (b) block diagram of sensor ASIC (from [20]).

Perhaps the best known example of an implantable, rechargeable device is the BION implantable neurostimulator [24], shown in Figure 1-3. Although not strictly intended for pressure sensing, the BION has been tested with an integrated pressure sensor. The latest incarnation of the device, the battery-powered-BION (BPB), uses a rechargeable (secondary) lithium-ion cell for power and transmits telemetry using an advanced binary quadrature phase-shift-keyed (BPSK) method at frequencies from 400 – 600 MHz. The BPB transmits 4-bit pressure information at a rate of 90 Hz. The BPB is intended for implantation in muscles, and can operate for over 4 days on a single charge. The implanted BPB can be wirelessly recharged as far as 10 cm from an external device transmitting RF energy at 125 kHz. Since it can be recharged, the BPB is suitable for chronic application, although its dimensions, weight, and pressure sensing dynamic range are not well matched to use in the bladder.

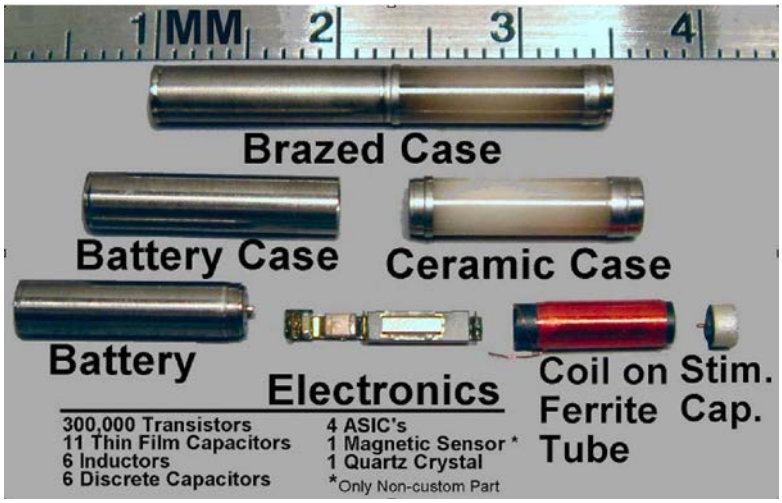


Figure 1-3. Exploded view of BPB stimulator. The assembled device is a 25 mm cylinder (from [24]).

1.3 Challenges and Constraints for a Chronically Implanted Bladder Pressure Sensor

Development of an implantable pressure sensor for chronic application in the human bladder requires adherence to strict constraints on size, implantation depth, packaging, and overall system efficacy. The requirements for the implanted device in this work were determined through literature review [25] and consultation with Dr. Hui Zhu, Chief of Urology at the Louis Stokes Cleveland VA Medical Center (LSCVAMC). A distillation of the important constraints is listed in Table 1-2.

To minimize patient risk and discomfort, the implanted device must be delivered in a minimally-invasive manner using existing urological instruments. Furthermore, the implanted device must be thin enough to fit beneath the mucosa layer, where it is shielded from the urine stream, to prevent mineral encrustation and stone formation. The device powering and telemetry methods must accommodate an implantation depth of up to 20 cm when implanted in obese patients. Finally, the device packaging must be biocompatible and the overall system should not limit patient mobility while enabling ambulatory operation.

TABLE 1-2. SUMMARY OF IMPLANTABLE PRESSURE SENSOR CONSTRAINTS.

Driving Constraint	***System Implication***
Implantation via 24-French[†] cystoscope	Device maximum dimension = 8 mm
Sub-mucosal implantation site	Device thickness = 4 mm
Implantation in obese patients	Implantation depth = 20 mm
Suitable for urodynamics / neuromodulation	Pressure range = 200 cm H_2O
Reject aliasing of high-frequency motion artifacts	Max. sampling frequency = 100 Hz
Chronic implantation (> 14 days)	Biocompatible packaging
Maximize patient mobility	Wireless operation

[†] The French scale is used to define catheter sizes, with the equivalent diameter in mm obtained by dividing the French size by 3. Cystoscopes can be ovoid, so the French size corresponds to the length of the major diameter.

1.4 Research Contribution

The goal of this work was the development of a wireless intra-cavity micro-manometer (WIMM) which can be implanted submucosally, between the bladder muscle and the self-healing mucosa layer, in a human bladder. The system concept consisting of implantable device and external power/data transceiver is depicted in Figure 1-4. The device must be quite small to enable minimally-invasive surgery in the proposed implant location. Typically, RF-powering would be used in lieu of a battery, but it is impractical to power a device implanted that deep in the body solely and continuously through an inductive link. Instead, the WIMM is powered by a small rechargeable onboard battery. An inductive antenna in the implant functions as a power link to an external wireless battery charger used during recharge, when the patient is sleeping, for example. A second antenna operating at a higher frequency transmits pressure telemetry to an external receiver. Based on a review of the published literature, this would be the first example of a chronically-implantable, wireless bladder pressure sensor capable of real-time pressure telemetry to an external recorder or neuromodulation controller.

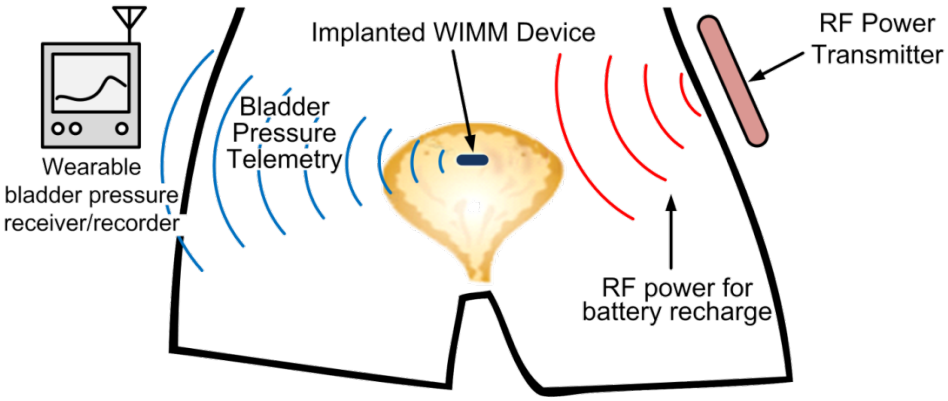


Figure 1-4. Illustration of WIMM system concept. The WIMM is implanted within the bladder wall and transmits telemetry to an external receiver. Intermittent RF recharge is used to maintain the battery charge.

The major contribution of this work can be classified into the following sub-contributions:

1. The design, fabrication, and testing of an ultra-low power system-on-chip ASIC (WIMM ASIC) that enables a deeply implanted pressure monitor requiring few external components besides a MEMS pressure sensor and telemetry passives.
2. The integration of the WIMM ASIC and other components into a wireless microsystem suitable for cystoscopic implantation. Design of a microsystem packaging technique to ensure biocompatibility and pressure sensitivity without significantly adding to the implant volume. Finally, design of an external radio capable of picking up the weak, intermittent transmissions from the implant, and a wireless battery recharger capable of recharging the implantable system even in obese patients.

1.4.1 *Contribution 1 – Ultra-low-power ASIC Design*

Compared to the specifications for existing devices in Table 1-1, the WIMM ASIC will perform better especially in the context of chronic, wireless bladder pressure sensing. The ASIC will deliver real-time telemetry at greater sample rates to avoid aliasing of motion artifacts and to reduce sample latency for closed-loop control applications. The ASIC current draw will be lower than all published examples of implantable pressure sensors delivering real-time telemetry, and

this will be achieved through novel circuit architecture and an adaptive rate transmitter specifically tuned to the dynamics of bladder pressure signals. Finally, the ASIC will incorporate useful features for chronic applications: wireless battery recharging, automatic DC baseline stabilization to mitigate sensor drift, and a wirelessly-commanded standby mode.

1.4.2 *Contribution 2 – Complete Wireless Pressure Sensing System*

A wireless, implantable prototype will be designed to integrate the low-power ASIC with other system components such as a battery, pressure sensor, telemetry, and recharge antennas. The microsystem dimensions will be sufficiently small to permit implantation with 24-French urologic cystoscopes into a suburothelial pocket within the bladder. The implant will be packaged by a custom process incorporating biocompatible materials to protect the electronic components from an aqueous biological environment for acute studies. A new method for creating a watertight pressure port reinforced by a tough membrane will be applied to protect the pressure sensor without attenuating physiological pressure signals. The performance of the electronics and packaging method will be evaluated *in vivo* using a wired version of the sensor with feline and canine animal models.

Maintaining such a small implant size requires tradeoffs in wireless performance, however, and the telemetry from the WIMM will be weak and highly intermittent. The external data receiver will be designed to be both sensitive and quick, so that it may lock into the transmitted signal faster than typical, coherent detection methods. Finally, by incorporating amplitude-shift-modulation (ASK) into the class-E amplifier which produces an otherwise static RF recharge field, shutdown commands can be sent to the WIMM implant. The wireless performance of the system will be verified by calculating the received bit-error-rate at various transmission distances,

and wireless battery recharge will be demonstrated at distances sufficient for implantation in obese humans.

1.5 Relevant Background Technology

1.5.1 *Wireless, implantable devices for biomedical applications*

Uses for wireless, implantable sensors span the breadth of the medical field, but several niche applications have been the focus of intense research and development. Neuroelectronic devices [26], [27], intraocular pressure sensors [9], [23], wireless endoscopes [28] and cardiac stent monitors [29], [13] account for a large portion of published work. Every device has unique characteristics determined by its application, but the basic electronic circuitry and system construction is fairly homogenous across the field.

As a starting point, implantable sensors can be classified based on the powering source for the device. Passive devices, such as shown in Figure 1-5a, contain no active circuitry and are interrogated through their influence on an externally-generated magnetic field [9], [23], [29], [30]. RF-powered devices, such as shown in Figure 1-5b, account for the majority of implantable devices, as they contain active circuitry for instrumentation and telemetry but maintain a small size by omitting onboard power storage [10] – [18], [26], [27]. Finally, some examples of miniature battery-powered implants exist, such as shown in Figure 1-5c, but they are typically designed for acute use, notably wireless endoscopy [28], and non-rechargeable batteries are often used for simplicity [20], [21], [22], [24], [31], [28].

(a) (b) (c)

Figure 1-5. Different types of implantable sensors: (a) a passive sensor, from [9], (b) an RF-powered sensor, from [16], and (c) a battery-powered implantable sensor [22].

Implantable sensors which contain active circuitry typically employ one or more ASICs to keep the system size as small as possible. Some designs effectively use only discrete, commercial ICs to build low-cost, mid-size devices. Regardless of the level of custom circuitry, most active implantable devices share a common platform of system-level building blocks. A generic implant system block diagram is presented in Figure 1-6, which shows that the implanted device contains circuitry necessary for power management, transduction and amplification, analog-to-digital conversion, and wireless telemetry.

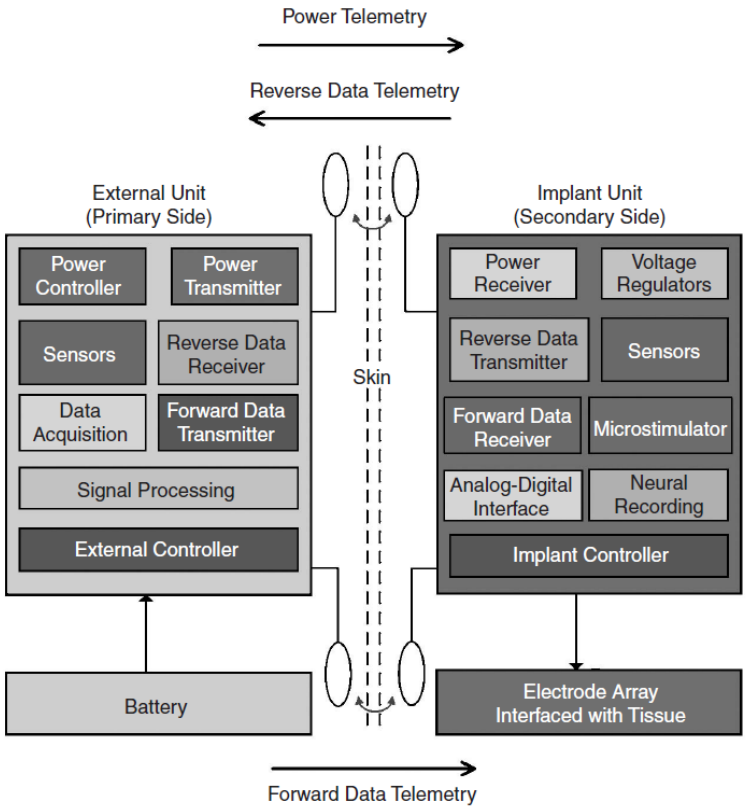


Figure 1-6. A generic block diagram for an implantable sensor containing active circuitry (from [32]).

RF-powered systems such as the one in Figure 1-6 use RF-DC conversion circuits to capture and regulate incoming electromagnetic energy. The available energy is limited, so both RF- and battery-powered implantable devices require low-power circuitry. The transduction, amplification, and digitization circuitry typically achieves a resolution less than 10 bits due to power constraints, but this is adequate for the application.

Unless high data-rate telemetry is required, RF-powered devices can efficiently provide reverse telemetry over the powering link using load-shift-keying (LSK). Battery-powered devices employ a traditional RF transmitter, and either use custom protocols or commercial standards such as IEEE 802.15.4 (ZigBee) [33]. Transmission consumes significant power so implantable systems employ data compression, very low sample rates, or burst transmission to save power, as the application allows.

1.5.2 *MEMS Pressure Sensors*

Silicon micromachining techniques have been widely used to enhance and miniaturize commercial pressure sensors. Modern MEMS pressure sensors are available as monolithic silicon dice and can be easily obtained from commercial vendors. Capacitive pressure sensors are widely reported in academic publications, but piezoresistive MEMS pressure sensors are much more commercially available and can operate using simpler interface electronics. Piezoresistive sensors are generally configured as a Wheatstone bridge, with the piezoresistors diffused into a flexible, silicon membrane. Implantable applications require an absolute pressure sensor, typically constructed with one side of the membrane exposed to a sealed vacuum cavity, as shown in Figure 1-7a with equivalent electrical schematic shown in Figure 1-7b. Generally the sensor is further packaged to ensure robustness, with the pressure-sensing side of the sensor die directly or indirectly exposed via a flexible diaphragm to the pressure source [34].

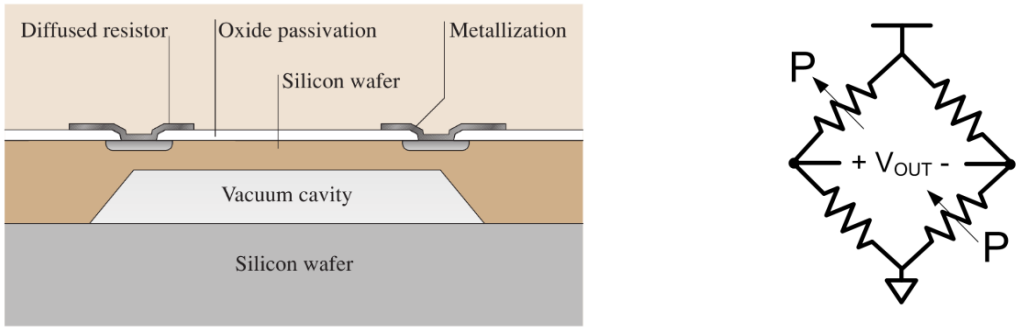


Figure 1-7. (a) Cross-section of MEMS pressure sensor (from [34]) and (b) equivalent circuit of piezoresistive sensor.

1.5.3 *Micro-battery technology*

The miniaturization of electronics has outpaced battery technology over the past few decades, but recent advances in micro-battery technology have made small, battery-powered implantable devices feasible. While battery chemistries are quite varied, there are currently very

few types of batteries that can be considered for an implantable device. In general, a wireless implantable device requires a battery that is physically small yet can store a reasonable amount of charge and provide levels of current in excess of 1 mA when needed. If the battery is a secondary (rechargeable) cell, then the total capacity should not degrade too quickly as the cell ages due to charge/discharge cycles.

Currently there are five commercial battery technologies that are attractive for use in a miniature implanted device. The capacity vs. volume for different types of batteries is plotted in Figure 1-8 to determine the scalability of the various technologies. The plotted points correspond to available batteries, while the trendlines predict the scalability of the various technologies. To keep the implant small, the battery must store a large amount of charge per unit volume, and the cell packaging should be negligible to minimize the cell size.

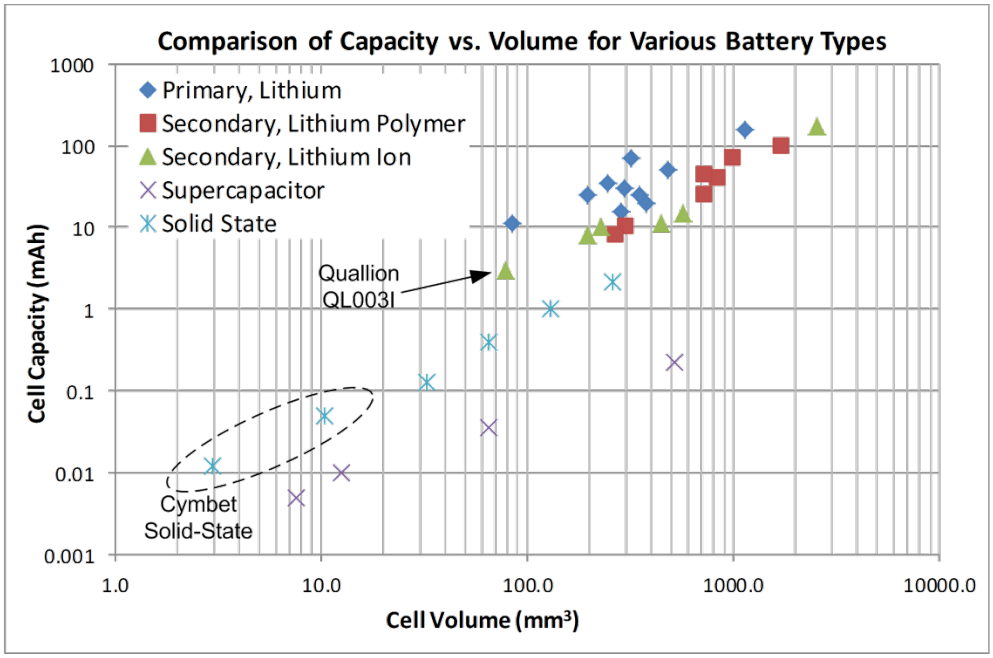


Figure 1-8. Capacity vs. volume for several commercially-available battery technologies. The plotted points correspond to existing commercial cells while the trendlines predict the scalability of the battery (Data compiled from [35], [36], [37]).

Primary lithium-based chemistries offer the largest charge density and best discharge characteristics, but these cells are not widely available with volume less than 100 mm^3. Secondary lithium-ion and lithium-polymer cells have about one-third the charge density of lithium cells, but can be recharged. Typically lithium-based secondary cells are not available below 200 mm^3, with the exception of the Quallion QL003I [38]. Solid-state batteries available from Cymbet [39] have a lower charge density but are available in smaller sizes and can be wired in parallel to achieve a larger capacity. Supercapacitors have a charge density at least one order of magnitude lower than electrochemical cells and have a linear discharge profile, which complicates full usage of the stored charge.

1.5.4 *RF powering for wireless implantable devices*

RF powering is a method for wirelessly transferring energy between coupled inductors and is a widely-used powering method for miniature wireless sensors [10] – [18], [40]. RF powering works by generating a strong magnetic field at a fixed frequency with a large external coil. The magnetic field induces a current within a smaller, tuned inductor located in the wireless sensor. The arrangement can be considered as a voltage transformer, but with a non-ferrous core material and much lower primary-secondary coupling coefficient, *k*. A typical schematic for an RF-powered device is shown in Figure 1-9.

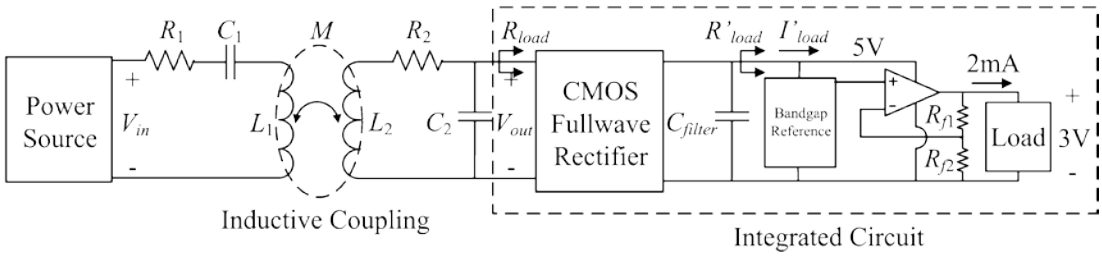


Figure 1-9. Schematic of typical wireless power coupling to implanted integrated circuit. Power is transferred via the mutual inductance M between coils L_1 and L_2 and is rectified for use in DC circuits (from [40]).

Coil L_1 is driven with fixed AC input voltage V_{IN} and is tuned to resonance with C_1. The wireless sensor has a complementary resonant circuit implemented by L_2 and C_2. The current flowing through L_1 induces a current into L_2 via the mutual inductance *M*. Rectification of the induced current produces a DC voltage which can be used to power the sensor. In [40] it is shown that the voltage gain across the link is given by

$$\frac{V_{OUT}}{V_{IN}} = \frac{\omega^2 L_2 M}{\left(R_1 R_2 + (\omega M)^2 + \frac{R_1 \omega^2 {L_2}^2}{R_{LOAD}}\right)}, \quad 1.1)$$

with

$$R_{LOAD} = \frac{R'_{LOAD}}{\sqrt{2}}, \quad 1.2)$$

the mutual inductance defined as

$$M = k\sqrt{L_1 L_2}, \quad 1.3)$$

and *k* representing the coupling coefficient between the two coils. The factor *k* is a unitless value ranging from 0 to 1 (no coupling to full coupling). Coupling coefficient is determined by the geometric parameters of the coils and the distribution of magnetic flux between them. Consequently *k* is highly variable with orientation and separation distance between the coils.

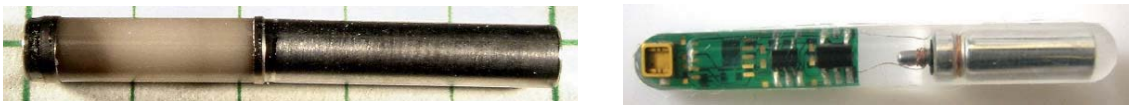
Besides wireless voltage gain, power efficiency is critical for the feasibility of continuous RF powering in a given application. The power transfer efficiency, denoted by η_{op}, represents the ratio of power received by the internal coil relative to the power burned in the external coil. Based on the inductive coupling structure of Figure 1-9, the maximum power transfer efficiency η_{op-max} is derived in [41] as

$$\eta_{op-max} = \frac{k^2 Q_1 Q_2}{\left(1 + \sqrt{1 + k^2 Q_1 Q_2}\right)^2}, \quad 1.4)$$

where Q_1 and Q_2 represent the quality factors of L_1 and L_2, respectively. Operating at peak efficiency is only possible when the system impedance matches a specific value, so in practice implantable systems are generally less efficient than the optimum. Miniature implantable sensors operating at separation distances greater than a few mm typically have $k < 0.1$ and correspondingly $\eta_{op} < 10$ % ([10] – [18], [40]). Even systems with carefully optimized coil geometries have typical efficiencies well below 1 % at separation distances greater than 5 cm [41]. In a typical RF-powered setup, the external coil is driven by a line-powered, multi-Watt Class-E amplifier to generate a few milli-Watts at the internal coil.

1.5.5 *Multi-layer, non-hermetic packaging for biocompatibility*

Historically, implanted devices have been packaged in hermetically-sealed packages consisting of biocompatible materials such as glass, metal, and ceramic which are brazed, welded, or fused to form an air- and water-tight seal. Some small devices such as the battery-powered BION [24] use a hybrid technique as shown in Figure 1-10a, but hermetic packaging in general adds cost, weight, and size to the final packaged device. Non-hermetic packaging techniques are an attractive option for the next generation of tiny, implantable electronic devices. Non-hermetic packaging uses a combination of materials which are hydrophobic (but not totally impermeable to water vapor [42], [43]) to reduce package size and weight by up to an order of magnitude [44] as shown in Figure 1-10b. Proper layering of the materials can potentially achieve high levels of biocompatibility, structural integrity, and operational lifetime.



(a) **(b)**

Figure 1-10. Hermetic and non-hermetic implantable devices: (a) the battery-powered BION uses a hybrid ceramic/titanium housing (from [24]); while (b) a low-cost implantable device uses PDMS as the only packaging material (from [21]).

Studies of non-hermetic encapsulants have identified a host of suitable polymeric materials which provided varying levels of performance depending on the application. These materials include polydimethylsiloxane (PDMS), silicone gels, polyimides, filled epoxies, and poly(p-xylylene) polymers, notably poly(chloro-para-xylylene) (also called Parylene C) [42], [43], [45], [46], [47]. Many of these materials are not biocompatible, so PDMS is often used as the outermost layer in implantable devices. Some devices use PDMS as the only encapsulation agent, but they are only intended for acute use [21], [22], [28]. Accelerated testing of some multi-layer non-hermetic packages indicates that an implant lifespan in excess of 5 years is feasible [48].

CHAPTER 2

WIRELESS IMPLANTABLE MICROSYSTEM

The specifications for the WIMM were chosen based on the desired functionality, implant location, implant method, and as a compromise between low power consumption and sensing accuracy, with basic system requirements summarized in Table 1-2. The microsystem electronics were designed specifically to meet the size limitations imposed by the application and limited by existing, commercially-available battery technology. A summary of the proposed specifications for the WIMM relative to existing implantable pressure sensors is shown in Table 2-1 below.

TABLE 2-1. PROPOSED SPECIFICATIONS RELATIVE TO EXISTING IMPLANTABLE PRESSURE SENSORS.

Ref.	Dimensions (mm)	Current Draw	Shut-down Mode	Power Source	Lifespan / charge	Wireless Telemetry	Transmit Distance	Sample Rate	Resolu-tion (cm H_2O)	Range (cm H_2O)
[10]	220 x 20 x 4	150 µA	N/A	RF	N/A	133 kHz LSK	10 cm	30 Hz	1.4	367
[17]	29 x 7 x 6	610 µA	N/A	RF	N/A	132 kHz LSK	8.5 cm	10 Hz	0.4	306
[20]	25 mm sphere	417 µA	No	Prima-ry Cell	14 days	434 MHz FSK	100 cm	3 mHz	3.1	351
[21]	40 x 5 mm cylinder	77 µA	No	Prima-ry Cell	7 days	None	NA	2 Hz	9.2	295
[22]	27 x 19 x 19	535 µA	Yes	Prima-ry Cell	2.3 days	434 MHz ASK	5 m	25 Hz	1.0	1022
[23]	30 x 4 x 0.3	4.5 nA	No	Capaci-tor	1 days	2.4 GHz OOK	10 cm	3 mHz	1.7	82
[24]	25 x 3.15 cylinder	33 µA	No	Sec-ondary Cell	4.2 days	400-460 MHz QPSK	10 cm	90 Hz	13.6	816
This work	17 x 7 x 4	15 µA	Yes	Sec-ondary Cell	8.3 days	27.12 MHz FSK / 4 MHz ASK	30 cm	100 Hz	0.8	2,200

The comparable sensors were selected from Table 1-1 by eliminating sensors which were not wireless, had wireless transmission distances less than 10 cm, or did not have reported measured results. Compared to existing work, the WIMM is more appropriate for chronic application. By integrating wireless recharge circuitry and designing for a low average current draw, the use of a rechargeable secondary cell is enabled. Including a shutdown mode means that the implant battery does not discharge during packaging, implantation, and inactive periods. The transmission distance of 30 cm is slightly below the average among existing work, but is sufficient for transmission through the tissue of obese patients. A pressure sensing resolution of less than 1 cmH_2O is in line with existing implantable systems, but a much larger total dynamic range of 2,200 cmH_2O ensures accurate operation in a chronic application, where baseline pressure drift may change due to scarification or migration of the implant.

2.1 Wireless microsystem for chronic implantation

The ultimate vision for the WIMM, as depicted in Figure 1-4, is a wireless pressure sensor that is small enough to be chronically implanted within the bladder wall. Onboard power storage permits greater patient mobility, and the implanted battery can be wirelessly recharged during patient rest periods. An external wireless receiver can detect transmitted pressure telemetry, and an RF-powering source can provide coupled energy for battery recharge. A block diagram of the proposed wireless system is shown in Figure 2-1a.

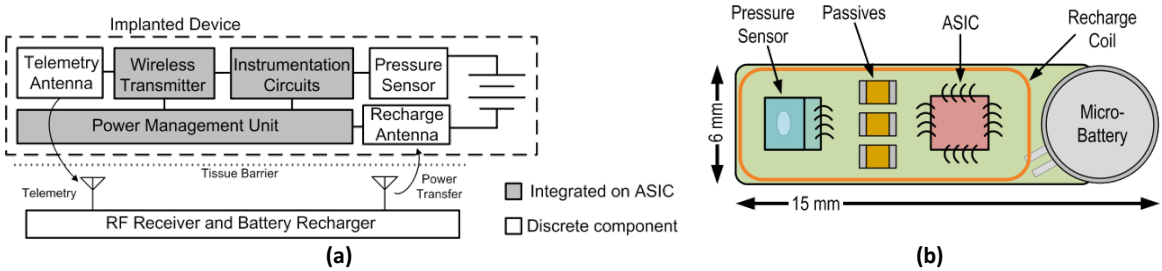


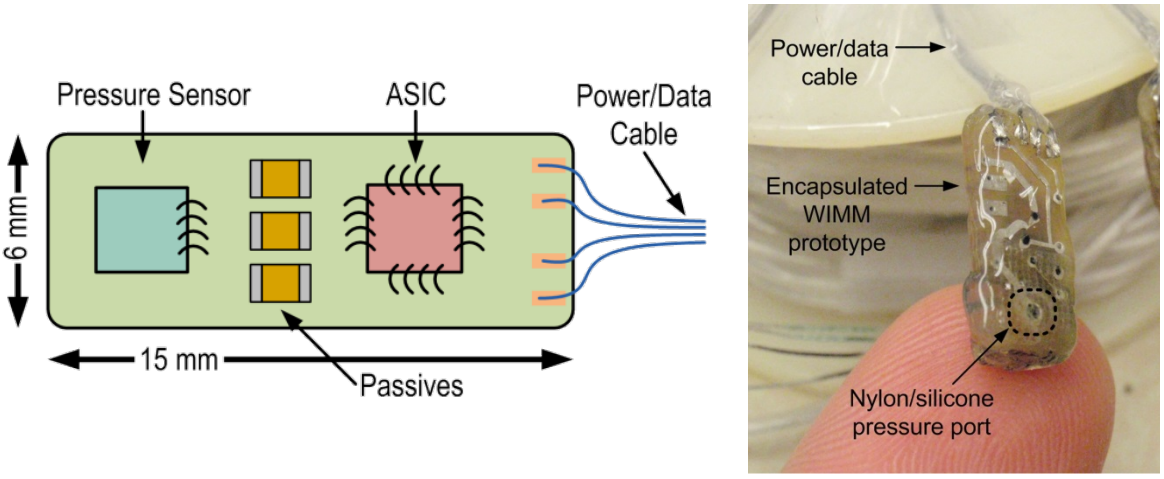
Figure 2-1. Schematic views of the proposed WIMM: (a) system block diagram consisting of implanted device communicating with external RF receiver and battery recharger. A physical layout for the implanted device is illustrated in (b).

The WIMM consists primarily of an ASIC, pressure sensor, and lithium-ion secondary battery. The ASIC integrates the circuitry for pressure measurement, power management and wireless telemetry, and interfaces directly with the piezoresistive MEMS pressure transducer. Wireless telemetry is transmitted using a discrete inductor; battery recharge is accomplished using another, custom-wound coil tuned to a different frequency. The only other microsystem components are a few passive capacitors, used to tune the antennas and to reduce voltage ripple from the battery supply.

The schematic for the microsystem shown in Figure 2-1b depicts the relative sizes of the system components. The battery and associated wireless recharge antenna are the size-limiting factors for the system since they consume over half of the WIMM volume. The implant includes two ferrite rods which improve the wireless recharge efficiency [49] by shielding the inductive recharge coil from the metal battery casing. All circuit elements and the MEMS pressure transducer are affixed to a system PCB. A rectangular solenoidal coil used for wireless battery recharge is wound around the implant perimeter.

2.2 *Wired microsystem for in vivo experimentation*

For the initial *in vivo* applications of the WIMM, a wired prototype was developed. The use of a power/data cable was justified to increase the success rate of the early studies, and to mitigate the requirement for accurate, wireless data transmission. Furthermore, the device was implanted through an incision in the bladder detrusor (not transurethrally as ultimately envisioned), so the presence of the power/data cable did not impede normal bladder function. The wired microsystem consisted of the same electronics as the wireless WIMM, but arranged on a slightly larger PCB to simulate the extra volume otherwise occupied by the battery. An illustration of the microsystem arrangement is shown in Figure 2-2a, and a photo of the final, packaged system is shown in Figure 2-2b.



(a) **(b)**

Figure 2-2. The wired WIMM used in *in vivo* trials: (a) illustration of microsystem internal component arrangement and (b) a photo of the packaged, wired microsystem.

CHAPTER 3

ASIC OVERVIEW, POWER MANAGEMENT, AND INSTRUMENTATION AMPLIFIER

The size constraints of the implantable bladder pressure sensor require that the active circuitry be highly integrated, while consuming very little power. High integration minimizes off-chip passive components and wirebonds, which require a surprising amount of area within an implantable device. Low power consumption enables the use of a micro-battery as the power source for the system. Standard instrumentation and digital circuitry can meet ultra-low-power consumption requirements, but peripheral components such as bias circuitry, regulators and clock generators are sometimes omitted from these specifications. Furthermore, the power consumption of wireless transmission can eclipse that of the rest of the electronics. The WIMM ASIC was designed for ultra-low-power operation at the system level, and achieves that goal mainly through precise use of low-duty-cycle operation.

In this chapter, and overview of the ASIC design is presented, then power management and the frontend instrumentation amplifier is described in detail.

3.1 WIMM ASIC Block Diagram

The WIMM ASIC block diagram is presented in Figure 3-1. The ASIC circuitry includes pressure sensing and telemetry circuits, power control circuits, and RF battery recharge circuits.

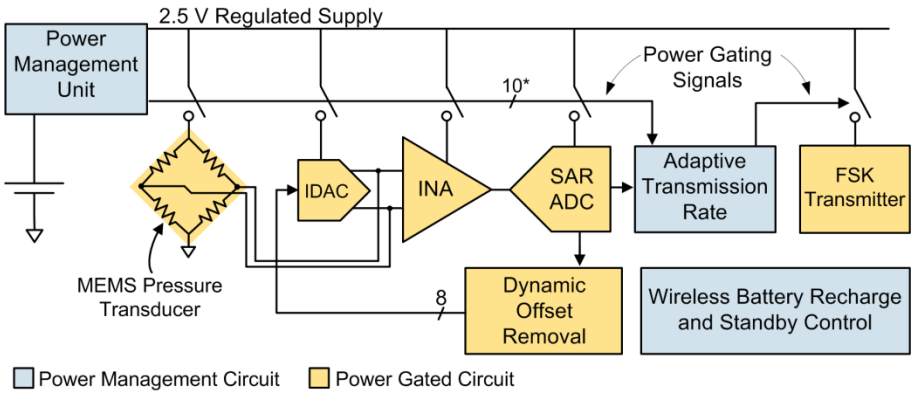


Figure 3-1. Block diagram of the WIMM ASI. Circuits are categorized as power management (blue) of power gated (yellow).

The pressure sensing and telemetry circuits form the instrumentation aspect of the bladder pressure sensor. The circuitry interfaces with a MEMS piezoresistive absolute pressure transducer (EPCOS C29 [50]). The piezoresistive sensor type was selected over capacitive due to greater process maturity and commercial availability. The sensor is excited with an intermittent stimulus to avoid large static power dissipation.

A programmable-gain instrumentation amplifier (PG INA) and successive-approximation analog-to-digital converter (SAR ADC) amplify and convert the transducer output to an 8-bit binary sample. The sample is sent to an auto-offset removal processor which continuously removes pressure baseline drift to maximize the resolution of the instrumentation system. Finally, each sample is inserted into a 14-bit packet in a custom format for robust wireless communication, and the packet is transmitted using a frequency-shift-keyed (FSK) transmitter and a 3-mm diameter, 3.3-µH surface-mount, inductive antenna. An adaptive rate transmitter with parameters customized for bladder pressure signals determines the optimum transmission rate of the 27.12-MHz frequency-shift-keyed (FSK) transmitter.

The key power-saving feature of the WIMM ASIC is the power management unit (PMU). The PMU is a suite of very low power circuits that are always running in the background but sequentially turn on and off the vital instrumentation and telemetry circuits such that power is not consumed when it is not needed. At the minimum duty cycle the system power consumption is minimized but only 100 samples per second are acquired. An adaptive transmission rate circuit determines whether or not a newly-acquired sample should be transmitted, such that further power is saved by transmitting at rates from 1.5 – 100 Hz. This technique could potentially add some latency in sample transmission, but the circuit was designed for a fast attack speed so that important samples are transmitted within 1 ms of acquisition.

A separate section of the ASIC is devoted to RF wireless battery recharge that operates at 3 MHz to prevent interference with the 27.12 MHz FSK telemetry. The battery recharge circuits capture RF energy that is provided by an external power transmitter in a resonant LC tank circuit and converts the energy to a regulated battery recharging current. The integrated battery recharge circuitry stops charging the micro-battery when the capacity is reached, and includes voltage limiting circuitry to protect the system in case more RF energy is received than is needed. An amplitude-shift-keyed (ASK) command decoder receives commands sent to the WIMM as ASK modulation of the RF recharge field. If a shutdown command is received, the whole system is put into nanowatt standby mode. The system wakes from standby if the external RF field is continuously applied for more than 3 seconds.

3.2 Power Management Unit

The WIMM achieves ultra-low-power operation through a combination of individual, low-power circuits as well as an architecture which leverages the speed advantage of CMOS circuitry compared to the rate of physiological pressure change. The power state of the WIMM is con-

trolled by a power management unit (PMU) which allocates power as needed to instrumentation circuits. The PMU also provides means for wirelessly recharging the implanted battery and wirelessly commanding the system into an extremely low power “standby” state.

The key power-saving concept for the PMU is that of the “sample conveyer”, in which the sensed pressure information is conveyed between successive instrumentation stages in the form of either charge or a digital value. With this technique, circuits that have already finished processing the sample can be switched off, and other circuits can remain in a low-power state until they are needed. Generally this approach is suitable for any low-power device in which the speed of the circuits greatly exceeds the required sample rate of the sensor. For simplicity the PMU on the WIMM ASIC simply uses a fixed pattern state machine to generate the power control signals.

3.2.1 *Power Management Unit Design and Operation*

The PMU circuits are always running and set the baseline current draw of the system. The power consumption of these circuits was reduced as low as possible while maintaining acceptable performance and matching. The power consumption of other analog circuits is reduced by a digital finite state machine which turns the instrumentation circuitry on/off in a pipelined manner to minimize the active time for each stage. A block diagram of the PMU is shown in Figure 3-2, and it consists of analog circuits for regulating the battery voltage, a low-power clock oscillator, and a power management state machine. The total current draw for the PMU is about 3.4 μA.

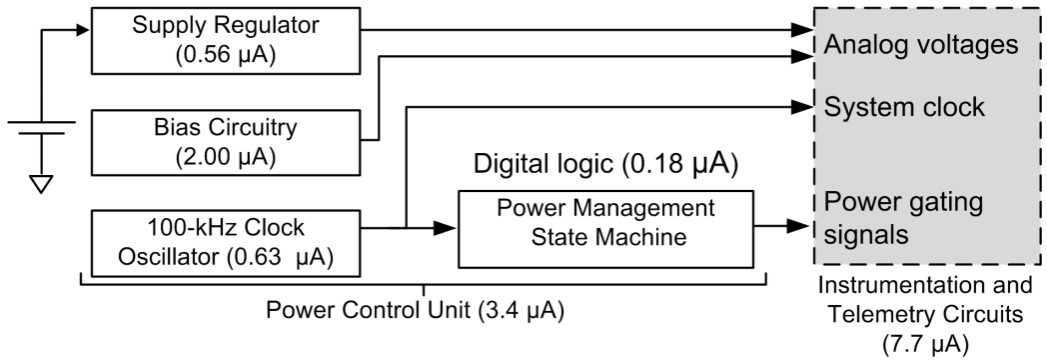


Figure 3-2. Block diagram of the individual circuits within the power management unit (after [51]).

3.2.2 *Low-Quiescent-Current Linear Voltage Regulator*

Because the wireless sensor is powered by a secondary cell with fairly large internal resistance, the battery voltage changes rapidly with changing load current and slowly as the stored charge is depleted. The PMU uses a simple linear voltage regulator to mitigate this effect so as to reduce instrumentation circuit and clock oscillator voltage coefficient requirements. The regulator schematic is presented in Figure 3-3 with device sizes in Table 3-1. Device sizes for the startup circuits are not critical and have been omitted.

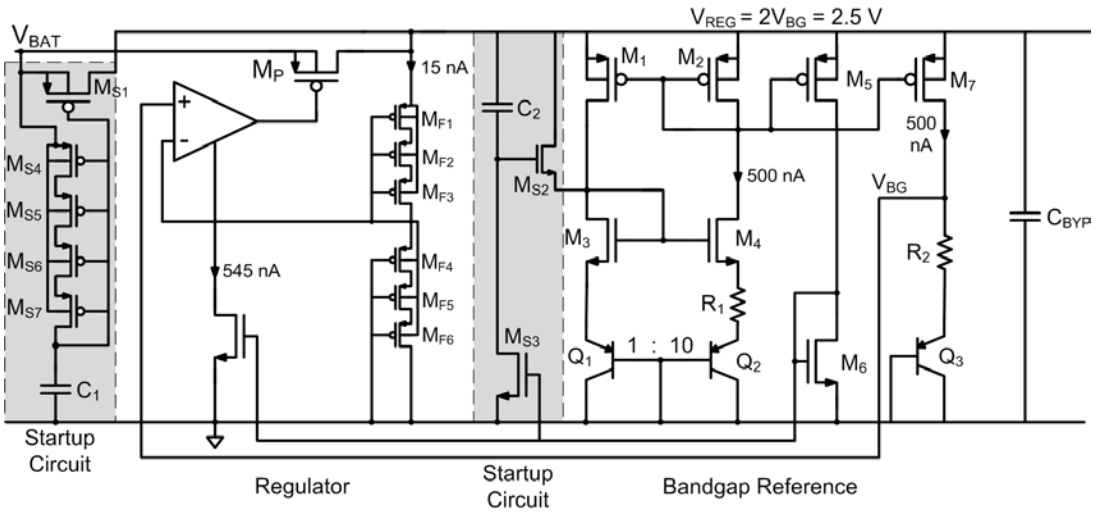


Figure 3-3. Schematic of low dropout regulator with bandgap reference derived from regulated supply. Startup circuits guarantee proper startup into the stable operating mode in which $V_{REG} = 2V_{BG}$.

TABLE 3-1. CIRCUIT PARAMETERS FOR FIGURE 3-3.

Device	Size	Inversion Coefficient
$M_{1,2,5,7}$	5.4 µm / 9 µm	10
$M_{3,4}$	7.2 µm / 1.8 µm	0.5
M_6	3.6 µm / 3.6 µm	2.1
$M_{F1\text{-}F6}$	2.7 µm / 90 µm	6.5
M_P	2.16 mm / 0.6 µm	3.5 (I_D=1 mA)
$Q_{1,3}$	16 μm^2	-
Q_{10}	10 x 16 μm^2	-
R_1	110 kΩ	-
R_2	1.2 MΩ	-

The regulator topology deviates from the traditional low-drop-out configuration by sourcing its bandgap reference from the regulated supply, V_{REG}, rather than the unregulated input voltage, V_{BAT}. This configuration provides excellent voltage regulation because the bandgap supply sensitivity is reduced by the loop gain of the regulator, but proper startup and overall stabil-

ity is more difficult to achieve. A voltage divider formed by matched, very long composite transistors M_{F1-F6} provides a feedback factor of ½ to the error amplifier; the resulting output voltage of the regulator is twice V_{BG}.

The pass transistor M_P supplies current to the entire IC, and in the low-dropout topology, it is configured as a common-source amplifier with the IC as an output load. As the IC load current changes, the transconductance of M_P varies, and this makes compensation of the voltage regulator difficult. A large external output capacitor C_{BYP} is used to provide a dominant pole regardless of the g_m variation. The capacitor also tends to smooth out supply voltage ripple caused when the PMU turns on/off individual circuits. The size of M_P was chosen to support a maximum regulator current of 1 mA. At this level of current draw, V_{BAT} must be at least 185 mV greater than VDD to maintain regulation.

Proper startup of the bandgap reference and regulator feed-back loop is essential for this topology, which has two undesirable operating points, including a zero-current everywhere solution and a second mode in which FETs M_{1-7} are in triode, Q_3 carries a very low current, and the voltage V_{BG} is determined by the equivalent resistance of M_7 and R_2. The AC-coupled startup networks ensure that current will flow and that the FETs will enter saturation, provided that the input supply V_{BAT} has a minimum ramp-up rate greater than 100 V/s. After the circuit begins operation the startup circuits do not draw any DC current and are effectively ignored.

3.2.3 *Low-Power 100-kHz Clock Oscillator*

The clock source for the PMU state machine is a low-power, current-limited relaxation oscillator, shown in Figure 3-4 with device parameters listed in Table 3-2.

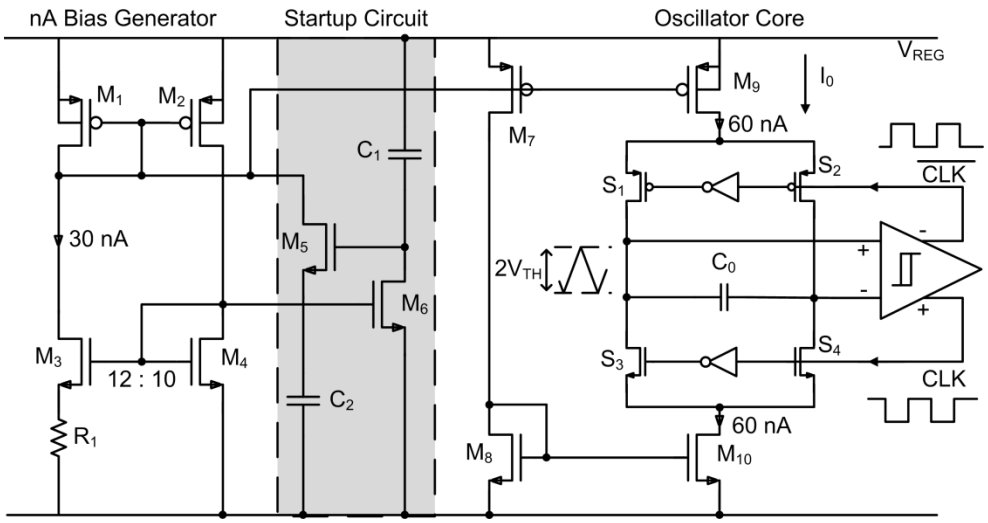


Figure 3-4. Low-power, 100-kHz clock oscillator schematic, including nA current reference and startup circuit.

TABLE 3-2. CIRCUIT PARAMETERS FOR FIGURE 3-4.

Device	Parameter	Inversion Coefficient
$M_{1,2,7}$	4.2 µm / 6 µm	0.6
M_3	12 x 6 µm / 15 µm	.025
M_4	10 x 6 µm / 15 µm	.033
R_1	160 kΩ	-
M_9	2 x 4.2 µm / 6 µm	0.6
M8	2.1 µm / 9 µm	0.6
M10	2 x 2.1 µm / 9 µm	0.6
S1-4	1.8 µm / 1.5 µm	-
C_0	3.5 pF	-
V_{TH}	175 mV	-

The oscillator symmetrically charges capacitor C_0 at a fixed rate of I_0 through an H-bridge switch configuration. When the differential voltage across C_0 exceeds the comparator hysteresis threshold V_{TH} [52], the capacitor polarity is flipped. The circuit produces a triangle wave of amplitude V_{TH} across C_0 and a corresponding binary clock waveform at the comparator outputs. The

oscillation period is given by $C_0 V_{TH}/I_0 + 2T_D$, where T_D is the total loop delay from the oscillator output through C_0. An oscillation frequency of 100 kHz was designed with C_0 = 3.5 pF, V_{TH} = 175 mV, and I_0 = 60 nA.

The charging current I_0 is generated by the bias generator of Fig. 3 [53] which was designed using an inversion-coefficient methodology to ensure reasonable current matching. Matched devices $M_{1\text{-}2}$, $M_{7\text{-}9}$, and $M_{8\text{-}10}$ are biased in moderate inversion to promote even copying of currents. Transistors M_3 and M_4 are biased deep into weak inversion with *IC* = 0.03 and as such their drain current is well described by the EKV model. The current mirror of $M_{1\text{-}2}$ requires the branch currents to be equal, and by equating currents the reference current can be calculated by

$$I_B = {}^{U_T \ln S}/_{R_1}\,, \tag{1.5}$$

where U_T is the thermal voltage and S is the size ratio between transistors M_3 and M_4. With chosen values of R_1 = 160 kΩ and K = ${}^{12}/_{10}$, I_B was designed as 30 nA. The current reference is temperature sensitive, with sensitivity determined by the temperature coefficient mismatch between the poly resistor R_1 and the thermal voltage, but in the implanted environment temperature should remain fairly constant so this is not a concern.

The common-mode voltage of C_0 is determined by the ratio of small-signal output resistances of M_9 and M_{10}; mismatches lead to a common-mode offset which is rejected by the comparator. Since NMOS devices have lower r_0 and increased junction leakage, the comparator uses a PMOS input pair which can tolerate input common-mode levels including 0V. Static differential-mode offsets caused by non-equal charge injection and comparator differential pair

offset can change the clock duty cycle from the nominal 50%. Dynamic differential-mode offsets such as the comparator input-referred thermal and 1/f noise and the uncorrelated channel noise between M_9 and M_{10} are the primary sources of oscillator jitter.

3.2.4 *Power Management State Machine*

The PMU state machine controls power consumption through low-duty-cycle operation of analog circuits. This is possible because of the huge speed difference between instrumentation circuitry and the required 100-Hz sampling rate for bladder pressure. The proposed PMU state machine applies power activation to individual circuits, creating a sample pipe-line in which sensed information is passed between sequential stages as charge stored on switched capacitors. Stages are switched off after settling the next sample/hold capacitor to minimize the active time for each stage and to reduce IC peak current. The PMU state machine timing diagram illustrated in Figure 3-5 corresponds to the power gating signals of Figure 3-1.

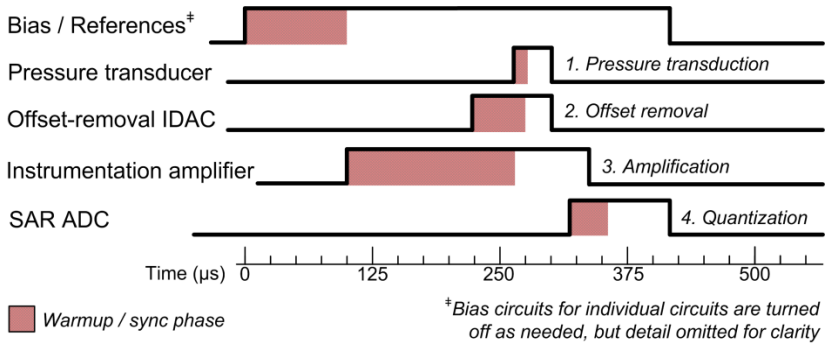


Figure 3-5. Timing diagram of PMU signals used during sample acquisition (transmission occurs in the next 450 µs). Circuits are sequentially activated to minimize active time per stage. This figure was modified from that presented in [51].

Fast-settling elements, such as the piezoresistive pressure transducer and IDAC, have lower duty factors than switched-capacitor and bias circuits, which have longer warmup, step response, and settling limitations. To reduce peak current draw and RF interference, The FSK

transmitter is separately activated for 450 µs after each sample period as determined by the adaptive transmission activity detector described in Section 4.3.

The overall sample rate of the pressure sensing system is 100 Hz, and the PMU state machine only requires 425 µs to acquire a sample. The time-averaged current for each instrumentation circuit is limited by duty factor of 1.4 to 6.5 percent per circuit. The average current for the pressure sensor IC is dominated by the transmission rate, as shown in Figure 3-6. The PMU and piezoresistive pressure transducer together account for at least 21% of the current usage and dominate system power when the transmission rate is less than 25 Hz.

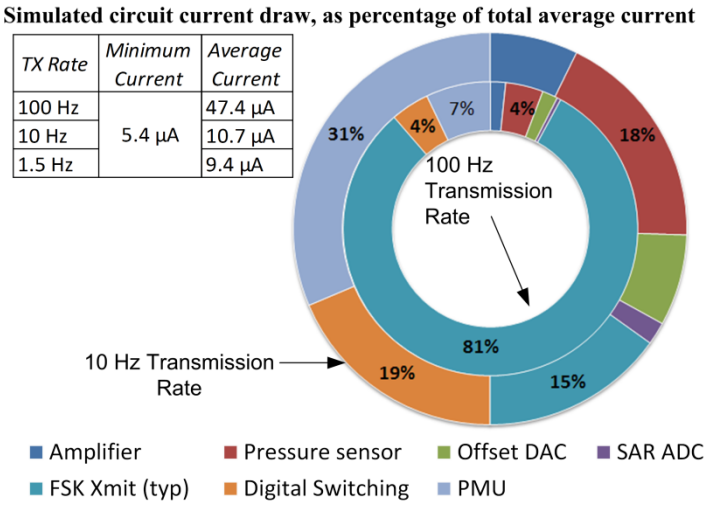


Figure 3-6. Chart showing current used by pressure sensor circuits as percentage of total IC current.

3.2.5 *PMU state machine Digital Implementation*

The PMU was designed using Verilog 2001 HDL code, RTL synthesis, and automatic place-and-route software. The PMU essentially consists of a large counter register plus state decoding logic. All of the PMU states are derived from lower counter bits; the upper bits are used to provide other clock sources for automatic offset updating and the standby command

receiver. Other taps from the clock divider are used to time switched-capacitor circuits on the IC. The counter never ceases operation, and the PMU digital circuits are likely the largest consumers of digital power on the WIMM ASIC. A summary of gates for the synthesized circuit is listed in Table 3-3 while the HDL code for this module is copied in Appendix 11.4.

TABLE 3-3. SUMMARY OF SYNTHESIZED GATES FOR THE PMU MODULE.

Gate Type	Instances	Area %
Sequential	40	40.4
Inverter	32	5.4
Buffer	2	0.5
Combinational	135	53.7

3.3 RF Battery Recharger

The wireless RF recharge circuits use an inductive coil antenna to pick up energy from an externally-applied magnetic field and convert it into a regulated charging current for the implant battery. An equivalent schematic for the RF recharge system is shown in Figure 3-7, and it consists of an external RF power transmitter which couples energy to a resonant LC circuit on the implant. A voltage doubler rectifier with output filter capacitor converts the received energy to a fairly smooth DC voltage, RFV_{DD}. A current reference operating from RFV_{DD} recharges the battery at a constant, 100-µA rate, as long as the rectified voltage is at least as great as the battery voltage. To protect the electronics, a voltage limiter shunts excess current from RFV_{DD} if the rectified voltage exceeds 4.5 V. Finally, to prevent battery over-charge, a comparator determines if the battery voltage is greater than 3.4 V; charging is prevented if the cell voltage is too great [54].

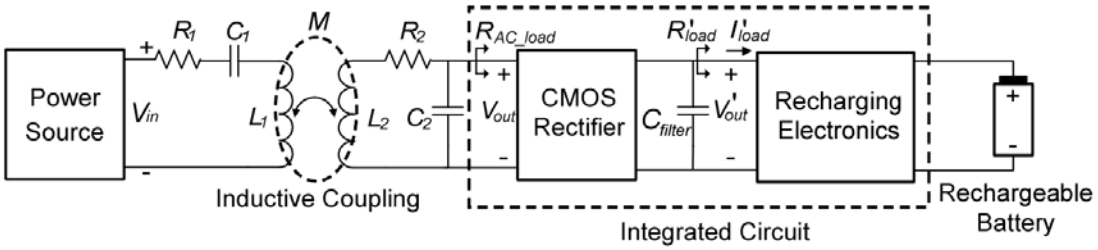


Figure 3-7. Simplified schematic of RF recharging system including coupling model between internal/external coils (from [55]).

The RF recharge circuitry was originally designed in a 1.5-µm process by fellow researchers Peng Cong and Michael Suster, with details reported in [55] and [49]. The circuit layout was migrated to the 0.5-µm process WIMM ASIC by shrinking contact vias to maintain DRC checks, but geometry was not scaled. Large, passive elements such as resistors were replaced by smaller structures to leverage the high-resistance implant options of the 0.5-µm process, and various other layout optimizations were added to improve the circuit performance.

The operating frequency was chosen to maximize the voltage gain of the wireless recharging system, given by

$$\frac{V_{OUT}}{V_{IN}} = \frac{\omega^2 L_2 M}{R_1 R_2 + (\omega M)^2 + \frac{R_1 \omega^2 {L_2}^2}{R_{LOAD}}}. \qquad (1.6)$$

The coil parameters were chosen based on overall system size constraints and are listed in Table 3-4. Assuming quality factors greater than 200 for both coils, an operating frequency of 3 MHz was chosen. With a worst-case coupling factor, *k*, of $2\text{x}10^{-4}$ (at a coil separation distance of 20 cm), the expected system power transfer efficiency is $7.5\text{x}10^{-3}$ %. At this efficiency, the external coil must dissipate about 10 W of power to accomplish wireless battery recharge.

TABLE 3-4.CHOSEN AND MEASURED PARAMETERS FOR THE RF RECHARGING SYSTEM.

Parameter	Name	Design Value
ω	Operating frequency	3 MHz
L_1	External coil inductance	5 µH
L_2	Internal coil inductance	11 µH
k	Coupling coefficient	$2x10^{-4}$
R_{LOAD}	Rectifier load impedance	7.5 kΩ

3.4 Wireless Standby Command

To preserve the battery charge when the WIMM system is not being used (during sterilization, implantation, etc.), the ASIC can be placed into a very low power, standby mode. In standby, power to the analog portions of the ASIC is disabled, while the digital circuits remain powered, but unclocked. This allows the ASIC to remain in standby once the standby control flip flop is set. The standby command is transmitted as 20% AM modulation on top of the battery recharge field, and a time-based command decoder verifies that the command signal timing is correct before entering standby. The ASIC exits standby after the wireless recharge field is again turned on for a minimum period of time.

The AM demodulation circuit and command decoder is illustrated in Figure 3-8. The RF input is taken from the wireless recharging coil, and the 3 MHz carrier is filtered out by $R_{1,2}$ and C_2. The resistors limit the loading of the recharge coil and also divide the signal by a factor of 3 to protect the CMOS logic circuits, and M_1 and M_2 function as clamps to limit V_X to about -0.5 – 5.0 V. During typical battery recharge, V_X is equal to 1.7 V with a 3-MHz ripple of about 70 mV. Schmitt trigger inverters are used to convert the voltage at V_X to a binary signal which drives a T-flip-flop. When the RF recharge signal drops suddenly, i.e. during AM modulation, the output

state of the T-flip-flop toggles. The command decoder interprets the digital signal to determine if a true standby command was sent.

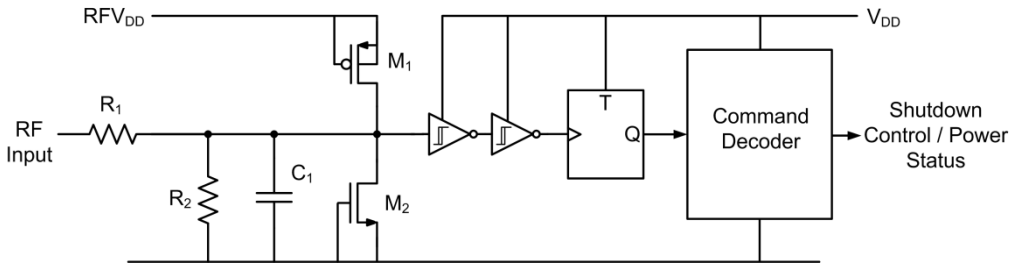


Figure 3-8. Simplified schematic of the RF recharge AM demodulator and command decoder.

The command decoder was synthesized from behavioral Verilog 2001 HDL. Because the standby command is used infrequently, the decoder timing was designed to be robust and convoluted to prevent accidental ASIC shutdown. The command decoder only places the ASIC into standby mode when a command matches both a time- and value-based check, as described in Figure 3-9. The decoder must receive exactly 3 negative edges followed by at least 10 ms of no activity, and this pattern must be repeated for 6 successive 40-ms periods, followed by a final, positive-going edge to enable the shutdown output.

If the decoder input pattern fails the checking process, the decoder is “locked” for 20 ms and ignores further modulation attempts. In standby mode the command decoder clock source is disabled, so the circuit is entirely edge-triggered. The ASIC can be activated out of standby by toggling the RF input modulation, then holding the level high for at least 3s. The HDL code used to synthesize the command decoder is provided in Appendix 11.3. A summary of synthesized gates is listed in Table 3-5.

TABLE 3-5. SUMMARY OF SYNTHESIZED GATES FOR THE STANDBY COMMAND DECODER.

Gate Type	Instances	Area %
Sequential	14	44.7
Inverter	10	5.3
Combinational	42	50

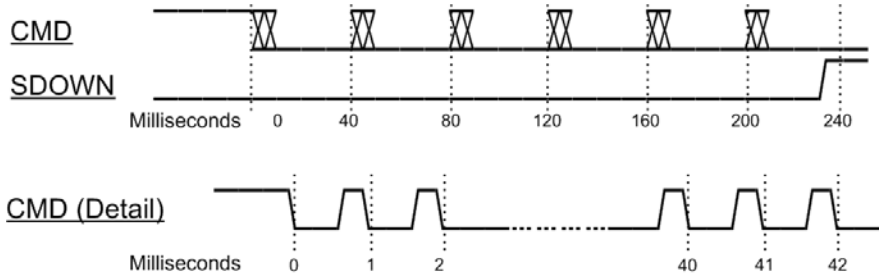


Figure 3-9. Timing diagram for the command decoder that puts the ASIC in standby.

Power control for the WIMM ASIC during standby mode is depicted in Figure 3-10. The PWREN signal is produced by the command decoder, and when PWREN is high, the system operates normally, with AV_{DD} (which is produced by the regulator) coupled to analog and digital supply lines. When PWREN first goes low, the digital supply is momentarily shorted to the battery voltage before being disconnected from the regulator. This is to ensure that the digital circuits remain powered throughout the supply changeover, or else the latched shutdown command could be lost. The pass transistors were sized equally to that of the regulator to ensure they can carry the ASIC peak current.

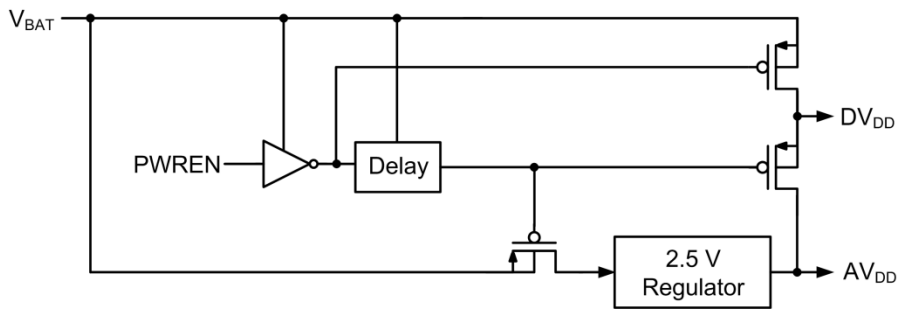


Figure 3-10. Schematic showing how the standby power switch is controlled by command decoder output, PWREN.

3.5 Pressure Sensor Selection

The properties of the WIMM ASIC had to be designed to match a specific pressure sensor, or at least the range of common commercial examples. Varying sensor electrical parameters such as sensitivity, bridge resistance, and offset voltage were considered. To reduce the number of analyzed sensors, only piezoresistive sensors which used back-side media access ports were considered. Finally, only pressure sensors which could be obtained from commercial sources in die form were analyzed, as other large-volume or research prototype sensors were difficult to procure. A summary of some commonly-available commercial pressure sensor dice meeting the basic criteria is shown in Table 3-6.

TABLE 3-6. SUMMARY OF BARE-DIE, BACKSIDE-ACCESS COMMERCIAL PRESSURE SENSORS.

Sensor	Bridge Resistance (kΩ)	Total Atmospheric + Manufacturing Offset (mV/V)	Average Sensitivity (mV/V/bar)	Dimensions (mm)
Silicon Microstructures SM5112 [56]	4.0 – 6.0	15 - 35	25	2.0 x 2.0 x 1.4
Sensonor SW415 [57]	12.0	7.7 - 20	12.8	2.5 x 2.0 x 1.4
EPCOS C29 [50]	2.1 – 3.3	4 - 23	17	2.7 x 2.2 x 1.6
Merit Sensor H1C-1000-L2 [58]	4.0 – 6.0	5 - 25	15	2.1 x 2.1 x 1.4

The pressure sensor size, full-scale range, and burst pressure parameters were not considered to be important, as all of the commercial MEMS sensors are quite small, and have burst pressures well above the physiological range. To minimize power consumption, the ideal pressure sensor for the WIMM would have high bridge resistance, high sensitivity, and low offset voltage. There is a tradeoff, however, because a pressure sensor with lower resistance can settle faster, and could be switched at a lower duty cycle by the PMU. Based on commonality of parameters, the WIMM ASIC was designed to work with a pressure sensor having a bridge resistance of 4 kΩ and a sensitivity of about 15 mV/V/bar. Early prototypes of the implantable microsystem used the Silicon Microstructures SM5112. However, due to sourcing difficulties for other sensors, the Sensonor SW415 was eventually adopted, even though it is a poor match to the ASIC designed parameters.

3.6 Hybrid Continuous-Time / Switched-Capacitor Instrumentation Amplifier

The output of the pressure sensor is amplified by an instrumentation amplifier (INA) which was designed to have low noise and offset and precisely-defined, programmable gain. A schematic of the pressure sensor and instrumentation amplifier is shown in Figure 3-11. The pressure sensor draws significant power while active, so the INA was designed to minimize its active time. To reduce the RC settling time of the pressure sensor, the hybrid INA uses a continuous-time, fully-differential preamplifier with low input capacitance. Low offset and 1/f noise is achieved by chopping of both the preamplifier and 2nd-stage amplifier, which uses a correlated-double-sampling (CDS) architecture with a single-ended output to drive the ADC.

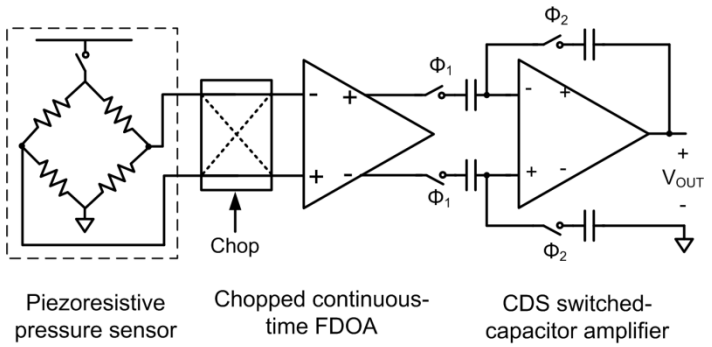


Figure 3-11. Schematic of the 2-stage INA consisting of a continuous-time preamplifier and a switched capacitor 2nd stage.

The INA was designed assuming an ADC full-scale range of 1.4 V and a sensor maximum output voltage of 10 mV at 200 cm H_2O. The 2nd-stage INA has programmable gain from 150 – 260 V/V, and for the purposes of analysis the maximum gain was assumed. With the full-scale assumptions, the sensor output would exceed the ADC range at maximum INA gain; however it is expected that packaging- or implantation-related attenuation would reduce the maximum sensor output.

3.6.1 *Continuous-Time, Fixed-Gain Preamplifier*

The INA preamplifier design constraints were driven by input capacitance, settling time and input-referred noise limits. A schematic of the preamplifier is shown in Figure 3-12, and this simple topology uses an all-NMOS amplifier core with PMOS biasing elements. The gain is defined as the transconductance ratio of the input pair to its active loads, or

$$A_{V,preamp} = \frac{g_{m1,2}}{g_{m3,4}+g_{mbs3,4}}, \quad (1.7)$$

where g_{mbs} is the bulk-source transconductance of $M_{3,4}$. The g_{mbs} of $M_{1,2}$ is neglected because the source voltage is a small-signal ground and the bulks are tied to the substrate ground. With

careful layout and matching, the transconductance ratio, and hence the gain, is a very stable parameter over temperature and time. PMOS current sources $M_{6\text{-}7}$ are configured to "steal" bias current from the active loads thereby reducing $g_{m3,4}$ and increasing the gain.

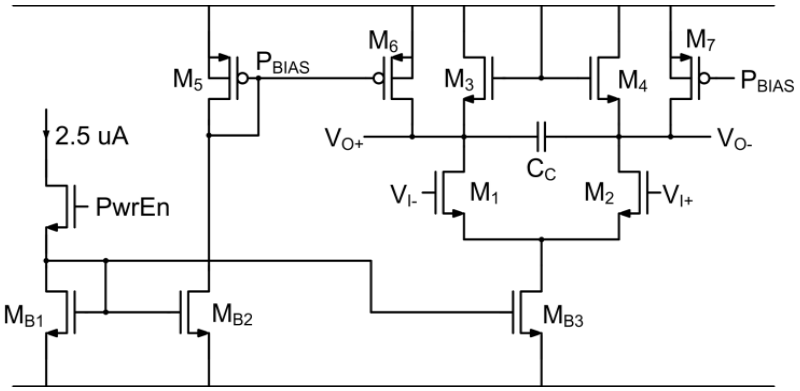


Figure 3-12. Schematic of the INA preamplifier.

TABLE 3-7. DEVICE SIZES FOR THE INA PREAMPLIFIER.

Device	*Value*	*Bias Current*	*Inversion Coefficient*
$M_{1,2}$	1.575 mm / 2.7 µm	2.5 µA	0.02
$M_{3,4}$	3 µm / 6 µm	625 nA	5.5
$M_{6,7}$	18 µm / 3 µm	1.875 µA	4.0
M_{B3}	24 µm / 3 µm	5.0 µA	2.8
C_C	10 pF	-	-

The single-stage amplifier is inherently a wideband design, so capacitor CC was added to reduce the bandwidth as low as possible while still satisfying the GBW limit as described above. Assuming a differential loading of 8 pF from the 2nd stage switched-capacitor amplifier, the pre-amplifier has a -3dB bandwidth of 40 kHz. With the values of Table 3-7 and assuming a noise bandwidth of 60-kHz, the preamplifier has an input-referred noise of 5.4 µVrms, as analyzed in Appendix 11.2.1. Because the preamplifier is chopped, its gain and output-referred noise is dou-

bled. Including the chopping, the preamplifier has an effective gain of 13 and an output-referred noise of 70 μVrms.

3.6.2 *Switched-capacitor, programmable-gain 2nd-stage amplifier*

The 2nd stage of the instrumentation amplifier is implemented by a well-known switched-capacitor (SC) amplifier [59] which uses correlated double sampling (CDS). Power to the amplifier is periodically turned off to save power, so 1/f noise is reduced [60] and the CDS topology further limits the amplifier offset due to charge injection and input pair mismatch. The amplifier is implemented as a folded-cascode single-stage amplifier.

To first order, the transconductance of the amplifier in a SC circuit does not contribute to the thermal noise because the transconductance effect on thermal noise floor and circuit bandwidth cancels [61]. Moreover, folded-cascode amplifiers typically have very high open loop gain due to high output impedance, so the main design criteria were output voltage swing and settling time. To maintain high output impedance and low offset, cascode and current mirrors were designed in moderate to strong inversion, and a V_{GS}-V_T replica circuit was used to generate a low-voltage cascode level [62]. The input pair transconductance was designed to provide 8-bit settling as described by Equations (1.18) and (1.19).

The schematic of the SC amplifier is shown in Figure 3-13. The settling time limitation is driven by the ADC sampling requirement when the system runs at its maximum possible rate of $F_s = {f_{CLK}}/{9}$ in which the ADC samples the input voltage for only one clock period (10 μs). This operation mode is typically only used when the system leaves standby and calibrates the initial pressure sensor offset. At the end of ϕ_2 and when ϕ_S is also high, the worst-case settling time

occurs when the amplifier drives C_{ADC}, C_3 and the feedback capacitors. Under this condition the amplifier g_{mi} of 55 µS was designed to achieve a 1.8-MHz GBW.

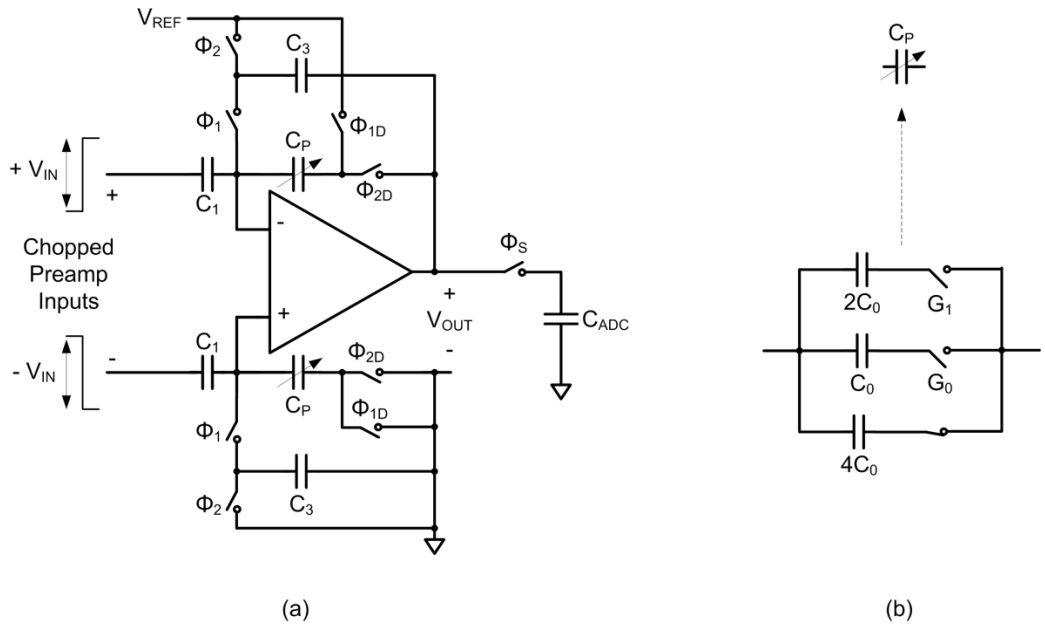


Figure 3-13. Schematic of the switched-capacitor second-stage amplifier in (a) with the programmable resistor CP depicted in (b). Gain controls $G_{0\text{-}1}$ determine the total gain from 11.4 to 20.

Because the preamplifier is chopped, the 2nd-stage SC amplifier does not require input sampling switches. The preamplifier is chopped by the same ϕ_1/ ϕ_2 clock scheme in order to transfer a differential input charge of $2V_{IN}C_1$ to the SC amplifier. The amplifier has programmable gain through the network denoted as C_P. The unit capacitance C_0 was chosen as 100 fF to satisfy noise requirements as detailed in Appendix 11.2.2. Including the preamplifier gain of 6.5 and a chopper gain of 2, the total INA gain range is 150 - 260 V/V. The resulting 2nd-stage input-referred thermal noise is 59.3 µVrms yielding a total INA input-referred noise of 7.06 µVrms. This level exceeds the ADC quantization noise slightly at the maximum gain setting, but other amplifier gain settings meet the quantization noise requirement.

3.6.2.1 Switched capacitor amplifier warm-up phase

The chosen switched-capacitor architecture does not use a reset phase to charge the common-mode level of the input capacitor summing nodes. During normal operation, the common-mode level of the summing nodes eventually stabilizes to that of V_{in}. However, because the amplifier is periodically turned off to save power, the common-mode voltage drifts. To ensure proper operation, the amplifier is turned on for a period before a sample is acquired, and the inputs are connected to V_{ref}. The amplifier is cycled through phases $\phi_{1,2}$ six times before the pre-amplifier inputs are connected and normal operation continues, as shown in Figure 3-14.

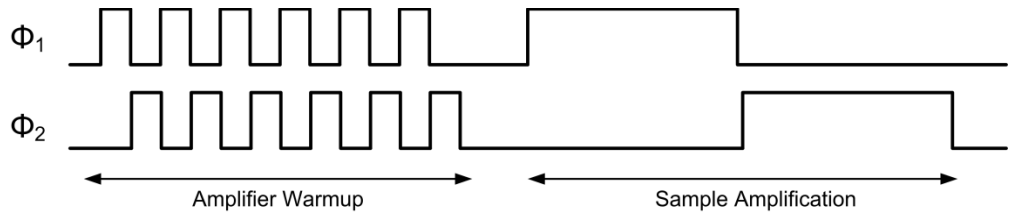


Figure 3-14. Timing diagram showing the INA 2nd-stage timing during warmup and amplification phases.

CHAPTER 4

ASIC DATA CONVERSION, SIGNAL PROCESSING, AND WIRELESS COMMUNICATIONS

4.1 8-bit Successive-Approximation Analog-to-Digital Converter

Successive-approximation analog-to-digital converters (SAR ADCs) convert an analog input to a digital code through a binary search algorithm. This ADC architecture is well-suited for low-power applications since it requires a small number of analog circuits, and runs only slightly above the Nyquist rate, typically producing *N*-bit samples in *N+1* clock cycles.

The basic architecture of a SAR ADC is shown in Figure 4-8 and consists of a sample-and-hold (S/H) circuit, a digital-to-analog converter (DAC), a voltage comparator, and control logic. In the illustrated example, the S/H circuit has been combined with the DAC; this configuration enhances comparator precision because the common-mode input level is set by V_{ref} and not by V_{in}. The ADC full-scale (FS) range is determined by two additional reference voltages, V_{R+} and V_{R-} which correspond to the ADC maximum and minimum input voltages. Furthermore, it is assumed that $V_{ref} = \frac{V_{R+}+V_{R-}}{2}$ to simplify the ADC analysis.

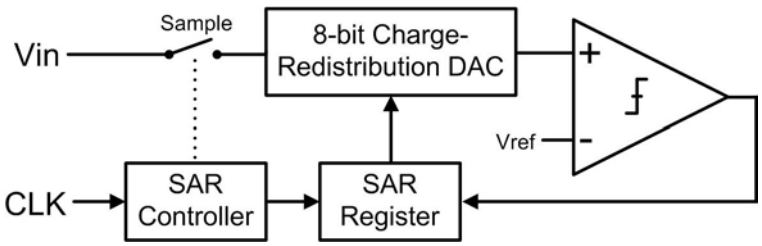


Figure 4-1. Schematic of a basic SAR ADC using combined sample/hold and charge-redistribution DAC.

A schematic of the charge-redistribution DAC and ADC comparator preamp is shown in Figure 4-2. The 8-bit DAC is created by an array of binary-weighted capacitors of base value C_u with total capacitance of $2^N C_u = 256C_u$ for an 8-bit DAC. An additional unit capacitance without switches has been added as a modeling capacitor to simplify analysis of the ADC, but this capacitor was not included in the actual circuit since it is not needed and degrades signal-to-noise ratio. The configuration of the DAC is controlled by the value stored in the SAR, which determines the positions of the bottom plate switches. To minimize charge leakage, the DAC capacitor array top plate, designated as the summing-node V_X, is only connected to a comparator auto-zero reset switch.

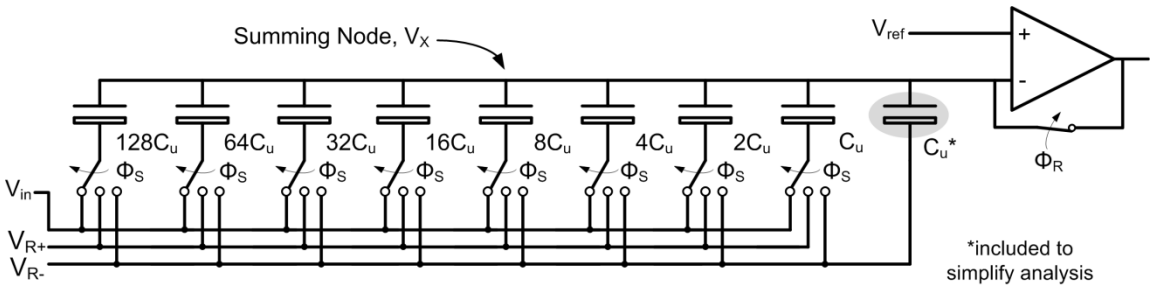


Figure 4-2. Schematic of the SAR ADC capacitive DAC and comparator during sample phase.

The summing node, V_X, is pre-charged to $V_{ref} + V_{os}$ where V_{os} is the input-referred offset plus 1/f noise of the comparator preamplifier. V_{in} is simultaneously sampled on the DAC capacitor bottom plates. Then, beginning with the MSB, N clock cycles are used to find a DAC code such that $V_X \cong V_{ref}$, i.e. the virtual voltage $V_{DAC} \cong V_{in}$, where $V_{DAC} = V_{R-} + V_{FS} \cdot \sum_{i=1}^{N} b_i 2^{-i}$

and each b_i is 0 or 1. In other words, the MSB has a place value of ½, the next bit has a place value of ¼, etc. Details of this switching sequence are provided in the remainder of this section.

After the S/H phase ends, the capacitor switch arrangement is updated as shown in Figure 4-3 and the ADC conversion phase begins by determining the correct value of the conversion MSB, or bit number 7. At the end of the conversion cycle the comparator value is latched in the SAR, storing a "0" for the MSB of the result, if $V_{in} < \frac{V_{FS}}{2} + V_{R-}$.

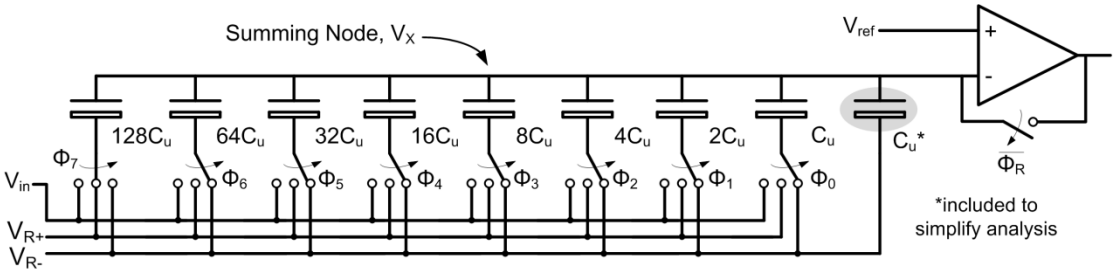


Figure 4-3. Schematic showing the SAR ADC capacitive DAC and comparator during first (MSB) bit test cycle.

As shown in Figure 4-4, the ADC repeats a similar pattern for converting the remaining bits of the result. The switches corresponding to each bit that has already been tested are set to V_{R+}/V_{R-} corresponding to a 1/0 value for that bit. The switches for bits not yet determined are held at V_R-. The bit being tested (bit number *n*) is temporarily set to "1" coupling a voltage proportional to $V_{FS} \cdot 2^{-(N-n)}$ to the summing node. Once all switches are updated and the system has settled, the comparator is strobed to produce a decision for the value of the bit being tested, and the result is stored in the SAR.

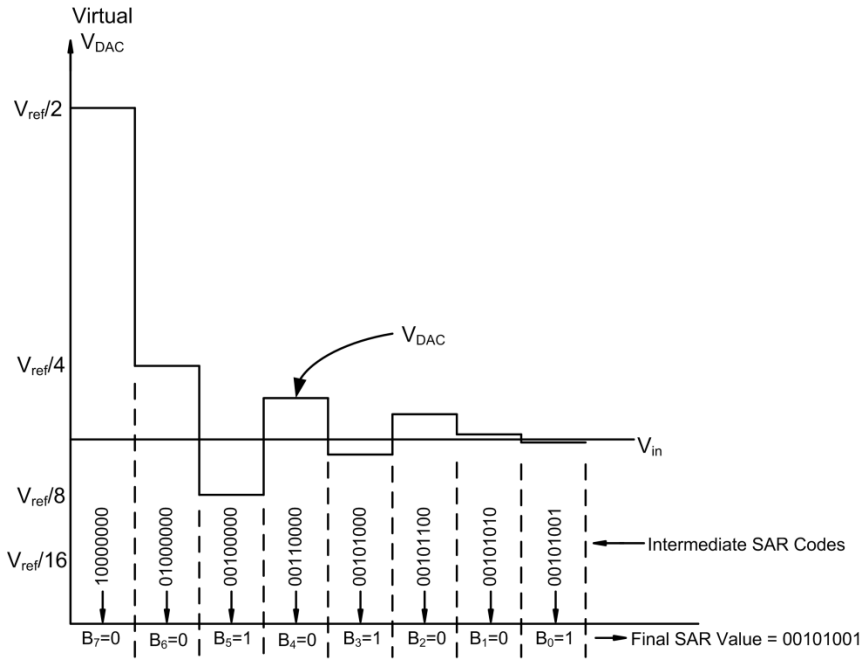


Figure 4-4. Example waveform showing V_{DAC} during the SAR quantization cycle.

4.1.1 *SAR ADC Clock Phase Timing*

The SAR ADC is controlled by a state machine which generates clock phases for the sample and bit test phases as shown in Figure 4-5a. The comparator auto-zero and strobe (re-generation) clocks are derived from the other phases. The state machine starts in the sample phase ϕ_S and progresses linearly through each bit test phase, $\phi_{7\text{-}0}$. After 9 clock cycles the ADC conversion is complete, and the ADC halts operation until the controller is reset.

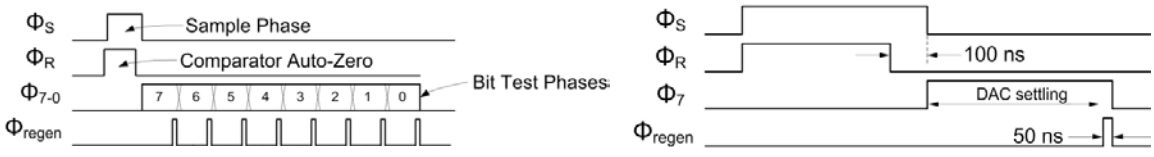


Figure 4-5. Timing diagram showing (a) SAR ADC clock phases; and (b) detailed timing of the comparator auto-zero and regeneration clock signals.

A detailed timing diagram for the sample phase is shown in Figure 4-5b. The comparator auto-zero phase ends 100 ns before the input voltage sample switch is opened; this is to allow

dissipation of any “kick-back” charge released when the preamplifier switches into its open-loop state. The comparator strobe signal ϕ_{regen} is derived from the main ADC clock and the state machine outputs, and forces a comparator decision when it goes high. The timing for ϕ_{regen} was chosen to allow for maximal DAC settling time after a bit test begins, while still permitting sufficient time for the comparator to latch before the next bit test cycle starts.

To avoid charge loss errors due to transient switching currents, the ADC uses a break-before-make (non-overlapping clocks) switch structure. This technique also reduces power consumption by preventing shoot-through conduction losses from V_{in} to $V_{R+,-}$ and directly between $V_{R+,-}$. For each state transition in which switch configurations change, all closed switches open before new switches close. This ensures that the switched-capacitor nodes always transition to a new state from a high-impedance state, thus preserving the stored charge. A chain of 8 long inverters is used to generate a non-overlap delay of about 20 ns.

4.1.2 *Charge-Redistribution DAC design*

The accuracy of the SAR converter is limited by noise and charge injection. The DAC unit capacitor was sized to satisfy noise and offset errors as described in Appendix 11.2.3. A unit capacitor size of Cu=15 fF was chosen to limit noise and offset errors below the quantization noise floor for an 8-bit ADC. The resulting total DAC capacitance is 3.8 pF, which is low enough to attain low dynamic power consumption and good settling time without an ADC buffer driver. Including parasitic capacitance effects, the ADC systematic offset is 13 mV and the anticipated gain error is 10%. The ADC offset can be addressed by the pressure-sensing system automatic offset cancellation, and the gain error should not change over time and be well matched between different chips.

4.1.3 *SAR ADC Comparator Design*

The SAR ADC comparator was designed for low continuous current draw while still being capable of medium-speed operation. The design constraints for the comparator were driven by power consumption, settling time requirements during auto-zero and bit testing cycles, and thermal noise limits. The basic comparator schematic is shown in Figure 4-6, and it consists of a preamplifier followed by two regenerative latches. The preamplifier is used to amplify the differential input voltage beyond the offset of the regenerative latch stages, and its design details are discussed in Appendix 11.2.4. The topology is pseudo-differential, to enable a single-ended VDAC input, so switch S_R is used during the ADC sample phase to auto-zero the preamplifier offset voltage, as described in Appendix 11.2.5. Finally, the regenerative latches are periodically strobed to force a binary decision based on the preamplifier output polarity.

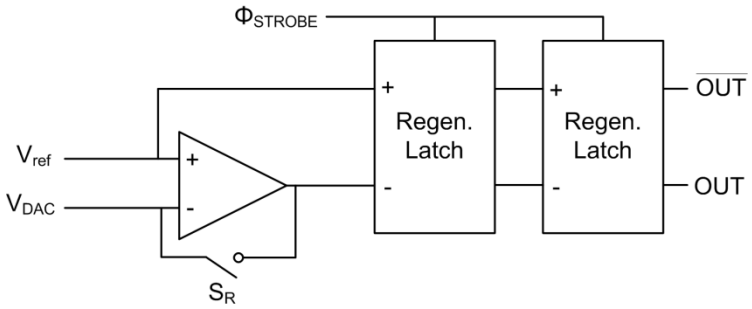


Figure 4-6. Block diagram of the comparator used in the SAR ADC.

The binary comparison action of the comparator is performed by cascaded regenerative latches. The function of the regenerative latches is to form an instantaneous binary decision about whether V_{IN} is greater or less than V_{REF}. The conceptual schematic for the regenerative latch is shown in Figure 4-7a, and the circuit uses positive feedback to generate very high open-loop gain and switching times. Once the latches have made a decision they must be reset before

making a new comparison. This technique, known as “strobing” uses a strobe clock, ϕ_S, to force periodic comparator decisions.

When ϕ_{regen} is low in Figure 4-7a, both complementary latch outputs are held high and the latch positive feedback loop is broken. The differential inputs Vi+ and Vi- control transconductors Gm+ and Gm-, respectively. When ϕ_{regen} goes high, the positive feedback loop is enabled, and the circuit moves towards one of two stable equilibrium points where the complementary latch outputs are not equal. The speed with which each NAND gate can pull its output down is determined by the differential input voltage through transconductors Gm+/-, and thus the latch determines if $V_{i+} > V_{i-}$ every time ϕ_{regen} goes high.

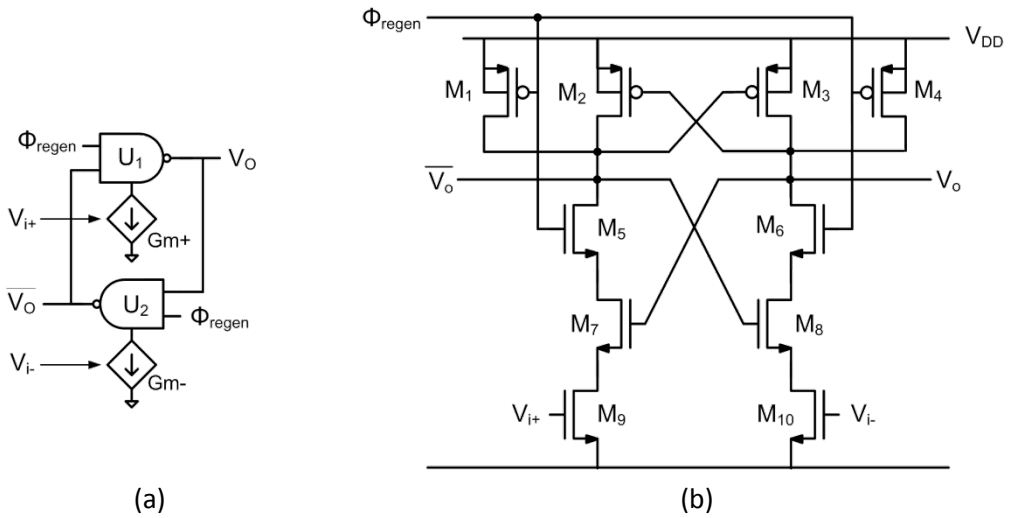


Figure 4-7. The conceptual schematic for (a) the comparator regenerative latch in which the input transistors are modeled as ideal transconductors; and (b), the full schematic in which the input pair is formed by matched NMOS FETs.

The transistor-level schematic of Figure 4-7b shows the latch implementation. Transistors $M_{1,4}$ and $M_{5,6}$ are used to pull the complementary VO outputs high when ϕ_{regen} is low. Once ϕ_{regen} goes high, the input voltages on transconductors $M_{9,10}$ determine which way the loop will equalize. Transistors $M_{7,8}$ are initially turned on since the V_O outputs are pre-charged to V_{DD}, causing the complementary V_O outputs to swing towards ground. The rate at which $M_{7,8}$ can pull

the outputs low is determined by the gate voltages of M_9 and M_{10}. The regenerative action of the latch is triggered when one of the latch output nodes reaches $V_{DD} - V_{TP}$, turning on either $M_{2\ or}\ M_3$. After the positive feedback loop is triggered, the latch rapidly switches to its final state based on which output reached the critical voltage first.

All transistor sizes are kept at the process minimum to enhance switching speed and to reduce the preamplifier output loading capacitance. The latch is not biased with quiescent current or feedback, so the input-referred offset will be fairly large. However, once referred to the preamplifier input by the preamp gain, the tolerable latch offset voltage is 400 mV to maintain $V_{offset,i} < V_{LSB}/2$. This level of offset is easily attainable through careful layout of $M_{9,10}$.

4.2 Pressure Sensor Offset Drift Cancellation System

Measuring absolute pressure from a submucosal implant location is difficult because lumen bladder pressure is a function of the bladder as well as the abdominal cavity pressure. Abdominal pressure is ever-changing due to atmospheric pressure changes and physiological factors such as posture variations and tissue aging. The static pressure of the bladder is an important parameter to measure, however, so it cannot simply be ignored as in traditional AC-coupled instrumentation architectures. Moreover, because the pressure sensor is frequently turned off to save power, an AC-coupled architecture would not be feasible without introducing additional DC current draw. A differential approach—i.e. using a sham pressure sensor sealed so as to eliminate its pressure response—would potentially eliminate offset effects due to temperature, packaging materials, and manufacturing tolerances (if the reference sensor was fabricated on the same die as the active sensor), but this would not eliminate naturally-occurring offsets

such as those caused due to physiological effects at the implant location, such as tissue scarring or positional shifts of organs within the peritoneal cavity.

To maintain accuracy over a wide dynamic range and to eliminate implant-related offset effects, the WIMM ASIC uses an offset-removal system to reject all DC offsets. A block diagram of the offset removal system is shown in Figure 4-8.

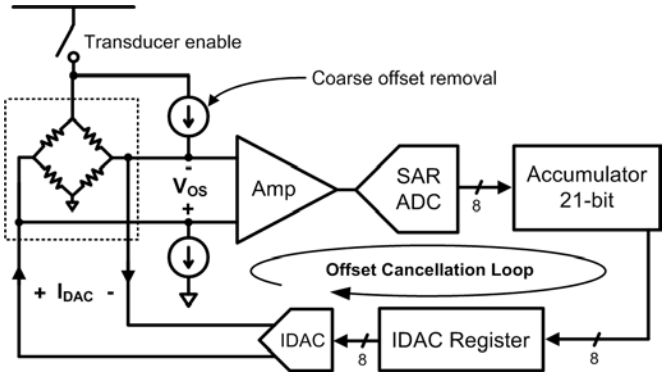


Figure 4-8. Block diagram of the offset cancellation loop on WIMM ASIC.

The offset-cancellation circuitry uses an accumulator to perform a long-term average, with ADC samples added to the accumulator as signed operands. Every 32 samples, the 8 most-significant bits of the accumulator are copied to the IDAC register, which sets the IDAC output current. This procedure is effectively the same as dividing the accumulator value by $2^{(N_A-8)}$, where N_A is the accumulator length. Thus the value copied to the IDAC register represents a running average of the pressure samples. In steady state, the accumulator value varies with AC pressure changes, but the average value remains the same (assuming zero-mean pressure changes) [51].

To prevent saturation of the analog instrumentation, offset cancellation operates continuously while samples are acquired. The cancellation feedback loop maintains an average output of 128, or half of the ADC FS range, at the ADC output. This maximizes the amplifier and ADC

dynamic range, allowing for high resolution measurements of quick pressure changes (the ADC samples) and lower resolution measurements of low-frequency pressure baseline drift (the offset IDAC values). Pressure information is not lost with this technique, since both the ADC samples and the offset values are wirelessly transmitted within the data packets. Since normal filling information is transmitted as offset values, clinicians should be able to separate the average level of bladder pressure (useful to measure bladder fullness, compliance, etc.) while still benefiting from enhanced accuracy of high-frequency events such as bladder contractions.

4.2.1 *Offset Cancellation System Frequency Response*

The analog electronics have a fairly narrow dynamic range of 8 bits and a sudden step change in offset increments the accumulator at a slew rate of ±127 codes per sample. Once the pressure offset falls within the 8-bit range of the electronics, the offset-cancellation system performs linearly with an effective time constant given by

$$\tau_a = \frac{1}{F_I F_S} \cdot \left(\frac{2^{(N_A - N_D - 1)}}{R_{DA}} \right), \tag{1.8}$$

where the parameters of Equation (1.8) and the values used on the WIMM ASIC are contained in Table 4-1.

TABLE 4-1. PARAMETERS OF THE OFFSET CANCELLATION SYSTEM FOR TIME-CONSTANT CALCULATION.

Variable Name	*Description*	*Value on WIMM ASIC*
F_S	ADC sampling frequency (Hz)	100
F_I	IDAC update rate (Hz)	0.20
N_A	Accumulator length (bits)	22
N_D	IDAC resolution (bits)	8
R_{DA}	Average ratio of ADC codes per IDAC code	6 – 9*

*depending on amplifier gain setting

The time constant is a function of the accumulator size (N_A), the IDAC resolution (N_D), scaling term R_{DA}, the ADC sample rate F_S and the IDAC update rate F_I. The factor R_{DA} is a system parameter describing the IDAC LSB "weight" in ADC codes, or how many ADC codes are equal to a 1-bit change in the IDAC output. This factor is essentially the loop gain of the offset cancellation system.

The offset cancellation system has a low-pass frequency response with corner frequency equal to $\frac{1}{2\pi\tau_a}$. However, once this low-pass system is coupled back into the WIMM instrumentation circuitry as negative feedback, the frequency response is flipped, transforming the WIMM instrumentation circuitry into a high-pass system. Thus, the WIMM can amplify AC pressure signals while rejecting DC offset. The values for the offset cancellation system were chosen to produce a long time constant of 68–46 seconds, for a high-pass corner frequency of about 2.3-3.5 mHz, for amplifier gain settings of 150–260 V/V. This time constant was chosen to be long enough such that slow, naturally-occurring pressure changes are captured at full resolution, while rejecting long-term drift which could lead to saturation of the instrumentation circuitry.

4.2.2 *Triggered Offset Cancellation Mode*

The WIMM system can be placed into a low-power standby mode, in which the system clock is halted and power consumption is dropped to the bare minimum. This mode might be used during system sterilization and implantation, for example, so it is likely that the baseline offset will be large when the system first exits standby. To prevent a long delay while the automatic offset loop slews to its linear settling range, the offset removal system can quickly calculate a minimum offset when triggered.

The triggered offset removal begins when the system leaves standby mode. To accelerate the process, the instrumentation system and ADC run at the maximum, non-power-managed rate of 11.1 kilosamples/s and the accumulator lower bits are bypassed. Instead, the upper accumulator bits, which control the offset removal IDAC, are simply incremented from the minimum value, generating an offset ramp at the pressure sensor. The triggered offset removal operation is halted once the ADC output codes fall within a range of 2-8. Once the baseline offset has reached this minimum level the instrumentation circuitry responds linearly, and normal, low-power operation with automatic offset cancellation resumes. An example of this process is shown in Figure 4-9.

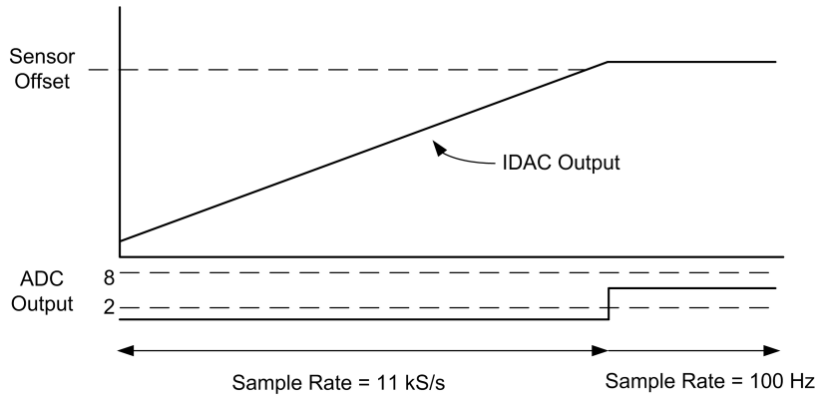


Figure 4-9. Illustration of the simple ramp calibration that is performed when the system leaves standby mode.

4.2.3 *Offset Cancellation Digital Implementation*

The accumulator and accompanying arithmetic was implemented in HDL using Verilog 2001. The accumulator was defined as an unsigned register, and the add/subtract logic was explicitly defined as sign-magnitude. The offset removal system attempts to maintain an average ADC output of 128, so the ADC MSB was used as a sign bit while the other 7 ADC bits are added/subtracted to the accumulator. Any value greater than 128 has a "1" MSB, and the magnitude bits are simply subtracted from the accumulator. The magnitude bits of any ADC sample with a "0" MSB are inverted before adding to the accumulator. The end result of this process is to increment/decrement the accumulator by the distance that the magnitude is from the center value of 128.

To save power, the offset calculation system is only clocked once per sample period. The HDL implementation includes logic for both the automatic and triggered offset cancellation modes. A summary of gates for the synthesized circuit is listed in Table 4-2 while the HDL code for this module is copied in Appendix 11.5.

TABLE 4-2. SUMMARY OF SYNTHESIZED GATES FOR THE OFFSET REMOVAL MODULE.

Gate Type	Instances	Area %
Sequential	34	27.8
Inverter	69	9.4
Buffer	1	0.2
Combinational	228	62.6

4.2.4 *Offset Removal Current-Mode Digital-to-Analog Converter*

Pressure sensor offset is removed by a current output digital-to-analog converter (IDAC) as depicted in Figure 4-10. The IDAC is bipolar so that it does not change the amplifier input common-mode level when changing codes. While the IDAC has 8-bit resolution, coarse offset removal is additionally achieved through fixed current sources. This topology is used because the absolute pressure sensor used in the WIMM will always have a large offset due to atmospheric pressure. After the coarse offset removal, the linear IDAC removes dynamic offset.

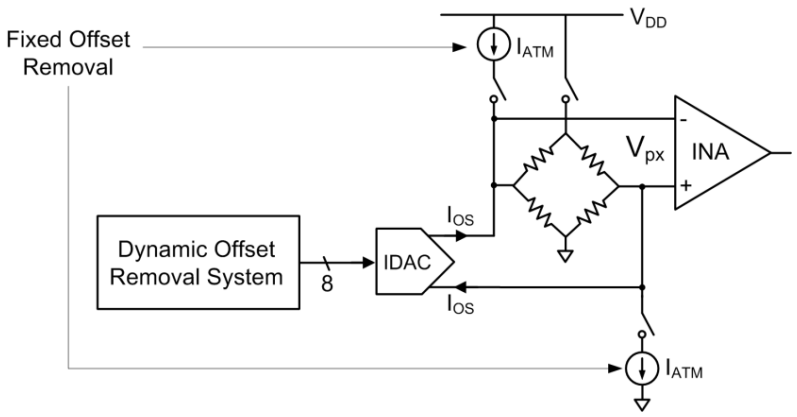


Figure 4-10. Conceptual schematic of the pressure sensor offset removal IDAC, consisting of fixed and programmable offset removal current sources.

The IDAC was designed to remove 34 – 74 mV of pressure sensor offset, corresponding to a pressure offset range of -50 – 1,000 cm H_2O, using the sensitivity parameters of the EPCOS C29

sensor [50], which has an output voltage of approximately 32 mV at 1 atm. The fixed current sources of Figure 4-10 each provide 20 µA, which translates to a 54 mV differential offset over the sensor bridge resistance of 2.7 kΩ. This fixed offset corresponds to the center of the total IDAC range, and the 8-bit IDAC fine-tunes the offset to balance other offsets caused by manufacturing tolerances or environmental factors. The IDAC center range was chosen to be higher than the natural sensor atmospheric offset to allow for inevitable offsets caused by packaging materials.

A schematic for the bipolar IDAC is shown in Figure 4-11. The IDAC is built from a 7-bit binary-weighted array of unit elements (B_X), with each B_X consisting of a PMOS and NMOS current source plus pass transistors for enabling the element current. To maintain low offset the PMOS and NMOS current sources provide identical amounts of current. The D_X control signals for higher-order bits are connected together to provide the binary weighting, and the $I_{U+/-}$ element outputs are all summed to produce two array output currents, I_{PX} and I_{NX}. The B_X outputs are finally routed through a polarity control switch which can reverse the polarity of the IDAC currents. This switch increases the total IDAC resolution to 8 bits by doubling the differential dynamic range to $2 \cdot I_U \cdot 2^N$.

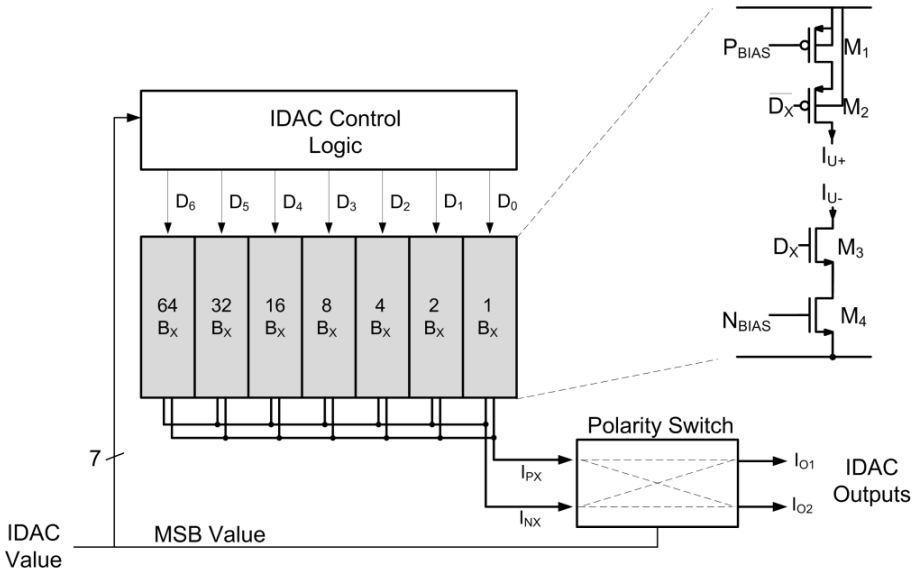


Figure 4-11. Illustration of the IDAC structure, which consists of a 7-bit binary-weighted array of unit current elements, a polarity switch to enable bipolar operation, and control logic to determine sign and magnitude based on the programmed value.

The P_{BIAS} and N_{BIAS} levels which determine the element current $I_{U+/-}$ are generated in a replica copy of the B_X element as shown in Figure 4-12. Diode-connected devices $M_{1,4}$ provide the bias levels to the rest of the IDAC, and switches $M_{2,3}$ are used for turning the IDAC on and off. The input reference currents are generated as identical copies from the oscillator nA current reference. Transistor sizes for M_{1-4} are listed in Table 4-3 and are identical to those used in the B_X elements. The transistors are biased in moderate inversion for good matching and IDAC linearity.

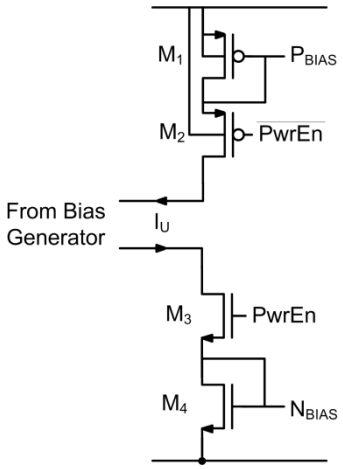


Figure 4-12. Schematic of the IDAC replica bias circuit used to generate P_{BIAS} and N_{BIAS} voltages for each current element.

TABLE 4-3. TRANSISTOR SIZES AND BIAS POINTS FOR IDAC UNIT REPLICA BIAS CIRCUIT.

Name	Value	Inversion Coefficient
M_1	3.6 µm / 11.7 µm	2.6
M_4	3.6 µm / 11.7 µm	1.0
$M_{2\text{-}3}$	3.6 µm / 0.9 µm	-
I_u	60 nA	-

The IDAC control logic performs sign-magnitude conversion on the programmed IDAC value depending on the sign of the MSB as shown in Figure 4-13a. The logic for only one bit is shown for simplicity. When the programmed value MSB is 0, the polarity is defined as negative, and the remaining value bits are flipped. The inversion step is needed to satisfy the dynamics of the offset control loop, which drives the IDAC value toward 0000 0000 to achieve maximum positive offset and 1111 1111 for maximum negative offset. An IDAC output current of zero can be represented by values of 0111 1111 or 1000 0000. This introduces a 1-bit differential nonlineari-

ty in the IDAC transfer function, but the offset control loop does not require a linear or even a fully monotonic IDAC response.

Bipolar operation is achieved with the IDAC polarity flipping circuit shown in Figure 4-13b. The polarity flipping circuit operation is effectively the same as a full H-bridge. Depending on the programmed IDAC value MSB, DIR, the I_{PX}/I_{NX} currents are routed to either one of the I_{O1}/I_{O2} outputs. A value of 1111 1111 produces the maximum IDAC output current of +/- 7.68 µA for the I_{O1}/I_{O2} outputs, while 0000 0000 produces the same output magnitude but of opposite polarity. The enable input, EN, is used for power control, and the IDAC current draw is shutoff when EN=0. The pass transistors in the polarity switch operate in triode and have a negligible effect on the IDAC performance.

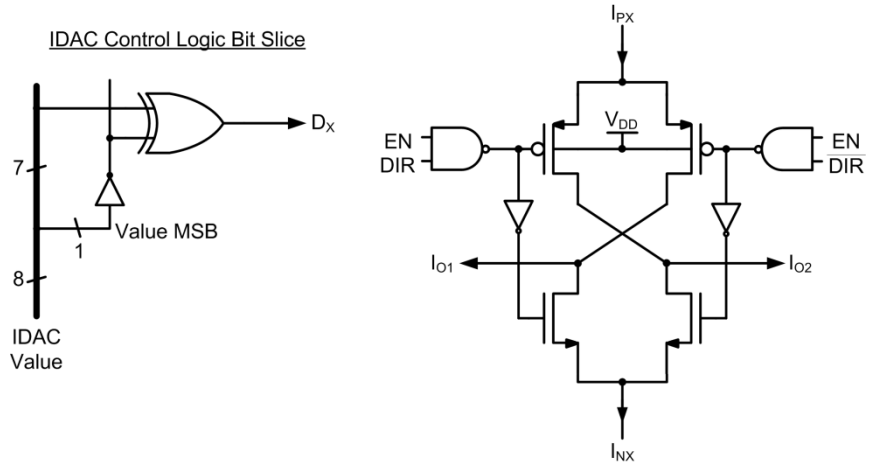


Figure 4-13. Schematics showing how (a) the IDAC control logic inverts the polarity of each programmed bit; (b) the entire IDAC output polarity is flipped depending on the value of the programmed MSB.

4.2.5 *IDAC Noise Analysis*

Because the IDAC injects current directly into the pressure sensor, its noise contribution is multiplied by the full gain of the instrumentation amplifier. Therefore, the IDAC noise performance must be lower than the ADC input-referred LSB spacing, or

$$V_{IDAC,o} < \frac{V_{LSB}}{A_{V,max}\sqrt{12}}, \tag{1.9}$$

where $A_{V,max}$ is the maximum programmable instrumentation amplifier gain. Since V_{LSB} is about 5.5 mV and the maximum gain is 260, the equivalent IDAC noise at the pressure sensor outputs must be less than 6 μV_{RMS}. The measured noise of the IDAC has proved to be problematic. As such, a detailed analysis of its noise is provided in Appendix 11.2.6.

4.3 Activity Detector for Adaptive Transmission Rate Control

Bladder pressures change quite slowly during filling, but contractions and motion artifacts can lead to occasionally rapid pressure increases. The WIMM ASIC senses pressure at 100 Hz to avoid aliasing of these high-frequency signals, but data transmission is the dominant power consumer. To further save power, an activity detector was designed to modify the transmission rate based on the level of bladder activity. Burst-mode transmission could perform a similar function by sending out multiple samples all during the same transmission window, but this would introduce significant latency. To enable real-time, closed-loop bladder control applications, the activity detector was designed to have zero latency; important samples are transmitted immediately while unimportant samples are not transmitted. The activity detector block diagram is shown in Figure 4-14. When the activity detector output is low, the transmitter power-control signal is held low, keeping the transmitter turned off.

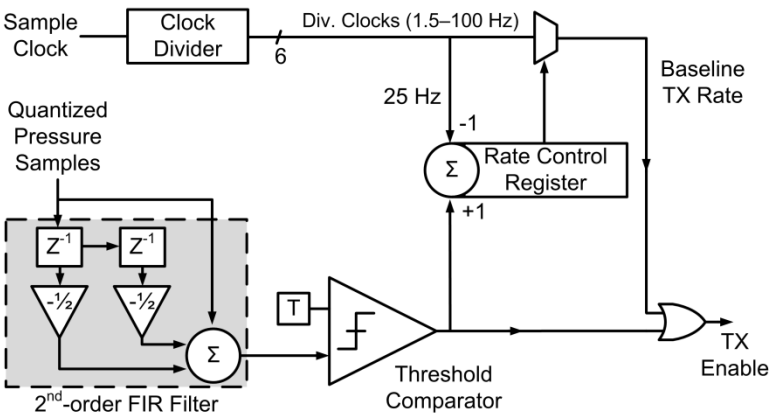


Figure 4-14. Block diagram of the activity detector.

The activity detector is based on the first- and second-order differences of the signal, which approximate the instantaneous first- and second-derivatives. These terms contain frequency information which can be used to determine the optimal sample rate [63]. When these discrete differences are combined, the expression becomes that of a 2nd-order FIR filter given by

$$y(x) = f(x) + \alpha f(x-1) + \beta f(x-2). \quad (1.10)$$

Coefficients α and β can be selected such that y(x) is an indicator of activity. Coefficient values of -½ were chosen to create a high-pass filter with a peaking response at $F_S/_4$, unity gain at $F_S/_2$ and zero DC gain, as shown in Figure 4-15, where F_S is the system sample rate of 100 Hz. The FIR filter output is compared to a threshold by a magnitude comparator; if the sample is significant enough, it is transmitted.

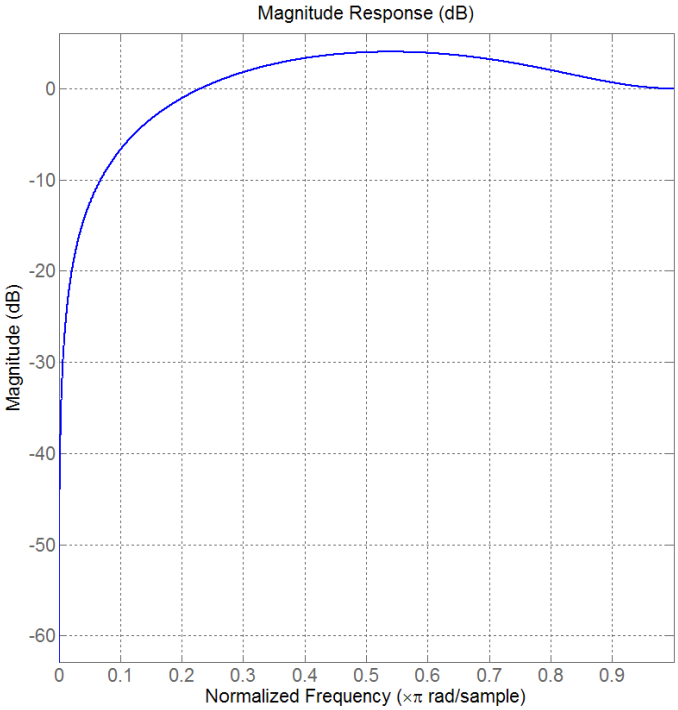


Figure 4-15. Calculated frequency response of the activity detector FIR filter.

The activity detector was designed to have "attack" and "release" times corresponding to typical bladder contractions. Bladder contractions begin with a sharp rise in pressure, followed by a gradual relaxation back to the resting, baseline pressure. The magnitude comparison sets the filter's attack time, or the transmission delay when a sample has been determined to be significant. The attack sensitivity is set by the magnitude comparator threshold; a default value of 3 is used, although the ASIC can be programmed to use values from 1 to 5.

The activity detector was designed to have a long release time so that samples are sent at a slightly increased rate for a period after a contraction starts. The long release time is controlled by a rate control register, which sets the baseline transmission rate from 1.5 – 100 Hz depending on the level of pressure activity. Samples are transmitted at the baseline rate even if the comparator does not indicate activity. The rate control register is incremented when the magnitude comparator detects activity, and is decremented at a constant rate of 40 ms. Thus,

transmission rate remains high for a period of time after activity. Waveforms demonstrating this operation are shown in Figure 4-16 for representative, non-voiding bladder contractions.

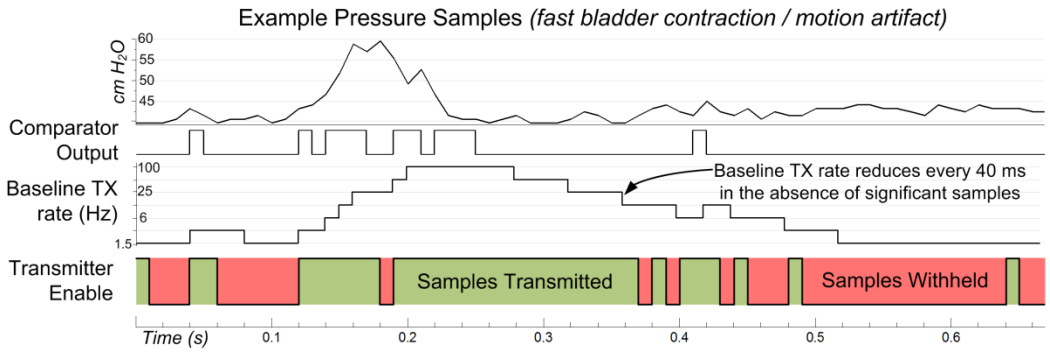


Figure 4-16. Example waveforms of the activity detector showing increased sample transmission rate during periods of high activity. The slow release of the detector provides increased transmission rates after an event.

4.3.1 *Activity Detector Power Saving Estimate*

The primary power draw of the WIMM system is data transmission. Figure 3-6 showed a breakdown of the power consumption by individual circuit. If every sample is transmitted, the system current draw is greater than 47 µA, with transmission accounting for 81% of the system current. The total system current varies from 9.4 to 47.4 µA, for transmission rates from 1.5 to 100 Hz. Assuming that bladder contractions are fairly rare (less than one per minute) the activity detector would yield average system currents below 15 µA.

4.3.2 *Activity Detector Digital Implementation*

To save power the activity detector was implemented using all digital circuits. The circuit was defined in HDL using Verilog 2001. The z^{-1} delays were implemented with a linear shift register and the FIR coefficients of ½ were obtained through single bit right shifting. Signed, 2s-complement addition was used, and the magnitude comparator performs an absolute value on the filter output before comparison to the fixed threshold. To reduce the switching frequency,

the activity detector is clocked only once per sample cycle. A summary of gates is shown in Table 4-4 and the HDL code for this module is contained in Appendix 11.6.

TABLE 4-4. SUMMARY OF SYNTHESIZED GATES FOR THE ACTIVITY DETECTOR MODULE.

Gate Type	Instances	Area %
Sequential	24	30.6
Inverter	39	8.4
Combinational	101	61.0

4.4 Frequency-shift-keyed transmitter

Data is transmitted wirelessly using a frequency-shift-keyed (FSK) transmitter operating at a center frequency of 27.12 MHz. The transmitter is implemented as shown in Figure 4-17 as a negative-resistance oscillator [64]. This topology provides a negative conductance of $-G_m$ and can sustain oscillation in the LC tank providing that its negative conductance is larger in magnitude than the equivalent loss conductance of the tank at resonance. The nominal transmitter oscillation frequency is determined by the resonant frequency of the off-chip LC tank, but an on-chip capacitance C_m is switched in parallel to create an FSK signal having frequency deviation given by

$$\Delta f = \frac{1}{2\pi}\frac{\sqrt{L/C}-\sqrt{L/C+C_m}}{L}. \tag{1.11}$$

Capacitor C_m was chosen to be 1 pF to yield a frequency deviation of 800 kHz with typical external LC values. This frequency deviation is sufficient for the data rate of 100 kbps, and because it is wideband, it does not require coherent detection to receive.

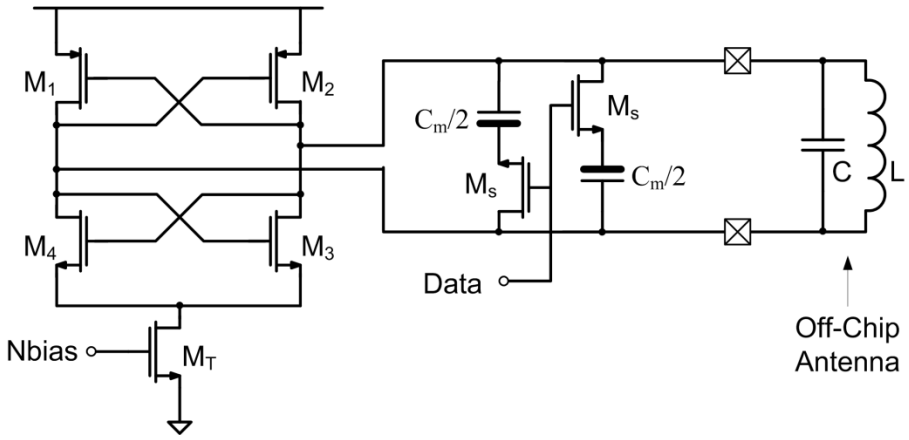


Figure 4-17. Schematic of the FSK transmitter on the WIMM ASIC.

A 3-bit programmable current mirror (not shown) is used to set the bias conditions of the transmitter and thus the transmitted power, since the voltage swing across the tank is approximately $V_{LC} = I_{BIAS}Z_{LC}$. The transmitter power consumption can therefore be optimized for different applications in consideration of factors such as antenna Q, transmission distance, and medium absorption. At the maximum current draw of 490 µA, the transmitter provides -4.5 mS of negative transconductance, yielding a $2V_{PP}$ swing across an LC tank with Q of 25.

4.4.1 *Wireless telemetry protocol*

The WIMM does not require the sophisticated network protocols used by low-power intermittent transmission standards (i.e. IEEE 802.15.4/ZigBee), so a custom telemetry protocol was designed which would minimize the transmitter active time (Figure 4-18). The transmitter sends out 14-bit packets rates of 1.5 -100 Hz depending on the level of bladder activity. Each packet includes an 8-bit pressure sample plus a start frame, and a 680-µsec start-up phase is used in which the transmitter operates at frequency f_0. This start-up period allows the transmitter and external receiver to synchronize before the packet is delivered.

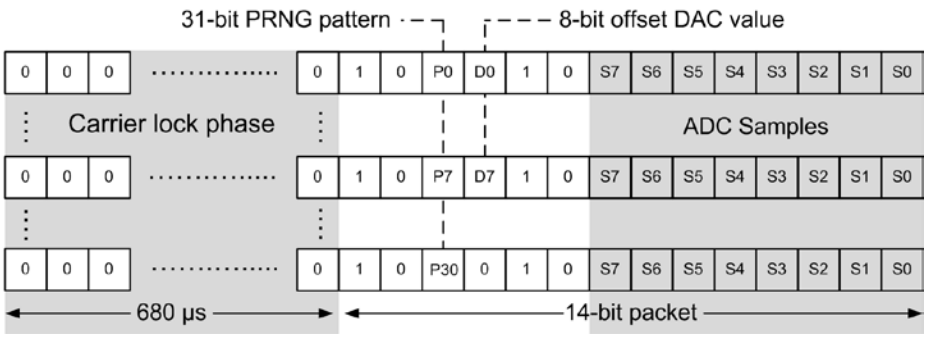


Figure 4-18. Illustration of the WIMM telemetry protocol, which uses a 680-µs synchronization phase, followed by a 14-bit data packet, including a start pattern. A pseudo-random bit pattern and the offset IDAC value are interleaved throughout successive packets to enable synchronization with minimal overhead.

Data packets begin with a 1-0 start pattern which is followed with two interleaved bits, corresponding to the nth bit of a pseudo-random pattern and the *m*th bit of the offset IDAC value. The pseudo-random pattern generator (PRNG) is implemented as a 5-bit linear-feedback shift register which yields a pattern that is 31 bits long, and the next value of the pattern, P_n, is generated for each packet [65]. The offset IDAC updates once every 32 samples, so the IDAC D_m values are also interleaved across multiple packets. The PRNG pattern allows the receiver to determine packet order, and calculate the bit-error-rate of the wireless link. This is useful because the bladder pressure data can contain discontinuous motion artifacts which may be misinterpreted as errors, while the PRNG pattern is deterministic.

4.5 ASIC Performance Summary

The design specifications for the ASIC are summarized in Table 4-5. Specific parameters relating to pressure sensitivity and DAC offset range are listed assuming that the EPCOS C29 sensor is used.

TABLE 4-5. SUMMARY OF ASIC DESIGN SPECIFICATIONS.

Power Management Unit		
Supply regulator output voltage	2.5 V	
Oscillator Clock Frequency	100 kHz	
PMU base current	5.4 µA	Including dynamic digital current
RF recharge current	100 µA	
Standby current	20 nA	

Instrumentation Amplifier		
Gain	150 - 260 X	Programmable
Sample Rate	11.1 kS/s	
Thermal Noise	7 µVrms	Input-Referred
Active Current Draw	36 µA	
Duty Cycle / Sample	3.90%	

SAR ADC		
Resolution	8 bits	
Sample Rate	11.1 kS/s	
Dynamic Range	1.4 V	
Active Current Draw	8 µA	
Duty Cycle / Sample	2.00%	

Offset DAC		
Resolution	8 bits	
Base Output Current	40 µA	Differential output
Dynamic Output Range	+/- 7.62 µA	
Output noise	2.7 µVrms	Into 2.7-kΩ load, 50-kHz BW
Update Rate	3.1 Hz	
Duty Cycle / Sample	2.00%	

FSK Transmitter		
Center Frequency	27.12 MHz	
Frequency Deviation	800 kHz	
Data Rate	100 kbps	
Active Current Draw	0 - 490 µA	Programmable
Duty Cycle / Sample	0.125 - 8.5%	Varies by TX rate

ASIC Performance Summary		
Input Voltage	2.5 - 5 V	3V typical
Sample Rate	100 Hz	
Transmission Rate	1.5 - 100 Hz	
Latency	850 µs	After sample taken
Pressure Resolution	0.8 cm H2O	Using EPCOS C29 sensor
Pressure Range	1,300 cm H2O	
Average System Current	9.4 – 47.4 µA	For TX rate of 1.5 – 100 Hz

CHAPTER 5

ASIC TEST RESULTS

The WIMM ASIC was fabricated in the On-Semiconductor 0.5-µm C5F process, and occupied a die area of about 2.5 x 2.5 mm as shown in Figure 5-1.

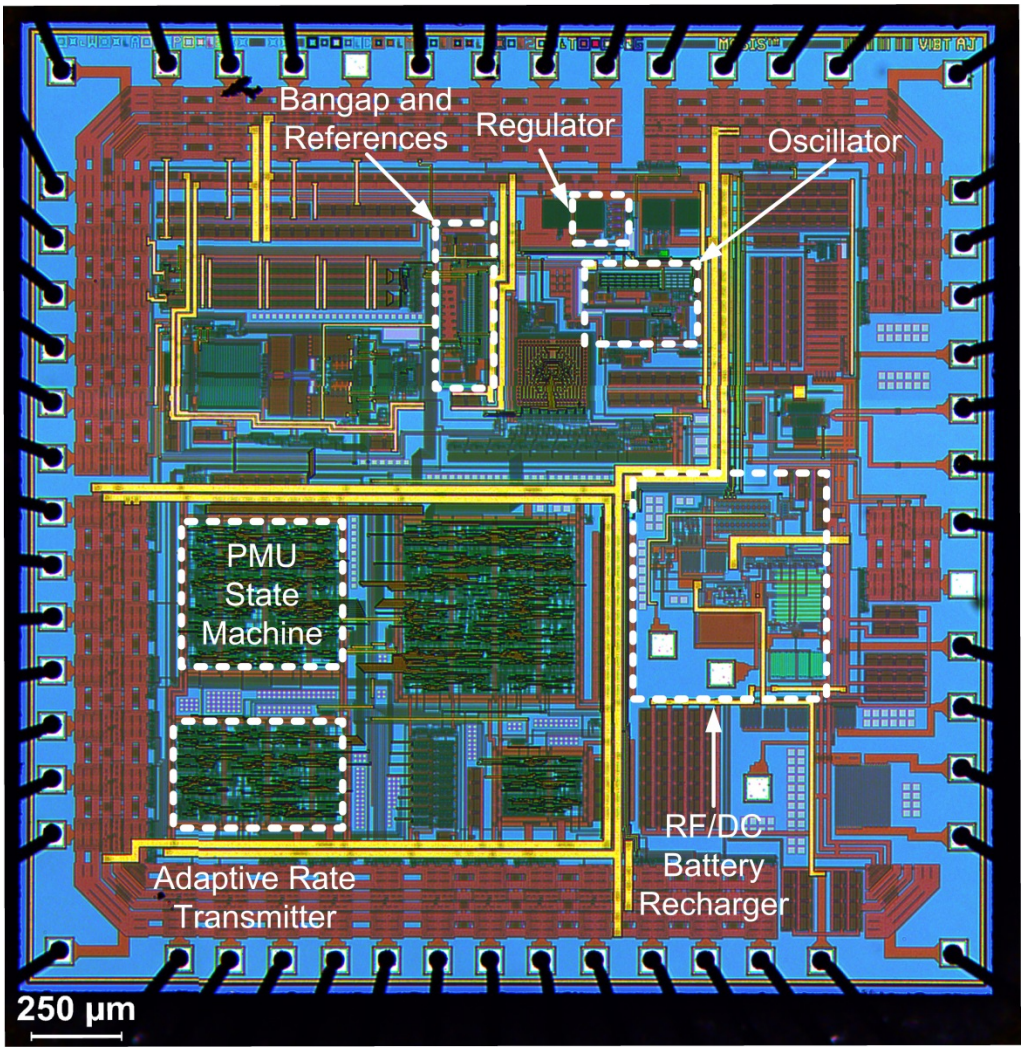


Figure 5-1. WIMM ASIC die photo.

The WIMM ASIC was fully bench-tested before being integrated into an implantable system. The ASIC was wirebonded into a ceramic LCC-52 package and mainly tested with the configuration shown in Figure 5-2. Generally, the test environment was more ideal than the implant so that the ASIC performance limits could be measured. An external 3-MHz RF field generator was used to test the RF recharge and command decoder functionality, while a 27.12-MHz receiver was used to receive data telemetry. A secondary circuit was used to AC-couple differential signals into the INA inputs, while supplying an appropriate 1.3-V DC common-mode level. The piezoresistive pressure sensor bridge was emulated with fixed resistors, and a programmable potentiometer was used to unbalance the bridge for offset cancellation step response testing. Generally, Labview was used to acquire and decode digital data packets from the ASIC and store them for later analysis in MATLAB.

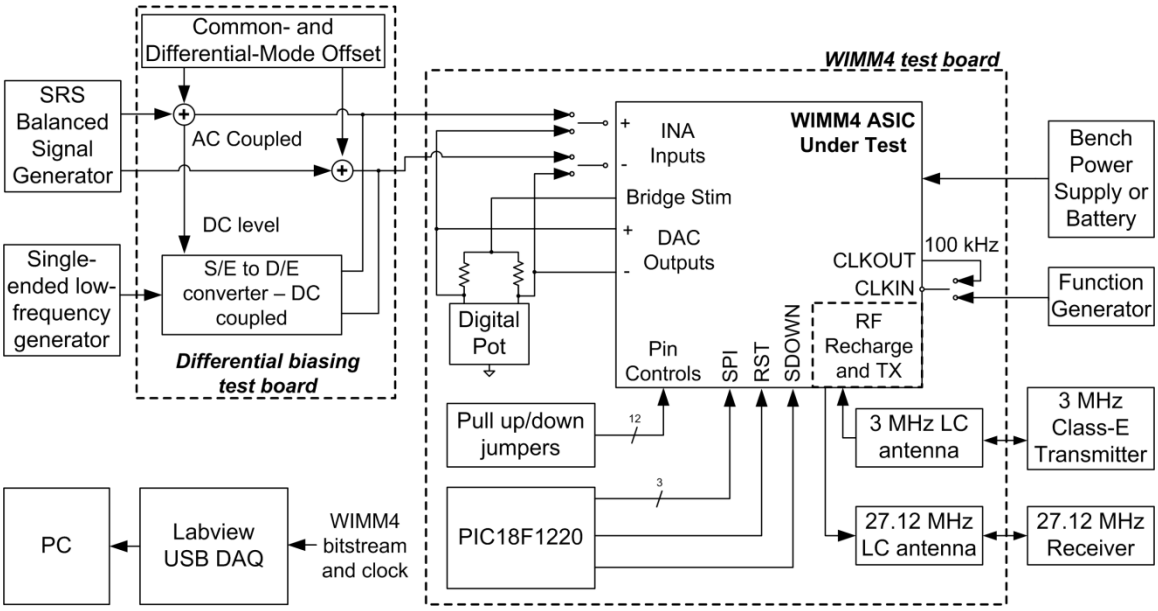


Figure 5-2. Block diagram of the ASIC bench-test environment.

5.1 Power Management Unit Testing

The PMU consists of numerous circuits, which were all bench-tested and verified to be working as intended. These general tests are omitted from in this section for brevity. Key performance metrics for the PMU-such as ASIC dynamic current draw, wireless standby command, and RF battery recharge—are described instead.

5.1.1 *PMU/ASIC Dynamic Current Draw*

The dynamic current draw of the ASIC, as modulated by the PMU, was measured as the differential voltage across a 10 Ω resistor in series with the ASIC power supply. After calibrating the sensitivity of the measurement setup, current measurements were obtained with an oscilloscope, as shown in Figure 5-2. Raw voltage samples were downloaded from the oscilloscope and the ASIC current waveform for one 10-ms sample period was reconstructed by padding the oscilloscope data with the minimum values.

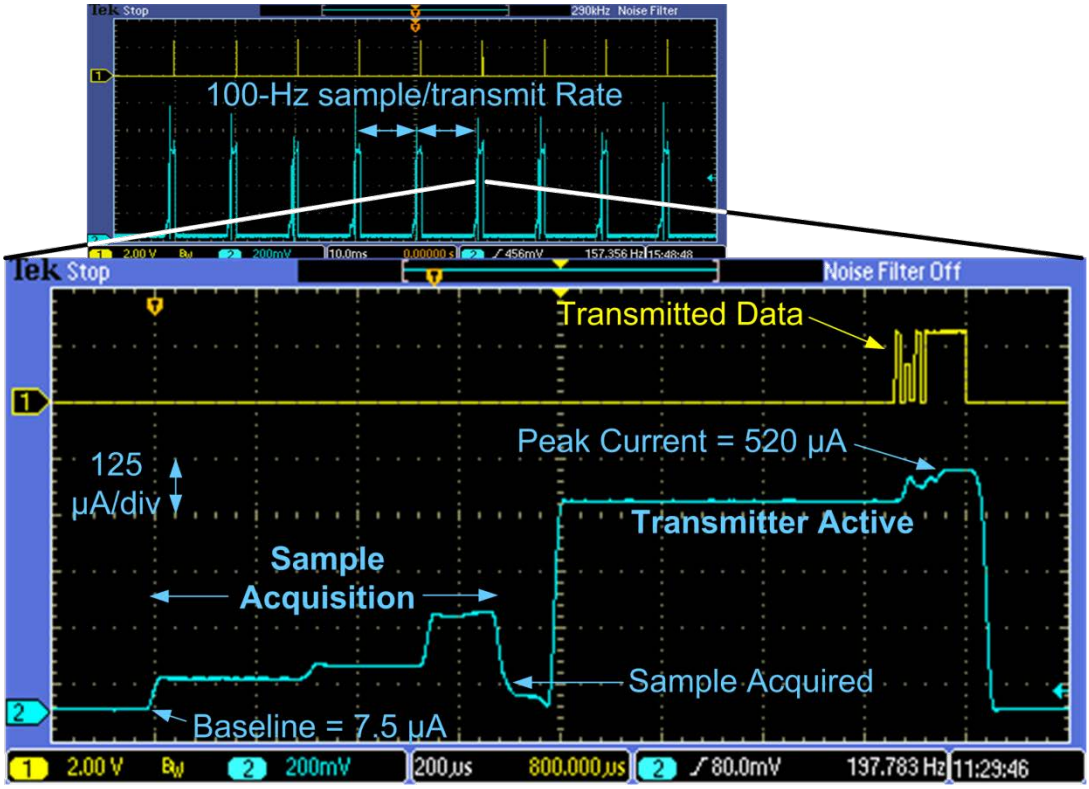


Figure 5-3. Oscilloscope trace of ASIC dynamic current draw during sample acquisition and packet transmission phases.

As expected, the ASIC power consumption is time-dependent since circuits are dynamically turned off. The minimum dynamic current draw of 7.5 µA is about 40% greater than the expected value of 5.4 µA. The increased minimum current draw is possibly due to digital switching currents in the PMU state machine, oscillator, and clock distribution circuits, which run continuously. Current draw for these circuits was estimated as 2 µA in ASIC simulations, but this does not account for all parasitic loading effects which decrease rise/fall time and lead to greater CV^2f power loss.

The peak current draw of the ASIC occurs as the transmitter is modulated during sample transmission, when the ASIC draws 520 µA. Whenever the transmitter is inactive, the average ASIC current draw is 15 µA, and this level increases to a maximum of 74 µA when the ASIC is transmitting at the 100 Hz rate. The ASIC current draw as a function of transmission rate was

measured and is shown in Figure 5-4. The measured current differs quite a bit from the as-designed value, but this could be due to current mirror mismatch, since the transmitter bias current is scaled up by 170X from the base level. Furthermore, the increased power draw of the transmitter during modulation was not accounted for in initial power estimates. For typical transmission rates of 1.5 – 10 Hz, the ASIC average current draw is less than 20 µA.

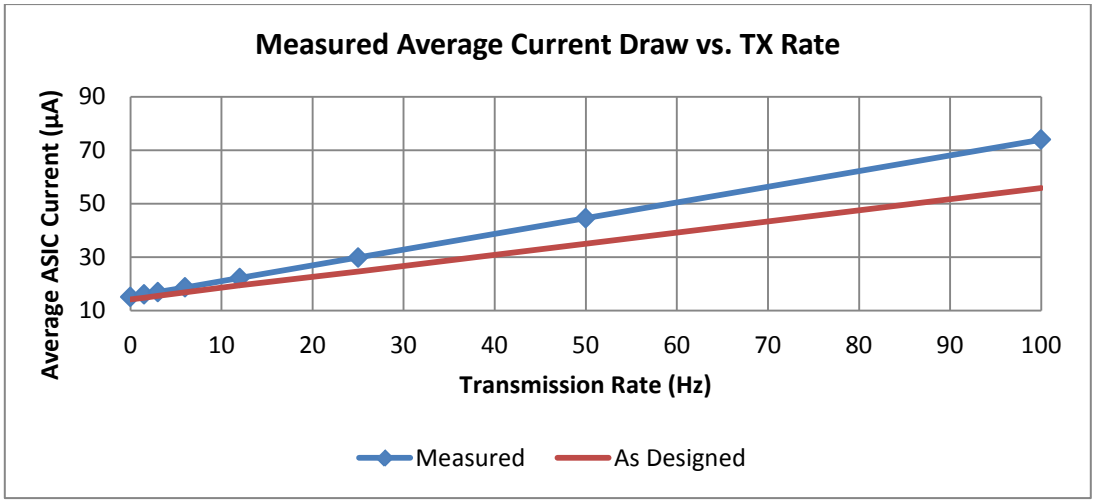


Figure 5-4. Measurement of the ASIC average current draw at different transmission rates.

5.1.2 *Standby Command Receiver and Standby Control*

The standby command receiver was tested by modulating the power provided to the external, 3-MHz RF battery recharger to create an ASK-modulated carrier with about 10% modulation depth. The received RF amplitude (including modulation) was about 10 V peak at the input to the command decoder. The command decoder output was coupled to the ASIC shutdown pin so that after successful reception of the standby command, the analog parts of the ASIC (including the clock oscillator) would be shut off.

An example recording of the standby receiver function is shown in Figure 5-5. In this test, the trace labeled “Command Rx Input” is the input to the external RF ASK modulator. This

waveform sets the envelope of the RF signal, which is extracted by the command decoder. A 100-Hz AM-modulated RF signal and corresponding command decoder output is shown in Figure 5-6 for reference.

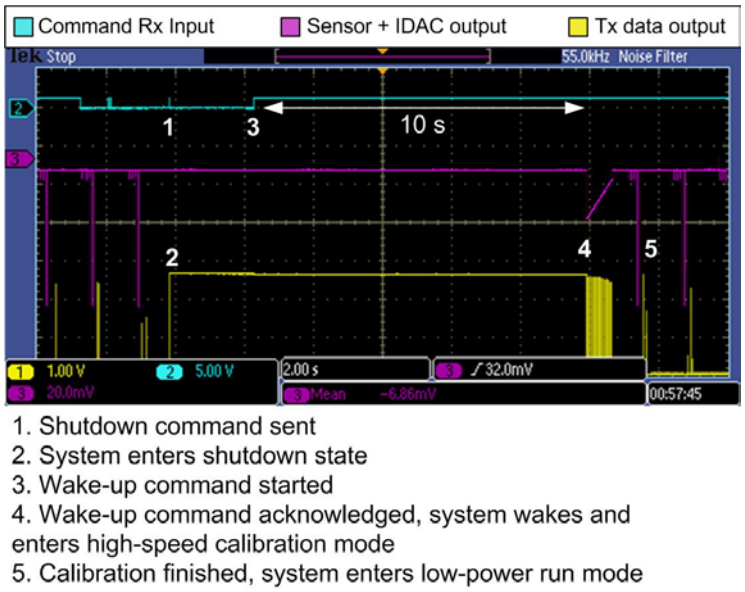


Figure 5-5. Dynamics of system shutting down and waking from standby mode.

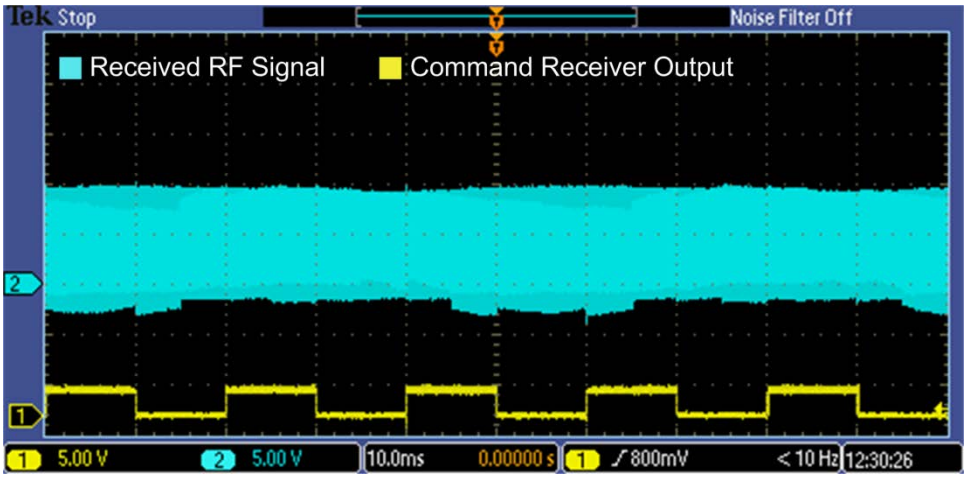


Figure 5-6. The command receiver recovered signal from 10% modulation on 3-MHz wireless recharge field.

The oscilloscope trace of Figure 5-5 demonstrates both the standby and resume functionality of the command decoder. After the shutdown command is sent (1), the system enters a shutdown state (2); the cessation of transmitted data packets indicates that the analog clock oscillator has stopped. When the RF recharge field is turned back on (3), the command decoder monitors the signal for 10 seconds. If the RF field stays on continuously for the 10-s duration, the command decoder turns the ASIC back on (4). As soon as the ASIC turns on it enters a high-speed offset calibration mode in which the IDAC ramps up from its minimum value, as shown in detail in Figure 5-7. When the ADC begins to respond with valid codes the calibration is finished (5) and the system enters the normal, low-power 100-Hz sampling mode.

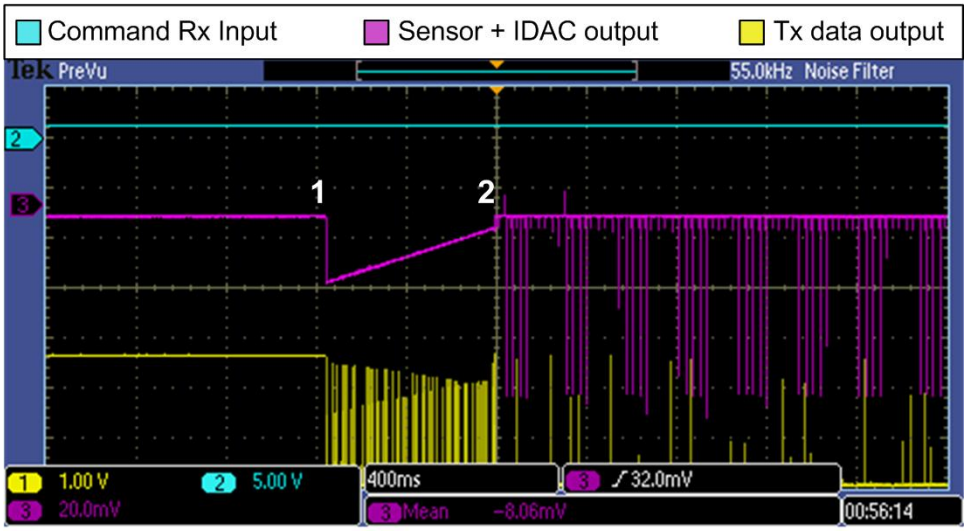


Figure 5-7. ASIC wake from shutdown and calibration phases.

5.2 Pressure Sensor Instrumentation Testing

The performance of the ASIC instrumentation circuits was verified using a high-resolution function generator (SRS DS360) capable of producing single-tone sinusoids of low amplitude and distortion. Resistors equal to the bridge impedance of 2700 ohms were placed in series with the ASIC amplifier inputs to mimic the equivalent output impedance of the pressure sensor. ADC samples were collected using an FPGA and a Labview DAQ.

Rather than a direct measurement of the ADC differential non-linearity (DNL) and integral non-linearity (INL), which requires a fairly sophisticated ramp generator, these performance metrics were extracted directly from the single-tone sinusoid measurement. Since the ASIC samples at 100 Hz, a sinusoid of 2.86 Hz was chosen to be non-harmonically related to the sample rate such that the sinusoid was sampled randomly. The collected samples were analyzed in the frequency domain by taking the discrete Fourier transform (DFT) of the data and computing various performance measurements. This method cannot explicitly describe the ADC DNL, but the INL can be inferred through the harmonic distortion of the DFT. The ADC quantization noise, DC offset and gain errors can also be calculated directly from the DFT.

5.2.1 *SAR ADC Performance*

The ADC on the WIMM ASIC was separately tested from the instrumentation amplifier by enabling a special test mode which decoupled the amplifier output and allowed the ADC to be driven directly. The ADC performance was verified prior to instrumentation amplifier testing because during normal operation the amplifier output is only observable through the ADC samples. A 2.86-Hz, full-scale amplitude sinusoid was applied at the ADC input to sweep through all the available ADC codes. The spectrum of the output samples is shown in Figure 5-8, with an

assumed ADC bandwidth of 50 Hz due to the overall sample rate of 100 Hz. There is almost no evidence of harmonic distortion after the 2nd harmonic, and the recorded tone at 32 Hz was due to interference in the test setup.

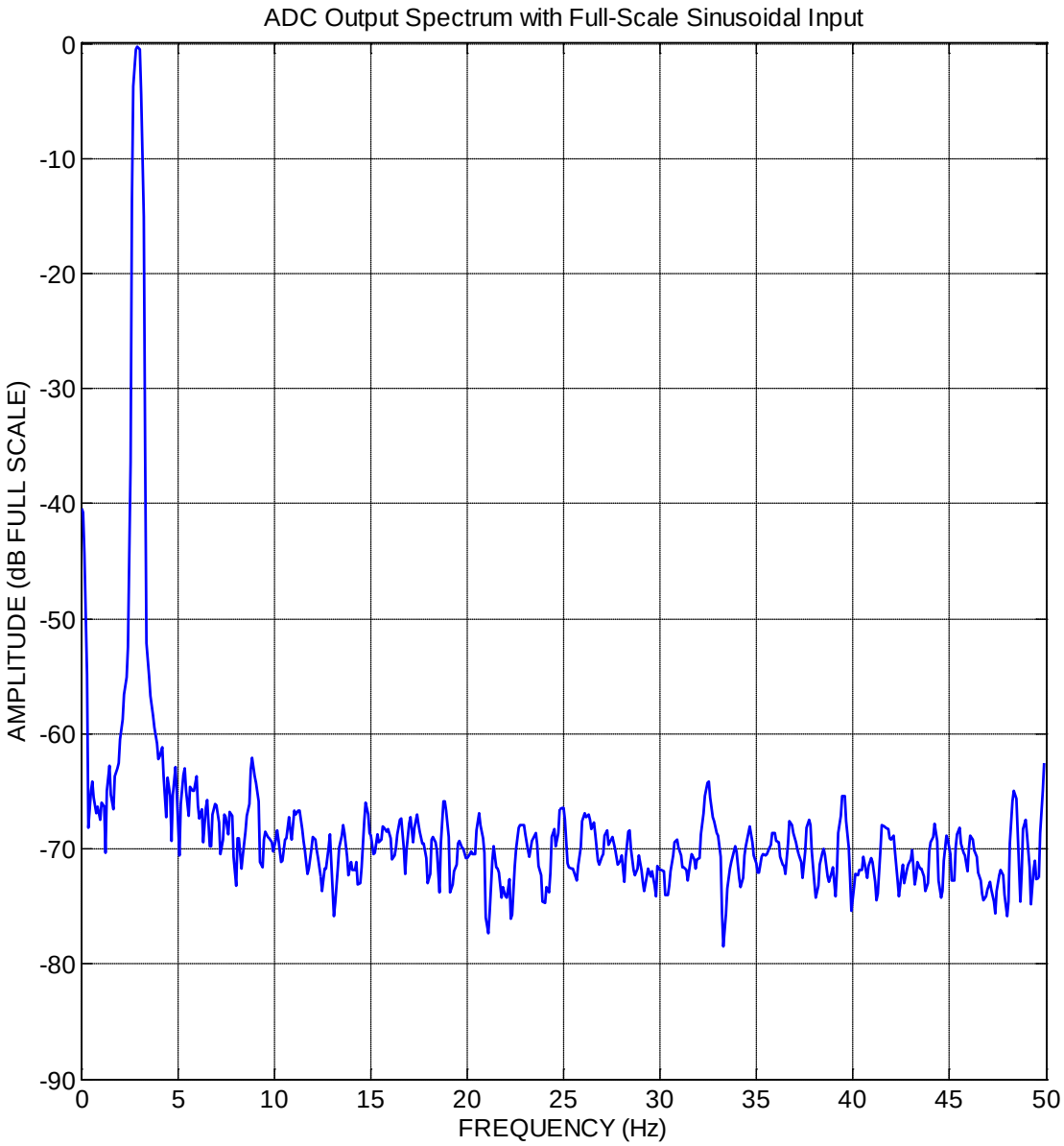


Figure 5-8. Power spectrum of ADC samples used to calculate ENOB.

A histogram of the samples is shown in Figure 5-9, confirming that the ADC has no missing codes in its transfer function. There is a reduced but non-zero number of hits at code 207, as well as reduced counts at integer multiples of 8 from this code. It is likely that on the particular IC tested here that the ADC 3rd capacitor has the largest mismatch and is therefore contributing the most ti DNL and distortion, with a maximum DNL error occurring at code 207.

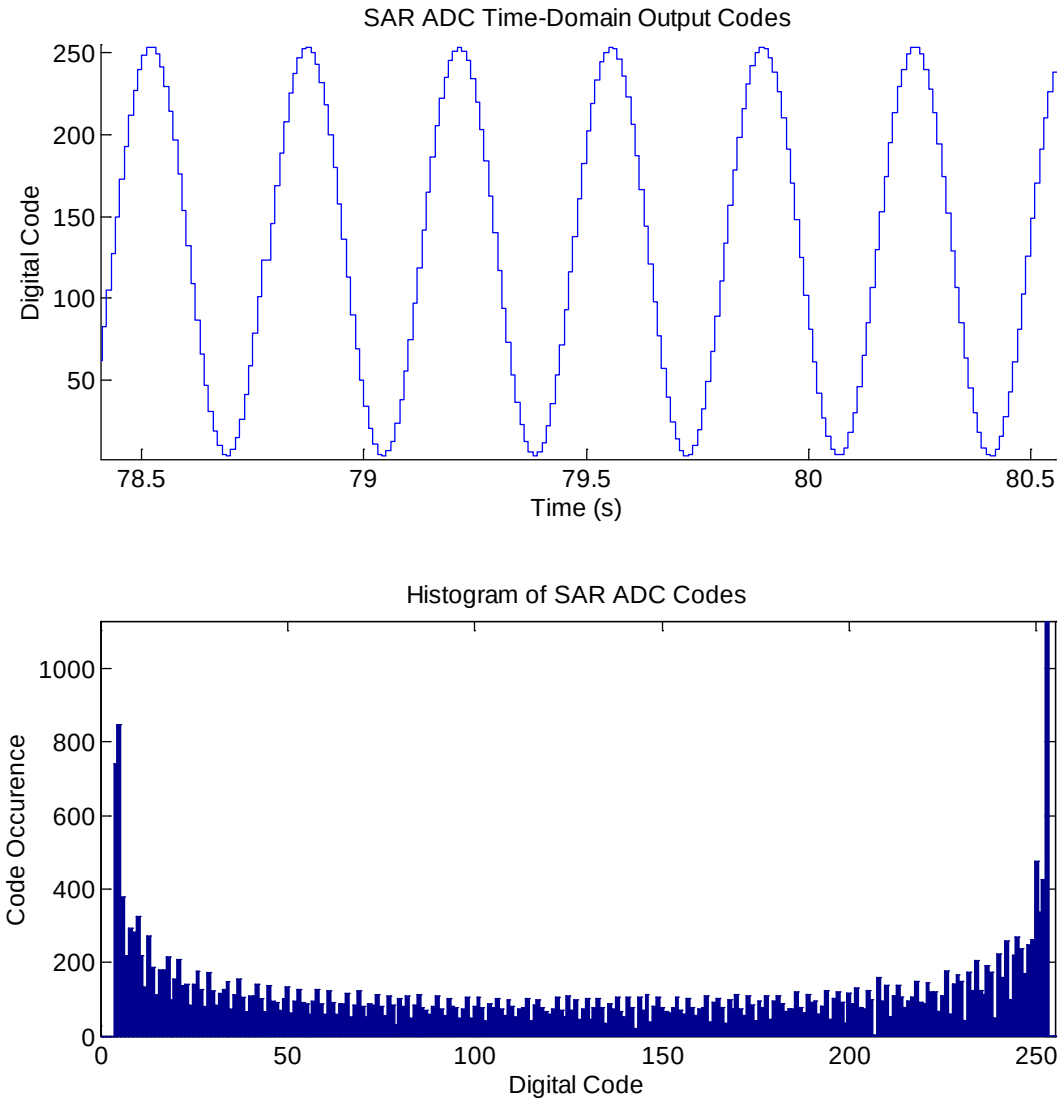


Figure 5-9. Time-domain ADC samples and histogram of 300-second recording indicating no missing codes.

The ADC performance parameters were extracted directly from the DFT using a MATLAB program copied in Appendix 11.7. The signal power was computed by integrating the main tone width across a small number of frequency bins to account for jitter in the ADC clock and signal generator. The SNDR was calculated using the first 9 harmonics of the output tone, and the effective number of bits (ENOB) of the ADC was calculated using the formula

$$ENOB = \frac{SNDR - 1.76}{6.02}, \tag{1.12}$$

in which the 6.02 term converts the SNDR from dB ($\log_{10}$) to bits ($\log_2$) and the factor of 1.76 represents the quantization noise of an ideal ADC. Only an ideal ADC can achieve an ENOB equal to the ADC target resolution, but generally an ENOB within 0.5 bits of the target resolution indicates an ADC with less than 1-bit DNL. The measured ADC performance parameters are summarized in Table 5-1.

TABLE 5-1. MEASURED ADC PARAMETERS

ADC Parameter	Measured Result
DC offset	< 1 LSB
Gain error	< 0.5% full-scale
ENOB	7.79 bits
SNR	> 48 dB

5.2.2 *Instrumentation Amplifier and SAR ADC Performance*

Because the instrumentation amplifier output is directly sampled by the ADC, it is not possible to measure amplifier-specific performance such as bandwidth, thermal noise floor, etc. without being limited by the ADC resolution. Therefore, the primary measurement outcome for the INA was to confirm that it could provide the desired level of programmable gain without

degrading the ADC ENOB by adding nonlinearity or noise. A balanced signal was applied to the INA inputs through bridge-matching resistances, and the ADC samples were analyzed with MATLAB. The INA gain range was calculated by measuring the amplitude of the output tone, and the DC offset was measured as the mean of the ADC codes over an integer number of sinusoidal cycles. The INA ENOB was calculated by applying the largest signal at the INA input that caused ADC clipping to ensure full-scale output amplitude. Recorded spectra of the INA at all gain settings is shown in Figure 5-10 and the measured performance parameters of the INA are summarized in Table 5-2.

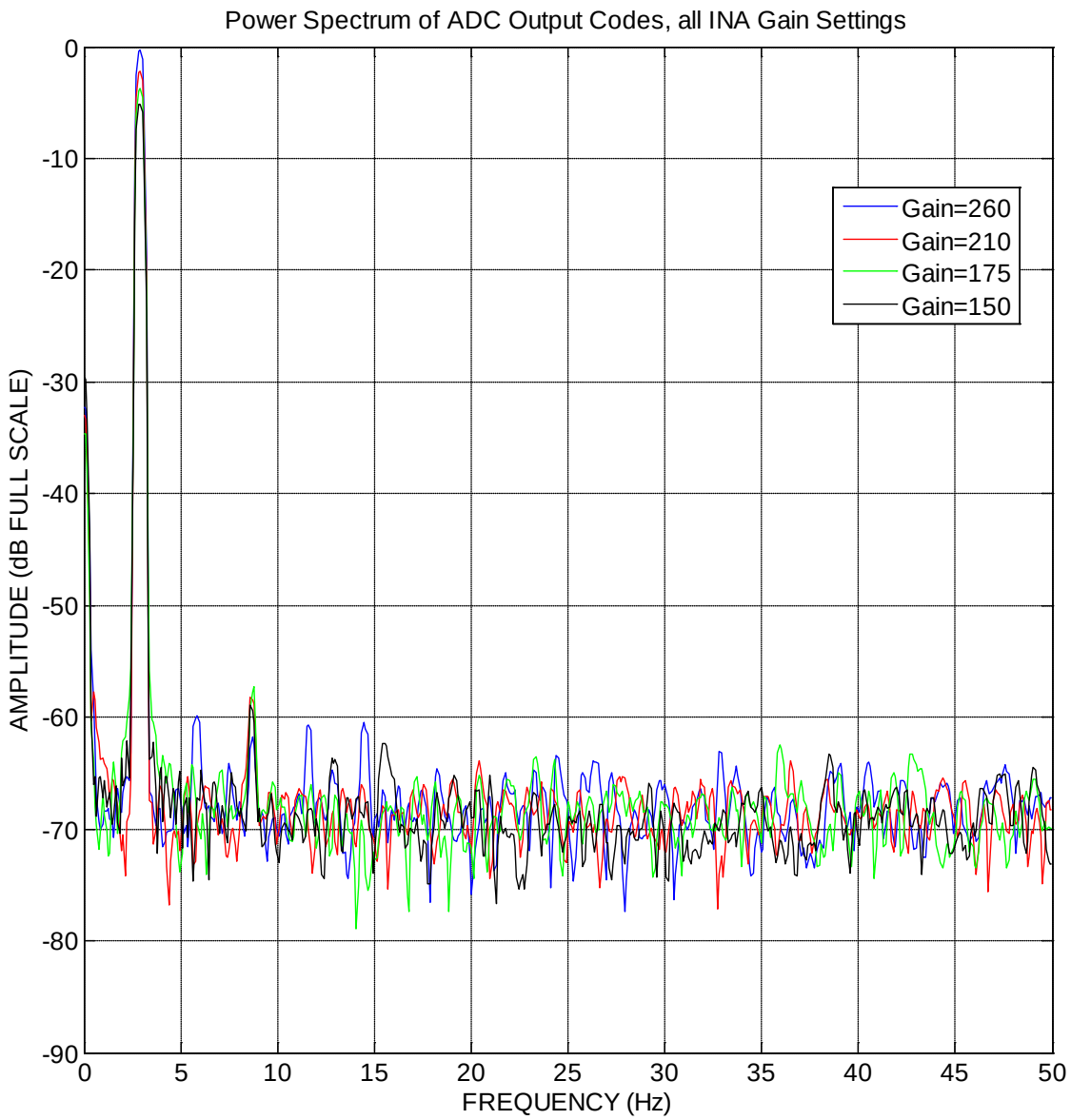


Figure 5-10. Power spectrum of ADC samples when testing the INA at all gain settings.

TABLE 5-2. MEASURED INA PARAMETERS

INA Parameter	Measured Result
Differential gain	261.2 – 208.0 – 174. 4 – 150.1 V/V
Gain inaccuracy	< +/- 1%
DC offset (input-referred)	< +/- 8 mV
ENOB	7.45 – 7.68 bits
Noise floor (input-referred)	< 20 µVrms

5.3 Pressure Sensor Offset Removal Testing

The offset removal system was tested using a simulated pressure sensor built from 4 matched, 2.7-kΩ resistors arranged in a Wheatstone bridge configuration. A programmable digital potentiometer was used to unbalance the bridge to test the automatic removal system step response. First, the noise and linearity of the offset IDAC were tested, then the time constant of the offset removal loop was measured to analyze the frequency response of the WIMM system.

5.3.1 *IDAC output noise*

Because the IDAC is only turned on for brief periods during sample acquisition, its noise contribution cannot be directly measured by conventional instruments. However, an approximate measurement of the IDAC noise was made by pausing the ASIC clock during the sample period to force the IDAC to output a DC current. The output current was connected to one half of a 2.7-kΩ bridge to simulate the load resistance of a pressure sensor, and the resulting noise spectrum was captured with an active probe and spectrum analyzer. It was assumed that the noise of both IDAC outputs was uncorrelated and that this single-ended measurement could be doubled to account for the effective differential-mode IDAC noise.

To account for the thermal noise contributions in the test setup, the noise spectrum was measured with and without the IDAC connected to the half bridge. The measured IDAC noise power (in $^{V}/_{\sqrt{Hz}}$) was subtracted from the reference measurement to obtain a power spectrum of the noise added just by the IDAC, as shown in Figure 5-11. The total IDAC noise was calculated by integrating the noise spectrum over a 50-kHz bandwidth and doubling to account for the differential mode output. The measured noise of 7.79 µVrms is about twice as large as the designed value, but this is still below the input-referred ADC quantization noise at the maximum INA gain. This measurement is also pessimistic because it includes very low frequency flicker noise which is partially suppressed since the IDAC is switched off at a rate of 100 Hz.

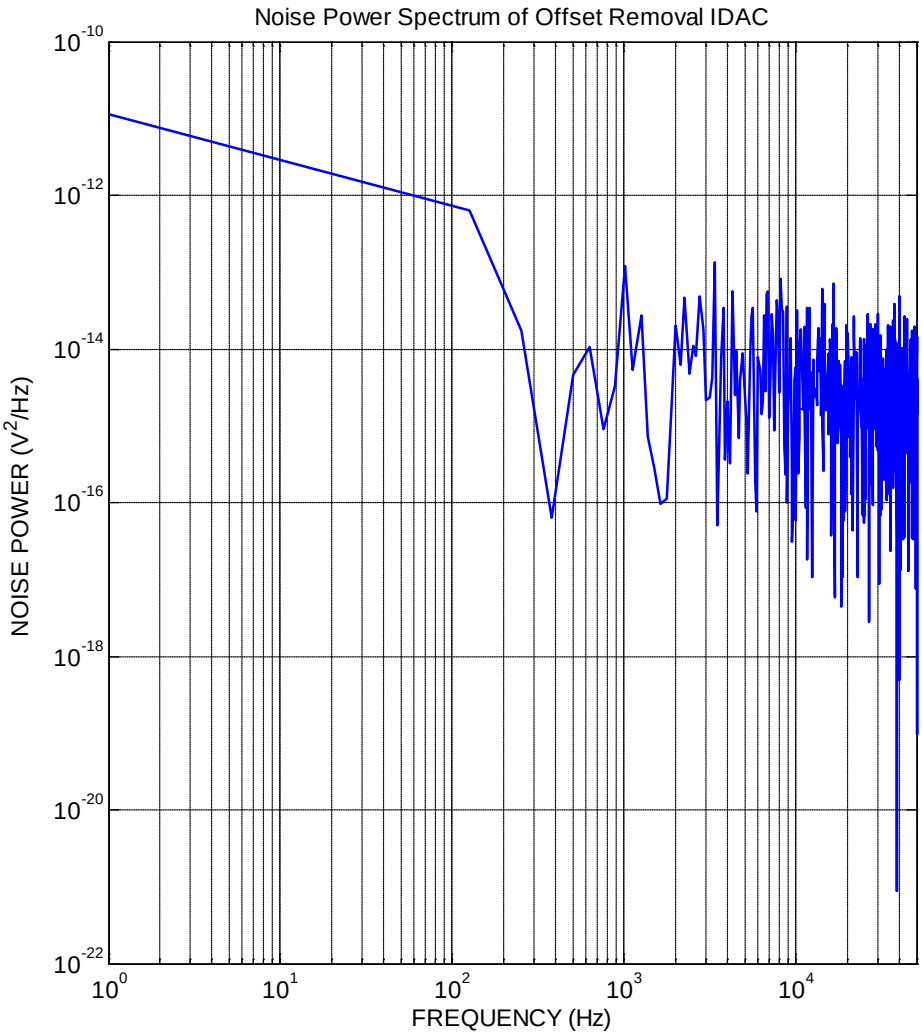


Figure 5-11. Measured frequency response of single-ended IDAC output noise over INA bandwidth.

The IDAC noise is observable in the normal mode of operation, even though the IDAC itself produces noise lower than the ADC quantization limit. When the fixed-resistance bridge is connected to the offset removal system however, the ADC produces noise codes in the range of +/- 2-3 codes depending on the INA gain setting. Typical plots for the time-domain samples of the noise are shown in Figure 5-12. Histograms of the data show that the IDAC noise is approximately normally distributed, suggesting that the noise is independent and random.

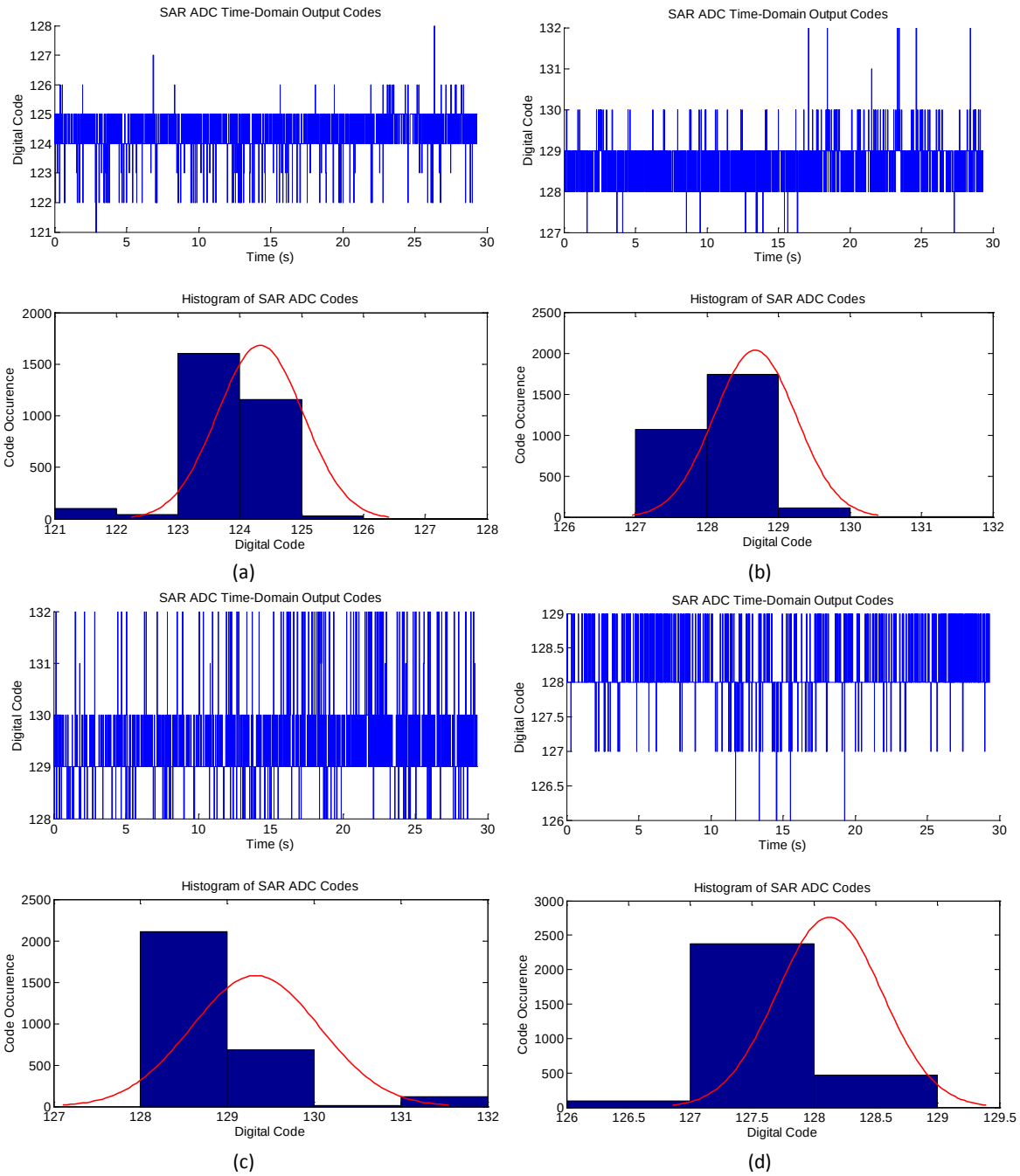


Figure 5-12. Collected IDAC noise recordings in low-power sampling mode, INA gain settings 260 – 150 in (a) – (d). The histograms of the data roughly match normal distributions suggesting that the noise is random.

The likely cause for the increase in IDAC noise during the low-power, sampling mode of ASIC operation is due to insufficient warmup and/or settling time for the IDAC. Since the IDAC

operates at such low current levels, any parasitic capacitances within the current reference must slew to the quiescent voltage levels before the IDAC output is stable. The IDAC turns on 60 µs before the sensor bridge is activated and sampled, but this period may not be long enough. Furthermore, when the sensor bridge turns on, the IDAC output current is temporarily shifted by the sudden change in the load resistance, which creates an additional settling requirement. The increased level of IDAC noise effectively reduces the system pressure sensing resolution to the 7-bit level over the full 50-Hz bandwidth. However, if the recorded samples are low-pass filtered to a bandwidth less than 12 Hz, 8-bit sensing resolution can still be achieved.

5.3.2 *IDAC linearity*

High IDAC linearity is not critical for proper functionality of the offset-removal system, but it does reduce 2^{nd}-order effects in the overall system frequency response. In the automatic offset removal mode, the IDAC updates too slowly to effectively test the system without hitting timing limits in common test equipment, so the linearity was roughly measured by setting the ASIC into a mode in which offset is rapidly removed once when the ASIC powers up. By connecting the pressure sensor to the ASIC with reverse polarity, the removal system enters a forever loop in which the IDAC continuously ramps through its full range while the ADC remains saturated, as shown in Figure 5-13. The full-scale IDAC ramps were collected by an oscilloscope and analyzed in MATLAB with a linear fit. Residuals of the fit were collected and averaged to determine the average nonlinearity of the IDAC. The largest residual represents the maximum measured nonlinearity. The residuals were normalized to the full-scale output of the IDAC and an average nonlinearity of 0.62% with 1.87% maximum nonlinearity was observed. This is below the 8-bit level of the IDAC, but the measured transfer function was monotonic, which increases the stability of the automatic offset removal system.

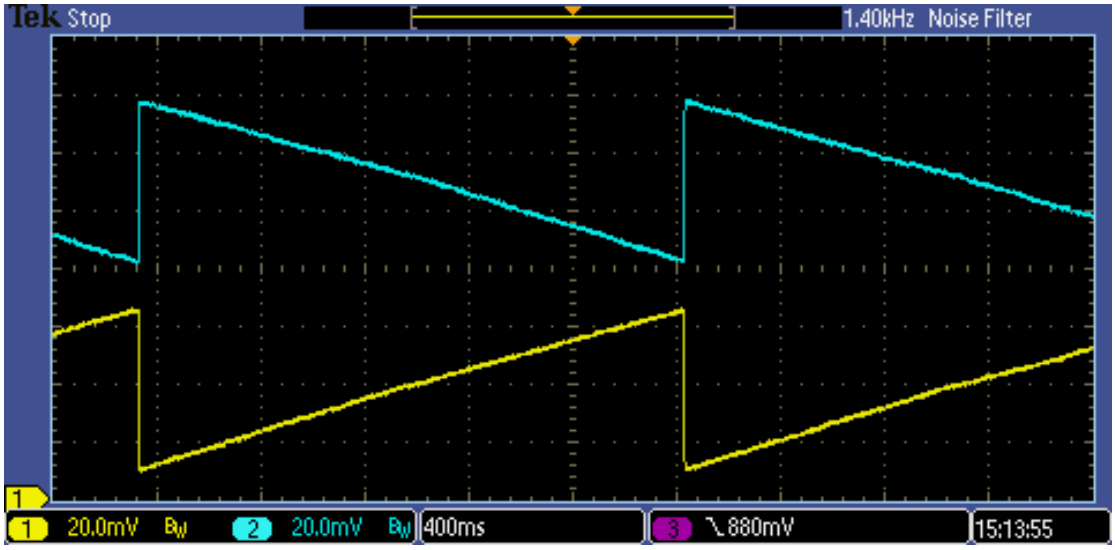


Figure 5-13. Differential IDAC output voltages collected at the INA input during rapid offset cancellation.

5.3.3 *Offset cancellation step response*

The automatic offset removal system step response was tested by first allowing the system to stabilize for about 10 minutes. This was verified by checking that the average output of the ADC was stable near 128 codes. After recording was started, a step input change of +/- 50 Ω (about +/- 10 mV) was applied using a digital potentiometer. The resulting step response at the ADC output was recorded and the IDAC raw values were extracted from the PRNG-synchronized data packets. A MATLAB program was used to analyze the data by fitting an exponential to the IDAC values. The IDAC values are used for the fit since they do not saturate at the beginning of the step, like the ADC values, and the IDAC values are not corrupted by noise. An example plot showing the IDAC and ADC values is shown in Figure 5-14, with the ADC samples shifted down by 128 codes. The offset removal system always drives the average ADC value back to 0, regardless of gain setting. The final IDAC value required to balance the offset is gain dependent, as shown by the final settled IDAC value in each step response.

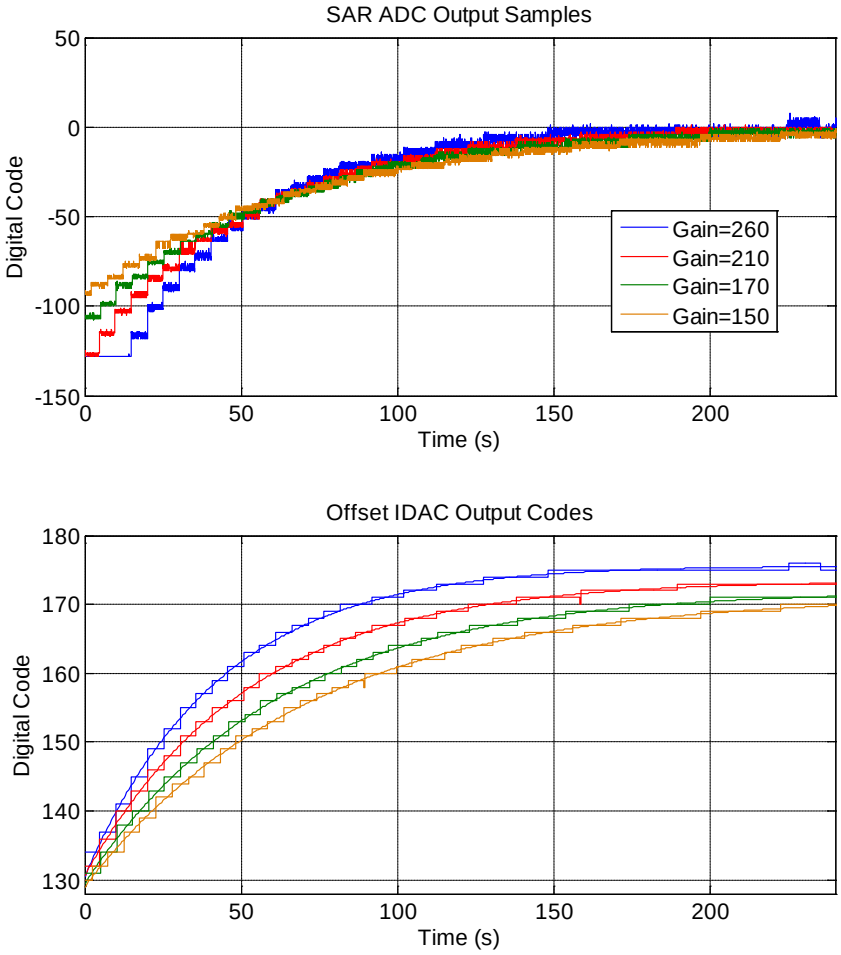


Figure 5-14. The auto-offset removal system step response at all INA gain settings.

The size of the input step was chosen to be slightly larger than the full-scale range of the INA at the largest gain range. This was chosen so that the step would still be a large portion of the full-scale range at lower gain settings. As a result, the ADC saturates for a brief period and the offset removal system step response is slew limited. The transition period from slew-based to linear settling slightly affects the precision in the measured time constants. Time constants were extracted from 2nd-order exponential fits shown as solid lines on the IDAC values plot of Figure 5-14. The time constants τ_{OS} for the different gain settings are summarized in Table 5-3

and agree with expected values. The effective system frequency response to small-scale AC offsets can be estimated as $^{1}/_{2\pi\tau_{OS}}$ and is also listed in the table.

TABLE 5-3. MEASURED TIME CONSTANTS OF THE AUTOMATIC OFFSET REMOVAL SYSTEM.

INA Gain	Estimated time constant (seconds)	Measured time constant (seconds)	Offset system high-pass corner frequency (mHz)
150	68.3	70.2	2.3
170	60.3	62.0	2.6
210	48.8	51.3	3.1
260	45.5	42.2	3.8

5.4 Telemetry and Digital Implementation

The telemetry and digital portions of the ASIC were mostly tested under wired conditions, so that the telemetry packets could be recorded without error. Many of the ASIC outputs were wirebonded for observation; in practice these signals would be ignored or simply re-routed back into another IC pin.

5.4.1 *Adaptive Rate Transmission / Bladder Activity Detector*

The activity detector was tested with a variety of simulated signals to evaluate its performance. The ASIC can be configured to transmit every sample, while the detector output can be monitored to determine what samples would have been sent by adaptive transmission. When the activity detector output is high, the corresponding sample would have been transmitted. Thus, with each test two sets of data are generated: one in which every ADC sample is collected (D_O) and a second in which the ADC data is re-sampled by the activity detector output (D_A). The re-sampled data is reconstructed using a zero-order-hold to simulate the samples which would have been received wirelessly using an adaptive transmission rate.

The data compression level is calculated as a percentage of withheld samples, or as the ratio of the sample lengths of D_O and D_A. This performance metric essentially represents the level of power savings achieved by adaptive transmission, because the transmitter is never turned on for a withheld packet.

Another key performance metric for the activity detector is the level of error it introduces. The root-mean-square-error (RMSE) added by the activity detector is calculated as

$$RMSE = \sqrt{\sum_{i=1}^{N_D} \left[{(D_{Oi} - D_{Ai})}/{N_D} \right]^2}, \tag{1.13}$$

where ND is the sample length for the recorded data. The RMSE is normalized to a unitless quantity (NRMSE) by dividing the RMSE by the range (min/max values) in D_O. The NRMSE can be expressed as a percentage of added error and allows comparison between different data sets.

The activity detector was tested with a variety of slowly-varying signals to determine the typical compression levels and NRMSE added. One example recording is shown in Figure 5-15, in which simulated, very-slow EKG signals were generated by a waveform generator and fed into the ASIC INA inputs. This signal was chosen for convenience, and because it represents dynamic, fast-changing features along with slower periods, similar to the bladder. In Figure 5-15a, the red dots correspond to ADC samples while the black line is the output of the activity detector and zero-order-hold. Figure 5-15b shows the binary activity detector output, and as expected the output remains high consistently when the data exhibits high rate-of-change.

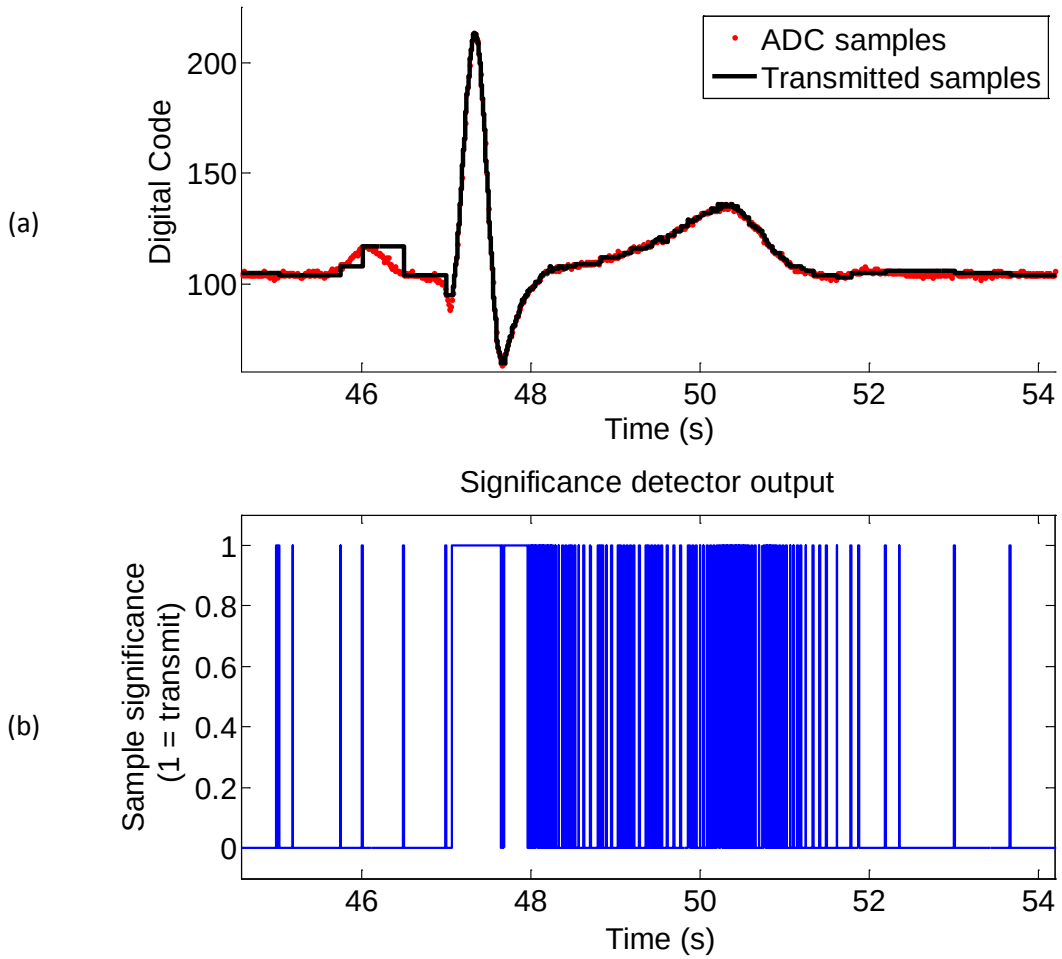


Figure 5-15. Measurement of the (a) as-recorded and adaptively-transmitted data and (b) the activity detector transmission enable output.

In this example, the average compression level is 76%, and the NRMSE is about 1.8%. In general, the detector output captures the rapid changes with high fidelity and introduces greater error during slow periods. This is desirable in applications like bladder pressure measurement where contractions and symptoms of urological disorder tend to be very fast compared to filling-related pressure changes.

The activity detector was also tested with pre-recorded bladder pressure signals obtained through *in vivo* testing of the implanted WIMM system. A Labview DAC was used to recreate the measured signals which were fed directly into the ASIC INA inputs. An example of the

activity detector responding to a voiding contraction in an ambulatory canine is shown in Figure 5-16.

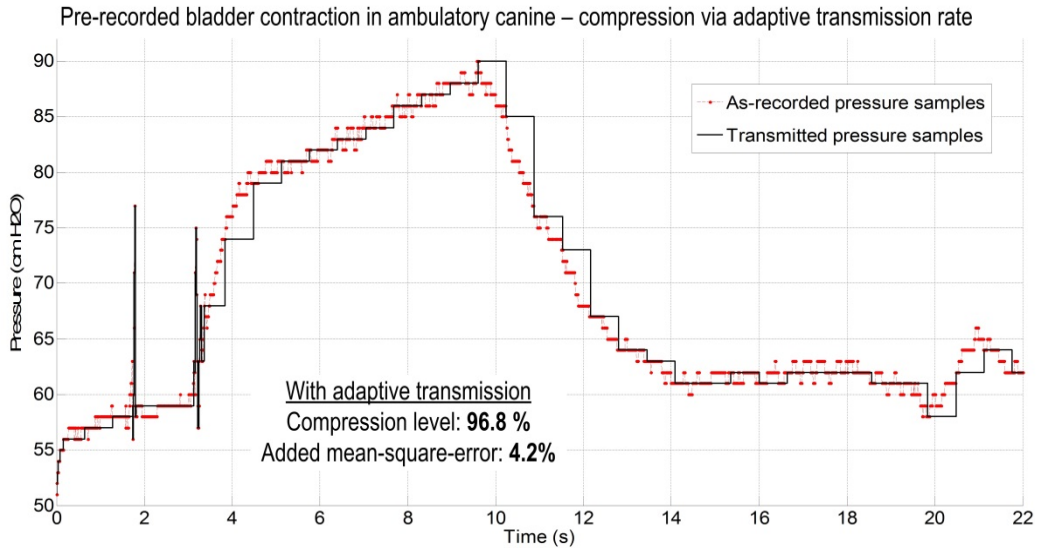


Figure 5-16. Measured response of the activity detector to pre-recorded bladder pressures from an ambulatory canine.

As before, the activity detector transmits rapid pressure changes without delay, as can be seen in the first 5 seconds of the recording. These rapid spikes are likely motion artifacts but are transmitted immediately since they could be the start of a meaningful bladder event. In this example the activity detector used an average transmission rate of 1.5 Hz, introducing 4.2% average error while saving about 97% that would have been consumed through 100-Hz transmission.

As a final test, pre-recorded bladder pressure signals from a resting human subject were applied to the ASIC. The subject suffered from urinary incontinence and electrical stimulation was applied twice to arrest unwanted contractions. The contraction portions of the data are physiological, but the bladder filling (slow pressure rise) was accelerated by catheter-based uro-

dynamics equipment which pumps saline into the bladder at a faster than physiological filling rate. The measured and "as-transmitted" signals are plotted in Figure 5-17.

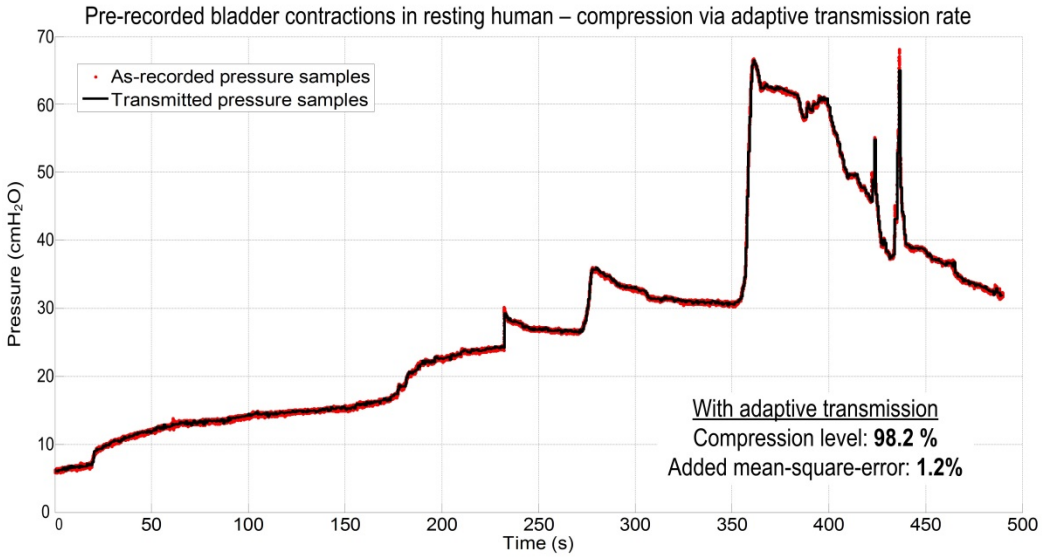


Figure 5-17. Measured response of the activity detector response to bladder pressure signals obtained from a human subject during cystometry.

As in the previous example, for slowly-varying data such as this, the adaptive transmission rate can provide very large compression levels (98.2%) while introducing a relatively small level of error (1.2%). Furthermore, the added error predominantly occurs during slow periods, in which high precision is not required for typical urodynamics or closed-loop bladder control applications.

CHAPTER 6

WIMM SYSTEM DESIGN

The WIMM system consists of the implantable device plus external modules for wireless communication, data recording, and RF battery recharge. Because the implant was designed to be as small and simple as possible, the external devices required unconventional designs to properly function with the WIMM implant. Generally, the external components of the WIMM system were designed for functionality, rather than meeting specific constraints of size or power consumption.

6.1 WIMM External Wireless Receiver Design

The WIMM implant transmits a weak and intermittent RF signal which is modulated using wideband FSK. Because the ASIC clock is not derived from a precision reference and the center frequency of the FSK transmitter can be affected by environmental parasitic capacitance, the receiver was designed to avoid direct digital or synchronous demodulation. Instead, a modified Armstrong topology was used, as depicted in Figure 6-1. In this architecture a local oscillator (LO) multiplies the received radio signal to downshift it to a 10.7-MHz intermediate frequency (IF). Demodulation takes place at IF using a quadrature detector. A comparator converts the received signal to binary, and a field-programmable gate array (FPGA) performs deglitching and clock/data recovery. A microcontroller is used to synchronize the activities of many of the re-

ceiver components, and can reprogram the LO to track slow frequency shifts in the received RF signal.

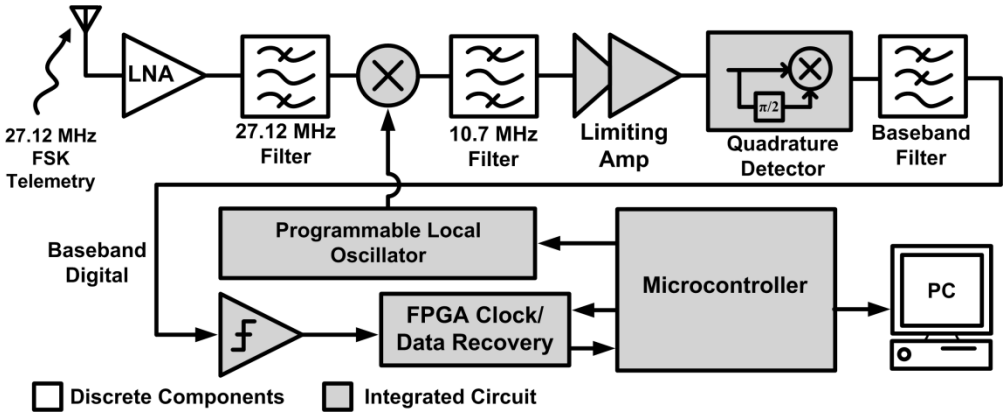


Figure 6-1. Block diagram of the WIMM system receiver and data recording backend.

6.1.1 *Receiver Antenna and Low-Noise Preamplifier*

The WIMM transmits data on the 27.12 MHz band to reduce the effects of tissue absorption and to permit the use of an inductive antenna [64]. The transmitting antenna is not an efficient E-field producer, but it does radiate a magnetic field whose strength drops off rapidly with distance. Flux lines of the radiated field can be captured by a loop antenna, causing current to flow into the RF preamplifier. The loop antenna for the WIMM was designed to work at a distance of 30 cm from the implant and be fairly intolerant to orientation. Because the WIMM inductive antenna produces a field aligned with the winding axis, the strongest field is received when the receiving and transmitting antennas are coaxially aligned. Multi-turn antennas can be more sensitive in this configuration but are potentially difficult to align with an implanted device. To sacrifice sensitivity for robustness, the receiver antenna was designed as a single turn loop as shown in Figure 6-2, which can capture radiated flux within a cone-shaped area up to

30° off-axis of the transmitting antenna. The loop antenna was constructed with semi-rigid coaxial cable, and a split was added in the outer shield. The center conductor is connected to form the loop antenna while the shield is grounded at both ends. The shield reduces the reception of FM-band signals on the loop antenna and prevents electrostatic drift.

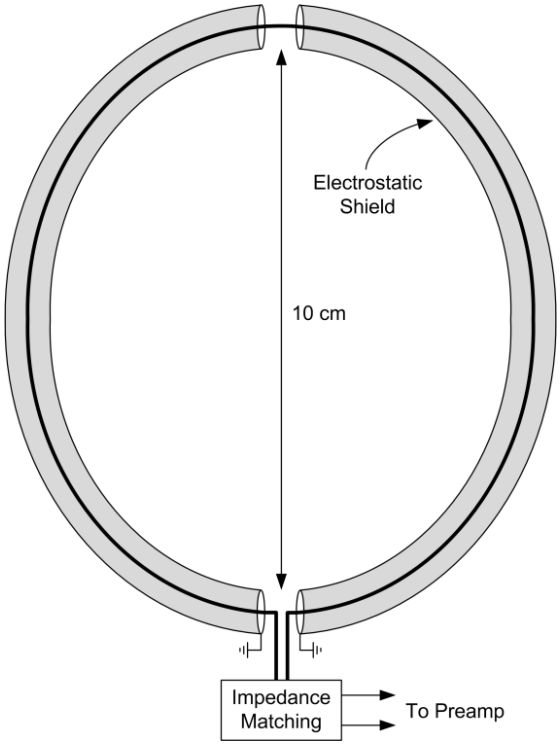


Figure 6-2. Illustration of the receiver antenna.

The front-end of the receiver is a low-noise amplifier (LNA) which is tuned to provide at least 30 dB gain in a 6-MHz bandwidth around 27 MHz as shown in Figure 6-3. This bandwidth is greater than what is needed to receive the WIMM FSK signal, but it permits simpler receiver tuning if the WIMM carrier frequency drifts due to environmental shifts near the implant. The receiver has a moderately low input-referred noise of 4.9 µVrms for an equivalent noise figure of 4.4 dB, due to wide bandwidth. The signal-to-noise ratio is improved after mixing to IF where

fixed, narrowband filters may be used. The preamplifier performance is summarized in Table 6-1.

TABLE 6-1.RECEIVER PREAMPLIFIER PERFORMANCE SUMMARY.

Gain (27 MHz)	34 dB
Bandwidth	6 MHz
Noise Figure (ref. to 50 ohm)	4.4 dB
Current Draw	12 mA

Because the LNA is paired with a custom antenna, 50-ohm matching is not required at the input. The LNA output, however, is matched to 50 ohms in order to drive standard RF filters and cables. The LNA input passive elements were tuned to resonance at 27.12 MHz with a band-width of about 6 MHz to present a high input impedance to the low-impedance antenna. This impedance mismatch does not produce optimum power transfer but maximizes voltage gain and provides basic frequency selectivity.

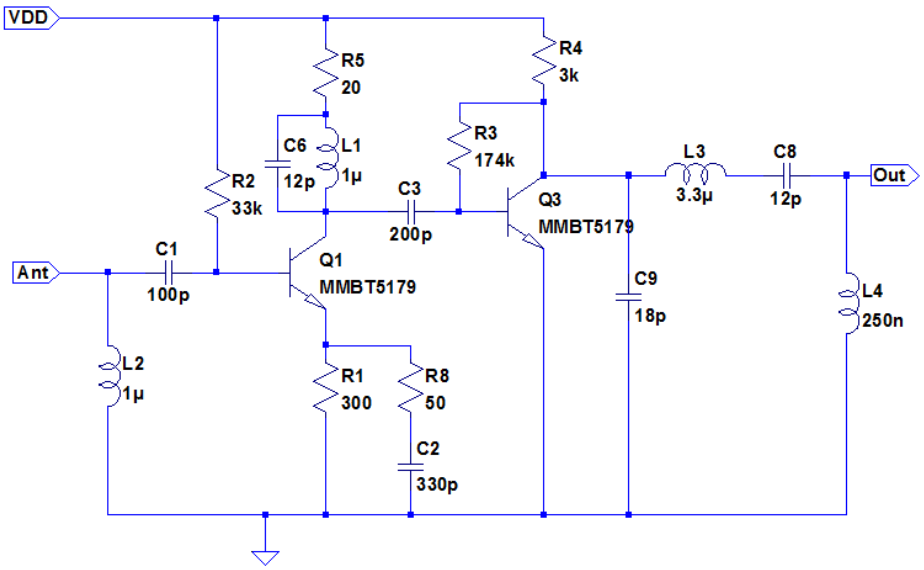


Figure 6-3. Receiver low-noise preamplifier schematic.

6.1.2 *Receiver IF Stage and Demodulation*

The IF stage of the receiver uses a wideband approach with a center frequency f_{IF} of 10.7 MHz. The wide bandwidth is required for accurate detection of the FSK signal, and it prevents the receiver from being sensitive to carrier drift. The IF mixer, limiting amplifier, and detector are all integrated within the NXP SA58641 IC. External components set the IF frequency response and 50-ohm matching at the IF input.

Demodulation of the FSK signal is performed using a multiplier configured as a quadrature detector as shown in Figure 6-4. This non-coherent demodulation method was chosen instead of conventional, more sensitive detectors such as phase-lock loops (PLLs) or Costas-architecture receivers because it does not require a lock-in period and is insensitive to absolute carrier frequency. Since the WIMM transmits intermittently on a center frequency that is prone to drift, a synchronous receiver would have to re-establish phase lock before each data packet is transmitted. At present, the WIMM transmits a fixed frequency for more than 400 µs before sending the data packet. This period is long enough to establish lock in a conventional PLL, but is wasteful of battery power. Future versions of the WIMM will transmit with a shorter lock-in time, forcing the use of a quadrature detector for demodulation.

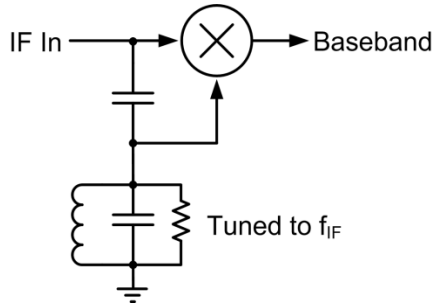


Figure 6-4. Schematic of the FSK demodulator.

For single-tone modulation at frequency ω_c, the quadrature detector output voltage is proportional to the phase difference ϕ between the two inputs as given by the identity

$$\cos(\omega_c t) \cdot \cos(\omega_c t + \varphi) = \frac{1}{2}\cos(2\omega_c t + \varphi) + \frac{1}{2}\cos(\varphi). \quad (1.14)$$

After conversion to IF, the received FSK signal has frequency components primarily at $f_{IF} \pm \Delta f$, where Δf is the frequency deviation of the modulated signal. An LC tank bandpass filter is placed on one of the detector inputs to generate an additional, frequency-dependent phase shift. Assuming the LC tank is tuned to resonance at f_{IF}, the phase response is approximately linear over the filter bandwidth of f_{IF}/Q, where Q is the quality factor of the LC tank. The LC tank Q was designed to be 20 for an effective phase detection bandwidth of 530 kHz. Since Δf is slightly greater than this bandwidth the instantaneous FSK frequency is additionally shifted by either 45° or 135° before reaching the detector, and this produces voltage shifts at the detector output corresponding to the transmitted binary data. Further filtering, amplification, and voltage limiting is used to finish the conversion to baseband digital data.

6.1.3 *Receiver Clock/Data Recovery and Decoding*

The serial bitstream which leaves the baseband processing electronics is a reconstruction of the transmitted packet, and a data clock is extracted from the NRZ bitstream using a high-speed FPGA and the code shown in Appendix 11.8. The FPGA mainly performs two functions—deglitching and clock recovery—using *a priori* knowledge of the approximate data rate much like RS-232 receivers. The WIMM data rate is 100 kilobits/second (kbps) but this can vary by +/- 25% due to chip variation, low battery voltages, etc. The clock recovery algorithm was thus designed to track long-term changes in the data rate, while still tolerating some timing jitter in the received bitstream.

Deglitching of the data is performed by a two-step process which filters out short and long glitches. First, the bitstream is oversampled with a 64 MHz clock such that all bits are over-sampled by 640. Short glitches in the bitstream are removed by a majority vote algorithm, which "averages" the last four samples of a bit and then rounds to the nearest binary digit according the formula

$$Z = AB + AC + AD + BC + BD + CD. \quad (1.15)$$

The short deglitching algorithm can remove glitches shorter than 31 ns without introducing much timing error to true bit edges. To remove longer glitches, the data is simply passed through a similar majority vote algorithm operating at a lower oversampling ratio of 16. This process removes glitches shorter than 625 ns while introducing a maximum timing jitter of about 6%.

After deglitching, a clock/data recovery (CDR) algorithm is used to resample the received data in order to properly clock out the packets to successive stages. Because the WIMM transmits intermittent packets with an RS-232 style start bit, the CDR begins from a "pause" state in which a positive data edge has not been detected in 8 recovered clock cycles. The recovered clock continues to run at a fixed frequency while the system is paused; the frequency is determined by a 9-bit SPEED register. When the start bit is detected, the CDR loads the SPEED register value into a counter, which is decremented every 31 ns until it reaches zero or another data edge is detected. If the counter underflows before the next data edge, the SPEED register is possibly set faster than the data rate, and is incremented for the next bit cycle. Alternatively, if a data edge occurs before the counter underflows, the SPEED register is decremented to speed up the recovered clock. The CDR algorithm resamples the received bitsteam by the recovered clock

such that the bitstream edges align with the falling edges of the recovered clock; the recovered clock rising edges are set when the clock counter reaches one-half of the SPEED register value.

6.1.4 *Receiver Performance Summary*

The as-designed performance of the WIMM receiver is summarized in Table 6-2. The IF bandwidth is determined by the limiting amplifier in the IF stage IC, but the IF and baseband bandwidths were designed for the WIMM transmitted data rate. Due to the large gain and fairly low noise figure, the receiver was expected to pick up transmissions from a WIMM at distances up to 30 cm.

TABLE 6-2. WIMM RECEIVER DESIGN SUMMARY

Input sensitivity	-100 dBm
Total gain	120 dB
Bandwidth (RF: 27 MHz)	10 MHz
Bandwidth (IF: 10.7 MHz)	2.2 MHz
Bandwidth (baseband)	130 kHz
Effective reception distance	30 cm

6.2 WIMM Wireless Recharger Design

The WIMM wireless recharger produces a very strong, directional magnetic field which is inductively coupled to the implanted WIMM. The WIMM ASIC extracts power from the radiated field to supply DC recharging current to the onboard battery. The field generator is implemented with the well-known Class-E amplifier topology, which was modified slightly to allow for

DC power control and envelope modulation of the power carrier. A simplified schematic of the wireless recharger is shown in Figure 6-5.

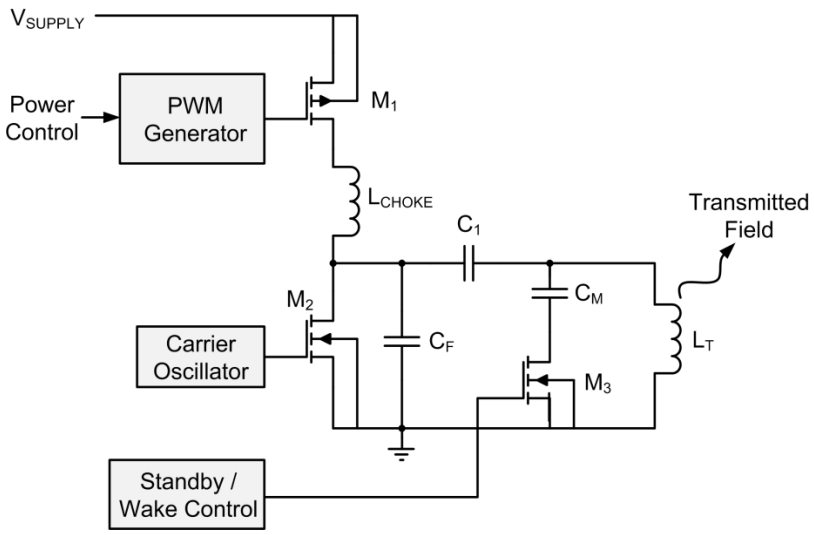


Figure 6-5. Schematic of the FSK class-E wireless power transmitter.

The Class-E circuit generates a large voltage in the transmitting antenna, L_T in order to produce a very large current and emitted magnetic field strength. Filter choke L_{CHOKE} is chosen to be large such that current flow into the circuit is essentially DC. FET M_2 is then switched at the carrier frequency ω_0 for the wireless recharge field. Capacitor C_F is chosen to limit the transient voltage spikes at the M_2 drain, while C_1 and L_T are tuned to resonance at ω_0. In steady-state, L_{CHOKE} carries approximately a constant current, and M_2 periodically shunts that current to ground. When M_2 turns off, L_{CHOKE} forces additional current to flow in the resonant load, which generates a large voltage across L_T.

The power coupling between the external recharger and internal implant can be expressed as a voltage gain if the coupled coils are treated as a loosely coupled transformer, as introduced in Section 1.5.4. For the chosen implant coil dimensions, and desired wireless re-

charge distance of 20 cm, the expected voltage gain of the recharging system is 16 mV/V. Since the voltage gain is so low, the class-E circuit was designed to produce at least 300 V_{AC} across the transmitting coil, from a 25-V DC power supply. The class-E output voltage amplitude is roughly a function of the quality factor of the resonant load and the size of filter inductor L_{CHOKE}. Coupling capacitor C_1 is a dipped-mica capacitor for low dissipation factor, while the transmitting inductor is formed from 7 turns of 18-AWG solid copper wire around a 15-cm diameter, as shown in Figure 6-6.

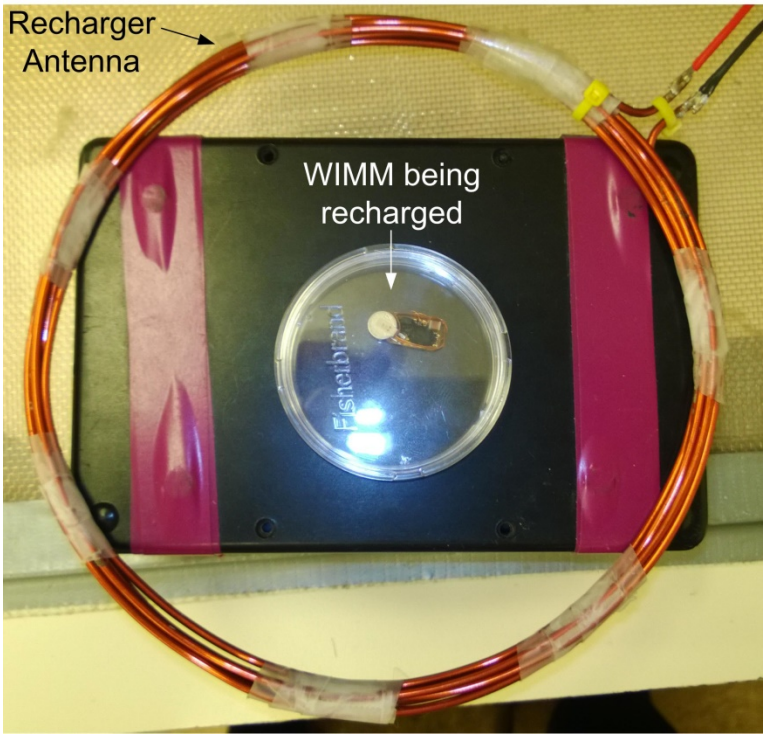


Figure 6-6. RF recharger antenna and WIMM for size reference.

The total output power of the recharger was designed to satisfy the power transfer requirements at a distance of 30 cm from the implant, but this level is too high when the implant

is closer. If the implanted device receives voltage greater than is required for battery recharge, a limiter circuit provides a small amount of over-voltage protection. However, if the received signal is too large, the WIMM ASIC could become damaged. The ASIC monitors the level of received power and transmits back a power status bit for closed-loop power control. If the power status bit is high, then the externally-transmitted power level can be reduced. In steady-state for this simple control scheme the power status bit should have a roughly 50% duty cycle as the transmitted power reaches the level for optimum power reception. Power control is implemented in the wireless recharger by FET M_1, which is driven by a pulse-width-modulated (PWM) signal. Filter L_{CHOKE} averages out the switching current, and the transmitted power is roughly proportional to the duty factor of the M_1 PWM.

The power control system implemented by M_1 provides roughly DC control over the transmitter power level due to the long time constant of L_{CHOKE}. The WIMM ASIC can be placed into a standby mode by transmitting a digital pattern during wireless recharge, which requires amplitude modulation of the recharge signal. The modulation speed requires rapid changes in the transmitted power level, so the circuit of C_M and M_3 was added to the recharger. When M_3 turns on, some current is instantly shunted from the resonant circuit while C_M further detunes the resonant transmitter. This effectively permits very rapid changes of the transmitted power envelope, and although it is not an efficient form of modulation, standby commands are very rarely sent to the device. Finally, the modulation depth can be adjusted by sizing CM and placing resistance in series with M_3. Values were chosen to provide a modulation depth of 20%.

CHAPTER 7

WIMM RECEIVER MEASURED RESULTS

The WIMM receiver was fully characterized by measuring the performance of individual stages, as well as the overall reception performance from a wireless WIMM. Because the base-band circuitry is based on well-known circuitry, most of the measurements were performed to validate the RF sections of the design. Unless otherwise noted, the receiver was tested with the WIMM development board with an antenna separation of 10 cm. A photo of the receiver is shown in Figure 7-1.

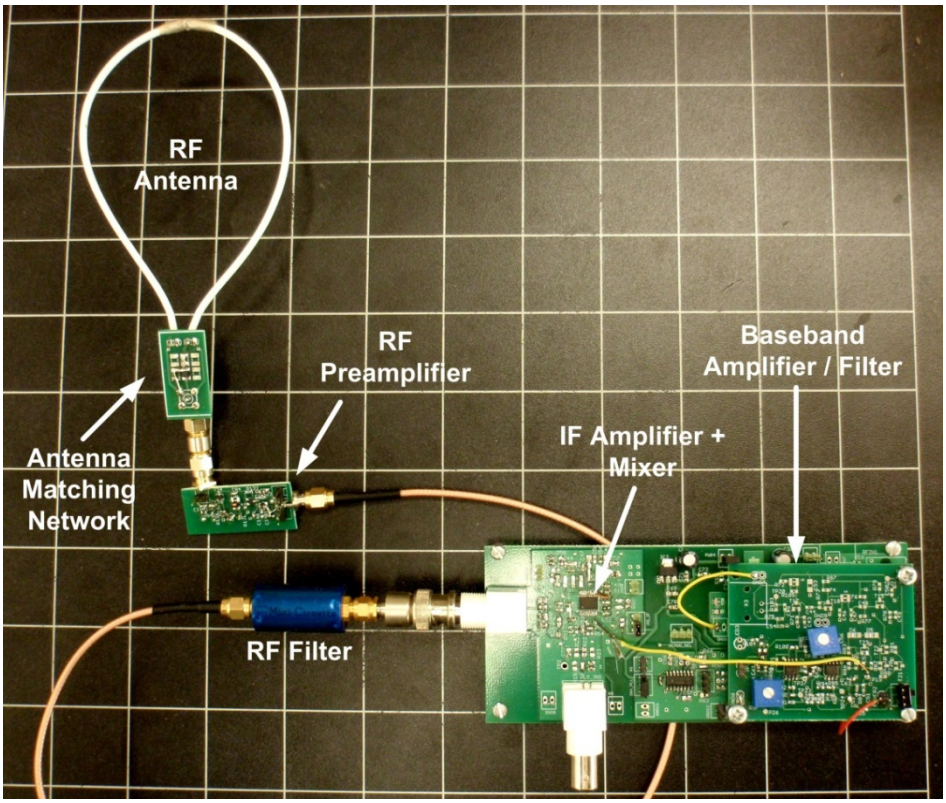
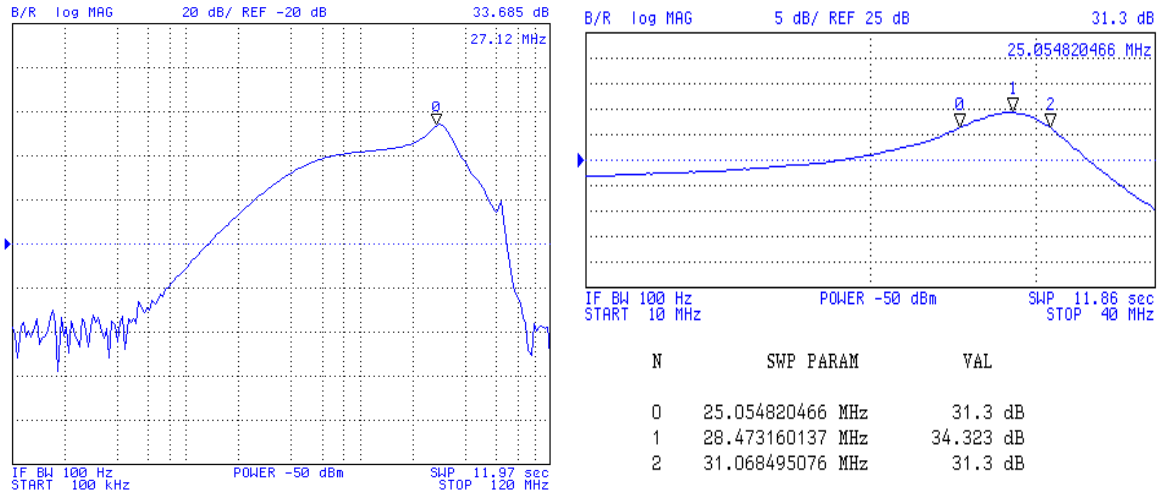


Figure 7-1. WIMM receiver RF and baseband components.

7.1 Preamplifier Characterization

The receiver preamplifier frequency response was measured with a network analyzer set to a source power of -50 dBm to prevent gain compression. To simplify the measurement the test signal was applied directly to the preamplifier input instead of through the antenna. Calibration was performed to account for impedance mismatch, and the preamplifier drove the 50-ohm analyzer input port directly. The measured frequency response is shown in Figure 7-2 and the preamplifier provided about 34 dB gain over a 6-MHz bandwidth. The measured frequency response does not account for the 2nd-order bandpass response of the tuned antenna, so in the actual implementation the preamplifier bandwidth will be narrower and centered on 27 MHz.



(a) (b)

Figure 7-2. Measured frequency response of the receiver preamplifier, (a) 10 – 100 MHz and (b) 3-dB bandwidth.

7.2 Clock/Data Recovery

The clock/data recovery performance of the receiver is largely based on the received signal strength (RSS) of the transmitted signal. The receiver adjusts the IF stage gain inversely proportional to the level of received power to prevent clipping of the high-gain IF amplifiers. When the RSS is below the detectable limit, the IF amplifiers use the maximum gain setting,

which increases harmonic distortion and represents a low signal-to-noise ratio at IF. Under this condition, the demodulated data contains glitches and the data edges are advanced/delayed, leading to data timing errors. The CDR circuits can deglitch the data, but if the jitter in the data timing exceeds about 25% of the nominal data rate it disrupts the clock recovery algorithm.

The receiver performance under with low RSS was measured by placing the receiver antenna at distances of 20-30 cm from the WIMM. An example data reception is shown in Figure 7-3 with a detailed view in Figure 7-4. The WIMM begins transmission with an unmodulated carrier tone to allow the receiver to calculate the RSS and adjust the IF gain. In the examples of Figure 7-3 and Figure 7-4, the received signal strength indicator (RSSI) increases slightly above the minimum detectable level, indicating moderate reception quality.

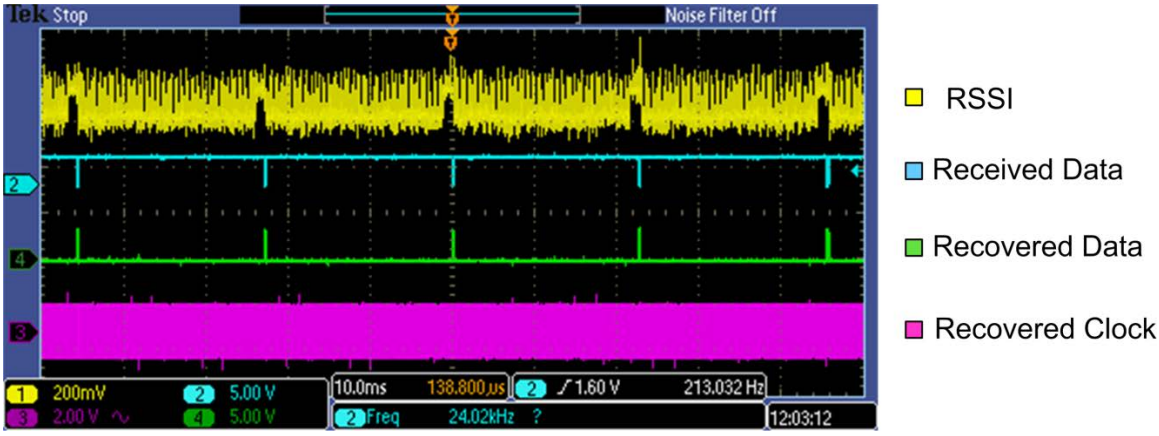


Figure 7-3. Example data reception from WIMM transmitting at 50 Hz. The increase in RSSI during receptions indicates that the receiver is applying automatic gain control.

Figure 7-4. Detail of packet reception by WIMM receiver. The recovered clock is derived from the received data.

The plotted received data is the demodulated bitstream after baseband filtering and level-shifting. The binary data is further processed by an FPGA, which recovers the clock from the data using an *a priori* assumption that the data rate is near 100 kilo-bits per second (kbps). The data is also processed and synchronized to the FPGA clock to filter out glitches which exceed the 100 kbps expected data rate.

7.3 Receiver Bit Error Rate

The bit-error-rate (BER) was measured by forcing the WIMM to transmit at 100 Hz and analyzing the packet headers for correctness while varying the transmit distance. The 6-bit packet header has 5 bits that are determinstic (4 framing bits and the sequential PRNG bit), while the remaining data is influenced by the pressure sensor and instrumentation circuitry. The FPGA which performs CDR also approximates the BER by measuring the time between corrupted header frames. Since each packet is 14 bits long and only 5 bits are analyzed the BER is estimated by

$$BER \approx \frac{5}{14} \cdot \frac{\tau_{TX}}{\tau_{ERR}}, \tag{1.16}$$

where τ_{TX} is the time between transmitted packets (nominally 10 ms) and τ_{ERR} is the time between header mismatch errors. In the example of Figure 7-3, the RSSI was sufficient to limit the BER to less than 10^{-5}.

The measured BER versus transmit distance is shown in Figure 7-5. The BER increased exponentially with transmission distance, and started to severely degrade when the WIMM was more than 50 cm from the receiver antenna. Even with the higher BER at 40-50 cm, the system could still be useful for general urodynamics because the data is oversampled and can be filtered to a much lower bandwidth. If the bit errors occur in the less important packet header, many uncorrupted pressure samples could still be received under high BER conditions. Finally, single-bit errors in the pressure data could be corrected by the decoder by analyzing the step height of successive samples; if the step height is greater than 32 ADC codes, for example, a single-bit error is the likely cause.

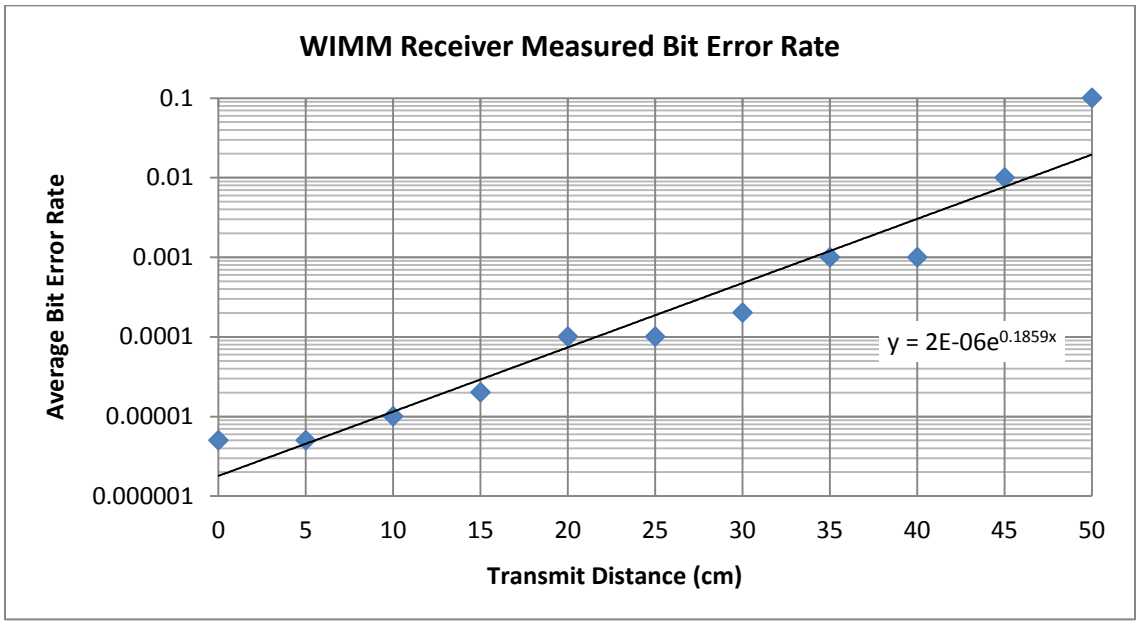


Figure 7-5. Measured BER versus distance for the WIMM receiver.

7.4 Measured Receiver Performance Summary

The overall performance of the WIMM receiver is satisfactory for wireless data reception at about 30 cm range. The architecture is fairly insensitive to carrier drift at the expense of sensitivity; nevertheless the receiver achieved an input sensitivity of -102 dBm. A performance summary of the WIMM system receiver is shown in Table 7-1.

TABLE 7-1. MEASURED RECEIVER PERFORMANCE SUMMARY

Input sensitivity	-103 dBm	
RF gain	34 dB	
IF gain	110 dB	
Baseband gain	10 dB	
RF Bandwidth	6 MHz	
IF Bandwidth	2.2 MHz	
Current draw (not including FPGA)	48 mA	
Effective reception distance	BER < 10^{-5}	18 cm
	BER < 10^{-3}	32 cm

7.5 External Recharger Measurements

The external recharger for the WIMM system was tested by coupling its transmitted power to the implant development board. The transmission power efficiency versus distance was measured by adjusting the recharger power supply voltage to the minimum level required to provide 200 μA of recharge current to the implant at various separation distances. The test was performed only under ideal coupling conditions in which the implant and external recharge coil were coaxially aligned. The measured power transfer efficiency versus distance is plotted in Fig-

ure 7-7. As expected, the power transfer efficiency is low at all distances due to small size of the implant recharge coil, but the implant battery could still be recharged at distances up to 20 cm despite an exponential drop in power transfer efficiency with distance.

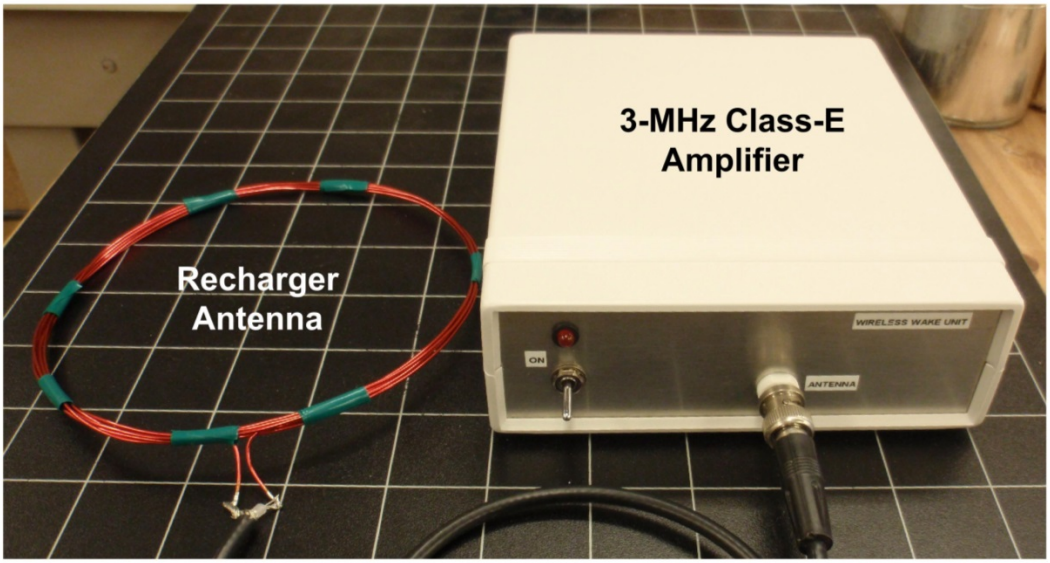


Figure 7-6. 3-MHz wireless recharger.

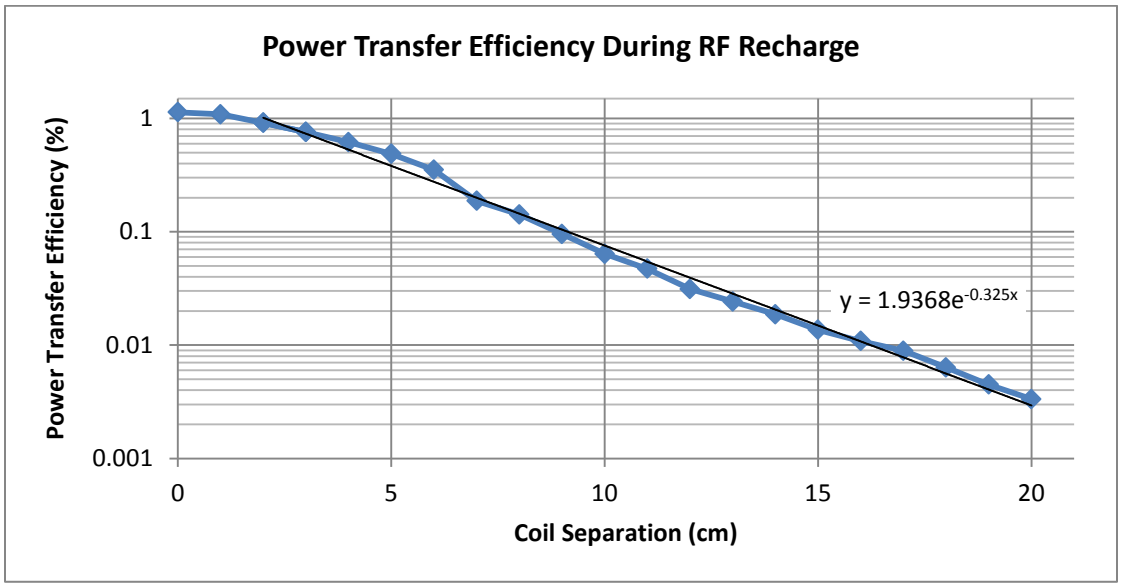


Figure 7-7. Measured wireless recharge efficiency versus coil separation distance.

Ultimately, the external recharge coil could be embedded in a pad which could be placed close to a patient's skin during wireless recharge periods. The class-E transmitter which produces the RF field is highly efficient, so most of the energy used is dissipated in the transmission coil and some is converted to heat due to the resistance of the coil windings. The recharge coil was insulated on one side by 15 mm dense of foam to provide padding and insulation similar to that needed in a clinical device. The temperature rise at the coil surface was measured using an infrared thermometer, as shown in Figure 7-8. The coil temperature reached a maximum of 17.1° C above ambient but no temperature rise was observed at the outer edge of the insulating foam.

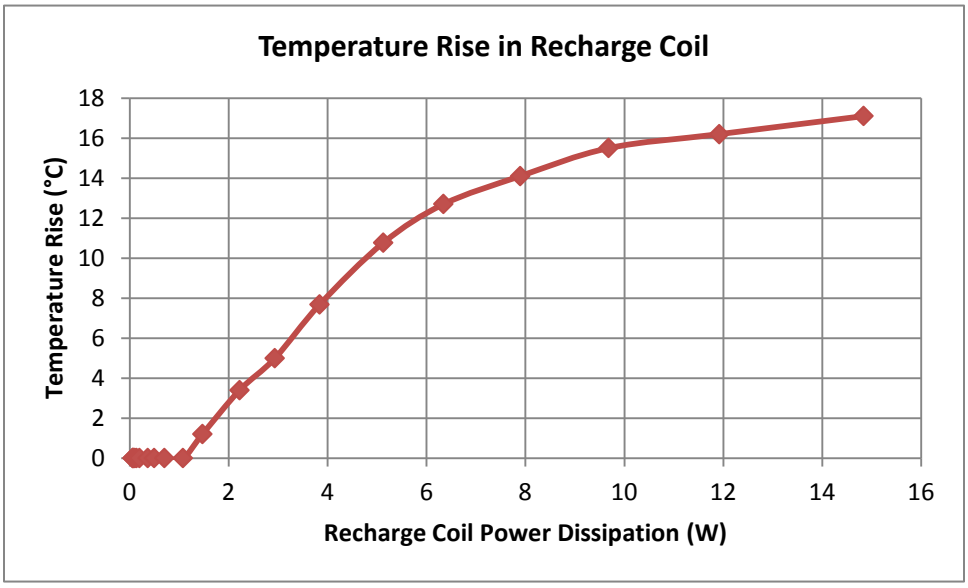


Figure 7-8. Measured temperature rise at the recharge coil surface when insulated by a foam pad.

CHAPTER 8

IMPLANT DESIGN AND ASSEMBLY

An implantable WIMM prototype was designed by combining the WIMM ASIC, a MEMS pressure sensor, a battery, and various passive components into a compact, waterproof package. A conceptual view of the component arrangement is shown in Figure 8-1. Generally, the implant was designed to be as narrow and thin as possible, so that it could fit through a urological cysto-scope.

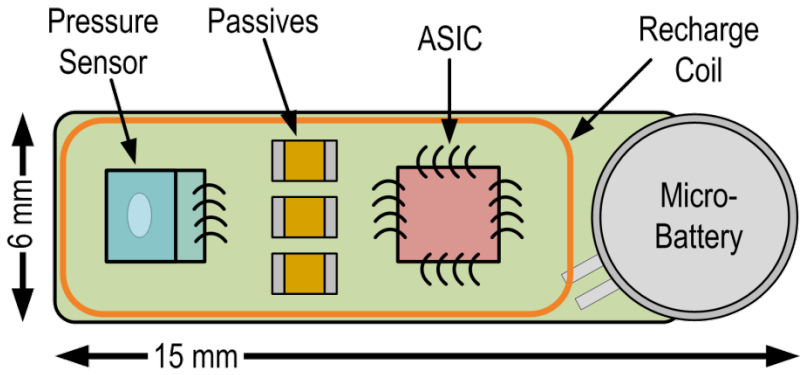


Figure 8-1. Schematic illustration of WIMM component arrangement.

8.1 Microsystem Design

The WIMM ASIC was designed for testability, not maximal integration, and so it requires a few external components and jumper connections. Different operation modes and features can be selected depending on the application for the device by wirebonding configuration pins to V_{DD} or GND. These configuration pins are not shown in the system schematic of Figure 8-2 for

simplicity. The external components of the microsystem are all capacitors used for supply bypass or tuning of RF circuits. Because the required values and operating voltages are low, all capacitors are 0201-size surface-mount devices (SMDs). This size was chosen as the smallest size component that can be soldered by hand.

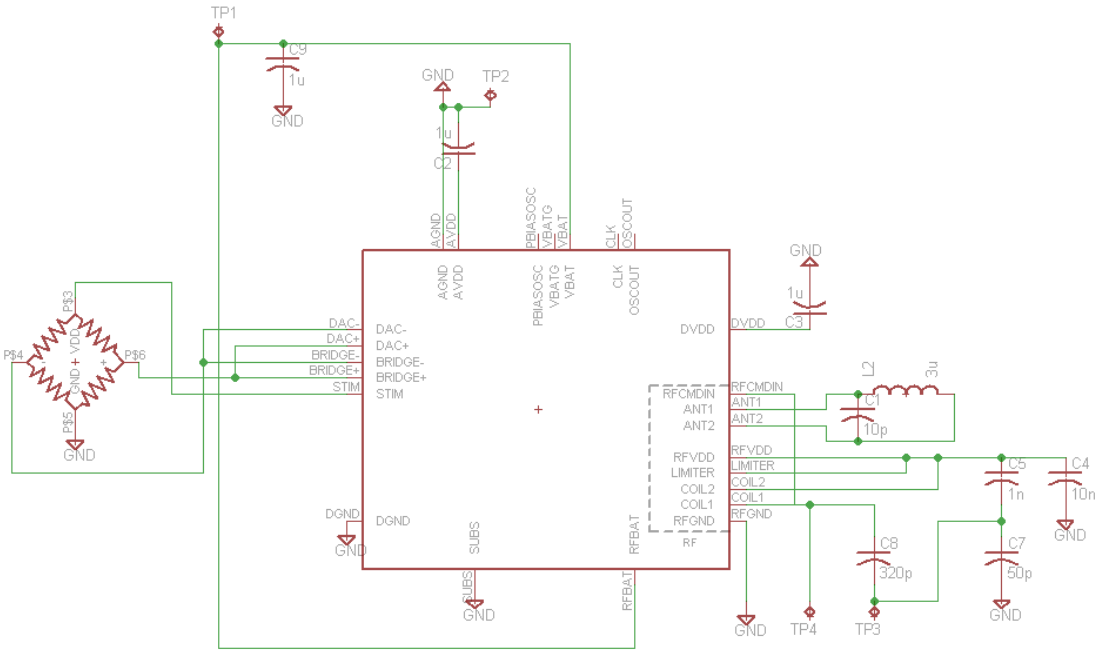


Figure 8-2. Schematic of the WIMM implant. Pin-programmable pins of the WIMM ASIC are not shown for clarity.

Inductor L2 functions as the transmitting antenna for the 27.12-MHz FSK transmitter, and C1 is chosen to tune the inductor to resonance. The inductor for RF recharge/standby control is not shown, but would be connected between TP3-4. Capacitor C8 is primarily used to tune the RF recharge coil to 3 MHz, while capacitors C4, C5, and C7 are used by the RF-DC rectifier circuit. Capacitors C2, C3, and C9 are not strictly necessary, but they enhance the stability of the system supply voltage, especially during RF recharge phases.

While implant-grade batteries such as the Quallion QL003I exist, they are difficult to obtain in the small quantities required for research. The main advantage of these high-quality batteries is a low internal resistance, high cell voltage, and low capacity degradation with recharge cycles. Cheaper watch batteries, however, are still capable of powering the WIMM, although they have lower operating voltages due to large internal resistances, and cannot tolerate more than a few hundred charge cycles. To simplify the construction of the WIMM prototype the Seiko MS621FE battery was selected due to its small size and wide availability.

8.2 Microsystem Layout

The core of the WIMM prototype is a thin printed circuit board (PCB) which provides electrical connections between components, as well as mechanical stability for the system. The PCB was designed so that all components fit on one side, but traces are plated on both sides. Key specifications for the PCB are listed in Table 8-1 with a PCB layout shown in Figure 8-3.

TABLE 8-1. PCB DETAILS FOR THE WIMM IMPLANT.

Attribute	Value
Thickness	0.5 mm
Trace spacing (min)	100 µm
Drilled hole size	250 µm
Surface finish	Electroless plated nickel, 250-nm immersion plated gold (ENIG)
Dimensions	17 x 6.7 mm including battery

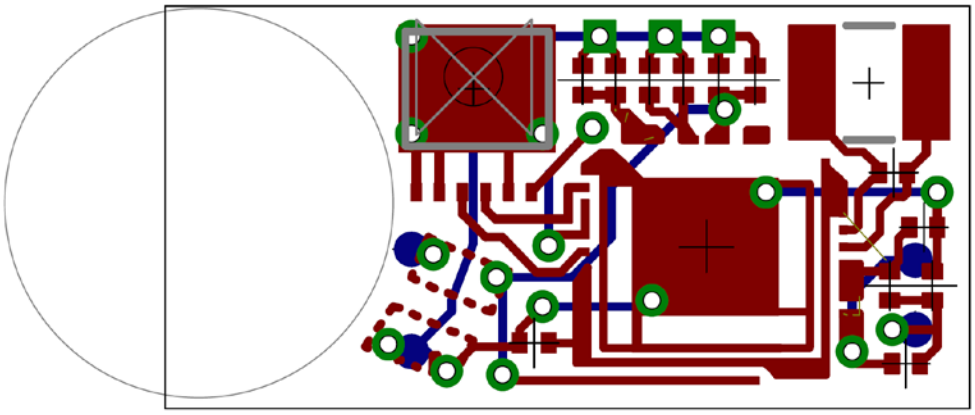


Figure 8-3. PCB layout for the implantable WIMM prototype.

The critical aspect of the PCB layout is the arrangement of the pads around the ASIC. The pads and VDD/GND rings were placed a minimum of 200 µm from the die edge to permit manual wirebonding.

8.3 Microsystem Assembly

Assembly of the WIMM implant prototype consisted of PCB preparation, die attachment and wirebonding, protective epoxy encapsulation, solder reflow, and manual soldering steps. First, the PCB was trimmed and sanded to its final dimensions using 1200 grit sandpaper. Next, the PCB was cleaned with DI water and acetone to remove surface contamination. The ASIC and pressure sensor were mounted using Crystalbond© die attach, which was applied at 80 degrees C on a hot plate. The ASIC was wirebonded using ultrasonic wedgebonding, in which the first wirebond was placed on the PCB and the second on the ASIC pad. This was necessary because of the height difference between the ASIC and the PCB traces. The pressure sensor was similarly wirebonded, but with the first wedge bonds being placed on the sensor to avoid collision between the bonder head and the sensor body.

Next, clear epoxy encapsulant (Loctite E-180NC) was applied to the wirebonds to protect them from accidental damage. The epoxy was allowed to partially cure at room temperature for 12 hours. Because the low-viscosity epoxy was applied without an encapsulation dam, some of the epoxy flowed onto the solder pads for other components and was mechanically scraped away. Solder reflow paste (Indium 8.9HF-1) was applied to the solder pads and components were hand-placed. The PCBs were next loaded into an oven and heated through the recommended solder reflow temperature profile.

At this stage, the PCBs were mostly functional and were quickly bench-tested by attaching power leads. Once functionality was verified, the RF-recharge coil was hand-soldered to the PCB backside along with the battery +/- terminal connections. The assembled microsystem prior to packaging is shown in Figure 8-4 with a US penny for size reference.

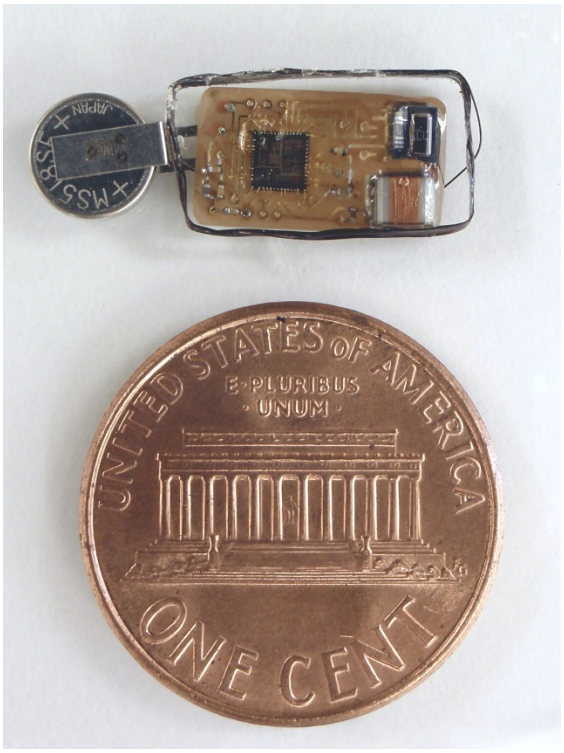


Figure 8-4. Photograph of the assembled WIMM prototype prior to encapsulation steps.

8.4 Microsystem Packaging

The microsystem packaging technique for the WIMM was evaluated on a number of early, wired prototypes which were tested in *in vivo* animal models for acute biocompatibility. For acute implantations, polydimethylsiloxane (PDMS), a liquid silicone rubber, is an acceptable vapor barrier with excellent biocompatibility and can be used as the sole encapsulation agent. Uncured PDMS is a poor void filler and provides no mechanical rigidity for the implantable device, so Dow Corning MDX-4210 was selected only as the outermost, biocompatible layer for the implantable device. Mechanical stability and additional dielectric insulation was provided by Hysol FP4650, an electronics-grade epoxy with high bulk resistivity, good void-filling characteristics, and low chemical out-gassing levels. The epoxy was used to coat and underfill all electronic

components, including the wirebonded ASIC and MEMS pressure sensor. A cross-section illustration of the encapsulated WIMM prototype is shown in Figure 8-5.

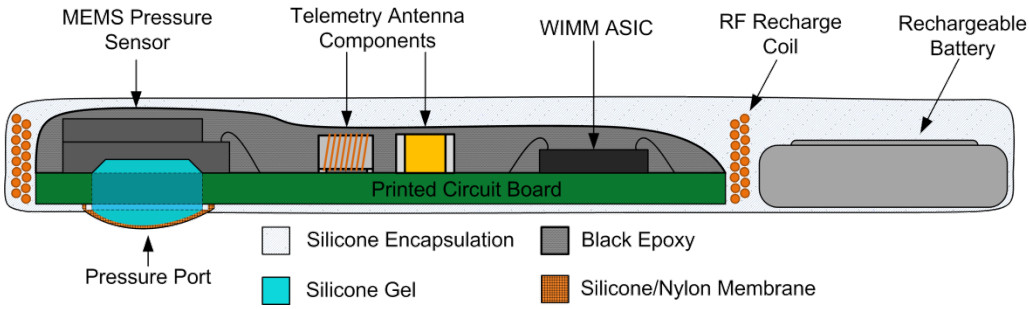


Figure 8-5. Cross section of the packaged WIMM designed for cystoscopic implantation.

8.4.1 *PDMS-compatible pressure transducer packaging*

The combination of epoxy and PDMS used to protect the electronics provides a mechanically robust platform, but a "pressure port" had to be created directly above the pressure transducer. This region was designed to be equally biocompatible and waterproof, but more compliant than the surrounding encapsulation. Pressure changes cause the compliant pressure port to deflect, transmitting pressure changes inside the encapsulated device while keeping biological media safely out of contact with the silicon pressure transducer. The outer PDMS encapsulant for the prototype does not stick well to non-silicones, so the materials used in the pressure transducer packaging were largely silicone-based to prevent weak bonding at the PDMS-port interface. An illustration of the pressure port construction process is shown in Figure 8-6.

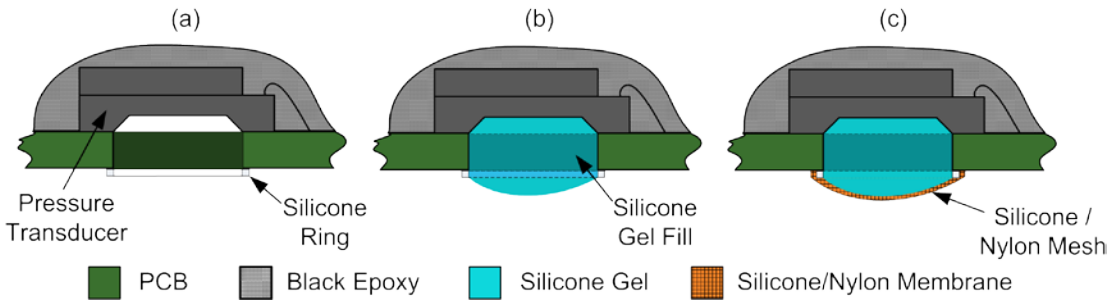


Figure 8-6. Illustration of construction process for compliant, all-PDMS pressure port in (a) - (c).

A backside pressure transducer was used so that the PCB material could provide structural integrity for the port structure. The port must be rigid in the plane parallel to the transducer diaphragm so that pressure changes are transmitted axially (perpendicular to the sensor diaphragm), thereby minimizing pressure attenuation. A ring of silicone tubing was attached opposite of the pressure transducer to form a 200-µm tall chimney as in Figure 8-6a. Next, the port cavity was filled with an incompressible silicone gel (Sylgard 527). The gel was overfilled to form a convex shape which further improved pressure sensitivity and reduced air bubble entrapment in further processing steps, as shown in Figure 8-6b.

The cured gel has a very soft durometer and must be protected to prevent tearing or displacement. Gel protection was achieved by creating a 50-µm thick, nylon-reinforced PDMS membrane. Without the nylon reinforcement, a pure PDMS membrane would be fragile and prone to tearing during surgical implantation. With nylon reinforcement, the PDMS membrane was significantly more durable, without sacrificing flexibility or attenuating pressure. After encapsulating the entire prototype with PDMS, PDMS-PDMS bonding was maintained near the pressure transducer, eliminating concerns over PDMS bond strength to dissimilar materials.

A photograph of the packaged WIMM prototype is shown in Figure 8-7. The implant was also tested with a cystoscope to ensure that it meets the size requirements imposed by this im-

plantation method. Figure 8-8 shows that the WIMM prototype can be inserted into the human bladder through the cystoscope sheath, as desired.

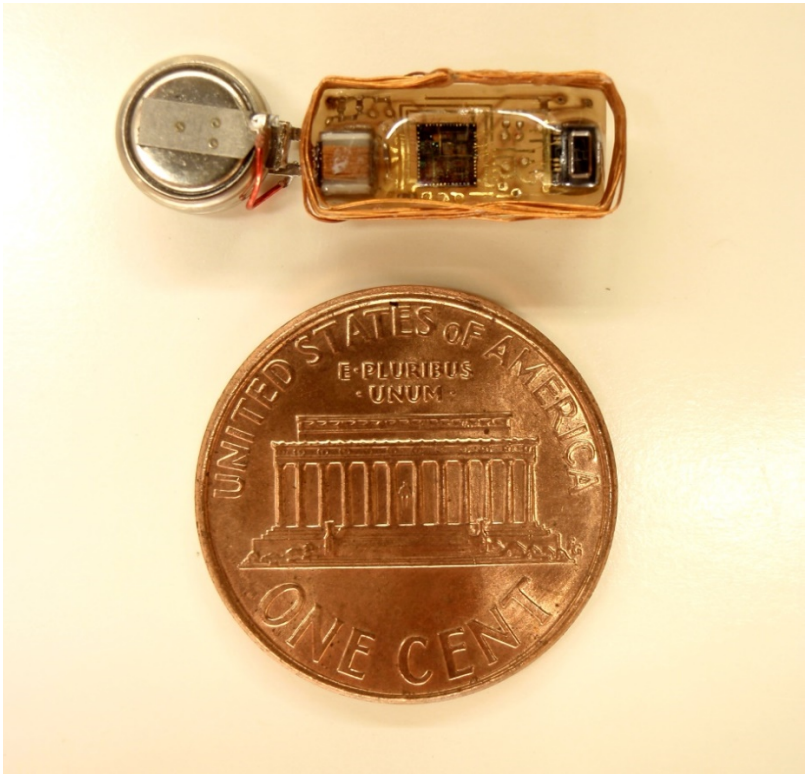


Figure 8-7. Prototype WIMM with US penny for size reference.

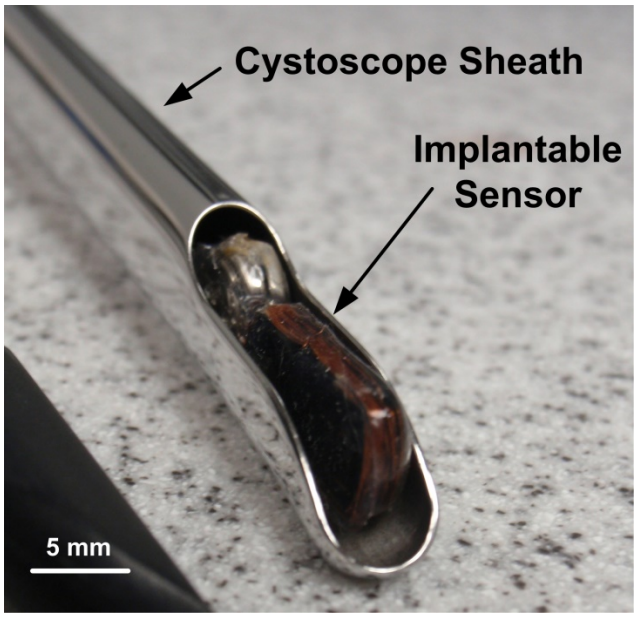


Figure 8-8. Packaged WIMM shown in distal end of cystoscope, next to sheath obturator for size reference.

CHAPTER 9

IMPLANT TEST RESULTS

The WIMM implant was fully bench tested to ensure proper function when used for *in vivo* experiments. After the unit is packaged it is not possible to directly measure the battery voltage, so a WIMM implant development board was designed. The development board measures 6.8 x 5.9 cm, is functionally equivalent to the WIMM implant, and is shown in Figure 9-1.

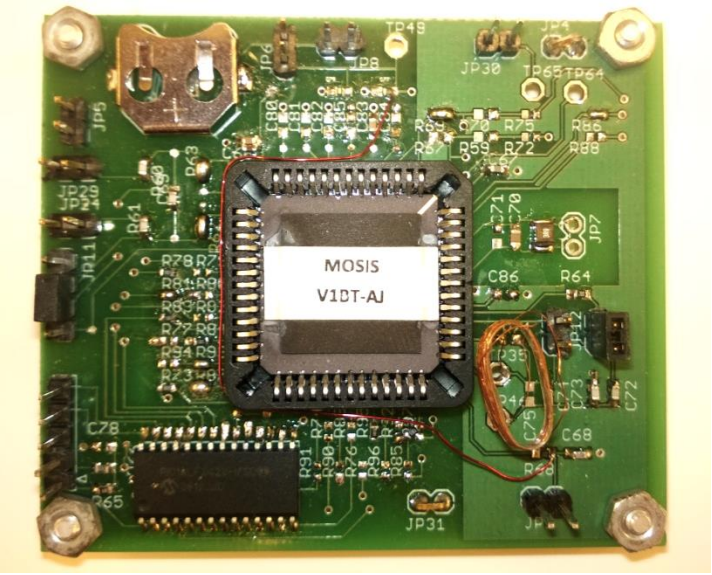


Figure 9-1. WIMM development board used for most wireless recharge tests.

The development board was primarily used to measure the efficacy of the RF recharge circuitry. Other wireless testing of the WIMM implant was performed with the implantable microsystem housed in a small pressure chamber for static and dynamic testing.

9.1 WIMM Implant Battery Charge Management

The battery status of the implantable WIMM can be quantified in two phases: discharging and charging. When the implant operates normally, the battery is discharged at roughly a linear rate, assuming low rates of pressure, and hence transmission, activity. This operational phase can be described by the implant operational lifespan, or the time it takes for the battery to discharge to a level which affects the system performance.

The WIMM ASIC requires V_{BAT} > 2.6 V to maintain saturation of the voltage regulator. When the linear regulator is not saturated V_{DD} simply tracks V_{BAT} with almost no voltage drop, and the ASIC can operate with V_{BAT} as low as 1.5V. However, the ADC performance is reduced with V_{BAT} < 2.1 V and the ASIC oscillator frequency varies slightly with supply. The operational lifetime specification for the WIMM implant was chosen as the length of time for the battery to discharge to 2.4V to provide some circuitry overhead.

The operational lifetime was measured using the development board so that battery voltage and system current draw could be monitored. The test was performed under pessimistic conditions in which the implant was programmed to transmit at a rate of 25 Hz. In a chronic implantation it is estimated that this rate is roughly 20X faster than the adaptive rate transmitter would otherwise choose. Furthermore, due to parasitic capacitance of the packaged ASIC, the power draw of the system was increased, with the development board drawing roughly 40 µA from the battery.

The development board was allowed to run for about 42 hours while the battery voltage (V_{BAT})was logged using a Labview DAQ system. A plot of V_{BAT} during this period is shown in Figure 9-2. For the first 18 hours, the external RF recharger was turned on, which recharged the

battery to its full level of about 3.4V. After 18 hours, the recharger was turned off and the system was allowed to discharge the battery naturally. After 24 hours of operation V_{BAT} remained above the cutoff of 2.4V, and the estimated lifetime of operation is about 60 hours before the system full-scale range becomes affected by low supply voltage.

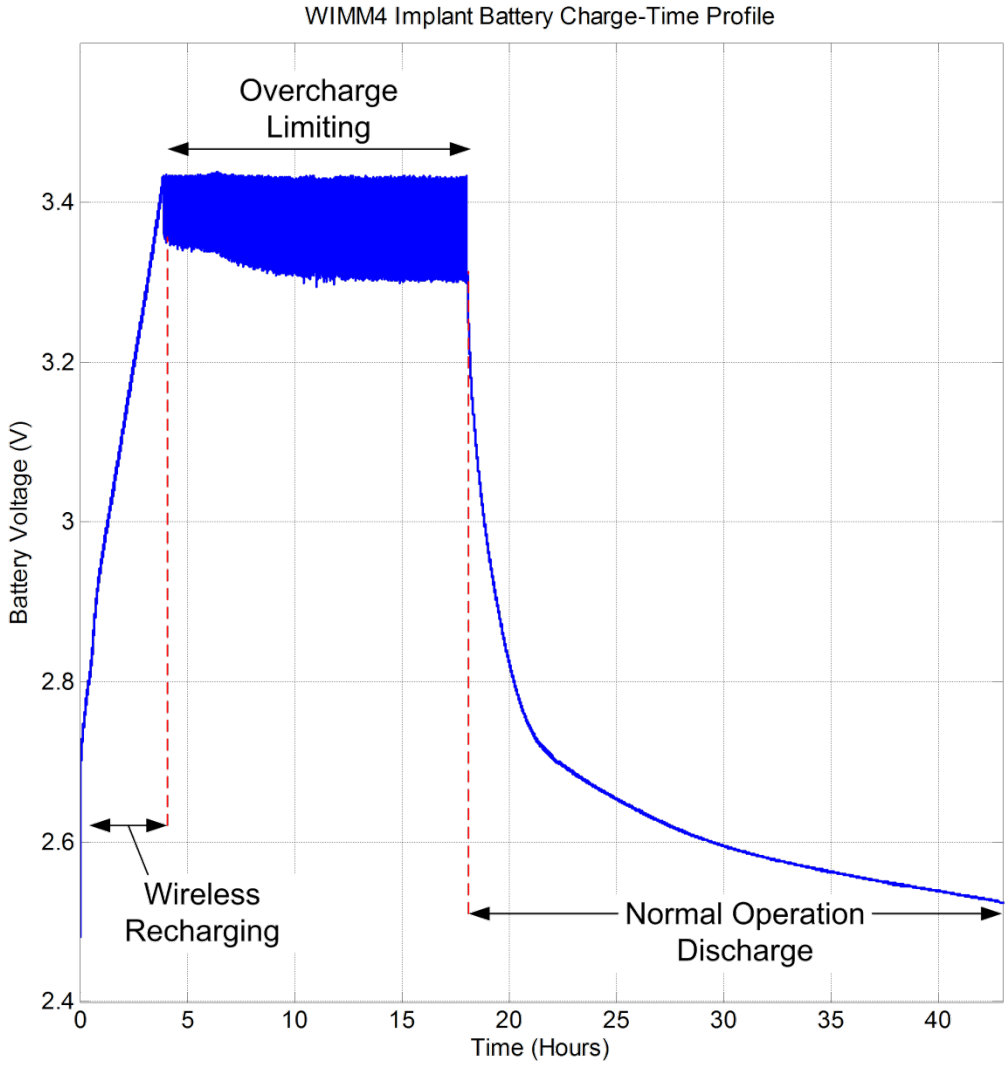


Figure 9-2. Measured WIMM battery voltage during recharge and normal operation.

During the recharge phase of the test the development board was placed 10 cm away from the recharge coil and wireless charging was performed with the recharger consuming 150 mA from a 25 V supply. The RF/DC recharge circuits on the WIMM ASIC rectified the received power and provided a 200 μA recharge current to the battery. Because the ASIC was still running, the net amount of recharge current was about 160 μA. The battery voltage increased during RF recharge until it hit a limit of about 3.4 V. Once the limit was reached the recharging circuits automatically stopped supplying current to prevent overcharge. Because the external recharger was left on for several more hours, the system entered a charge maintenance cycle of about 130 mV due to the built-in hysteresis in the battery overcharge circuitry, as shown in Figure 9-3.

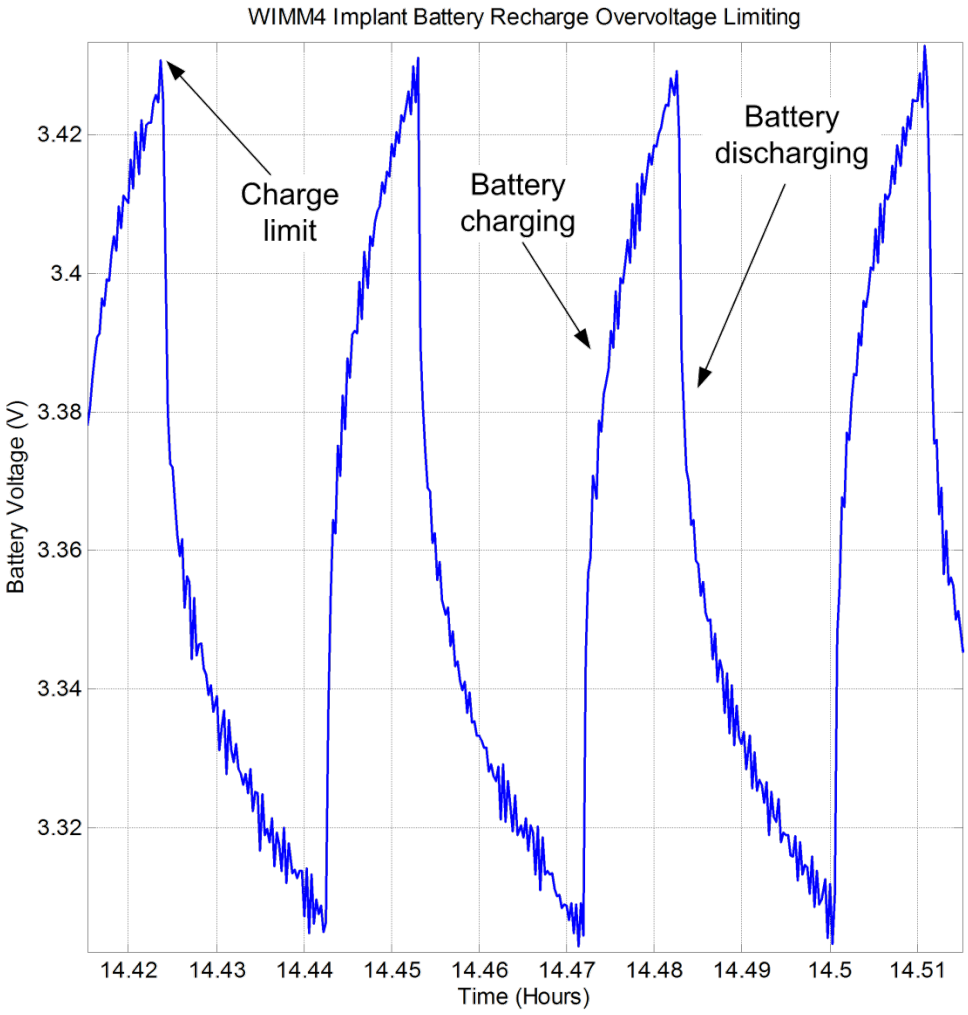


Figure 9-3. Measured hysteresis in battery overcharge limiting circuitry.

Finally, the system standby function was tested to ensure that the device could be placed into a very low power state to maintain battery charge when not in use. The RF recharge transmitter was modulated with about 50% depth to send the standby command to the device when placed 10 cm from the recharging coil. As shown in Figure 9-4, after receiving the standby command the WIMM internal regulator was disabled, effectively pausing the digital circuitry. Reactivation of the recharge field woke up the implant, which resumed normal operation. When in standby the ASIC drew about 60 nA, indicating a standby time in excess of one year.

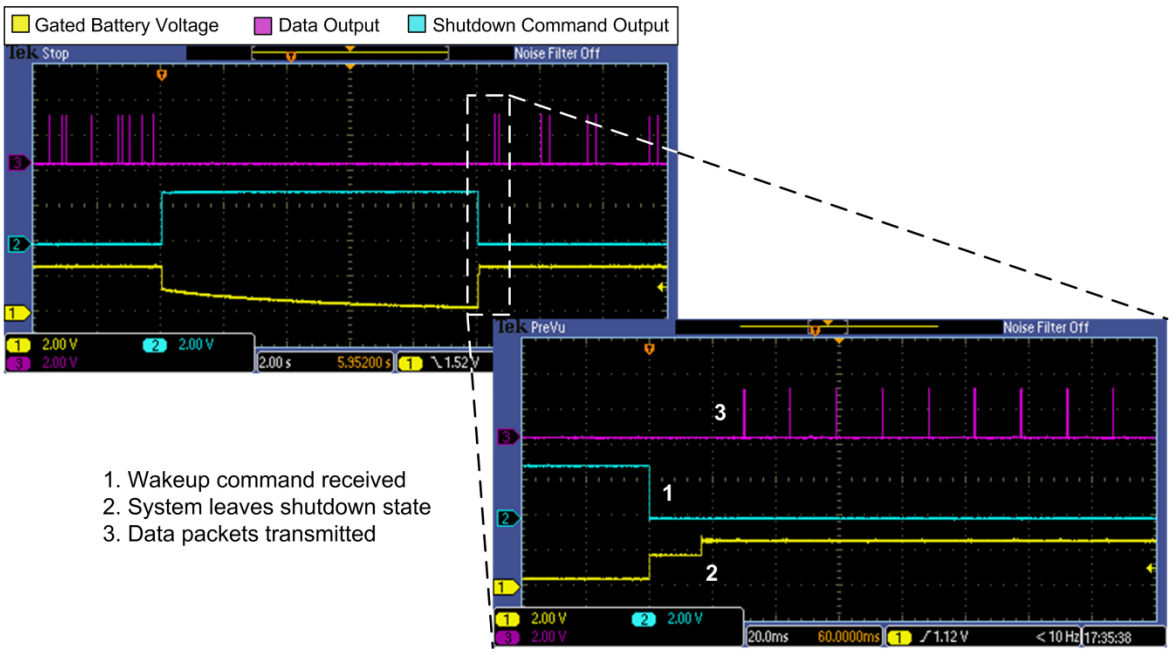


Figure 9-4. Measured ASIC power supply gating behavior during when entering and leaving standby mode.

9.2 WIMM Implant Pressure Sensitivity

To judge the impact of packaging on pressure sensor sensitivity, the WIMM implant was tested using static pressure sweeps before and after PDMS encapsulation. The device was loaded into a small pressure chamber with a commercial blood pressure sensor as a reference. The chamber was filled with air and a syringe pump was used to generate slow pressure changes. A Labview DAQ recorded correlated measurements of pressure and the received data from the WIMM prototype.

Although the WIMM implant was originally designed to work with the EPCOS C32 sensor, the implant was constructed with the Sensonor SW415 [57] sensor instead, as it was easier to procure in the volumes needed for future work. The SW415 sensor has greater bridge resistance, which reduces its power consumption, but also has reduced sensitivity and offset. Furthermore, because the offset removal system uses a current-mode IDAC, the increased bridge

resistance leads to increased input-referred IDAC thermal noise, an increase in the offset removal system loop gain, and an increase in the level of fixed offset removal. The WIMM removes 240 mV of offset with the 12-kΩ resistance of the SW415, which is about three times larger than the atmospheric offset of the part.

To counteract the effects of the larger fixed offset, the pressure sensor was connected as shown in Figure 9-5 to halve the amount of removed offset. This arrangement produces nominally zero atmospheric offset with R_0=47 kΩ, and the automatic removal system removes any residual offset due to manufacturing tolerances. While the offset removal IDAC current is increased threefold by the larger sensor resistance, since only one IDAC output is used the offset removal dynamic range is about 1,450 cm H_2O. Moreover, using only half of the IDAC output removes the benefits of common-mode noise rejection, and the equivalent level of IDAC noise is further increased by a factor of 3 due to the mismatch in C32 and SW415 bridge resistances. When referred to the ADC output at the largest INA gain setting, the IDAC produces about +/- 15 codes of Gaussian noise. The filter capacitor C_0 was added to reduce the IDAC noise bandwidth at the cost of settling time and a loss of sensitivity. A value of 22 nF was chosen to strike a balance between pressure sensitivity and noise reduction.

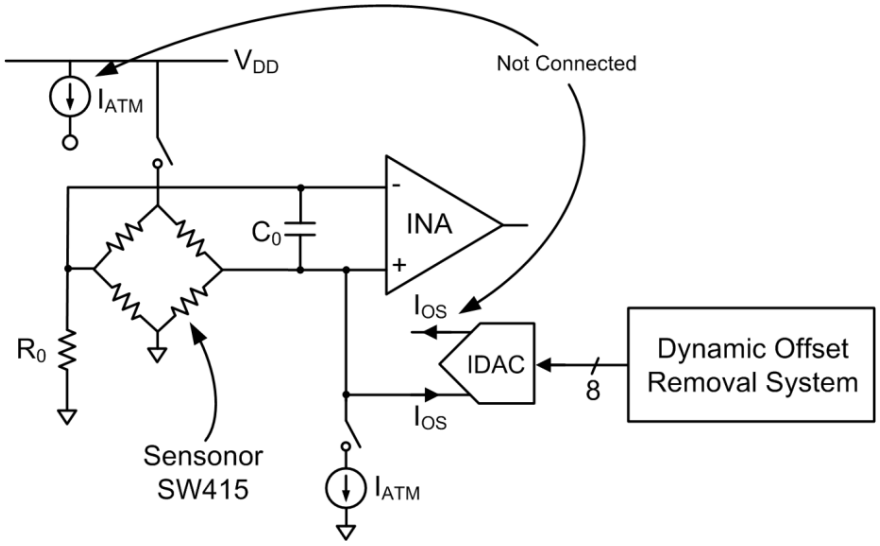


Figure 9-5. Updated connections to the offset removal system for the SW415 sensor.

The measured WIMM pressure response is shown in Figure 9-6. The data was collected with the wireless WIMM in an air-filled pressure chamber which was pressurized to 0 – 200 cm H_2O above atmospheric pressure. The measurements were performed fairly quickly to minimize the effect of the auto-offset removal system; however, the offset system changed the sensor offset about 3 times per measurement. The collected values were corrected for offset by applying an average offset removal of 15 ADC codes/IDAC code to linearize the collected data.

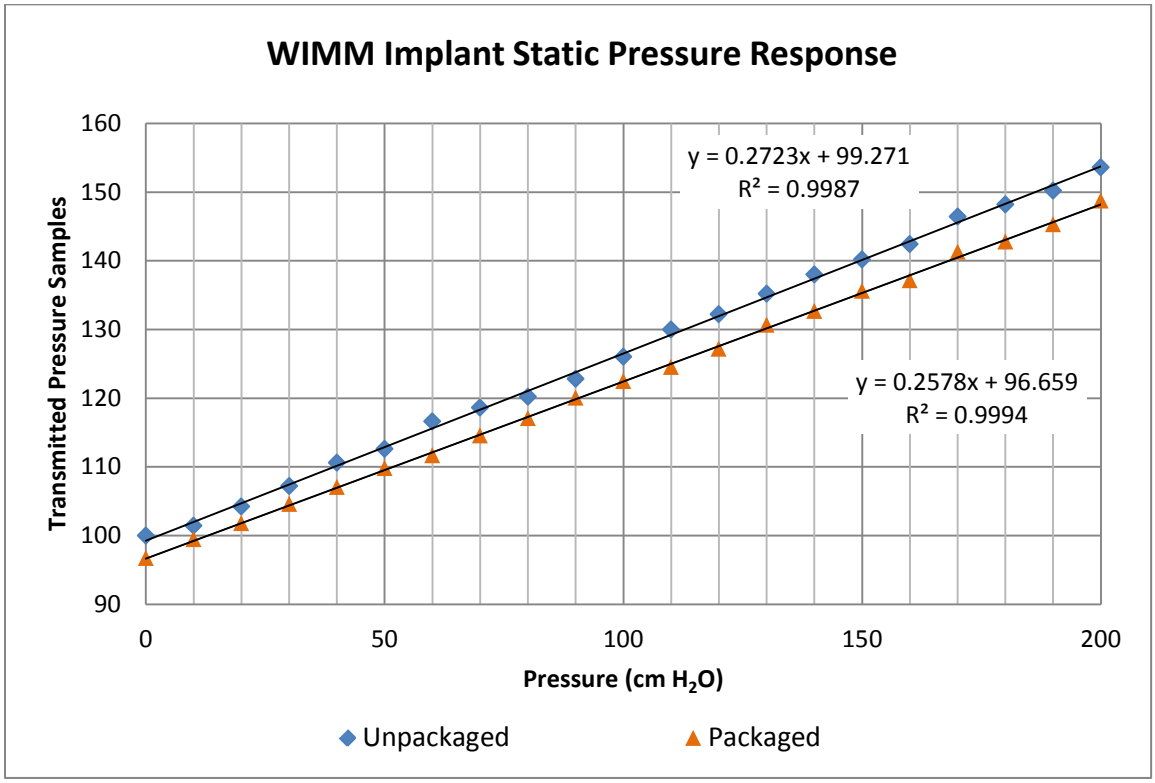


Figure 9-6. Measured WIMM pressure sensing response for packaged and unpackaged sensors.

A summary of the static pressure sensing performance is shown in Table 9-1. A linear fit was performed on the measured data and error was calculated using the differences between the fitted and measured points, normalized to the full-scale range of 200 cm H_2O. Overall, the packaging had little effect on the pressure sensor performance, and the loss of sensitivity due to packaging was about 5.4%. The standard deviation of the noise was less than 1 percent of full-scale at a 15-Hz bandwidth for both packaged and unpackaged sensors, although the measured pressure sensitivity was fairly low. However, since pressure samples are transmitted at 100 Hz, it would be possible to increase the effective sensitivity and to reduce the noise by decimating the received samples by a factor of 4 or more.

TABLE 9-1. WIMM IMPLANT PRESSURE SENSING PERFORMANCE SUMMARY.

Parameter	Unpackaged	Packaged
Average Sensitivity	3.7 cm H_2O / code	3.9 cm H_2O / code
Noise Standard Deviation (50 Hz bandwidth)	2.3 cm H_2O	2.4 cm H_2O
Noise Standard Deviation (15 Hz bandwidth)	1.8 cm H_2O	1.8 cm H_2O
Average Fitted Error	0.26 %	0.21 %
Maximum Fitted Error	0.50 %	0.43 %

9.3 WIMM Implant in Vivo *Trials*

The WIMM was tested in four *in vivo* animal trials. The first three trials proved the feasibility of the ASIC-based implant and implantation method, while the final trial investigated the complications associated with a minimally-invasive implantation procedure. A total of four animal experiments were performed, as summarized in Table 9-2.

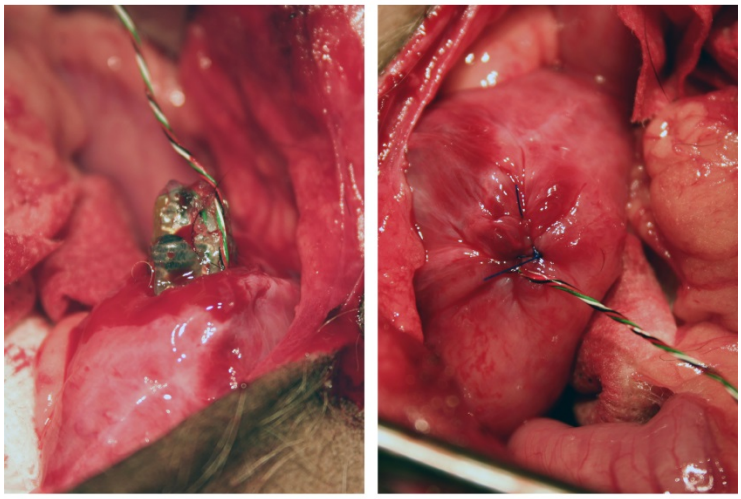
TABLE 9-2. SUMMARY OF *IN VIVO* ANIMAL TRIALS USED TO VALIDATE WIMM FEASIBILITY.

Trial	Model	Animal condition	Duration	Implant details
1	Feline	Anesthetized, non-survival	< 8 hours	Submucosal in bladder lumen, implanted via transverse incision, leads exposed in pelvic cavity
2	Canine			
3	Canine	Ambulatory, survival	10 days	Submucosal in bladder lumen, implanted via transverse incision, leads tunneled to transcutaneous port at animal shoulder
4	Calf	Anesthetized, non-survival	< 8 hours	Submucosal in bladder lumen, implanted via cystoscope, wireless

9.3.1 *Wired Implant Trials*

Early versions of the WIMM device were wired due to the chosen implantation method and to limit experimental risk. In the first three animal trials, the WIMM device was implanted submucosally through a transverse incision of the bladder detrusor. The power/data cable exited through the incision, and the bladder was sutured shut to allow for urodynamics testing. In

Trials 1 and 2, the pelvic cavity was left exposed so that manual- and electrical-induced bladder contractions could be performed. In Trial 3, the power/data cable was tunneled subcutaneously to an exit site near the animal shoulder, the surgical cavity was sutured, and the animal was allowed to heal naturally. A photo of the implanted WIMM from Trial 2 is shown in Figure 9-7 below.



a. b.

Figure 9-7. (a) View of WIMM partially implanted within canine bladder and (b) the fully implanted WIMM with power/data cable leaving sutured detrusor muscle.

The WIMM performed satisfactorily through all animal trials, although some complications related to surgical techniques and animal handling only permitted data recording in fairly short windows. The WIMM transmitted wireless data in all animal trials, but only the power-spectrum was captured, as shown in Figure 9-8a. Recorded pressure data came solely from the wired connection. Bladder contractions were captured in all animal trials, and the WIMM recordings generally correlated well with reference lumen pressure recordings. Differences in the recorded signals were attributed to the device implant location beneath the mucosa, rather than in the bladder lumen. Air bubbles trapped between the pressure port and mucosa, or the

compressive action of the detrusor muscle might explain these discrepancies. A sample bladder contraction recorded by the WIMM in an anesthetized canine is shown in Figure 9-8b. The recorded signal was post-processed by filtering and applying a gain correction that was calibrated before the experiment began.

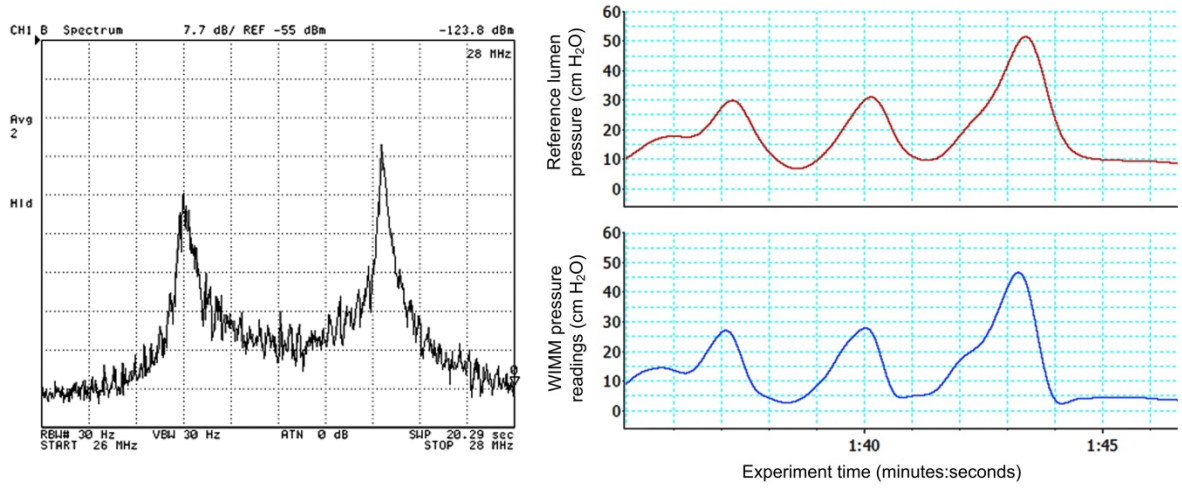


Figure 9-8. (a) Recorded power spectrum of 27.12-MHz FSK transmission from WIMM implanted in canine bladder and (b) bladder contractions recorded by the WIMM from a submucosal implant location.

Correlation coefficients between the implanted device and a reference lumen catheter were calculated to ensure that the device was accurately capturing vesical pressures. In the first animal trial, the device was only tested positionally—implanted within the bladder lumen—and significant correlation was observed. In the second trial, because of the observed pressure drops, only moderate positional correlation was observed. However, when the device was explanted and placed directly in the bladder lumen, good correlation between the device and the reference was observed, indicating proper function. Finally, in the ambulatory trial, positional correlations were not obtained because the animal did not tolerate an indwelling catheter. During necropsy the device was explanted and placed in the bladder lumen, and high correlation to the reference was observed. The extracted coefficients are summarized in Table 9-3.

TABLE 9-3. SUMMARY OF *IN VIVO* ANIMAL TRIALS USED TO VALIDATE WIMM FEASIBILITY.

Trial	Model	Average Correlation Coefficient	
		Submucosal	Intraluminal
1	Anesthetized Feline	0.994 +/- 0.003	-
2	Anesthetized Canine	0.893 +/- 0.032	0.983
3	Ambulatory Canine	-	0.971

9.3.2 *Wireless Implant Trials*

A functional WIMM was implanted cystoscopically into a female calf for the final validation experiment. The device functioned electronically, but due to a processing error during packaging, liquid epoxy flowed onto the pressure sensor diaphragm, freezing it in place. Consequently, the device did not have any pressure sensitivity and continually transmitted a fixed pressure reading. Regardless, the device was successfully implanted in the bladder, thereby confirming that the dimensions are appropriate for cystoscopic implantation. An image of the implanted WIMM was captured with a transverse CT fluoroscopy scan of the animal midsection, as shown in Figure 9-9.

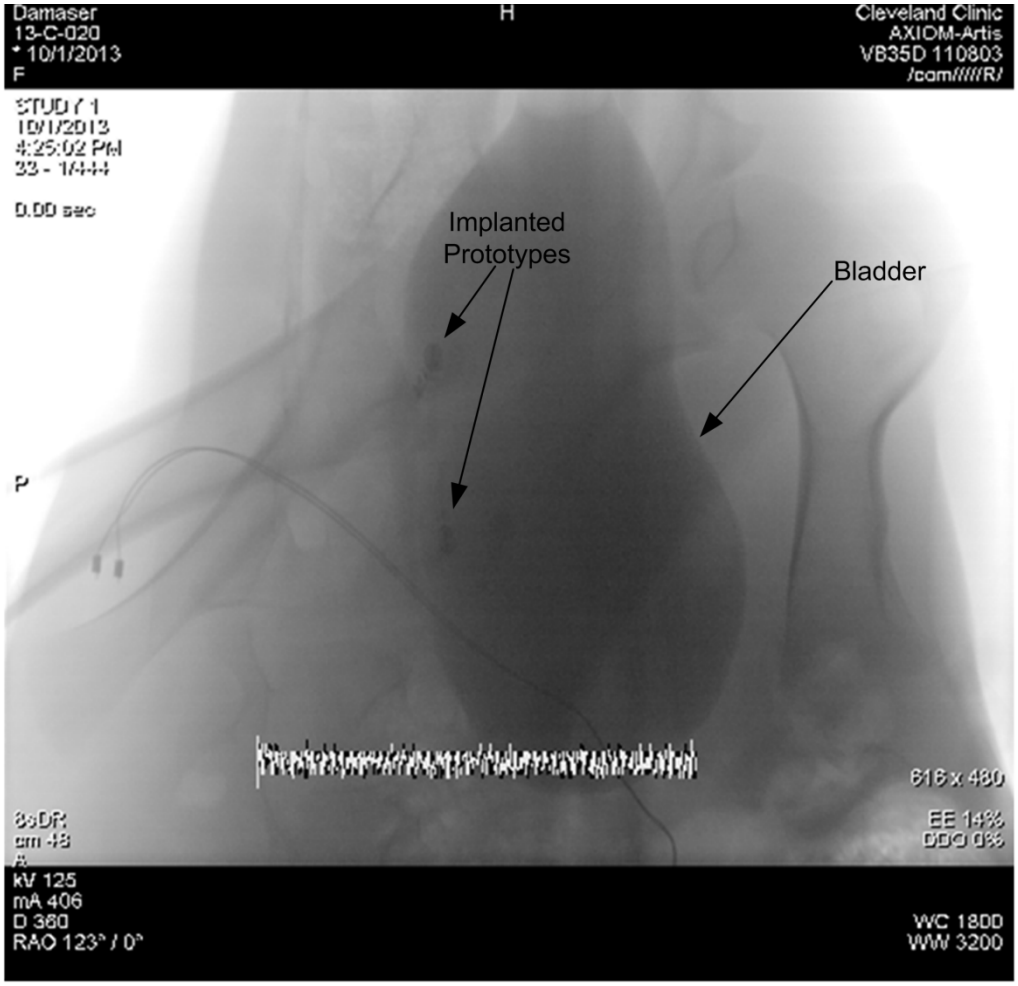


Figure 9-9. CT scan of WIMM prototypes cystoscopically implanted in a female calf bladder.

CHAPTER 10

CONCLUSIONS AND FUTURE WORK

This research has demonstrated the feasibility of a wireless, implantable pressure sensor suitable for chronic bladder pressure measurement in humans. The wireless implantable micro-manometer (WIMM) dimensions were chosen to allow for cystoscopic implantation into a suburothelial location within the bladder lumen, where the sensor is shielded from the urine stream, preventing stone formation and permitting chronic use. Unlike previously described implantable pressure sensors, which were RF-powered or provided sub-Hz sample rates to save energy, the WIMM is battery-powered to maximize patient mobility and provides 100-Hz sample rates to enable conditional neuromodulation or ambulatory urodynamics. The implant battery is recharged wirelessly using a coil antenna which may be integrated into a mattress or other cushion to provide unobtrusive charging during periods of patient rest.

To maintain a small implant size, and to achieve the low levels of power consumption required by an implantable device, a custom ASIC was designed for the WIMM. The ASIC integrates instrumentation, power management, and RF telemetry circuitry on a 6 mm^2 die using a 0.5-µm CMOS process. Low-power operation at a 100-Hz pressure sampling rate is provided by a novel circuit architecture in which a power management unit dynamically switches circuitry off when it is no longer needed. An adaptive rate transmitter further reduces the ASIC power consumption by calculating an appropriate transmission rate based on the level of pressure activity, for an average ASIC current draw of approximately 15 – 75 uA for 1.5 – 100 Hz data transmission

rates. An automatic offset-removal system digitally calculates the offset of the pressure sensor and subtracts it using a bipolar 8-bit IDAC, extending the system dynamic range to 2,200 cm H_2O with an effective high-pass response of about 3 mHz. An RF voltage doubler rectifier converts received magnetic energy into a DC voltage, and battery recharge circuitry provides constant-current recharge and battery overcharge protection.

The ASIC was combined with a commercial piezoresistive pressure sensor, RF recharge antenna, micro-battery, and other passive components to form an implantable system capable of insertion through a conventional urologic cystoscope. Traditional metal/glass encapsulation was not used to avoid RF shielding effects and to reduce the overall implant assembly cost. Instead, the implant was encapsulated using non-hermetic, biocompatible polymers. Electrical epoxy was used to fill voids and to provide structural strength for the implant, while the area near the pressure sensor diaphragm was filled with silicone gel to provide a void-free but compliant area. A thin silicone/nylon mesh membrane was cast and glued above the silicone gel for abrasion resistance. Finally, the implant was coated in medical-grade PDMS to guarantee biocompatibility and to prevent water ingress. Bench-testing of the implant confirmed the low-power operation, with an expected lifespan of 60 hours per battery charge. Wired prototype implants were tested in several animal models, and recorded bladder pressure correlated well with intraluminal catheter reference measurements ($r = 0.893 – 0.994$).

An external RF receiver/recharger was designed to implement a clinical WIMM system capable of maintaining an implanted sensor. The high-gain RF receiver used an Armstrong topology to receive FSK-modulated pressure telemetry at 27.12 MHz, and had a low noise figure of 4.4 dB for an input sensitivity of -103 dBm. Because the WIMM transmits intermittently and semi-randomly, an open-loop quadrature demodulator was used to allow for a fast transient re-

sponse over closed loop demodulators such as PLLs. The receiver provided adequate fidelity to maintain a bit-error-rate greater than 10^{-3} at reception distances beyond 30 cm. The RF battery recharger was implemented using a tuned Class-E amplifier capable of generating > 300 V_{RMS} across a 6-turn, 15-cm diameter loop antenna. While the RF recharge efficiency at large separation distances was low, the WIMM was successfully recharged at up to 20 cm distance while dissipating 15 W of power in the recharger circuit.

10.1 Future Work

This research proved the feasibility of creating an implantable bladder pressure sensor system, but future studies should address the long-term stability of the implant, such as aging of the micro-battery over repeated charge/discharge cycles or the change in pressure sensitivity with time. Furthermore, the packaging method developed here was only validated in acute animal studies; long-term implantations in greater numbers will be required to prove the biocompatibility and impermeability of the encapsulation. Further refinement of the external components of the system—the RF receiver and wireless recharger—can improve the performance and reliability, especially if they are used clinically. Full integration of the recording apparatus with the RF receiver could be pursued by integrating the demodulating FPGA circuitry with a solid-state storage solution (i.e. SD card) to achieve a wearable bladder pressure recorder for ambulatory urodynamics.

Ultimately, the performance of the WIMM system is determined by the accuracy and low power consumption of the WIMM ASIC, and future refinement of the design would improve the system greatly. The major flaws revealed in bench testing of the ASIC (apart from minor, easily fixed errors), were the larger-than-expected noise in the offset removal circuitry, specific re-

sistance requirement for the pressure sensor, and an increased level of current draw beyond designed values.

10.1.1 *Reduced Offset IDAC Noise and Insensitivity to Sensor Resistance*

The increased level of offset removal noise, as well as the resistance requirement for the pressure sensor, stem from the current-output DAC topology and are related. A sensor with larger resistance converts the current noise to a larger noise voltage, and disrupts the offset removal system loop gain and frequency response. This effect could be lessened through an architectural shift to a voltage-mode offset removal mechanism as illustrated in Figure 10-1. The existing IDACs could drive an on-chip resistive load, creating an offset voltage with known magnitude and independence from the pressure sensor resistance. Furthermore, the resistor magnitude could be fairly low and the IDAC reference current could be increased, thereby increasing the inversion level of all IDAC FETs, reducing settling time, and reducing the noise current magnitude. Added filter capacitance at the IDAC output could be used to set the noise power bandwidth such that the target noise level is achieved. Depending on settling requirements, the offset voltages could be sampled directly by the CDS amplifier during the normal switching cycle, or small buffer amplifiers could be used. This approach would increase the power draw of the offset removal system and would require a wider dynamic range or lower gain preamplifier, but would otherwise have few drawbacks.

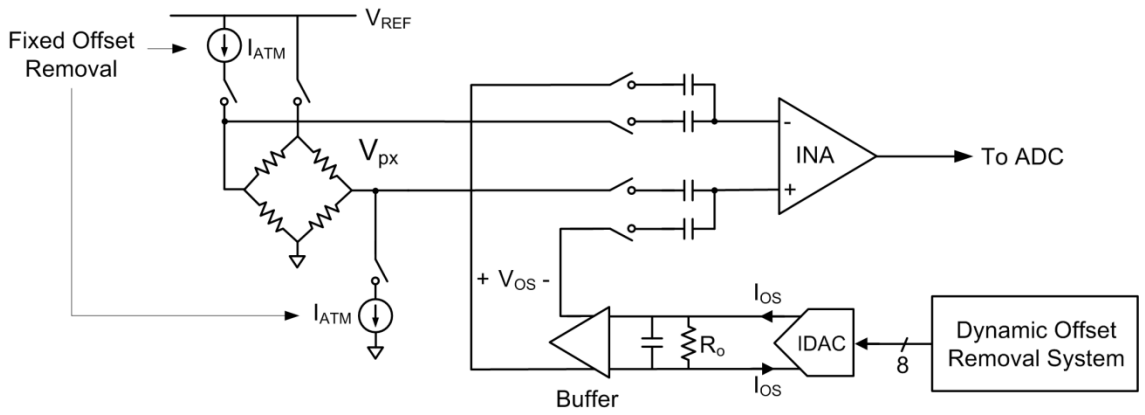


Figure 10-1. Potential architecture change to reduce the dependence on pressure sensor resistance and the effects of IDAC noise on the offset removal system.

10.1.2 *Reduced Transmitter Active Time and Error-Correcting Data Encoding*

Reducing the power consumption of the ASIC could be achieved on multiple levels. The simplest power reductions would require changes to the HDL code to reduce dynamically-powered circuit duty cycles and to add power-saving features such as clock-gating to key digital circuits. For example, the data packet generator is always clocked, even though a new data packet is produced just once per sampling period. Individual circuit warm-up periods were chosen conservatively, and bench testing has shown that this period is at least 50% longer than it must be for every circuit. Furthermore, the external receiver can respond within 1 µs of the start of transmission (as shown in Figure 10-2), and so the transmitter synchronization period can be reduced dramatically to only 1% of its present value.

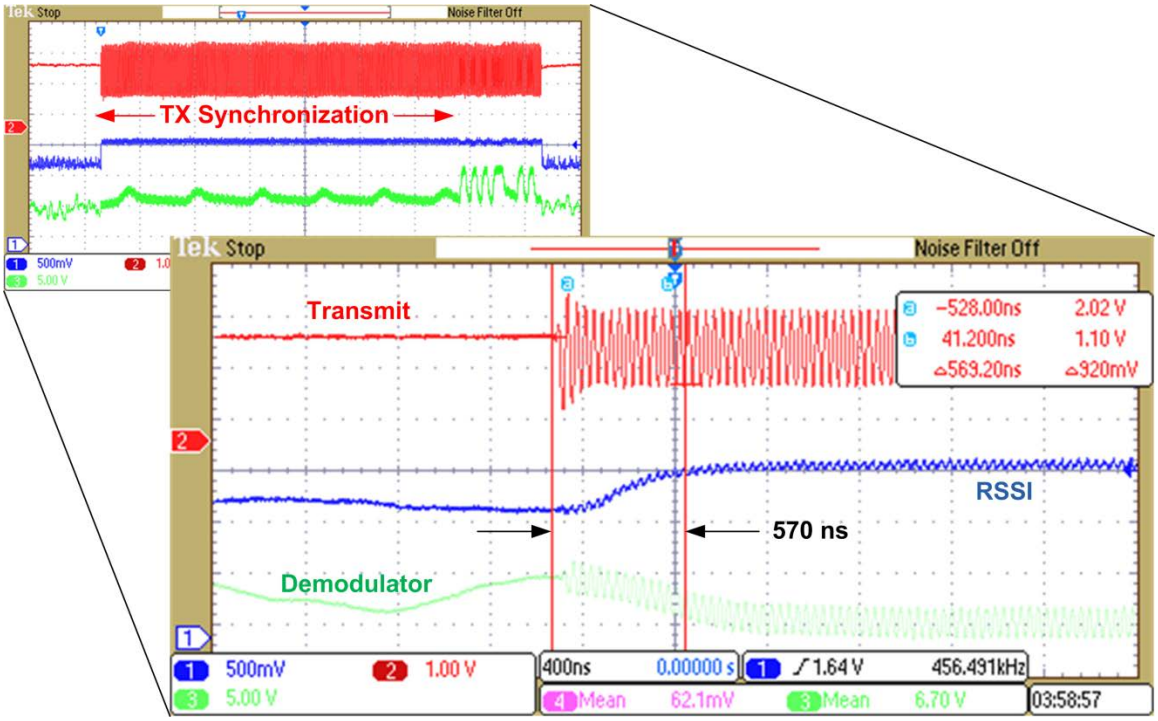


Figure 10-2. The receiver RSSI response time is well below the synchronization period used by the WIMM.

Because the WIMM transmitter synchronization period is much longer than it needs to be, the data packet length could also be increased without any additional power draw, although this would affect the transmitter power draw if the synchronization period was reduced to a minimal level. The most useful information to add to the transmitted packets would be error-correcting codes, such as Hamming codes, which can correct 1- or 2-bit errors based on the level of parity overhead bits [66]. For example, by increasing the packet length by 35% to 19 bits, single bit errors can be corrected, assuming that each data packet carries only 10 bits of “critical” information (with the other bits used for packet framing and alignment). Since the transmitted power is so low and transmission distance for the WIMM is currently limited by BER, adding even a small amount of error-tolerant encoding would increase the effective transmission distance by

several factors. The use of Hamming code error correction would only add slightly to the WIMM digital circuit area and computation would have a negligible power impact.

10.1.3 *Reduced ASIC Power Draw Through Multirate Clocking, Adaptive Sampling, Event Detection and Predictive Sampling*

Further reduction in the ASIC power consumption could be achieved through minor architectural changes. Since the digital circuitry does not run very quickly, it could be powered from a separate, 1.5-V regulator to achieve a 3X reduction in current draw, and level shifters could be added at the analog/digital boundary. The dominant power draw in the digital circuitry is the 20-bit clock divider that is always clocked at 100-kHz to generate 100-Hz and 0.3-Hz clock signals. It would be possible to create a slow and a fast oscillator; digital circuitry could run from a simple 1-kHz oscillator and occasionally switch to the 100-kHz clock source during a sampling period. Although the ASIC is presently powered through an integrated regulator, the analog circuits do not require it as they use a supply-independent voltage reference. The pressure sensor, however, is powered from the regulated supply, and has a ratiometric output sensitivity and offset. The pressure sensor could be driven by a buffered reference voltage to eliminate the background power draw of the always-on voltage regulator.

Major architectural changes could also be employed to reduce the power draw of the analog circuitry; the adaptive transmission scheme could be extended to an adaptive sample rate, for example. A low-precision, but very low-duty cycle “activity monitor” circuit could be used to poll the pressure sensor at a fairly high rate (200 Hz, e.g.). Full-resolution samples could then be initiated once the activity monitor detected a certain magnitude difference in successive samples. One potential circuit for the activity monitor could be a time-to-digital converter, which would use the output voltage from the pressure sensor to charge a fixed capacitor during a very

short sampling period (approximately 1 µs to allow for settling). After turning off the pressure sensor, the capacitor would discharge through the passive sensor resistance, and a high-speed digital counter could measure the time constant, thereby estimating the pressure to a low level of precision. Comparison of successive samples could be performed with an asynchronous digital comparator to ensure low-power operation.

Another possibility to implement predictive sampling, as well as a reduction in the data transmission rate, might be to use a digital event detection "expert system" with bladder-specific signal processing. This approach could classify important bladder events, and set the overall sampling rate for the system accordingly. For example, certain contractions might be followed by a refractory period of lower activity which would require a very low sampling rate. These activity patterns could vary from patient to patient, and the system could be designed to have a "learning" phase in which high-power constant sample rates are used while the patient is evaluated in a controlled urodynamics setting. After learning the specific patterns of contraction, the expert system could then control the overall sample rate by periodically sampling the pressure sensor to observe small windows of bladder activity, then determining the appropriate sample rate for the next 20 seconds of operation. Furthermore, with this system the WIMM would only have to transmit simple information about the type of bladder event, reducing the required transmission rate and permitting power savings in the long periods between classifiable events.

10.1.4 *Future Implantable Applications for the WIMM*

Finally, future pressure sensing applications for the WIMM can easily be envisioned across a variety of clinical disciplines and organ implantations. Electrically, the WIMM would not re-

quire any changes to chronically sense pressure in deep organs such as the stomach or anus. For acute applications such as a floating bladder pressure sensor or swallowable sensor for gastrointestinal diagnosis, the WIMM could be powered by a primary cell battery, permitting weeks of operation without requiring the external RF recharger. Furthermore, the WIMM implant could be used as a batteryless, RF-powered device by coupling the output of the RF rectifier to the monolithic voltage regulator. This configuration would be particularly useful in applications where very small size and weight are advantageous, such as an instrumented arterial catheter guide wire, small animal sensor platform, or pressure-sensing “smart” stent/graft. Although the WIMM was designed to measure pressure, the ASIC can interface to a wide array of voltage-output sensors (i.e. for temperature and strain), and the RF rectifier for battery recharge can receive energy from any resonant circuit, such as a piezoresistive energy scavenger. This flexibility could allow the WIMM to work in a variety of other applications where a tiny, low-power sensor would be useful.

CHAPTER 11

APPENDIX

11.1 Inversion coefficient design methodology

In traditional analog CMOS designs, the MOS transistor operating point and characteristic equations are classified into three simple operation regions: cutoff, triode, and saturation. The transistor behavior in saturation is described by the square-law model, which predicts that drain current varies as the square of the gate overdrive voltage V_{GS}-V_T. Realistically, the inversion charge layer grows exponentially with small V_{GS}, and thus the transistor moves through a continuum of states from cutoff towards full saturation. These states can be roughly classified by the level of charge inversion from weak to strong inversion. The drain current is only accurately predicted as a square-law function gate overdrive voltage V_{GS}-V_T when the device is in strong inversion, as depicted in Figure 11-1.

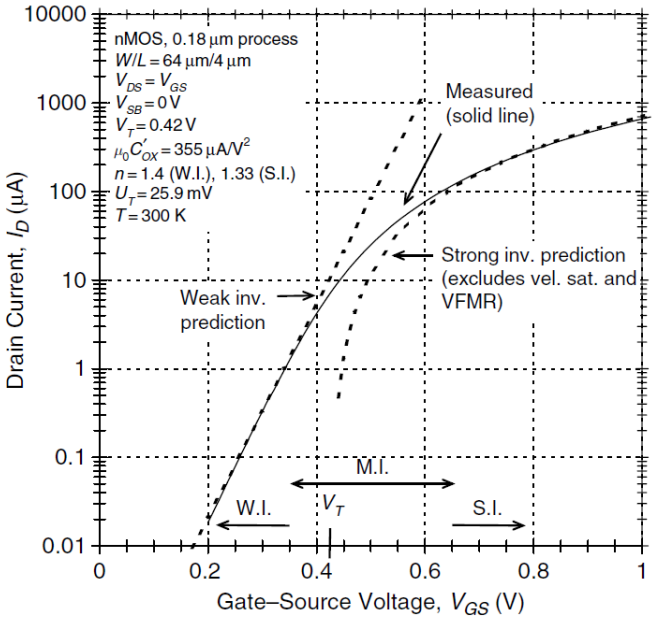


Figure 11-1. Modeled log(I_D) versus V_{GS}, which shows that the square-law model prediction is only valid for devices in strong inversion (S.I. region). The drain current dependence in moderate inversion (M.I. region) or weak inversion (W.I. region) is exponential (from [67]).

The device is only strongly inverted when $V_{GS} - V_T \gg U_T$. For smaller levels of gate overdrive the transistor channel is only moderately inverted, and if $V_{GS} - V_T < 3U_T$ the device operates in weak inversion, where diffusion currents dominate the behavior. Self-biased, low-power analog CMOS designs generally do not use enough current or large enough supply voltages to bias transistors in strong inversion. Therefore, it is best to design such circuits using a methodology that is valid in all regions of MOS operation.

The EKV model [68] is perhaps the simplest and most commonly-used model for describing MOS behavior in weak, moderate, and strong inversion. This model defines a process-dependent technology current I_S as

$$I_S = 2\mu C_{OX} U_T^2 n \cdot \frac{W}{L}, \qquad \text{(A.1)}$$

where μC_{OX} is the mobility-gate oxide capacitance term sometimes represented by k', W and L are the MOS width and length, and *n* is the substrate coefficient sometimes represented by $\kappa = 1/n$. The technology current I_S is dependent on the MOS shape factor and must be recalculated for each transistor to be modeled. Small-signal transconductance is calculated by

$$g_m = \frac{I_D}{nU_T} \cdot G'(I_D), \tag{A.2}$$

where I_D is the drain bias current, and $G'(I_D)$ is the transconductance adjustment factor given by

$$G'(I_D) = \frac{1-e^{-\sqrt{I_D/I_S}}}{\sqrt{I_D/I_S}}. \tag{A.3}$$

In (A.3), the factor I_D/I_S is commonly called the inversion coefficient (IC) because it represents the level of channel inversion. For very low IC the expression for$G'(I_D)$ approaches one, and ultimately the small-signal transconductance saturates as

$$g_{m_{min}} \approx \frac{I_D}{nU_T}, \tag{A.4}$$

indicating that transconductance cannot simply be increased by growing the W/L ratio indefinitely.

The EKV model is not typically used by SPICE-based simulators, and the substrate factor *n* is not included in the common BSIM3v3 models provided by foundries. Simulations were performed to quantitatively extract the effective *n* factor from existing models by parametrically sweeping the MOS shape factor and measuring g_m. When the MOS enters deep weak inversion, g_m approaches the value calculated by Equation (A.4), and *n* can be estimated. For the 0.5-µm

process, an *n* of 1.4 was extracted. Resulting technology currents of $220 \cdot \frac{W}{L}$ nA and $75 \cdot \frac{W}{L}$ nA were calculated for NMOS and PMOS devices, respectively.

Once the technology current is known, it is simple to calculate the inversion coefficient as the ratio of the drain current to the technology current [67]. Generally, *IC* less than 0.1 describes devices in weak inversion, *IC* between 0.1 and 10 corresponds to moderate inversion, and *IC* greater than 10 indicates a device in strong inversion, as shown in Figure 11-2. The *IC* is also used to calculate the gate overdrive voltage (denoted V_{EFF}) as

$$V_{EFF} = V_{GS} - V_T = 2nU_T \ln\left(e^{\sqrt{IC}} - 1\right), \tag{A.5}$$

and the minimum drain-source voltage to maintain saturation is estimated by

$$V_{DSAT} \cong 2U_T\sqrt{IC + \frac{1}{4}} + 3U_T. \tag{A.6}$$

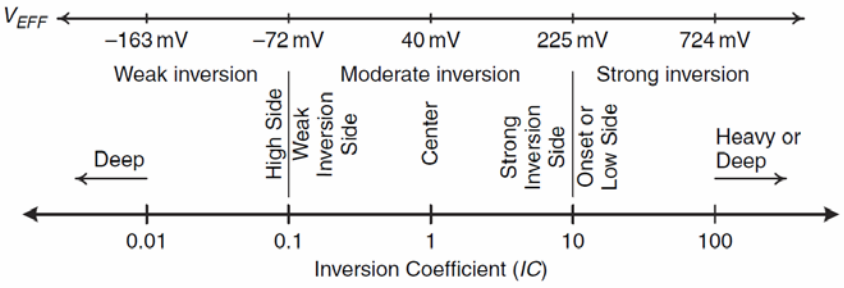


Figure 11-2. Chart of MOS inversion coefficient versus effective V_{GS}-V_T (from [67]).

While the BSIM3v3 model does describe weak to strong inversion performance, designing a circuit by an inversion coefficient methodology provides a useful starting point for choosing device W/L ratios to match a desired operating current. Generally, the tradeoffs outlined in

Figure 11-3 are used when designing with an *IC*-based methodology. Weak inversion operation is avoided except for cases in which large a large g_m/I_D ratio is required, such as amplifier input pairs. Current mirrors are generally sized with long L to operate at least in moderate inversion and to improve matching while reducing flicker noise.

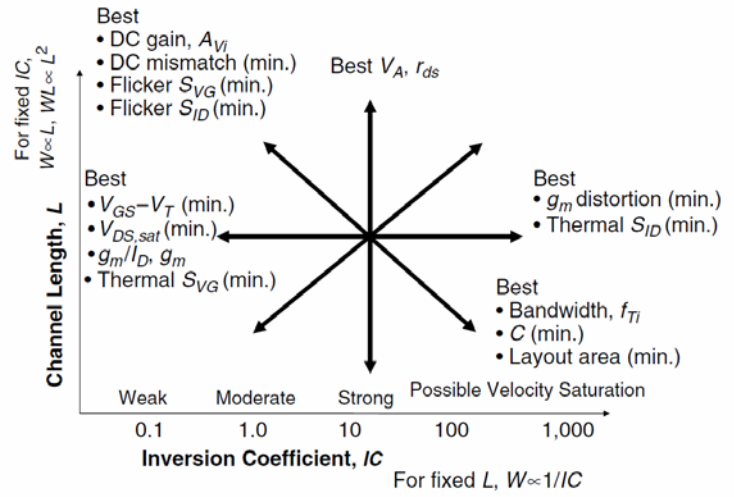


Figure 11-3. A graph showing the tradeoffs between MOS shape factors and inversion coefficient. Generally, low-power circuits use IC less than 10 (from [67]).

11.2 Design Details of ASIC Circuits

11.2.1 *INA Preamplifier Noise Analysis*

The PMU turns the pressure sensor on for 140 µs per sample, which in turn determines the input capacitance and settling time limitations for the INA. The input capacitance limit is given by

$$C_{in} < \frac{6 \cdot (t_{ON} - 40\mu s)}{R_{BRIDGE}}, \tag{1.17}$$

where t_{ON} is the on-time of the pressure sensor, 140 µs, and R_{BRIDGE} is the output impedance of the pressure sensor, 4 kΩ. Six linear settling time constants are allowed for 8-bit resolution, leading to a C_{in} limit of 210 pF.

The settling time of the preamplifier output is limited to 40 µs, or 4 clock periods which is the chopper switch rate while the preamplifier is active. The preamplifier has a "warmup" phase prior to amplifying the pressure sensor in which the output voltage slews to a its quiescent point, so it is assumed that during sensor amplification only linear settling occurs. This is a fair assumption since the preamplifier gain is low and the amplifier differential input voltage is small. Therefore, the preamplifier settling time constraint is given by

$$t_{settle,preamp} = 6 \cdot \tau_{SS} < 40\ \mu s, \tag{1.18}$$

where the small-signal settling time constant, τ_{SS} can be approximated by

$$\tau_{SS} = {}^{1}/_{\beta \cdot GBW}, \tag{1.19}$$

in which β is the feedback factor and GBW is the unity-gain bandwidth for the preamplifier. Since the preamplifier is open-loop the β term is ignored and the preamplifier GBW must be at least 48 kHz to satisfy the settling time requirement.

Once the GBW is determined the preamp input-referred thermal noise limitation can be considered. The thermal noise limit should be less than the input-referred ADC quantization noise, or

$$\overline{v_{in,preamp}^2} <= \frac{V_{FS}^2}{12 \cdot 2^{2N} \cdot A_{V,INA}^2}, \tag{1.20}$$

where $A_{V,INA}$ is the maximum INA voltage gain of 260X, V_{FS} is the ADC full-scale range of 1.4 V and *N* is the resolution of 8 bits. With these values, the input-referred thermal noise limit is 2.2×10^{-10} V^2/Hz, or equivalently, about 6 µVrms. This noise figure must account for both amplifier stages, so the noise contributions were split such that the 2nd stage amplifier provides roughly one-third of the input-referred noise power as that of the preamplifier.

The preamplifier input pair $M_{1,2}$ was sized to operate deep in weak inversion to maximize the transconductance, while other transistors were maintained in moderate inversion. The input-referred thermal noise power for the amplifier is given by

$$\overline{v_{in,preamp}^2} = 2 \cdot \frac{8kT}{3g_{m1}}\left(1 + \frac{g_{m3}}{g_{m1}} + \frac{g_{m6}}{g_{m1}}\right), \quad (1.21)$$

where the additional factor of 2 is due to the differential topology. The preamplifier was designed for a differential gain of 6.5 V/V, and has an input-referred noise density of 22 nV/$\sqrt{\text{Hz}}$.

11.2.2 *INA 2nd-stage amplifier noise analysis*

The amplifier thermal noise is analyzed by dividing the amplifier into its configurations during ϕ_1 and ϕ_2 as depicted in Figure 11-4. In these configurations, the input-referred thermal noise of the opamp is denoted $\overline{v_{ni,amp1}^2}$ and $\overline{v_{ni,amp2}^2}$, while the sampling noise of the input capacitor is represented by $\overline{v_{C1,sw1}^2}$ and $\overline{v_{C1,sw2}^2}$. Capacitors are based off of a unit capacitor C_0, with C_1=80C_0, C_2=C_3=4C_0. The value of C_0 was chosen to satisfy thermal noise requirements, as detailed below.

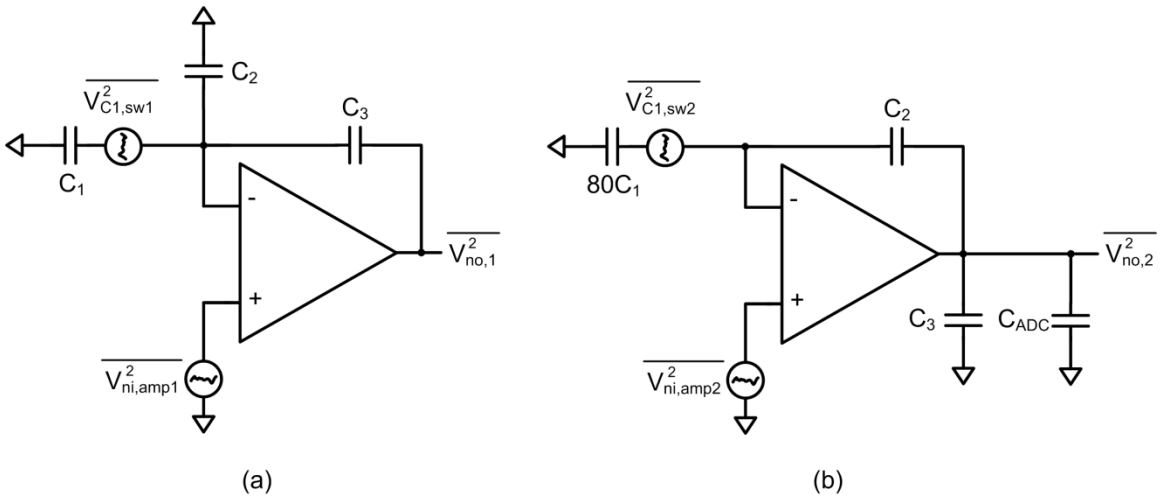


Figure 11-4. Noise analysis equivalent circuits for the SC amplifier with the ϕ_1 phase in (a) and the ϕ_2 phase in (b). Only half of the circuit is analyzed, with switch noise multiplied by 2 to account for the full amplifier.

In ϕ_1 the amplifier thermal noise is given by $\overline{v_{ni,amp1}^2} = \frac{4kT}{3}\frac{\beta_1}{C_{L,1}}$, where β_1 is the phase 1 feedback factor equal to $\frac{1}{22}$ and $C_{L,1}$ is the amplifier load capacitance of $\frac{42}{11}C_0$. The amplifier transconductance does not appear in this equation because the noise reduction and bandwidth increase effects cancel each other [61]. Effectively, the amplifier input-referred thermal noise is a function of the unit capacitance, C_0. The thermal noise sampled onto C1 is given by $\overline{v_{C1,sw1}^2} = \frac{kT}{84C_0}$ because C_1 and C_2 are in parallel. Both noise contributions can be combined and represented as a charge stored on C_1.

When the amplifier switches into ϕ_2, all of the noise charge on C1 is integrated by C_2. Moreover in ϕ_2 the ADC sampling capacitor must be considered, since it changes the amplifier bandwidth. The amplifier thermal noise in phase 2 is $\overline{v_{ni,amp2}^2} = \frac{4kT}{3}\frac{\beta_2}{C_{L,2}}$, with β_2 equal to $\frac{1}{20}$ and $C_{L,2}$ equal to approximately $C_{ADC}+4C_0$. Finally, the thermal noise sampled onto C1 is equal to

$\overline{v_{C1,sw2}^2} = \frac{kT}{80C_0}$. Adding all of the noise sources, at the end of ϕ_2 the total input-referred noise voltage can be calculated as

$$\overline{v_{in,tot}^2} = 2\left(\overline{v_{ni,amp1}^2} + \overline{v_{C1,sw1}^2} + \overline{v_{ni,amp2}^2} + \overline{v_{C1,sw2}^2}\right), \tag{1.22}$$

where the factor of 2 is added since only a half-circuit was analyzed in Figure 11-4.

After entering values and ignoring negligible terms, Equation (1.22) can be simplified to

$$\overline{v_{in,tot}^2} \cong \frac{2kT}{C_0}\left(\frac{1}{40} + \frac{4}{229}\right). \tag{1.23}$$

The stage 2 amplifier noise can be designed by selecting C_0 such that the noise does not contribute noticeably to the total input-referred noise of the INA. The preamplifier noise at the input of stage 2 is about 70 µVrms, so the maximum tolerable stage 2 input-referred noise is 36 µVrms, achieved with $C_{0,min}$ = 270 fF. A smaller C0 of 100 fF was used to limit the amplifier area in layout, and to reduce the settling time limitation of the 2nd-stage amplifier. The resulting 2nd-stage input-referred thermal noise is 59.3 µVrms yielding a total INA input-referred noise of 7.06 µVrms. This level exceeds the ADC quantization noise slightly at the maximum gain setting, but other amplifier gain settings meet the quantization noise requirement.

11.2.3 *SAR ADC Redistribution DAC capacitor sizing*

The most critical design decision for the charge-redistribution DAC is the size of C_{min}, since this affects the total DAC layout area, settling time limitations, and matching for linearity. As a starting point, the thermal noise stored on the output of any switch in series with a sampling capacitor is given by

$$\overline{V_{switch}^2} = \frac{k_B T}{C}. \qquad 1.24)$$

where k_B is Boltzmann's constant and T is the temperature in Kelvin [61]. The thermal noise must be less than the RMS ADC quantization noise, or

$$\frac{k_B T}{C_u} < \frac{V_{LSB}^2}{12} = \frac{V_{FS}^2}{2^{2N} \cdot 12}, \qquad 1.25)$$

where V_{LSB} is the is the minimum code difference for an N-bit ADC with a full-scale conversion range of V_{FS}. In this design V_{FS} of 1.4 V was chosen, with a corresponding V_{LSB} of 5.5 mV; the resulting C_u to satisfy the thermal noise requirement is 1.7 fF. This capacitor size is smaller than the minimum that can be created in the chosen 0.5-µm technology, so thermal switch noise can be neglected in this design.

Another important consideration in the sizing of C_u is charge injection error caused by the closing of MOS switches. In the ON state, the inversion layer charge of a MOS switch is approximately given by

$$Q_{inv} = WLC_{ox}(|V_{GS}| - |V_T|), \qquad 1.26)$$

where W and L are the width and length of the transistor, C_{ox} is the gate capacitance density, V_{GS} is the gate-to-source voltage, and V_T is the threshold voltage of the switch. In the chosen 0.5-µm process, C_{ox} is 2.46 fF/µm^2, and $|V_T|$ is 0.7 and 0.9 for NMOS and PMOS FETs respectively.

When a MOS switch leaves saturation and turns off, the additional charges in the inversion layer flow out of the source/drain terminals, and this can cause voltage changes on high-impedance (sampled) nodes.

The charge injection error can be mitigated to first order by simply using complementary NMOS/PMOS transmission gates on switched-capacitor nodes, as depicted in Figure 11-5. A simple approximation for the flow of inversion layer charge is to assume that half of the charge leaves each side of the FET channel. The charge polarities are opposite, and, assuming equal-sized N and P devices, the net voltage change on the sampled node due to charge injection can be calculated by

$$\Delta V_x = \frac{WLC_{ox}[(|V_{GS_N}|-|V_{T_N}|)-(|V_{GS_P}|-|V_{T_P}|)]}{C_H}, \qquad 1.27)$$

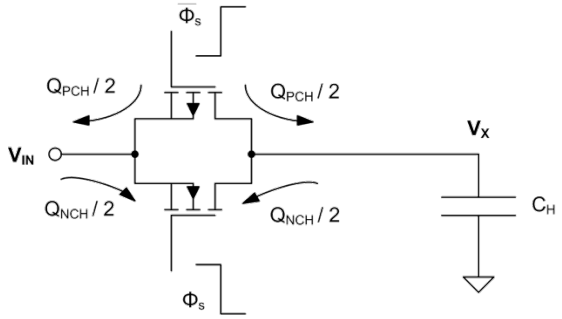


Figure 11-5. Circuit model of transmission gate showing charge injection paths when the switch opens.

For the chosen process, ideal charge cancellation ($\Delta V_X = 0$) occurs when V_{in} is 1.4 V, assuming a 2.6 V supply voltage. For the SAR ADC with input voltage range from 0.7 – 2.1 V, the charge injection is most unbalanced at the extremes of the input voltage range. At these values, only 60% of the total injected switch charge is canceled. Therefore, the charge injection error must still be considered when choosing C_u.

Charge injection error can affect the systematic offset, as well as the differential nonlinearity (DNL) of the ADC. Systematic offset generally does not affect ADC linearity since it is generally DC, but reduces dynamic range if the offset value approaches V_{LSB}. Charge injection errors affect DNL because the amount of charge injection varies with the code being tested, due to the switching action of the charge redistribution DAC, and can lead to missing codes in the ADC transfer function. In this ADC topology, the dominant source of systematic charge injection error is the comparator auto-zero switch connected to the DAC summing node and the deterministic switching pattern used by the SAR algorithm. The switches connected to VR+/VR- on the DAC capacitor bottom plates are the major source of DNL-affecting charge injection error.

The systematic charge injection error can be determined using the schematic of Figure 4-3 above. After the auto-zero phase ends and switch S_X opens, the summing node voltage V_x can change by a maximum of

$$\Delta V_{x,auto-zero} = 0.4 \cdot \frac{Q_{CH}/_2}{2^N C_u}, \quad 1.28)$$

for an N-bit ADC, and assuming worst-case complementary charge injection. This assumption is pessimistic because charge injection from matched complementary MOSFET pairs with V_{ref}=1.4 V and V_{DD} = 2.6 V should be perfectly balanced.

The switching behavior of the capacitive DAC is partly deterministic due to the SAR algorithm. Regardless of input voltage, each capacitor of the DAC will be toggled to V_{R+} once during the conversion. Depending on the result of that SAR cycle, the switch might subsequently reconnect to V_{R-}, but each bit testing cycle of the SAR will change V_x by

$$\Delta V_{x,bit-test} = 0.4 \cdot \frac{Q_{CH}/_2}{(2^N - 2^n) C_u}, \quad 1.29)$$

where *n* is the value of the bit being tested. (1.29) was derived by noting that when each capacitor is tested, the injected charge flows into the remaining, untested capacitors in the binary-weighted DAC. Expanding (1.29) to cover all 8 bits of the SAR cycle and adding the contribution of (1.28) gives a total systematic offset error of

$$\Delta V_{x,systematic} = 0.4 \cdot \frac{Q_{CH}/_2}{C_u} \cdot \sum_{n=0}^{N-1} \frac{1}{(2^N - 2^n)}. \quad (1.30)$$

The systematic offset is not a function of input voltage, and therefore will not affect the ADC DNL since the ADC will incur systematic offset with each conversion. However, depending on the value of V_{in}, after each bit test cycle the bit being tested may remain connected to V_{R+} or get switched to V_{R-} for the next bit testing cycle. When the tested bit is switched to V_{R-} a second charge injection arises, and this contributes to DNL. The worst-case input-dependent charge injection error occurs for the ADC output code of "0000 0001", and is equal to

$$\Delta V_{x,DNL} = 0.4 \cdot \frac{Q_{CH}/_2}{C_u} \cdot \sum_{n=2}^{N-1} \frac{1}{(2^N - 2^n)}. \quad (1.31)$$

To avoid DNL and offset errors, the minimum DAC capacitor size must be chosen such that the total charge injection error is less than half the step height of the ADC LSB, or in other words

$$v_{LSB}/_2 > \Delta V_{x,systematic} + \Delta V_{x,DNL}. \quad (1.32)$$

With the design parameters of v_{LSB} = 5.5 mV and a minimum MOS switch size of 1.8 x 0.6 µm, C_u > 6.5 fF is required to avoid charge injection errors.

One final consideration in the sizing of C_u is parasitic capacitance on the DAC summing node. This capacitance is mostly due to wiring of the DAC array and the input capacitance of the comparator and can lead to further systematic offset errors as well as ADC gain error. If the total

parasitic capacitance on the summing node is C_P and the total capacitor array size is C_{TOTAL}, the ADC offset is increased by a factor of roughly

$$\Delta V_{x,parasitic} = V_R \frac{C_P}{C_P + C_{TOTAL}}. \quad (1.33)$$

The ADC gain error is affected because after V_{in} is sampled, part of the stored charge is redistributed over C_P, and the actual value of the sampled voltage is

$$V_{sampled,eq} = V_{in} \frac{C_{TOTAL}}{C_P + C_{TOTAL}}. \quad (1.34)$$

The value of CP does not affect the comparator auto-zero offset removal because it is in parallel with the DAC array and is charged to the same voltage, $V_{ref}+V_{OS}$, during the comparator reset phase.

The value of C_P can be reduced through good IC layout practices, and to maintain low power consumption and reduced die area this is preferable over increasing the size of C_{TOTAL}. In this ADC design, it was estimated that a C_P of 400 fF could be attained, so a unit capacitor size of C_u=15 fF was chosen. This value limits thermal noise, systematic offset, and voltage-dependent charge injection errors below the quantization noise for an 8-bit ADC. The resulting total DAC capacitance is 3.8 pF, which is reasonably low to attain low dynamic power consumption and good settling time without and ADC buffer driver. Including the parasitic capacitance effects, the ADC systematic offset is 13 mV and the anticipated gain error is 10%. The ADC offset can be addressed by the pressure-sensing system automatic offset cancellation, and the gain error should not change over time and be well matched between different chips.

11.2.4 *SAR ADC Comparator Preamp Design*

The SAR ADC preamp schematic is shown in Figure 11-6, and the topology is a simple single-stage differential amplifier. This configuration typically achieves an open-loop gain of

about 100 with good bandwidth and input/output signal swing ranges. The single-ended topology has a well-defined common-mode output level without need for common-mode feedback, and the input-referred offset is typically about 10 mV with good layout techniques. Switch $M_{b,1}$ is included to allow for power control; when PwrEn < V_{TN} the preamplifier draws no bias current.

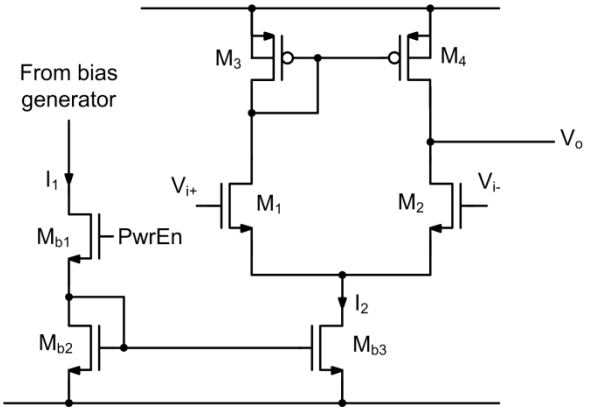


Figure 11-6. Schematic of the SAR comparator preamplifier.

Name	Value	Inversion Coefficient
M_{1-2}	5.4 µm / 1.8 µm	5
M_{3-4}	3.6 µm / 1.2 µm	5
M_{b2-b3}	7.2 µm / 3.6 µm	15
I_1	2.5 µA	-
I_2	2.5 µA	-

Transistors M_{b2-b3} form a current mirror for biasing and power control, and when M_{b1} is on, M_{b3} sinks 2.5 µA of bias current. The bias current was chosen to satisfy requirements of noise and settling time, but kept fairly large to increase inversion levels and device matching. Transistors M_{3-4} were sized to operate in moderate inversion to enhance matching and to limit offset. The input pair M_{1-2} were sized to meet constraints of thermal noise and bandwidth. The large-signal output range of the preamplifier is 0.35 – 2.4 V, which covers the ADC FS range of 0.7 – 2.1 V. Due to open-loop operation the preamplifier leaves its linear gain region with very

large differential inputs. However, the comparator preamplifier only needs to overcome the uncompensated latch offset, and accurate gain is not required for large differential inputs. When operating at its quiescent point the preamplifier voltage gain is given by

$$A_V = g_{m1,2}(r_{o4}//r_{o2}), \tag{1.35}$$

where $g_{m1,2}$ is the input pair transconductance and r_{o2}-r_{o4} are the small-signal output resistances of M_2 and M_4. For the given device sizes and bias currents, A_v is equal to 136 V/V.

The input-referred thermal noise for the preamplifier must be less than the ADC quantization noise or

$$\overline{V_{ni}^2} < \frac{v_{LSB}^2}{12}, \tag{1.36}$$

where the preamplifier input-referred thermal noise is calculated by

$$\overline{V_n^2} = \frac{16kT}{3g_{m1}}\left(1 + \frac{g_{m3}}{g_{m1}}\right)BW. \tag{1.37}$$

In Equation (1.37), *k* is Boltzmann's constant, T is the temperature in Kelvin, g_{m1} and g_{m3} are the transconductances of M_1 and M_3, and BW is the noise bandwidth as defined by the 3-dB bandwidth of the amplifier multiplied by $\pi/2$ to account for the single-pole frequency rolloff. Because the preamplifier is auto-zeroed before each conversion and the total conversion time is less than 1 ms, it is assumed that the low-frequency (1/f) noise of the preamplifier will appear as a drifting, canceled offset, and can be neglected. Using the device sizes and bias currents, the input-referred thermal noise for the preamplifier is about 40 µVrms. This value is well below the quantization noise limit defined by (1.36), so the preamplifier noise is negligible in the ADC design.

11.2.5 *SAR ADC Comparator Preamplifier Offset Cancellation*

During each ADC sample cycle the comparator offset is automatically removed, or auto-zeroed. This is required because the comparator offset directly affects the total ADC offset, and offset below V_{LSB} cannot be guaranteed through layout matching alone. Because the comparator preamp is single-ended, its offset can be stored by configuring it as a buffer using a switch as shown in Figure 11-7. The input-referred offset voltage V_{OS} has been added to model the trans-conductance mismatch of the preamp differential input pair. While S_R is closed, the voltages at Vo and Vi- are given by

$$V_O = V_{i-} = \left(V_{ref} - V_{os}\right)\left(1 - \frac{1}{A_V}\right), \tag{1.38}$$

where V_{OS} is the input-referred offset of the preamp and A_V is the preamplifier voltage gain. With A_V> 100, at least 99% of the input-referred offset is stored on the DAC capacitor array. Since V_{OS} remains stored for the ADC conversion cycle, subsequent preamplifier operation is nearly offset free.

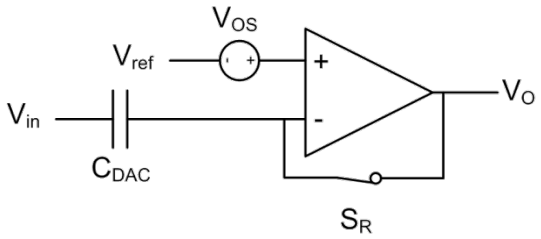


Figure 11-7. Equivalent schematic of the comparator preamplifier during auto-zero phase. Voltage source VOS has been added to model the input-referred preamplifier offset.

The preamplifier bandwidth during the conversion cycle is very high because it is loaded only by the regenerative latch capacitance. However, during the auto-zero/sample cycle, the preamplifier drives the entire SAR DAC capacitor array through S_R. It is important that the pre-amplifier store V_{REF}+V_{OS} on the array during this period, to an accuracy better than $100/2^N$, or about 0.5% for an 8-bit ADC. The preamplifier worst-case settling time is roughly predicted by

$$t_{settle} = t_{slew} + t_{settle,ss} = \frac{(V_{ref} - V_{R-}) \cdot C_{DAC}}{I_B} + 6 \cdot \tau_{RC}, \quad (1.39)$$

where t_{SLEW} represents the worst-case time for the preamplifier to slew the capacitor voltage close to V_{ref} and $t_{settle,SS}$ is the small-signal, linear settling time. The slewing time is a function of I_B, the total preamplifier bias current, and the linear settling time constant which can also be expressed as

$$\tau_{RC} = \frac{1}{GBW}, \quad (1.40)$$

where the preamplifier unity-gain bandwidth GBW is a function of the preamplifier output resistance and C_{DAC}. Six time constants of small-signal settling time are allowed so that the preamplifier can reset the DAC to an accuracy of 0.25%, or better than 8-bit resolution. For the given bias currents, the preamplifier worst-case settling time is about 1.16 µs. The settling time is over-designed when the ADC is clocked at 100 kHz, but allows the ADC to run faster in other applications, if needed.

11.2.6 *Offset cancellation IDAC noise analysis*

The total IDAC output-referred noise is a function of the fixed offset removal current, the IDAC unit bias current, the pressure sensor bridge resistance, and the current bandwidth. The equivalent circuit to analyze the noise of the fixed offset current sources is shown in Figure 11-8. The main current reference produces a 500 nA bias current I_B which is mirrored and scaled to produce the fixed offset sources I_{ATM}.

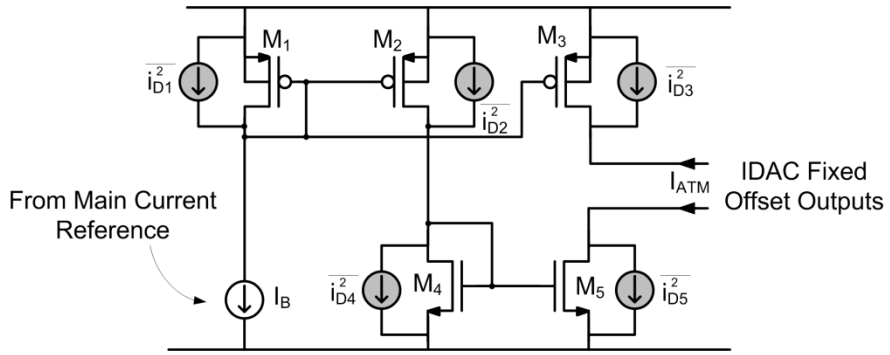


Figure 11-8. Schematic for analyzing the IDAC fixed offset current noise.

TABLE 11-1. TRANSISTOR SIZES AND BIAS POINTS FOR IDAC FIXED OFFSET CURRENT NOISE ANALYSIS.

Name	Value	Bias Current	Inversion Coefficient
$M_{1,2}$	5.4 µm / 9.0 µm	0.5 µA	10
M_3	20 x 5.4 µm / 9.0 µm	10 µA	10
M_4	3.6 µm / 3.6 µm	0.5 µA	2.3
M_5	20 x 3.6 µm / 3.6 µm	10 µA	2.3

To simplify the noise analysis, it is assumed that and all mirror copies are exact and offset-free. Thus, the differential output current $2I_{ATM} = 2 \cdot 20I_B$ and is equally carried by the NMOS and PMOS output sources. Furthermore, the noise bandwidth of $\overline{\imath_{D1}^2}$ is so low that it can be ignored and the reference current is similarly noise-free. The differential output current noise density $\overline{\imath_{DO,fixed}^2}$ is then equal to the combination of $\overline{\imath_{D3}^2}$ and $\overline{\imath_{D5}^2}$ or

$$\overline{\imath_{DO,fixed}^2} = \overline{\imath_{D3}^2} + \overline{\imath_{D5}^2} + 20^2 \cdot \left(\overline{\imath_{D2}^2} + \overline{\imath_{D4}^2}\right) \approx 20^2 \cdot \left(\overline{\imath_{D2}^2} + \overline{\imath_{D4}^2}\right). \quad (1.41)$$

Next, the IDAC unit current output noise can be analyzed using the circuit of Figure 11-9. The unit enable switches have been removed since they are in triode and contribute negligible thermal noise. It is assumed that the nA current reference contributes negligible noise, since its bandwidth is limited by bypass capacitance and that matched current mirrors have equal ther-

mal noise generators. The total worst-case differential unit output current noise $\overline{i_{DO,unit}^2}$ occurs when all of the IDAC elements are turned on and is given by

$$\overline{i_{DO,unit,max}^2} = 255 \cdot \left(2 \cdot \overline{i_{D2}^2} + 2 \cdot \overline{i_{D4}^2}\right) = 510 \cdot \left(\overline{i_{D2}^2} + \overline{i_{D4}^2}\right). \quad (1.42)$$

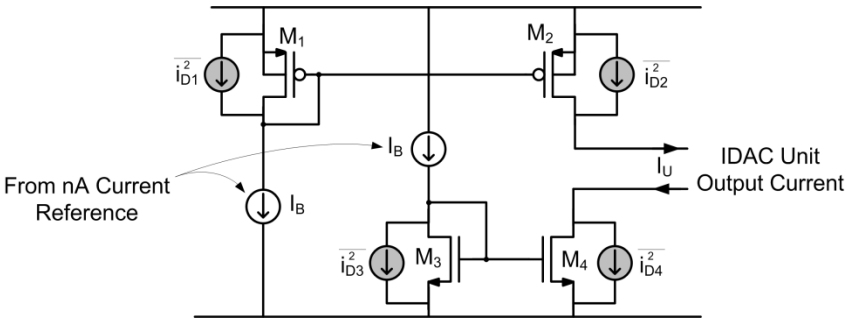


Figure 11-9. Schematic for analyzing the IDAC unit current noise.

TABLE 11-2. TRANSISTOR SIZES AND BIAS POINTS FOR IDAC UNIT CURRENT NOISE ANALYSIS.

Name	Value	Bias Current	Inversion Coefficient
$M_{1,2}$	3.6 µm / 11.7 µm	60 nA	2.6
$M_{3,4}$	3.6 µm / 11.7 µm	60 nA	1.0

Using the device sizes and inversion coefficients of Table 11-2, the value for $\overline{i_{DO,fixed}^2}$ was calculated to be about 5×10^{-23} A^2/Hz. Similarly, the worst-case $\overline{i_{DO,unit,max}^2}$ was calculated as 1.5×10^{-23} A^2/Hz, for a total combined output noise spectral density $\overline{i_{DO,IDAC}^2}$ of 6.5×10^{-23} A^2/Hz. Assuming the instrumentation amplifier bandwidth BW_{INA} dominates the frequency response, and converting to voltage because the IDAC noise current flows into the sensor bridge resistance R_{BRIDGE}, the total IDAC RMS output noise voltage is given by

$$v_{n,IDAC} = \frac{R_{BRIDGE}}{2} \cdot \sqrt{\left(\overline{i_{DO,fixed}^2} + \overline{i_{DO,unit,max}^2}\right) \cdot BW_{INA} \cdot \frac{\pi}{2}}. \quad (1.43)$$

Using design values of R_{BRIDGE} = 2.7 kΩ and BW_{INA} = 40 kHz, the equivalent IDAC output noise voltage is about 2.7 µVrms.

11.3 Command Decoder HDL Code

```
module wimm4_shutdown(
        input Mclk,
        input SampleClk100,
        input SampleClk050,
        input SampleClk003,
        input CMD,
        input SDownMode,
        input POR,
        output SysRst,
        output SDownOut
);

reg SDown;
reg SDownOvrEdge;
reg [3:0] SysRunCtr;
wire por_sdown;
reg [1:0] CMDCtr;
reg [2:0] RepCtr;
reg lockout;
wire SDownState;

always @ ( posedge CMD )      SDownOvrEdge = ~SDownOvrEdge;

assign SysRst = POR | SDownState;
wire SDowng;
assign SDowng = SDown & ~CMD;
assign SDownOut = SDownMode ? SDownOvrEdge : SDowng;
assign SDownState = SDownMode ? SDownOvrEdge : SDown;
reg CMDbuf;
wire CMDnegedge;
assign CMDnegedge = ~CMD & CMDbuf;
reg Clk050buf;
wire Clk050negedge;
assign Clk050negedge = ~SampleClk050 & Clk050buf;

always @ ( posedge Mclk )     begin
        CMDbuf = CMD;
        Clk050buf = SampleClk050;
end

always @ ( negedge Mclk )     begin
        if (Clk050negedge || lockout) CMDCtr <= 2'h0;
        else if (CMDnegedge & ~lockout)       CMDCtr <= CMDCtr + 1;
        else    CMDCtr <= CMDCtr;

        if ( (CMDCtr == 2'h3) && (CMDnegedge | CMD)) lockout <= 1'b1;
        else if ( Clk050negedge ) lockout <= 1'b0;
        else    lockout <= lockout;
end

wire Clk100;
assign Clk100 = SampleClk100 & ~SDown;
```

```
always @ ( negedge Clk100 )   begin
        if ( (CMDCtr == 2'h3) && ~CMD)        RepCtr <= RepCtr + 1;
        else if ( CMD || lockout || SampleClk003)    RepCtr <= 3'h0;
        else    RepCtr <= RepCtr;
end

always @ (negedge SampleClk100)       begin
        if ( (SysRunCtr == 4'hF) || (RepCtr != 3'h6) )       SDown <= 1'b0;
        else if (RepCtr == 3'h6)      SDown <= 1'b1; //Shutdown command has been received
        else    SDown <= SDown;
end

always @ ( posedge SampleClk003 ) begin
        if (~SDowng)   SysRunCtr <= SysRunCtr + 1;
        else    SysRunCtr <= 2'h0;
end

endmodule
```

11.4 Power Management Unit HDL Code

```
module wimm4_PCU(
        input Mclk,
        input FreeCtl,
        input INAClkIn,
        input RateCtl,
        input BridgeLong,
        input reset,
        output wire SampleStart,
        output reg Sampleen,
        output [7:0] CKTen,
        output [8:0] PCUCtr,
        output INAClkOut
);

reg [7:0] PCUctl;
reg [12:0] SampleCtr;
wire [7:0] PCUctl_g;
wire INAclk_g;
wire H10;
wire H50;
wire H100;

parameter PCU_default =       8'b10010000;   //default PCU states when SAMPLEEN = 0
parameter SampleTime =        8'd200; //number of clock cycles per sample, 100k clock rate
parameter INAon =             8'd01;
parameter INAoff =            8'd71;
parameter INAclk_p1 =         8'd01;
parameter INAclk_p2 =         8'd63;
parameter INAwarm_on =        8'd01;
parameter INAwarm_off =       8'd57;
parameter ADCon =             8'd01;
parameter ADCoff =            8'd78;
parameter PacketStart =       8'd61;
parameter BRIDGEon1 =         8'd45;
parameter BRIDGEon2 =         8'd55;
parameter BRIDGEoff =         8'd69;
parameter DACon =             8'd32;
parameter WarmP1 =            8'd32;

wire temp;
assign temp    = FreeCtl & ~reset;
assign CKTen = temp ? 8'b11101001 : PCUctl_g;
```

```
wire TempEn;
assign TempEn = Sampleen & ~reset;
assign PCUctl_g = TempEn ? PCUctl : PCU_default;
assign INAClkOut = FreeCtl ? INAClkIn : INAclk_g;
assign INAclk_g = PCUctl[2] ? SampleCtr[1] : PCUctl[1];
assign PCUCtr = SampleCtr[8:0];
assign H20 = (SampleCtr[12:0] >= 13'h1400);  //20 Hz
assign H100 = (SampleCtr[12:0] >= 13'h0400); //100 Hz
assign SampleStart = RateCtl ? H20 : H100;

always @ (posedge Mclk)       begin

if (SampleStart)      begin
        SampleCtr <= 13'h000;
        Sampleen <= 1'b1;
end

else    SampleCtr <= SampleCtr + 1'b1;


if (Sampleen)  begin

        if (PCUCtr == 8'h00)   PCUctl <= PCU_default; //initial PCU state
        if (PCUCtr == INAon)          PCUctl[0] <= 1'b1;
        if (PCUCtr == INAoff)         PCUctl[0] <= 1'b0;
        if (PCUCtr == INAclk_p1)      PCUctl[1] <= 1'b1;
        if (PCUCtr == INAclk_p2)      PCUctl[1] <= 1'b0;
        if (PCUCtr == INAwarm_on)     PCUctl[2] <= 1'b1;
        if (PCUCtr == INAwarm_off)    PCUctl[2] <= 1'b0;
        if (PCUCtr == DACon)          PCUctl[6] <= 1'b1;
        if (PCUCtr == BRIDGEon1)      PCUctl[5] <= BridgeLong;
        if (PCUCtr == BRIDGEon2)      PCUctl[5] <= 1'b1;
        if (PCUCtr == BRIDGEoff)      begin
                PCUctl[5] <= 1'b0;
                PCUctl[6] <= 1'b0;
        end

        if (PCUCtr == PacketStart)    PCUctl[7] <= 1'b0;
        if (PCUCtr == ADCon)          PCUctl[3] <= 1'b1;
        if (PCUCtr == ADCoff)         PCUctl[3] <= 1'b0;
        if (PCUCtr == WarmP1)         PCUctl[4] <= 1'b0;
        if (PCUCtr == SampleTime) begin

        Sampleen <= FreeCtl;   //this forces SampleEn to 1 if FreeCtl is 1
        PCUctl <= PCU_default;
        end
        end
else    PCUctl <= PCUctl;
end
endmodule
```

11.5 Offset Removal HDL Code

```
module WIMM4_auto_offset(
          input mclk,
          input sample_sync,
          input [7:0] ADCIN,
          input reset,
          input auto,
          input FreeCtlIn,
          output reg CAL_EN,
          output wire FreeCtlOut,
         output [7:0] OS_val,
          output OS_range
```

```
);

wire over, under;
wire TooHigh;
wire [6:0] ADCInv;
reg [21:0] accum;
assign OS_val[7:0] = accum[20:13];
assign OS_range = accum[21];
assign FreeCtlOut = FreeCtlIn | CAL_EN;      //free_run signal goes to PCU to enable all circuitry, ignore CAL_EN if auto =1

//over/under lockout logic
assign over = ~&accum[21:8];    //over = 0 if accum too high
assign under = |accum[21:8];    //under = 0 if accum too low
assign ADCInv[6:0] = ~ADCIN[6:0];
assign TooHigh = |ADCIN[7:3];   //TooHigh = 0 if ADCIN is less than 8

wire test;
assign test = reset ? ~mclk : sample_sync;

reg [2:0] calctr;

always @ (posedge test)         begin
        if (reset)  begin
                    accum[21] <= 1'b0;              //IDAC in lower range

                    if (auto)   accum[20] <= 1'b1;              //nominal offset
                    else        accum[20] <= 1'b0;              //minimum offset

                    accum[19:0] <= 20'h000000;
        end

        else if (auto)          begin               //auto offset calculation
                    if  (ADCIN[7] && under)         accum <= accum - ADCIN[6:0];
                    else if (~ADCIN[7] && over)     accum <= accum + ADCInv[6:0];
                    else                    accum <= accum;     //default condition
        end

        else        begin               //in forced cal mode, only add ADC results, to drive the offset to zero
                    if (TooHigh && CAL_EN)          begin
                                accum <= accum + ADCIN[7:0];    //add ADC result only if it is greater than 8
                                calctr <= 3'h0;
                    end
                    else if (CAL_EN)        calctr <= calctr + 1;
                    else        begin
                                calctr <= 3'h0;
                                accum <= accum;     //default condition
                    end
        end
end

always @ (posedge mclk)         begin
        if (reset)              CAL_EN <= 1'b1;     //start a calibration on every power-up
        else if (calctr == 3'h7) CAL_EN <= 1'b0;
        else                    CAL_EN <= CAL_EN;
        end
endmodule
```

11.6 Activity Detector HDL Code

```
module wimm4_sig_detect(
        input Mclk,
        input sample_sync,
```

```
    input [5:0] sample_clks,
    input SampleStart,
    input TxRate,
    input TxCtl,
    input unsigned [7:0] sample_data,
    input SPICtl,
    input SPICompCtl,
    input [1:0] SPIThresh,
    input SPIreset,
    output reg TxEnable,
    output wire sig_detect
);

    wire reset;
    assign reset = SPIreset & SPICtl;

    parameter DefposThresh =  3'h3;       //FIR significance threshold
    parameter SPIposthresh0 = 3'h1;       //FIR threshold - SPI controlled
    parameter SPIposthresh1 = 3'h2;       //FIR threshold - SPI controlled
    parameter SPIposthresh2 = 3'h4;       //FIR threshold - SPI controlled
    parameter SPIposthresh3 = 3'h5;       //FIR threshold - SPI controlled
    parameter DefRate      = 3'h4;        //default Tx Rate if TxRate = 1

    reg [2:0] rate_control_reg;
    reg dec_latch;
    wire [2:0] rate_control;
    reg unsigned [6:0] FIR1;      //delay line, reg 1
    reg unsigned [6:0] FIR2;      //delay line, reg 2
    wire signed [8:0] FIRout;     //output of FIR
    reg [2:0] SPIposThresh;
    wire [2:0] DefThresh;
    wire signed [7:0] posthresh;
    wire signed [7:0] negthresh;
    wire compsel;
    reg FIRcomp;                  //FIR threshold comparator
    wire auto_tx;
    reg AutoTx_reg;
    wire auto_comp;
    assign auto_comp = AutoTx_reg | FIRcomp;
    assign compsel = SPICtl & SPICompCtl;
    assign sig_detect = compsel ? FIRcomp : auto_comp ;

    //perform FIR calculation using signed arithmetic
    assign FIRout = sample_data - FIR2 - FIR1;

    always @ (posedge sample_sync)        begin
           FIR1 <= sample_data[7:1];
           FIR2 <= FIR1;
    end

    always @ (posedge sample_sync)        begin

           if (FIRcomp)   begin
                  if (rate_control_reg != 3'h6)
                         rate_control_reg <= rate_control_reg + 1'b1;
                  else
                         rate_control_reg <= rate_control_reg;
           end

           else if ((dec_latch == 1'b1) && (sample_clks[4])) begin

                  if (rate_control_reg != 0)
                         rate_control_reg <= rate_control_reg - 1'b1;
                  else
                         rate_control_reg <= rate_control_reg;
           end

           else   rate_control_reg <= rate_control_reg; //FIRcomp is 0
```

```
        end

        always @ (posedge sample_sync)       dec_latch <= ~sample_clks[4];

        assign rate_control = TxRate ? DefRate : rate_control_reg;

        //SPI threshold decoder:
        always @ (*)   begin
               case (SPIThresh)
                      0:            SPIposThresh = SPIposthresh0;
                      1:            SPIposThresh = SPIposthresh1;
                      2:            SPIposThresh = SPIposthresh2;
                      3:            SPIposThresh = SPIposthresh3;
                      default:      begin
                             SPIposThresh = SPIposthresh0;
                      end
               endcase
        end

        assign DefThresh = DefposThresh;
        assign posthresh[2:0] = SPICtl ? SPIposThresh : DefThresh;
        assign posthresh[7:3] = 5'd0;
        assign negthresh = -posthresh;
        always @ (posedge sample_sync)       begin
               if (reset || TxRate)                  FIRcomp <= 1'b0;
        else if( FIRout >= posthresh )       FIRcomp <= 1'b1;
               else if ( FIRout <= negthresh )       FIRcomp <= 1'b1;
               else
        FIRcomp <= 1'b0;
        end

wire auto_clk1;
wire auto_clk2;
wire auto_clk3;
wire auto_clk4;
wire auto_clk5;

assign auto_tx = rate_control[2] ? auto_clk5 : auto_clk4;
assign auto_clk5 = rate_control[1] ? SampleStart : auto_clk3;
assign auto_clk4 = rate_control[1] ? auto_clk2 : auto_clk1;
assign auto_clk3 = rate_control[0] ? sample_clks[0] : sample_clks[1];
assign auto_clk2 = rate_control[0] ? sample_clks[2] : sample_clks[3];
assign auto_clk1 = rate_control[0] ? sample_clks[4] : sample_clks[5];

assign SDrst = ~(TxCtl);      //this signal rising edge should reset the SD output

reg buf_rst;
wire rst_posedge = (SDrst & ~buf_rst);
reg buf_auto;
wire auto_posedge = (auto_tx & ~buf_auto);

always @ (posedge Mclk)       begin
        buf_rst <= SDrst;     //finds SDrst pos edge
        buf_auto <= auto_tx;
end

reg TxEnable_test;
always @ (posedge Mclk)       begin
        if (rst_posedge)              AutoTx_reg <= 1'b0;
        else if (auto_posedge) AutoTx_reg <= 1'b1;
        else                          AutoTx_reg <= AutoTx_reg;
end

always @ (posedge Mclk)       begin
        TxEnable <= sig_detect;
end
endmodule
```

11.7 MATLAB ADC Spectral Analysis Code

```
clear all;

filename='INA_ADC_Gain11_2_832Hz_16_5_mVpp-12_30_2013-4_27_04 PM.dat';
format;

data = dat_import(filename, 'all');
data_adc = data;

fs = 500;
Tend = length(data)/fs;
time = [0:1/fs:Tend-1/fs];
data_ts = timeseries(data,time);
FilterPassInterval = [0.5 50];
data_smoothed = idealfilter(data_ts, FilterPassInterval , 'pass');

rows = floor(length(data_adc)/2);
data = data_adc(1:rows*2)';      %truncate data for reshape
data_r = reshape(data_adc,2,rows)';

data_adc = data_r(:,2);

rows = floor(length(data_adc)/5);
data = data_adc(1:rows*5)';      %truncate data for reshape
data_r = reshape(data_adc,5,rows)';
data_adc = data_r(:,3);
%create time vector:
fs = 100;
Fs = fs;
Tend = length(data_adc)/fs;
time = [0:1/fs:Tend-1/fs];

numpt = length(data_adc);   %number of samples
numsamp = numpt;

cycle = 29; %number of signal periods
fsig_in = 1/( numpt/cycle/fs)  % expected signal frequency using coherent sampling
n = 8;

bins = 0:1:(2^n)-1;

data_hist = hist(data_adc,bins);

figure(98);
subplot(2,1,1);
hold on;
stairs(time, data_adc);
%stairs(time, data_ideal,'-k');
title('SAR ADC Time-Domain Output Codes');
xlabel('Time (s)');
ylabel('Digital Code');
hold off;

subplot(2,1,2);
hist(data_adc,bins);
title('Histogram of SAR ADC Codes');
xlabel('Digital Code');
ylabel('Code Occurence');
axis([0 255 0 max(data_hist)]);

data_adc = data_adc - 128;

%Window the data:
numpt = 2^10;
numsamp = numpt;
fftsamp = 4;   %number of FFTs to average together - 6 seems to work best?
Dout_spect_array  = zeros(fftsamp,numpt);
```

```
ADC_PSD_array  = zeros(fftsamp,numpt);

bw = fs/2;
binwidth = fs / numpt; %bin width in Hz
fb = floor( bw / binwidth );     %bandwidth in bins
w=flattopwin(numpt,'symmetric');

start = 1;

for k = 1:fftsamp
    Doutw=data_adc(start:start+numpt-1).*w;
    Dout_spect_array(k,:) = fft(Doutw,numpt);  %Perform FFT
    ADC_PSD_array(k,:) = abs(Dout_spect_array(k,:)).*abs(Dout_spect_array(k,:));
    start = start+numpt+1;
end

Dout_spect = mean(abs(Dout_spect_array),1);  %average of FFT magnitudes
ADC_PSD = mean(ADC_PSD_array,1);        %average of PSDs

%Recalculate to dB
Dout_dB = 10*log10(ADC_PSD);

Dout_dB = Dout_dB - 83; %for flattop

fin = find(Dout_dB(6:(numpt/2))== max(Dout_dB(6:(numpt/2))));

figure(99);
plot([0:numpt/2-1].* (fs/numpt) , Dout_dB(1:numpt/2));
grid on;
xlabel('FREQUENCY (Hz)');
ylabel('AMPLITUDE (dB FULL SCALE)');
axis([0 Fs/2 -90 0]);

%Calculate SNR, SINAD, THD and SFDR values
span = floor( 6 + numpt/180 );
spanh=4;       %Approximate search span for harmonics on each side
spectP=(abs(Dout_spect)).*(abs(Dout_spect)); %Determine power spectrum
Pdc=sum(spectP(1:5)); %Find DC offset power
Ps=sum(spectP(fin-span:fin+span)); %Extract overall signal power
%Vector/matrix to store both frequency and power of signal and harmonics
Fh=[];
%The 1st element in the vector/matrix represents the signal, the next element represents
%the 2nd harmonic, etc.
Ph=[];

%Find harmonic frequencies and power components in the FFT spectrum
for har_num=1:10
%Input tones greater than fSAMPLE are aliased back into the spectrum
tone=rem((har_num*(fin-1)+1)/numpt,1);
if tone>0.5
%Input tones greater than 0.5*fSAMPLE (after aliasing) are reflected
tone=1-tone;
end
Fh=[Fh tone];
%For this procedure to work, ensure the folded back high order harmonics do not overlap
%with DC or signal or lower order harmonics
har_peak=max(spectP(round(tone*numsamp)-spanh:round(tone*numsamp)+spanh));
har_bin=find(spectP(round(tone*numsamp)-spanh:round(tone*numsamp)+spanh)==har_peak);
har_bin=har_bin+round(tone*numsamp)-spanh-1;
Ph=[Ph sum(spectP(har_bin-1:har_bin+1))];
end

%Determine the total distortion power
Pd=sum(Ph(2:10));
%Determine the noise power
Pn=sum(spectP(1:fb))-Ps-Pd-Pdc;

format;
SNDR=10*log10(Ps/(Pn+Pd))
```

```
SNR=10*log10(Ps/Pn)
PsigdB = 10*log10(Ps)
ENOB = (SNDR - 1.76)/6.02
```

11.8 Receiver Clock/Data Recovery Code

```
module wsd2cdr(mclk, slowclk, rst, inc, dec, inv, DataIn, cdrC, cdrD, lock, res);

        parameter ctr_init = 320;     //for 100-kHz
        parameter ctr_min = 140;      //further shifted by ctr_os
        parameter ctr_max = 380;      //further shifted by ctr_os
        input mclk,DataIn; // master clock and data bit stream
        input rst, inc, dec, slowclk, inv;

        reg [2:0] Dreg; // synchronized input data for deglitching

        reg lastD; // last cdrD, used to detect edges

        output cdrC;                  // recovered clock
        output cdrD;                  // buffered data
        output reg lock;              // lock status, 1 = CDR locked in
        output reg [3:0] res;  // residual of counter, for lock accuracy display

        //reg [N:1] ctr = 0; // MSB is recovered clock
        //reg [N:1] ctr_mod = 0;
        reg [9:0] ctr_mod = ctr_init;
        reg [7:0] ctr_os = 128;               //ctr offset value
        reg [3:0] loss_ctr = 0;
        reg [9:0] ctr = ctr_init;
        reg clk_en = 0;
        reg INVsel = 0;
        reg clkR = 0;  //recovered clock register controlled by code
        wire D;

        assign cdrC = clkR;
        assign cdrD = majority(Dreg[2],Dreg[1],Dreg[0]); // deglitched data
        assign D = INVsel ? DataIn : ~DataIn;

        always @ (posedge slowclk)    begin
                if (rst)                        ctr_os = 128;
                else if(inc && ctr_os < 255)  ctr_os = ctr_os + 1;
                else if(dec && ctr_os > 0)    ctr_os = ctr_os - 1;
                else                            ctr_os = ctr_os;

                if (inv)        INVsel = ~INVsel;
                else            INVsel = INVsel;
        end

        always @ (posedge mclk) begin
                lastD <= cdrD;
                Dreg <= (Dreg << 1) | D; // synchronized data

                if (rst)        begin
                        ctr_mod <= ( ctr_min + ctr_os + 20 );
                        ctr <= ( ctr_min + ctr_os + 20 );
                        clk_en <= 0;
                        clkR <= 0;
                end
                else if (lastD ^ cdrD) begin
                        //data change (edge) detected
                        clk_en <= 1;            //begin clock recovery
                        loss_ctr <= 0; //data reception resumed
                        lock <= 1;
                        clkR <= 0;              //recovered clock goes low
                        ctr <= ctr_mod + ctr_os;      // reset counter on data change
```

```
                        if (ctr > 24) begin
                                res <= 4'b0000;
                                if (ctr_mod > ctr_min) ctr_mod <= ctr_mod - 2;
                                else                                ctr_mod <= ctr_min;
                        end
                        else if (ctr > 8)       begin

                                if              (ctr < 12)      res <= 4'b0111;
                                else if (ctr < 18)      res <= 4'b0011;
                                else                            res <= 4'b0001;

                                if (ctr_mod > ctr_min) ctr_mod <= ctr_mod - 1;
                                else                                ctr_mod <= ctr_min;
                        end
                        else    begin
                                res <= 4'b1111;                     //best lock accuracy
                                ctr_mod <= ctr_mod;             //hold value
                        end
                end

                else if (ctr == 0) begin
                        clkR <= 0;
                        ctr <= ctr_mod+ctr_os;

                        if(clk_en)      begin
                                if (ctr_mod < ctr_max) ctr_mod <= ctr_mod + 1;
                                else                                ctr_mod <= ctr_max;
                                loss_ctr <= loss_ctr + 1;
                        end
                        else    begin
                                loss_ctr <= 0; //loss_ctr holds state
                        end
                end

                else begin
                        ctr <= ctr - 1;                 //decrement ctr if no data change
                        if (ctr == (( ctr_mod+ctr_os)>>1 ) ) clkR <= 1;
        end
                if (loss_ctr == 8) begin
                        if (ctr_mod > ctr_min + 12)
                                ctr_mod <= ctr_mod - 12;
                        else    ctr_mod <= ctr_min;

                        clk_en <= 0;    //halt clock recovery
                        loss_ctr <= 0; //loss_ctr holds state
                        lock <= 0;      //data lock lost
                end
        end

        function majority;
                input a,b,c;
                majority = a&(b|c) + b|c;
        endfunction

endmodule
```

CHAPTER 12

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