ELECTRICAL CHARACTERIZATION OF SiC JFET-BASED INTEGRATED CIRCUITS

by
CHIA-WEI SOONG

Submitted in partial fulfillment of the requirements
for the degree of Doctor of Philosophy

Dissertation Advisor: Prof. MEHRAN MEHREGANY

DEPARTMENT OF ELECTRICAL ENGINEERING AND
COMPUTER SCIENCE

CASE WESTERN RESERVE UNIVERSITY

January, 2014

CASE WESTERN RESERVE UNIVERSITY

SCHOOL OF GRADUATE STUDIES

We hereby approve the thesis/dissertation of

Chia-Wei Soong

candidate for the Doctor of Philosophy degree *.

Prof. Mehran Mehregany
(chair of the committee)

Prof. Pedram Mohseni

Prof. Swarup Bhunia

Prof. Mark De Guire

Date of Defense 10/25/2013

*We also certify that written approval has been obtained for any proprietary material contained therein.

To my parents

Table of Contents

TABLE OF CONTENTS ..... **I**

LIST OF TABLES ..... **IV**

LIST OF FIGURES ..... **VI**

ABSTRACT ..... **XIII**

1 INTRODUCTION **1**

1.1 Motivation and Objective **1**

1.2 Thesis Organization **3**

2 BACKGROUND AND LITERATURE REVIEW **5**

2.1 Temperature Effect on 6H-SiC Properties **5**

2.1.1 Bandgap energy and intrinsic carrier concentration 5

2.1.2 Mobile carrier concentration 7

2.1.3 Carrier mobility 8

2.1.4 Sheet resistance 9

2.1.5 Junction built-in potential 10

2.2 Review of Discrete Devices and Circuits in SiC Technology for High Temperature Applications **11**

2.2.1 Discrete SiC-based transistors 11

2.2.2 SiC-based logic circuits 12

2.2.3 Analog circuits in SiC technology 14

2.3 Junction Field Effect (JFET) Transistors and Integrated Circuits Fabricated at CWRU **16**

2.3.1 Fabrication process 16

2.3.2 JFET transistors modeling and characterization 18

2.3.3 Differential pairs and hybrid differential amplifiers 20

2.3.4 Design and characterization fully-integrated amplifiers 22

3 UNIFORMITY OF ELECTRICAL CHARACTERISTICS OF CWRU-FABRICATED DISCRETE JFETS **26**

3.2 On-State Parameter Measurement 28
3.2.1 Room temperature testing 28
3.2.2 High temperature testing 30
3.3 Off-State Parameter Measurement 32
3.4 Summary 34

4 6H-SIC CIRCUIT CHARACTERIZATION 36
4.1 Logic Circuits 36
4.1.1 Circuit design 36
4.1.2 Characterization of core inverter 37
4.1.3 Dynamic characteristics of NAND gate and NOR gate 41
4.2 Transimpedance Amplifier 42
4.2.1 Transimpedance amplifier characterization 43
4.2.1.1 Circuit design 43
4.2.1.2 Test results 46
4.2.2 Sensor interface capability 49
4.2.2.1 Variable capacitor calibration 49
4.2.2.2 High temperature test results 56
4.3 Summary 57

5 6H-SIC DEVICE CHARACTERIZATION 58
5.1 Noise Analysis of Integrated Amplifiers 58
5.1.1 Sources of noise in semiconductors 58
5.1.2 Noise in SiC-based devices 59
5.1.3 Test results 60
5.1.3.1 Single stage differential amplifier 62
5.1.3.2 Single-stage amplifier with resistor load 64
5.1.3.3 Two-stage amplifier with current source load in the 1st stage and resistive load in the 2nd stage 65
5.1.4 Discussion 67
5.2 P-N Junction Characterization of 6H-SiC JFET 68
5.2.1 Theory of p-n Junction 68

5.2.1.1 Thermal equilibrium 68
5.2.1.2 Forward bias 69
5.2.1.3 Generation-recombination process 69
5.2.1.4 High injection and series resistance 70
5.2.2 I-V characterizations of parasitic p-n diode 71
5.2.2.1 Room temperature test results 73
5.2.2.2 High temperature test results 77
5.2.2.3 Discussion 80
5.2.3 Parasitic BJT devices 81
5.2.3.1 Theory 81
5.2.3.2 I-V characterization results and discussion 83

6 4H-SIC JFET-BASED INTEGRATED CIRCUIT DESIGN 87
6.1 Temperature Effect of 4H-SiC Properties 88
6.2 Integrated Circuit Design 92
6.2.1 Logic circuits 93
6.2.1.1 Logic gates 93
6.2.1.2 SR Latch 94
6.2.2 Analog circuits 96
6.2.2.1 Single-stage differential amplifier with resistive load 96
6.2.2.2 Transimpedance amplifier 99
6.3 Summary 101

7 CONCLUSION AND FUTURE WORK 102
7.1 Conclusion 102
7.2 Future Work 104

BIBLIOGRAPHY 105

List of Tables

Table 2-1 Parameters values of Cauhey-Thomas equation for carrier mobility calculation. 9

Table 2-2 Summary of SiC-based logic gates 13

Table 2-3 Summary of SiC-beased amplifiers for high-temperature applications 15

Table 3-1 Statistical summary of JFET electrical parameters across a 2 inch diameter 6H-SiC wafer. 34

Table 3-2 Statistical summary of on-state parameters with JFET W/L = 100µm/100µm across a 2 inch diameter 6H-SiC wafer at elevated temperatures up to 280 °C. 34

Table 3-3 Statistical summary of on-state parameters with JFET W/L = 500µm/500µm across a 2 inch diameter 6H-SiC wafer at elevated temperatures up to 280 °C. 35

Table 4-1 DC performance metrics of the SiC inverter 40

Table 4-2 JFET sizes and biasing voltage for single-ended single-stage transimpedance amplifier. 44

Table 4-3 Resistor values for single-ended single-stage transimpedance amplifier. 44

Table 4-4 Table of measured output and expected output from the single-stage, single-ended transimpedance amplifier. 50

Table 5-1 Calculated saturation current (I_s) and ideality factor (η) of three copies of devices with junction area of 1×10^{-4} cm^2 74

Table 5-2 Calculated saturation current (I_s) and ideality factor (η) of three copies of devices with junction area of 2.5×10^{-3} cm^2 75

Table 5-3 Measured current gain with different device size at I_B = 205 µA and V_{EC} = 40V. 85

Table 6-1 Comparisons of selected electrical properties between 4H- and 6H- SiC at 300K [71]. 87

Table 6-2 Designed parameters of channel epi-layer and its important electrical properties in 4H- and 6H- SiC technology. 89

Table 6-3 JFET sizes and biasing voltage for single-stage amplifier with resistive load. 97

Table 6-4 Resistor values for s single-stage amplifier with resistive load. 97

Table 6-5 Simulated gain and supply current at three different operating temperatures. 98

Table 6-6 JFET sizes and biasing voltage for single-ended single-stage transimpedance amplifier. 100

Table 6-7 Resistor values for single-ended single-stage transimpedance amplifier. .. 100

Table 6-8 Simulated gain and supply current at three different 101

List of Figures

Figure 1-1 A simplified block diagram of a capacitive sensor measurement system. . 2

Figure 1-2 SiC sensor module for harsh environment application [10]. 2

Figure 2-1 Temperature dependence of calculated 6H-SiC bandgap energy. 5

Figure 2-2 Temperature dependence of 6H-SiC intrinsic carrier concentration [2]..... 6

Figure 2-3 Energy band diagram for n-type 6H-SiC [12]. 7

Figure 2-4 Temperature dependence of calculated mobile carrier concentration in 6H-SiC..... 8

Figure 2-5 Temperature dependence of calculated electron mobility in 6H-SiC..... 9

Figure 2-6 Temperature dependence of calculated sheet resistance in 6H-SiC. 10

Figure 2-7 Temperature dependence of calculated p-n junction built-in potential in 6H-SiC. 11

Figure 2-8 Schematic cross-section of the JFET structure [35]. 16

Figure 2-9 SEM of a JFET with W/L = 100µm/10µm [35]. 18

Figure 2-10 Comparison of measured and modeled drain current characteristics for JFETs with W/L = 100µm/100µm up to 595 ^{o}C [37]. 19

Figure 2-11 (a) Schematics, and (b) SEM image of a differential pair with W/L = 110 µm/10µm SiC JEFTs [10]..... 20

Figure 2-12 (a) DC characteristics, and (b) transconductance of a differential pair with W/L = 100µm/10µm [10]. 21

Figure 2-13 Circuit schematic of a hybrid two-stage differential amplifier with active loads [33]. 21

Figure 2-14 Measured AC response of the hybrid amplifiers at room temperature and at 450 ^{o}C [33]..... 22

Figure 2-15 Schematic of (a) Single-stage differential amplifier with passive loads , and (b) two-stage differential amplifier with current source loads in 1st stage and resistor loads in 2nd stage [5]. 23

Figure 2-16 Measured voltage gain of the two-stage differential amplifier with current source loads in the 1st stage and resistor loads in the 2nd stage at various temperatures [5]. 24

Figure 2-17 Schematic of a single-stage and single-ended transimpedance amplifier [10]..... 25

Figure 2-18 The measured frequency response of the transimpedance amplifier from two copies on the same die at room temperature [10]. 25

Figure 3-1 Yield map of JFETs on the 2 inch-diameter 6H-SiC wafer..... 27

Figure 3-2 JFETs with W/L = 100µm/100µm: (a) V_{TH}; and (b) I_{DSS}. The box width is proportional to the sample size. The bottom and top of the box represents 25^{th} and 75^{th} percentile of the data. The band and the cross inside the box are the median and mean, respectively. 29

Figure 3-3 Box plots of measured (a) V_{TH}; and (b) I_{DS} of JFETs with W/L = 100µm/100µm at 100 °C and 280 °C. 31

Figure 3-4 JFETs with W/L = 100µm/100µm: (a) I_{GSS}; and (b) I_{OFF}. 33

Figure 4-1 Circuit Schematics of 6H-SiC (a) inverter, (b) NAND and (c) NOR gates.. 36

Figure 4-2 Optical micrograph of fabricated 6H-SiC JFETs based NOR. 37

Figure 4-3 VTC of the SiC inverter at (a) 25 ºC and (b) elevated temperatures. All experiments were conducted in an ambient environment with V_{sub} = 0 V, V_{DD} = +14 V and V_{SS} = -14 V. 39

Figure 4-4 Supply Current with temperature dependence at (a) low output level and (b) high output level. 40

Figure 4-5 Measured dynamic characteristics of SiC NAND gate and NOR gate at 25 ºC and 550 ºC with V_{sub} = 0 V, V_{DD} = +14 V and V_{SS} = -14 V. 41

Figure 4-6 Generic sensor interface circuit for capacitive sensors [44]. 42

Figure 4-7 Schematic of a single-ended, single-stage transimpedance amplifier. 44

Figure 4-8 Optical microphotograph of the single-ended, single-stage transimpedance amplifier 45

Figure 4-9 Schematic of the transimpedance amplifier test setup. 46

Figure 4-10 Measured frequency response of a single-stage, single-ended transimpedance amplifier (CR0975-10-R6C6) at elevated temperature with V_{DD} = 20 V, V_{SS} = V_{sub} = -10 V, V_{bias} = -2 V, and I_{in} = 1 µA. 47

Figure 4-11 Measured supply current of a single-stage, single-ended transimpedance amplifier (CR0975-10-R6C6) at elevated temperature 48

Figure 4-12 Calibration of variable capacitor: screw positions and corresponding values 49

Figure 4-13 Single-stage, single-ended transimpedance amplifier output vs. input ΔC at room temperature. 50

Figure 4-14 Measured output of the transimpedance amplifier with 1 *k*Hz stimulus signal. V_{DD} = 20 V, V_{ss} = -10 V, V_{bias} = -2 V, and five adjustment screw positions. 53

Figure 4-15 Measured output of the transimepedance amplifier vs. different frequency of stimulated signal. V_{DD} = 20 V, V_{ss} = -10 V, V_{bias} = -2 V, and ΔC = max. 54

Figure 4-16 Gain sensitivity to (a) positive and (b) negative power supply voltages with $V_{DD,nom}$ = 20V, $V_{SS,nom}$ = -10V, V_{bias} = -2 V, and ΔC = max. 55

Figure 4-17 Measured and expected output of transimpedance amplifier output at elevated temperatures..... 56

Figure 5-1 Noise spectra at 25 °C of a 6H-SiC JFET device under different bias condition [50]..... 60

Figure 5-2 Differential pair circuit including input-referred noise model..... 61

Figure 5-3 Test setup for noise measurement of SiC-based amplifiers..... 62

Figure 5-4 Output-referred noise voltage of a differential-pair at room temperature. 63

Figure 5-5 Output-referred noise voltage of a differential pair at elevated temperatures..... 63

Figure 5-6 Output-referred noise voltage of a single-stage amplifier with resistor loads at elevated temperatures. 64

Figure 5-7 Output-referred noise voltage of a two-stage amplifier with current source load in the 1st stage and resistor load in the 2nd stage. 66

Figure 5-8 output-referred noise voltage of a two-stage amplifier with current source load in the 1st stage and resistor load in the 2nd stage. 67

Figure 5-9 P-n junction in thermal equilibrium (without bias)..... 68

Figure 5-10 I-V characteristics of a silicon diode [13]..... 71

Figure 5-11 Setup of parasitic p-n diode I-V characteristics..... 72

Figure 5-12 Measured forward-biased I-V characteristics from three copies of devices with junction area of 1×10^{-4} cm^2 at room temperature. 74

Figure 5-13 Measured forward-biased I-V characteristics from three copies of devices with junction area of 2.5×10^{-3} cm^2..... 75

Figure 5-14 Measured reverse-biased I-V characteristics from three copies of devices with junction area of (a) 1×10^{-4} cm^2 and (b) 2.5×10^{-3} cm^2. 76

Figure 5-15 Measured forward-biased I-V characteristics of a device with junction area of 1×10^{-4} cm^2 at elevated temperatures..... 78

Figure 5-16 Arrhenius plot showing temperature dependence of saturation current with calculated activation energy EA = 1.21 eV. 78

Figure 5-17 Measured reverse-biased I-V characteristics of a device with junction area of 1×10^{-4} cm^2 at elevated temperatures..... 79

Figure 5-18 The calculated generation component of reverse current of our SiC p-n junction as function of temperature. 80

Figure 5-19 A vertical p-n-p BJT structure in our JFET device..... 82

Figure 5-20 A test setup for I-V characteristics measurement in BJT operation mode. 83

Figure 5-21 DC I-V characteristics of (a) 100µm/100µm, and (b) 500µm/500µm devices..... 84
Figure 6-1 Temperature dependence of calculated 4H-SiC bandgap energy. 88
Figure 6-2 Temperature dependence of calculated mobile carrier concentration in 4H-SiC..... 90
Figure 6-3 Temperature dependence of calculated electron mobility in 6H-SiC..... 91
Figure 6-4 Temperature dependence of calculated sheet resistance in 4H-SiC. 91
Figure 6-5 Schematic cross-section of the JFET structure in 4H-SiC technology. 92
Figure 6-6 Schematic of 4H-SiC JFET-based (a) inverter, (b) NAND, and (c) NOR gate. 93
Figure 6-7 Simulated VTC of the 4H-SiC inverter at three different operating temperatures. 94
Figure 6-8 Schematic of (a) NOR latch and (b) NAND latch. 94
Figure 6-9 Simulated transient characteristics from 4H-SiC (a) NAND, and (b) NOR latch at room temperature. 95
Figure 6-10 Simulated DC response of the single-stage differential amplifier with resistive load at (a) room temperature (b) 427 ºC with V_{DD} =30V, V_{SS} = -6V..... 97
Figure 6-11 Simulated AC response of the single-stage differential amplifier with resistive load at three operating temperatures with V_{DD} = 30 V, V_{SS} = -6 V. 98
Figure 6-12 Schematic of 4H-SiC single-ended single-stage transimpedance amplifier. 99
Figure 6-13 Simulated AC response of the single-ended single-stage transimpedance amplifier with resistive load at three operating temperatures with V_{DD} = 30 V, V_{SS} = -6 V. 100

Acknowledgement

In the first twenty years of my life, Ph.D. was never an option in my future plan. However, now I am so grateful for having this opportunity and going through this long journey. Completing this degree has become one of the most valuable experiences in my life.

My gratitude first goes to my advisor, Professor Mehran Mehregany, a mentor with vision and support. He is also a person full of sense of humor, wisdom, and energy. He provides necessary advice, at the mean time, lets students explore their own research interests. He always tells us to examine for all possibilities and opportunities, to be enthusiastic, and to be proactive—both in life and career. Without his encouragement, I would never have had the opportunity to join a doctoral program, and I would never have known what I had missed.

I would also like to express my great appreciation to the late Professor Steven Garverick. Even though I was not in his group, he was always willing to spend time discussing my research in detail and provide tremendous input for my project. I would not have been able to complete this thesis without his guidance. He was always humble, always patient, and will be missed deeply.

Many kind thanks to Professors Mark De Guire, Swarup Bhunia and Pedram Mohseni for agreeing to serve on my thesis committee. Thanks also go to Dr. Xiao-An Fu (previously with Mehregany Lab and now a faculty at the Chemistry Department of the University of Louisville) and Dr. Amita Patil (previously with Mehregany Lab and now with GE Research Laboratories). Dr. Patil designed and completed the layout of the devices and circuits studied here, as well as performed initial characterizations of

fabricated devices and circuits. Dr. Fu fabricated the wafers and also characterized the fabrication process diagnostic devices.

Here in Cleveland, I shared the most wonderful, the most frustrated, the most self-questioned, the most depressed, and the most fun moments with all my lovely friends inside and outside the EECS department.

I would like to thank the members of Mehregany Lab, especially Hari Rajgopal and Chia-Hua Lin. Hari is a great colleague and friend. He is knowledgeable—basically the human-version of a search engine tool. He is always willing to help others no matter how busy he is at the time. Chia-Hua Lin is the type everyone would like to have around an office; he is a funny and always able to make us laugh. I deeply appreciate his support and friendship in the past five years.

Thanks you my EECS friends—Amita Patil, Dan Howe, Bobby Lu, Peng Wang, Kanokwan Limnuson, Dan Goff, Steve Majerus, Tina He, Jaesung Lee, Andrew Barnes, Di Sun, and many others—for help, discussions, and most importantly, friendship. My graduate student life was more rich and fun because of you.

Staying away far from home is never easy for international students; however, it turned out not to be that difficult because of a lot of sweet friends. I feel so blessed to have you and your love around me. You—I-Jung Feng, Andrew Lin, Victoria Chou, May Wang, Sandy Gu, Frank Hsu, Stephanie Liu, Daniel Lee, Kate Chou, Lee Rivera, Kuan-Lin Lee, Josephine Ma, Wilson Kao, Monica Wu, Kevin Kuo, Pin-Ann Lin, Rachel Liang, and Ting-Jung Chen—are the reason that Cleveland feels like my second home now. Our friendship is the most valuable asset along my journey. I would love to express my special thank to Yating Liao and James Liao; because of their kindness and

hospitality, I stayed with them in the last six months of my graduate life, which made everything much easier for me. It is a great privilege to spend eight years in such a lovely city with a group of wonderful people. I am so grateful for sharing this life experience with you.

It is great to know that my friends in Taiwan—especially Tina Yiu, Brenda Chen, Joy Lin, and Amanda Liu—waiting for my return. It is your love and support that I have also relied on while in Cleveland. Also, I would not have been able to go through this period without the great patience of my fiancé, Chang-Wen Hsieh.

Last but not least, I would like to take this opportunity to thank my parents. I become who I am today because of their unconditional love and support. They have always encouraged me to pursue my life dreams and are always there for me.

This work was partially supported by Defense Advanced Research Projects Agency (DARPA) under grants # NBCH2050002.

Electrical Characterization of 6H-SiC JFET-based Integrated Circuits

Abstract

by

CHIA-WEI SOONG

6H-SiC, n- channel, depletion-mode JFET-based devices and integrated circuits for high temperature sensing applications have been studied extensively in this dissertation. To further understand the performance of basic integrated circuit building blocks at the wafer-scale, as well as the limitations of 6H-SiC technology, key electrical parameters of various devices have been studied from room temperature up to 600 °C. Integrated circuits, including digital logic gates and analog amplifiers, have also been demonstrated at elevated temperatures, the latter enabling sensor interface capability.

A uniformity study of 229 JFETs' on- and off-state parameters across a 2 inch-diameter wafer, consisting of varying W/L ratios within each die, showed an overall yield of ~93%. The coefficient of variance for the measured on-state parameters was relatively small at tested operating temperatures from room to 280 °C; it did however increase with the die distance from the wafer center. Orders of magnitude variations in the off-state gate reverse current at room temperature suggests poor uniformity of crystalline quality across the wafer. Off-state drain leakage current also exhibited large variations across the wafer. Nevertheless, an on/off current ratio > 182 was seen across the wafer at 280 °C.

The 6H-SiC core inverter has an outstanding DC characteristic transfer function with a steep slope, including a gain > 20 from room temperature to 500 °C, and a logic threshold well centered in the logic swing. NOR and NAND gates were likewise tested in this temperature range, with the measured dynamic characteristics presented.

A high-temperature, fully monolithic, high gain-bandwidth 6H-SiC transimpedance amplifier for capacitive sensor interfacing was tested. The amplifier demonstrated a gain of 235 kΩ and a bandwidth of 0.61 MHz at room temperature. The gain and bandwidth were 774 kΩ and 0.17 MHz at 450 °C, respectively. Results from measurements with variable capacitors—simulating sensor capacitance—confirmed differential capacitive sensing at room operating temperatures to 450 °C.

The voltage noise performance of integrated differential amplifiers fabricated in this process was studied from room temperature to 500 °C. A noise dependence of $1/f^{\gamma}$ (where $1<\gamma<2$) was seen across different types of differential amplifiers. A universal noise behavior was not observed in the differential amplifiers, even among the same circuit topology, which suggests the existence of defects in the epitaxial layer or substrate.

Parasitic p-n diodes were investigated, and the I-V characteristics were found to vary from sample to sample. A well-behaved p-n junction was further characterized, and an ideality factor of 2 with a thermal activation energy of 1.21 eV was shown, which suggests generation-recombination current dominance.

Due to the superior material properties of 4H-SiC over 6H-SiC and the non-availability of 6H-SiC wafers, a process technology conversion from 6H- into 4H-SiC is suggested, including initial simulations of enhanced circuit performance expectations.

1 Introduction

1.1 Motivation and Objective

Silicon carbide (SiC) is widely recognized as a promising material for electronics for harsh environment applications due to its superior electrical and physical characteristics [1-2]. Conventional silicon-based electronics usually fail at temperatures above 250 ºC, and require cooling systems and control circuits for functionality in such harsh environments. These additional control and cooling systems increase cost, introduce noise, consume energy and increase real estate use. Therefore, interest in high temperature sensor and interface electronics has been increasing, particularly in aerospace, automotive and other high-operating-temperature industrial systems [3-4].

A simplified block diagram of a sensor measurement system is shown in Figure 1-1. The amplifier is designed to convert the small sensed signal to current or voltage. The amplifier must provide a reasonable gain across a wide temperature range, and the in-band noise must be carefully designed, since it is the major noise source in the system and limits the sense input signal level. The front-end amplifier is followed by an analog-to-digital converter to convert the voltage or current to a digital signal for further data processing.

Ultimately, the goal is to develop a sensor module with MEMS-based sensors integrated with SiC interface circuits for high-temperature operation as shown in Figure 1-2. To this end, researchers at CWRU have successfully designed and fabricated a family of n- channel depletion-mode JFET-based integrated circuits for high temperature sensing applications using 6H-SiC technology [5]. However, only selected circuits have been previously tested at high temperature. In order to develop a better understanding of

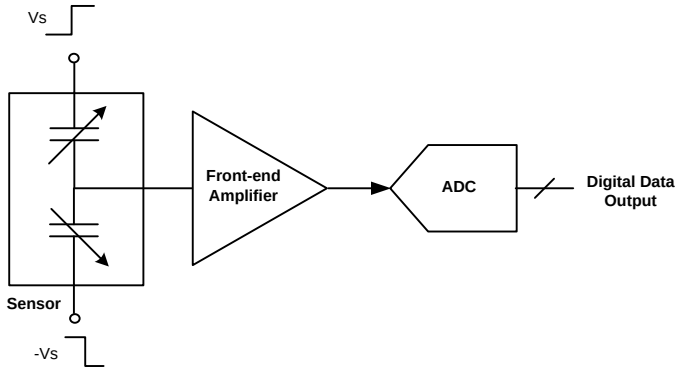


Figure 1-1 A simplified block diagram of a capacitive sensor measurement system.

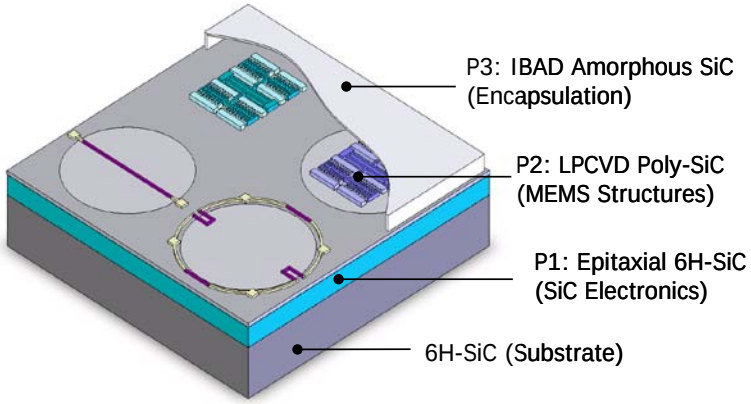


Figure 1-2 SiC sensor module for harsh environment application [6].

the technology, additional electrical characteristics of the discrete devices and integrated circuits are studied in this work, including:

1. **Yield and uniformity of the discrete JFETs:** According to Cree, Inc., the wafer manufacturer, there are variations of 50% in the doping concentration and 10% in thickness of 6H-SiC epitaxial layers [7]. Process variations directly impact the fundamental performance of transistors. Thus, a uniformity study provides (i) a better understanding of the basic integrated circuit building blocks for wafer-scale fabrication and (ii) elucidates the available flexibility in design parameters;

2. **Circuit characterization:** basic logic gates and transimpedance amplifier were not characterized previously. These circuits are characterized to demonstrate control and sensing capability for high temperature applications. The demonstration of a high-temperature-capable, integrated SiC-based capacitive sensing integrated circuit is a significant achievement.

3. **Device characterization:** Noise behavior of selected integrated circuits and parasitic p-n diode I-V characteristics is studied. The noise study helps to understand the lower limit of sense signal level of the integrated circuits. Although not optimized for practical applications, characterization of the parasitic p-n diodes may provide more information on leakage current, which increases with temperature and (eventually) causes failure of operation and/or undesirable power dissipation [8].

4. **Technology conversion:** the move to 4H-SiC from 6H-SiC technology in the power device industry and the consequent lack of availability of 6H-SiC wafers necessitates circuit redesign from 6H-SiC to 4H-SiC wafers. With larger bandgap, lower intrinsic carrier concentration and higher carrier mobility over 6H-SiC, device and circuit performance improvements are expected in 4H-SiC technology. Selected circuits are redesigned and simulated to demonstrate the benefits from this technology conversion.

1.2 Thesis Organization

This thesis is organized into seven chapters. Chapter 2 gives a brief introduction about the state-of-the-art of SiC-based devices and circuits for high temperature sensing applications. A study of yield and uniformity study of the discrete JFETs across a 2 inch-diameter wafer at operating temperature up to 280 °C is presented in Chapter 3. Chapter 4 presents characterization of the integrated circuits, including digital logic gates and

analog transimpedance amplifier, across a wide temperature range. Chapter 5 presents noise analysis of the integrated amplifiers, as well as the I-V characteristics of parasitic p-n diodes at elevated temperatures. A process technology conversion from 6H-SiC into 4H-SiC is demonstrated in Chapter 6, using select integrated circuits as design examples. Finally, the key achievements of this work are summarized in Chapter 7, along with suggestions for future work.

2 Background and Literature Review

2.1 Temperature Effect on 6H-SiC Properties

2.1.1 Bandgap energy and intrinsic carrier concentration

The wide bandgap energy (E_g) and low intrinsic carrier concentration (n_i) are the fundamental advantages that make SiC a superior material for high temperature application over Si. The band-gap energy of 6H-SiC as a function of temperature is given by [9]

$$E_g(T) = 3 - 3.33 \times 10^{-4}\,(T - 300K)\text{eV}. \tag{2.1}$$

Figure 2-1 shows the relationship between calculated bandgap energy and temperature.

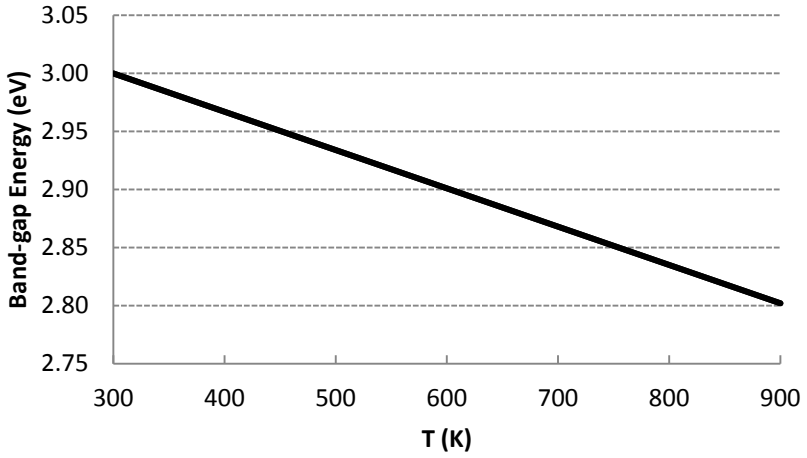


Figure 2-1 Temperature dependence of calculated 6H-SiC bandgap energy.

The intrinsic carrier concentration in 6H-SiC is determined by the bandgap energy and the effective density -of-states masses [10]:

$$n_i(T) = 2\left(\frac{kT}{2\pi\hbar^2}\right)^{3/2}(m_c m_v)^{3/4} e^{\frac{-E_g(T)}{2kT}}, \tag{2.2}$$

where $k = 8.62 \times 10^{-5}\ eV/K$ is the Boltzmann constant, $\hbar = 4.135 \times 10^{-15}$ eV is the reduced Plank's constant, m_C and m_V are the effective density-of-state masses for the conduction and valence band, respectively. Figure 2-2 shows the intrinsic carrier concentration increases as temperature increases. At 227 ^{o}C, the intrinsic carrier concentration in Si reaches 10^{15} cm^{-3}, close to lightly doped extrinsic dopant level. As such, the lightly doped regions become influenced by the intrinsic level and fail to operate. On the contrary, even at 600 ^{o}C, the intrinsic carrier concentration of 6H-SiC is only around 10^{12} cm^{-3}, far lower than the extrinsic dopant level that enables the operation of SiC devices at high temperatures.

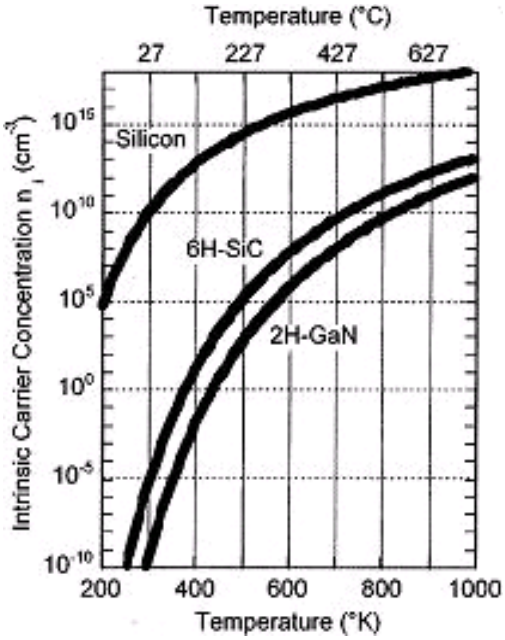


Figure 2-2 Temperature dependence of 6H-SiC intrinsic carrier concentration [2].

2.1.2 Mobile carrier concentration

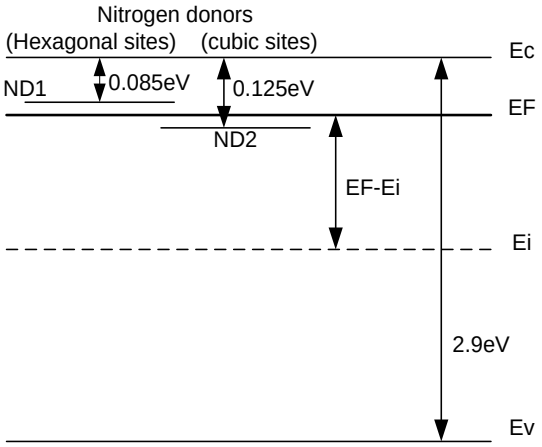


Figure 2-3 Energy band diagram for n-type 6H-SiC [9].

As shown in Figure 2-3, there are two donor levels in n-type 6H-SiC that determine the carrier concentration (n) in the semiconductor.

$$n_i\, exp\left[\frac{E_F - E_i}{kT}\right] = N_{D1}\left[1 - \frac{1}{1 + \frac{1}{g}\exp\left(\frac{E_{D1}-E_F}{kT}\right)}\right] + N_{D2}\left[1 - \frac{1}{1 + \frac{1}{g}\exp\left(\frac{E_{D2}-E_F}{kT}\right)}\right] + n_i ex\, p\left[\frac{E_i - E_F}{kT}\right], \quad (2.3)$$

where N_{D1} and N_{D2} are doping concentration for shallow and deeper level, respectively [10]. Figure 2-4 illustrates the mobile carrier concentration versus temperature with the impurity density of 10^{17} cm^{-3}. At room temperature, only 39% of the dopants are ionized and 90% at 200 ^{o}C.

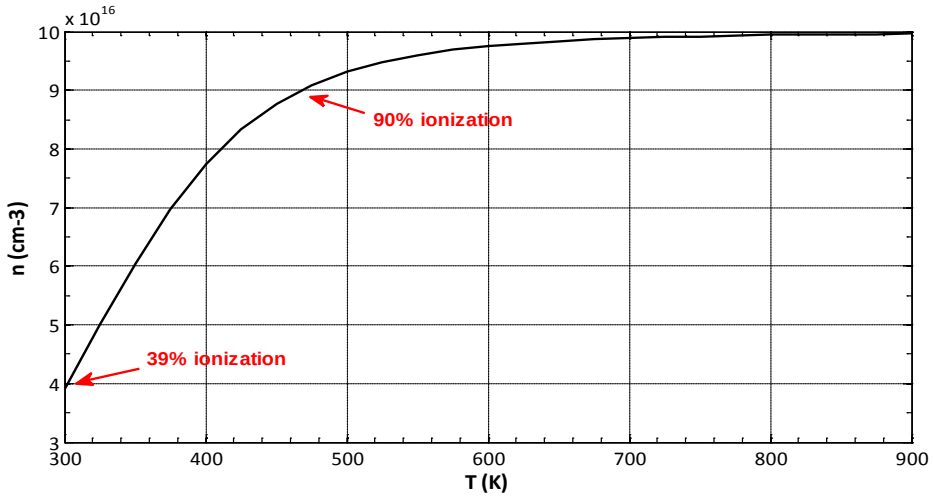


Figure 2-4 Temperature dependence of calculated mobile carrier concentration in 6H-SiC.

2.1.3 Carrier mobility

The low-field electron mobility (μ_n) is modeled by the Caughey-Thomas equation [9] as

$$\mu_n = \mu_{n,p}^{min} + \frac{\mu_{n,p}^{delta}}{1 + \left(\frac{N_D + N_A}{N_{n,p}^{\mu}}\right)^{\gamma_{n,p}}} \left(\frac{T}{300K}\right)^{\alpha_{n,p}}, \tag{2.4}$$

Table 2-1 summarizes the numbers for calculation of carrier mobility. It is noticeable that hole mobility is much smaller than electron mobility at temperature range of interest here, leading to a lower transconductance for comparable p-type JFETs. Thus, only n-type JFETs are pursed here.

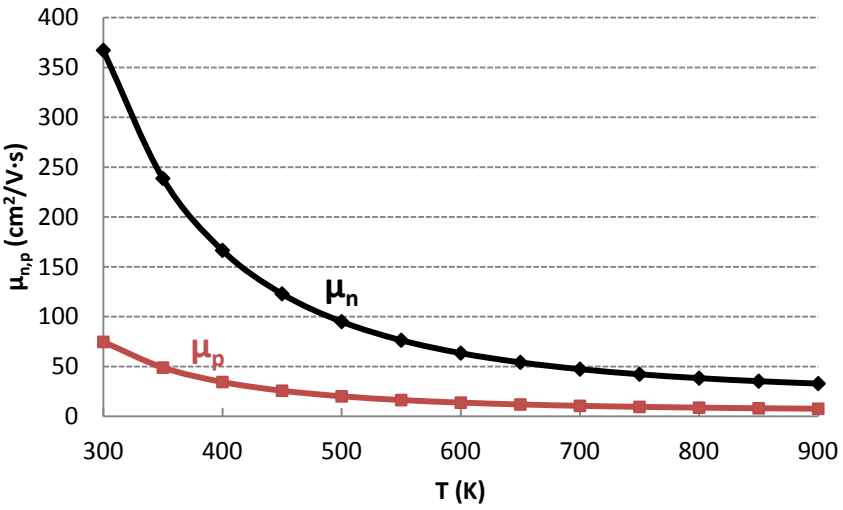


Figure 2-5 Temperature dependence of calculated electron mobility in 6H-SiC

Table 2-1 Parameters values of Cauhey-Thomas equation for carrier mobility calculation.

	μ^{min} (cm^2/Vs)	μ^{delta}(cm^2/Vs)	N^{μ}(cm^{-3})	γ	α
Electron (n-type)	20	380	4.5×10^{17}	0.45	-3
Hole (p-type)	5	70	1×10^{19}	0.5	-3

2.1.4 Sheet resistance

Sheet resistance is given by

$$R_{sh} = \frac{1}{q\mu_{n,p}nD}, \tag{2.5}$$

where D is the epi layer thickness. In this project, the resistors and transistors are fabricated in the n-type channel epi layer; Figure 2-6 shows the relationship between sheet resistance and temperature for D = 0.3μm.

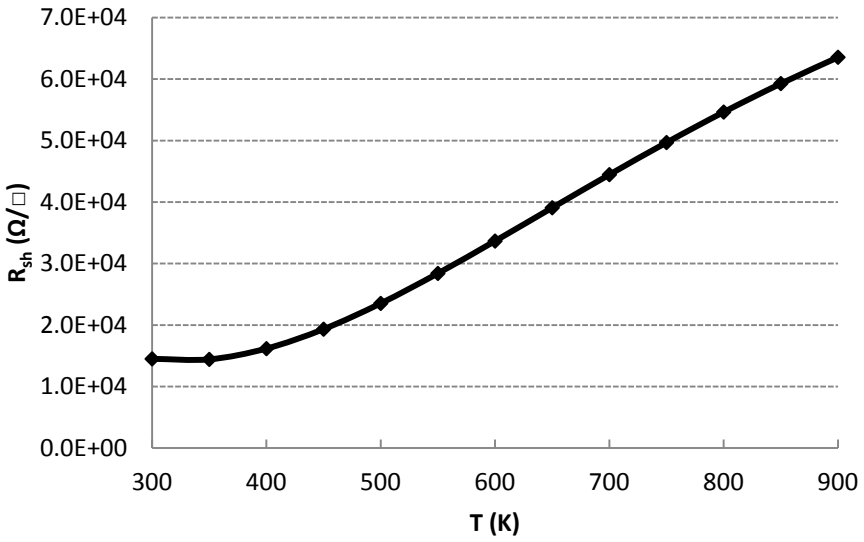


Figure 2-6 Temperature dependence of calculated sheet resistance in 6H-SiC.

2.1.5 Junction built-in potential

At thermal equilibrium, the electrostatic potential difference between the p-n neutral regions is called built-in potential (V_{bi}) and is given by [10]

$$V_{bi} = \frac{KT}{q} \ln \frac{N_A N_D}{{n_i}^2}, \tag{2.6}$$

With $N_A = 10^{17}$ cm^{-3} and $N_D = 10^{19}$cm^{-3}, at room temperature the built-in potential in 6H-SiC is 2.88V, while it is generally ~ 0.75V in Si p-n junction.

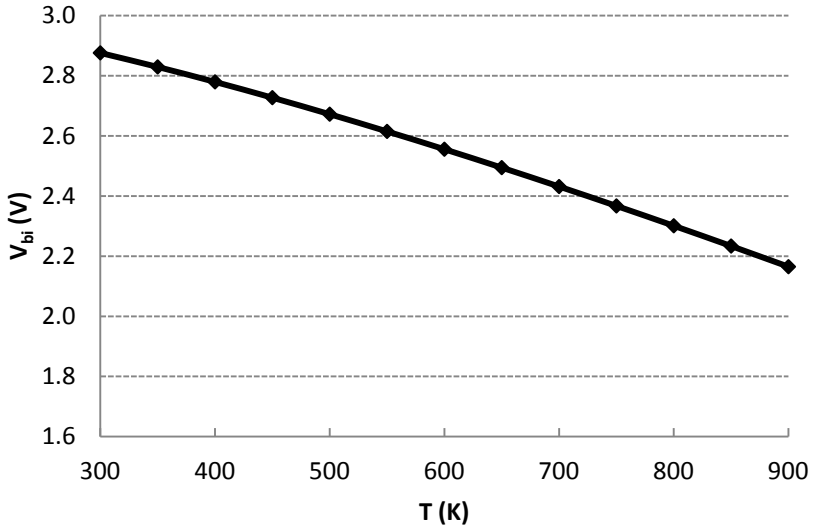


Figure 2-7 Temperature dependence of calculated p-n junction built-in potential in 6H-SiC.

2.2 Review of Discrete Devices and Circuits in SiC Technology for High Temperature Applications

2.2.1 Discrete SiC-based transistors

Discrete SiC devices have been modeled across a wide temperature range: A non-IC compatible n-channel 6H-SiC JFET is modeled up to 500 ºC using standard abrupt-junction long-channel JFET device equations [9]. An IC-compatible, n-channel 6H-SiC JFET is modeled up to 400 ºC incorporating substrate effect [11]. 6H-SiC MOSFET modeling up to 300 ºC is reported in [12] for analog IC design. A successful IC-compatible MOSFET model with only 1-2% error in DC characteristics is reported up to 300 ºC in [13].

The fabricated MOSFET in [12] shows large variation of threshold voltage above 200 ºC, thus limiting operation at high temperature. A fabricated 6H-SiC JFET with low leakage current (< 10pA) under room temperature is presented in [14]; the JFET was

tested up to 400 ºC and showed ~ 60% reduction in transconductance (g_m) and saturation drain current (I_{DSS}). A SiC MESFET is fabricated in [15] and tested at 500 ºC for 500 hours continuously; it exhibited < 10% variation of transistor parameters. However, the gate leakage current is ~ 80 µA at 500 ºC. A 6H- SiC JEFT is fabricated and tested at 500 ºC for 3007 hours, and demonstrates stable operation at high temperatures [4].

2.2.2 SiC-based logic circuits

SiC-based logic integrated circuits (ICs) have been previously demonstrated using JFETs [4], [16], BJTs [17] and MOSFETs [18-19]. The BJT circuits provided significantly better electrical performance at room temperature, but degraded rapidly at operating temperatures above 300 ºC. The MOSFET circuits operated to just 300 ºC. SiC integrated logic gates using BJTs [20-21] have been reported to show outstanding noise margins, as well as high-speed performance for temperatures as high as 355 ºC. The same seems to be the case up to 400 ºC using MOSFETs [22]. A MOSFET-based 4-bit counter and flip-flop have been demonstrated up to 300 ºC [23]. While most logic circuits seem to degrade at higher temperature, BJT-based logic gates show a stable noise margin, ~ 1V, up to 500 ºC [24]. A summary of integrated logic gate using SiC technology is listed in Table 2-2.

Table 2-2 Summary of published work on SiC-based logic gates

Authors	Devices	Max Operation Temperature (ºC)	Description
Neudeck [4]	JFET	500	NOR gate, Long-term testing for 2000 hours, -13.6% change in V_{OH} <1% change in V_{OL}
Lee [17]	BJT	300	TTL circuits with fan-out of ten, At 300 ºC, 25% change in V_{NML}* and V_{NMH}**
Schmid [18]	MOSFET	300	Inverter and 17-stage ring oscillators
Ryu [19]	MOSFET	300	CMOS technology, Variety of logic gates exhibited stable operation up to 300 ºC
Lanni [20]	BJT	300	ECL OR-NOR gate, Stable noise margin ~ 1V across tested temperature
Singh [21]	BJT	355	TLL gate, Limited operation at high temperature due to metallization
Le-Huu [22]	MOSFET	400	Inverter and flip-flop
Patil [23]	MOSFET	300	4-bit Counter, Stable operation for 300 hours at 300 ºC
Lanni [24]	BJT	500	OR/NOR gate, Stable noise margin ~ 1V across 0 ºC – 500 ºC

* V_{NML} (noise margin for low level) = V_{IL}-V_{OL}
** V_{NML} (noise margin for low level) = V_{OH}-V_{IH}

2.2.3 Analog circuits in SiC technology

Table 2-3 lists published work on SiC-based amplifiers for high-temperature applications. A hybrid SiC MESFET-based differential amplifier is presented in [25]. A voltage gain of 61 dB, common mode rejection ratio (CMRR) of 60 dB, gain bandwidth (GBW) of 0.91 MHz and power dissipation of 178 mW are reported at 350 ºC. An operational amplifier using NMOS with a voltage gain of 53 dB and GBW of 269 kHz at 300 ºC is reported in [26]. Later, A CMOS-based IC-compatible operational amplifier is reported in [27], which shows a voltage gain ~80 dB and GBW of 571 kHz at 300 ºC. An integrated differential amplifier in JFET technology demonstrated long-term (i.e., 3007 hours) operation capability with a very stable voltage gain of 2.91 (i.e., <1% change) at 500 ºC [4]. A high gain and CMRR SiC JFET–based operational amplifier is reported at room temperature to demonstrated the feasibility of overcoming design challenges, such as low intrinsic gain and low gate-to-source voltage range [28]. Another IC-compatible SiC-JFET based operational amplifier is presented in [29]; at 300 ºC, it shows a voltage gain of 57 dB and ~1000 hours of operation [30]. An AC-coupled SiC vertical JFET-based differential amplifier is reported in [31] and tested at 450 ºC, showing a voltage gain of 47.8 dB.

Table 2-3 Summary of published work on SiC-beased amplifiers for high-temperature applications

Authors	Devices	Max Operation Temperature (ºC)	Description
Tomana [25]	MESFET	350	Differential amplifier, at 350 °C, Gain > 60 dB GBW = 0.91 MHz
Brown [26]	MOSFET	300	Operational amplifier, At 300 °C, Gain = 53 dB GBW = 269 kHz
Sheppard [27]	CMOS	300	Operational amplifier, At 300 °C, Gain ~80 dB GBW = 571 kHz
Neudueck [4]	JFET	500	Differential amplifier, At 500 °C Gain @1 KHz = 2.91, GBW = 32 kHz, Gain change <1% & GBW change <3% after 3007 hrs operation
Maralani [28]	JFET	26	Operational amplifier, At 26 °C, Gain = 67dB, CMRR = 73dB
Stum [29]	JFET	300	Operational amplifier, At 300 °C, Gain = 57dB Long-term operation demonstration
Yang [31]	JFET	450	Differential amplifier, At 450 °C, Gain = 47.8dB,

2.3 Junction Field Effect (JFET) Transistors and Integrated Circuits Fabricated at CWRU

2.3.1 Fabrication process

The JFET-based ICs described in this thesis were design by Amita Patil (a previous member of Garverick Lab) and fabricated by Dr. Xiao-an Fu (a previous member of Mehregany Lab) based on a process originally developed at NASA Glenn Research Center [16] that subsequently was modified for our microfabrication facilities. The p-type, Al-doped (1.0 – 5.0 Ω-cm) 2-inch SiC substrate wafers with three customized epitaxial layers were sourced from Cree, Inc. As shown in Figure 2-8, the first layer is a 7.0 μm-thick Al-doped p^- epitaxial layer with a doping concentration of ~2.0×10^{15} cm^{-3}; it was grown on the substrate to serve as the bulk of the transistor, ensuring channel depletion is dominated by gate bias. Then, a 0.3 μm-thick, nitrogen-doped epitaxial layer with a doping concentration of ~1.0×10^{17} cm^{-3} was grown on the p^- buffer layer for the n-channel of the JFETs. Finally, a p^+ Al-doped epitaxial layer with a thickness of 0.2 μm and a doping concentration of ~2.0×10^{19} cm^{-3} was grown and used for the gates of the JFETs.

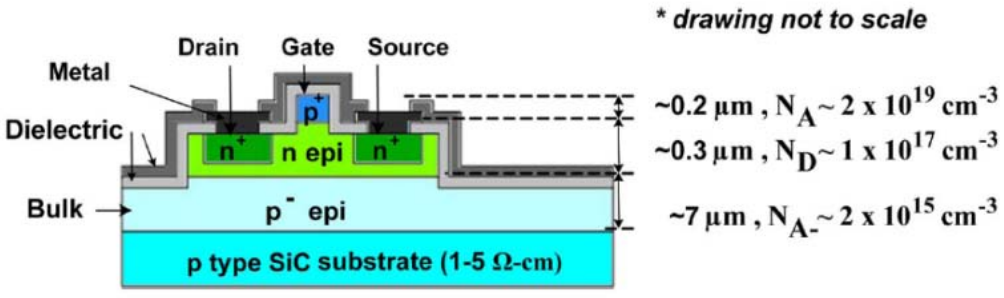


Figure 2-8 Schematic cross-section of the JFETs in this work [32].

The gates and channels of the JFETs were patterned by inductively-coupled plasma (ICP) reactive ion etching (RIE) using nickel as etch masks, which allowed a well-controlled etch rate with nearly vertical side walls. A 1.5-μm low temperature oxide (LTO) mask was deposited at 400 ºC by low-pressure chemical vapor deposition (LPCVD) to delineate n^+ source and drain ohmic contact areas. Multiple nitrogen implants with a box doping concentration profile of 6×10^{19} atoms/cm^3 was implanted at 600 ºC; the implanted dopants were activated in a nitrogen atmosphere at 1200 ^oC for 30 mins to form Ohmic contacts. Next, a 25-nm oxide was thermally grown on the surface at 1100 ºC in a wet O_2 ambient for surface passivation. A Ti/$TaSi_2$/Pt metallization was sputtered at a base pressure lower than 10^{-7} Torr; the wafers were then annealed at 950 ºC for 10 minutes in a forming gas (5% H2 in N2) to form the n^+ and p^+ Ohmic contacts. Discrete JFETs devices were completed at this stage.

Figure 2-9 shows a scanning electron micrograph (SEM) of a fabricated JFET device. Interconnect metallization and passivation layers were used to realize the ICs. Low temperature oxide (LTO) was used for the dielectric layer between contact metal and interconnect metals. The first interconnect metal layer was deposited by sputtering Ti followed by Pt, then patterned by lift-off process. The more complex ICs, such as two-stage amplifiers, required an additional interlayer dielectric and interconnect metal, which were formed using $SiO_2/Si_3N_4/SiO_2$ and Ti/TaSi2/Pt. The fabricated wafers were diced and packaged in ceramic dual-in line packages (DIPs) for characterization at elevated temperatures.

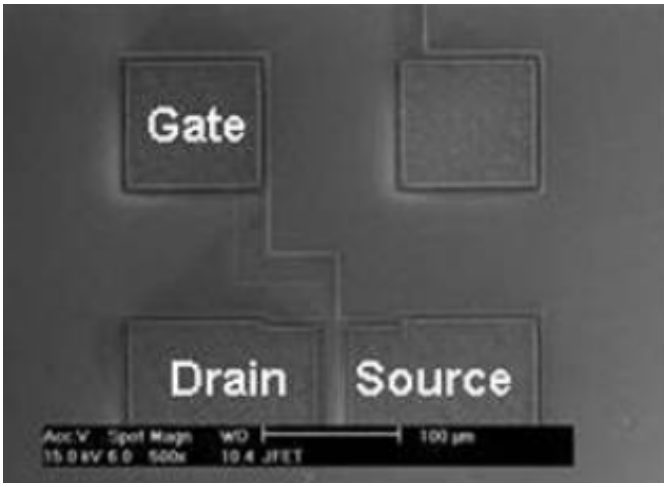


Figure 2-9 SEM of a JFET with W/L = 100μm/10μm [32].

2.3.2 JFET transistors modeling and characterization

Instead of using the well-known square-law approximation Schichman-Hodges model [33], a traditional 3/2-power model was employed in Chompoonoot Anupongongarch's work [34] to accurately model transistor behavior with large overdrive voltage. (Chompoonoot Anupongongarch is a previous member of Garverick Lab.) In contrast to prior work, the *bulk bias effect* was included by Anupongongarch to characterize JFET behavior with temperature dependence.

In triode region, $V_{DS} < V_{DSAT} \equiv \{V_{GS} - (V_{bi} - V_{po})\}$,

$$I_{DS} = \left(\frac{W}{L}\right) I_p{}' \left[\frac{3V_{DS}}{V_{po}} - 2\left[\left\{\frac{V_{DS} - V_{GS} + V_{bi}}{V_{po}}\right\}^{3/2} - \left\{\frac{(-V_{GS} + V_{bi})}{V_{po}}\right\}^{3/2}\right]\right](1 + \lambda V_{DS}) \qquad (2.7)$$

Three essential parameters for transistor modeling—built-in voltage between gate and channel (V_{bi}), pinchoff voltage (V_{po}), and normalized pinchoff current (I_p')—are studied in this work. These parameters are given by

$$V_{bi} = \frac{kT}{q} \ln\left(\frac{N_A N_D}{n_i^2}\right) \tag{2.8}$$

$$V_{po} = \left(\frac{qN_D D^2}{2\varepsilon_s}\right) \tag{2.9}$$

$$I_p' = \left(\frac{q^2 N_D n \mu_n D^3}{6\varepsilon_s}\right) \tag{2.10}$$

In Saturation region, $V_{DS} > V_{DSAT}$,

$$I_{DSAT} = \left(\frac{W}{L}\right) I_p' \left[1 - 3\left(\frac{-V_{GS} + V_{bi}}{V_{po}}\right) + 2\left(\frac{-V_{GS+}V_{bi}}{V_{po}}\right)^{3/2}\right](1 + \lambda V_{DS}) \tag{2.11}$$

where D, W and L are channel depth, width, and length, respectively. n_i is intrinsic carrier concentration, λ is the channel length modulation parameter, n is the channel ionized carrier concentration, μ_n is the mobility of carriers, and ε_s is the permittivity of 6H-SiC.

The fabricated JFETs were characterized on a probe station with varying bulk bias and temperature. Device parameters were extracted for model verification at operating temperatures up to 450 ºC. The measured and simulated drain current behavior of JFETs is shown in Figure 2-10 for room temperature to 595 ºC.

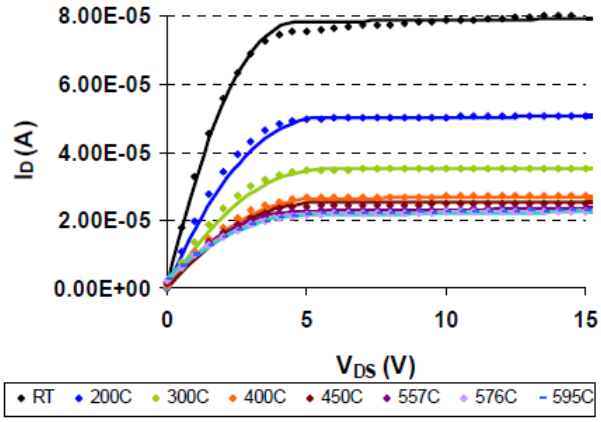


Figure 2-10 Comparison of measured and modeled drain current characteristics for W/L = 100µm/100µm JFETs from room operating temperature to 595 °C [34].

2.3.3 Differential pairs and hybrid differential amplifiers

The schematic and SEM image of a SiC JFET differential pair are shown in Figure 2-11. (The initial device and circuit characterizations reviewed in this Chapter 2 were performed mostly by Dr. Amita Patil, a previous member of Garverick Lab.) The measured DC transfer characteristic and transconductance are plotted in Figure 2-12 from room temperature to 450 ºC. Multi-stages hybrid amplifiers were constructed by these SiC JFET differential pairs and external passive components. A two-stage hybrid differential amplifier is shown in Figure 2-13. This configuration yields a voltage gain of 80 dB at room temperature, and 70 dB at 450 ºC. The measured bandwidth at room temperature and 450 ºC is 1.8 MHz and 1.3 MHz, respectively. The measured AC response with multi-stage differential amplifiers is presented in Figure 2-14.

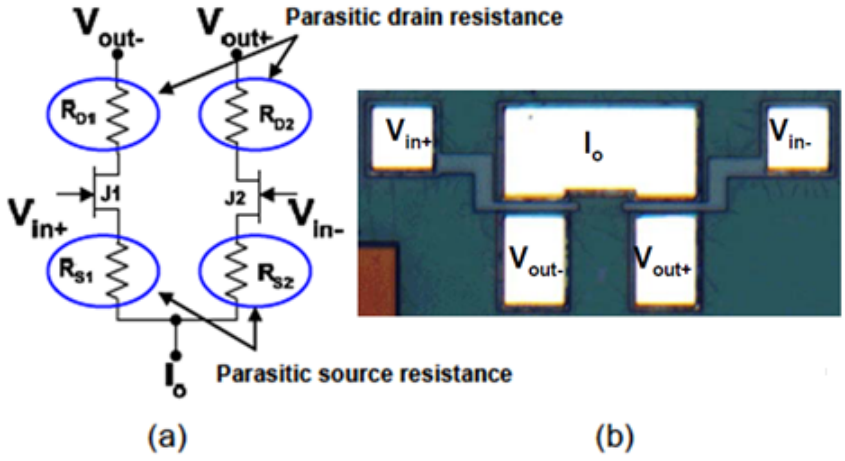


Figure 2-11 (a) Schematic and (b) SEM image of a differential pair with W/L = 110 µm/10µm SiC JEFTs [35].

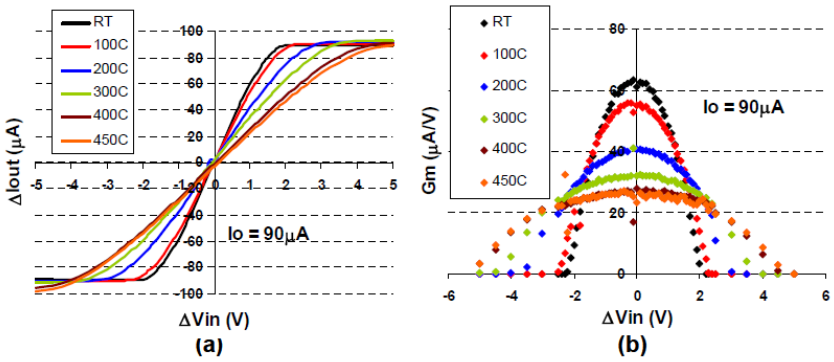


Figure 2-12 (a) DC characteristics, and (b) transconductance of a differential pair with W/L = 100 μm/10μm [35].

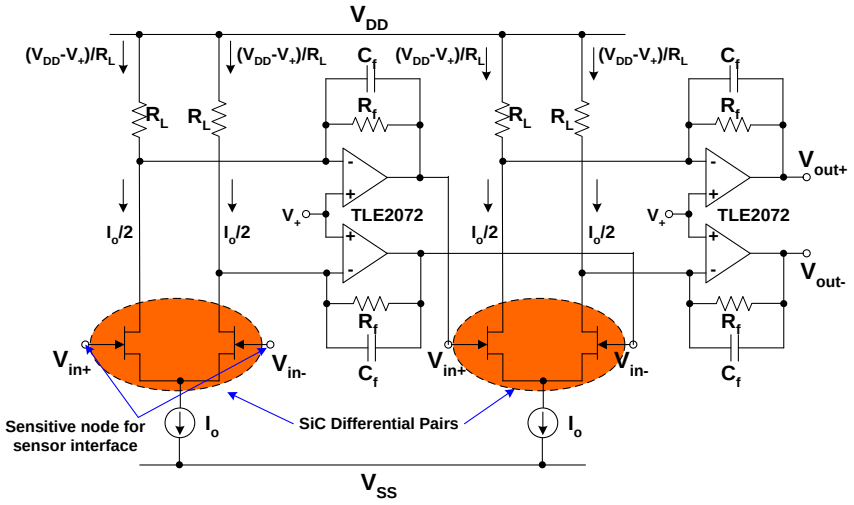


Figure 2-13 Circuit schematic of a hybrid, two-stage differential amplifier with active loads [33].

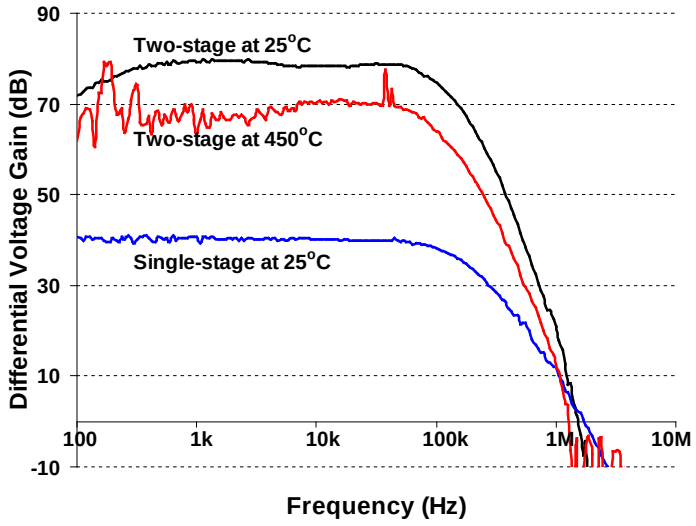


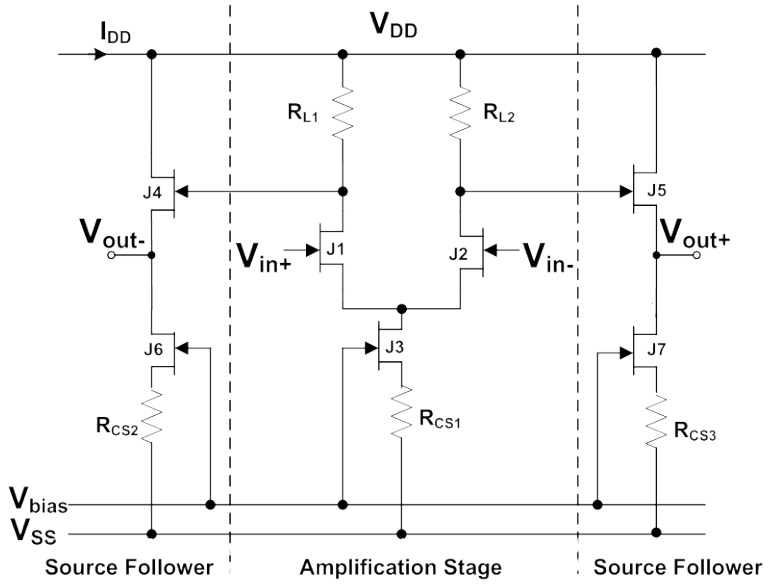
Figure 2-14 Measured AC response of hybrid amplifiers at room temperature and at 450 °C [33].

2.3.4 Design and characterization fully-integrated amplifiers

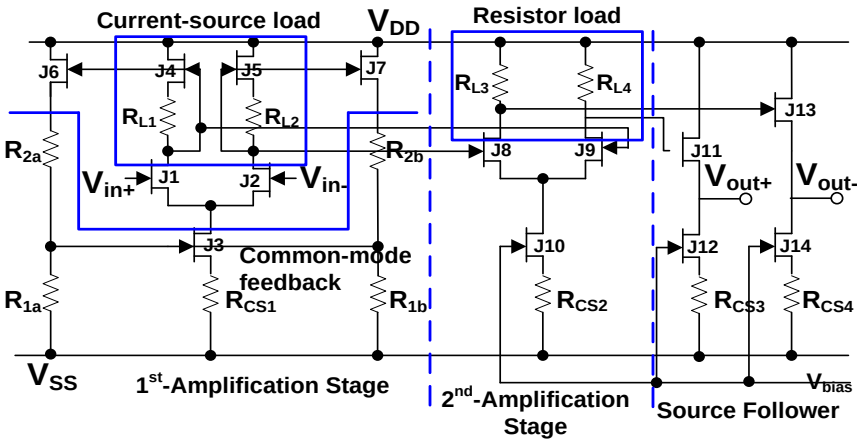
A family of fully-integrated differential amplifiers was also designed and fabricated. A fully-integrated, single-stage differential amplifier with resistive loads and a source-follower output stage is shown in Figure 2-15(a). The current-sources were carefully designed to reduce offset and noise. The voltage gain of this amplifier is given by

$$|A_{dm}| = (g_{m1,2}(r_{o1,2}||R_{L1,2})) \times \frac{g_{m4,5}}{g_{m4,5} + g_{mb4,5}} \approx g_{m1,2} \times R_{L1,2}. \qquad (2.12)$$

The two-stage differential amplifier with active loads is shown in Figure 2-15(b). The measured gain of this amplifier at room temperature and up to 575 ºC is presented in Figure 2-16. The amplifier has a differential gain of ~69 dB from room temperature to 575 ºC; the gain variation is ~ 5%.



(a)



(b)

Figure 2-15 Schematic of (a) a single-stage, differential amplifier with passive loads and (b) a two-stage, differential amplifier with current source loads in the 1st stage and resistor loads in the 2nd stage [5].

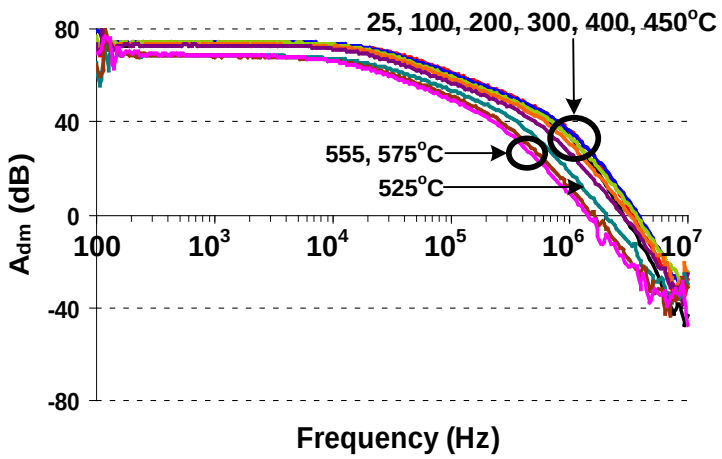


Figure 2-16 Measured voltage gain of the two-stage, differential amplifier in Fig. 2-15(b) [5].

High gain-bandwidth, monolithic, transimpedance amplifiers were also designed and fabricated for capacitive or resonant sensor interface applications. Figure 2-17 is the circuit schematic of a single-stage, transimpedance amplifier. The amplifier can also be used as a voltage amplifier. A gain measurement result at room temperature is shown in Figure 2-18 from two identical copies on the same die. The gain difference is ~ 2% for these two copies.

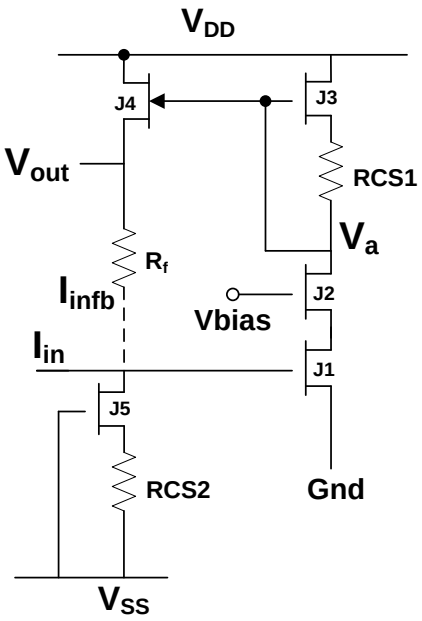


Figure 2-17 Schematic of a single-stage, single-ended transimpedance amplifier [35].

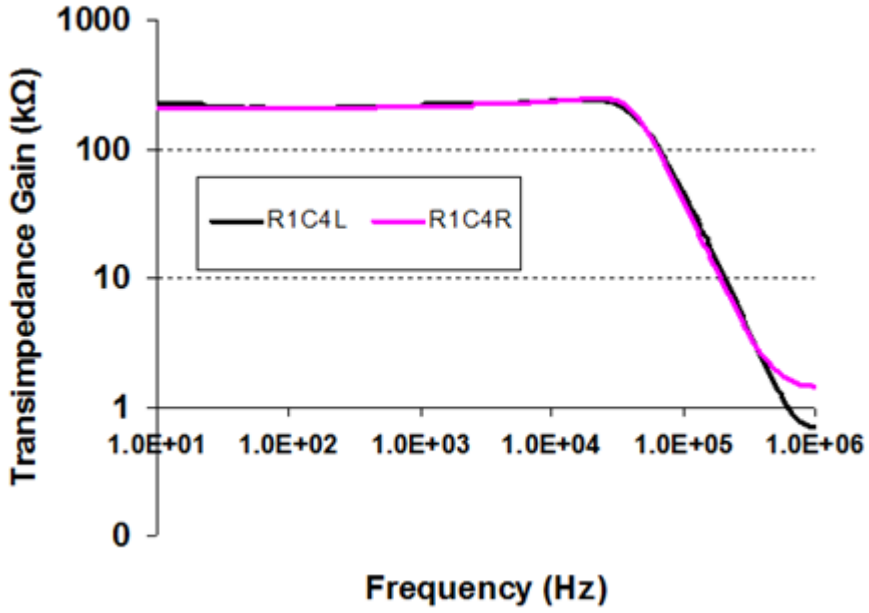


Figure 2-18 The measured frequency response, at room temperature, for two copies of the transimpedance amplifier of Fig. 2-17 on the same die [35].

3 Uniformity of Electrical Characteristics of CWRU-Fabricated Discrete JFETs

The 2 inch-diameter wafer (CR0975-12) texted here consisted of 46 identical dies, each die containing a set of five JFETs with varying W/L ratios (i.e., a total of 229 JFETs—one less than expected because of one incomplete device at the edge of the wafer. The wafer was tested on a probe station, and the current-voltage (I-V) characteristics of the JFETs were measured with Keithley source measure units (SMUs). Values for threshold voltage (V_{TH}), saturation drain current (I_{DSS}), gate reverse leakage current (I_{GSS}) and off-state drain leakage current (I_{OFF}) were measured for each set of five JFETs on a die. To illustrate the variation of these parameters across the wafer, the measurements were grouped by increasing radial distance from wafer center. From a total of 229 JFETs (excluding incomplete devices at the edges), 215 were deemed operational. The corresponding yield map is shown in Figure 3-1, defining die regions with 100%, 80%, 60% and 0% yield corresponding to five, four, three and zero JFETs with well-defined I-V characteristics, respectively. There were no die regions with 20% or 40% yield. The sizes of defective/failed devices are also indicated in the map. N/A signifies that JFETs were not fabricated at the die location. Most of the defective/inoperable devices failed to enter the OFF state and were mostly located at the outer edges of the wafer. They were thought to be compromised by the significant epitaxial layer thickness non-uniformity at the edges of the wafer.

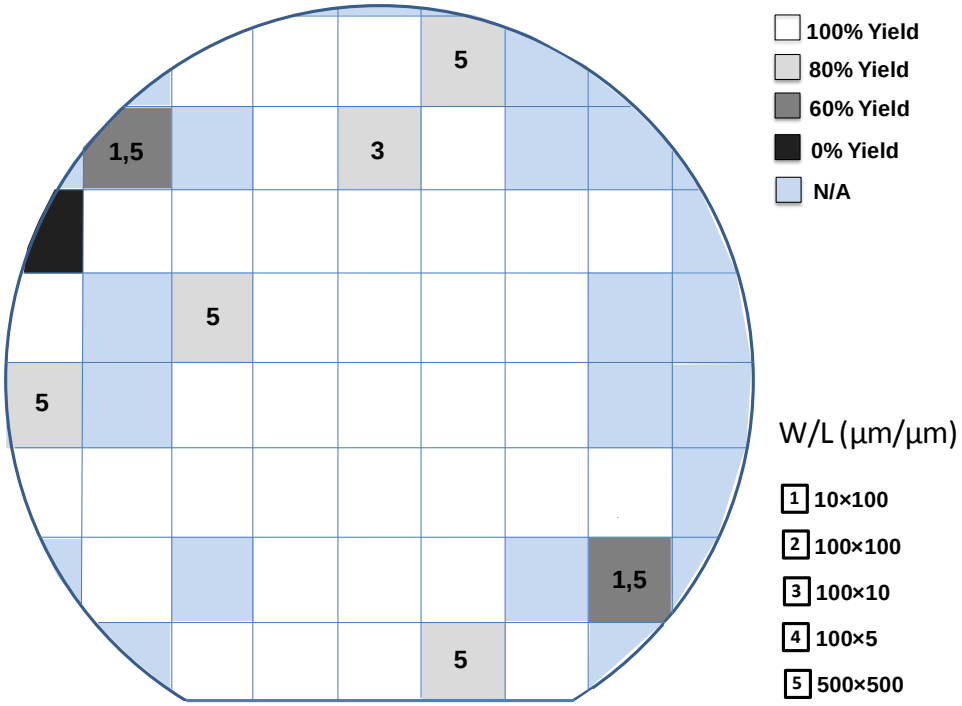


Figure 3-1 Yield map of JFETs on the 2 inch-diameter 6H-SiC wafer.

3.2 On-State Parameter Measurement

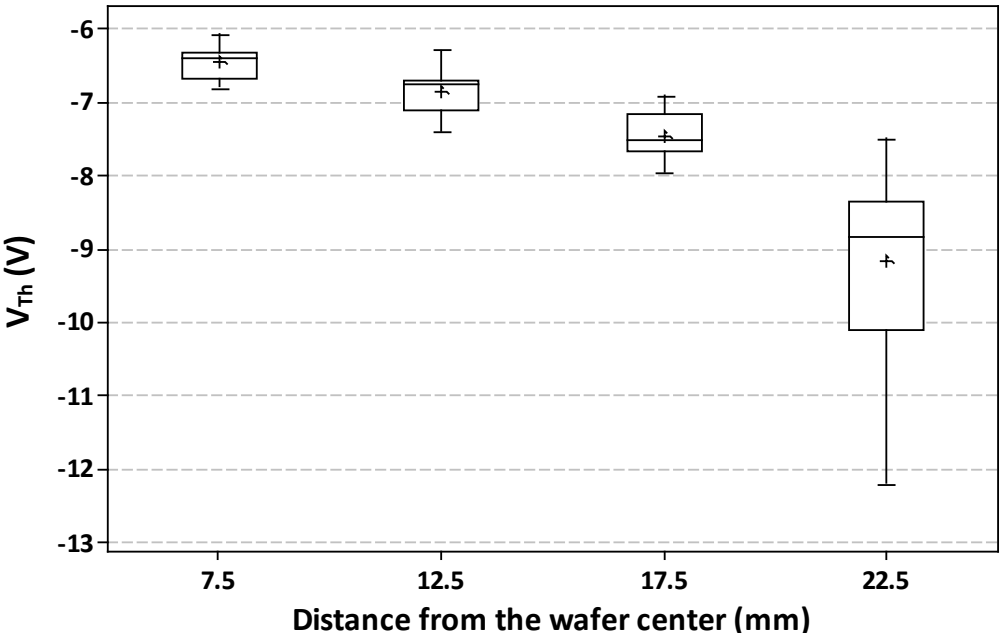
The discussion in this Section 3.2 pertains to JFETs with W/L = 100µm/100µm.

3.2.1 Room temperature testing

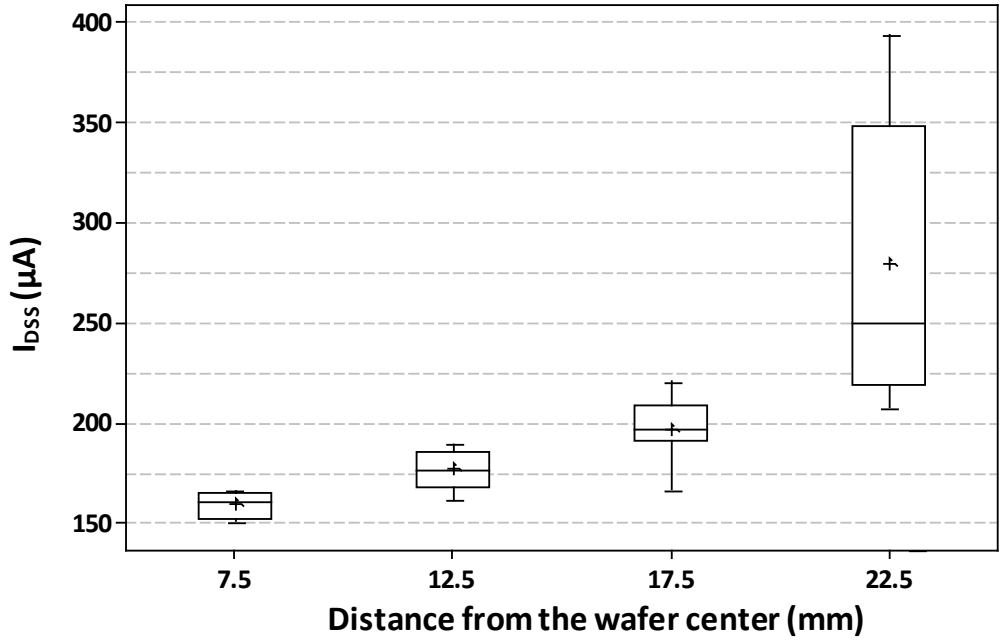
V_{TH} is extracted from the I_{DS}-V_{GS} sweep, with V_{BS} = 0 V. Figure 3-2(a) plots V_{TH} as a function of radius from the wafer center. V_{TH} is seen to vary from -6.05 V to -12.18 V with a mean of -7.74 V and a standard deviation (σ) of 1.36 V, respectively. The designed nominal value was -5.00 V (with a calculated variation of -0.50 V to -12.50 V due to doping and thickness variations of ±50% and ±10%, respectively, for the channel epitaxial layer). I_{DSS} in the ON state was measured with V_{GS} = 0 V, V_{DS} = 40 V, and V_{BS} = 0 V. As shown in Figure 3-2(b), I_{DSS} had a variation between 151.13 µA to 394.15 µA, with a mean of 214.70 µA and a σ of 63.98 µA. The epi-layer thickness at the wafer edge was inferred to be thicker than at the center of the wafer [36]. Therefore, larger pinchoff-voltages were expected near the edge of the wafer—and thus larger $|V_{TH}|$—as compared to the center. Both $|V_{TH}|$ and I_{DSS} values showed an increasing spread with distance from the wafer center, consistent with the relationship between I_{DSS} and $|V_{TH}|$. Per the square-law model,

$$I_{DSS} = \frac{W}{L} k'(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \tag{3.1}$$

where k' is transconductance parameter. Thus, high/low values of one parameter translate to high/low values of the other.



(a)



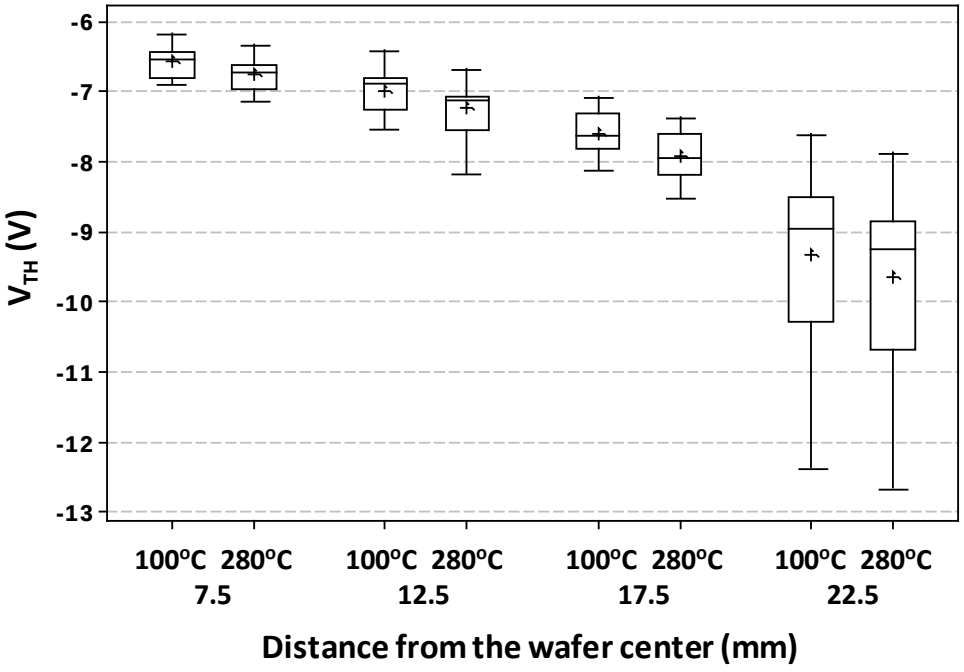
(b)

Figure 3-2 JFETs with W/L = 100µm/100µm: (a) V_{TH}; and (b) I_{DSS}. The box width is proportional to the sample size. The bottom and top of the box represents 25th and 75th percentile of the data. The band and the cross inside the boxes are the median and mean, respectively.

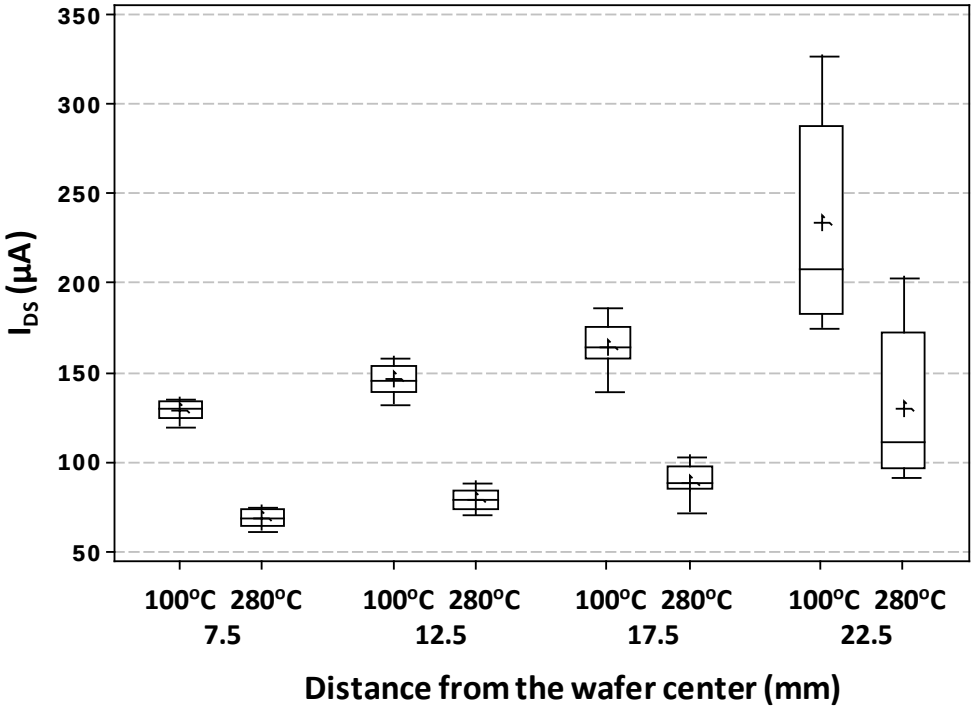
3.2.2 High temperature testing

The JFET devices were tested on a probe station at room temperatures to 280 ºC, limited by the hot chuck heating ability. A thermocouple sensor monitored the temperature of the hot chuck. Measured V_{TH} and I_{DSS} as a function of radius from the wafer center are shown in Figure 3-3 at elevated operating temperatures. The designed nominal V_{TH} at 100 ºC was -5.33 V. The measured V_{TH} was seen to vary from -6.16 V to -12.36 V with a mean of -7.85 V and a σ of 1.34 V, respectively. I_{DSS} has a variation between 120.25 µA to 326.75 µA, with a mean of 176.84 µA and a σ of 53.47 µA. At 280 ºC, the designed nominal V_{TH} is -5.54V. The variation range for measured V_{TH} is between -6.32 V to -12.64 V, with a mean of -8.13 V and a σ of 1.39 V. I_{DSS} varies between 61.97 µA to 203.23 µA, with a mean of 96.43 µA and a σ of 33.72 µA.

All the measured data are within the expected variation range calculated based on manufacturer-stated specifications. Similar with room temperature measurement results, both $|V_{TH}|$ and I_{DSS} values show an increasing spread with distance from the wafer center.



(a)



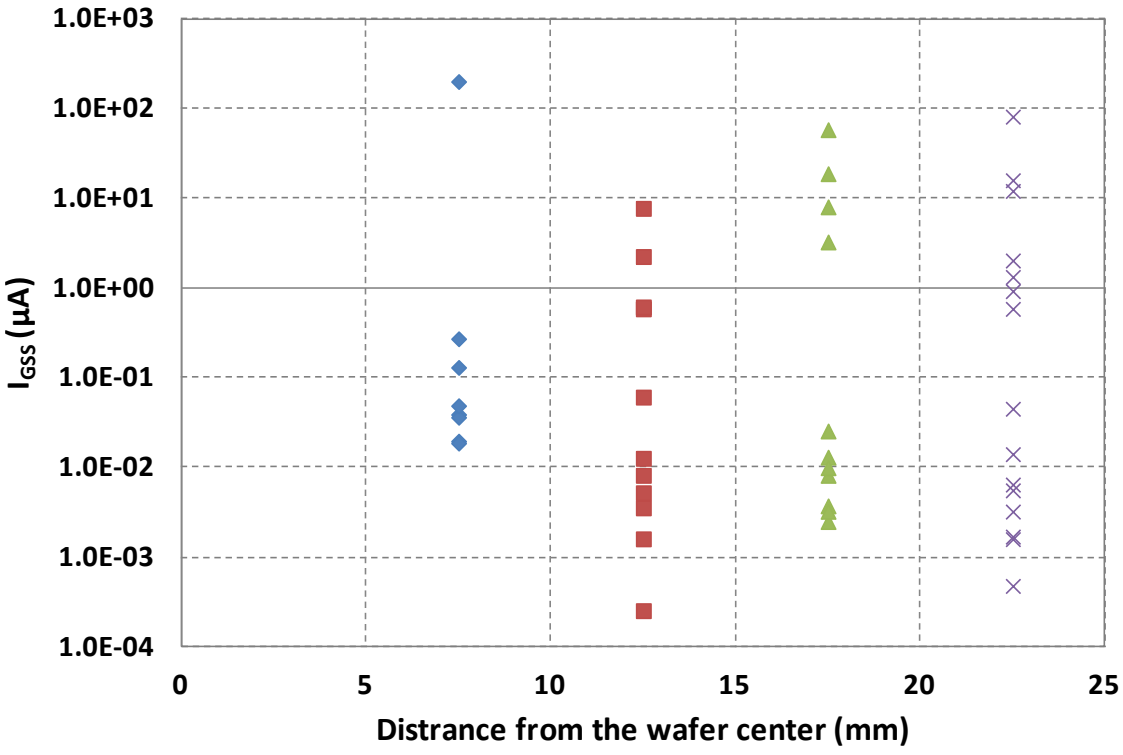
(b)

Figure 3-3 Box plots of measured (a) V_{TH} and (b) I_{DS} of JFETs with W/L = 100µm/100µm at 100 °C and 280 °C.

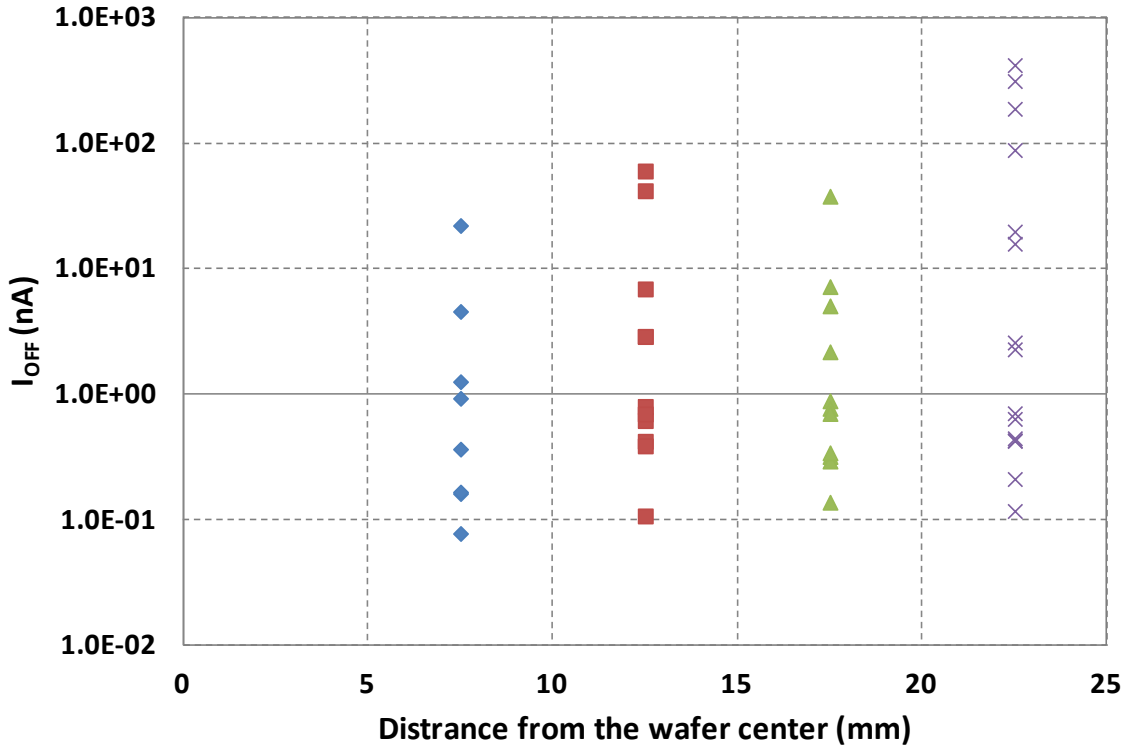
3.3 Off-State Parameter Measurement

The off-state characteristics, including I_{GSS} and I_{OFF}, were also measured. The scatter plots of these two parameters are shown in Figure 3-4. I_{GSS} is the gate-to-channel leakage current of the reverse biased p-n junction. Test conditions for I_{GSS} were: V_{GS} = -15 V, V_{DS} = 0 V and V_{BS} = 0 V. The measured I_{GSS} varies by four to five orders of magnitude at a given distance from the wafer center and across the wafer; it has a mean value of -9.46 μA with a σ of 33.41 μA. The measured I_{GSS} is several orders of magnitude higher than that theoretically expected (nA or lower).

I_{OFF} is the channel leakage current in the OFF state. Test conditions for I_{OFF} were: V_{GS} = -15 V, V_{DS} = 40 V and V_{BS} = 0 V. It is important to keep the I_{OFF} small since it is the main contributor to static power consumption of circuits in standby mode. Measured I_{OFF}, showed a mean of 28.86 nA and a σ of 82.60 nA. A worst-case (CR0975-12-R3C1) on/off current ratio of *539* was seen at room temperature and a ratio of 182 at 280 °C.



(a)



(b)

Figure 3-4 JFETs with W/L = 100µm/100µm: (a) I_{GSS}; and (b) I_{OFF}.

3.4 Summary

The same trends are observed for JFETs with different W/L. Table 3-1 summarizes the distributions of the measured device parameters for all five sizes of JFETs at room temperature. Measured on-state characteristics at high temperatures with devices with W/L = 100µm/100µm and 500µm/500µm are listed in Table 3-2 and Table 3-3, respectively. Overall, the V_{TH} and I_{DSS} for the five sizes show relatively close values of coefficient of variance (CV) across the tested temperature range. Large variation of I_{GSS} and I_{OFF} are observed across all five JFET sizes. I_{GSS} is related to the quality of p-n junction in the devices; as the results, a study on the behavior of parasitic p-n diodes in the discrete JFET devices at elevated temperatures is presented in Chapter 5. Across the wafer, an on/off current ratio > 539 is seen at room temperature.

Table 3-1 Statistical summary of JFET electrical parameters across a 2 inch-diameter 6H-SiC wafer.

	10µm/100µm (n = 43)		**100µm/100µm (n = 45)**		**100µm/10µm (n = 44)**		**100µm/5µm (n = 45)**		**500µm/500µm (n = 39)**	
	Mean	CV*	Mean	CV	Mean	CV	Mean	CV	Mean	CV
V_{TH} (V)	-7.34	15.65	-7.74	16.23	-6.99	14.59	-8.34	15.82	-6.69	11.16
I_{DSS} (µA)	41.20	28.85	214.70	29.79	1189.96	24.14	1785.58	26.42	178.20	22.16

* CV (coefficient of variation) CV (%) = (STD/ Mean) ×100%.

Table 3-2 Statistical summary of on-state parameters for W/L = 100µm/100µm JFETs across a 2 inch-diameter 6H-SiC wafer up to 280 °C.

	23 °C		100 °C		280 °C	
	Mean	CV	Mean	CV	Mean	CV
V_{TH} (V)	-7.74	16.23	-7.85	17.27	-8.13	17.21
I_{DSS} (µA)	214.70	29.79	176.84	30.23	96.43	29.96

Table 3-3 Statistical summary of on-state parameters for W/L = 500µm/500µm JFETS across a 2 inch diameter 6H-SiC wafer up to 280 °C.

	23 °C		100 °C		280 °C	
	Mean	CV	Mean	CV	Mean	CV
V_{TH} (V)	-6.69	11.16	-6.85	13.57	-7.08	14.82
I_{DSS} (µA)	178.20	22.16	146.15	21.85	83.16	24.56

4 6H-SiC Circuit Characterization

4.1 Logic Circuits

4.1.1 Circuit design

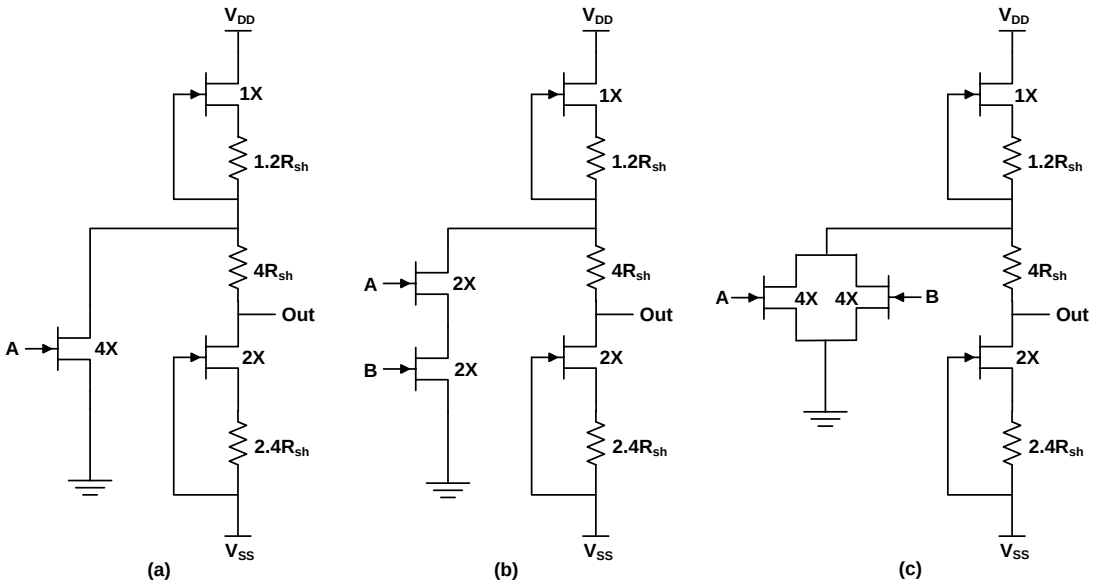


Figure 4-1 Circuit Schematics of 6H-SiC (a) inverter, (b) NAND and (c) NOR gates.

Circuit schematics of the logic gates are provided in Figure 4-1. An active-load topology, based on the depletion-mode NMOS topology popular *circa* 1980 [37], was used to obtain high performance, i.e., a sharp transfer characteristic that is well centered in the range of logic swing. In the core inverter circuit of Figure 4-1(a), the A input controls a 4x JFET driver device, whose drain current is supplied by a degenerated 2x JFET which acts as a current source. The size of the unity device, 1x JFET, is W/L = 160µm/10µm. The remaining circuits perform level shifting that ensures the output level to the next logic circuit stage is ≤0 V, as required by its JFET input. The NAND and

NOR gates were designed for constant area. The NAND gate of Figure 4-1(b) uses two series 2x JFETs in the pull-down driver network. The NOR gate in Figure 4-1(c) uses two parallel 2x JFETs in the pull-down driver network. The resistors are all fabricated from the n-channel epitaxial layer. Figure 4-2 shows an optical micrograph of a fabricated NOR gate.

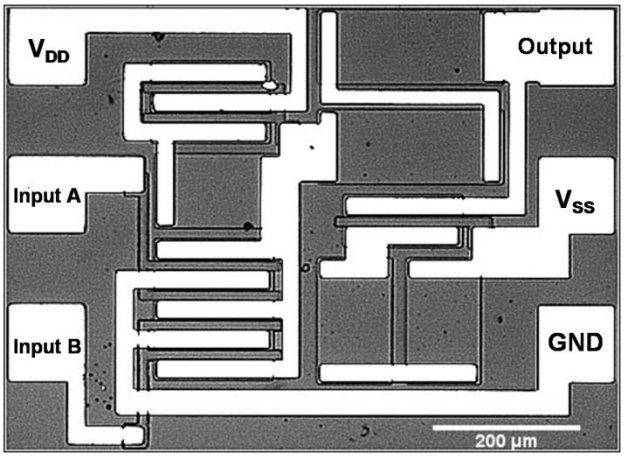


Figure 4-2 Optical micrograph of fabricated 6H-SiC JFETs based NOR.

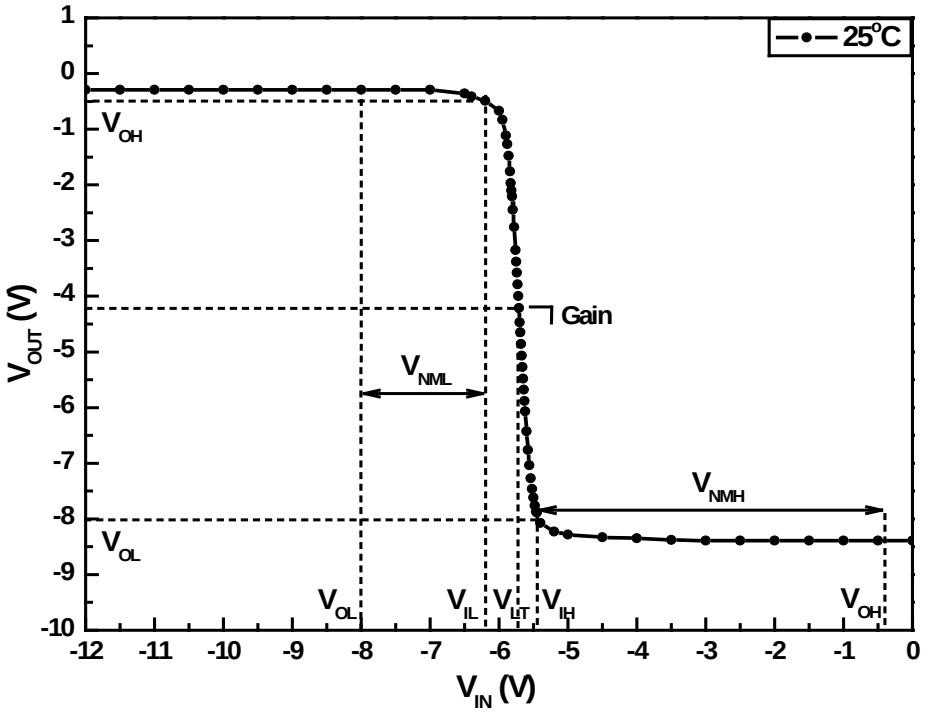
4.1.2 Characterization of core inverter

Testing conditions for all logic gates were as follows: V_{DD} and V_{SS} are +14 V and -14 V, respectively; input logic high = 0 V; and input logic low = -7 V. All three logic gates were verified to operate from room temperature to 550 ºC. The voltage transfer characteristic (VTC) of the core inverter across the measured temperature range is shown in Figure 4-3. At all temperatures, the slope of the VTC is quite steep, with voltage gain > 20 up to 500 ºC, and is well centered in the range of logic swing.

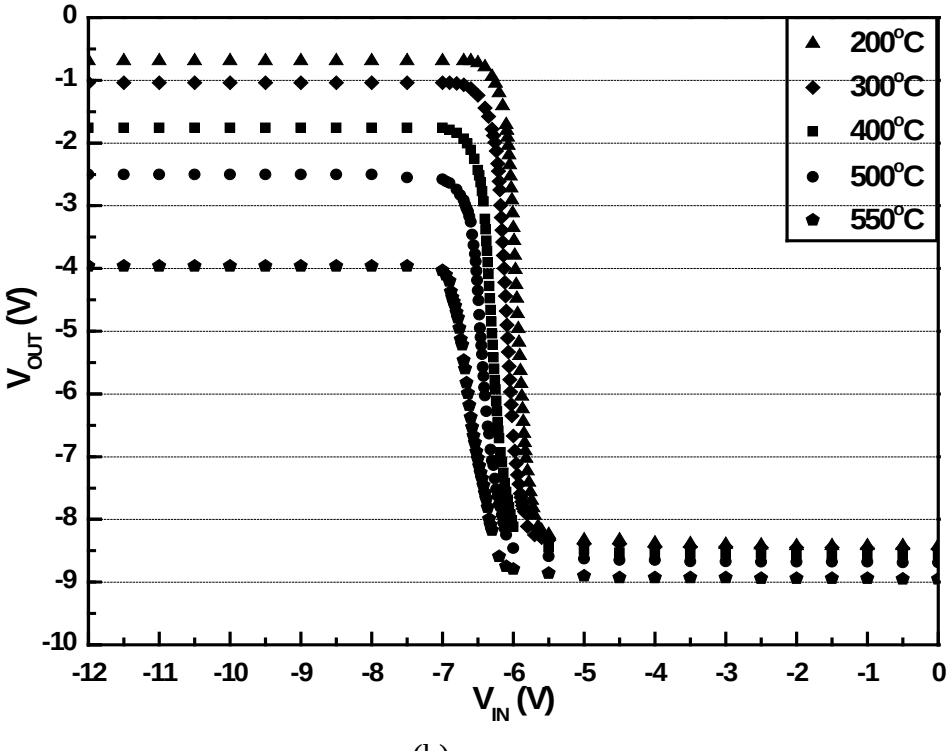
Six key DC performance metrics of the inverter, namely the minimum output voltage in the high state (V_{OH}), maximum output voltage in the low state (V_{OL}), logic gate threshold voltage (V_{LT}), voltage gain (Gain), noise margin for low level (V_{NML}) and noise margin for high level (V_{NMH}), are summarized in Table I, for all measured temperatures. By design, these metrics hold relatively constant over temperature. The observed variation is caused primarily by the variation in JFET threshold voltage, $dV_{TH}/dT \cong -2.3$ mV/C [32]. Parameters V_{LT} and V_{OL} vary at the same rate, $\sim dV_{TH}/dT$ so V_{NML} remains nearly constant. The high logic level V_{OH} varies at a greater rate, $(1 + 4/2.4)\, dV_{TH}/dT$, so V_{NMH} is noticeably degraded.

All test results are based on unity fan-out, but since the FETs have negligible gate current, fan-out does not affect DC performance. It is relatively difficult to compare the measured noise margin with prior work, since the power supply voltage is not standardized. However, it is clear that the magnitude, symmetry, and stability of the noise margin is adequate over this very wide temperature range for logic circuits of moderate complexity.

For digital applications, power consumption is a critical characteristic. In order to estimate the power consumption of the core inverter, supply currents at low and high output levels were measured (Figure 4-4). At 25 ºC, with ±14V power supply, the power consumption for the low and high output levels were 6.748 W and 4.956 W, respectively. Supply current decreased as temperature increased. Up to 550 ºC, the power consumption for the low and high output levels were 1.34 W and 1.09 W, respectively.



(a)



(b)

Figure 4-3 VTC of the SiC inverter at (a) 25 ºC and (b) elevated temperatures. All experiments were conducted in an ambient environment with V_{sub} = 0 V, V_{DD} = +14 V and V_{SS} = -14 V.

Table 4-1 DC performance metrics of the SiC inverter.

	25 ºC	200 ºC	300 ºC	400 ºC	500 ºC	550 ºC
V_{OL}	-8.00	-8.12	-8.15	-8.20	-8.37	-8.69
V_{LT}	-5.71	-5.94	-6.11	-6.34	-6.51	-6.72
V_{OH}	-0.50	-0.79	-1.10	-1.86	-2.64	-3.97
Gain	-26	-24	-23	-20	-20	-12
V_{NML}	1.80	1.67	1.54	1.42	1.47	1.52
V_{NMH}	4.91	4.85	4.67	4.13	3.4	2.17

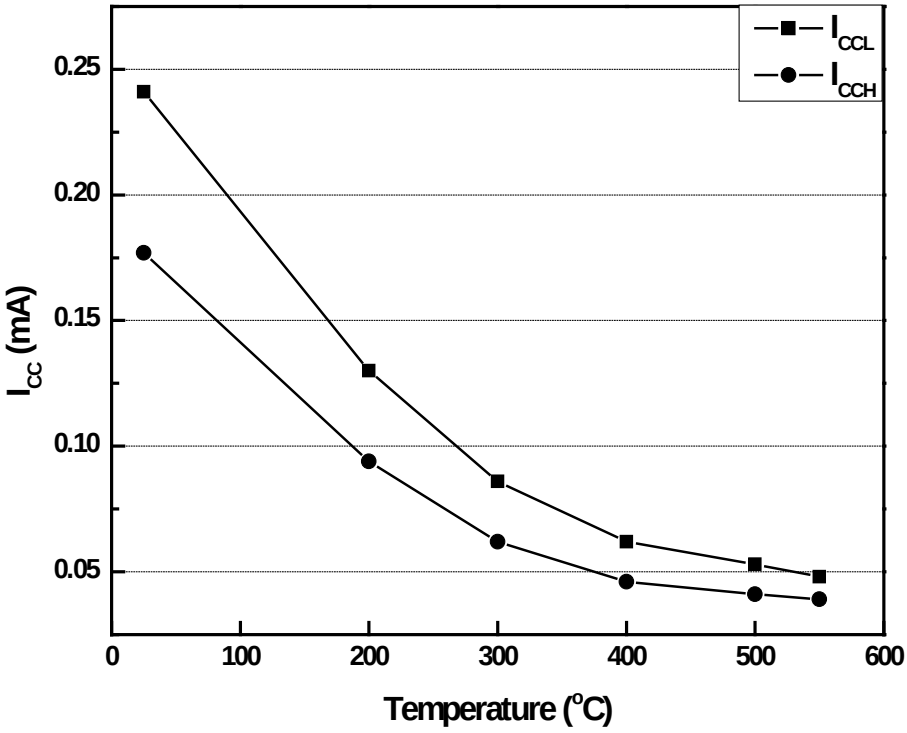


Figure 4-4 Supply Current with temperature dependence at (a) low and (b) high output levels.

4.1.3 Dynamic characteristics of NAND gate and NOR gate

Figure 4-5 shows the dynamic characteristics of the NAND and NOR gates at 25 ºC and 550 ºC. Although the output high level seems to degrade at high temperature, from the previous input inverter VTC, the gates are functional and have similar DC characteristics to the inverters described previously. Switching speed is limited by capacitance in the test setup.

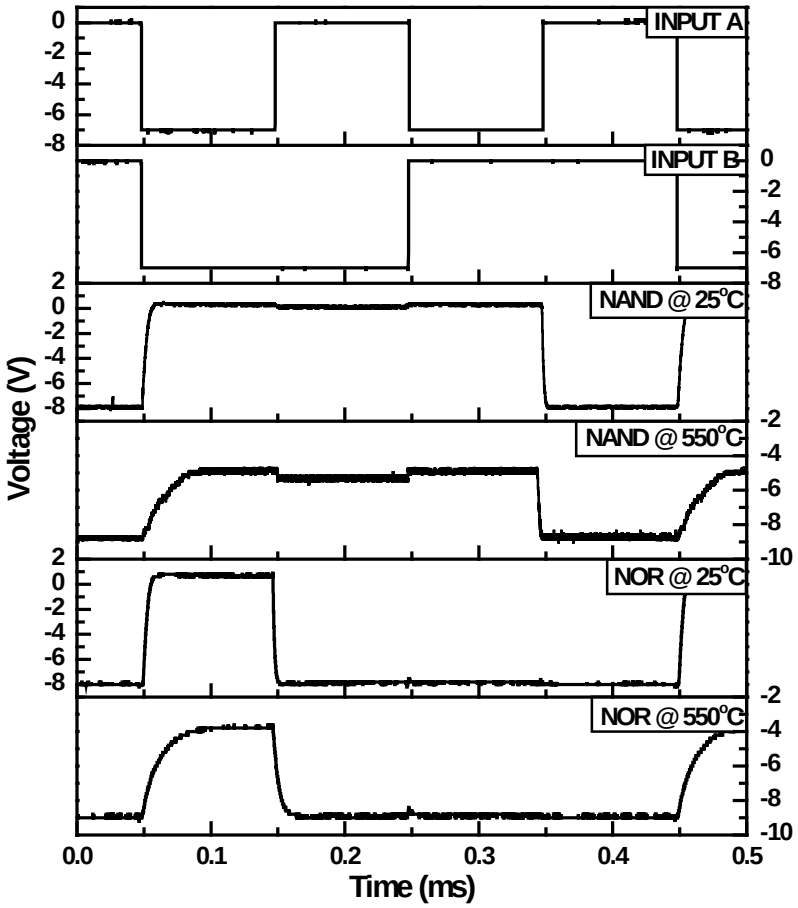


Figure 4-5 Measured dynamic characteristics of SiC NAND gate and NOR gate at 25 ºC and 550 ºC with V_{sub} = 0 V, V_{DD} = +14 V, and V_{SS} = -14 V.

4.2 Transimpedance Amplifier

Capacitive transduction is used in many sensing micfrosystems. Numerous capacitive sensors for high temperature applications have been reported [38-41]. Capacitive sensors usually exhibit high impedance within the signal bandwidth; it is crucial that the sensor signal is initially pre-amplified using an amplifier in close proximity to the sensor. As illustrated in Figure 4-6, the primary noise sources of the sensing system are (i) ground noise, which has a relative gain of C_p/C_s, and (ii) amplifier noise, which has a relative gain of $1+ (C_a + C_p)/C_s$. Both of these gain factors may be minimized by locating the interface circuits in close proximity to the sensing node. Ultimately, the integration of sensors and interface circuits in the same package can optimize signal/noise ratio, which leads to a more accurate reading, lower power consumption, and elimination of the weight and cost of a cooling system. Thus far, the integration of a SiC-based capacitive sensing interface circuits with a commercial or fabricated sensing elements has not been demonstrated.

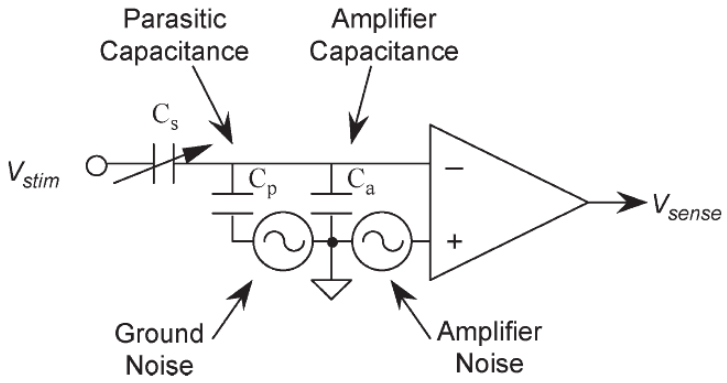


Figure 4-6 Generic sensor interface circuit for capacitive sensors [42].

4.2.1 Transimpedance amplifier characterization

4.2.1.1 Circuit design

A circuit schematic of a 6H-SiC JFET-based transimpedance amplifier, which is based on the circuit technique in [43], is shown in Figure 4-7. Designed transistor sizes and resistor values are summarized in Table 4-2 and Table 4-3, respectively. An optical microphotograph of the fabricated transimpedance amplifier is shown in Figure 4-8. In the schematic, J1 is the input driver device, and J2 is a cascode device that enables higher open-loop voltage gain. J3 and J5 are degenerated to serve as current sources, where RCS1 and RCS2 are used to set the current. J4 is configured as a source follower to provide a low impedance ($\sim 1/g_{m4}$), while feedback resistor, R_f, sets the transimpedance gain and provides a downward level shift necessary to maintain saturation of the driver device. The connection between R_f and the input of the transimpedance amplifier is realized off-chip so that the open-loop circuits can be tested as a voltage amplifier, if desired. The transimpedance gain is given by

$$R_m = \frac{R_f \cdot A_v}{1 + A_v}, \tag{4.1}$$

where $A_v \cong g_{m1}[(g_{m2} \cdot r_{o1} \cdot r_{o2})||(g_{m3} \cdot r_{o3} \cdot R_{CS1})]$. Thus, the gain of the transimpedance amplifier is approximately equal to R_f when A_v is >>1.

Resistor R_f is fabricated in the n-type channel epitaxial layer, having a resistance proportional to sheet resistance (R_{sh}). Given that R_{sh} was previously measured to be about 13.8 kΩ/□ at room temperature [44], the expected transimpedance gain is ~ $15R_{sh}$ = 207 kΩ at room temperature. Since R_{sh} is inversely proportional to the $n\mu_n$ product, resistance decreases somewhat at slightly elevated temperatures as ionization fraction increases [9];

however, the product will generally decrease with temperature as electron mobility decreases. Therefore, an increasing gain with temperature is expected.

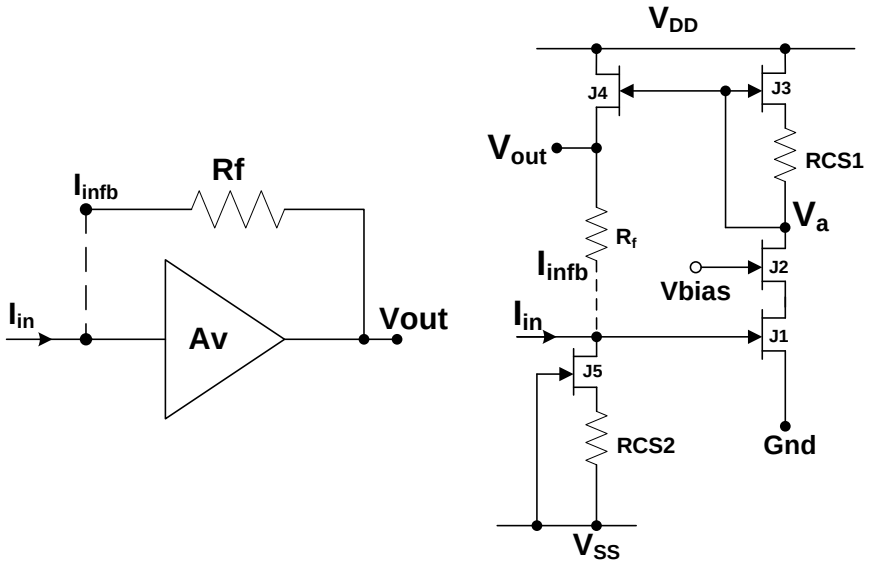


Figure 4-7 Schematic of a single-ended, single-stage transimpedance amplifier.

Table 4-2 JFET sizes and biasing voltages for the single-ended, single-stage transimpedance amplifier of Fig. 4-7.

	Device	W/L (μm/ μm)	(V_{GS}-V_T)
Driver devices	J1,J2	160/10	2
Current source	J3	160/10	2
	J5	80/10	2
Source follower	J4	320/10	1

Table 4-3 Resistor values for the single-ended, single-stage transimpedance amplifier of Fig. 4-7.

Device	Value (□)
RCS1	2.4
RCS2	4.8
R_f	12

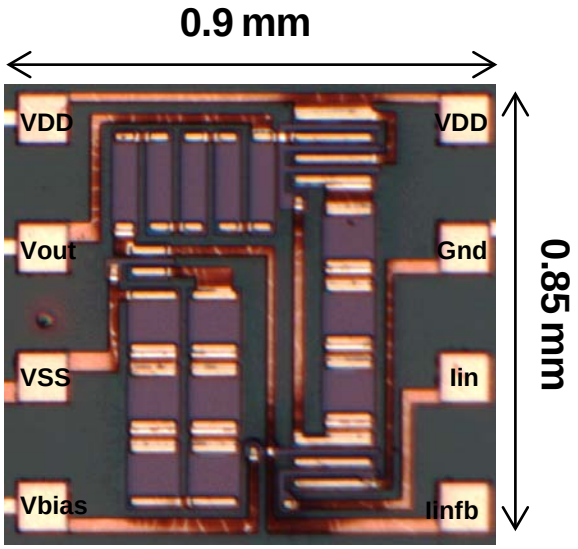


Figure 4-8 Optical microphotograph of the single-ended, single-stage transimpedance amplifier of Fig. 4-7.

A block diagram of the transimpedance amplifier test circuit is shown in Figure 4-9. The frequency response of the transimpedance amplifier was first characterized with test setup (1). A 1-MΩ input resistor was used to convert the voltage test signal from a network analyzer into an input current for the amplifier. In test setup (2), the amplifier was connected to a differential capacitor to simulate sensing functionality. Trimmer capacitors were excited by two ac-signal sources from a function generator that provides 180° phase difference.

The transimpedance amplifier was packaged in a ceramic dual-in-line package using gold bond wires. The IC die (not including the trimmer capacitors) was heated by a spot infrared heater in an ambient environment. Die temperature was measured using a thermocouple sensor. Before recording the measured data, the die was left heating under the spot infrared heater to achieve a stable operating temperature.

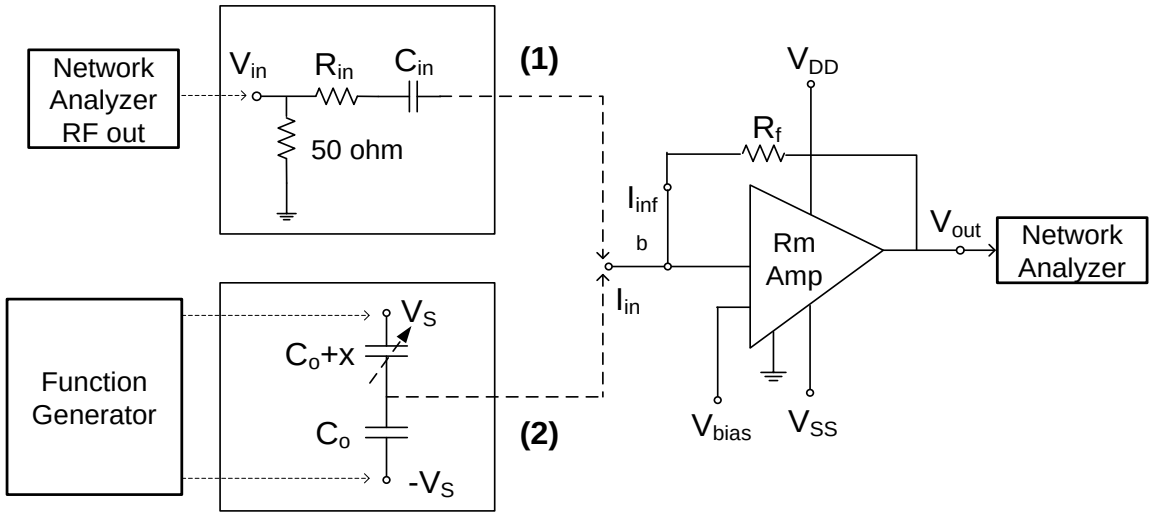


Figure 4-9 Schematic of the transimpedance amplifier test setup.

4.2.1.2 Test results

The measured frequency response of the transimpedance amplifier is presented in Figure 4-10 for operating temperatures as high as 500 °C. The measured transimpedance gain is calculated by multiplying the known R_{in} (1 MΩ) by the measured voltage gain. At room temperature, the amplifier had a measured gain of 235 kΩ at low frequency, a 3-dB bandwidth of 0.61 MHz, and an input-referred noise floor of 0.8 $pA/\sqrt{Hz}$ at 10 kHz. With V_{DD} = 20 V, V_{SS} = -10 V, and V_{bias} = -2 V, the transimpedance amplifier required 134 µA. The input dc level was -4.1 V, and the output was biased at 11.3 V.

With increasing temperature, an increasing transimpedance gain and decreasing supply current were expected. At 450 °C, the transimpedance gain was 774 kΩ with a bandwidth of 0.17 MHz and input-referred noise floor of 1.2 $pA/\sqrt{Hz}$. Above 450 °C,

however, the transimpedance gain and supply current hit a maximum and minimum, respectively, as shown in Figure 4-11. These behaviors suggested reduced resistor values, which may be caused by a decrease in the contact resistance, which is a significant contributor to the total resistance. The spike observed at the higher frequency region might have been caused by the oscillation associated with the high gain and parasitic capacitance between the input and output nodes. Adding a feedback capacitor in parallel with R_f may help stabilize the circuit at the expense of bandwidth.

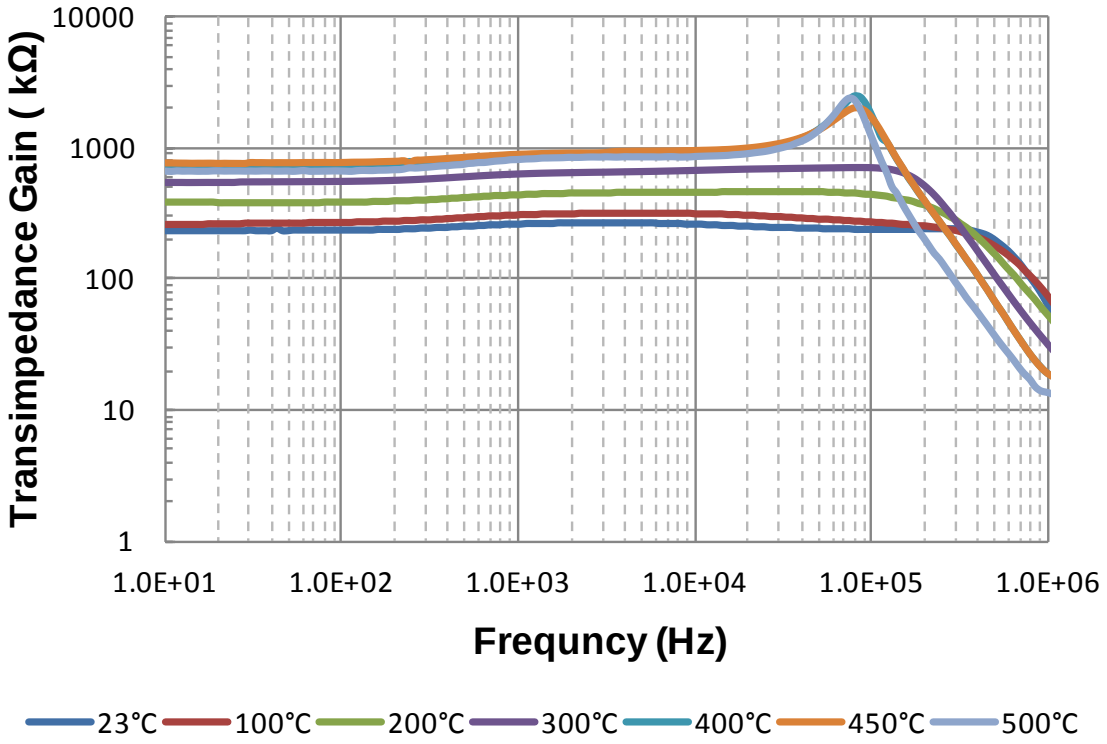


Figure 4-10 Measured frequency response of a single-stage, single-ended transimpedance amplifier (CR0975-10-R6C6) as a function of operating **temperature, with V_{DD} = 20 V, V_{SS} = V_{sub} = -10 V, V_{bias} = -2 V, and I_{in} = 1 µA.**

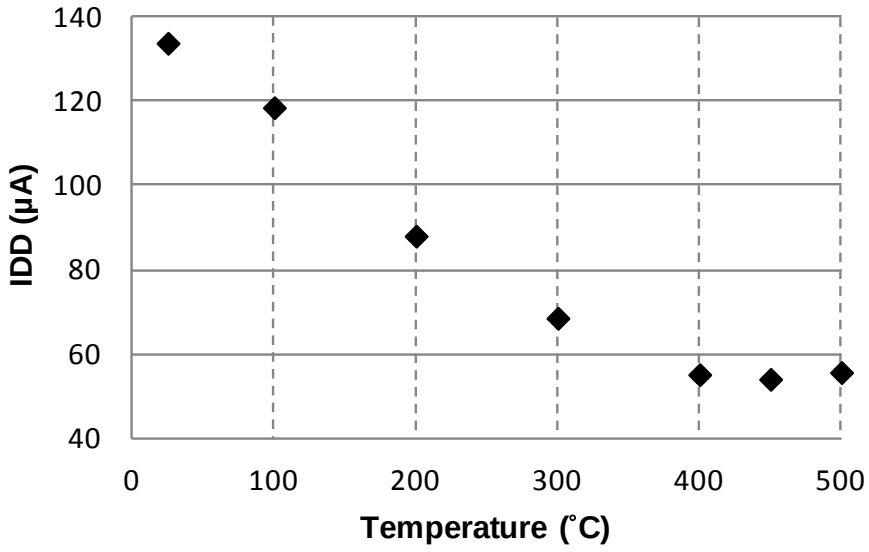
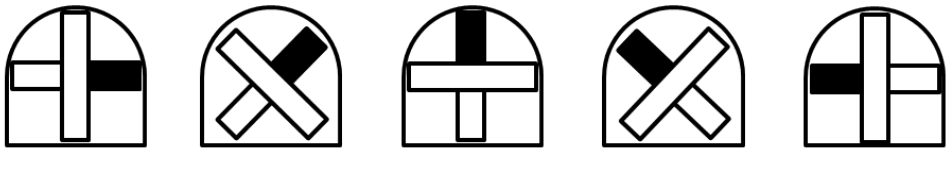


Figure 4-11 Measured supply current of a single-stage, single-ended transimpedance amplifier (CR0975-10-R6C6) as a function of operating temperature.

4.2.2 Sensor interface capability

4.2.2.1 Variable capacitor calibration

Half-turn (180 degrees) trimmer capacitors were used to demonstrate the potential of the transimpedance amplifier in capacitive sensing. The variable capacitors were first calibrated at five settings, illustrated in Figure 4-12, which shows the adjustment screw positions and their corresponding capacitance, measured using a precision capacitance meter with results of three test trials averaged.



	Pos1	Pos2	Pos3	Pos4	Pos 5
C (pF)	1.39	1.65	2.13	2.64	2.92

Figure 4-12 Calibration of the variable capacitors—screw positions and corresponding values.

The transimpedance amplifier was tested with the calibrated trimmer capacitors at room temperature as was shown in Figure 4-9. With a given stimulus level, V_{stim}, the expected output amplitude of the transimpedance amplifier is given by

$$V_{out} = 2\pi f \times \Delta C \times V_{stim} \times Rm\_Gain(f) \qquad (4.1)$$

where ΔC is the capacitance difference between the variable and reference capacitors. *Rm_Gain(f)* is the transimpedance amplifier gain that was previously measured using a known 1-MΩ resistor. With the reference capacitor's value fixed at Pos3 (half way from

minimum to maximum), the transimpedance amplifier output was measured using five different screw positions for the variable capacitor, i.e., from minimum to maximum capacitance value. The nominal operating conditions were V_{DD} = 20 V, V_{SS} = -10 V, V_{bias} = -2 V, V_{stim} = 30 Vp-p, and f = 10 kHz.

The output amplitude of the transimpedance amplifier was in excellent agreement with the expected values, as shown in Figure 4-13. The difference between the measured and expected output amplitudes was mostly due to the uncertainty of the position of the adjustment screw.

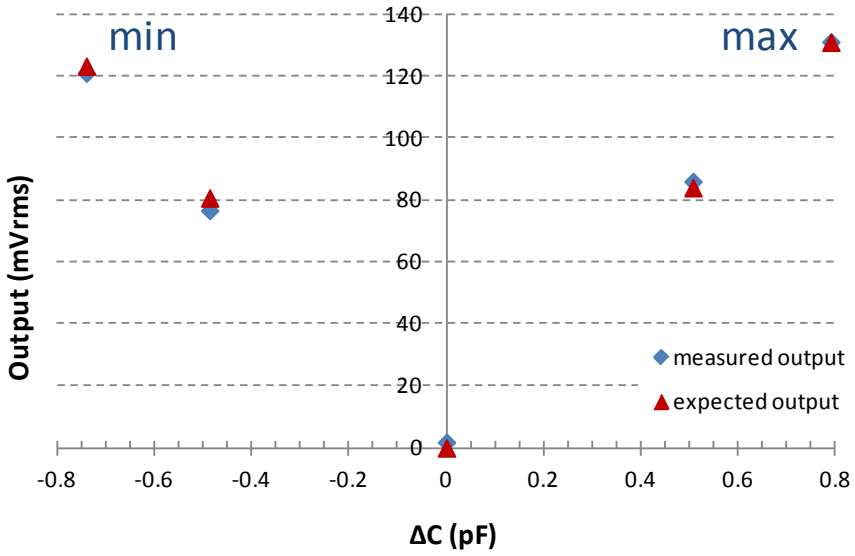


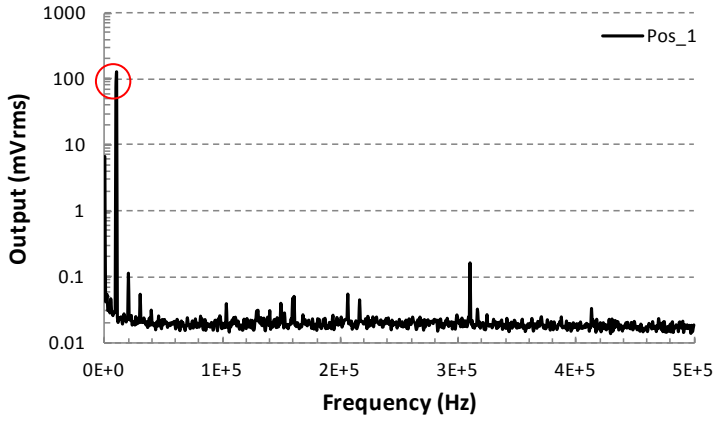
Figure 4-13 Single-stage, single-ended transimpedance amplifier output versus input ΔC at room temperature.

Table 4-4 Table of measured output and expected output from the single-stage, single-ended transimpedance amplifier.

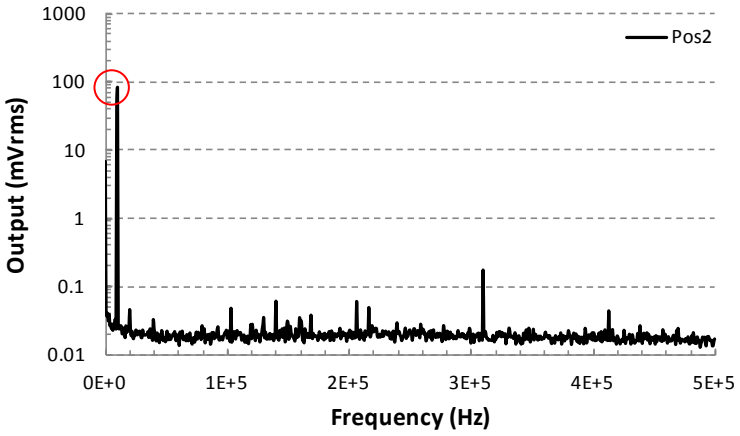
ΔC (pF)	-0.74	-4.87	0	0.50	0.79
Measured output (mVrms)	121.02	76.65	1.83	86.05	131.11
Expected output (mVrms)	123.27	80.71	0	84.02	131.02

Figure 4-14 shows a frequency spectrum plot of measured output of the transimpedance amplifier with 1 kHz stimulus signal. The amplifier output as a function of input stimulus frequency is presented in Figure 4-15. As expected, the amplitude of the voltage increases proportionally with frequency across this wide dynamic range, which further proves that the change of capacitance is indeed being sensed and amplified by the transimpedance amplifier.

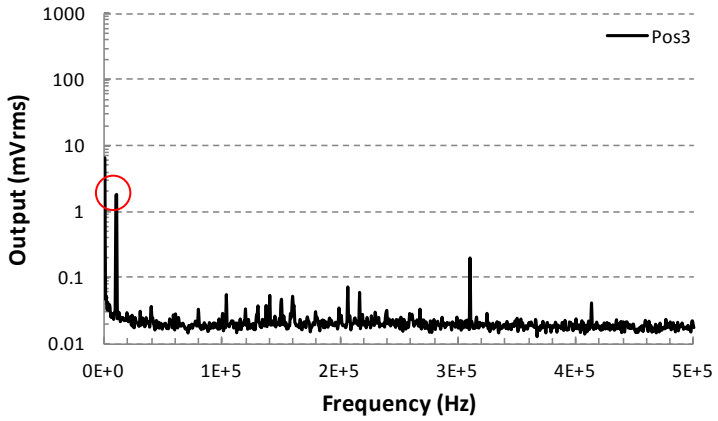
Next, gain sensitivity to power supply change (i.e., changes in V_{DD} and V_{SS}) is measured, as illustrated in Figure 4-16. Transimpedance gain is quite stable, ~1% variation, with respect to positive supply voltages V_{DD} ranging from 12 V to 25 V. Transimpedance gain is more sensitive to the negative supply voltage, for which a variation of ~11% was measured for V_{SS} ranging from -10 V and -20 V. Thus, it appears that the effects of the finite output impedance of transistors J3 and J4 are mostly cancelled, while that of J5 is contributing more to the transimpedance gain.


1000
100
10
1
0.1
0.01
Output (mVrms)
Pos_1
0E+0
1E+5
2E+5
3E+5
4E+5
5E+5
Frequency (Hz)

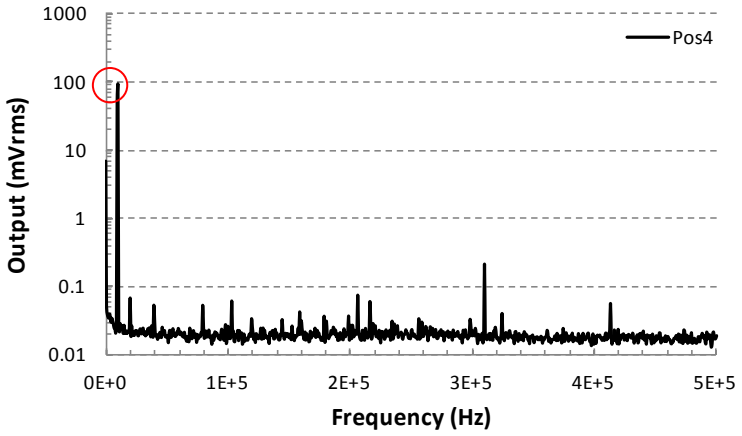
(a)


1000
100
10
1
0.1
0.01
Output (mVrms)
Pos2
0E+0
1E+5
2E+5
3E+5
4E+5
5E+5
Frequency (Hz)

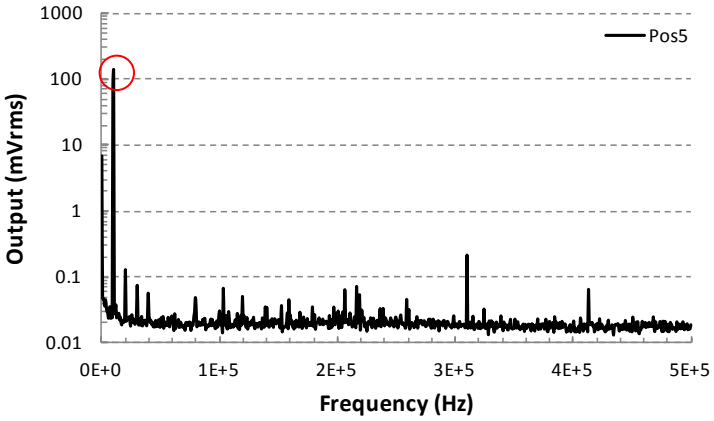
(b)


1000
100
10
1
0.1
0.01
Output (mVrms)
Pos3
0E+0
1E+5
2E+5
3E+5
4E+5
5E+5
Frequency (Hz)

(c)



(d)



(e)

Figure 4-14 Measured output of the transimpedance amplifier with 1 *k*Hz stimulus signal. V_{DD} = 20 V, V_{ss} = -10 V, V_{bias} = -2 V, and five adjustment screw positions.

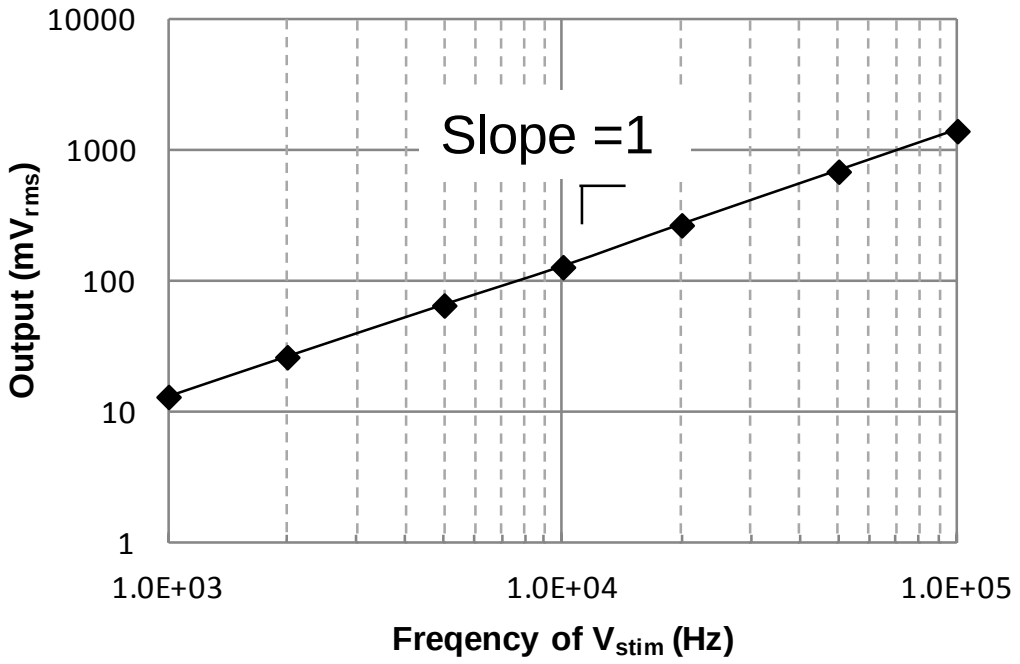
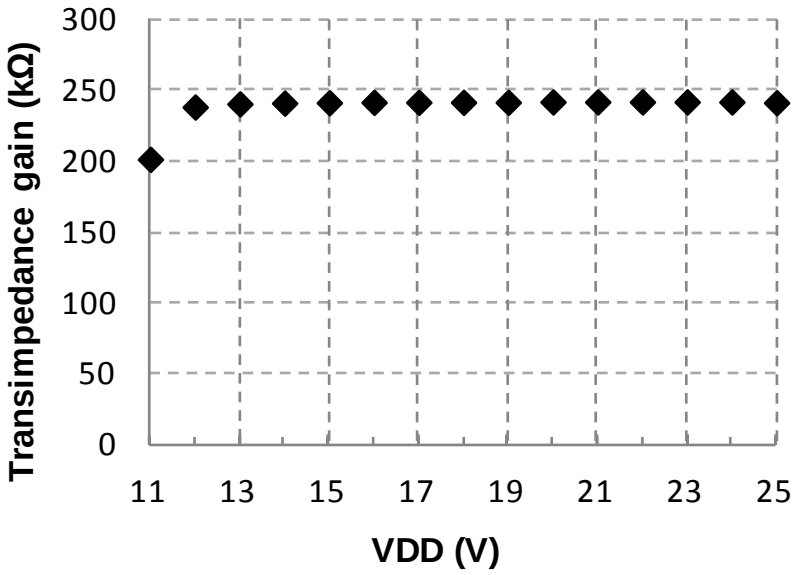
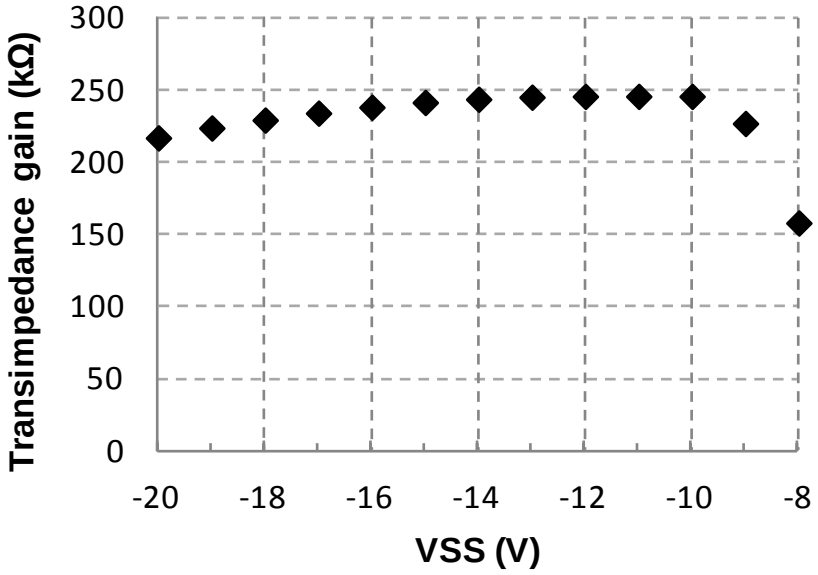


Figure 4-15 Measured output of the transimepedance amplifier versus varying frequency of stimulus signal. V_{DD} = 20 V, V_{ss} = -10 V, V_{bias} = -2 V, and ΔC = max.



(a)



(b)

Figure 4-16 Gain sensitivity to (a) positive and (b) negative power supply voltages with $V_{DD,nom}$ = 20V, $V_{SS,nom}$ = -10V, V_{bias} = -2 V, and ΔC = max.

4.2.2.2 High temperature test results

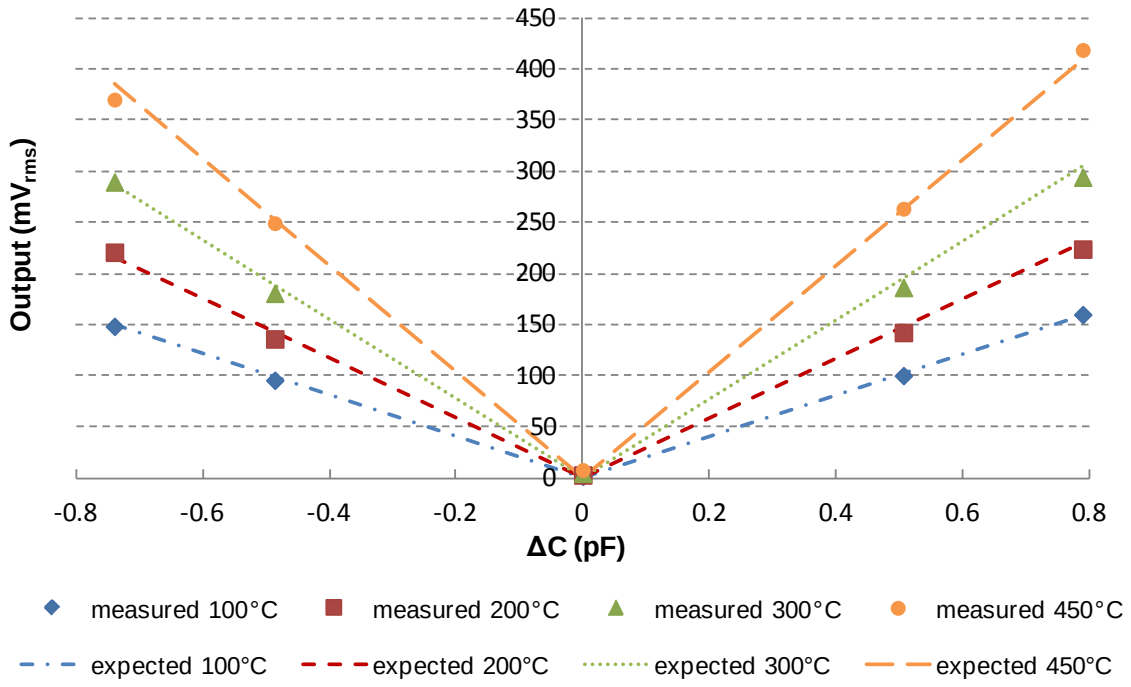


Figure 4-17 Measured and expected output of transimpedance amplifier output as a function of operating temperature.

Finally, the transimpedance amplifier was heated using the spot infrared heater and tested with the trimmer capacitors at five different operating temperatures up to 450 °C. The measured and expected output amplitudes are shown in Figure 4-17. As before, the measured results were consistent with the expected output calculated from Equation (2) using the transimpedance gain that was measured with the known 1-MΩ resistor. Each data point is recorded 5 minutes after reaching the given temperature. Similar to the measured results at room temperature, the difference between the measured and expected output amplitudes was thought to be largely due to the uncertainty of the position of the adjustment screw.

4.3 Summary

SiC-based integrated circuits for high temperature sensing applications were demonstrated across a wide operating temperature range. All logic circuits, including core inverter, NAND and NOR gates, function with high performance at operating temperatures from 25 °C to 550 °C. The DC and transient characteristics of JFET-based, 6H-SiC inverters, NAND, and NOR gates have been designed to achieve and maintain a sharp and stable dc transfer characteristic with large noise margin for operating temperatures up to 550 °C.

A fully monolithic, single-stage, single-ended transimpedance amplifier was characterized at operating room temperature to 450 °C. At room temperature, a high gain-bandwidth of 235 kΩ by 0.61 MHz and power consumption of 4.5 mW were measured. At elevated temperatures, the gain increased as expected (e.g., 774 kΩ at 450°C) and bandwidth remained >0.17 MHz. The capacitive sensing capability was demonstrated using trimmer capacitors to simulate sensing elements, with the IC operated to 450 °C.

5 6H-SiC Device Characterization

5.1 Noise Analysis of Integrated Amplifiers

5.1.1 Sources of noise in semiconductors

Thermal noise

Thermal noise (Johnson noise) occurs in any linear passive resistor. It is generated by current or voltage fluctuations due to the random thermal motion of the electrons. Thermal noise is the fundamental noise in electronics and it is determined by

$$\overline{V^2} = 4kTR\Delta f \tag{5.1}$$

$$\overline{I^2} = 4kT\Delta f/R \tag{5.2}$$

Thermal noise is independent to frequency and directly proportional to temperature.

Shot noise

Shot noise is related to direct current flow in diode or p-n junctions and is generated randomly. It was first introduced by Schottky and is generally defined by

$$\overline{I^2} = 2qI_D\Delta f \tag{5.3}$$

where I_D is average current across the device. Shot noise is proportional to the measured bandwidth.

Flicker noise

The mechanism of flicker noise is not well-understood like other noise sources. It is associated with capture and release by traps and mostly occurs in low frequency. Flicker noise is described by

$$\overline{I^2} = \frac{k_i\Delta f}{f^{\alpha}} \tag{5.4}$$

where K_i is constant for the particular process or device, and α is usually unity. Therefore flicker noise is often called 1/f noise.

Generation-recombination noise

This type of noise is caused by the carrier fluctuation during the generation – recombination process of traps. It is associated with temperature, bias conditions and frequency. It usually decreases as $1/f^2$.

Burst noise

Burst noise is also called popcorn noise and it is of similar form as generation-recombination noise decreasing as $1/f^2$.

5.1.2 Noise in SiC-based devices

At low frequency, $1/f$ noise in 6H-SiC JFETs were reported in [45-46] up to 600 K (327 °C) and it is also reported in 4H-SiC JFET [47]. $1/f^{1.5}$ noise in SiC JFETs was proved to be associated with surface noise induced by passivation layer [48] as shown in Figure 5-1. Later, $1/f^{\gamma}$ noise where γ = 1.3 - 1.5 was observed in low frequency on SiC FET devices at low frequency [49]. $1/f^{1.5}$ noise at very low frequency was attributed to be bulk noise in [50-51]. At T > 600 K, the main noise contribution was reported to arise from generation-recombination noise at the local level. In these cases, Hooge parameter for SiC JFETs was further determined to be ~10^{-5}. At room temperature, $1/f^{\gamma}$ noise (where 0.73< γ < 0.847) was also found in [52] for 6H-SiC MOSFETs.

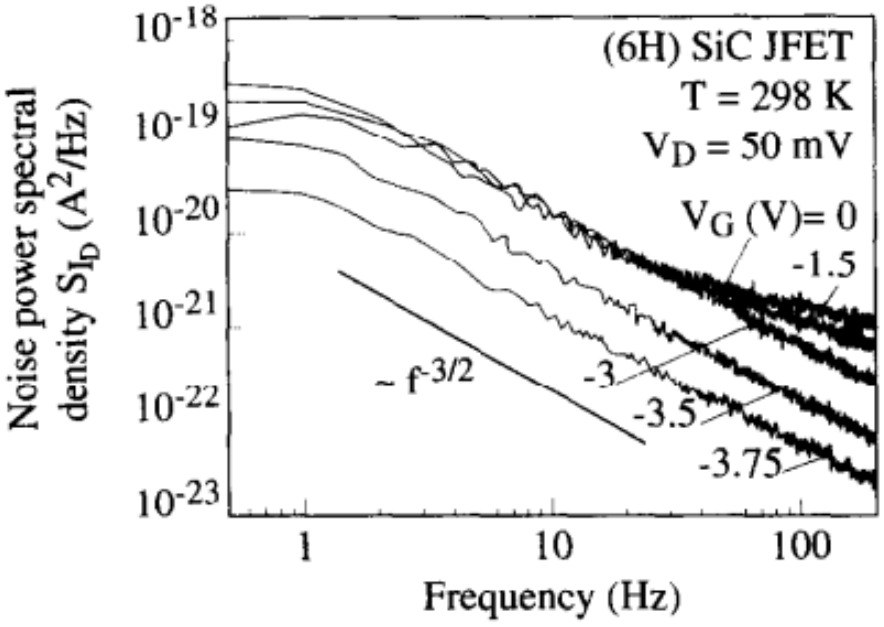


Figure 5-1 Noise spectra at 25 °C for a 6H-SiC JFET device under different bias conditions [48].

5.1.3 Test results

In single-stage or two-stage integrated amplifiers, the differential pair is the major noise contributor. The noise behavior of a differential pair is shown in Figure 5-2. The output thermal noise of the differential pair is determined by

$$\overline{V_{n,out}^2} = \left(\overline{I_{n1}^2} + \overline{I_{n2}^2}\right) r_o^2 = 4kT\left(\frac{2}{3}g_m + \frac{2}{3}g_m\right) r_o^2 = 2\frac{8}{3}kTg_m r_o^2. \qquad (5.5)$$

Since the voltage gain of the differential pair is equal to $g_m r_o$, the input-referred noise can be given by

$$\overline{V_{n,in}^2} = \frac{\overline{V_{n,out}^2}}{\text{gain}^2} = \frac{\overline{V_{n,out}^2}}{(g_m r_o)^2} = 2\frac{8}{3}\frac{kT}{g_m} \qquad (5.6)$$

For the designed parameters: $V_{GS} - V_T = 0.5\text{V}$ and $^{W}/_{L} = 252$, the input referred noise level is calculated to be ~ 8.6 $\text{nV}/\sqrt{\text{Hz}}$.

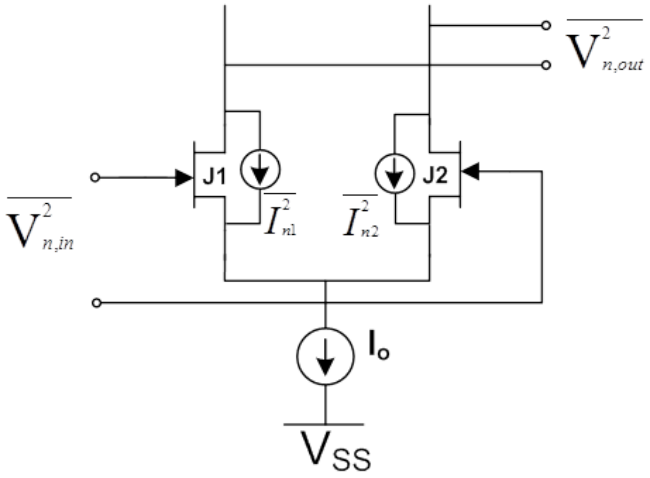


Figure 5-2 Differential pair circuit including input-referred noise model.

Noise measurement of integrated amplifiers, including differential pair, single–stage differential amplifier with resistive loads, and two-stage amplifier with current source load for 1st stage and resistor load for 2nd stage was carried out at room temperature and elevated temperatures. Amplifiers were packaged for measurement. Figure 5-3 shows a schematic of the amplifier test setup. R_{in} and R_f resistors are used to stabilize the operating point where R_{in} =3.48 MΩ and R_f = 22MΩ.

The amplifiers were packaged in a ceramic dual-in-line package using gold bond wires. A spot infrared heater was used to heat the IC/die; all measurements were performed in an ambient environment.

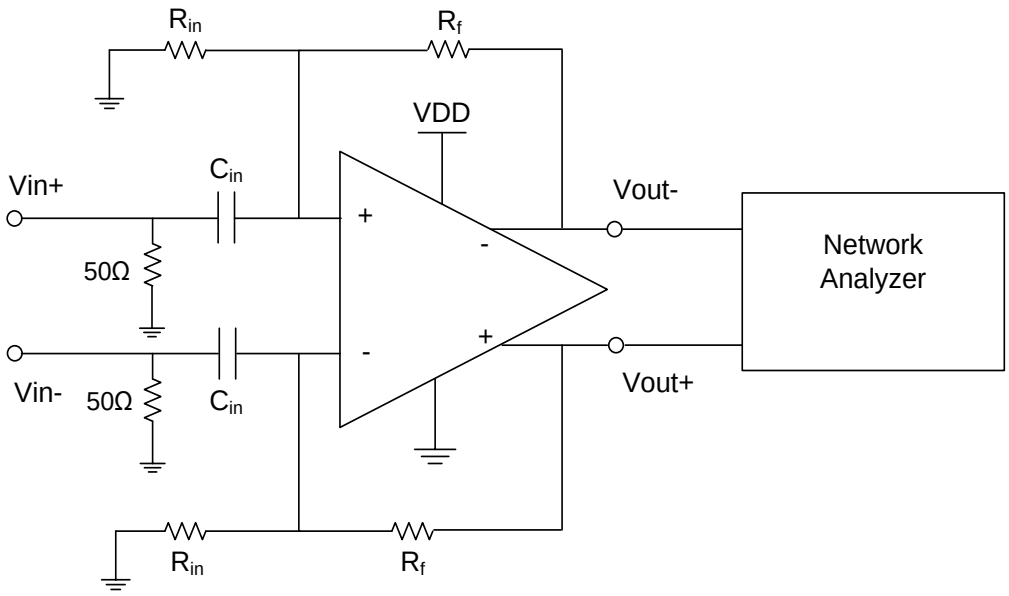


Figure 5-3 Test setup for noise measurement of SiC-based amplifiers.

5.1.3.1 Single stage differential amplifier

At room temperature, $1/f^{1.5}$ noise in frequency up to ~20 Hz is observed in one of our differential pair sample (CR0975-12-R4C6) as shown in Figure 5-4. The $1/f$ is dominant between ~20 Hz to ~ 100Hz. A 92 $nV/\sqrt{Hz}$ input-referred thermal noise level presents above 100 Hz which is ~10 times larger than the theoretical value.

$1/f^{1.5}$ and $1/f$ noise were consistent for all temperatures up to 500 °C as shown in Figure 5-5. Thermal noise increased with temperature, being proportional to T/g_m where g_m decreases as temperature increases. At 200 °C, the measurement showed an increase of 1.7x, which is lower than the expected value of 2.3x. At 500 °C, only flicker noise was observed.

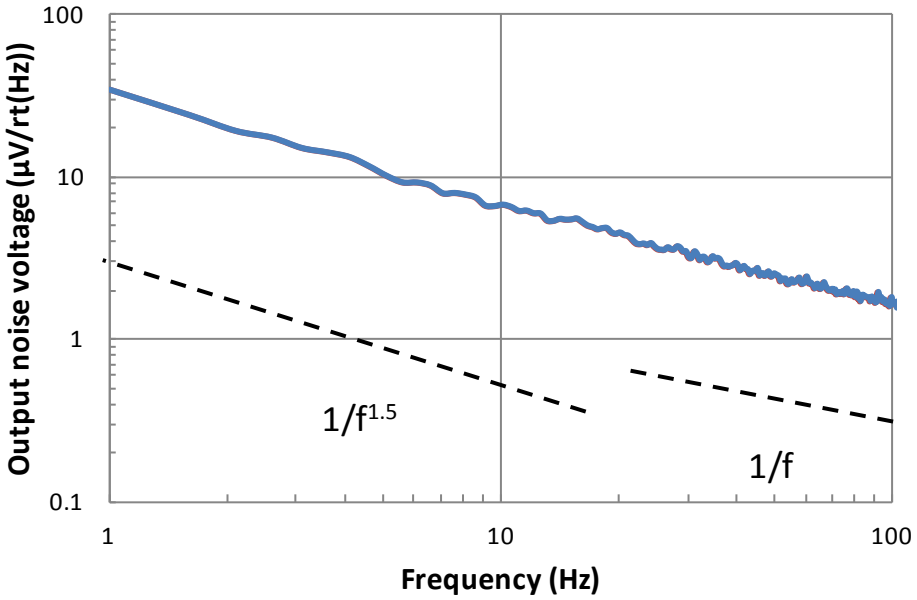


Figure 5-4 Output-referred noise voltage of a differential-pair at room temperature.

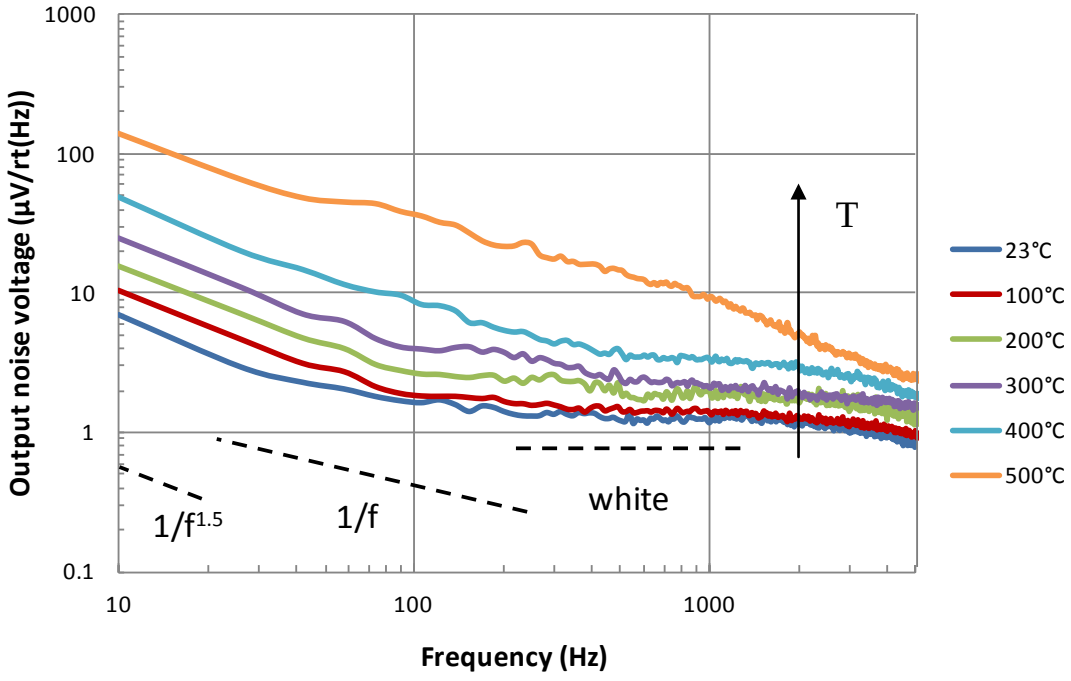


Figure 5-5 Output-referred noise voltage of a differential pair at elevated temperatures.

5.1.3.2 Single-stage amplifier with resistor load

In this sample (CR0975-12-R4C5), only $1/f$ noise is observed up to 10 kHz as shown in Figure 5-6. The $1/f$ dependence is consistent at every operating temperature up to 500 °C. Taking this sample as an example, in a frequency bandwidth of interest, the total output referred noise is given by

$$\overline{V_{n,out}^2} = \int_{f_L}^{f_H} \frac{K}{f} df \tag{5.7}$$

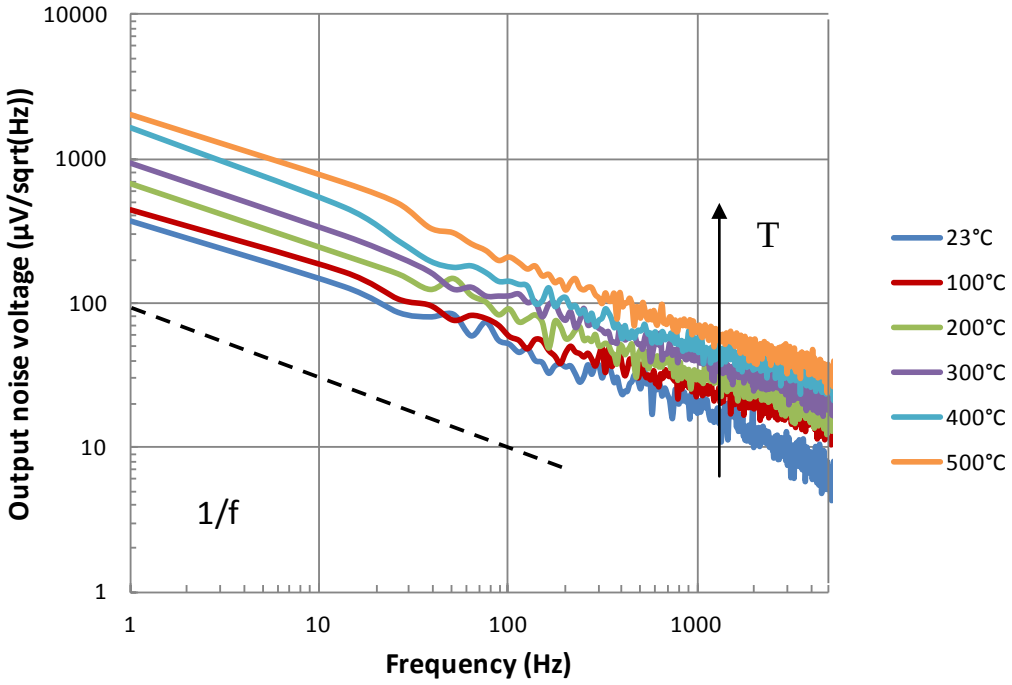


Figure 5-6 Output-referred noise voltage of a single-stage amplifier with resistor loads at elevated temperatures.

At 1 Hz, the noise spectral density is 438 $\mu V/\sqrt{Hz}$; therefore, the total equivalent input referred noise in the 1 to 10 *k*Hz band is

$$\overline{V_{n,out}^2} = \int_{f_L=1\,Hz}^{f_H=1\,kHZ} \frac{K}{f} df = (438\ \mu V)^2 \ln\frac{10000}{1}$$

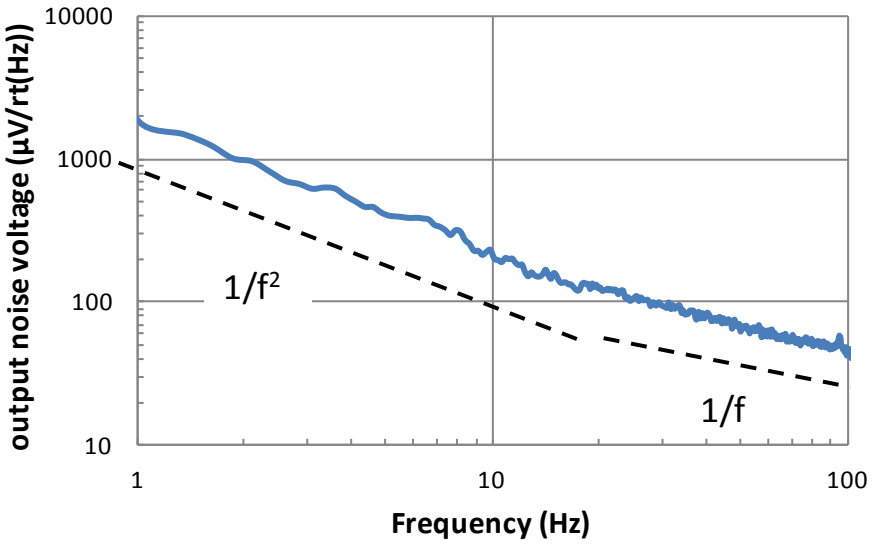
$$\overline{V_{n,out}} = 438\mu V\sqrt{\ln\frac{10000}{1}} = 438\ \mu V \times \sqrt{\ln 10000} = 1329.3\ \mu V$$

$$\overline{V_{n,in}} = \frac{\overline{V_{n,out}}}{\text{gain}} = 23.6\ \mu V_{rms}$$

where gain is 56.2 at room temperature. It was noticeable that the absence of thermal noise level in the measurement plot was because of the large level of flicker noise. At 500 °C, the input noise voltage was 118.3 μV_{rms}.

5.1.3.3 Two-stage amplifier with current source load in the 1st stage and resistive load in the 2nd stage

$1/f^2$ noise in frequencies up to ~20 Hz was observed in one of the two-stage



amplifiers (CR0975-12-R4C6) with current source load in the 1st stage and resistive load in the 2nd stage, as shown in Figure **5-7**. Above 20 Hz, $1/f^2$ dependence was reduced to the power of 1; $1/f$ was dominant at frequencies above 20 Hz. It was noticeable that thermal noise was not observed 10 kHz in this sample, perhaps be due to the high $1/f^{\gamma}$ noise.

Figure 5-8 shows the input referred noise density at elevated temperatures. $1/f^2$ dependence was observed for all operating temperatures up to 500 °C. Above ~20 Hz, $1/f$ dependence was generally observed at each temperature.

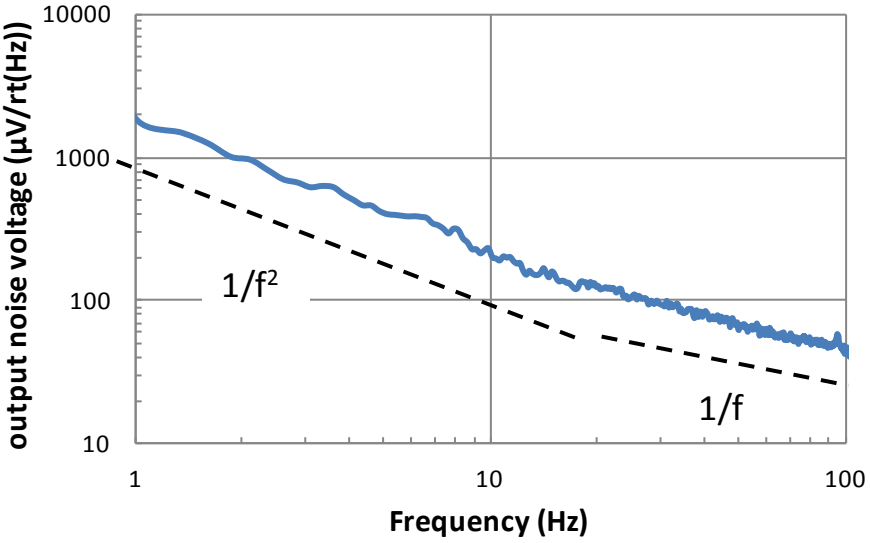


Figure 5-7 Output-referred noise voltage of a two-stage amplifier with current source load in the 1st stage and resistive load in the 2nd stage.

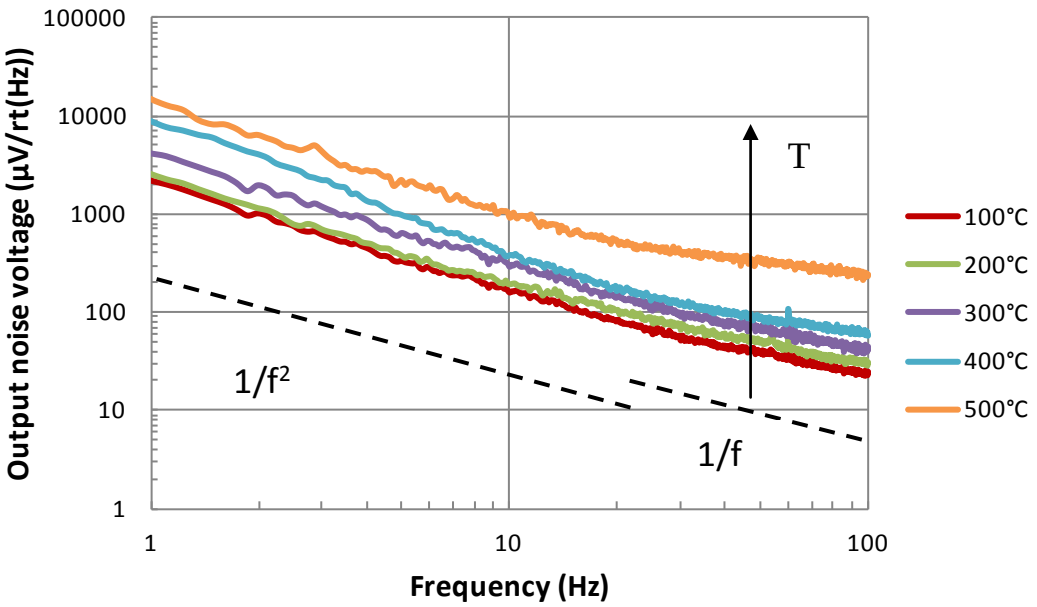


Figure 5-8 Output-referred noise voltage of a two-stage amplifier with current source load in the 1st stage and resistive load in the 2nd stage.

5.1.4 Discussion

$1/f^{\gamma}$ noise was observed in our 6H-SiC amplifiers, where $1< \gamma < 2$. The higher values of γ were observed in the lower frequency range. Above a few tens of Hz, γ decreased to close to unity. The noise behavior observed in our samples implied the existence of defects in the epitaxial layers and substrate. Although a universal noise mechanism/model could not be identified here, the noise study provided a better understanding (i.e., $1/f^{\gamma}$ noise dependence) of our 6H-SiC technology.

5.2 P-N Junction Characterization of 6H-SiC JFET

5.2.1 Theory of p-n Junction

In order to understand the physical limitation of our 6H-SiC JFET devices and circuits behaviors, it is necessary to study the I-V characteristics of p-n junctions in our devices.

5.2.1.1 Thermal equilibrium

In the absence of external biased, the total charge in the p-region need to be equal to that in n-region, which is

$$N_a W_p = N_d W_n \tag{5.8}$$

where W_i is the depletion width in the certain region. The total depletion width can be calculated by

$$W_d = \sqrt{\frac{2\varepsilon(N_a+N_d)V_{bi}}{qN_aN_d}} \tag{5.9}$$

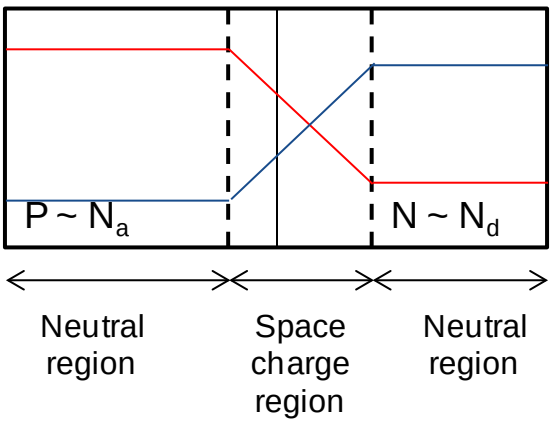


Figure 5-9 P-n junction in thermal equilibrium (without bias).

5.2.1.2 Forward bias

Under forward bias, the voltage mainly drops across the depletion region. In other word, the supply voltage reduces the built-in field by reducing built-in potential. As a consequence, holes diffuse into the n-region (or electrons into the p-region). The total excess hole current injected into the n-region is given by

$$I_{IN} = \frac{AqD_p}{L_p}\Delta p_{n,max} = \frac{AqD_p}{L_p} p_{no}(e^{V_D/V_T} - 1)\ . \tag{5.10}$$

Similarly, the total electron current injected into the p-region is given by

$$I_{IP} = \frac{AqD_n}{L_n} n_{po}(e^{V_D/V_T} - 1). \tag{5.11}$$

The current in p-n diode is the sum of the hole and electron currents

$$I = I_{IN} + I_{IP} = (\frac{AqD_p}{L_p} p_{no} + \frac{AqD_n}{L_n} n_{po})(e^{V_D/V_T} - 1) \tag{5.12}$$

The saturation current I_s is defined as

$$I_s \equiv qA\left(\frac{D_p p_{no}}{L_p} + \frac{D_n n_{po}}{L_n}\right), \tag{5.13}$$

Therefore, an ideal diode equation can be expressed as

$$I_D = I_s(e^{V_D/V_T} - 1). \tag{5.14}$$

This equation is also called the Shockley equation. For a practical diode however, the I-V behavior must be described in an improved form.

5.2.1.3 Generation-recombination process

We now consider the recombination-generation in the depletion region of a p-n junction. During forward bias, both holes and electrons exceed their equilibrium

concentration values. Therefore, the carrier concentrations will try to return to the thermal equilibrium state by recombination.

$$J_F = J_{F,diff} + J_{F,rec} = q\sqrt{\frac{D_P}{\tau_p}}\frac{n_i^2}{N_D}e^{qV/kT} + \frac{qn_iW_D}{2\tau_r}e^{qV/2kT} \qquad (5.15)$$

where τ_r is the effective recombination lifetime.

Under reverse bias conditions, only junction generation currents exist due to the lack of free carriers in the depletion region, making the capture rates negligible. The total reverse bias current in a p-n junction is the sum of diffusion current in the neutral region and the generation current in the depletion region:

$$J_R = J_{R,diff} + J_{R,gen} = q\sqrt{\frac{D_P}{\tau_p}}\frac{n_i^2}{N_D} + \frac{qn_iW_D}{\tau_g} \qquad (5.16)$$

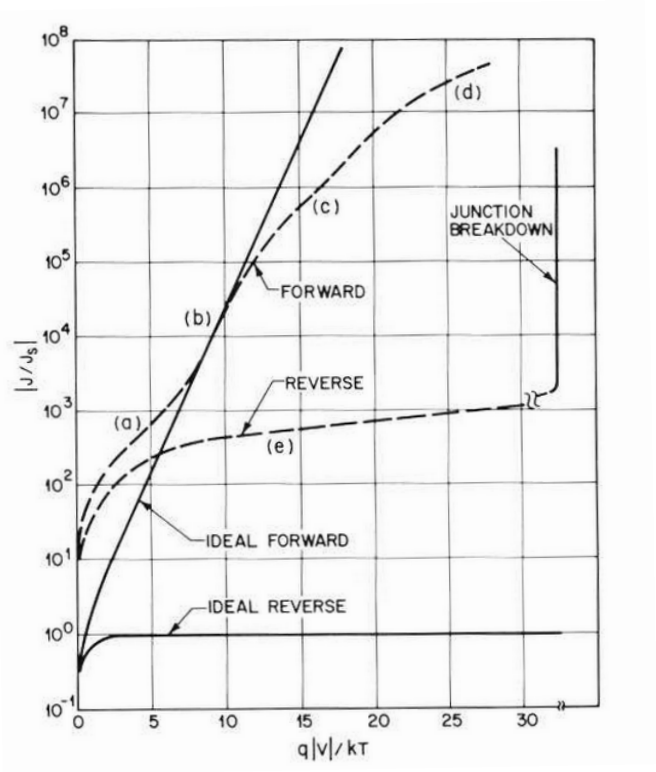
where, τ_p is the minority carrier lifetime (holes) in *n* region, $\tau_g$is the generation lifetime, and W_D is the depletion width of the p-n junction. Because of the low intrinsic carrier concentration in SiC, it is the *generation current* in depletion region that is the dominant reverse current of the p-n junction.

5.2.1.4 High injection and series resistance

In practice, p-n diodes are also affected by: (1) high injection, which occurs under forward bias conditions wherein minority carrier density exceeds/ or is comparable with majority carrier density; and (2) series resistance due to contact resistance between metal and semiconductor or semiconductor resistance, which at higher bias voltages limits the current.

Figure 5-10 describes the I-V characteristics of both ideal and practical p-n diodes. When the total forward current is dominated by the diffusion current, η is close to unity.

When the recombination current is dominant, $\eta = 2$. If both diffusion and recombination currents contribute, $1 < \eta < 2$.



(a) generation-recombination current
(b) diffusion current
(c) high-injection
(d) series resistance
(e) reverse current: generation-recombination

Figure 5-10 I-V characteristics of a silicon diode [10].

5.2.2 I-V characterizations of parasitic p-n diode

All the tested devices were first characterized on a probe station at room temperature. Selected samples were later wire bonded in a dual-in-line ceramic package and heated by a spot IR heater for high temperature measurements. The test setup for the p-n junction I-V characterization is shown in Figure 5-11.

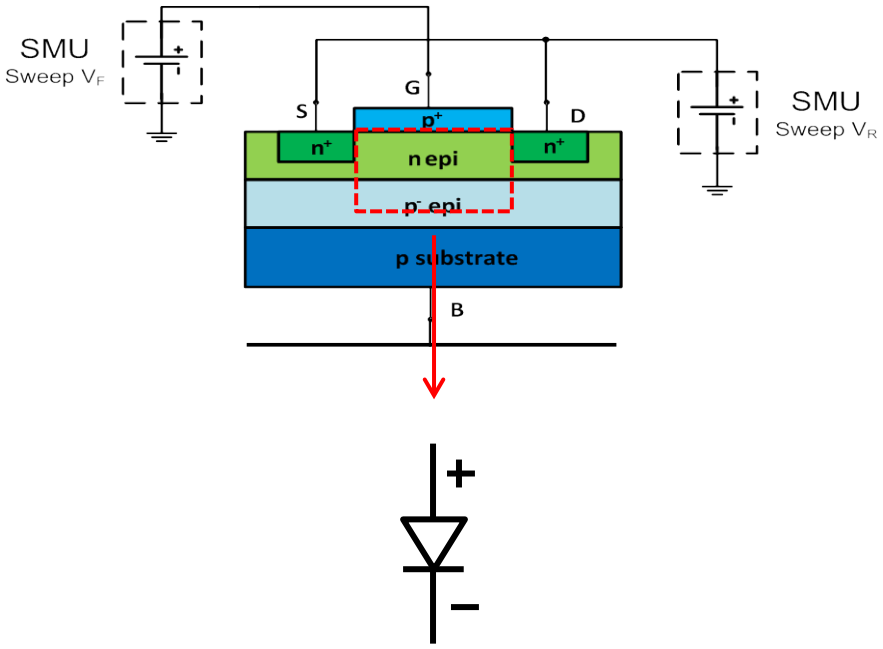


Figure 5-11 Setup for characterization of the parasitic p-n diode I-V behavior.

5.2.2.1 Room temperature test results

The measured forward I-V characteristics from three copies of parasitic p-n diode with junction area of 1×10^{-4} cm^2 (W/L = 100µm/100µm JFET) are shown in Figure 5-12. Two well-behaved p-n diodes (CR0975-12-R5C4, CR0975-12-R5C5) and a leaky p-n diode (CR0975-12-R3C4) were seen. The leaky device had higher saturation current, as well as a high ideality factor η (Table 5-1). The well-behaved devices showed η close to 2 at room temperature, suggesting recombination current as the dominant forward current in the space charge region [53-54]. (η will be closer to one if the diffusion current dominates the forward current mechanism.)

Devices with large junction area, 2.5×10^{-3} cm^2 (W/L = 500µm/500µm JFET), were tested and the forward-biased I-V characteristics are shown in Figure 5-13. Compared with small-junction-area devices, all three randomly picked samples were leaky, with large η (Table 5-2). The tunneling effect may explain such behavior [53, 55-56].

Reverse-biased I-V characteristic of small-junction-area devices and large-junction-area devices are shown in Figure 5-14(a) and Figure 5-14(b), respectively. Overall, large-junction-area devices exhibited higher reverse current, likely due to capturing more of the crystal defects.

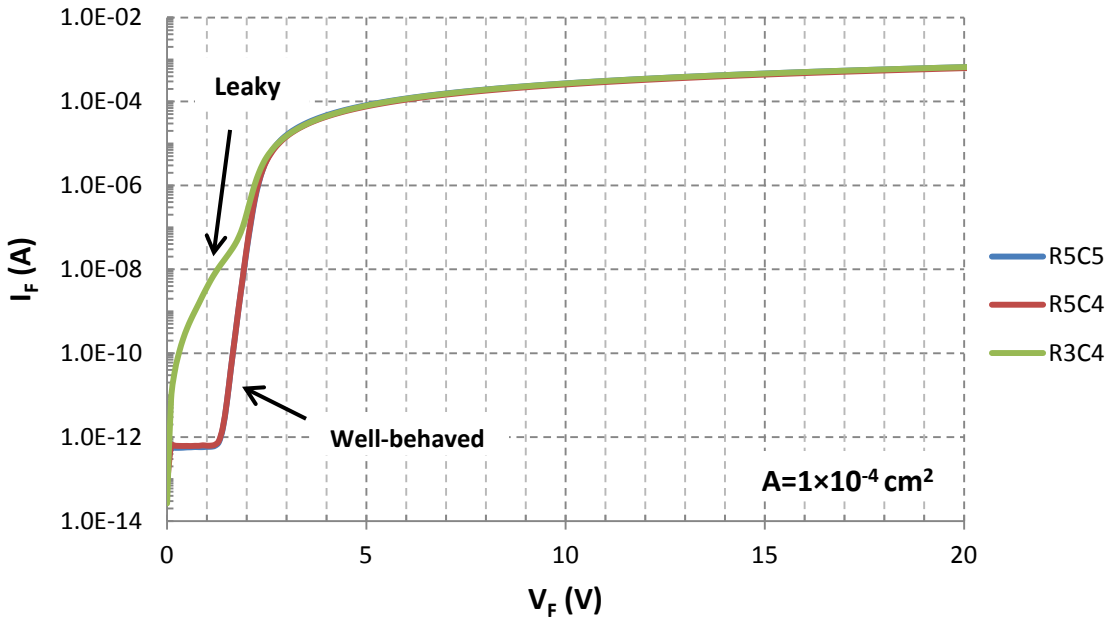


Figure 5-12 Measured forward-bias I-V characteristics at room temperature for three copies of devices with junction areas of 1×10^{-4} cm^2.

Table 5-1 Calculated saturation current (I_s) and ideality factor (η) of the devices in Fig. 5-12.

	Saturation current (I_s)	Ideality factor (η)
R3C4	8.1×10^{-14} A	5.2
R5C4	1.2×10^{-20} A	2.1
R5C5	1.2×10^{-20} A	2.1

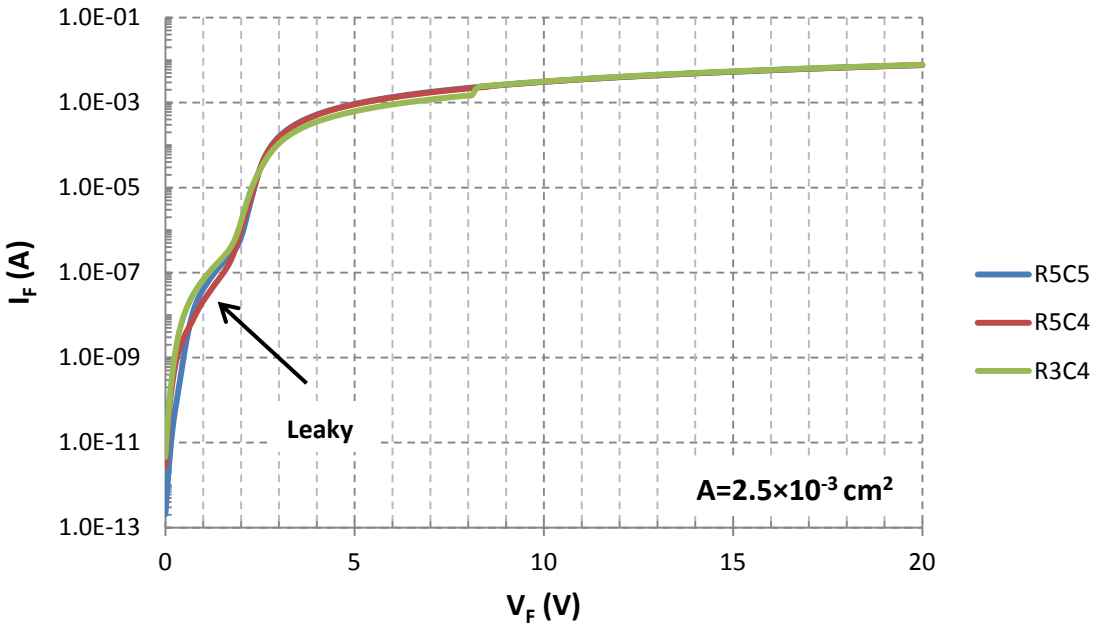
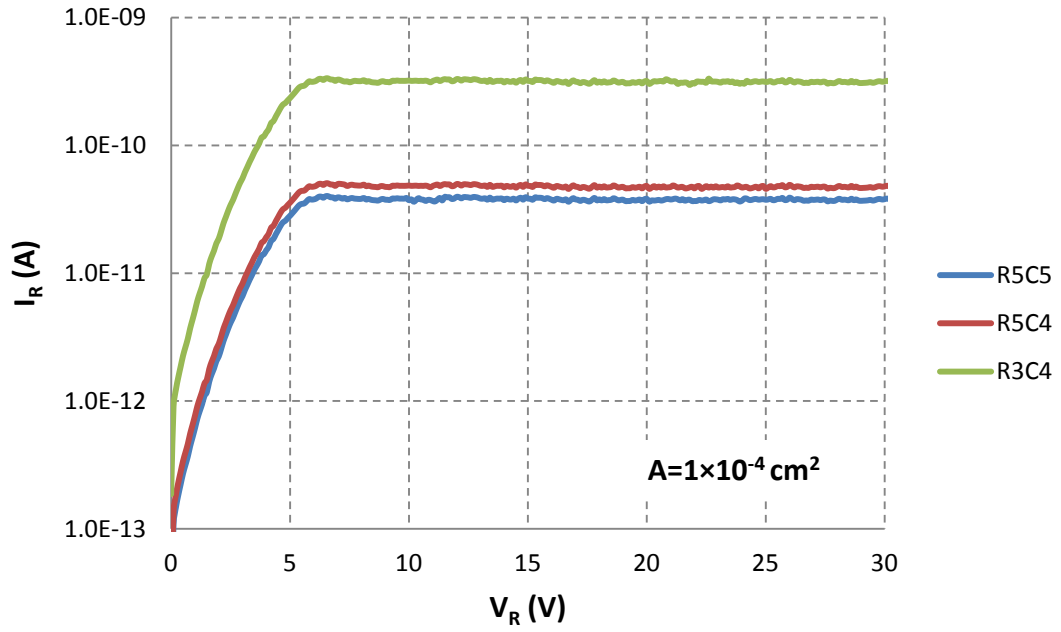


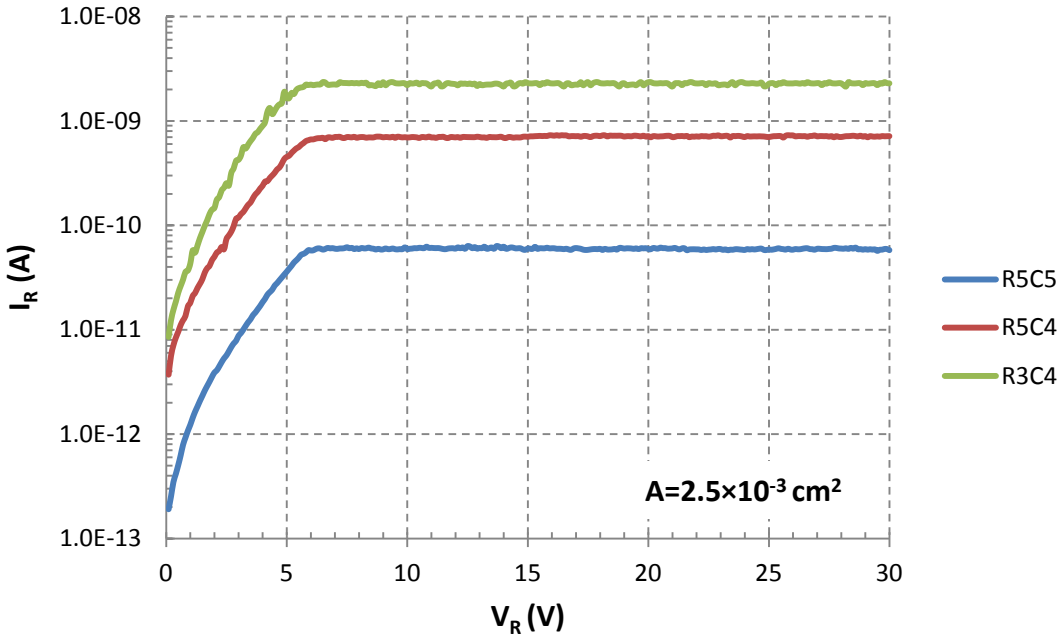
Figure 5-13 Measured forward-bias I-V characteristics at room temperature for three copies of devices with junction areas of 2.5×10^{-3} cm^2.

Table 5-2 Calculated saturation current (I_s) and ideality factor (η) of the devices in Fig. 5-13.

	Saturation current (I_s)	Ideality factor (η)
R3C4	2.3×10^{-12} A	5.7
R5C4	1.9×10^{-12} A	5.9
R5C5	8.0×10^{-14} A	4.9



(a)



(b)

Figure 5-14 Measured reverse-bias I-V characteristics of the devices of (a) Fig. 5-12 and (b) Fig. 5-13.

5.2.2.2 High temperature test results

The forward I-V characteristics as a function of temperature are shown for 100μm/100 μm devices in Figure 5-15. Since the built-in potential has negative temperature dependence, the measured results were expected to have decreasing turn-on voltage with increasing temperature. The activation energy, E_a, for the well-behaved device ($\eta = 2$, recombination current dominant in the forward current) is calculated by fitting the measured data with Arrehenius equation given by

$$y = Ae^{-E_a/kT} \tag{5.17}$$

where k is Boltzmann constant. For the recombination current curve fitting, the alternative form of Arrehenius equation was used:

$$I_s \propto T^{5/2} e^{-E_a/kT} \tag{5.18}$$

The saturation current as a function of temperature is shown in the Arrehenius plot of Figure 5-16. The calculated activation energy for the well-behaved p-n diode is ~1.21eV, compared with ideal activation energy of $E_g/2 = 3/2 = 1.5$ eV for generation-recombination current in a 6H-SiC diode:. In an ideal p-n junction, the activation energy of the recombination current is usually close to half of the bandgap.

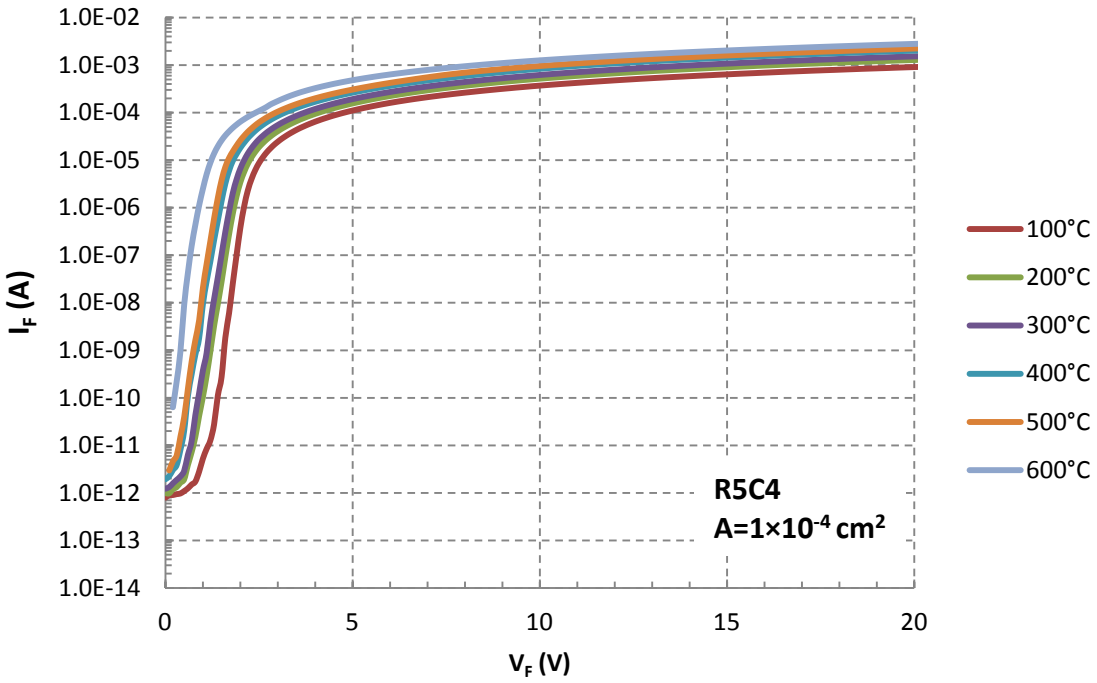


Figure 5-15 Measured forward-bias I-V characteristics of a device with junction area of 1×10^{-4} cm^2 as a function of temperature.

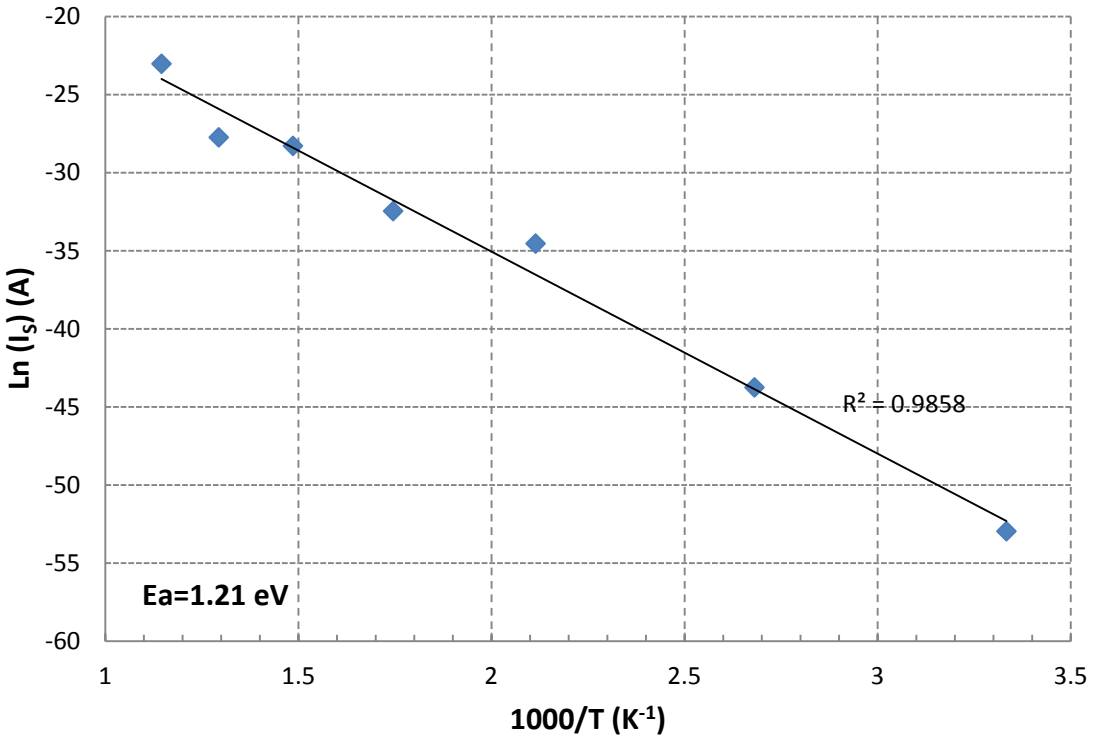


Figure 5-16 Arrhenius plot showing temperature dependence of saturation current with calculated activation energy E_a = 1.21 eV.

Reverse-bias I-V characteristics measured as a function of temperature are shown in Figure 5-17. Reverse current increases with increasing temperature as expected, due to the temperature dependence of generation-recombination current. The calculated generation current component of reverse current density in our 6H-SiC p-n junctions is shown in Figure 5-18. For a junction area = 1×10^{-4} cm^2, the theoretical reverse leakage current at 600 °C is only ~3.0 nA. The mechanism of the excessive reverse leakage current observed needs further studied. At a given temperature, the reverse current is proportional to the square root of the applied voltage ($J_{gen}\sim(V_{bi}+V)^2$), which also agrees with our measured characteristic.

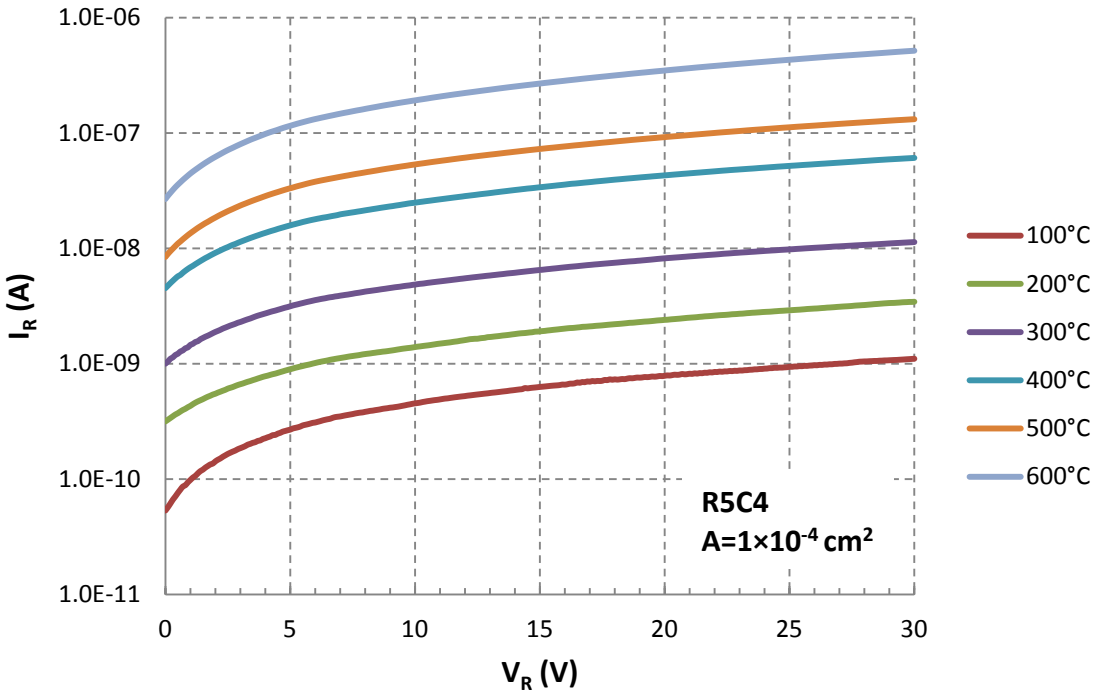


Figure 5-17 Measured reverse-bias I-V characteristics as a function of temperature for of the device with the junction area of 1×10^{-4} cm^2.

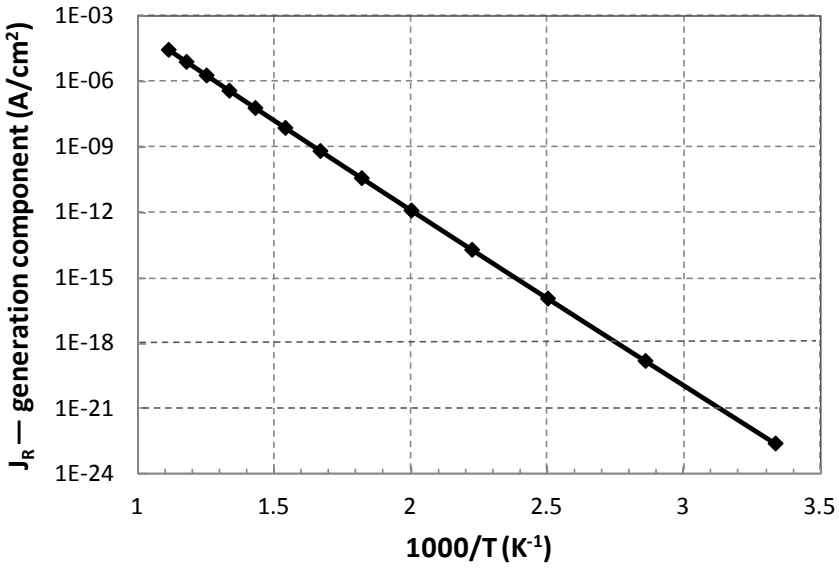


Figure 5-18 Calculated generation component of the reverse current of the device in Fig. 5-17 as function of temperature.

5.2.2.3 Discussion

Parasitic p-n diodes with two different junction-areas, 1×10^{-4}cm^2 and 2.5×10^{-3}cm^2, were characterized from three randomly picked dies (i.e., total 6 devices) as a function of temperature. Two of the small-junction-area devices exhibited an I-V characteristic close to a well-behaved diode, having a sharp turn-on. Conversely, the leaky devices conducted considerable current at lower voltages and had high ideality factors (>2).

The device behavior depended primarily on the active region associated with epi-layer. The quality of epi-layer is clearly important to the device performance. It has been proved that the common crystal defects of epi-layers (e.g., micropipes and dislocations) limit device performance, particularly leakage current [57-60]. The large-junction-area devices exhibit higher leakage current due to the fact that they are more likely to include more crystal defects. With wafer and epi-layer quality improvement, more consistent behavior of p-n junction, as well as improved leakage current, would be expected.

5.2.3 Parasitic BJT devices

5.2.3.1 Theory

A BJT is usually operated under active mode, which means the B-E junction is forward-biased, and B-C junction is reverse-biased. In a p-n-p BJT, the largest current component is due to the holes injected from emitter. Current is induced by minority carrier concentration gradient, so it is dominated by diffusion current. From junction theory, the excess minority carrier (hole) charge just outside the emitter junction depletion region is given by:

$$p_n(0) = p_{no}\exp\left(\frac{eV_{EB}}{kT}\right) \tag{5.19}$$

At the collector end, x = W_B, $p_n(W_B) \approx 0$. The total emitter current is the sum of the hole current injected from emitter to collector and the electron current injected from base to emitter terminals.

$$I_E = I_{Ep} + I_{En}, \tag{5.20}$$

where

$$I_{Ep} = \frac{qAD_p n_i^2}{N_B W}\left(e^{qV_{EB}/KT} - 1\right) + \frac{qAD_p n_i^2}{N_B W} \tag{5.21}$$

and

$$I_{En} = \frac{qAD_E n_{E0}}{L_E}\left(e^{qV_{EB}/KT} - 1\right) \tag{5.22}$$

Collector current is defined as the hole current injected into collector from emitter across the base, given by

$$I_{Cp} = \frac{qAD_p n_i^2}{N_B W}\left(e^{qV_{EB}/KT} - 1\right) + \frac{qAD_p n_i^2}{N_B W} \tag{5.23}$$

Since only the holes injected into the base terminal contribute to collector current, emitter injection efficiency is often used to evaluate the performance of a BJT and is given by

$$\gamma = \frac{I_{Ep}}{I_{Ep} + I_{En}} = \frac{{D_p p_{no}}/{W_B}}{{D_p p_{no}}/{W_B} + {D_E n_{Eo}}/{L_E}} = \frac{1}{1 + \frac{D_E n_{Eo} W_B}{D_P P_{no} L_E}}. \quad (5.24)$$

Figure 5-19 illustrates a parasitic vertical p-n-p BJT structures in our JFET device. The p^+ gate, n-type channel, and p-type substrate correspond to the emitter, base and collector of the BJT structure, respectively.

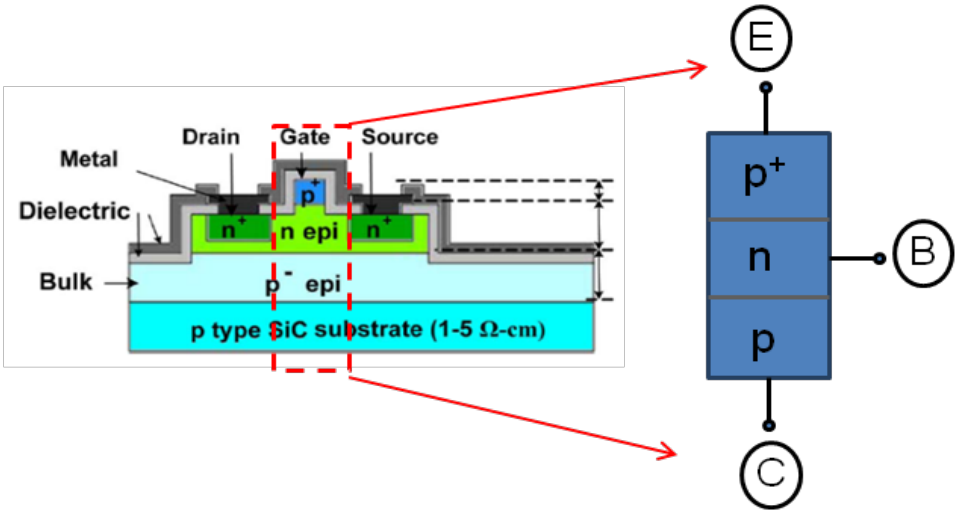


Figure 5-19 A vertical p-n-p BJT structure in our JFET device.

Ideally, in a p-n-p BJT, the largest current component is due to the holes injected from the emitter. With a well-designed transistor, the emitter injection efficiency should be high, which means most holes will be injected into the collector and increase the collector current. The current gain, β, of a p-n-p BJT is given by [10]

$$\beta = \frac{i_C}{i_B} = \frac{D_p}{D_E} \times \frac{N_E}{N_B} \frac{L_E}{W_B} \quad (5.25)$$

where D_p is the diffusion constant of minority carriers, D_E is the diffusion constants in the emitter, and L_E is the diffusion length in the emitter. N_E and N_B are the impurity

doping in the emitter and base, respectively. W_B is the width of the base, corresponding to the thickness of our n-epi layer here.

When $W_E << L_E$ (short quasi-neutral region), L_E is substituted with W_E. For the parasitic BJT device in this work, we can calculate the current gain as

$$\beta = \frac{\mu_{PB} N_{dE} W_E}{\mu_{nE} N_{aB} W_B} = \frac{75 * 2 \times 10^{19} * 0.2}{400 * 1 \times 10^{17} * 0.3} = 25$$

As long as $N_E \gg N_B$, $L_E \gg W_B$, a high β can be achieved.

5.2.3.2 I-V characterization results and discussion

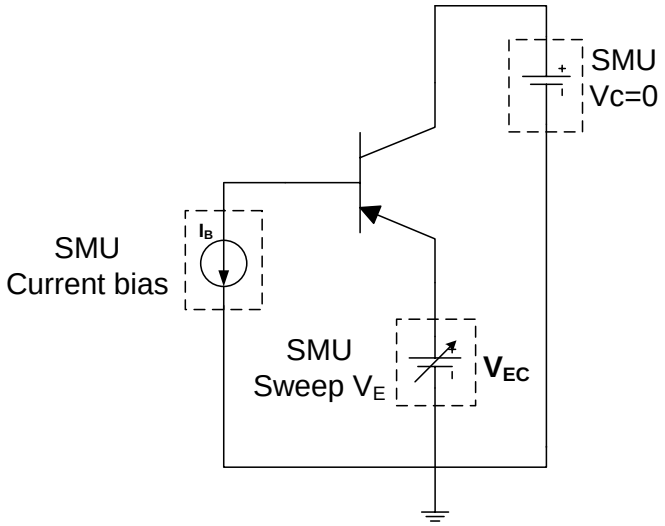
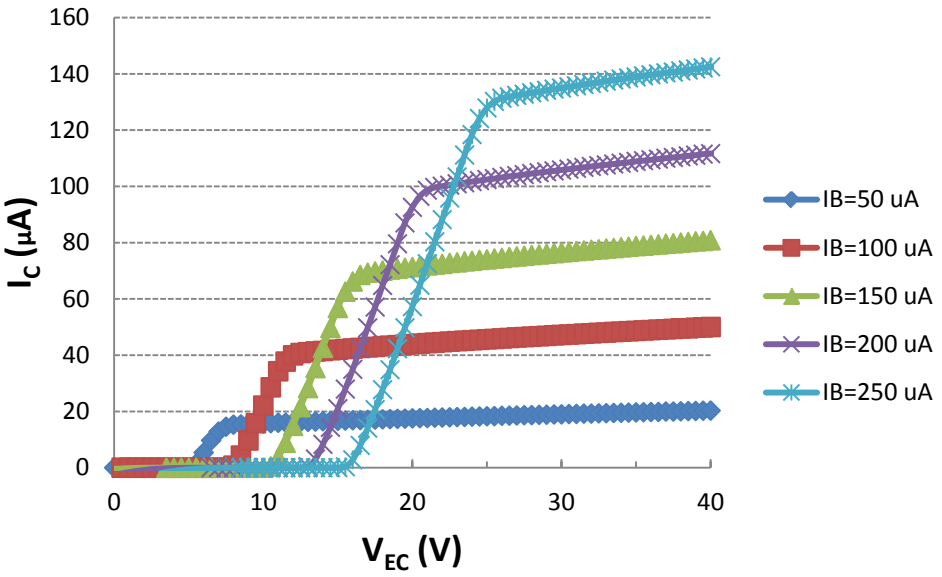
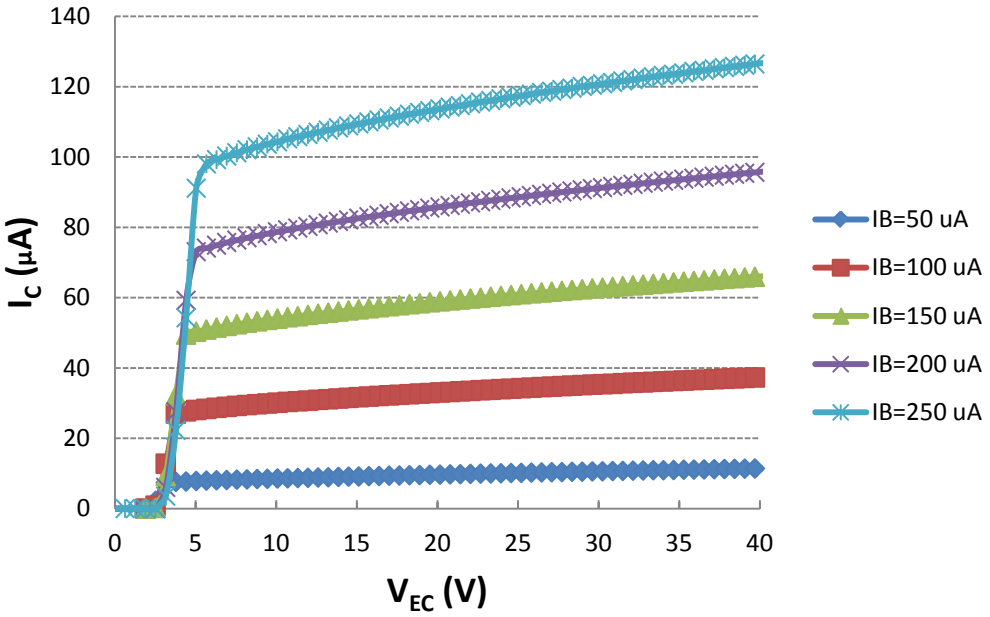


Figure 5-20 The test setup for I-V measurements in the BJT mode.

Device (CR0975-12-R5C5) was characterized on a probe station using the test setup illustrated in Figure 5-20. The base current was stepped from 50 μA to 250 μA, and the emitter voltage was swept from 0V to 40V. The DC I-V characteristics of two different sizes of BJT structures are shown in Figure 5-21. All the devices exhibited extremely low current gain (<1), as shown in Table 5-3.



(a)



(b)

Figure 5-21 DC I-V characteristics of BJT mode from (a) a 100μm/100μm and (b) a 500μm/500μm device.

Table 5-3 Measured current gain for different device sizes at I_B=205 μA and V_{EC}=40V.

Device Size (μm/μm)	10/100	100/100	10/100	100/5	500/500
beta	0.62	0.57	0.62	0.59	0.50

One of the most important limiting factors of BJT current gain is surface-recombination on the device surface. One aspect of this effect relates to the device geometry:

(1) **Spacing between emitter and base:** It has been proved that the spacing between the heavily implanted base contact region and the edge of the emitter is critical for achieving high current gain [61-63]. Current gain is improved with increasing emitter-base spacing.

(2) **Emitter width and thickness:** There are several studies that show the current gain to be highly dependent on the emitter periphery-to-area ratio, which is often referred to as *emitter size effect*. It is reported that the current gain can be improved by widening the emitter width [63-64] to minimize the carrier recombination between the emitter and base. The effect of emitter thickness and current gain has also been investigated. It is suggested that the thickness of emitter should be larger than a minority carrier diffusion length and usually at least ~1μm [65].

Another aspect relates to the device geometry:

(3) **Surface passivation:** It has been demonstrated that the current gain can be improved by applying surface passivation process to suppress the surface recombination [66-67].

(4) **Epitaxial growth:** Growing the emitter and base epitaxial layers without interruption is believed to be an important factor for achieving high current gain. It is thought that doing so may decrease the defects in the emitter-base interface and decrease the resulting recombination. A five times current gain improvement with continuous epitaxial growth was reported in [68].

For the parasitic BJT devices, neither geometry nor process related factors was taken into consideration in our design, since the focus was on JFETs. The emitter thickness (0.2 μm) is relatively thin compared to the 1 μm thickness guidance in the literature. The emitter-base gap is not optimized to minimize carrier recombination between the emitter and base. Moreover, the poor carrier lifetime in p-type SiC may be a critical factor in limiting the current gain.

6 4H-SiC JFET-based Integrated Circuit Design

With rapid progress in SiC technology in the past decade, 4H-SiC has become the preferred substrate material. 4H-SiC exhibits better electrical properties compared to 6H-SiC, including larger bandgap, lower intrinsic carrier concentration, and higher electron/hole mobility (see Table 6-1). A conversion of select integrated circuits from 6H-SiC technology to 4H-SiC is presented in this chapter.

Table 6-1 Comparisons of selected electrical properties between 4H- and 6H- SiC at 300K [69].

	4H-SiC	6H-SiC
Bandgap Energy (eV)	3.2	3
Thermal conductivity (W/cm-K)	3-5	3-5
Intrinsic carrier concentration (cm-3)	~10^{-7}	~10^{-5}
Electron mobility ($cm^2V^{-1}s^{-1}$)*	~800	~400
Hole mobility ($cm^2V^{-1}s^{-1}$)*	~115	~90

*at $N_D = 10^{16}\ cm^{-3}$

6.1 Temperature Effect of 4H-SiC Properties

The band-gap energy of 4H-SiC as a function of temperature is given by [70]

$$E_g(T) = 3.266 - 6.5 \times 10^{-4}\,(T + 1300K)\text{eV}. \tag{2.1}$$

Figure 6-1 shows the relationship between calculated bandgap energy and temperature.

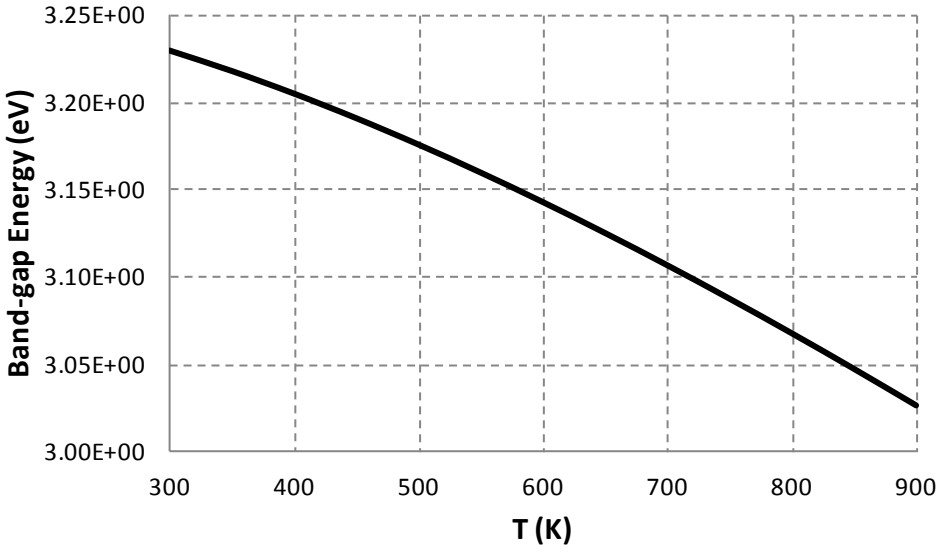


Figure 6-1 Temperature dependence of calculated 4H-SiC bandgap energy.

The intrinsic carrier concentration in 4H-SiC is determined by the same equation as 6H-SiC [10]:

$$n_i(T) = 2\left(\frac{kT}{2\pi\hbar^2}\right)^{3/2}(m_c m_v)^{3/4} e^{\frac{-E_g(T)}{2kT}}, \tag{2.2}$$

where $k = 8.62 \times 10^{-5}\ eV/K$ is the Boltzmann constant, $\hbar = 4.135 \times 10^{-15}$ eV is the reduced Plank's constant, m_C and m_V are the effective density-of-state masses for the conduction and valence band, respectively.

Considering variations of ±25% in the doping concentration and ±20% in thickness of 4H-SiC epitaxial layers [7], the channel epi-layer parameters were re-designed to accommodate these variations; the resulting electrical parameters are listed in Table 6-2.

Table 6-2 Design parameters of channel epi-layer and its important electrical properties in 4H- and 6H- SiC technology.

	4H-SiC	6H-SiC
N_D (cm^{-3})	1.2×10^{17}	1×10^{17}
N_A (cm^{-3})	2×10^{19}	2×10^{19}
D (μm)	0.25	0.3
V_T (V)	-3.9	-5.2
k′ ($\mu A/V^2$)	~7.9	~1.5
μ_n ($cm^2v^{-1}s^{-2}$)	582	325
Rsh (kΩ/□)	4.53	19.6

Figure 6-2 illustrates the mobile carrier concentration versus temperature for a dopant density of 1.2×10^{17} cm^{-3}. At room temperature, dopant activation (79%) of 4H-SiC is nearly *twice* that of 6H-SiC (39%).

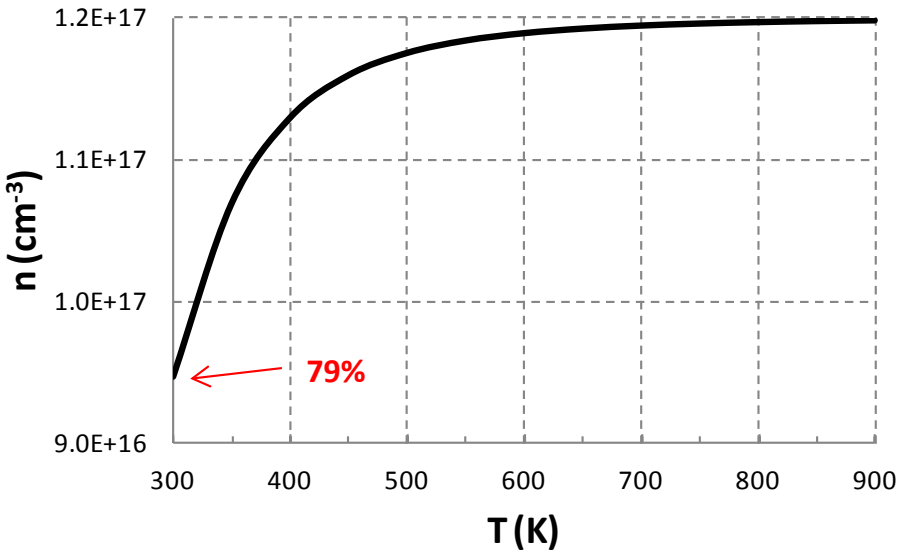


Figure 6-2 Temperature dependence of calculated mobile carrier concentration in 4H-SiC.

The low-field electron mobility (μ_n) is modeled by the Caughey-Thomas equation [71] as

$$\mu_n = \mu_n^{min} + \frac{\mu_{max} - \mu_{min}}{1 + \left(\frac{N}{N_{ref}}\right)^{\alpha}}, \tag{2.3}$$

Where the temperature dependent parameters are given:

$$\mu_{max} = 950 \times \left(\frac{T}{300K}\right)^{-2.4}$$

$$\mu_{min} = 40 \times \left(\frac{T}{300K}\right)^{-0.5}$$

$$N_{ref} = 2 \times 10^{17} \times \left(\frac{T}{300K}\right)$$

$$\alpha = 0.76$$

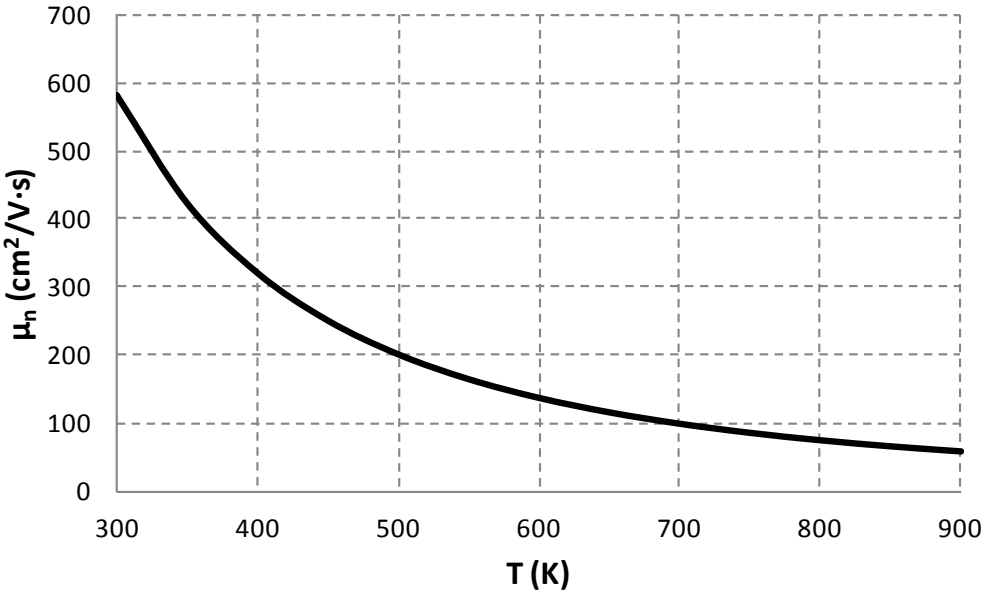


Figure 6-3 Temperature dependence of calculated electron mobility in 6H-SiC

Sheet resistance is also given by equation (2.4). Figure 6-4 shows the relationship between sheet resistance and temperatures with D = 0.25μm.

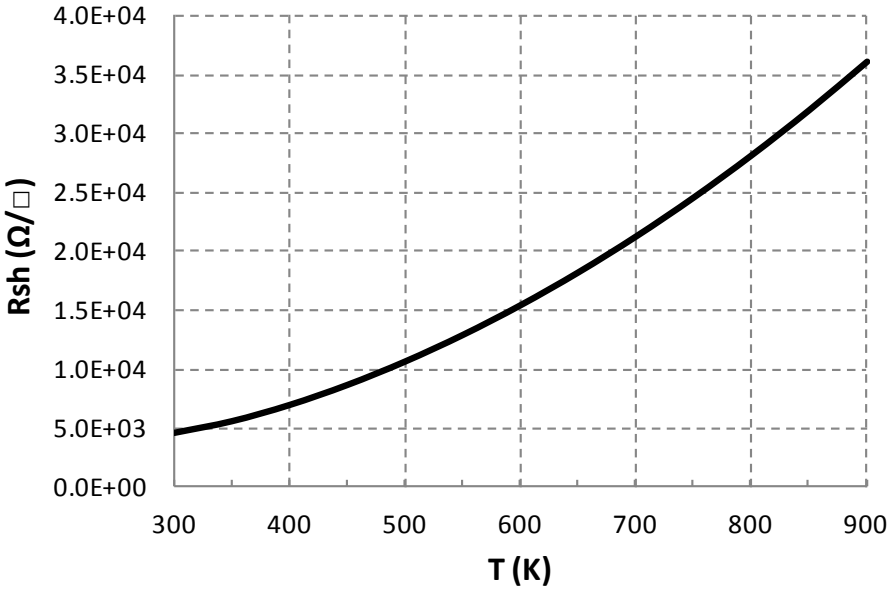


Figure 6-4 Temperature dependence of calculated sheet resistance in 4H-SiC.

With the given design parameters and material properties of 4H-SiC channel epi-layer, the transconductance parameter, k', of 4H-SiC JFET is five times higher than that in 6H-SiC technology. Higher k' leads to higher transconductance, and thus higher voltage gain and transition frequency.

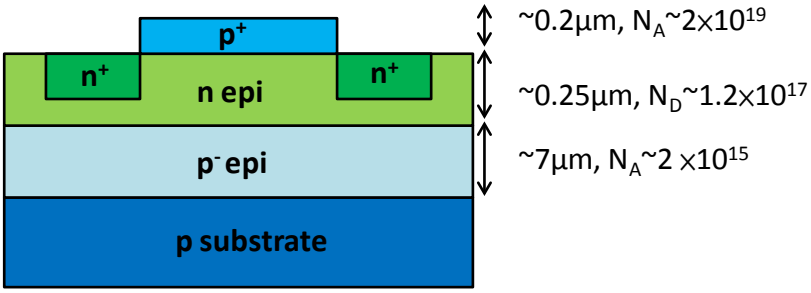


Figure 6-5 Schematic cross-section of the JFET structure in 4H-SiC technology.

6.2 Integrated Circuit Design

In order to convert the circuits from 6H-SiC to 4H-SiC technology, a new model of 4H-SiC JFET has been developed at three different operating temperatures. The circuits are then simulated with Pspice. The following design rules are applied for the technology conversion:

(1) The circuit topology is not changed. Main building blocks, such as differential pairs, cascade stage, current source, and source follower are used in the new technology design with a few modifications for some circuits.

(2) The devices sizes are unchanged.

(3) The main biasing current is unchanged, where possible. Bias current is given by

$$I_{DS} = \left(\frac{W}{L}\right) k'(V_{GS} - V_T)^2,$$

Given $k'_{4H} = 5 \times k'_{6H}$, in order to keep the bias current the same, $(V_{GS} - V_T)_{4H}{}^2 = \frac{1}{5}(V_{GS} - V_T)_{6H}{}^2$. Then, the resistors in current source are chosen to achieve the desired $(V_{GS} - V_T)_{4H}$.

6.2.1 Logic circuits

6.2.1.1 Logic gates

Figure 6-6 shows the modified logic gates schematics for 4H-SiC technology. The size of the unity device, 1x JFET, is W/L=160µm/10µm. The current from current source device, J2, remains 200 µA/100 µA. The inverter is simulated at three different temperatures and VTC plot is shown in Figure 6-7. As in 6H-SiC technology, the circuit exhibits a steep slope, and the transition is well centered in the range of logic swing. Total power supply requirement, ±12 V, decreases to 4V compared with ±14 V of the 6H-SiC inverter.

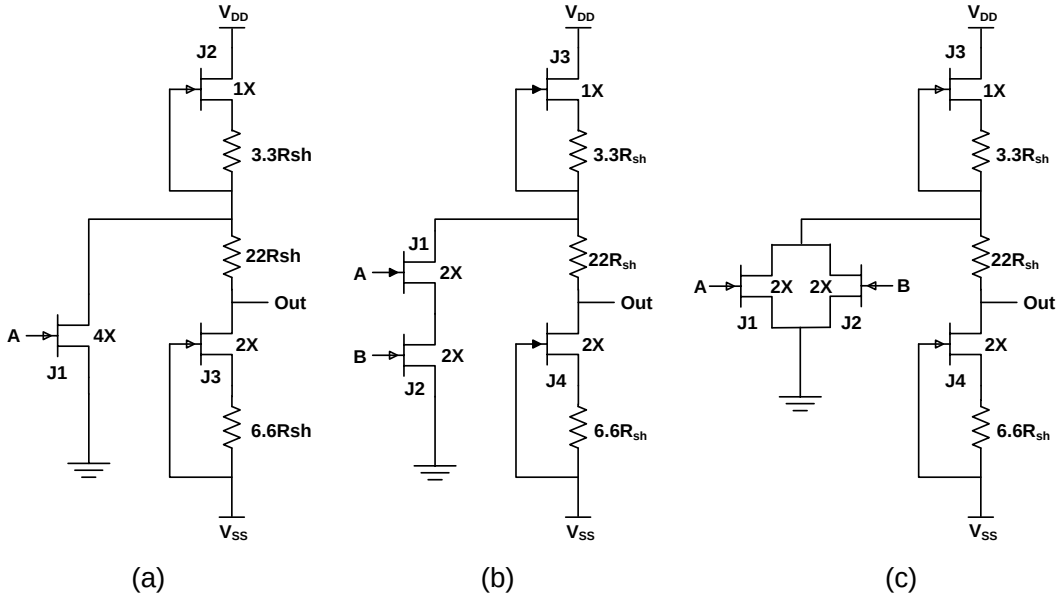


Figure 6-6 Schematic of the 4H-SiC JFET-based (a) inverter, (b) NAND, and (c) NOR gate.

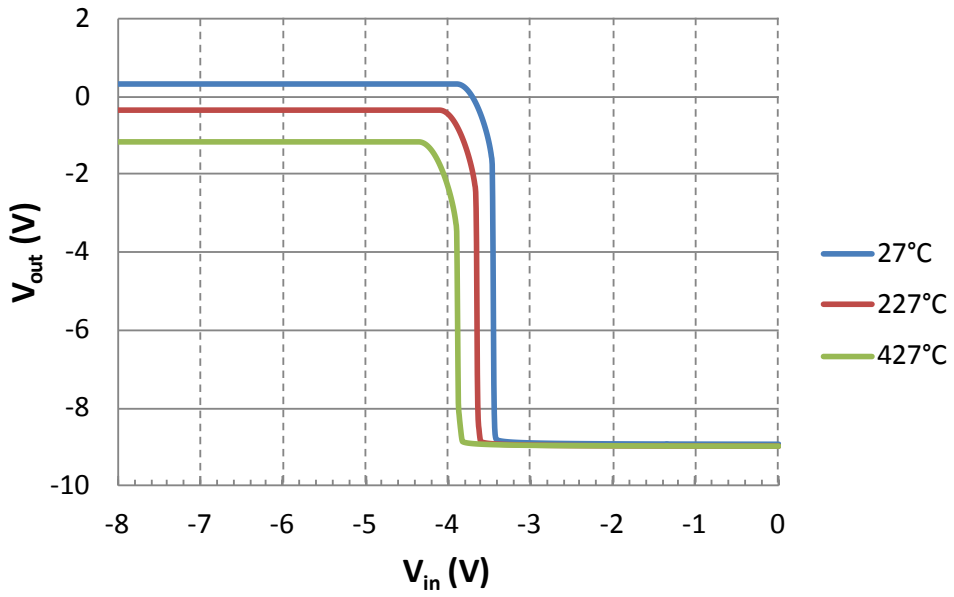


Figure 6-7 Simulated VTC of the 4H-SiC inverter at three different operating temperatures.

6.2.1.2 SR Latch

SR latch, the fundamental building block for sequential logic, is designed using NAND and NOR gates. Two types of latches, $\overline{SR}$ NAND latch and SR NOR latch are constructed from a pair of cross-coupled NAND and NOR gates, respectively. Simulated transient characteristics at room temperature are illustrated in Figure 6-9.

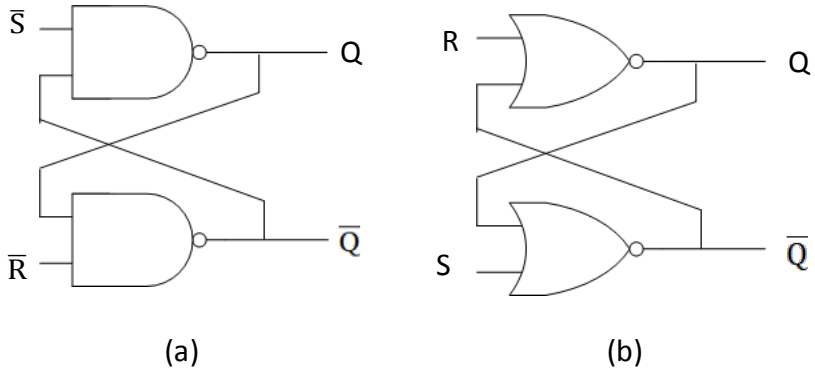


Figure 6-8 Schematic of (a) NAND and (b) NOR latches.

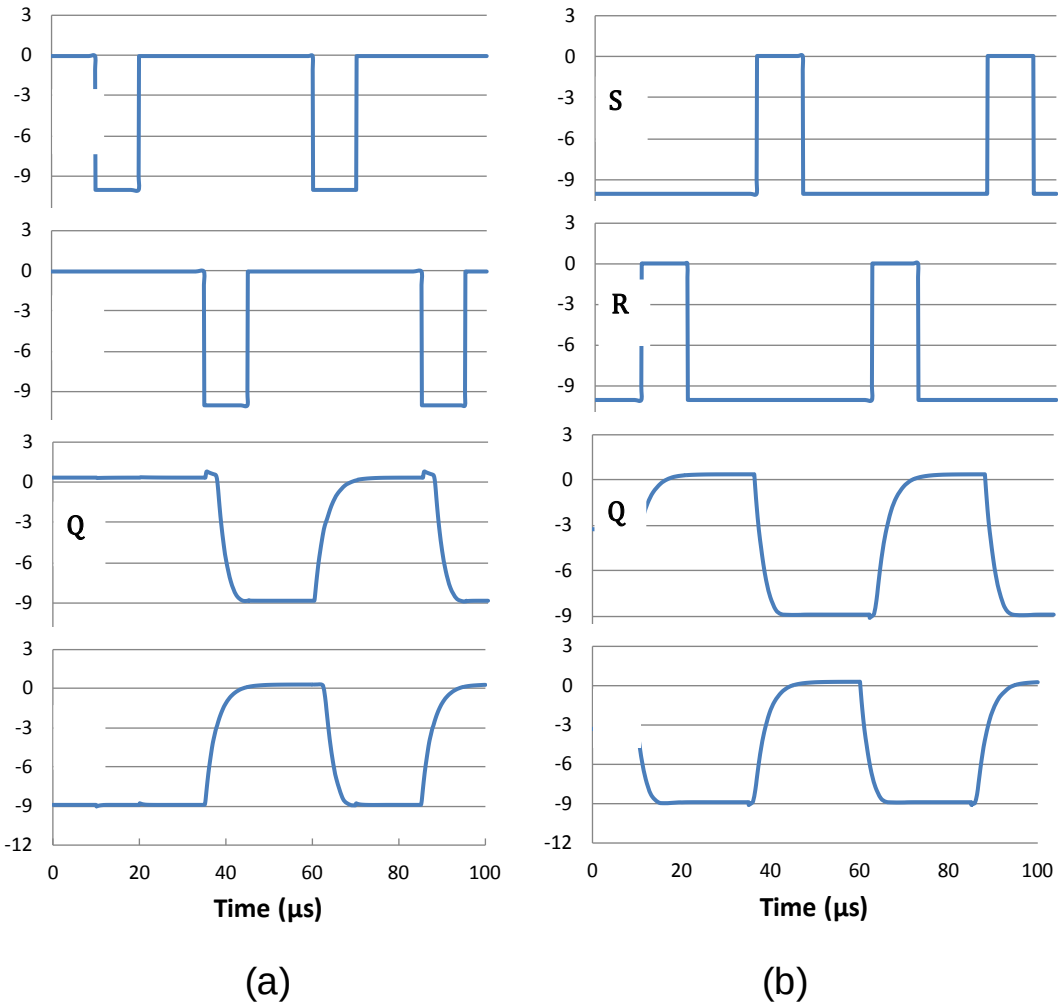


Figure 6-9 Simulated transient characteristics from 4H-SiC (a) NAND and (b) NOR latches at room temperature.

6.2.2 Analog circuits

In the new design, a consistent and optimized power supply, V_{DD} = 30 V and V_{SS} = -6V, is chosen to enable design of a two-stage amplifier from a single single-stage amplifier. As the result, the circuit topology is modified to accommodate the revised power supply specs.

6.2.2.1 Single-stage differential amplifier with resistive load

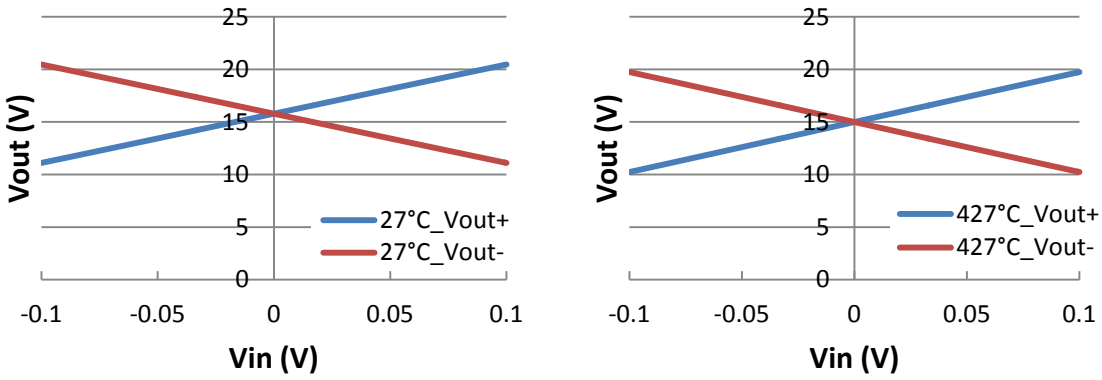
The schematic of 4H-SiC single-stage differential amplifier with resistive load is as shown previously in Figure 2-15 (a). The summary of device sizes and designed biasing voltage for 4H-SiC technology are listed in Table 6-3. Load resistor and degeneration resistor values are listed in Table 6-4. At room temperature and 427 °C, symmetric and linear DC response for both V_{out+} and V_{out-} are shown in simulation results of Figure 6-10. Again, the amplifier gain is $\approx g_{m1,2}R_{L1,2}$ as in previous design; therefore, temperature dependence of amplifier gain has been canceled out. Simulated gain change across temperature range is less than 2% which agrees with design. Figure 6-11 provides the frequency response across temperature ranges of the differential amplifier. The unity-gain frequency is 2 MHz at 427 °C. The simulated gain and supply current for each temperature are listed in Table 6-5. Compared to the original circuit design in 6H-SiC, a 10V reduction has been achieved in power supply and supply current reduces almost 50% from 1.2mA to ~600µA.

Table 6-3 JFET sizes and biasing voltage for single-stage amplifier with resistive load.

	Device	W/L (µm/ µm)	(V_{GS}-V_T)
Driver devices	J1,J2	320/10	0.62
Current source	J3	640/20	0.89
	J6, J7	320/10	0.89
Source follower	J4,J5	320/10	0.89

Table 6-4 Resistor values for the single-stage amplifier with resistive load.

Device	Value (□)
R_{L1},R_{L2}	38
RCS1, RCS2, RCS3	6.6



(a) (b)

Figure 6-10 Simulated DC response of the single-stage differential amplifier with resistive load at (a) room temperature and (b) 427 ºC, with V_{DD} = 30V, V_{SS} = -6V

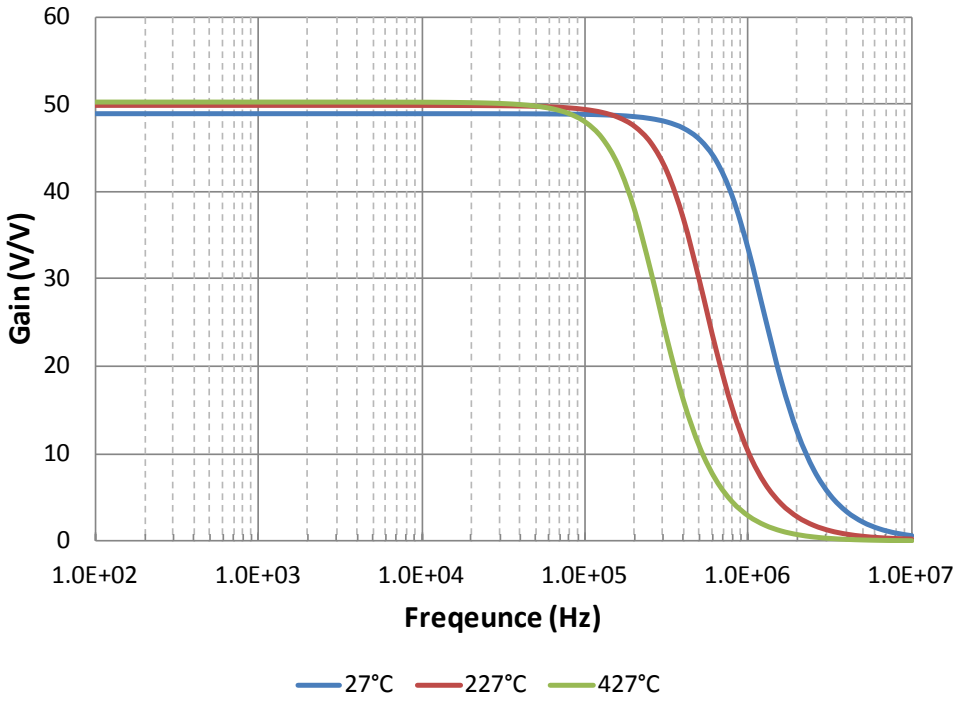


Figure 6-11 Simulated AC response of the single-stage differential amplifier with resistive load at three operating temperatures, with V_{DD} =30 V, V_{SS} = -6 V.

Table 6-5 Simulated gain and supply current at three different operating temperatures.

Temp (°C)	Gain (V/V)	I_{DD} (µA)
27	49.01	607.78
227	49.81	275.42
427	50.34	146.89

6.2.2.2 Transimpedance amplifier

The circuit schematic of the transimpedance amplifier in 4H-SiC technology is shown in Figure 6-12. The circuit topology has been modified compared with the original design; a driver device, J6, a current source circuit, J7, and degeneration resistor RCS3 are added to accommodate the power supply change, as well as to maintain the open loop gain (see Figure 4-7 for the circuit schematic in 6H-SiC technology). Therefore, an increasing supply current is expected. Table 6-3 and Table 6-4 list designed device sizes and resistor values, respectively. Simulated amplifier frequency response at elevated temperatures is presented in Figure 6-13. Transimpedance amplifier gain, R_f, increases with temperature as would be expected.

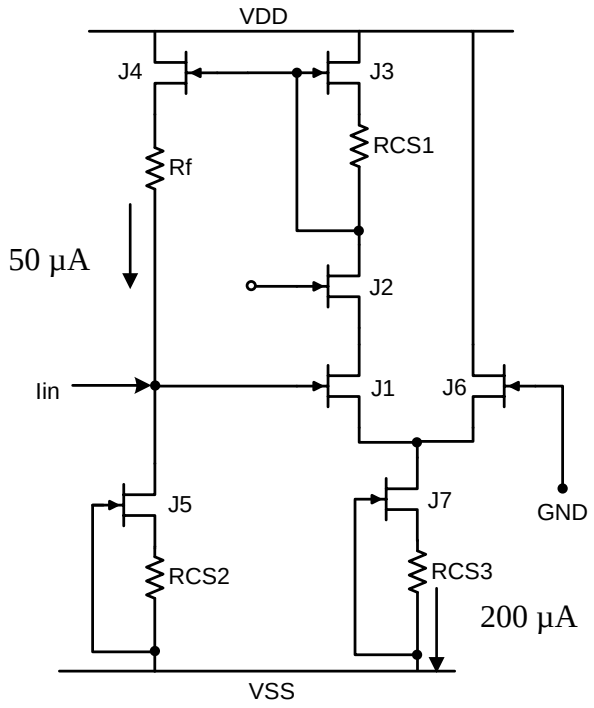


Figure 6-12 Schematic of the 4H-SiC single-ended, single-stage transimpedance amplifier.

Table 6-6 JFET sizes and biasing voltages for the single-ended, single-stage transimpedance amplifier.

	Device	W/L (μm/ μm)	(V_{GS}-V_T)
Driver devices	J1,J2,J6	160/10	0.89
Current source	J3	160/10	0.89
	J5	80/10	0.89
	J7	320/10	0.89
Source follower	J4	320/10	0.44

Table 6-7 Resistor values for the single-ended, single-stage transimpedance amplifier.

Device	Value (□)
RCS1	6.6
RCS2	13.2
RCS3	3.3
R_f	68

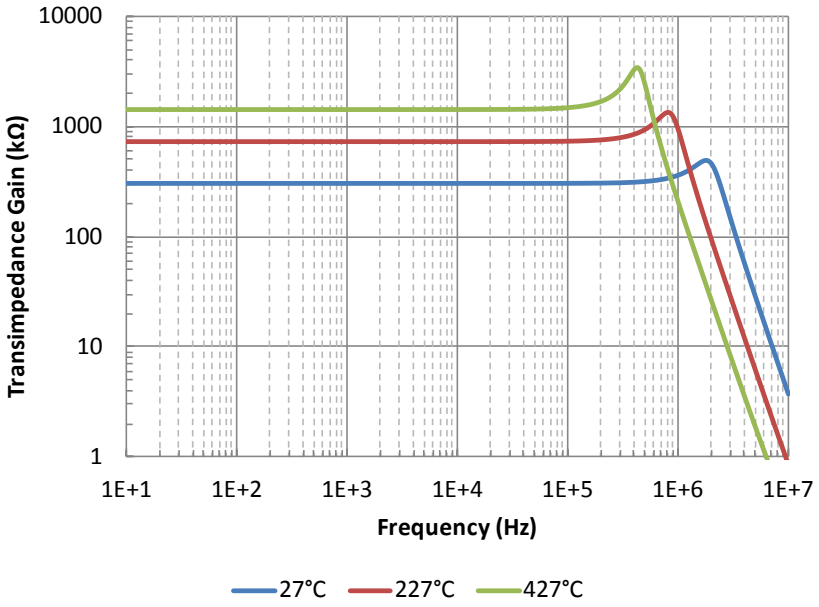


Figure 6-13 Simulated AC response of the single-ended, single-stage transimpedance amplifier with resistive load at three operating temperatures, with V_{DD} = 30 V, V_{SS} = -6 V.

Table 6-8 Simulated gain and supply current at three different operating temperatures.

Temp (°C)	Gain (kΩ)	I_{DD} (µA)
27	307.64	251.04
227	719.55	114.55
427	1437.99	60.95

6.3 Summary

In this chapter, a technology conversion from 6H- to 4H-SiC has been demonstrated with selected integrated circuits as design examples. Device model has been converted into 4H-SiC based on its material electrical properties. Having higher electron mobility and mobile carrier concentration over 6H-SiC, 4H-SiC results in a ~5x improvement in transconductance parameter (k') for the chosen designed parameters.

Most of the circuits have been simulated following the same circuit approach in 6H-SiC ones. Degenerated resistors in current source are designed based on the desired overdrive voltage and bias current. Circuits are simulated at three different operating temperatures up to 427 °C. For the digital circuits, basic logic gates and SR latches have been designed and simulated. A 20% power supply reduction is achieved in the single-stage differential amplifier with resistor load compare to the amplifier in 6H-SiC while maintaining the same amplifier gain. Circuit topology of the single-stage, single-ended transimpedance amplifier has been modified to accommodate the universal power supply for all analog circuits.

7 Conclusion and Future Work

7.1 Conclusion

This thesis provides an extended study on the electrical characteristics of 6H-SiC JFET-based devices and ICs for high temperature sensing applications. The devices and circuits were designed and fabricated at CWRU by previous members of Mehregany Lab and Garverick Lab.

Electrical characteristics of depletion mode n-channel JFETs were measured across a 2 inch-diameter 6H-SiC wafer at elevated temperatures up to 280 °C. Of the 229 tested devices, 215 were properly operational, resulting in a yield of ~93%. The on-state parameters showed relatively close values of coefficient of variance across the tested temperature range. Non-uniformity of the channel epitaxial layer thickness was identified as the main reason for $|V_{TH}|$ and I_{DSS} variations across the wafer. Large variations in I_{GSS} and I_{OFF} were observed, which may be attributed to the crystallographic imperfections in the 6H-SiC epitaxial layers [72]. Across the wafer, the minimum on/off current ratio was 539 at 25 °C and 182 at 280 °C.

Integrated logic circuits using 6H-SiC JFETs were demonstrated and characterized at operating temperatures ranging from room temperature to 550 °C [73-74]. The core inverter has outstanding DC characteristics with a gain of -26 at 25 °C and > -20 up to 500 °C. Dynamic characteristics of NAND and NOR logic circuits were tested and behaved well at operating temperatures up to 550 °C. These logic building blocks provide a pathway for high-temperature computation. The measurement results indicate that logic circuits of moderate complexity are indeed feasible for this temperature range, enabling simple controllers that are embedded with engines, generators, and so on.

A single-stage, single-ended transimpedance amplifier for high-temperature capacitive sensing applications was characterized up to 450 °C [75]. At room temperature, a high gain-bandwidth of 235 kΩ by 0.61 MHz and a power consumption of 4.5 mW were measured. At elevated temperatures, the gain increased as would be expected (774 kΩ at 450°C) and the bandwidth remained > 0.17 MHz. The input-referred noise density at room temperature and 450°C were $0.8\ \mathrm{pA}/\sqrt{\mathrm{Hz}}$ and $1.2\ \mathrm{pA}/\sqrt{\mathrm{Hz}}$, respectively. A capacitive sensing system composed of the transimpedance amplifier with trimmer capacitors (simulating sensing capacitances) was also demonstrated at temperatures up to 450 °C. The gain varied with frequency and temperature as would be expected, providing evidence that sub-pF values of capacitance are indeed being accurately measured.

IC noise performance was analyzed up to 500 °C. $1/f^{\gamma}$ noise (where $1< \gamma <2$) was found in our randomly selected circuit samples, including: differential pair; single-stage, differential amplifier with resistive load; and two-stage, differential amplifier with current source load in the 1st stage and resistive load in the 2nd stage. Overall, there was not a universal behavior in the amplifier noise; $1/f^{\gamma}$ (where $\gamma>1$) was below tens of Hz. Noise sources (e.g., bulk noise and generation-recombination noise) depend on fabrication process and temperature, and also suggest the existence of crystal imperfection.

I-V characteristics of parasitic p-n diodes were studied across operating temperatures up 600 °C. Same as in practical I-V behavior of Si diode, a non-ideal behavior was found, with large ideality factor. This behavior may be attributed to tunneling current. Large-junction-area devices tend to exhibit larger leakage current, which is consistent with the assumption that larger areas are more likely to contain (more) crystal defects. The small-

junction-area devices with well-behaved I-V characteristic showed a $\eta = 2$ and a calculated thermal activation energy of 1.21 eV. Parasitic vertical BJT devices were also characterized; large unwanted recombination processes stemming from the non-optimized geometry design of the devices may be the cause of their extremely low current gain.

Finally, the feasibility of converting from 6H-SiC to 4H-SiC technology was demonstrated. In addition to basic logic gates, SR latches were designed and simulated at three different operating temperatures, reaching 427 °C. Due to the superior electrical characteristics of 4H-SiC, a 20% decrease in power supply voltage was obtained for the 4H-SiC single-stage, differential amplifier with resistive load. Circuit topology of the 4H-SiC JFET-based single-stage, single-ended transimpedance amplifier was modified to for this power supply level.

7.2 Future Work

In order to investigate the noise sources in the ICs, a noise analysis of a single JFET device should be conducted across a range of bias conditions and temperatures. Once the fundamental noise sources are understood, the noise behavior of the more complex ICs may be estimated more accurately. Transmission electron microscopy (TEM) may be used to study the type of crystal defects found in the samples to associate the leakage current and noise mechanism with the defects.

A fully differential transimpedance amplifier present on the wafer has not yet been characterized. Long-term reliability studies of our ICs and their packaging remain to be studied across the operating temperature range of interest.

.

Bibliography

[1] D. Brown, D. McGrath, M. Nielsen, N. Krishnamurthy, J. W. Kretchmer, and M. Ghezzo, "Progress Towards a Manufacturable SiC Mixed Analog-Digital Integrated Circuit Technology," *Materials Science Forum,* vol. 338-342, pp. 1291-1294, 2000.

[2] P. G. Neudeck, R. S. Okojie, and C. Liang-Yu, "High-temperature electronics - a role for wide bandgap semiconductors?," *Proceedings of the IEEE,* vol. 90, pp. 1065-1076, 2002.

[3] J. A. Cooper, Jr., M. R. Melloch, R. Singh, A. Agarwal, and J. W. Palmour, "Status and prospects for SiC power MOSFETs," *Electron Devices, IEEE Transactions on,* vol. 49, pp. 658-664, 2002.

[4] P. G. Neudeck, D. J. Spry, L.-Y. Chen, G. M. Beheim, R. S. Okojie, C. W. Chang, R. D. Meredith, T. L. Ferrier, L. J. Evans, M. J. Krasowski, and N. F. Prokop, "Stable Electrical Operation of 6H-SiC JFETs and ICs for Thousands of Hours at 500 ^{o}C," *Electron Device Letters, IEEE,* vol. 29, pp. 456-459, 2008.

[5] A. C. Patil, F. Xiao-an, M. Mehregany, and S. L. Garverick, "Fully-monolithic, 600 ^{o}C differential amplifiers in 6H-SiC JFET IC technology," in *Custom Integrated Circuits Conference, 2009. CICC '09. IEEE*, 2009, pp. 73-76.

[6] A. P. Pisano, et al., , "SiC TAPS (Temperature, Acceleration, Pressure, and Strain) Sensors for Extreme Harsh Environments," *Proposal to DARPA,* Sept. 2004.

[7] Cree, Inc., http://www.cree.com [Online].

[8] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits," *Proceedings of the IEEE,* vol. 91, pp. 305-327, 2003.

[9] F. B. McLean, C. W. Tipton, J. M. McGarrity, and C. J. Scozzie, "Modeling the electrical characteristics of n-channel 6H-SiC junction-field-effect transistors as a function of temperature," *Journal of Applied Physics,* vol. 79, pp. 545-552, 1996.

[10] S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. New York: Wiley, 1981.

[11] S. Zappe, E. Obermeier, S. T. Sheppard, U. Schmid, V. Lauer, and W. Wondrak, "Advanced SPICE-modelling of 6H-SiC JFETs including substrate effects," *Proc. HITEC,* pp. 261-264, 1998.

[12] N. S. Rebello, F. S. Shoucair, and J. W. Palmour, "6H silicon carbide MOSFET modelling for high temperature analogue integrated circuits (25-500^{o}C)," *Circuits, Devices and Systems, IEE Proceedings* vol. 143, pp. 115-122, 1996.

[13] A. S. Kashyap, C. Cheng-Po, and V. Tilak, "Compact modeling of silicon carbide lateral MOSFETs for extreme environment integrated circuits," in *Semiconductor Device Research Symposium (ISDRS), 2011 International*, 2011, pp. 1-2.

[14] S. T. Sheppard, V. Lauer, W. Wondrak, and E. Niemann, "High Temperature Performance of Implanted-Gate n-Channel JFETs in 6H-SiC," *Materials Science Forum,* vol. 264-268, pp. 1077-1080, 1998.

[15] D. Spry, P. Neudeck, R. Okojie, L. Y. Chen, G. Beheim, R. Meredith, W. Mueller, and T. Ferrie, "Electrical Operation of 6H-SiC MESFET at 500 C for 500 Hours in Air Ambient," *IMAPS* International *High Temperature Electronics Conference,* 2004.

[16] P. G. Neudeck, G. M. Beheim, and C. S. Salupo, "600 C Logic Gates Using Silicon Carbide JFET'S," *Government Microcircuit Applications Conference Tech. Digest,* pp. 421-424, 2000.

[17] J.-Y. Lee, S. Singh, and J. A. Cooper, "Demonstration and Characterization of Bipolar Monolithic Integrated Circuits in 4H-SiC," *Electron Devices, IEEE Transactions on,* vol. 55, pp. 1946-1953, 2008.

[18] U. Schmid, S. T. Sheppard, and W. Wondrak, "High temperature performance of NMOS integrated inverters and ring oscillators in 6H-SiC," *Electron Devices, IEEE Transactions on,* vol. 47, pp. 687-691, 2000.

[19] S.-H. Ryu, K. T. Kornegay, J. A. Cooper, Jr., and M. R. Melloch, "Digital CMOS IC's in 6H-SiC operating on a 5-V power supply," *Electron Devices, IEEE Transactions on,* vol. 45, pp. 45-53, 1998.

[20] L. Lanni, R. Ghandi, B. G. Malm, C. Zetterling, and M. Ostling, "Design and Characterization of High-Temperature ECL-Based Bipolar Integrated Circuits in 4H-SiC," *Electron Devices, IEEE* Transactions *on,* vol. 59, pp. 1076-1083, 2012.

[21] S. Singh and J. A. Cooper, "Bipolar Integrated Circuits in 4H-SiC," *Electron Devices, IEEE* Transactions *on,* vol. 58, pp. 1084-1090, 2011.

[22] M. Le-Huu, M. Grieb, F. F. Schrey, H. Schmitt, V. Häublein, A. J. Bauer, H. Ryssel, and L. Frey, "4H-SiC N-MOSFET Logic Circuits for High Temperature Operation," *Materials Science Forum,* vol. 679-680, p. 734, 2011.

[23] A. C. Patil, N. Rao, and V. Tilak, "300 oC Capable Digital Integrated Circuits in SiC Technology," in Materials Science Forum, 2012, pp. 1261-1264.

[24] L. Lanni, B. G. Malm, M. Ostling, and C. M. Zetterling, "500 ^{o}C Bipolar Integrated OR/NOR Gate in 4H-SiC," *Electron Device Letters, IEEE,* vol. 34, pp. 1091-1093, 2013.

[25] M. Tomana, R. W. Johnson, R. C. Jaeger, and W. C. Dillard, "A hybrid silicon carbide differential amplifier for 350 ^{o}C operation," *Components, Hybrids, and Manufacturing Technology, IEEE Transactions on,* vol. 16, pp. 536-542, 1993.

[26] D. M. Brown, E. Downey, M. Ghezzo, J. Kretchmer, V. Krishnamurthy, W. Hennessy, and G. Michon, "Silicon Carbide MOSFET Integrated Circuit Technology," *physica status solidi (a),* vol. 162, pp. 459-479, 1997.

[27] S. T. Sheppard, D. B. Slater, J. Lipkin, L. A. , M. K. Das, A. V. Suvorov, and J. W. Palmour, "High-temperature demonstration of a CMOS operational amplifier using 6H silicon carbide N-well technology and ONO dielectrics," in *Proc. 5th Int. High-Temperature Electronics Conf.*, Albuquerque, NM, , 2000, pp. XI.3.1–XI.3.8.

[28] A. Maralani and M. S. Mazzola, "Design of a Silicon Carbide JFET based operational amplifier for gain and CMRR performance," in *Circuits and Systems, 2009. ISCAS 2009. IEEE International Symposium on*, 2009, pp. 1953-1956.

[29] Z. Stum, V. Tilak, P. A. Losee, E. A. Andarawis, and C. P. Chen, "300ºC Silicon Carbide Integrated Circuits," *Materials Science Forum,* vol. 679-680, pp. 730-733, 2011.

[30] A. V. Vert, E. A. Andarawis, and C. P. Chen, "Reliability of Silicon Carbide Integrated Circuits at 300°C," *Materials Science Forum* vol. 717-720, pp. 1265-1268, 2012.

[31] J. Yang, J. Fraley, B. Western, M. Schupbach, and A. B. Lostetter, "A 450°C High Voltage Gain AC Coupled Differential Amplifier," *Materials Science Forum,* vol. 717-720, pp. 1253-1256, 2012.

[32] A. C. Patil, X.-A. Fu, C. Anupongongarch, M. Mhregany, and S. L. Garverick, "6H-SiC JFETs for 450 ^{o}C Differential Sensing Applications," *Journal of Microelectromechanical Systems,* vol. 18, pp. 950-961, 2009.

[33] S. Zappe, M. Leone, F. Yang, and E. Obermeier, "Characterisation of silicon carbide JFETs with respect to microsystems for high temperature applications," *Microsystem Technologies,* vol. 3, pp. 134-138, 1997.

[34] C. Anupongongarch, "Measurements and models of SiC JFET for temperatures up to 450 ^{o}C," MS Thesis, Department of Electrical Engineering and Computer Science, Case Western Reserve University, 2007.

[35] A. C. Patil, "Silicon Carbide JFET Integrated Circuit Technology for High Temperature Sensors," Ph.D., Case Western Reserve University, Cleveland 2009.
[36] J. C. H. Carter, V. F. Tsvetkov, R. C. Glass, D. Henshall, M. Brady, S. G. Müller, O. Kordina, K. Irvine, J. A. Edmond, H. S. Kong, R. Singh, S. T. Allen, and J. W. Palmour, "Progress in SiC: from material growth to commercial device development," *Materials Science and Engineering: B,* vol. 61–62, pp. 1-8, 1999.
[37] C. Mead and L. Conway, *Introduction to VLSI Systems*: Addison-Wesley, 1979
[38] L. Chen and M. Mehregany, "A silicon carbide capacitive pressure sensor for in-cylinder pressure measurement," *Sensors and Actuators A: Physical,* vol. 145–146, pp. 2-8, 2008.
[39] G. Wieczorek, B. Schellin, E. Obermeier, G. Fagnani, and L. Drera, "SiC Based Pressure Sensor for High-Temperature Environments," in *Sensors, 2007 IEEE*, 2007, pp. 748-751.
[40] D. J. Young, D. Jiangang, C. A. Zorman, and W. H. Ko, "High-temperature single-crystal 3C-SiC capacitive pressure sensor," *Sensors Journal, IEEE,* vol. 4, pp. 464-470, 2004.
[41] L. S. Pakula, H. Yang, and P. J. French, "A CMOS compatible SiC accelerometer," in *Sensors, 2003. Proceedings of IEEE*, 2003, pp. 761-764 Vol.2.
[42] S. L. Garverick, S. Chia-Wei, and M. Mehregany, "SiC JFET integrated circuits for sensing and *control* at temperatures up to 600^{o}C," in *Energytech, 2012 IEEE*, 2012, pp. 1-6.
[43] N. Scheinberg, R. J. Bayruns, and T. M. Laverick, "Monolithic GaAs transimpedance *amplifiers* for fiber-optic receivers," *Solid-State Circuits, IEEE Journal of,* vol. 26, pp. 1834-1839, 1991.
[44] A. C. Patil, "Silicon Carbide JFET Integrated Circuit Technology for High-Temperature *Sensors*," Dissertation, EECS, Case Western Reserve University, Cleveland, 2009.
[45] M. E. *Levinshtein*, J. W. Palmour, and S. L. Rumyantsev, "Nature of the 1/f noise in 6H-SiC," *Semiconductor Science and Technology,* vol. 9, 1994.
[46] M. E. *Levinshtein*, S. L. Rumyantsev, M. S. Shur, R. Gaska, and M. A. Khan, "Low frequency and $1 / f$ noise in wide-gap semiconductors: silicon carbide and gallium nitride," *IEE Proceedings - Circuits Devices and Systems,* vol. 149, p. 32, 2002.
[47] H. K. Chen, R. C. Stevens, J. P. Goss, N. G. Wright, and A. B. Horsfall, "Low Frequency Noise in 4H-*iC* Lateral JFET Structures," *Materials Science Forum,* vol. 717-720, pp. 473-476, 2012.
[48] P. Flatresse and T. Ouisse, "Noise analysis of silicon carbide JFETs," *Solid-State Electronics,* vol. 38, pp. 971-975, 1995.
[49] N. V. *Dyakonova*, M. E. Levinshtein, J. W. Palmour, and S. L. Rumyantsev, "Broadening of noise spectra in semiconductors and the $1/f^{1.5}$ problem," *Semiconductor Science and Technology,* vol. 10, 1995.
[50] J. W. Palmour, M. E. Levinshtein, S. L. Rumyantsev, and G. S. Simin, "Low-frequency noise in 4H-*silicon* carbide junction field effect transistors," *Applied Physics Letters,* vol. 68, pp. 2669-2671, 1996.
[51] M. E. Levinshtein, S. L. Rumyantsev, J. W. Palmour, and D. B. Slater, "Low frequency noise in 4H *silicon* carbide," *Journal of Applied Physics,* vol. 8, p. 1758, 1997.
[52] J. B. Casady, W. Dillard, R. W. Johnson, A. K. Agarwal, R. R. Siergiej, and W. E. Wagner, III, "Low frequency noise in 6H-SiC MOSFET's," Electron Device Letters, IEEE, vol. 16, pp. 274-276, 1995.
[53] P. G. Neudeck, D. J. Larkin, J. E. Starr, J. A. Powell, C. S. Salupo, and L. G. Matus, "Electrical *properties* of epitaxial 3C- and 6H-SiC p-n junction diodes produced side-by-side on 6H-SiC substrates," *Electron Devices, IEEE Transactions on,* vol. 41, pp. 826-835, 1994.
[54] R. L. Y. Sah, R. N. Noyce, and W. Shockley, "Carrier Generation and Recombination in P-N Junctions and P-N Junction Characteristics," *Proceedings of the IRE,* vol. 45, pp. 1228-1243, *1957*.

[55] M. E. Dunn, "Electrical Characterization of 4H-Silicon Carbide P-N Junction Diodes," Air force *insititute* of technology, 1995.
[56] J. M. Shah, Y. L. Li, T. Gessmann, and E. F. Schubert, "Experimental analysis and theoretical *model* for anomalously high ideality factors(n>>2) in AlGaN/GaN p-n junction diodes," *Journal of Applied Physics,* vol. 94, pp. 2627-2630, 2003.
[57] M. *Dudley*, X. R. Huang, W. Huang, A. Powell, S. Wang, P. Neudeck, and M. Skowronski, "The mechanism of micropipe nucleation at inclusions in silicon carbide," *Applied Physics Letters,* vol. 75, pp. 784-786, 1999.
[58] P. G. *Neudeck* and J. A. Powell, "Performance limiting micropipe defects in silicon carbide wafers," *Electron Device Letters, IEEE,* vol. 15, pp. 63-65, 1994.
[59] T. Kimoto, N. Miyamoto, and H. Matsunami, "Performance limiting surface defects in SiC *epitaxial* p-n junction diodes," *Electron Devices, IEEE Transactions on,* vol. 46, pp. 471-477, 1999.
[60] A. R. Powell and L. B. Rowland, "SiC materials-progress, status, and potential roadblocks," *Proceedings of the IEEE,* vol. 90, pp. 942-955, 2002.
[61] H. Chih-Fang and J. A. Cooper, Jr., "High current gain 4H-SiC npn bipolar junction transistors," *Electron Device Letters, IEEE,* vol. 24, pp. 396-398, 2003.
[62] M. Domeij, H. S. Lee, E. Danielsson, C. M. Zetterling, M. Ostling, and A. Schoner, "*Geometrical* effects in high current gain 1100-V 4H-SiC BJTs," *Electron Device Letters, IEEE,* vol. 26, pp. 743-745, 2005.
[63] R. Sei-Hyung, A. K. Agarwal, S. Ranbir, and J. W. Palmour, "1800 V NPN bipolar junction *transistors* in 4H-SiC," *Electron Device Letters, IEEE,* vol. 22, pp. 124-126, 2001.
[64] P. A. Ivanov, M. E. Levinshtein, J. W. Palmour, A. Agarwal, and S. Krishnaswami, "Current gain *of* 4H–SiC high-voltage BJTs at reduced temperatures," *Semiconductor Science and Technology,* vol. 22, pp. 613-615, 2007.
[65] A. *Agarwal*, "A Case for High Temperature, High Voltage SiC Bipolar Devices," *Materials Science Forum,* vol. 556-557, pp. 687-692, 2006.
[66] Z. Jianhui, L. Yanbin, P. Alexandrov, L. Fursin, and J. H. Zhao, "A high current gain 4H-SiC NPN power bipolar junction transistor," *Electron Device Letters, IEEE,* vol. 24, pp. 327-329, 2003.
[67] H. S. Lee, M. Domeij, C. M. Zetterling, M. Ostling, F. Allerstam, and E. O. Sveinbjornsson, "Surface passivation oxide effects on the current gain of 4H-SiC bipolar junction *transistors*," *Applied Physics Letters,* vol. 92, pp. 082113-3, 2008.
[68] H. *Miyake*, T. Kimoto, and J. Suda, "4H-SiC bipolar junction transistors with record current gains of 257 on (0001) and 335 on (000–1)," in *Power Semiconductor Devices and ICs (ISPSD), 2011 IEEE 23rd International Symposium on*, 2011, pp. 292-295.
[69] M. E. Levinshtein, S. L. Rumyantsev, and M. S. Shur, *Properties of Advanced Semiconductor Materials: GaN, AIN, InN, BN, SiC, SiGe*: Wiley, 2001.
[70] M. E. Levinshtein, S. L. Rumyantsev, and M. S. Shur, *Properties of Advanced SemiconductorMaterials GaN, AlN, SiC, BN, SiC, SiGe*. New York: John Wiley & Sons, Inc., 2001.
[71] M. Roschke and F. Schwierz, "Electron mobility models for 4H, 6H, and 3C SiC [MESFETs]," *Electron Devices, IEEE Transactions on,* vol. 48, pp. 1442-1447, 2001.
[72] C.-W. Soong, X. Fu, S. Rajgopal, S. L. Garverick, and M. Mehregany, "Electrical Characteristics of JFETs Across a 2-Inch 6H-SiC Wafer," presented at the MRS spring *meeting*, San Francisco, CA, 2012.
[73] C. W. Soong, A. C. Patil, S. L. Garverick, X. Fu, and M. Mehregany, "550 ^{o}C Integrated Logic *Circuits* using 6H-SiC JFETs," *Electron Device Letters, IEEE,* vol. 33, pp. 1369-1371, 2012.

[74] S. L. Garverick, C.-W. Soong, and M. Mehregany, "SiC JFET integrated circuits for sensing and control at temperatures up to 600°C," in *Energytech, 2012 IEEE*, 2012, pp. 1-6.
[75] C.-W. Soong, S. L. Gaverick, X. Fu, A. Patil, and M. Mehregany, "A Fully-Monolithic, 6H-SiC JFET-based Transimpedance Amplifier for High-Temperature Capacitive Sensing," *Transaction on Electron Devices,* 2013.