DESIGN AND RAPID-PROTOTYPING OF MULTIDIMENSIONAL-DSP BEAMFORMERS USING THE ROACH-2 FPGA PLATFORM

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Thesis

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ABSTRACT

Radio frequency (RF) antenna array beamforming based on electronically steerable wideband phased-array apertures find applications in communications, radar, imaging and radio astronomy. High-bandwidth requirements for wideband RF applications necessitate hundreds of MHz or GHz frame-rates for the digital array processor. Systolic array architectures are often employed in multi-dimensional (MD) signal processing for linear and rectangular antenna arrays. Thus, this research used a FPGA hardware platform, the ROACH-2, which is equipped with a Xilinx Virtex-6 SX475T FPGA chip, and which is widely used in the field of radio astronomy. The research concentrated on the prospects of implementation of systolic array based MD beamformers on the ROACH-2, and on methods of extending the operating frequency to GHz range by using polyphase structures. The proposed systolic array architectures employ a differential form 2-D IIR frequency planar beam filter structure which is low in hardware utilization. The study highlights techniques that can be used to overcome the limitations of the ROACH-2 signal processing platform to achieve high operating frequencies.

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CHAPTER I

INTRODUCTION TO MULTI-DIMENSIONAL SIGNAL PROCESSING

Processing of signals in nature is of utmost importance and can be defined as the art of modifying acquired time-series data for the purpose of analysis or enhancement [4, 5]. A review of the history of signal processing clearly portrays that signal processing has revolutionized the living standard of human beings. The study of processing electromagnetic waves in the radio frequency (RF) spectrum has been one of the popular research topics to modern day. The applications of RF signal processing are broad, mainly in areas such as mobile communications, radar [2], cognitive radio and radio astronomy [6].

The techniques used for RF signal processing vary depending on the size and configuration receiver antennas, which can range from large structures up to small elements [7, 8]. The goal is to build mechanisms and devices to capture the required signal component while rejecting unwanted noise signals. Directional sensing (or directional enhancement) involves processing RF signals that are received from a particular direction of arrival (DOA) while suppressing both interfering signals from other directions and additive white Gaussian noise (AWGN).

In order to perform directional sensing, the antennas should be aligned towards the desired DOA such that the main beam is able to absorb a greater

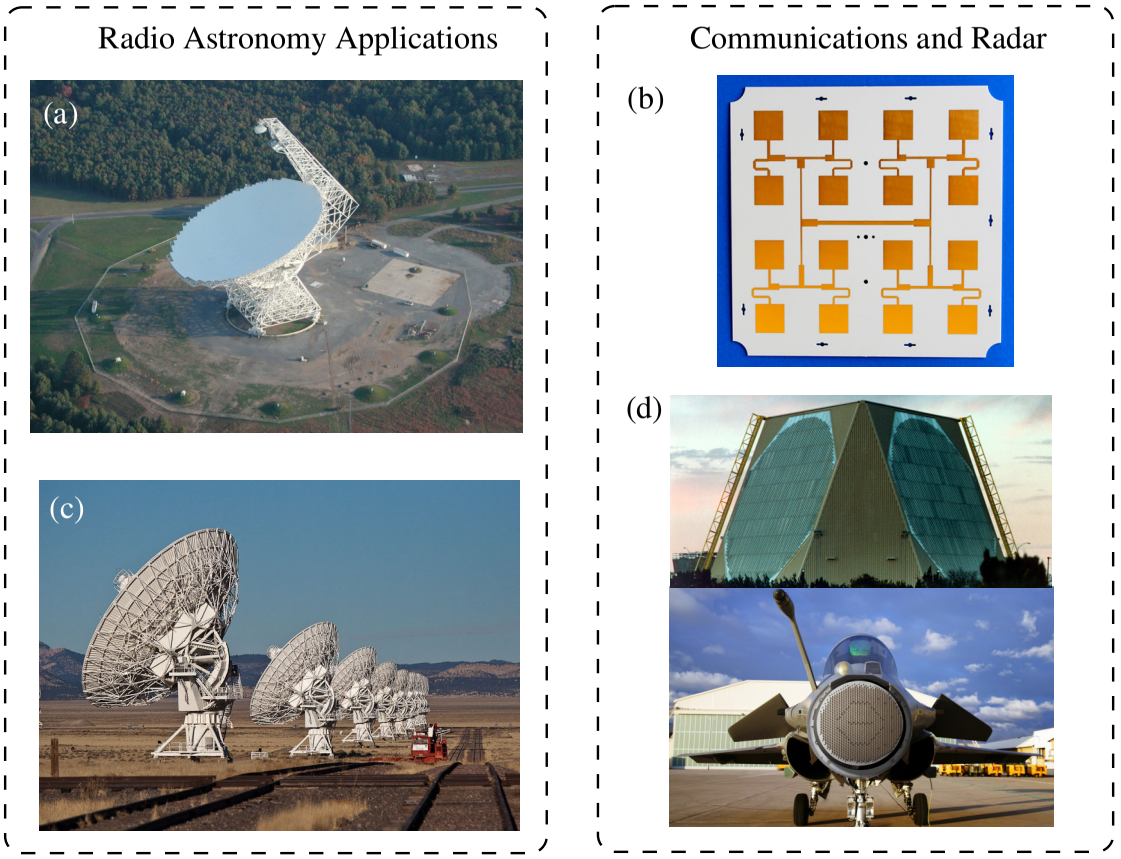

Figure 1.1: Types of antennas used in RF signal processing for beamforming applications. (a) Mechanically steerable large antenna structure, Green bank telescope (WV), (b) Small rectangular patch antenna array, (c) Large antenna array with mechanical steering to align to the desired DOA, Very large array (NM), (d) Phased array based radar systems used in Military applications. [2]

portion of the energy. Steering antennas mechanically [9, 10] [see Fig. 1.1(a)] is tedious and time consuming process and thus highly inefficient. These drawbacks can be overcome by using multi-dimensional (MD) space-time signal processing [11, 12] methods that employ antenna arrays [13, 14] [see Fig. 1.1(c)] while electronically steering the beamformer to align with the designated DOA with high precision. MD signal processing involves two or three dimensions in the mathematical analysis: the temporal domain and one or more spatial domains based on the signal of interest. A uniform linear array (ULA) [15, 16] can be used for two-dimensional (2-D) signal processing while three dimensional (3-D) processing can be performed using a rectangular array [17, 18].

Another important aspect of digital signal processing (DSP) is the hardware and computational complexity of the beamforming algorithms [19]. In general, beamforming systems that support wideband signals [20] have complex mathematical models compared to the narrowband realizations. By increasing the number of elements in the antenna array, it is possible to get better performance and directional selectivity at the expense of increased cost for additional hardware resources.

The scope of this thesis covers existing filtering models along with a review of available wideband and narrowband beamformers. Special attention is given to frequency-planar digital beam filters based on network resonance which are infinite impulse response (IIR) [11, 21, 21, 22] by nature. Moreover, we elaborate an improved version of 2-D IIR beam filters also known as the differential form [23] that has several advantages over the direct form version. The following ideas are highlighted in this

thesis as techniques of performance improvement when realizing IIR beamformers using field programmable gate array (FPGA) hardware.

1. MD IIR [24] digital filters are less complex compared to existing space-time filtering techniques, which are basically finite impulse response (FIR) [25] in nature. The proposed digital beam filters demonstrate similar directivity properties for a small number of digital hardware.

2. The structure of FIR beamformers contain only zero manifold thus leading to the requirement of higher order transfer function to get better directional enhancement properties while the recursive structure (with a feedback-loop) in IIR beamformers achieve a similar enhancement in directional performance with a low order transfer function.

3. MD signal processing beamformers based on network resonance [11] accept multiple inputs and produce multiple outputs leading to multiple input multiple output (MIMO) [26, 27] based designs while conventional beamformers produce a single output after processing signals from multiple inputs.

4. Electronically steerable [28, 29] realizations that can operate in real-time can be derived using closed-form relationship of the beam filter coefficients and the desired DOA.

5. Realizing beamformer designs in FPGA [30, 31, 32] hardware platforms are bound by limitations in both the designs and available technology. Thus, it

is essential to alter designs to suit the required specifications to achieve the desired performance.

1.1 Contributions to this Thesis

This thesis presents a study on enhancing the performance of existing beamforming techniques and their applications, by utilizing the unique characteristics of the MD beam filters. Contributions of this thesis can be summarized as follows;

1. The approach to derive a stable wideband differential for 3-D IIR frequency planar beam filter from 2-D beam filters based on network resonance using space-time techniques for uniform linear array of antennas at a designated DOA that can be realizable in FPGA signal processing platforms is proposed.

2. The differential form version of the 2-D IIR beam filters has the lowest hardware footprint on-chip leading to tremendous savings in cost, but the introduction of polyphases in the feedback loop leads to an increase in hardware resource consumption while maintaining identical performance as the direct form version.

3. The limitations of achievable fabric rates of sampling rates of multi-channel ADC chips and FPGAs of state of the art technologies determines the maximum achievable operating frequency of RF digital signal processing designs. We propose the use of polyphase structures combined with MD signal processing for antenna arrays with digital pipelining methods to gain improved beamformer

performance and operating frequency at the expense of high hardware resource consumption and computation complexity.

4. An approach to design a differential form 3-D IIR frequency planar beam filter using two 2-D IIR frequency planar beam filters in cascade is developed. An analysis of design specifications mapping to a real-world application further highlights feasibility of implementation.

1.2 Publications

The research contributions are reported in two conference publications as listed below.

1. V. Seneviratne, A. Madanayake, and N. Udayanga, "Wideband 32-element 200 MHz 2-D IIR beam filters using ROACH-2 Virtex-6 sx475t FPGA," In IEEE 9th International Workshop on Multidimensional (nD) Systems (nDS), Sept 2015, pages 1-5.

2. V. Seneviratne, A. Madanayake, and L. T. Bruton, "A 480MHz ROACH-2 FPGA Realization of 2-Phase 2-D IIR Beam Filters for Digital RF Apertures," In 2016 Moratuwa Engineering Research Conference (MERCon), Moratuwa, 2016, pp. 120-125. [Best paper award, Telecommunication systems category]

1.3 Thesis Outline

The rest of the chapters in this thesis unfolds as follows.

Chapter 2 introduces the concepts of plane waves in space and time and directional enhancement properties from a desired DOA for linear and rectangular antenna arrays (specifically highlighting 2-D and 3-D signals). A description of spectral properties of plane waves of 2-D and 3-D beam filters is followed by a review of existing space-time filtering techniques. The theoretical concepts of modeling of MD IIR beam filters using resistively terminated passive prototype network-resonant circuits and a review on existing narrowband and wideband beamformers is also introduced. Finally, an overview of the ROACH-2 signal processing platform and its key features related to RF-based MD signal processing applications for emerging technologies is also introduced.

Chapter 3 explains a realization of 2-D IIR frequency planar beam filter in ROACH-2 hardware platform at a fabric clock rate of 200 MHz. The system architecture proposed in this approach is based on a ULA of 32 antenna elements. We also describe the proper mechanism to feed buffered signals into the hardware platform without any loss of data and the capturing of the beamformed output to memory in ROACH-2. Simulation results verify the successful realization of the beam filters along with insight as to the resource consumption and timing details for two different word lengths.

Chapter 4 describes the realization of a polyphase system architecture of the 2-D IIR beam filter proposed in chapter 3 as a method to extend the operating frequency under the existing limitations in sampling using the 16-channel ADC card of ROACH-2. We propose a mathematical representation on how to apply look-ahead (LA) [33] techniques on the recursive loop of an IIR transfer function and derive the polyphase components of the highly complex polyphase beam filter design. The simulation results contain the frequency domain responses of phases, final beam filter output with the aliasing effects and results obtained by interleaved polyphase sampling.

Chapter 5 concentrates on the FPGA design and realization extending the differential form 2-phase polyphase 2-D IIR beam filter to 4-polyphases. In the simulation results section we present the directional enhancement properties along with a comprehensive explanation of the observations and the verification of successful realization. A numerical comparison of the resource consumption is provided to build insight into the increase in the number of multipliers/adders used for the beam filter block in systolic array implementations.

Chapter 6 presents a 3-D IIR frequency planar beam filter design that was realized in FPGA using the differential form transfer function. In this chapter it is highlighted that an RF signal received at a rectangular antenna array in 3-D space can be directionally enhanced by filtering the signal in two spatial dimensions orthogonal to each other but interconnected sequentially. The proposed architecture consists of two 2-D beam filters arranged in series to obtain the 3-D beam filter. Moreover,

the frequency domain response and the filtering characteristics are discussed. To get a better understanding of the hardware footprint, the ASIC hardware resource consumption and the achievable fabric rates for a few test cases are included. The latter part of the chapter focuses on a comprehensive analysis and technical specifications that can be used in existing and potential applications. We propose a beamformer that can be built by integrating all the concepts covered within this research. Another part of the review pays attention to the hardware resources required if this application was realized practically.

Chapter 7 concludes the thesis with a summary of the research outcome and a description of future work that will lead to applications.

CHAPTER II

MULTI DIMENSIONAL SIGNAL PROCESSING OF PLANE WAVES

Analysis of electromagnetic waves (EM) in the radio frequency spectrum is salient in many areas of electrical engineering, especially in areas such as wireless communications, radar, and radio astronomy. Beamforming or directional enhancement [34] of a far-field signal transmitted from an antenna at a significantly large distance employs antenna arrays at the receiver end [35, 36, 37]. The methods of processing a given signal of interest are based on its spatio-temporal nature. A one dimensional (1-D) signal in space $x \in \mathbb{R}$ can be described using two variables, with one independent temporal variable (preferably time, t) and one spatial variable. However, generally in nature EM waves propagate in the $(x, y, z) \in \mathbb{R}^3$ 3-D space and are described using a 4-D space-time plane wave signal [38] as illustrated in Fig. 2.1. An EM wave is a combination of a transverse electric field, $E_y(x, y, z, ct)$ and a magnetic field, $H_x(x, y, z, ct)$ oscillating orthogonally to each other, where $(x, y, z, ct) \in \mathbb{R}^4$, and $c \approx 3 \times 10^8 ms^{-1}$ is the speed of light in air. The wave front of a 3-D plane wave [38] is given by,

$$\alpha_1 x + \alpha_2 y + \alpha_3 z + ct = \lambda \tag{2.1}$$

where, $\lambda \in \mathbb{R}^1$ is constant-valued in the hyper-plane and $\alpha_k \in \mathbb{R}^1,\ k = 1, 2, 3$. The unit vector normal to the plane wave front can be defined as $\hat{n} = \alpha_1 \hat{x} + \alpha_2 \hat{y} + \alpha_3 \hat{z}$.

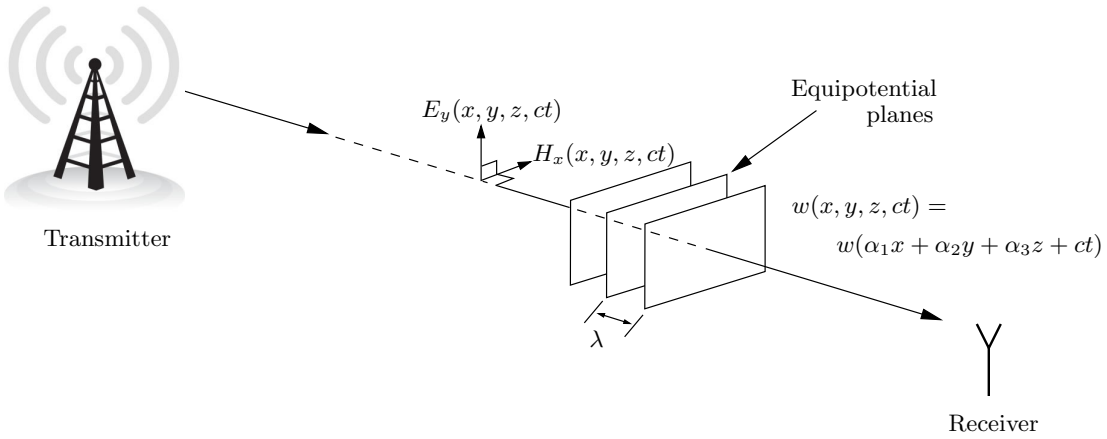

Figure 2.1: Plane wave propagation of a signal emitted from a transmitter received by an antenna at a faraway distance.

The signal processing technique for signals being transmitted is determined depending on the configuration at the receiver, i.e., number of antenna elements and their placements. 1-D signal processing techniques are used when only one antenna element is present at the receiver end. Since the spatial location of the antenna is a constant $P = (x_k, y_k, z_k)$, the signal can be extracted by means of the temporal variable. A 1-D signal can be represented as,

$$w_{pw}(\alpha_1 x_k + \alpha_2 y_k + \alpha_3 z_k + ct) = w(k + ct) = w(ct) \tag{2.2}$$

where k is a constant that defines the plane wave front. In this case, it is not possible to filter a signal transmitted by a specific transmitter of interest because there is no spatial variable involved. The filtering can be done only if the antenna is mechanically steered so that its beam is aligned with the direction of the received signals, such that the radiation pattern [39, 40, 41] of the signal extracts a considerable portion of energy in comparison with energy of undesired signals present at the receiver.

Hence, in order to detect a signal transmitted from a particular antenna, at least one spatial variable should be included in the signal processing technique. Introduction of one spatial variable will result in two dimensions (2-D) in the mathematical model and the corresponding system can be expressed using two independent variables x and ct,

$$w(x, ct) = w_{pw}(\alpha_1 x + ct) \tag{2.3}$$

where $x = n_x \Delta x$. Here, Δx is the spacing between two antenna elements and $n_x = 1, 2, ..., N$ is the antenna index. Since the system can be described using two variables, 2-D signal processing techniques are able to process signal data to obtain a desired output. Similarly, 3-D signal processing techniques should be employed to process the captured signal if the signal is spatially sampled using a rectangular antenna array as shown in Fig. 2.3(a).

Typically, receiver-side beamforming has been achieved using highly-directional receiver antennas, typically employing parabolic reflectors or horns and antenna array configurations with passive phasing networks such as phased arrays, delay-and-sum networks and reflect arrays.

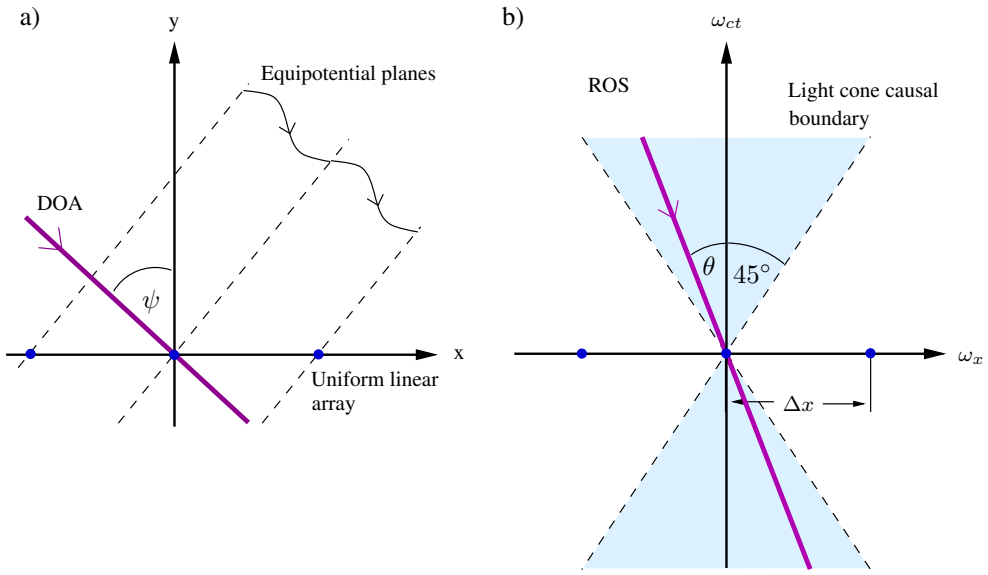

Figure 2.2: Plane wave received at a uniform linear array of antennas with spacing Δx in (a) 2-D space (x,y) domain and, (b) 2-D space-time (x,ct) domain.

2.1 Spectrum of a MD Plane Wave Signal

This section describes the time domain interpretation of 2-D/3-D plane wave signals and the transformations used to derive the frequency spectrum of a beamformer to obtain the region of support (ROS) of the signal of interest.

2.1.1 Spectrum of 2-D Plane Wave Signals

Consider a plane wave in 2-D space arriving from a direction of arrival (DOA) ψ [42], $(0° \leq \psi \leq 90°)$ as shown in Fig. 2.2(a). The direction of propagating is measured with respect to the broadside direction of the antenna array in the counter clockwise direction. An antenna array with inter-antenna spacing Δx is used to sample the plane wave in spatial direction x. From Fig. 2.2(a) the time taken for the wave front of the plane wave to travel from an antenna to the next antenna ΔT [43] can be

calculated as,

$$\Delta T = \frac{\Delta x}{c} \sin \psi \tag{2.4}$$

However, in the space-time (x, ct) domain the relationship between the space-time ROS θ [43] and the spatial DOA ψ is given by [Fig. 2.2(b)],

$$\theta = \tan^{-1}(\sin \psi) \tag{2.5}$$

Moreover, we can observe that the plane waves with spatial DOAs ($-90^\circ \leq \psi \leq 90^\circ$) are confined into a 45° light cone [44] ($-45^\circ \leq \theta \leq 45^\circ$) in the space-time domain.

The digital signals of the received signal are sampled using analog-to-digital converters (ADC) at each antenna. We can obtain the discrete domain interpretation of the 2-D space-time signal by sampling the signal at a sampling frequency of $F_s = 1/T$,

$$w\left[n_x, n_{ct}\right] = w\left(\Delta x\ n_x, c\Delta T\ n_{ct}\right) = w_{pw}\left(-\sin\psi\ \Delta x\ n_x + c\Delta T\ n_{ct}\right) \tag{2.6}$$

The 2-D Discrete Fourier Transform (DFT) of the plane wave denotes the frequency spectrum $(\omega_x, \omega_{ct}) \in \mathbb{R}^2$ of the digitized signal $w\left[n_x, n_{ct}\right]$.

The ROS of a plane wave signal is the region where the magnitude of the frequency spectrum is not defined to be zero. The ROS of a plane wave signal oriented at a DOA ψ is confined to a straight [45] line, which passes through the origin (0,0) at an angle θ to the ω_{ct} axis in the 2-D frequency domain (ω_x, ω_{ct}), as shown in Fig. 2.2(b). The equation of the ROS line is given by,

$$\omega_{ct} + \omega_x \sin \psi = 0 \tag{2.7}$$

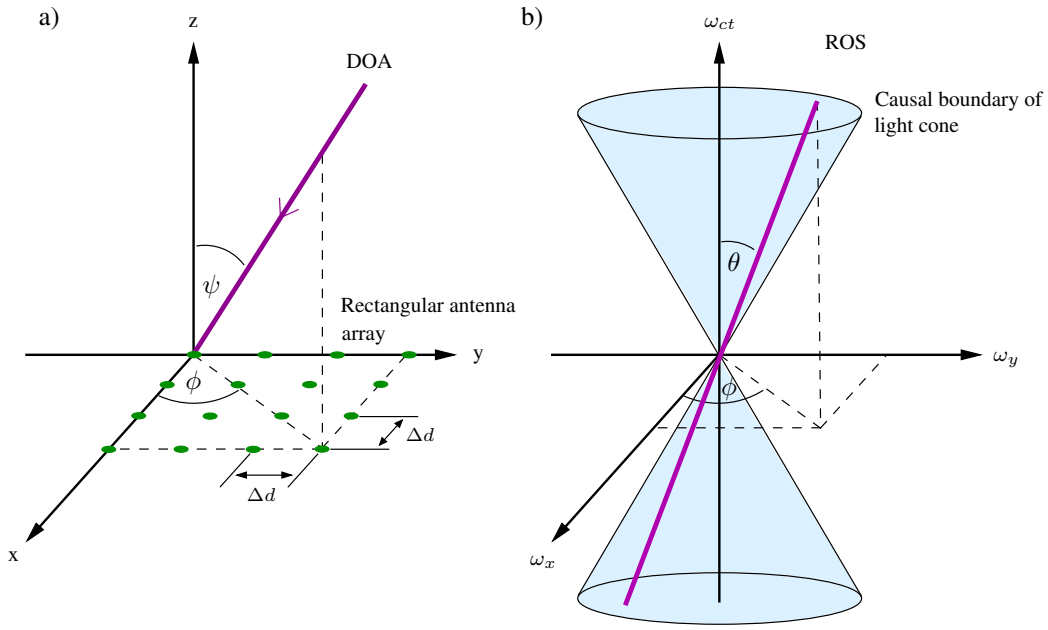

Figure 2.3: Plane wave received at uniform rectangular array of antennas with spacing Δd in (a) 3-D space (x,y,z) domain and, (b) 3-D space-time (x,y,ct) domain.

Each signal received from various directions at a linear antenna array is represented as a line in the frequency domain at angles θ_i for each plane wave i where $\tan\theta_i = \sin\psi_i$. Thus, by using an appropriate filtering system, we should be able to selectively enhance a signal from a designated DOA ψ.

2.1.2 3-D Space-time Plane Wave Signals and Their Spectra

Consider an EM plane wave received at an antenna in 3-D space as shown in Fig. 2.3(a), $w(x, y, ct) = w_{pw}(\sin\psi\cos\phi\ x + \sin\psi\sin\phi\ y + ct)$ arriving from a DOA (ψ, ϕ), where ψ is the elevation angle and ϕ is the azimuth angle [22]. A uniformly distributed rectangular array of antennas placed in the $x - y$ plane with $N_x \times N_y$ antenna elements (with identical omnidirectional characteristics) is used to spatially

sample the plane wave signal. Here, Δd is the inter-antenna spacing in both x and y directions and N_x, N_y are the number of antenna elements in x, y directions respectively. The signal received on an antenna element is sent through a low noise amplifier and a bandpass filter before being digitized by the ADC [43], which produces samples every ΔT seconds, where sampling frequency $F_s = \frac{1}{\Delta T}$. The 3-D discrete signal $w\left[n_x, n_y, n_{ct}\right]$ [11, 46] obtained at the ADCs can be written as,

$$w\left[n_x, n_y, n_{ct}\right] = w_{pw}\left(\sin\psi\cos\phi\ \Delta d\ n_x + \sin\psi\sin\phi\ \Delta d\ n_y + \cos\psi c\Delta T\ n_{ct}\right). \quad (2.8)$$

Fourier domain representation of the 3-D discrete signal $w\left[n_x, n_y, n_{ct}\right]$ can be used to determine the ROS and frequency domain properties of the 3-D plane wave. MD signal processing theory shows that the ROS (See Fig. 2.3(b)) of the plane wave coming from a DOA (ψ, ϕ) is confined to a beam in the $(\omega_x, \omega_y, \omega_{ct}) \in \mathbb{R}^3$ 3-D frequency domain, which passes through the origin, has an angle θ to the ω_{ct} axis and has an angle ϕ to the ω_x axis [11]. Here $\tan\theta = \sin\psi$. ω_x, ω_y are the normalized spatial frequency variables, and ω_{ct} is the temporal frequency variable. The equation of the ROS line is given by,

$$\frac{\omega_x}{\sin\theta\cos\phi} + \frac{\omega_y}{\sin\theta\sin\phi} + \frac{\omega_{ct}}{\cos\theta} = 0 \quad (2.9)$$

The next section focuses on beamforming techniques or filtering techniques in general while highlighting the specifics of multi-dimensional space-time plane wave beamformers for a given DOA which are designed to be directionally enhanced.

2.2 Space-time Beamforming Techniques for MD Signals

In beamforming [47], we estimate the signal of interest arriving from some specific direction in the presence of noise and interfering signals with the aid of an array of sensors. These sensors are located at different spatial locations to sample the propagating waves in space. The collected spatial samples are then processed to attenuate/null-out the interfering signals while spatially extracting the desired signal. As a result, a specific spatial response of the array is achieved with 'beams' pointing to the desired signals and 'nulls' towards the interfering ones [48].

One advantage of using an array of sensors, relevant at any wavelength, is the spatial filtering versatility offered by discrete sampling. It is important to alter the spatial filtering function in real-time to ensure effective suppression of interfering signals in many applications. This change is easily implemented in a discretely sampled system by modifying the way in which the beamformer linearly combines the signals. Changing the spatial filtering function of a continuous aperture antenna is impractical [49].

Space-time filtering techniques can be classified into two main categories based on the signal of interest as narrowband and wideband beamformers to perform directional enhancement in both time and frequency domain. Time domain signal processing takes place at the ADC outputs directly, whereas frequency domain systems obtain the frequency spectrum of the received signal prior to the signal processing.

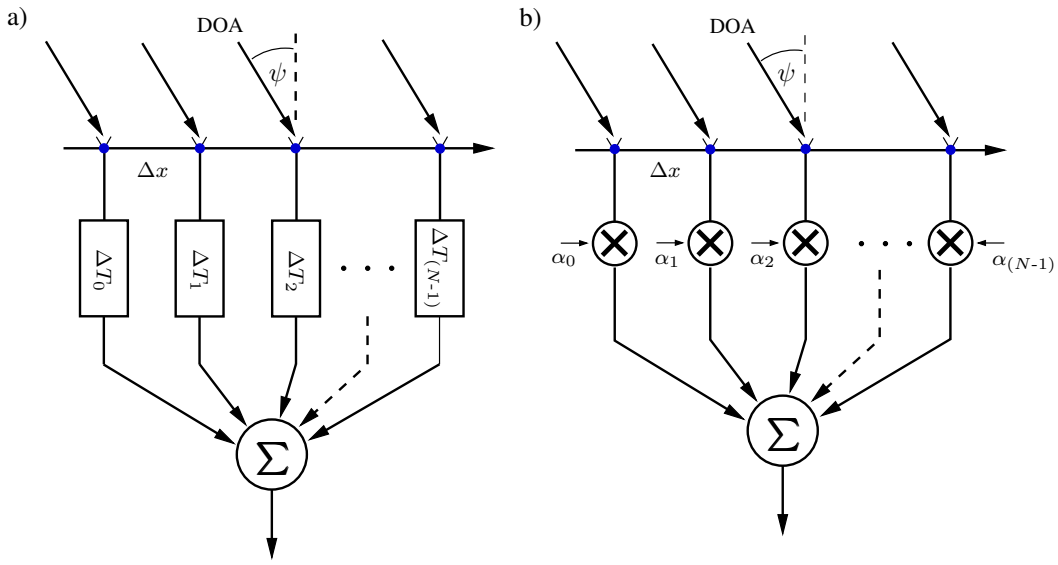

Figure 2.4: Narrowband beamformer models. (a) Delay-and-sum beamformer and, (b) Phased array beamformer.

2.2.1 Narrowband Beamformers

Narrowband beamformers perform spatial filtering at a particular frequency over a narrow bandwidth (<10%) or a small frequency range of the received signal. This means the phase difference between upper and lower band edges for propagation across the entire array is small. Typically many communication signals fit this model.

Delay-sum beamformer [50, 51, 52] is a widely known narrowband beamformer (see Fig. 2.4(a)) which is built by accumulating delayed samples of the received signal to construct the beamformed output. A delay parameter is changed to obtain the desired delay $\Delta_x T$ and in turn to obtain the beam direction of ψ and the effective radiation pattern of the array in the desired direction. Delay line lengths can be changed to get the appropriate delays, where $T = \frac{\Delta x}{c} \sin \psi$. Directionally

enhanced output $y[n_{ct}]$ can be expressed as [50, 51],

$$y[n_{ct}] = \sum_{n=0}^{N-1} p_n w\big(n, c\left(t - (N-n)\,\Delta_x T\right)\big) \tag{2.10}$$

where p_n are beamformer weights. When the delay is set to $T = \tau$, the channels are all time aligned for a signal from direction ψ. Gain in direction ψ is $\sum_{n=0}^{N-1} p_n$ and is less in other directions due to incoherent addition.

Another type of narrowband beamformer is the phased array beamformer [53] which can be considered as the most commonly used beamformer that can be used to filter narrowband signals (see Fig. 2.4(b)). Here, the delayed samples of the received signal are obtained by multiplying signal with a phase component $e^{-j\omega_0 t_0}$ as the weights to achieve a delay of t_0. Phase-rotated signals are then summed to obtain the directionally enhanced output $y[n_{ct}]$ as follows.

$$y[n_{ct}] = \sum_{n_x=0}^{N-1} w\left[n_x, n_{ct}\right] \times e^{-j(N-n_x-1)\omega_{ct_0}\Delta T} \tag{2.11}$$

This type of beamformer can be modeled using a spatial finite impulse response (FIR) [54] filter with N elements having the transfer function,

$$H(z) = \frac{1}{N} \sum_{n=0}^{N-1} \alpha_n z_x^{-n} \tag{2.12}$$

where α_n are filter coefficients corresponding to each antenna. The enhancing capabilities and order of the transfer function can be increased by adding more antenna elements N to the array.

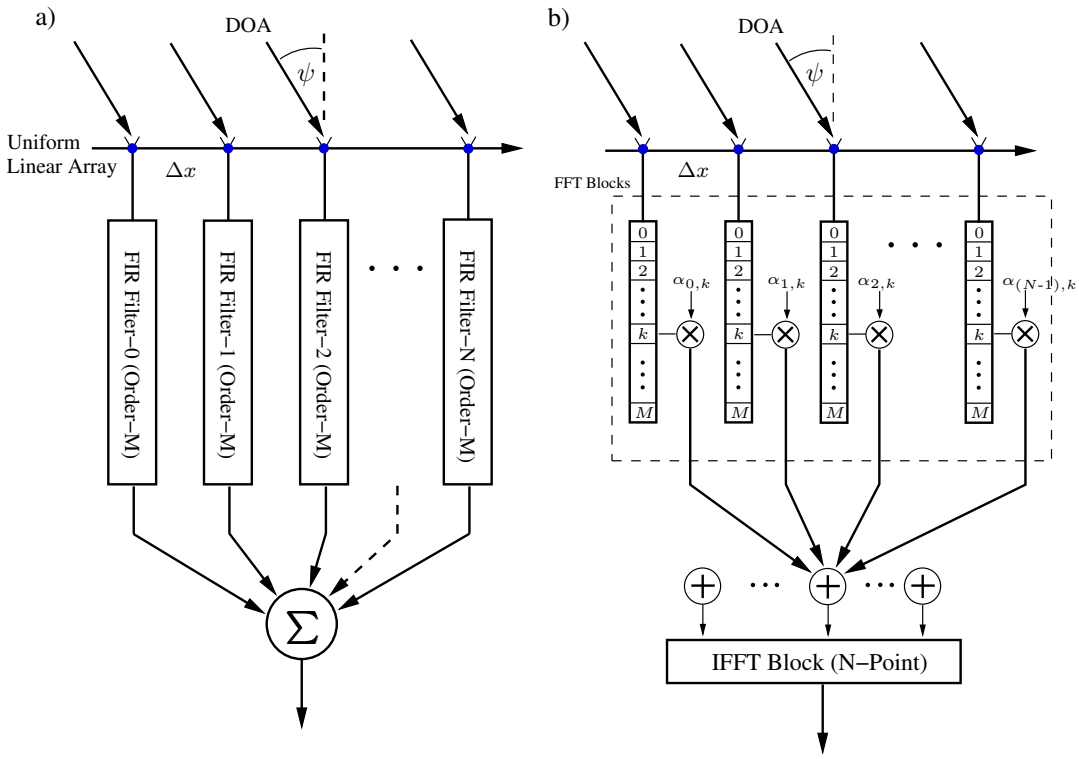

Figure 2.5: Wideband beamformer architectures corresponding to narrowband beamformers, (a) Filter-and-sum beamformer and, (b) FFT-based wideband beamformer.

2.2.2 Wideband Beamformers

Wideband beamformers [34] are capable of producing directional enhancement over a wide frequency range of received signal in comparison with narrowband beamformers. We can derive the respective wideband beamformer version of the phased array beamformer by extending the design with minor adjustments. The filter-and-sum architecture shown in Fig. 2.5(a) can be considered as an array of digital FIR filters where each filter output is combined to obtain the beamformed output $y[n_{ct}]$. Thus,

the discrete time output of the beamformer can be expressed as,

$$y[n_{ct}] = \sum_{n_x=0}^{N-1} \sum_{k=1}^{M} \alpha_{n_x,k} w\left[n_x, n_{ct} - k\right] \tag{2.13}$$

where $\alpha_{n_x,k}$ are the coefficients correspond to antenna index n_x and k^{th} tapped point linear FIR filter. FFT-based wideband beamformer [55, 56] shown in Fig. 2.5(b) is a frequency domain version of delay-sum beamformer. The M-point FFT of the input signal is obtained at each antenna, where M is the number of complex phasor weight multiplications of the received signal at a given antenna. The phase rotated signals are then added and fed in to an inverse fast Fourier Transform block to obtain the directionally enhanced outputs.

The next section introduces another method to realize digital filters, namely IIR filters along with modeling techniques to easily analyze the behavioral characteristics for MD plane wave signals while highlighting the unique advantages over FIR filters.

2.3 Modeling MD IIR Beam Filters using Passive LRC Networks

It has been shown that a plane wave with a specific DOA can be represented by a system which has a line shaped passband passing through the origin that satisfies Eq. (2.7) in 2-D space and Eq. (2.9) in 3-D space. These MD systems, which have IIR characteristics, can be modeled using resistively-terminated passive prototype networks.

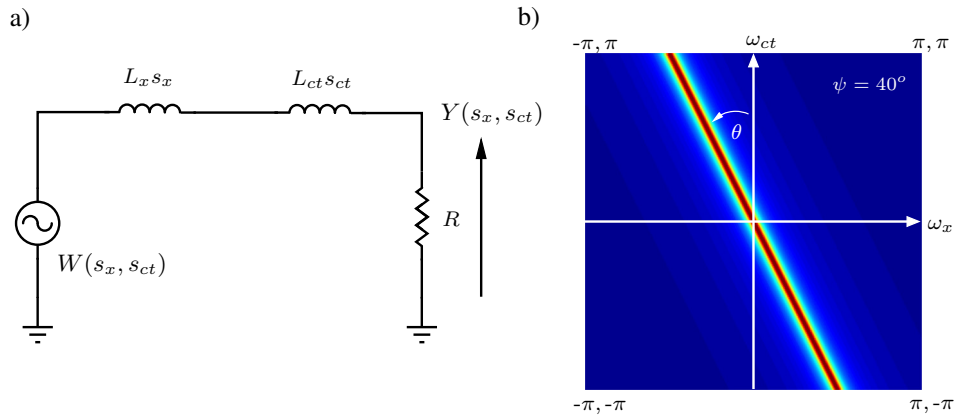

Figure 2.6: Passive prototype network model for the (a) 2-D first order passive prototype circuit and, (b) Frequency response of the 2-D beam filter with a $ROS = \theta$ in Laplace domain.

2.3.1 Passive Prototype Network of the 1^{st} Order 2-D IIR Beam Filter

Consider the 2-D first-order continuous-domain inductance-resistance network as shown in Fig. 2.6(a) with a spatial and temporal inductor $L_x \geq 0$ and $L_{ct} \geq 0$ respectively. The Laplace domain transfer function $H(s_x, s_{ct})$ of the network can be expressed as [11],

$$H(s_x, s_{ct}) = \frac{R}{R + L_x s_x + L_{ct} s_{ct}} = \frac{Y(s_x, s_{ct})}{W(s_x, s_{ct})} \tag{2.14}$$

where $R > 0$ and s_x, s_{ct} are Laplace variables corresponding to two dimensions x,ct. The corresponding input and output transforms are given by $Y(s_x, s_{ct})$ and $W(s_x, s_{ct})$. The frequency domain transfer function can be obtained by substituting $s_x = j\omega_x$ and $s_{ct} = j\omega_{ct}$ [11],

$$H(\omega_x, \omega_{ct}) = \frac{R}{R + jL_x\omega_x + jL_{ct}\omega_{ct}} = \frac{Y(\omega_x, \omega_{ct})}{W(\omega_x, \omega_{ct})} \tag{2.15}$$

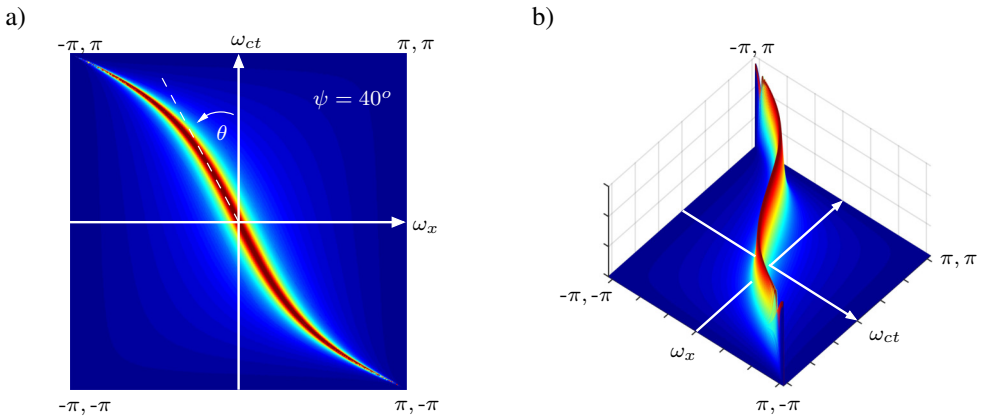

Figure 2.7: Frequency response of the 2-D IIR beam filter, $H(z_x, z_{ct})$ in z-domain showing the frequency warping effect at high temporal frequencies ($\omega_{ct} > 0.5\pi$).

By observing the above equation, we can note that the frequency response is maximum (at resonance) when the imaginary component of the transfer function is zero, that is, when $L_{ct}\omega_{ct} + L_x\omega_x = 0$. This represents a line shaped passband as expected (Fig. 2.6(b)). By choosing $L_x = \sin\theta$ and $L_{ct} = \cos\theta$, $(0° \leq \theta \leq 90°)$ we can align the passband of the beam at an angle θ leading to the expected DOA satisfying $\tan\theta = \sin\psi$. The digital version of the beamformer transfer function can be obtained by applying bilinear transform [57], substituting $s_x = \frac{1-z_x^{-1}}{1+z_x^{-1}}$ and $s_{ct} = \frac{1-z_{ct}^{-1}}{1+z_{ct}^{-1}}$ in Eq. (2.14),

$$H(s_x, s_{ct}) = \frac{R}{R + \sin\theta\left(\frac{1-z_x^{-1}}{1+z_x^{-1}}\right) + \cos\theta\left(\frac{1-z_{ct}^{-1}}{1+z_{ct}^{-1}}\right)} = \frac{Y(s_x, s_{ct})}{W(s_x, s_{ct})} \tag{2.16}$$

The z-domain transfer function can be expressed as,

$$H(z_x, z_{ct}) = \frac{\left(1 + z_x^{-1}\right)\left(1 + z_{ct}^{-1}\right)}{1 + b_{01}z_x^{-1} + b_{01}z_{ct}^{-1} + b_{11}z_x^{-1}z_{ct}^{-1}} \tag{2.17}$$

where the filter coefficients are given by,

$$b_{ij} = \frac{R + (-1)^i \cos\theta + (-1)^j \sin\theta}{R + \cos\theta + \sin\theta} \tag{2.18}$$

Here, note that the introduction of poles into the transfer function implies the inclusion of a feedback mechanism in the IIR beam filter. However, use of bilinear transformation in this approach cause a distortion of the beam-shaped passband at higher frequencies ($\frac{\pi}{2} < \omega_{ct} < \pi$) causing an effect known as *bilinear warping* [38]. This practical limitation can be avoided by oversampling the input signal appropriately in the spatial or temporal domain.

The discrete time-domain difference equation of the 2-D IIR frequency planar beam filter can be derived from Eq. (2.17) as follows,

$$y[n_x, n_{ct}] = \sum_{i=0}^{1}\sum_{j=0}^{1} w[n_x - i, n_{ct} - j] - \underbrace{\sum_{i=0}^{1}\sum_{j=0}^{1} b_{ij}}_{i+j\neq 0}\, y[n_x - i, n_{ct} - j] \tag{2.19}$$

where the coefficients b_{ij} are given by Eq. (2.18).

2.3.2 Passive Prototype Network of the 1^{st} Order 3-D IIR Beam Filter

Similarly, we can derive the multi-dimensional network resonant passive prototype network for the 3-D IIR beam filters by including an additional spatial inductor L_y to represent impact of the signal in the y-direction as shown in Fig. 2.8(a). The 3-D Laplace transform domain transfer function $H(s_x, s_y, s_{ct})$ of a resistively terminated inductor-resistor prototype [11, 58, 59] network is as follows.

$$H(s_x, s_y, s_{ct}) = \frac{R}{R + s_x L_x + s_y L_y + s_{ct} L_{ct}} \tag{2.20}$$

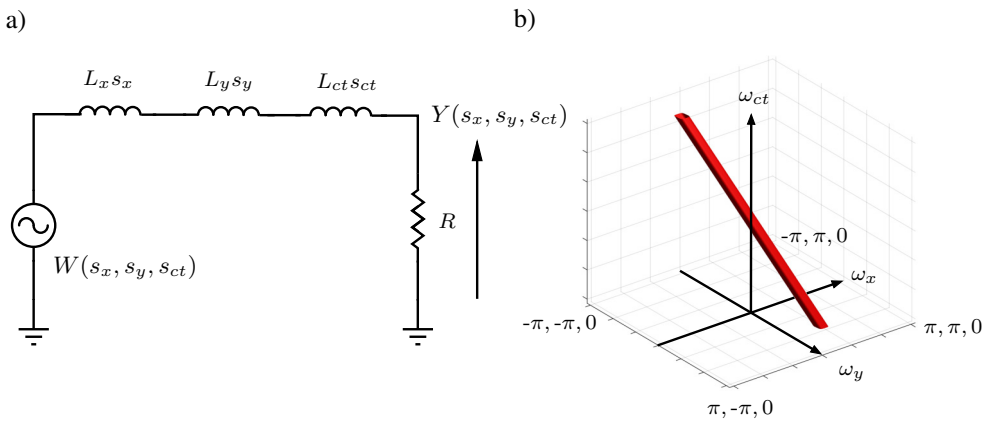

Figure 2.8: Passive prototype network model for the (a) 3-D first order passive prototype circuit and, (b) Frequency response of the 3-D beam filter with the beam shaped passband ($ROS = (\theta, \phi)$) in Laplace domain.

where $R > 0$ is the resistive termination and L_x, L_y, L_{ct} are passive inductors. Laplace variables s_x, s_y and s_{ct} correspond to spatial variables x, y and time variable ct respectively. By substituting $s_x = j\omega_x$, $s_y = j\omega_y$ and $s_{ct} = j\omega_{ct}$, the frequency domain response of this transfer function can be obtained as [11],

$$H(\omega_x, \omega_y, \omega_{ct}) = \frac{R}{R + j\omega_x L_x + j\omega_y L_y + j\omega_{ct} L_{ct}} \tag{2.21}$$

It can be noted that the passband of the 3-D beam filter form a beam passing through the origin in the 3-D frequency domain. The system achieves resonance when $L_x\omega_x + L_y\omega_y + L_{ct}\omega_{ct} = 0$. By setting $L_x = \sin\theta\cos\phi$, $L_y = \sin\theta\sin\phi$ and $L_{ct} = \cos\theta$, we can map the ROS of this 3-D IIR beam filter to satisfy Eq. (2.9) as expected for the 3-D scenario. Thus, a system that can directionally enhance signals arriving from a DOA (ψ, ϕ), where $\theta = \tan^{-1}(\sin\psi)$.

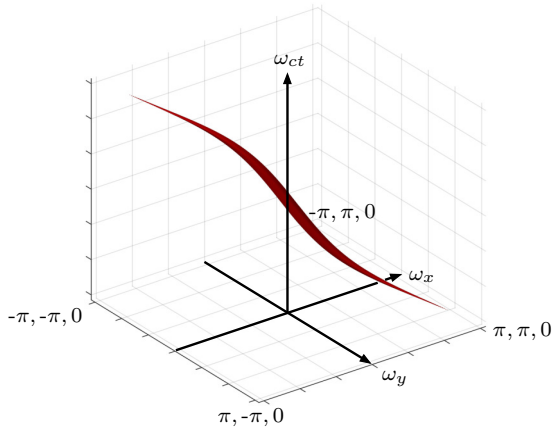

Figure 2.9: Frequency response of the 3-D IIR beam filter, $H(z_x, z_y, z_{ct})$ in z-domain showing the frequency warping effect at high temporal frequencies.

The digital domain transfer function can be obtained by applying bilinear transform in Eq. (2.21) for frequency variables, $s_x = \frac{1-z_x^{-1}}{1+z_x^{-1}}$, $s_y = \frac{1-z_y^{-1}}{1+z_y^{-1}}$ and $s_{ct} = \frac{1-z_{ct}^{-1}}{1+z_{ct}^{-1}}$. The 3-D z-domain transfer function is given by,

$$H(z_x, z_y, z_{ct}) = \frac{\sum_{i=0}^{1}\sum_{j=0}^{1}\sum_{k=0}^{1} z_x^{-i} z_y^{-j} z_{ct}^{-k}}{\underbrace{\sum_{i=0}^{1}\sum_{j=0}^{1}\sum_{k=0}^{1} b_{ijk} z_x^{-i} z_y^{-j} z_{ct}^{-k}}_{i+j+k\neq 0}} \tag{2.22}$$

where the new filter coefficients b_{ijk} are given by,

$$b_{ijk} = \frac{R + (-1)^i L_x + (-1)^i L_y + (-1)^k L_{ct}}{R + L_x + L_y + L_{ct}} \tag{2.23}$$

The corresponding input-output recurrence relationship described by the 3-D spatio-temporal difference equation is given by [58],

$$y\left[n_x, n_y, n_{ct}\right] = \sum_{i=0}^{1}\sum_{j=0}^{1}\sum_{k=0}^{1} w\left[n_x - i, n_x - j, n_{ct} - k\right] - \underbrace{\sum_{i=0}^{1}\sum_{j=0}^{1}\sum_{k=0}^{1} b_{ijk}\; y\left[n_x - i, n_y - j, n_{ct} - k\right]}_{i+j+k\neq 0} \quad (2.24)$$

where the filter coefficients b_{ijk} are defined in Eq. (2.23) and the system performance is limited by bilinear warping effect as in the 2-D scenario.

The 3-D IIR beam filters can also be modeled using two 2-D IIR beam filter which is enhancing signals from two different spatial variables which has the similar response as Eq. (2.24). A detailed analysis of this technique will be described in chapter 6. The next section reviews about another important aspect of IIR beamformers that determines the feasibility of practical implementation conditions on stability requirements of MD IIR beam filters.

2.4 Stability of MD Beamformers

It is important to evaluate the stability of a system and its input-output behavior. Conventionally a MD discrete system is considered to be Bounded-Input-Bounded-Output (BIBO) stable if, for every finite input sequence $|w\left(n_x, n_y, n_{ct}\right)| < \infty$, there exists a finite bounded output sequence $|y\left(n_x, n_y, n_{ct}\right)| < \infty$, i.e., the system response is deterministic for any finite valued sequence. Thus, the 3-D impulse response of the system requires to be absolutely summable in

conventional BIBO stability [60], leading to the stability requirement given by [61],

$$\sum_{n_x=0}^{\infty}\sum_{n_y=0}^{\infty}\sum_{n_{ct=0}}^{\infty}|h[n_x,n_y,n_{ct}]|<\infty \tag{2.25}$$

In practice, it is not feasible to have an infinite number of antenna elements. Hence, the limitations of the spatial index of uniform linear arrays (ULA) and rectangular arrays in reality fails to provide sufficient insight of the BIBO stability. Hence, it is needed to define alternate conditions to determine the stability of a practical systems. Thus, practical BIBO provides the relevant stability requirement where one or more of the multiple dimensions is allowed to be unbounded while preserving p-BIBO stability [62, 63]. Under p-BIBO, the stability criterion in Eq. (2.25) is,

$$\sum_{n_x=0}^{N_x-1}\sum_{n_y=0}^{N_y-1}\sum_{n_{ct=0}}^{\infty}|h\left[n_x,n_y,n_{ct}\right]|<\infty \tag{2.26}$$

IIR beamformers can be unstable under certain conditions due to the existence of the feedback mechanism in the transfer function. However, it has been shown that discrete domain transfer functions derived based on a passive prototype network are guaranteed to be p-BIBO-stable [62] as long as the selection of the Laplace domain coefficients are non-negative ($L_x \geq 0, L_y \geq 0, L_{ct} \geq 0$) and $R \geq 0$ to make the filter stable for $0^\circ \leq \psi \leq 90^\circ$. Moreover, all FIR beamformers are guaranteed to be stable due to the limited number of filter coefficients in practical implementations.

2.5 Polyphase Structures for Multirate Digital Signal Processing

A multirate DSP uses multiple sampling rates within the system [64, 65]. It involves altering the sampling rates by (increasing or decreasing) using decimators

and interpolators to achieve an expected rate that can be practically realizable in hardware. One efficient and straightforward structure utilized in digital multirate filters [66] is the polyphase structure. Such realizations, based on the original digital prototype interpolating transfer function without any modification, take advantage of the inherent multirate property and allow the main filter core to operate effectively at the lowest sampling rate of the system. Thus, the polyphase structure is appropriate for high-frequency filtering with added efficiency in terms of power and silicon area savings.

The use of multiple stages of decimation [67] can reduce computational and memory requirements of filters. Also it reduces the cost for processing because the memory and calculations for implementing a DSP system is proportional to the sampling rate. Reducing sampling rate results in a cheaper implementation. Downsampling by a factor M is implemented by keeping every M^{th} sample and throwing away $M-1$ samples in between. In polyphase implementation, first the signals are decimated and then filtered. Therefore only the outputs that will be used need to be calculated ultimately leading to an efficient computational load.

2.5.1 Nobel Identities for Decimators and Interpolators

Noble identities show us methods for changing the order of operations in signal flow graphs, when downsampling or upsampling operations are necessary. When a signal is down-sampled the anti-alias filtering can be done at a sub-sampled rate and when

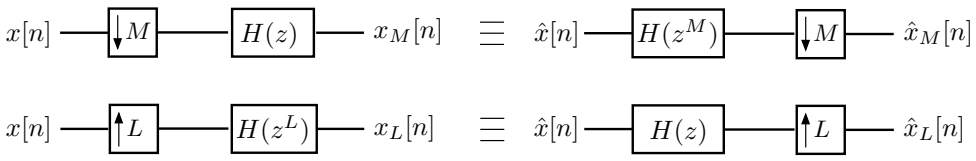

Figure 2.10: Polyphase noble identities for decimation and interpolation operations.

up-sampled the anti-imaging filtering can be done at the lower rate. Fig. 2.10 shows the Noble identities involved in polyphase structures [68].

2.5.2 Polyphase Decomposition and Interpolation

The polyphase decomposition multirate structure can be derived from the original by re-organizing the coefficients of a given filter into M-polyphase subfilters $H_m(z)$, where $m = 0, 1, ..., M-1$. The prototype filter $H_0(z)$ can be written in its M-band polyphase form as,

$$H_0(z) = \sum_{l=0}^{M-1} z^{-l} E_l(z^M) \tag{2.27}$$

where $E_l(z)$ is the l-th polyphase component of $H_0(z)$:

$$E_l(z) = \sum_{n=0}^{\infty} e_l[n] z^{-n} = \sum_{n=0}^{\infty} h_0[l + nM] z^{-n}, 0 \leq k \leq M \tag{2.28}$$

Substituting z with zW_M^k in the expression for $H_0(z)$ we arrive at the M-band polyphase decomposition of $H_k(z)$ as shown in Eq. (2.30).

$$H_k(z) = \sum_{l=0}^{M-1} z^{-l} W_M^{-kl} E_l(z^M W_M^{kM}) \tag{2.29}$$

$$H_k(z) = \sum_{l=0}^{M-1} z^{-l} W_M^{-kl} E_l(z^M) \tag{2.30}$$

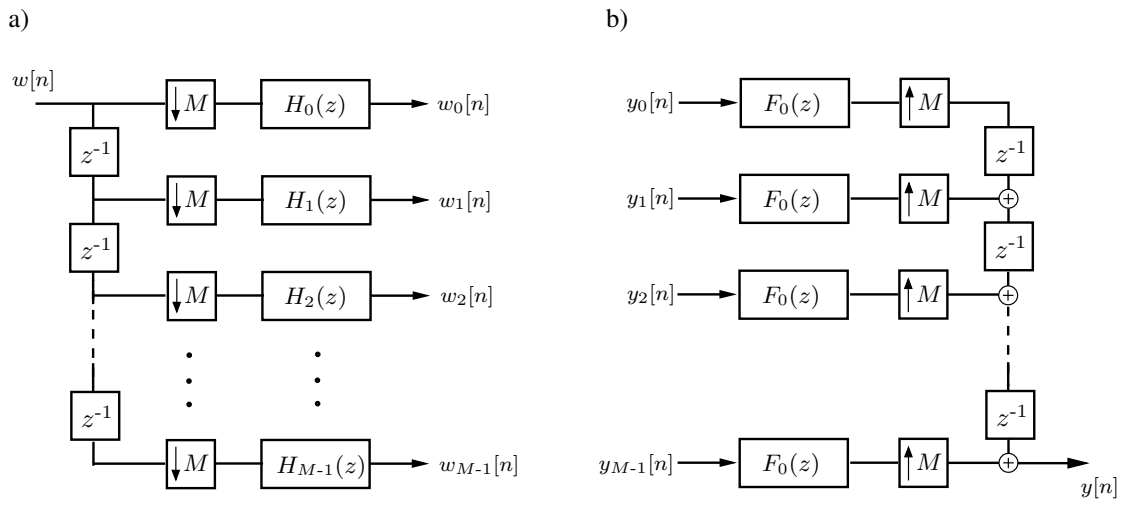

Figure 2.11: The signal flow graph (SFG) of polyphase structures. (a) Polyphase decomposition and, (b) Polyphase interpolation.

where $0 \leq k \leq M$ and $W_M^{kM} = 1$.

In the general case, we can describe the mechanics of this algorithm as follows. We design a low-pass filter that limits the spectral components to avoid aliasing and then decimate the filter, creating M-subfilters, one for each of the M-phases, by which we can decimate the input signal. This set of M subfilters is called a polyphase filter [66], and the combined set of M subfilters is known as a filter bank [64]. We apply the first polyphase subfilter to the decimated buffer, then shift in a new input sample and apply the second subfilter in the same way. This procedure is repeated M times to compute the first output. This entire procedure is depicted in Fig. 2.11.

Both FIR and IIR filters can be written in the polyphase form. The polyphase decomposition can be directly applied to the coefficients of an FIR filter to obtain the polyphase subfilters as explained earlier in 1-D and MD signal processing.

However, in IIR beam filters, the transfer function must sometimes be altered using look-ahead optimization methods to pipeline the structure before applying polyphase decomposition. The pipelining can be improved by employing look-ahead optimization techniques in IIR beam filters ultimately resulting a decrease in critical path delay of the filter. This enables the potential to improve the speed of operations. LA optimization methods are applied to the feedback mechanism of the beam filter based on the required number of polyphases involved in the design.

Polyphase structures have been further classified into different forms based on how the subfilters are designed [69] as direct, cascaded and hybrid polyphase structures in literature [70]. Thus, we can summarize that the concepts in polyphase structures can be considered a perfect alternative that can be used in DSP systems which demand improved data rates by appropriately eliminating the aliasing effects of subfilters.

The next section introduces a DSP platform that is gaining popularity in many fields for its appealing features and functionality.

2.6 ROACH-2 FPGA Platform

The "reconfigurable open architecture computing hardware version 2 (ROACH-2)" [71, 72] is an FPGA based hardware platform widely used in radio astronomy to process signals over a wide frequency range [73, 74]. It is the implementation platform of choice for many modern radio telescopes [75, 76] that require extensive digital signal processing for FX-correlations, multi-beamforming

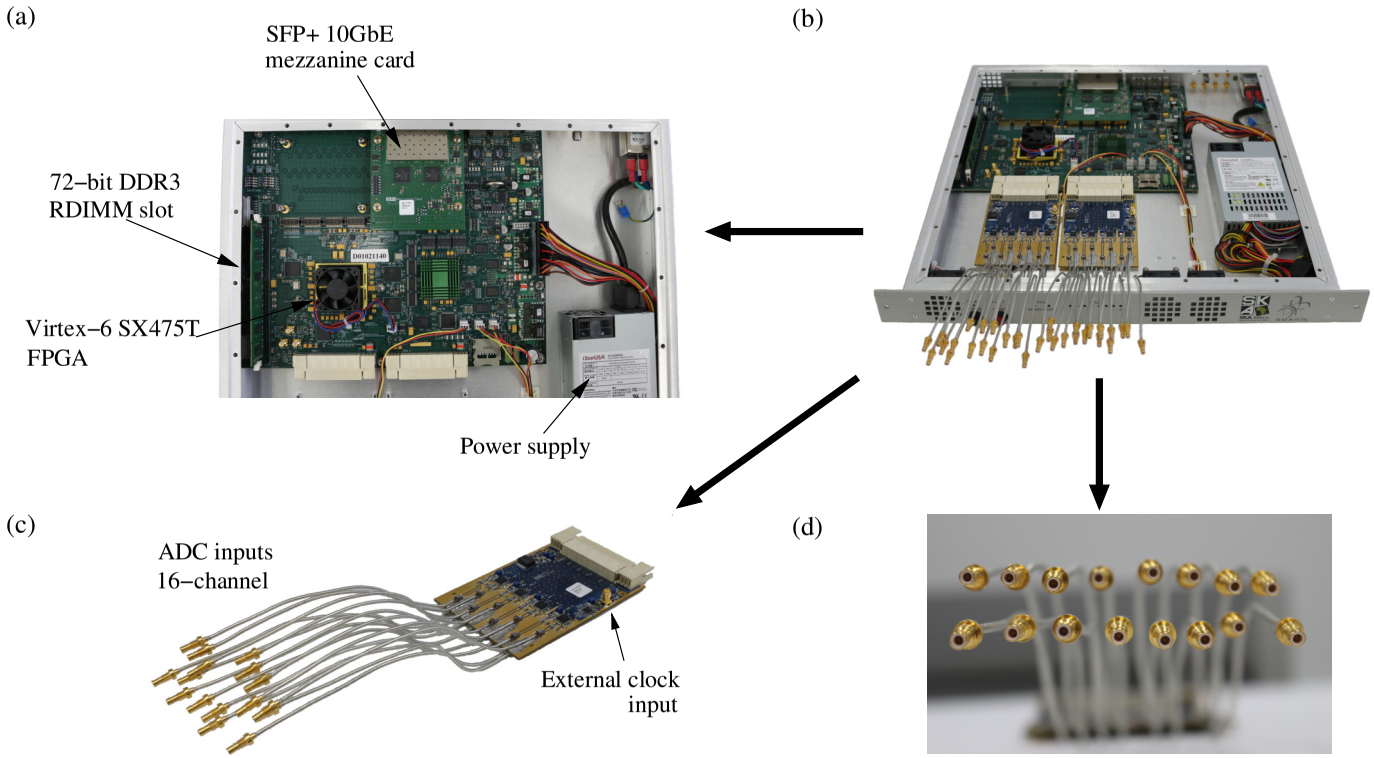

Figure 2.12: The ROACH-2 hardware platform with Xilinx Virtex-6 SX475T FPGA chip. (a) Top view of the ROACH-2 ver.2 motherboard, (b) ROACH-2 connected with two peripheral ADC cards and one SFP+ 10 GbE mezzanine card, (c) and (d) ADC card with 16-channel analog inputs.

and transient event detection. ROACH-2 [71, 72] is an open source FPGA platform designed in Cape Town, South Africa, together with CASPER collaborators as a part of the Square Kilometer Array (SKA) radio telescope project [77, 78]. The core processing module of ROACH-2 is a Xilinx Virtex-6 SX475T FPGA (XC6VSX475T-1FFG1759C) chip, equipped with on board inter-FPGA links interfaced and 10Gb ethernet interfaces using SFP+ mezzanine cards for all cross-FPGA communications. Key peripherals of a ROACH-2 consists of two multi-gigabit transceiver card slots supporting 4x10Ge links (SFP+), four 72Mb QDR II+ SRAMs and a 72-bit DDR3 RDIMM slot connected to the FPGA along with two ZDok+ interfaces supporting high speed DAC/ADC. A wide range of ADC boards are available to be interfaced with ROACH-2 with 1, 4, 8 and 16 ADC [79, 80] per board with maximum sampling rates up to 240, 480 and 960 MHz per output.

The clocking of the FPGA can be done by several methods. The internal system clock is used for designs that do not have any dependency with external clocked systems. However, when ADC cards are used in a design, it is important to clock the FPGA and the ADC boards using an external clock source to ensure synchronized operations. Fig. 2.12 shows the main components of a ROACH-2 motherboard and peripheral devices that can be integrated onto the platform when implementing experimental RF beamformers. Note the connectivity of inputs of 16-channel ADC cards (see Fig. 2.12(c)) are at the front side, the FPGA chip with cooling and the mezzanine cards are at the back-end of the housing.

The digital system design modeling method of ROACH is integrated with a widely used computational software package, Matlab. This gives access to the large community of DSP engineers who develop systems for many fields. Moreover, ROACH has its own Matlab Simulink modeling libraries with built-in modules to support a variety of functions such as polyphase structures, memory and more customized functions to ease the DSP designs. During the scope of research related to this thesis, we will be taking advantage of few modules in *MSSGE Toolflow [81]* to design IIR beamformers, as will be explained in detail in the upcoming chapters.

CHAPTER III

WIDEBAND 2-D IIR BEAM FILTER ON ROACH-2 FPGA PLATFORM

This chapter describes the digital realization of a 2-D IIR frequency planar beam filter in the ROACH-2 FPGA platform that can operate at 200 MHz. The technical specifications and configuration of integrating ADC cards and multi-gibabit networking interfaces to the digital design is discussed. Here, we propose a systolic array based approach for the 2-D IIR filter. Moreover, how ROACH-2 can be used to build integrated RF beamformers is also highlighted.

In [43], it has been shown that for a given selectivity, a network resonant IIR digital beam filter [82, 83] has significantly lower computational (multiplier) complexity compared with equivalent 2-D FIR beamformers. In certain cases, the 2-D IIR beam filter has about 90% lower multiplier count [22] compared to FIR beamformers having similar levels of performance in terms of directional selectivity and side-lobe level. The 2-D IIR frequency-planar beam filter may be suitable for applications such as communications and radio astronomy signal processing within VHF/UHF frequencies of operation where the observations are conducted using electronically steerable aperture array realizations. Towards this goal, the efficient and real-time implementation of 2-D IIR spatio-temporal beam filters for antenna array signal processing is an important engineering problem.

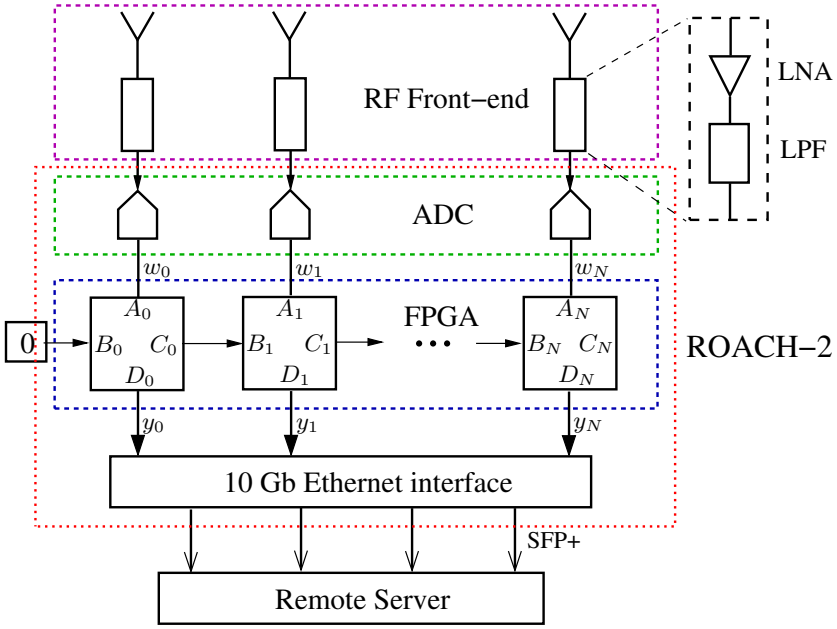

Figure 3.1: Proposed system architecture of the 32-element 2-D IIR beam filter in ROACH-2 hardware platform.

This research is the first stepping stone that leads to a final build of a steerable antenna array beamformer operating up to 200 MHz using the ROACH-2 FPGA platform that can provide the beamformed data in real-time.

3.1 System Architecture

An overview of the ROACH-2 based topology is shown in Fig. 3.1. Consider an RF plane wave $w(x, ct)$ which is received from the DOA ψ, sampled using a uniform linear array (ULA) with N wideband antenna elements, where $x = 0, 1, 2, ..., N$-1 is the spatial index and ct is the time normalized by speed of electromagnetic waves $c \approx 3 \times 10^8\ m/s$. The receiver RF front-end consists of an array of N antenna elements, each of them matched to a broadband low-noise amplifier (LNA), secondary

gain amplifiers and an anti-aliasing low-pass filter prior to being fed to an ADC in ROACH-2. The digitized array signal $w\left(n_x, n_{ct}\right)$ is used to process received signals in the ROACH-2 FPGA to selectively enhance signals from DOA ψ. Beamformer output can then be sent to a remote location through eight 10GbE links for further processing or storage. The proposed architecture uses 10Gb Ethernet cores to capture data output from parallel processing core modules(PPCM)and transmitted to a server though SFP+ interfaces for recording or further processing. The maximum data output rate for the architecture is about 80Gbps. Our goal is to build a complete and fabricated device with RF front-ends and high-speed networking interface that can be connected to 64-bit Linux server or digital signal processor having back-end software-defined radio applications. However, this research is primarily on design approach along with a detailed architecture and preliminary results of the 2-D IIR digital beam filter.

3.1.1 Differential Form 2-D IIR Digital Beam Filters

We use the 2-D digital beam filter described in section 2.3.1 for the systolic array in this study. However, by rearranging (2.17) we can deduce the transfer function to a more computationally efficient and low in hardware utilization model known as the differential form version. The differential-form **z-**domain transfer function of the beam filter $H(z_1, z_2)$ [43] is,

$$H(z_1, z_2) = \frac{1}{1 - \alpha_1 \frac{z_1^{-1}}{1+z_1^{-1}} - \alpha_2 \frac{z_2^{-1}}{1+z_2^{-1}}} = \frac{Y(z_1, z_2)}{W(z_1, z_2)} \tag{3.1}$$

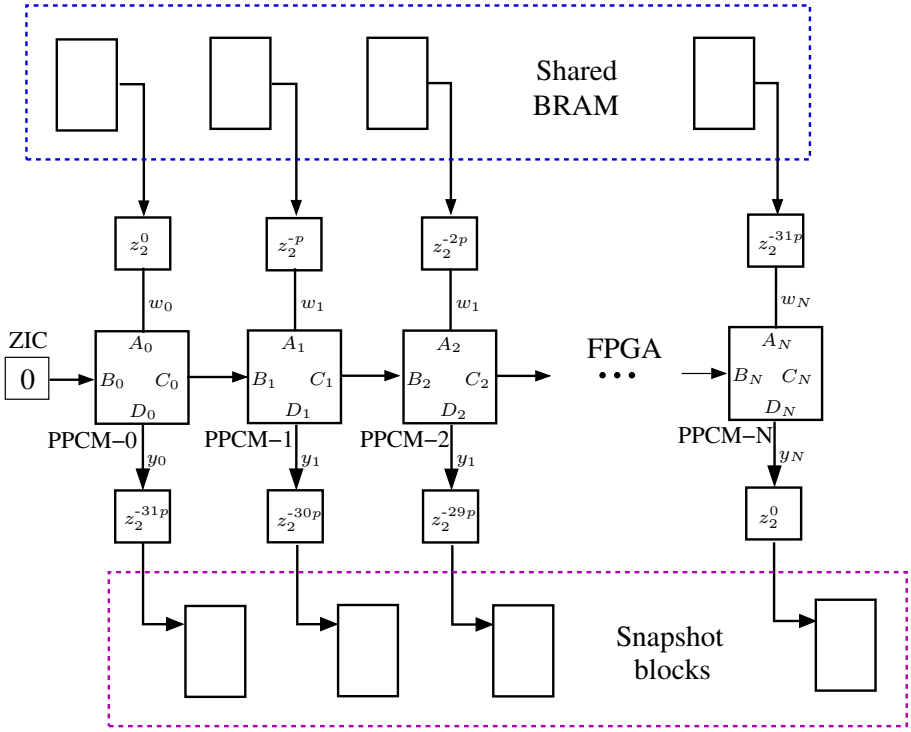

Figure 3.2: The simulated architecture of the systolic array based 2-D IIR beam filter on ROACH-2 hardware platform.

where the coefficients $\alpha_{1,2}$ are calculated for $0 \leq \theta \leq 45°$ by,

$$\alpha_1 = \frac{2\cos\theta}{R + \cos\theta + \sin\theta} \tag{3.2}$$

$$\alpha_2 = \frac{2\sin\theta}{R + \cos\theta + \sin\theta} \tag{3.3}$$

The selectivity parameter $R > 0$ and $\theta = \tan^{-1}(\sin\psi)$.

3.1.2 High-speed Low-complexity Architecture

$H(z_1, z_2)$ is implemented here as a low-complexity high-speed systolic array [84]. Fig. 3.2 shows the systolic-array architecture which consists of a pipelined mesh interconnection of identical PPCMs [84]. Shared BRAM and snapshot block groups

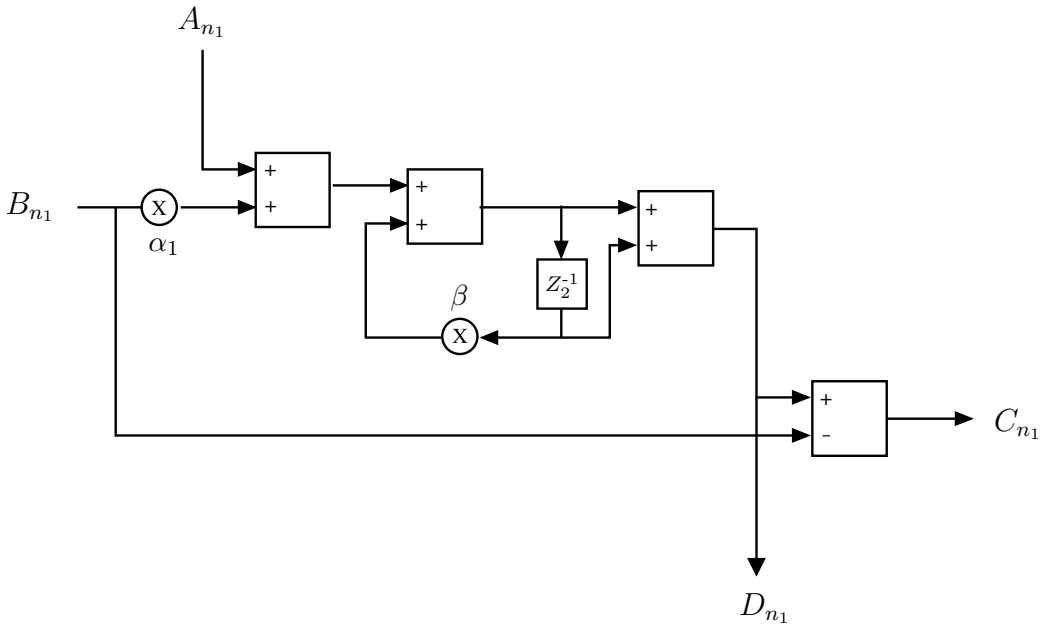

Figure 3.3: Digital logic design of an IIR beam filter block (PPCM module) of the systolic array.

are used to feed in sampled signals and store beamformed outputs. The delay elements placed at the input and output of the PPCM blocks helps to get synchronized beamformed outputs. A PPCM is designed using the differential-form by rewriting as,

$$Y(z_1, z_2) = \frac{W(z_1, z_2) + \alpha_1 \frac{z_1^{-1}}{1+z_1^{-1}} Y(z_1, z_2)}{1 - \beta z_2^{-1}} (1 + z_2^{-1}) \tag{3.4}$$

where $\beta = \alpha_2 - 1$. The proposed PPCM [Fig. 3.3] has *two parallel multipliers and four parallel adders/subtractors* having a 33% lower chip area than the direct form which requires three multipliers and six adders/subtractors per PPCM [21]. The key advantage of our proposed architecture is the very high real-time computational throughput of one complete array-frame per clock cycle (OFPCC). The mixed-domain representation of the transfer function implemented in a PPCM block is represented

as,

$$Y(n_1, z_2) = \frac{W(n_1, z_2) + \alpha_1 Y'(n_1, z_2)}{1 - \beta z_2^{-1}}(1 + z_2^{-1}) \tag{3.5}$$

where $(n_1, z_2) \in (\mathbb{Z}, \mathbb{C})$, and

$$Y'(n_1, z_2) = Y((n_1 - 1), z_2) - Y'((n_1 - 1), z_2) \tag{3.6}$$

3.1.3 ROACH-2 Realization Technique

Our 2-D IIR beam filter $H(z_1, z_2)$ will be implemented as a high-speed low complexity systolic array architecture within the Virtex-6 SX475T FPGA on the ROACH-2. The systolic array digital computation unit consists of a pipelined mesh interconnection of identical PPCMs. The systolic array is capable of producing N outputs in one clock period. The processor clock frequency is equal to the ADC sampling frequency at RF. For example, a typical FPGA clock frequency of 200 MHz, the processor produces 200 million linear output frames per second, in real-time. The high performance Xilinx Virtex-6 SX475T FPGA chip in ROACH-2 is capable of implementing the low-complexity electronically steerable 2-D IIR beam filter at RF so that it is producing beamformed output streams in real-time. The beamformed outputs can be transmitted to a remote server at 10-40 Gbps for further processing or storage.

3.1.4 System Overview

The current study is focused on a systolic array of 32 antenna elements ($N = 32$). In the proposed architecture the output of RF front-end is directly connected to the ADC boards in ROACH-2. By using two 16-input ADC boards we can directly feed

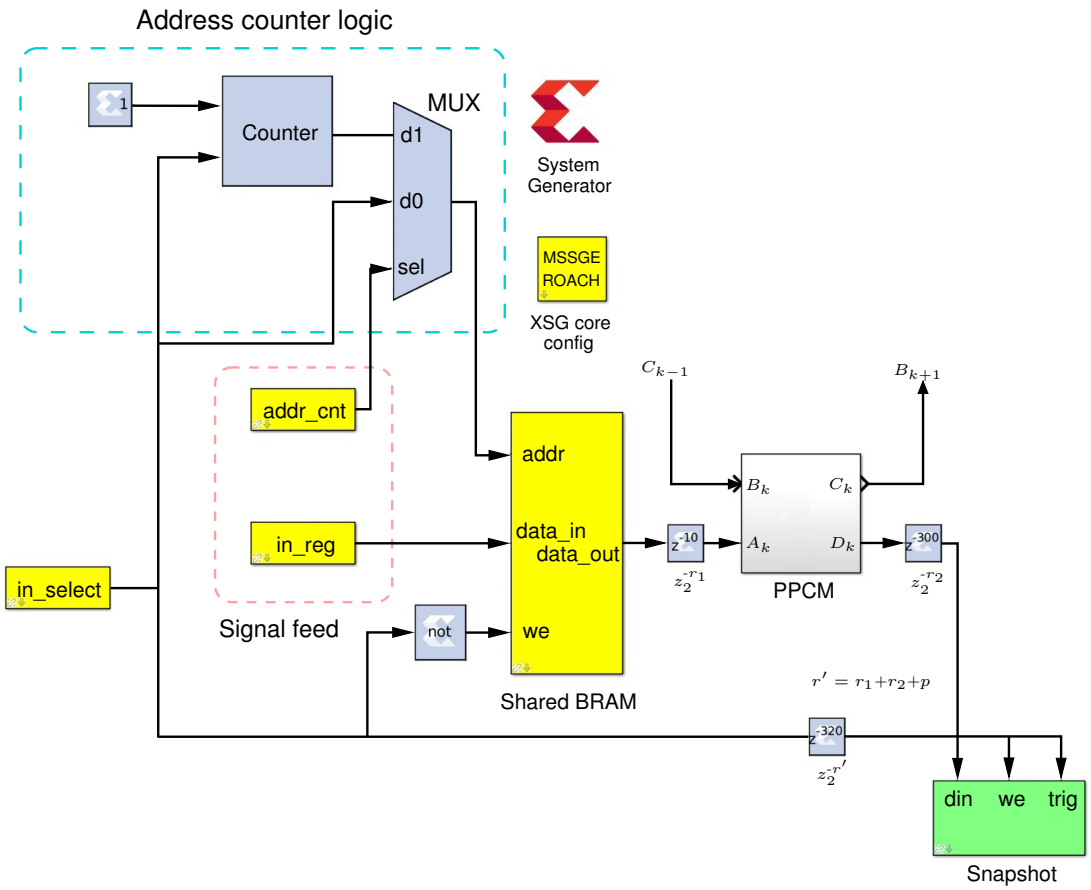

Figure 3.4: Operational model in Simulink to feed in and collect data from the ROACH-2 based systolic array.

32 digitized signals into the DPP systolic array. During this study we generated the input signals using computational software and stored them in shared memory blocks (shared BRAM) [Fig. 3.2]. However, in the proposed architecture the input signals will be generated by the ADC cards. The ROACH-2 ADC block for Simulink can be used to easily feed input signal vectors into the systolic array. The operational logic of the simulated model is shown in Fig. 3.4 for one PPCM. The *Address counter logic* is commonly shared with all PPCMs. A multiplexer is used to select the input method

to the *addr* input of the shared BRAM. Initially, the value of *in_select* is set to zero to write data into shared BRAMs. Input vectors stored in matrices are written to shared BRAM using a python script incrementing the address value. This procedure is necessary to ensure that all samples are fed correctly without any loss or delays to the DPP. Then, *in_select* is set to 1 to start the counter to trigger 'read enable' of the shared BRAMs and write enable of snapshot blocks. The digitized signals $w\left(n_x, n_{ct}\right)$ are then fed synchronously to the ROACH-2 beam filter at the designated clock rate, $F_{CLK} = F_S = F_{sys\text{-}clk}$ by reading data from memory blocks using an incremental counter.

Each of the signals fed to a PPCM pass through a delay element to match the propagation delay of the secondary input of the subsequent PPCM where $z_2^{np}, n = 0, 1, ..., N$ and p is the propagation delay though a PPCM. The differential form beam filter implemented in the PPCM will consist of two inputs A_n, B_n and will generate two outputs C_n, D_n as shown in Fig. 3.3. The secondary input B_0 of the first PPCM is fed with an infinite sequence of zeros to initialize the PPCM with zero input conditions (ZIC). The secondary inputs B_n of the subsequent PPCMs are fed with the secondary out $C_{n\text{-}1}$ of the preceding PPCM. The primary outputs D_n of the PPCMs are further delayed by $(N - n)p, n = 1, 2, ..., N$ clock cycles to get synchronized outputs. The snapshot block in MSSGE Toolflow is generally used to capture data over short durations. Therefore, by using snapshots in the design it is possible to demonstrate real-time signal processing capability of this design. Hence, the outputs are directed to a group of snapshots. Each PPCM is connected to a

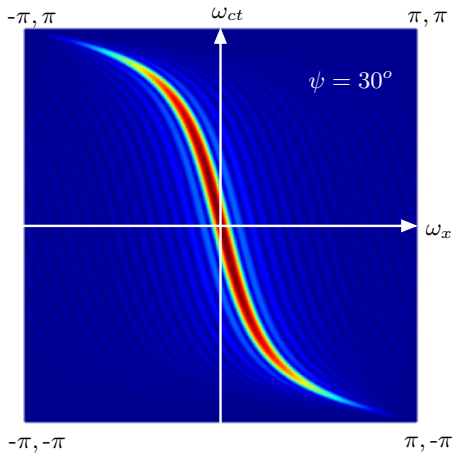

Figure 3.5: Frequency response of 2-D IIR frequency planar beam filter tuned at a DOA of $\psi = 30°$.

snapshot block with a considerable number of time samples to capture data from the PPCM output.

3.2 Simulation and Results

The input signal is fed to the DPP with 32 PPCMs. The propagation delay of a signal through a PPCM was set to 9 clock cycles while adjusting the external delays at input and output to multiples of 9 clock cycles to maintain synchronized outputs.The filter is tuned to enhance signals received at a DOA of $\psi_2 = 30°$ as its frequency response in Fig. 3.5. The array factor of the filter is illustrated in Fig. 3.6 clearly indicating the main beam of the filter tuned to an angle of 30°.

Simulation results were obtained to demonstrate filter performance using three input signals with DOAs $\psi_1 = 10°$, $\psi_2 = 30°$ and $\psi_3 = 70°$ with a sampling frequency of $F_s = 200$ MHz where 2-D frequency spectrum of the input signal is

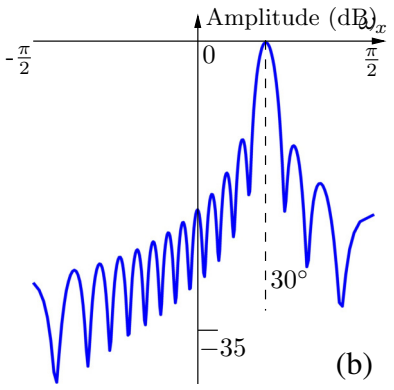

Figure 3.6: The array factor of 2-D IIR frequency planar beam filter indicating directional enhancement properties at $\psi = 30°$.

shown in Fig. 3.7(a). Fig. 3.7(b) shows the filter output which consists of the desired signal while suppressing the undesired signals. The time domain responses of the filter input and output signals are depicted in Fig. 3.7(d) and Fig. 3.7(e), respectively. We can clearly observe that the undesired signals are attenuated by 16 dB.

3.2.1 FPGA Implementation Results of The Proposed Architecture

The system architecture described above was physically realized on the ROACH-2, FPGA based rapid prototyping system for two separate inputs wordlengths and tested using on-chip hardware-in-the-loop co-simulation. The initial designs of digital realizations were done within MATLAB environment using Matlab/Simulink/System Generator/EDK (MSSGE) toolflow [81] for Casper ROACH-2. Xilinx Virtex-6 SX475T FPGA (XC6VSX475T-1FFG1759C) chip was employed to physically realize the architectures on FPGA with fine-grain pipelining for increased throughput. The realizations were verified on ROACH-2 chip using using its SX475T chip at a clock

Table 3.1: Comparison of VLSI FPGA resource consumption for 32 element differential form 2-D IIR beam filter at 18-bit and 12-bit inputs.

Resources	**18-bits**	**12-bits**
Slice registers	4,014	2,676
Slice LUTs	5,746	3,832
Occupied slices	1,767	1,121
LUT-FF pairs	6,016	4,069
T_{cpd} (ns)	5.6	5.0
Max. frequency (MHz)	178.57	200

frequency of 200 MHz. Input precision level was varied while maintaining the values normalized between -2 and +2 to compare the performance in terms of digital logic resource consumption at varied degrees of numerical accuracy and dynamic range. The hardware co-simulation was carried out at wordlengths 18 and 12 while applying 1024 random 32-point input test vectors. Test vectors were generated from within the

Table 3.2: ASIC synthesis results for AMS, 180nm CMOS for 32 element differential form 2-D IIR beam filter at 18-bit and 12-bit inputs.

Wordlength	Area (mm^2)	AT	T_{cpd} (ns)	F_{max} (MHz)	Gate Count	D_p (mW/MHz)
18-bits	13.813	27.364	1.981	504.80	230,447	10.778
12-bits	8.922	13.767	1.543	648.09	141,760	6.446

MATLAB environment and routed to the physical FPGA device using JTAG based hardware co-simulation. Then measured data from the FPGA was routed back to MATLAB memory space.

Evaluation of hardware complexity and real-time performance considered the following metrics: the number of used configurable logic blocks (CLB), flip-flop (FF) count, critical path delay (T_{cpd}), and the maximum operating frequency (F_{max}) in MHz. The `xflow.results` report file was accessed to obtain the above results. Dynamic (D_p) and static power (Q_p) consumptions were estimated using the Xilinx XPower Analyzer for the Xilinx Virtex-6 XC6VSX475T-1FFG1759C FPGA device and the results are shown in Table 3.1.

The Application Specific Integrated Circuit (ASIC) synthesis results [85, 86] obtained using Austria Micro Systems (AMS) libraries shown in Table 3.2 yield that the system can be implemented in a $13mm^2$ chip and can operate at frequencies above 500MHz.

3.3 Conclusion

A systolic-array architecture for 2-D IIR frequency-planar beam filters is highly efficient in realization in comparison with the corresponding FFT based FIR beam filter. It has relatively high gain, and reduced need for hardware resources while maintaining equivalent filter performance. From the results obtained from our research it is evident that ROACH-2 is an ideal platform to build integrated 2-D IIR beam filters for a variety of applications in different fields. Thus, the

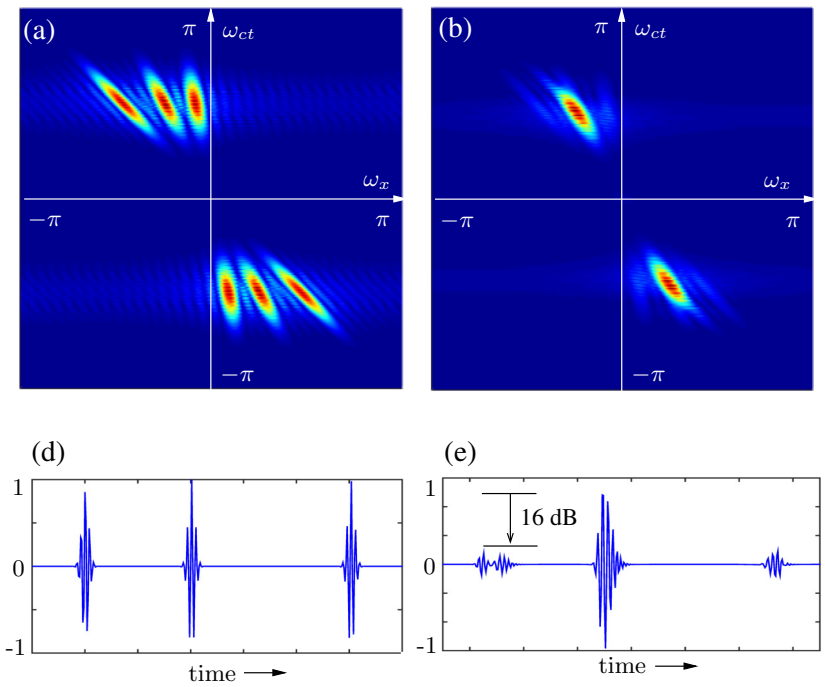

Figure 3.7: Directional enhancement simulation of the 2-D IIR beam filter using 3 Gaussian modulated pulses in frequency domain and time domain. (a) Wideband input signals with DOAs $(10°, 30°, 70°)$, (b) Filtered output signal with DOA $\psi = 30°$, (c) input signals in time and, (d) enhanced signal in time domain.

simulation results obtained show a promising future to build efficient beam filters operating at high speeds; the simulations carried out show significant attenuation of the undesired signals. The ROACH-2 testbed provides a sophisticated hardware platform to implement the complete end-to-end system and generate processed signals to do real-time analysis. We believe that modern day Ultra-Wideband (UWB) applications show promising potential to use such filters in high-speed digital wireless communications, imaging, radar and radio astronomy.

However, one key limitation of this ROACH-2 based design is the limited maximum operating frequency of 240 MHz when combined with the 16 input ADC

cards [79]. The next chapter describes a method that can be used to overcome the limitations in operating frequency by introducing polyphase structures to the design as a future extension of this concept. Moreover, in the later stages of this study will focus on fabricating the 32 element antenna/array RF front-end and build a complete system that will process RF signals at a designated DOA. This will be followed by extending this concept to design a 3-D IIR beam filter that can be implemented in an interconnected series of ROACH-2 hardware platforms.

CHAPTER IV

POLYPHASE 2-D IIR BEAM FILTERS FOR DIGITAL RF APERTURES ON ROACH-2

This chapter introduces a method to increase the operating frequency of the ROACH-2 based 2-D IIR beam filter described in the previous chapter. A study on the potential of realizing 2-D IIR beam filters in the ROACH-2 FPGA platform at a ceiling frequency of 200 MHz is presented in [87]. Our goal is to build a multirate steerable beam filter (2-phases) using the ROACH-2 FPGA platform that can operate at higher frequencies by extending the research explained in chapter 3 to overcome the existing limitations. The internal fabric of the FPGA operates at half the throughput (frame-rate) of the antenna array using a multi-dimensional polyphase structure that parallel processes two time-interleaved data converter channels for each antenna's receiver.

Multirate signal processing [88] can be used for increasing the real-time computational throughput at the cost of circuit complexity via massive-parallelism [89]. The multirate methods proposed in [1, 89] have been realized for direct-form and differential-form signal flow graphs (SFG). By using this technique, it has been shown that the achievable sampling frequency F_s can be increased by a factor of M compared to the nominal clock rate F_{CLK} of the

digital hardware. This allows us to build high speed digital beamformers that can operate in the tens-of-GHz range, as required for emerging UWB applications in such fields as radio astronomy and wireless communications. The availability of polyphase clocking schemes in time-interleaved RF analog-to-digital converters operating at multi-GHz rates makes the proposed multirate 2-D IIR beam filter architectures inherently suitable for emerging digital-RF and digital-microwave systems that require throughput levels that are greater than typical clock domains supported by today's VLSI technology.

4.1 Polyphase Architecture (M-phase) for 2-D IIR Beam Filters

The differential form 2-D IIR frequency-planar beam filter described in chapter 3 in section 3.1.1 and 3.1.2 can be further organized by pipelining to achieve a mathematical model that can be implemented in FPGA hardware to operate at high frequencies. Here, the pipelining takes place in the temporal feedback-loop thus resulting in a lowered critical path delay (CPD).

The M-phase polyphase architecture [1] with LA optimization of the differential form 2-D IIR frequency-planar beam filter can be written in the form,

$$Y(n_1, z_2) = \frac{V_{n_1}(z_2)}{1 - \beta^M z_2^{-M}} \left(1 + \sum_{k=1}^{M-1} \gamma^k z_2^{-k} + \beta^{M-1} z_2^{-M} \right) \tag{4.1}$$

where V_{n_1} is given by,

$$V_{n_1} = W(n_1, z_2) + Y'(n_1, z_2) \tag{4.2}$$

and γ_k for $k = 1, 2, ..., M$ are numerator coefficients which can be algebraically defined in terms of β such that,

$$\gamma_k = \beta^{k-1}(1 + \beta) \tag{4.3}$$

for $k = 1, 2, ..., M - 1$ and the feedback coefficient is given by $\gamma_M = \beta^M$. Here, the LA optimization helps to overcoming limitations on CPD [90, 33]. The application of LA of order M to (3.5) leads to the increase in the number of unit delays from 1 to M inside the temporal feedback loop of (4.1). The availability of M number of First-in-first-out (FIFO) delays in the feedback loop corresponding to (4.1) naturally leads to a polyphase decomposition of (4.1).

The term $1 - \beta^M z_2^{-M}$ in the denominator of (4.1) is a feedback mechanism in order to derive the desired Mth-order polyphase decomposition [88]. The resulting mixed-domain difference equation is implemented by the digital architecture of M parallel polyphase components, each operating at clock frequency F_{CLK}, to yield a combined frame rate of $F_S = M.F_{CLK}$. This is a very important point; the approach allows an M-fold increase in throughput, that is, the frame rate is M-times more than the clock rate of the digital engine. For systems limited by Moore's Law, for high-enough number of phases (M), there can be substantial acceleration beyond the clock rate of the platform. This gain in throughput comes at a tremendous cost in complexity and power consumption. This is an unavoidable price paid for such high throughput levels that are multiples of the clock rate.

The circuit complexity will further increase as a result of LA optimization. Such increases are dominated by the multiplier complexity due to the use of fully

parallel multiplier circuits. For the two-phase case, the number of multipliers per PPCM increases to 10, 12, and 12 for LA optimization of orders 1, 2 and 3, leading to reduced (best case) CPDs of $T_{CPD,No-LA}/2$, $T_{CPD,No-LA}/3$ and $T_{CPD,No-LA}/4$ where $T_{CPD,No-LA}$ is the best-case CPD that is achievable by pipelining the feed-forward sections of the SFG [90]. The third-order LA can be obtained (for infinite precision arithmetic) using the following algebraic equation [1],

$$\overbrace{\frac{1}{1-\beta z_2^{-1}}}^{No-LA} = \overbrace{\frac{1+\beta z_2^{-1}}{1-\beta^2 z_2^{-2}}}^{1st\ order\ LA} = \overbrace{\frac{(1+\beta z_2^{-1})(1+\beta^2 z_2^{-2})}{1-\beta^4 z_2^{-4}}}^{3rd\ order\ LA} \tag{4.4}$$

4.2 System Architecture

We used a two-phase architecture using (4.1) with 1st order LA optimization (4.4). The resulting hybrid differential-form input-output mixed-domain relation [1] is given by,

$$Y(n_1, z_2) = \frac{W(n_1, z_2) + \alpha_1 Y'(n_1, z_2)}{1-\beta^2 z_2^{-2}} \left(1 + \underbrace{(1+\beta)}_{\gamma_1} z_2^{-1} + \beta z_2^{-2}\right) \tag{4.5}$$

where $\gamma = (\beta + 1)$. Fig. 4.2 shows the two phase PPCM architecture rearranged using the polyphase Noble identities that can be implemented in an FPGA. The 2-phase 2-D IIR beam filter is implemented as a high-speed low complexity systolic array architecture within the Virtex-6 SX475T FPGA. Fig. 4.1 shows the systolic array architecture integrated with CASPER blockset [81] in Xilinx System Generator, which was used to realize the digital system inside ROACH-2 platform. The simulations pertinent to this research were carried out for a systolic array of 32 antennas ($N = 32$) in the array. Input signals were generated using computational

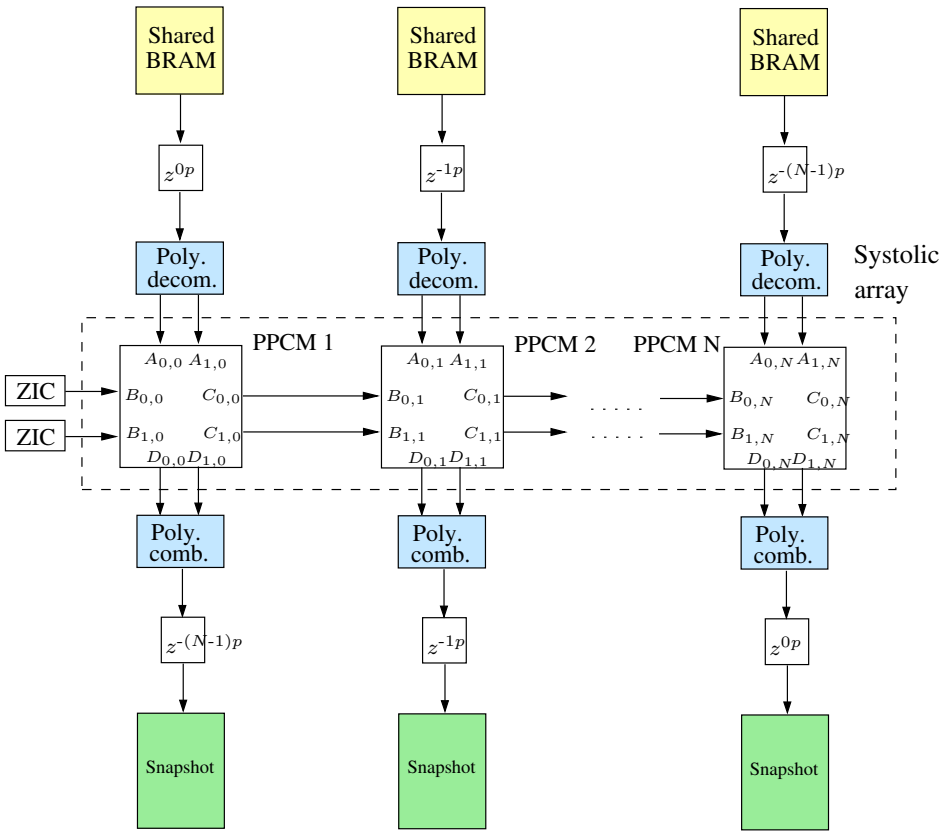

Figure 4.1: Two phase systolic array architecture of the 2-D IIR beam filter with intergration of polyphase decimators/interpolators and ROACH-2 hardware platform support.

software and stored in shared memory blocks (shared BRAM) [see Fig. 4.1] located in the ROACH-2's FPGA prior to feeding signals into the systolic array. The stored data are sent to the polyphase decomposition block to generate data streams that were fed into the 2-phase PPCM block [Fig. 4.2]. The output of the PPCM block will also produce two data stream which will be recombined in the polyphase combine block. The type of memory block used to collect the data from the combined outputs is called *snapshots*, which is built using shared BRAM. The each delay element connected to the shared BRAM and snapshot block is used to adjust propagation delay within

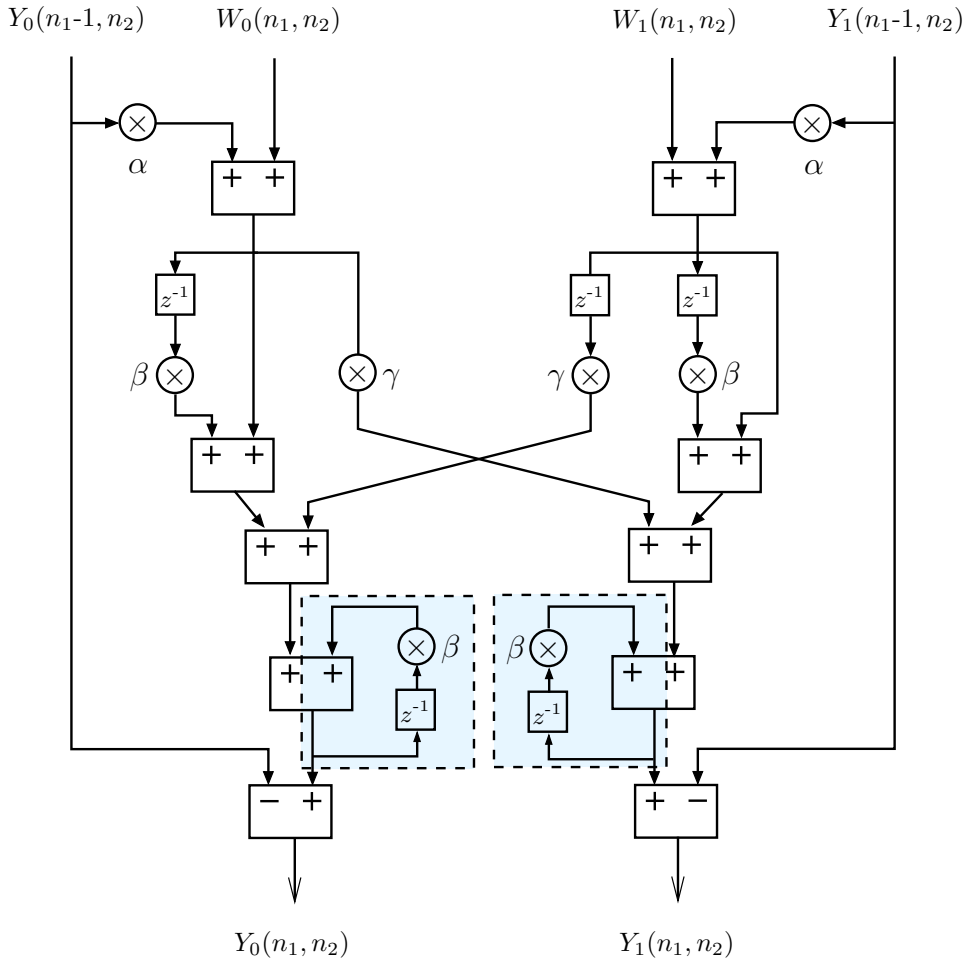

Figure 4.2: The time-interleaved polyphase PPCM digital design using a non overlapping clock.

the systolic array. The requirement in this study is to capture data only for a short duration of time to demonstrate real-time signal processing. Each PPCM is mapped to a snapshot block with a considerable number of time samples ($2^{12} = 4096$) to capture output data from each of the 32 PPCMs in the array processor.

Each of the signals fed to the corresponding PPCM passes through a clocked delay element (parallel D flops) to match the pipeline latency of the secondary input of

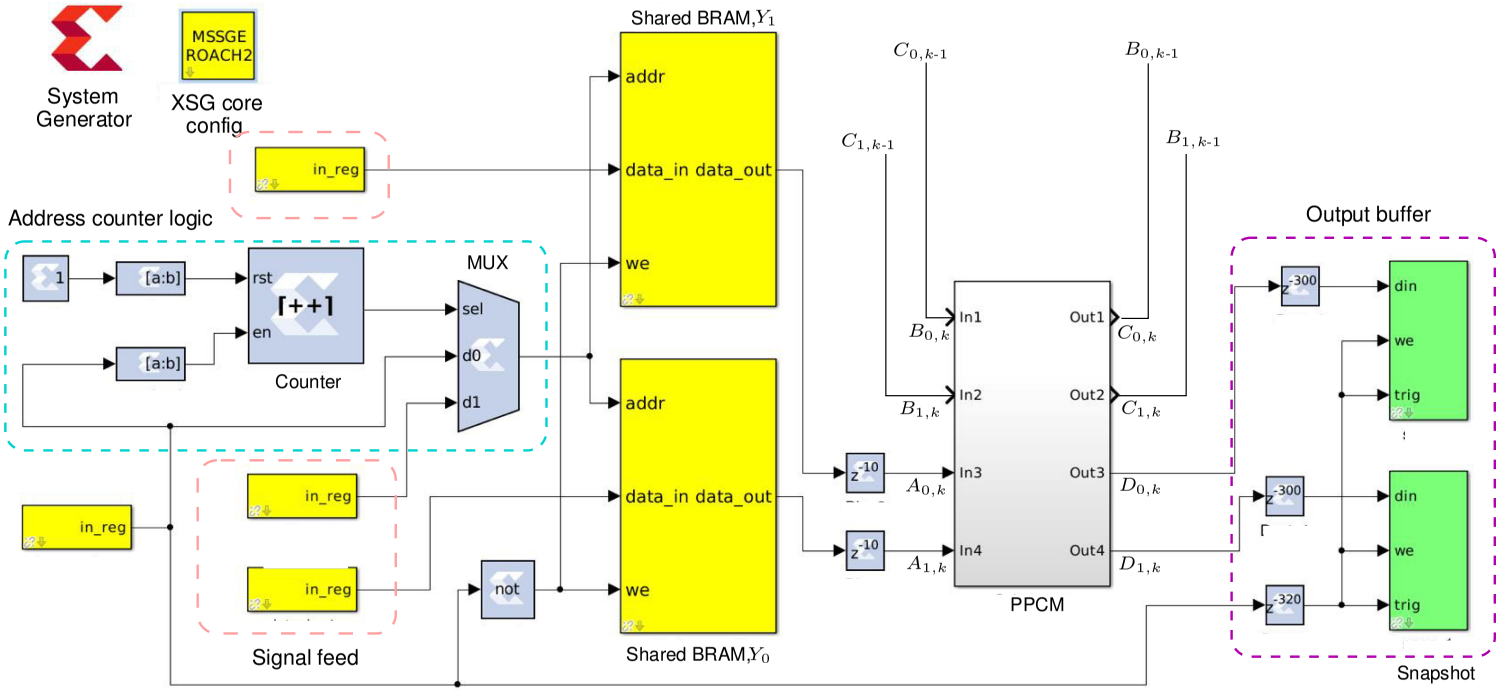

Figure 4.3: Data feed in and collection mechanism of the operational model in simulink of the ROACH-2 based systolic array.

the subsequent PPCM where $z_2^{np}, n = 0, 1, ..., N$ and p is the pipeline latency through a PPCM. The 2-phase differential form beam filter implemented in the PPCM will consist of four inputs A_0, A_1, B_0, B_1 and will generate four outputs C_0, C_1, D_0, D_1 as shown in Fig. 4.1. The first pair of secondary input B_0, B_1 is initialized with ZIC. The secondary inputs B_0, B_1 of the subsequent PPCMs are fed with the secondary output $C_{0,\text{-}1}, C_{1,\text{-}1}$ of the preceding PPCM. The combined data stream of the primary outputs D_0, D_1 are further delayed by $(N - n)p, n = 1, 2, ..., N$ clock cycles to achieve synchronized outputs.

The operational logic of a PPCM in ROACH-2 without polyphase decomposition/recombination is shown in Fig. 4.3. The *Address counter logic* is commonly shared with all PPCMs. A multiplexer is used to select the input method to the *addr* input of the shared BRAM. Initially, the value of *in_select* is set to zero to write data into shared BRAMs. Input vectors stored in matrices are written to shared BRAM using a python script incrementing the address value. This procedure is necessary to ensure that all samples are fed correctly without any loss or delays to the systolic array. Then, *in_select* is set to 1 to start the counter to trigger 'read enable' of the shared BRAMs and write enable of snapshot blocks. The digitized signals $w\left(n_x, n_{ct}\right)$ are then fed synchronously to the the ROACH-2 beam filter at the designated clock rate, $F_{CLK} = F_S = F_{sys\text{-}clk}$ by reading data from memory blocks using an incremental counter.

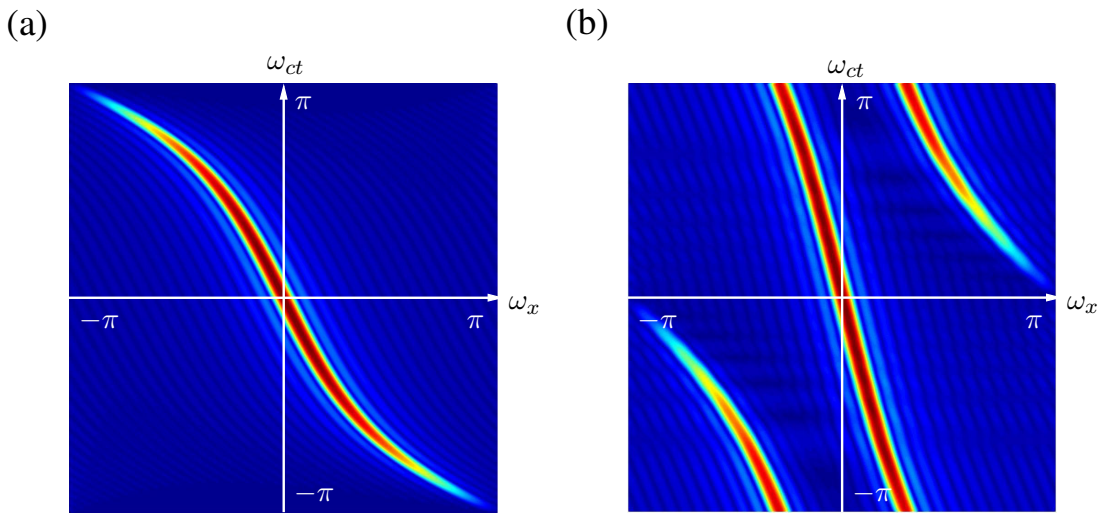

Figure 4.4: The frequency response of 2-phase 2-D IIR beam filter tuned to enhance RF signals arriving at a DOA of $\psi = 40°$. (a) Response after interpolating the beamformed output of two phases and, (b) Decomposed polyphase response of one phase illustrating the temporal domain aliasing affect.

4.3 Simulation and Results

4.3.1 Beam Specifications

The design was simulated in ROACH-2 hardware platform and compared with the results obtained from Matlab simulations. The beam directional- selectivity parameter was fixed at $R = 0.005$ for all the simulations. The number of input signals fed from the ADC's were limited to 32 to ensure a practical scenario. The pipeline latency through a PPCM was set to 10 clock cycles while adjusting the externals delays appropriately to maintain synchronized outputs. The frequency domain response [Fig. 4.4(a)] of the 2-phase 2-D IIR planar wave filter implemented on ROACH-2 was graphically determined from the output vectors generated by the snapshot blocks. The output response was constructed by computing the 2-D discrete

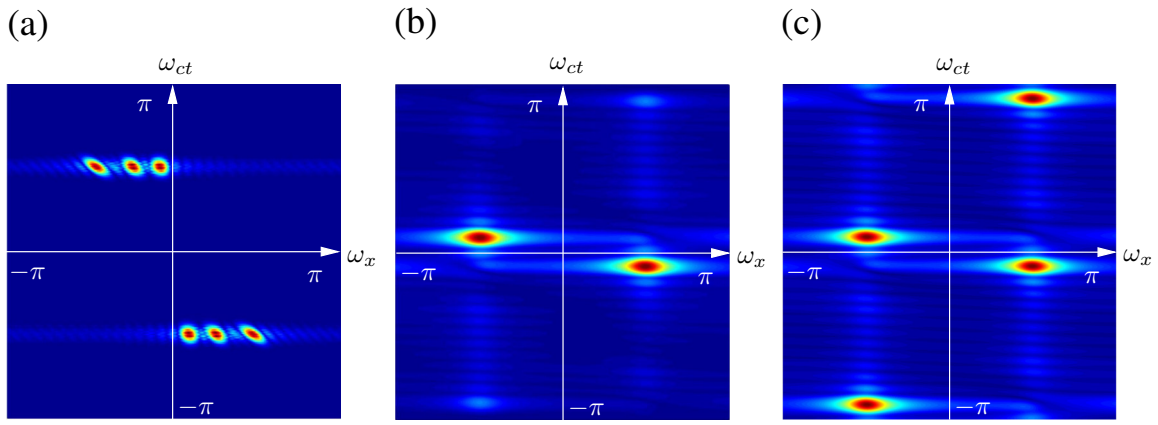

Figure 4.5: Directional enhancement simulation of the 2-phase polyphased 2-D IIR beam filter using 3 Gaussian modulated pulses in frequency domain and time domain. (a) Wideband input signals with DOAs $(10°, 40°, 70°)$, (b) Interpolated filtered output signal with directional enhancement, (c) Decomposed output of the filtered signal of one polyphase.

Fourier transform of the unit impulse response, which in turn, was measured from the ROACH-2 board. The input vectors corresponding to a unit impulse was fed into the shared BRAM blocks and the beam filter was tuned to filter out signals received from a DOA of $\phi = 40°$. All registers were assigned with a wordlength of 32 bits and binary point at 16 bits. The frequency response of a decomposed phase is shown in Fig. 4.4(b). The fixed point precision can be reduced to increase throughput (clock speed), reduce power consumption albeit at the cost of an increase in quantization noise within the architecture.

4.3.2 Model for Wideband Interference

The beam filter is electronically steered to enhance wideband RF plane-waves received at a DOA of $\psi_2 = 40°$. The necessary 2-D spatio-temporal frequency response is

Table 4.1: Comparison of FPGA hardware resource consumption for 32 element differential form polyphased 2-D IIR beam filter at 16-bit and 32-bit inputs.

Resources	**16-bits**	**32-bits**
Slice registers	6,646	13,740
Slice LUTs	16,740	36,432
Occupied slices	4,916	10,368
LUT-FF pairs	8,370	9,119
T_{cpd} (ns)	2.119	2.242
Max. frequency (MHz)	471.92	446.03

shown in Fig. 4.4(a). An input signal Fig. 4.5(a) comprised of three sinusoidal signals, a desired signal ($\psi_2 = 40°$) and two undesired signals with DOAs $\psi_1 = 10°$, $\psi_3 = 70°$, were fed into the beam filter to verify the performance of the filter. The beam filter successfully filtered out the desired signal [Fig. 4.5(b)] while directionally suppressing the undesired signals. The decomposed output in frequency domain of the filtered signal which has a DOA of $\psi_2 = 40°$ is illustrated in Fig. 4.5(c).

4.3.3 Polyphase Sampling using ROACH-2

To demonstrate the polyphase decomposition and high speed RF sampling capabilities using ROACH-2 platform, an input signal generated using a RF signal generator [Fig. 4.6(a)] with a frequency of 100 MHz was fed into a single channel the ROACH-2 32-channel ADC (two cards) [79] with a sampling clock rate of 240 MHz. The demux

setting on the ADC was set, such that the input signal is sampled at the highest achievable sampling frequency of 960 Msamples/s. In Fig. 4.6(b) we show how the sampled signal has been observed for 40 samples. At the highest demux setting, ADC chip [3] of the multi channel ADC cards supports 12 quantization levels. The highly quantized nature of the input waveform can thus be observed in the sampled signals as depicted in the Fig. 4.6(b).

The sampled signal (for a single element) was decomposed into a polyphase signal consisting of 4-phases, where each phase is represented by a polyphase non-overlapping clock. Internal to the FPGA, each phase drives a synchronous digital FPGA architecture driven by a single-phase clock operating at 240 MHz. The polyphase clocks exist within the ADC architecture, while the FPGA architecture is single phase. The FPGA clock is derived from the ADC clock input, which in turn, is derived from a reference oscillator synchronized to a 10 MHz frequency standard. Each signal [Fig. 4.6(c)] from the 4 phases inside the ADC chip is identical to a signal that was sampled at the rate of $960/M$=240 Msamples/second of the input waveform. That is, the external clock rate of the ADC board. The input signal [Fig. 4.6(d)] can be correctly recovered using the 4-phase time-interleaved sampling method.

The eventual realization of the aperture array will support 32 elements at frame rate 240 MHz, 16 elements at frame rate of 480 MHz, or 8 elements at frame rate 960 MHz, respectively. If the beamforming application requires in-phase and quadrature components for each channel, the number of supported elements will be reduced by 50%.

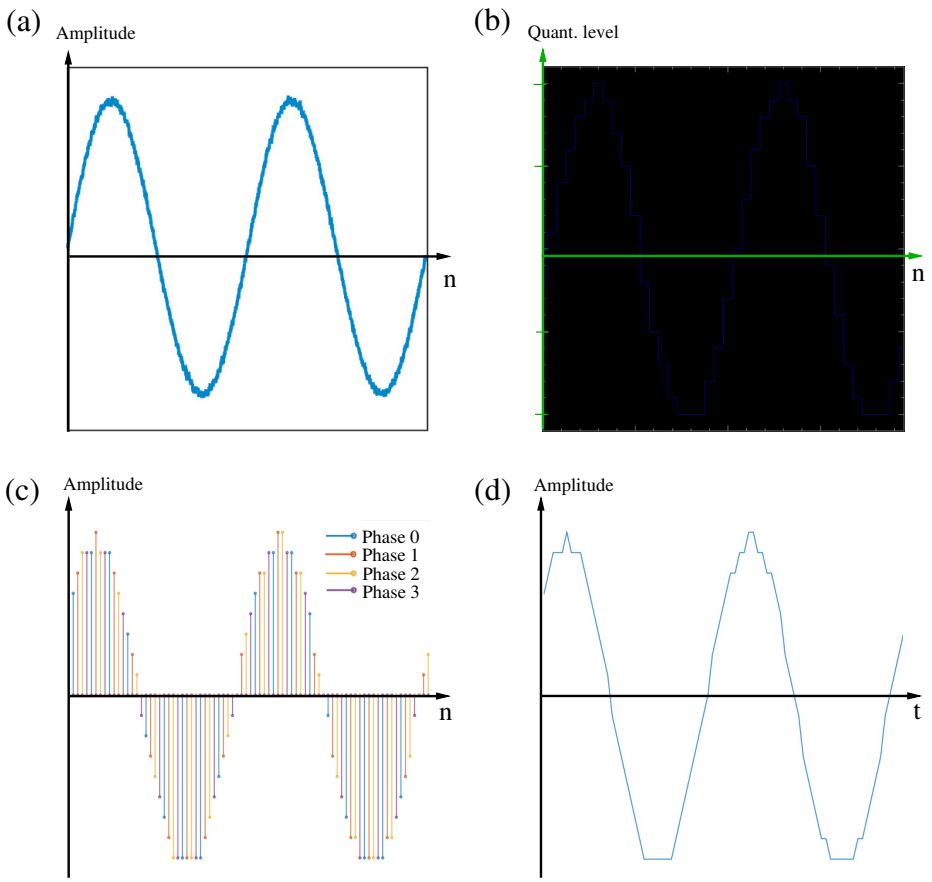

Figure 4.6: Sampling signals with ROACH-2 16-channel ADC [3] at clock rate 960 MHz with demux setting of 4. (a) True input signal fed into the 16-channel ADC, (b) Captured sampled signal at a sampling rate of 960 Msamples/s, (c) Decomposed 4 polyphase samples and (d) Interpolated output signal of all 4 polyphases.

4.3.4 FPGA Implementation

Table 4.1 shows the evaluation of hardware complexity and real-time performance considered the following metrics: the number of used configurable logic blocks (CLB), flip-flop (FF) count, critical path delay (T_{cpd}), and the maximum operating frequency (F_{max}) in MHz.

4.4 Conclusion

This study was focused on a method to extend the frequency of operation a 2-D IIR beam filter that was proven to have practical RF applications. Such plane-wave filters have emerging applications in broadband beamforming using antenna arrays, which are useful for applications such as radar, microwave imaging, wireless communications, navigation and radio astronomy. The design techniques of multirate beam filters can be used to overcome the limitations in operating frequencies in ADCs and FPGA clock rates. In our example 2-phase prototype design, which is based on the ROACH-2 FPGA platform, it has been possible to extend the speed of operation by 100% by trading-off chip-area and power consumption. This increase could have been as high as 200% had the FPGA implementation exploited the 4-phase time-interleaved sampling supported on the ROACH-2 platform. The 2-phase polyphase design has higher complexity than the direct-form and differential-form versions of the same 2-D filter, albeit with a doubled frame rate. Our FPGA implementation of the digital beam filter is 2-phases at present, although the ADC sampling has been verified for 1-phase, 2-phases and 4-phases, leading to signal sampling per antenna at 240, 480, and 960 MHz, respectively. The ROACH-2 testbed provides a sophisticated hardware platform to implement the complete end-to-end systems and generate processed signals to do real-time analysis. The potential of practical implementations at RF/microwave bandwidths for 2-D IIR beam filters has been verified.

CHAPTER V

FPGA REALIZATION OF 1 GHZ MULTIRATE 2-D IIR BEAM FILTER WITH 4-POLYPHASES

This chapter explains the extension of the 2-phase polyphase 2-D IIR beam filter described in chapter 4. With successful realization of the wideband 2-D IIR beamformer that can operate close to 500 MHz earlier, the research work carried out related to the scope of this chapter shows potential to reach the goal of building a wideband beamformer that can operate close to a bandwidth of 1 GHz. The digital realization was limited to FPGA implementation as the expected objective was a study. The 16-channel ADC board [79, 3] is capable of supporting a maximum sampling rate of 960 $MSamples/s$, when it is set to demux mode of 4 with an external clocked input of 960 MHz. This in turn implies that the sampling operation can go up to 4 times the ROACH-2 fabric rate. This will produce 4 digital samples of the received signal for every clock cycle at the FPGA operating rate. We expect to take advantage of this fact when exploring 4-polyphase designs.

5.1 System Overview

We consider an antenna array of 32-antenna elements for this realization. The received signal at each antenna is decomposed into 4-polyphases and fed to the

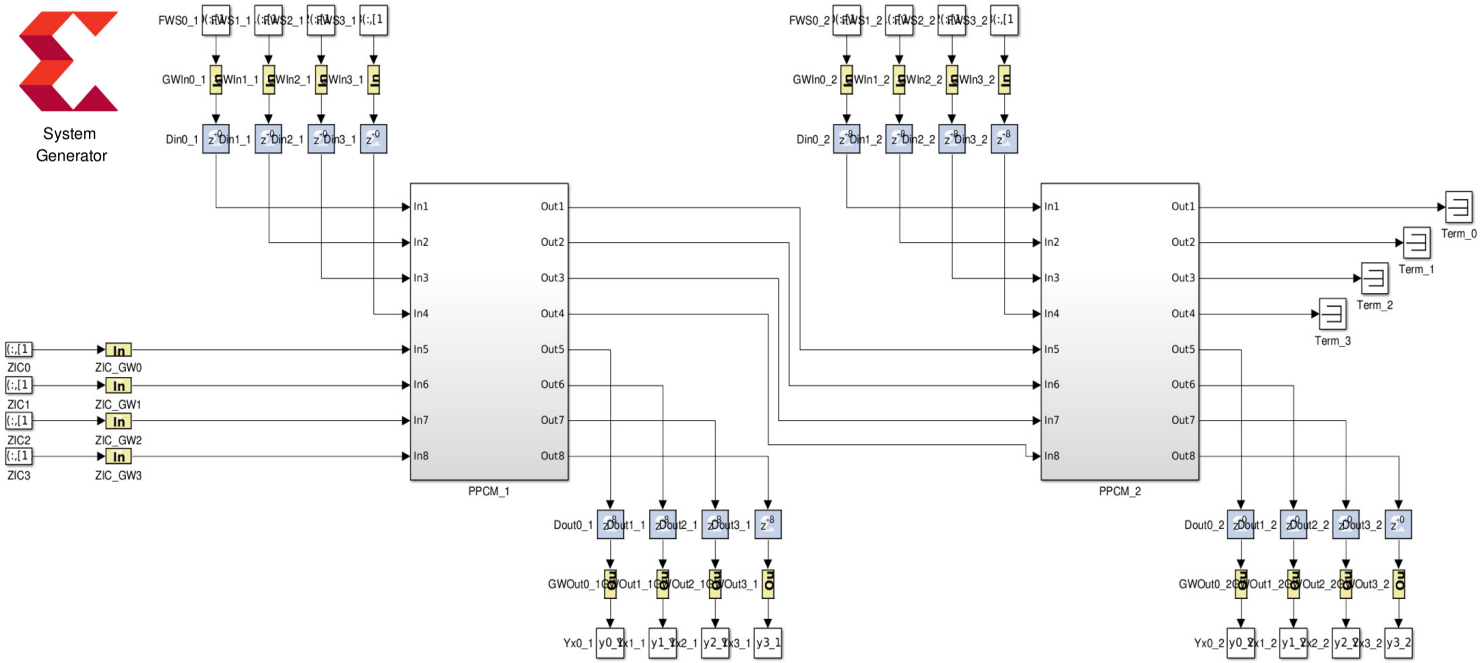

Figure 5.1: Four phase systolic array architecture of the 2-D IIR beam filter for a 2-element ULA.

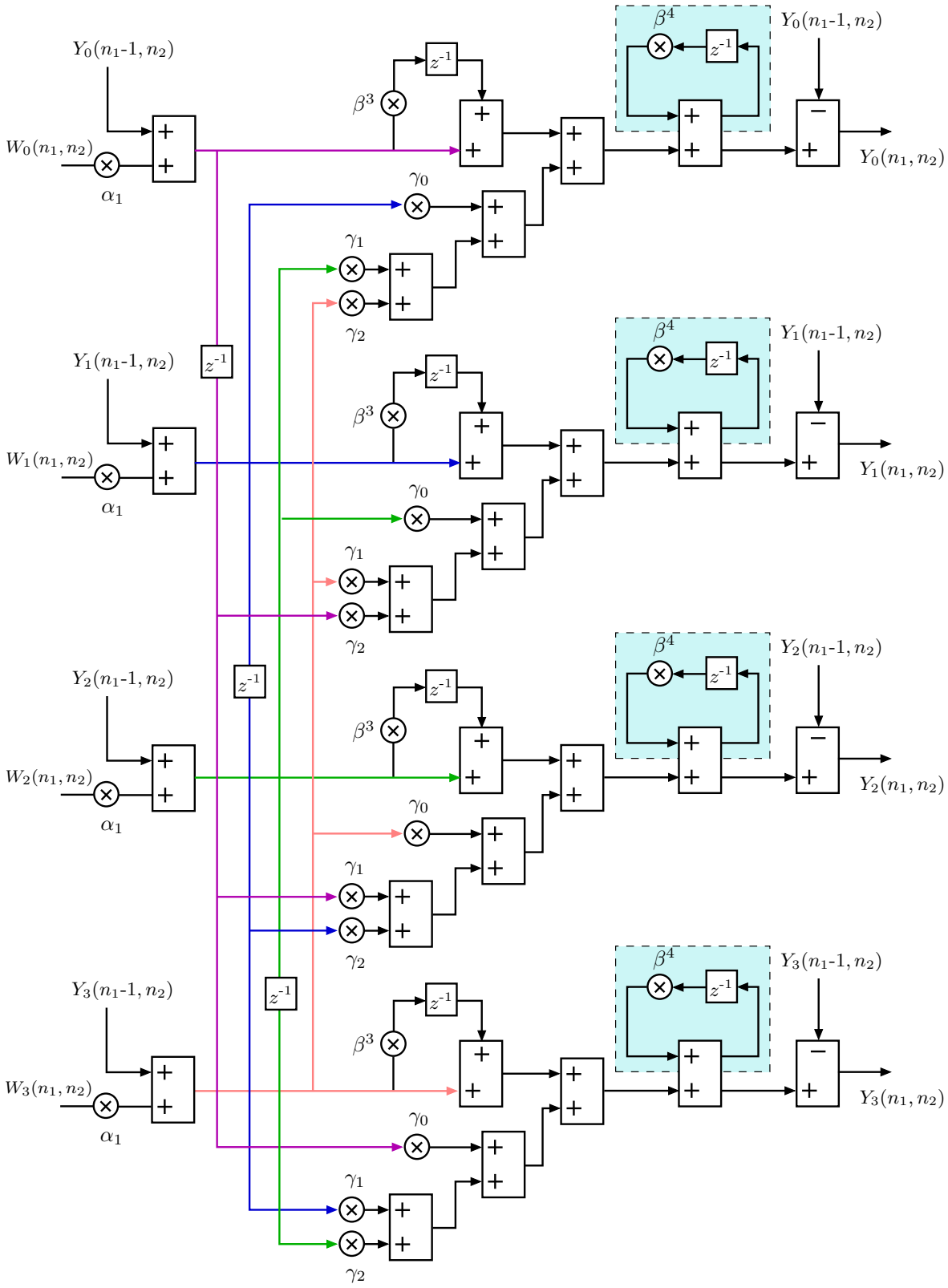

Figure 5.2: The time-interleaved polyphase PPCM block of the systolic array based 4-phase 2-D IIR beam filter.

corresponding input of each beam filter block. Similarly, the beam filtered output is also represented in a manner to obtain the 4-polyphases. Fig. 5.1 shows a part of the system architecture used during this simulation. For clarity, the figure illustrates 2 PPCM modules to shows the inter-PPCM connections and the connectivity to ZIC input blocks. The delay elements placed before the inputs and after the outputs of the PPCM enable synchronization of outputs.

5.1.1 LA-Optimized Transfer Function with 4-Polyphases

We derive the mathematical representation of the third-order LA-optimized transfer function using Eq. (4.1). The transfer function of the differential form 2-D IIR beam filter can be expressed as,

$$Y(n_1, z_2) = \frac{W(n_1, z_2) + \alpha_1 Y'(n_1, z_2)}{1 - \beta^4 z_2^{-4}} \left(1 + \gamma_0 z_2^{-1} + \gamma_1 z_2^{-2} + + \gamma_2 z_2^{-3} + \beta^3 z_2^{-4} \right) \quad (5.1)$$

where $\gamma_k = \beta^{k-1}(1+\beta)$ for $k = 1, 2, 3$, $\beta = \alpha_2 - 1$ and α_1, α_2 are defined as in section 3.1.1.

Comparatively the computational complexity and the hardware resource consumption for the digital beam filters depicted in this thesis increase drastically with the number of phases (see Fig. 3.3, 4.2 and 5.2). The 4-phase PPCM module requires a minimum of *24 multipliers, 28 adder/subtractors, and 11 delay elements*. Each block has 8 inputs and 8 outputs. Fig. 5.2 shows the complex architecture of the 4-phase PPCM architecture.

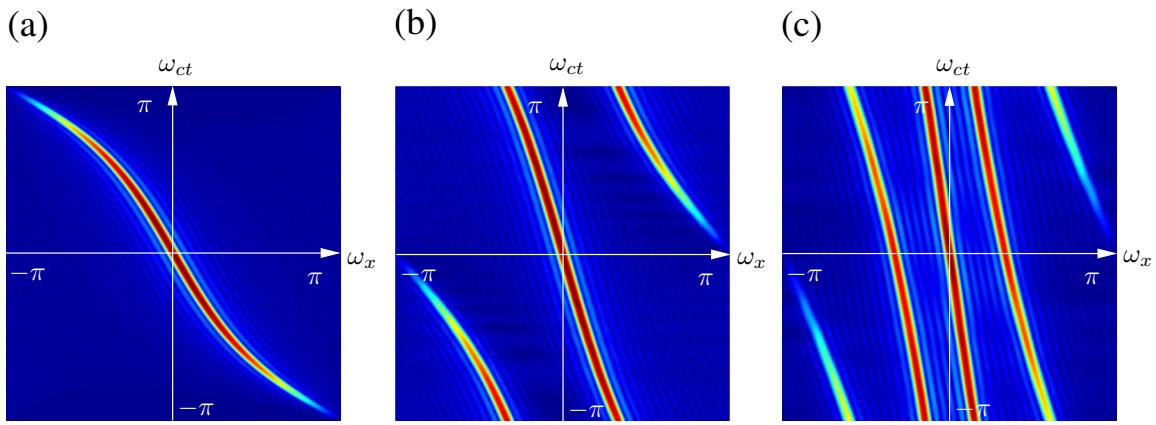

Figure 5.3: Frequency response of 4-phase 2-D IIR beam filter tuned to enhance RF signals arriving at a DOA of $\psi = 35°$. (a) Response after interpolating the beamformed output of four phases. Decomposed polyphase response of (b) two phase illustraring the temporal domain aliasing effect and, (c) frequency response of a single phase.

5.2 Simulation and Results

We use a systolic array of 32 antenna elements and the directional selectivity parameter was assumed to be $R = 0.005$ for all simulations. The frequency domain response of the 4-phase 2-D IIR beam filter was determined. Simulation results of the beamformed output of the interpolated signal as well as the individual phases were also determined for 16 and 32 bit input vectors. The filter was tuned to directionally enhance signals arriving at a DOA of $\psi = 35°$ with a pipelining latency of 16 clock cycles. The beam filter performance was determined by feeding in three Gaussian modulated pulses with DOAs $\psi_1 = 15°$, $\psi_2 = 35°$, $\psi_3 = 75°$ (shown in Fig. 5.4(a) assuming the RF antenna front-end sampling the received signal at a frequency of $F_s = 960\ MHz$. The beam filter successfully filtered out the desired signal with

Table 5.1: Computational complexity and throughput vs. number of phases for proposed low-complexity architectures with LA optimization. [1]

M-**phases**	# Multipliers (direct form)	# Multipliers (diff. form)	Relative gain	Frame rate
1	3	2	33%	F_{CLK}
2	10	8	20%	$2F_{CLK}$
3	21	15	28.6%	$3F_{CLK}$
4	36	24	33.3%	$4F_{CLK}$

DOA $\psi = 35^\circ$ while suppressing the undesired plane-wave signals. The decomposed outputs in frequency domain of the filtered signal which has a DOA of $\psi_2 = 35^\circ$ is illustrated in Fig. 5.4(c) and (d).

Table 5.1 gives an insight into the design complexity and variation in resource consumption. An increase in chip area is observed for both direct form and differential form version. However, the rate of increase in resource consumption in the differential form version designs is comparatively less.

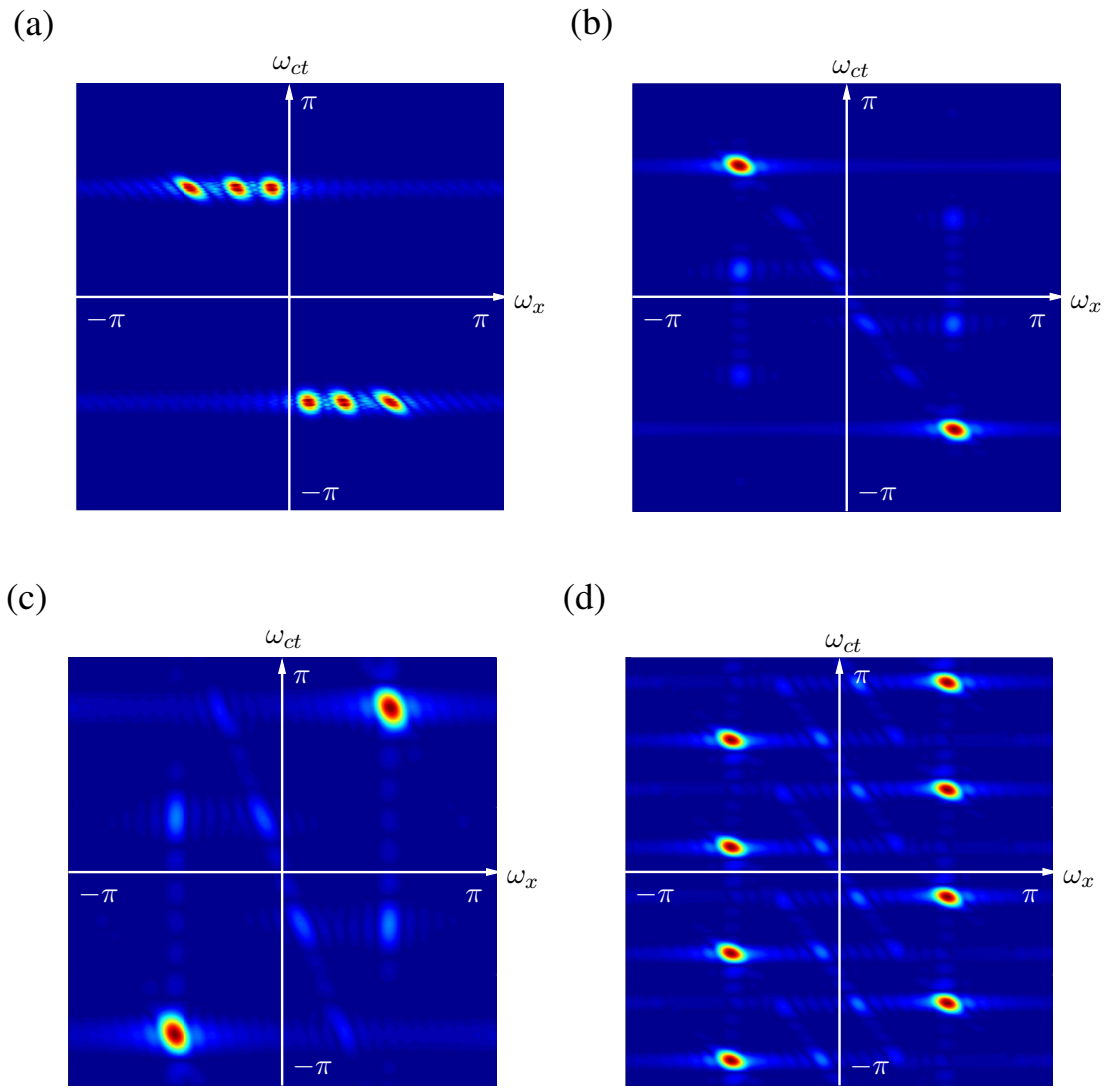

Figure 5.4: Directional enhancement simulation of the 4-phase polyphased 2-D IIR beam filter using 3 Gaussian modulated pulses in frequency domain. (a) Wideband input signals with DOAs $(15°, 35°, 70°)$, (b) Interpolated output signal with directional enhancement, (c) Decomposed output of the filtered signal of two polyphase, (d) Decomposed output of one phase with temporal aliasing effect.

5.3 Conclusion

The 2-D IIR multirate digital filter with 4-polyphases can be considered a fairly important design because it enables the hardware to operate at 4 times the fabric

rate of the non-polyphased design. Existing multi-input ADC cards used in FPGA DSP platforms generally operate in MHz. Hence, designs such as this enables to reach the gigahertz range. ROACH-2 realization of this polyphased digital beam filter with 16-channel ADC cards [79] at the frontend will further verify the potential for a $\approx$1 GHZ digital beamformer. This can be considered as a significant achievement of this research. Thus, we believe that $\approx$1 GHz beamformers will have a wide range of RF applications. However, this improvement in operating frequency comes with a trade-off in chip area. The number of multipliers and adder/subtractors has increased by 300% and 280% respectively in the 4-phase scenario comparing with the 2-phase digital filter. The polyphase structures tend to be complex in design and high in resource utilization. Thus, bulky and heavy power sources are needed in order to provide the required power for these designs. In conclusion, by using polyphase structures it is possible to increase the operating frequency of digital filters in multiples of non-polyphased designs. However, in practice the optimum number of polyphases used for a given beamformer should be decided based on the available hardware resources and power sources.

CHAPTER VI

DIFFERENTIAL FORM 3-D IIR FREQUENCY PLANAR BEAM FILTER FOR MILITARY RADAR APPLICATIONS

This chapter illustrates a detailed review on designing a 3-D IIR frequency planar beam filter, by extending a 2-D IIR beam filter into 3-D space-time domain using using the concept in [43, 91]. It is evident that a realization of a 3-D IIR beam filter better suits a practical scenario because of the use of two spatial dimensions. A step-by-step approach on designing the filter providing detailed explanation and results at each stage followed by a proposed systolic architecture with high-speed and low circuit complexity is also discussed in this chapter. This realization can be done by using both direct form [92, 21] and differential form version of the 2-D IIR beam filter described in chapter 3. However, we focus on the differential form version as it is computationally efficient and low in hardware foot print in FPGA turning out to be the best out of the two models. The 3-D IIR beam filter is designed using the differential form by cascading a pair of 2-D IIR beam filters. The simulation results presented in this section are based on (Xilinx) FPGA hardware co-simulation.

The chapter also describes a probable application in the military field. The state-of-the-art radar tracking systems in the military are based on phased-arrays and operates in the $\approx$3.5 GHz frequency range [93]. Phased arrays are based on FIR beam

filters which consume more hardware resources in comparison with IIR beamformers. We propose to use an IIR beamformer in place of the phased array to take advantage of lowered chip area and reduced cost. This section unfolds a technical analysis of a 3-D radar based on IIR beamformers designed using polyphase structures, cascaded MD IIR beam filters and ROACH-2 hardware platform comparing with technical specifications of SPY-1B radar [93]. The key goal is to elaborate on the relevance of this study as a better alternative to the existing designs.

6.1 Extending 2-D Beam Filters to 3-D

By referring to the plane wave theory described in chapter 2 (section 2.1.1 and 2.1.2), we can represent a plane wave in 3-D space as,

$$w(x, y, z, ct) = w_{PW}(\sin\psi\cos\phi x + \sin\psi\sin\phi y + \cos\psi z + ct) \tag{6.1}$$

where ψ is the elevation angle and ϕ is the azimuth angle [22] of the spatial DOA in 3-D space $|\psi| \leq 90^\circ$ (Fig. 6.1(a)). The ROS of a plane wave in 3-D space-time domain [94] has a beam shaped pass-band (Fig. 6.1(b)) passing through the origin (as explained in chapter 2).

The concept of building a 3-D beam filter using 2-D filters is based on filtering an RF signal from two different spatial dimensions. In the 3-D space-time domain, x, y and ct dimensions are orthogonal to each other. The signal components common to both x and y dimensions can be captured by using a 2-D beam filter directionally enhancing signals in the x-ct domain and sending it to a similar filter directionally

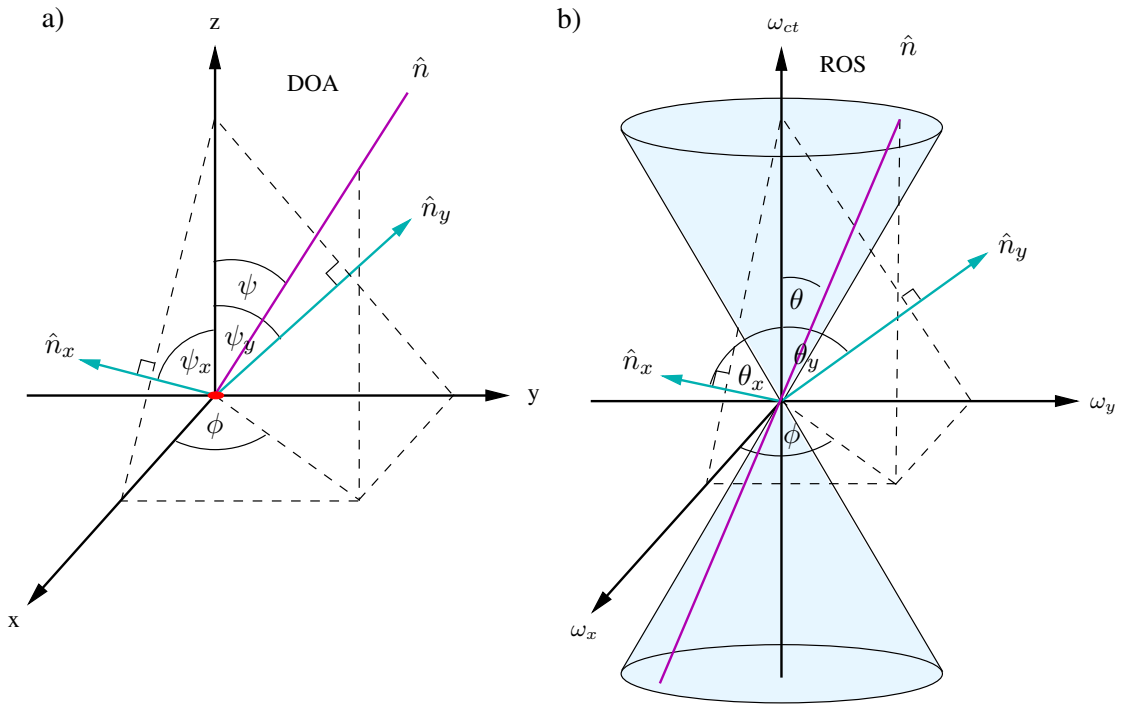

Figure 6.1: The graphical analogy of an incident plane wave used for 3-D beam filters derived by cascading two 2-D beam filter with two perpendicular spatial axis. (a) Incident plane wave in 3-D space domain and, (b) 3-D space-time domain.

enhancing signals in the y-ct domain. Hence, the view of the signal in x-ct and y-ct are totally different as shown in Fig. 6.1(b). The ROS can be defined as,

$$\theta = \tan^{-1}(\sin\psi) \tag{6.2}$$

$$\theta_x = \sin^{-1}(\sin\theta\cos\phi) \tag{6.3}$$

$$\theta_y = \sin^{-1}(\sin\theta\sin\phi) \tag{6.4}$$

in 3-D space-time $\omega(x, y, z, ct) \in \mathbb{R}$ [95, 96].

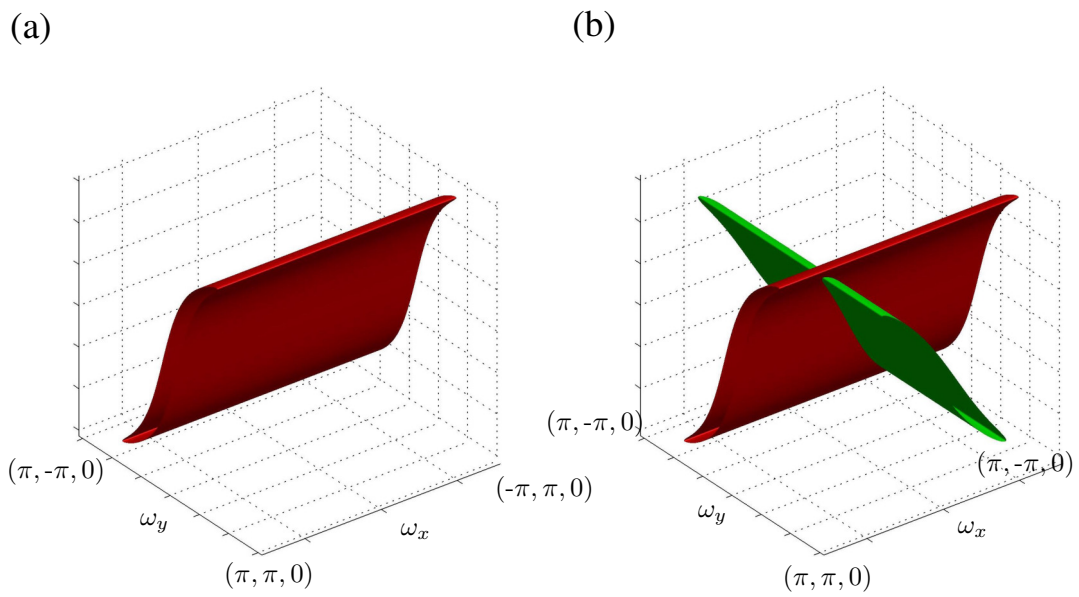

Figure 6.2: Frequency response of cascading of two 2-D IIR beam filters to obtain the 3-D IIR beam filter. (a) Frequency response of $H_1(\omega_x, \omega_{ct})$ and, (b) Responses of two filters before intersecting the beam filters.

6.1.1 3-D IIR Beam Filter

The above concept can be realized in hardware by cascading two 2-D beam filters in series directionally enhancing signals in (x, ct) and (y, ct) planes. Thus, the transfer function of the 3-D beam filter can be represented using 2-D beam filters as follows,

$$H(\omega_x, \omega_y, \omega_{ct}) = H_1(\omega_x, \omega_{ct}) H_2(\omega_y, \omega_{ct}) \tag{6.5}$$

The filter coefficients of $H_1(\omega_x, \omega_{ct})$ filtering the signal on (x, ct) plane is defined as [43],

$$\alpha_1 = \frac{2\cos\theta_x}{R + cos\theta_x + sin\theta_x} \tag{6.6}$$

and

$$\alpha_2 = \frac{2\sin\theta_x}{R + cos\theta_x + sin\theta_x} \tag{6.7}$$

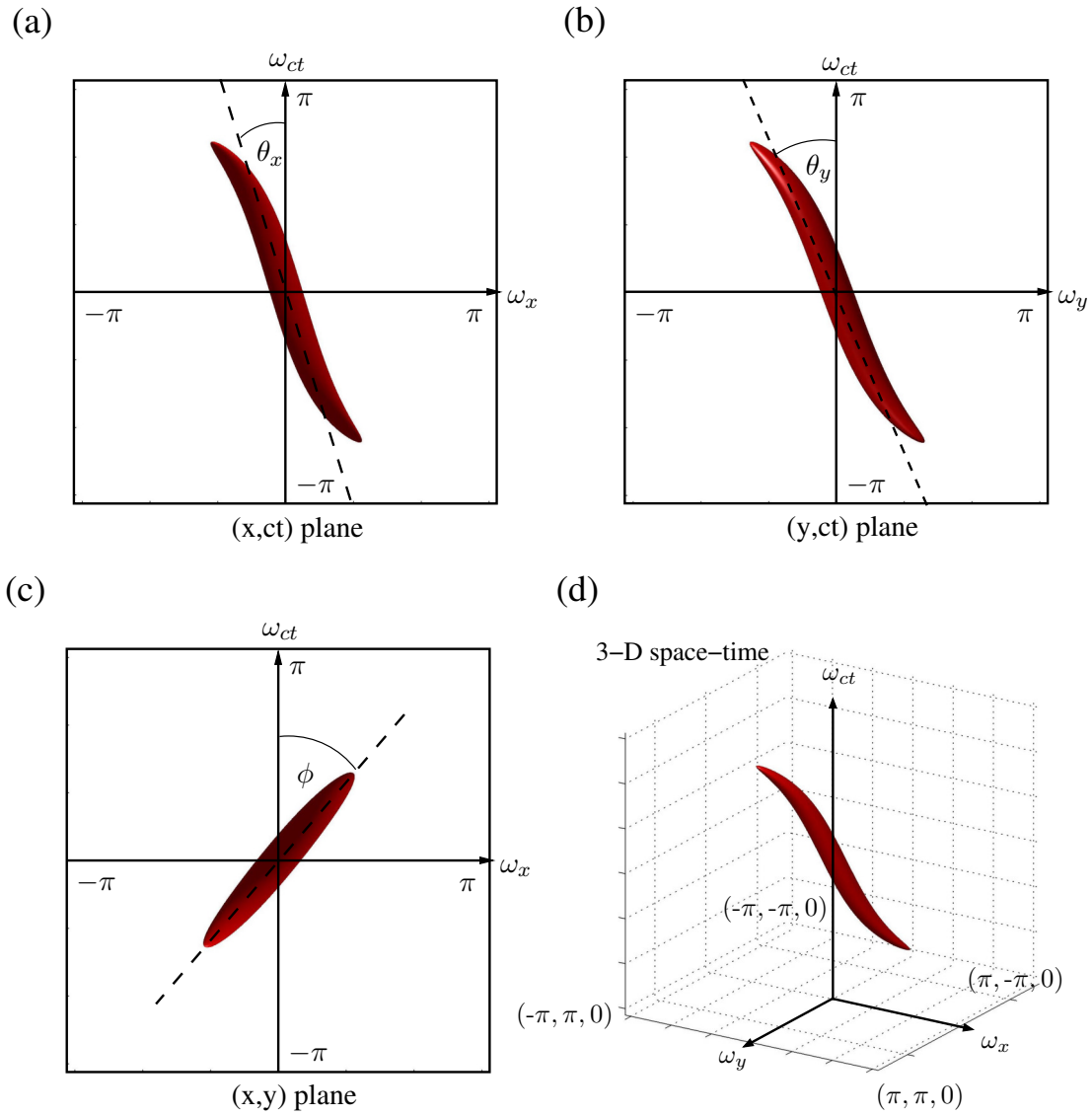

Figure 6.3: Frequency response of the 3-D IIR beam filter in (a) (x, ct) plane, (b) (y, ct) plane, (c) (x, y) plane and, (d) in (x, y, ct) 3-D space-time domain.

The filter coefficients for $H_2(\omega_y, \omega_{ct})$ filtering the signal on (y, ct) plane are defined as [43],

$$\beta_1 = \frac{2\cos\theta_y}{R + cos\theta_y + sin\theta_y} \tag{6.8}$$

and

$$\beta_2 = \frac{2\sin\theta_y}{R + cos\theta_y + sin\theta_y} \tag{6.9}$$

The selectivity parameter $R > 0$.

6.2 Simulation Results

The systolic array based hardware architecture for the 3-D beam filter is similar to that of the 2-D case (Fig. 3.3). The number of PPCMs required to implement the 3-D beam filter is two times the square of the number of antenna elements in a single one dimensional array ($N_{3D} = 2 \times {N_{2D}}^2$). Hence, the 3-D IIR filter demands heavy hardware resource consumption in comparison with the derived 2-D IIR beam filter.

6.2.1 Cascading 2-D IIR Beam Filters

To illustrate the intersecting of 2-D beam filters that produces the 3-D beam filter with a beam shaped passband, we use two 2-D IIR beam filters with DOAs $\psi = 30^\circ$ and $\phi = 50^\circ$ with selectivity parameter $R = 0.005$. Fig. 6.2(a) shows the frequency response of $H_1(\omega_x, \omega_{ct})$.

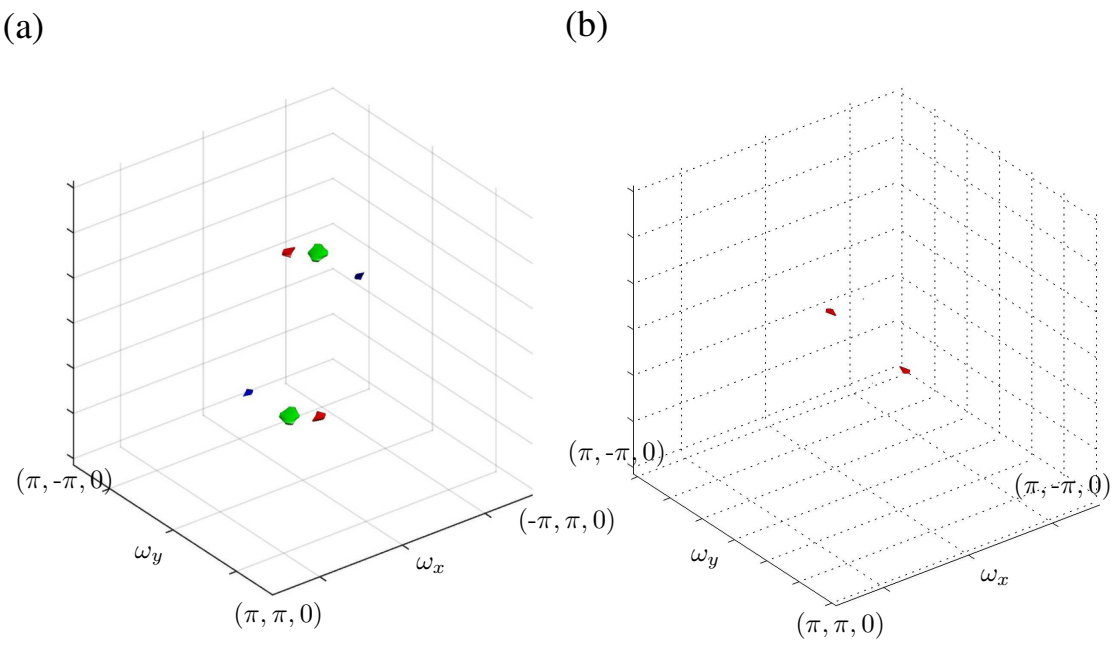

Figure 6.4: Directional enhancement of plane wave signals using the 3-D IIR beam filter. (a) Input signal and, (b) Filtered signal.

6.2.2 Frequency Response of 3-D IIR Beam Filter

The beam shaped passband (frequency response) obtained for the 3-D IIR frequency using the proposed method is shown in Fig. 6.3 for 32 antenna element arrays. The filter was tuned to a DOA of $\psi = 30°$ and $\phi = 40°$ in this scenario with selectivity parameter $R = 0.005$. The beam shape of the 3-D IIR beam filter was also graphically determined to observe the main lobes and side lobes as shown in Fig. 6.5.

6.2.3 Directional Enhancement Properties

Three raised cosine Gaussian modulated signals with three distinct DOA pairs, $(35°, 20°)$, $(40°, 55°)$ and $(80°, 110°)$ were fed to the filter to observe the performance of the filter as illustrated in Fig. 6.4(a) with the desired signal being $(80°, 110°)$. The

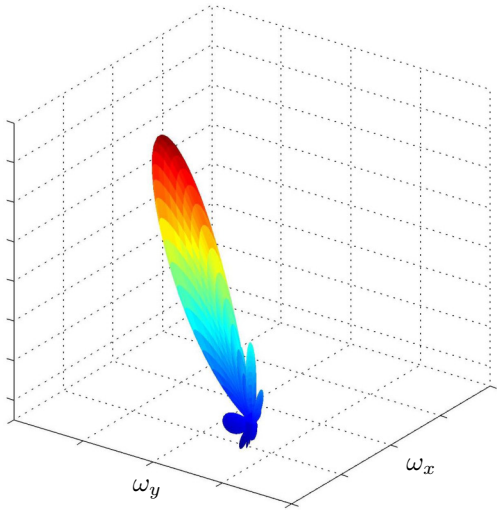

Figure 6.5: Beam shape of the 3-D IIR beam filter tuned as $\psi = 30°$ and $\phi = 50°$.

selectivity parameter was assumed to be $R = 0.00005$. The filter successfully filtered out the desired signal as shown in Fig. 6.4(b).

6.3 Military Radar Application Based on 3-D IIR Beam Filters

This section provides a comprehensive analysis of a promising potential application from a technical perspective of the 3-D IIR beam filter described in this chapter. The state-of-the-art research for radar tracking systems in warships in the military operates at approximately 3.5 GHz frequency range [93]. However, they are based on phased-arrays. As stated in previous chapters, phased arrays are based on FIR beam filters which consumes high hardware resources in comparison with IIR beamformers. Hence, a radar application based on IIR beam filters is likely to be efficient in chip area. This section unfolds how the results obtained on the research carried out

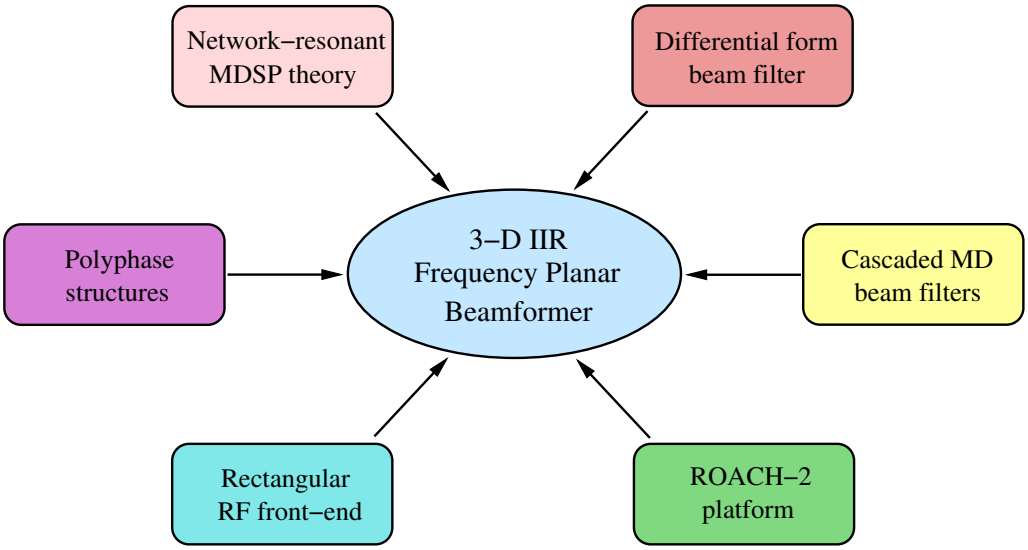

Figure 6.6: The building blocks of a multirate 3-D IIR frequency planar beam filter.

can be used to build a 3-D radar based on IIR beamformer that can have similar technical specifications as SPY-1B radar [93]. Alternatively how the combination of network-resonant MD network theory, polyphase structures, cascaded MD IIR beam filters and ROACH-2 hardware platform can effectively used for a practical application.

We consider an octagonal shaped symmetrical planar array with 4572 antenna elements. Hence, the planar array will consist of systolic array based ULAs of different sizes ranging from 36 to 72 antenna elements. The inter antenna spacing and the size of the antenna will vary on the operating frequency of the beam filter. By using multirate (with 4-polyphases) 2-D IIR beam filters (5) it is possible to have the FPGA fabric rate reduced by a factor of 4. The objective is to match the operating

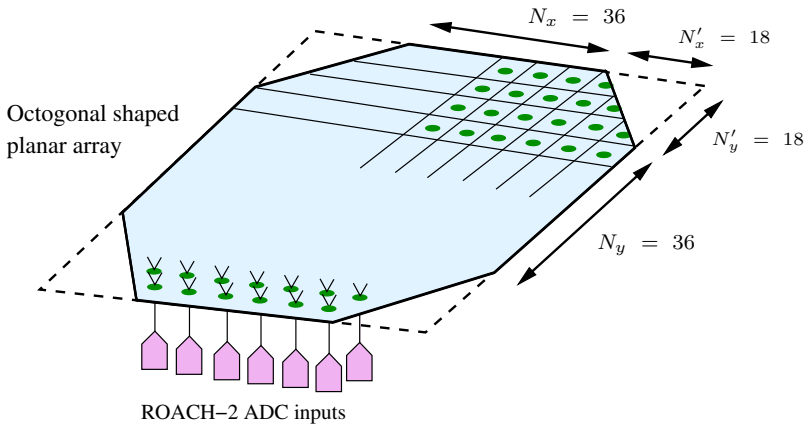

Figure 6.7: Proposed octogonal shaped 2-D planar antenna array front-end of the 3-D radar.

frequency at 3.5 GHz. Hence, the Nyquist sampling rate is bound at 7 GHz limiting the polyphase beam filters to operate at 1.75 GHz ($\frac{F_s}{M}$).

For our analysis we selected 3 available ADC boards that can be interfaced with ROACH-2 to sample RF signals in the GHz range [79]. The overall resource requirement varies depending on the ADC board of interest. We consider ADC16x250-8 RJ45 rev-1 [79], the 16-input ADC board as one option since it was used for simulations described in this research. ADC1x5000-8 and KatADC are 2-input ADC boards that can sample signals at 2.5 and 1.5 GHz respectively. All 3 ADC boards in consideration can sample signals with 8-bit quantization levels. KatADC is a popular ADC developed by Texas Instruments Inc. that is widely used in radio telescopes such as Square Kilometer Array (SKA) [77].

Table 6.1: Achievable operating speeds of the proposed 3-D radar at different ADC sampling rates.

ADC board	# ADC inputs	Poly freq., F_{poly} (GHz)	Samp. freq., F_s (GHz)	Oper. freq., F_{radar} (GHz)	Ant. space, Δ_d (mm)
ADC16x250-8	4	0.96	3.84	1.98	75.76
Kat-7 ADC	2	1.5	6	3.00	50
ADC1x5000-8	2	2.5	10	5.00	30

6.3.1 Hardware Complexity

This 3-D beamformer can be considered as highly complex design that requires a large chip area. Both cascaded 2-D IIR beamformers require the same number of multipliers and adder/subtractors; they require $(24 \times 4572 \times 2 =)$ 219456 multipliers and $(28 \times 4572 \times 2 =)$ 256032 adders respectively. One disadvantage of realizing the proposed application in ROACH-2 is the number of ROACH-2 boards is very large for this deployment (Table 6.2). The number of ROACH-2 boards required for second stage beam filter arrays are governed by maximum throughput of SFP+ 10 GbE interfaces. ROACH-2 can transmit and receive data a maximum rate of 80 Gbps using eight 10 GbE links. It is also important to note that intermediate subsystems should be placed at the end of each beamformer to perform networking and switching operations as needed. This module will have a very complex mechanism as the operating data rates are in the high-end.

Table 6.2: Hardware resource consumption, complexity and planar array sizes at different ADC sampling rates.

ADC board	Total # of ROACH-2 boards	Array size (m^2)
ADC16x250-8	1032	5.23×5.23
Kat-7 ADC	1829	3.45×3.45
ADC1x5000-8	2286	2.07×2.07

Using 16-input ADC boards is not practical due to the resulting large area of $\approx 25m^2$ required to accommodate the antenna array; such a large array would expose the warship to the enemy as an easy target. Moreover, the achievable maximum operating frequency is limited at ≈2 GHz. However, when the radar is designed using the other two ADC boards, the required area is significantly reduced. ADC1x5000-8 requires only $\approx$ 4 m^2 area and can operate at 5 GHz making it a better match. However, this comes with a trade-off in power consumption and cost for the increased hardware resources (Table 6.2).

6.4 Conclusion

We propose a novel speed-optimized architecture for real-time 3-D IIR frequency-planar beam filters. Such plane-wave filters have emerging applications in broadband beam forming using antenna arrays, which are useful for radar imaging, communications, navigation and radio astronomy.

From the simulation results of the extended 3-D IIR beam filter, it is evident that realization of this filter consumes a moderate amount of hardware on ASIC implementations with operating frequencies in the range of 0.5 GHz. Moreover, by optimizing the hardware architecture of PPCM design we can further achieve higher operating frequencies well beyond 1 GHz. i.e. we can potentially build a high performance 3-D IIR beam filter by fine tuning the delays of adder and multipliers and the feedback loop by minimizing the critical path delay.

One probable application is the 3-D radar to detect and track targets. From the analysis, we can clearly see that the hardware chip area and the computational complexity is on the high side for a planar array with a large antenna elements. The limitations in maximum fabric rate and 10 GbE networking interfaces in a ROACH-2 hardware platform affect the hardware resource consumption. Another key influencing factor is the type of ADC's used and their maximum sampling rate. Most of the ADC chips are limited to not more than few GSamples/s with the current technology. It is possible to build beamformer with better performance if ADC boards are able to sample in 10 GSamples/s and with more ADC inputs along with FPGA's that can support fabric rates required. However, since IIR beamformers are computationally efficient than FIR beamformers in general, we believe that this method would be suitable alternative for an application such as SPY-1B radar [93].

CHAPTER VII

CONCLUSION AND FUTURE WORK

7.1 Conclusion

The research studied within the scope of this thesis is unique to digital signal processing of RF signals using multidimensional network theory. Thus, the introduction of multidimensional signal theory has led the path to build applications to detect and process RF signals signals transmitted from a location in 3-D space. We can summarize by stating that multidimensional signal processing involves processing RF signals by employing a collection of antenna receivers organized in particular orientation to directionally enhance RF signals received from a designated DOA. FPGA platforms are a commonly used tool to verify hardware realization for DSP applications. The flow of chapters in this thesis presents a study on MD IIR beam filters realized in FPGA platforms that will lead to potential applications in emerging areas. We believe that modern day UWB applications show promising potential to use such filters in high-speed digital wireless communications, imaging, radar and radio astronomy.

Chapter 2 provides a detailed review on multidimensional network theory starting by introducing the characteristics of a planar wave signal and the building

blocks of MD network theory. The chapter unfolds two main types of MD signal processing methods of 2-D and 3-D space-time techniques and their representation in time and frequency domains. The chapter also introduces existing narrowband and wideband beamformers along with their characteristics. The basis for all realizations explained in the following chapters is network-resonant beam filter theory which is an extension of the conventional IIR beam filters to model using LC passive circuits. The mathematical derivations and the directional enhancement properties of this theory are also explained while mapping the relevant parameters to the RF space time domain. The introduction of polyphase structures and ROACH-2 DSP Platform lays the foundation for the realizations explained in rest of the chapters.

Chapter 3 This is the first attempt on realizing systolic array based 2-D IIR frequency planar beam filters in ROACH-2 hardware platform. The use of the differential form architecture leads to a computationally efficient architecture with the lowest possible resource utilization. The study successfully verifies the implementation of the 2-D IIR beam filter at an operating frequency of 200 MHz. The resulting filters are well suited for compact designs that use peripheral cards with two 16-channel ADC analog inputs for which the sampling frequency of a channel is limited to 240 MHz. This is the first implementation of its kind on a processing platform that takes advantage of the peripheral ADC cards to build an integrated RF beam filter. This leads to new research and improvements to realize real-time implementations for 2-D IIR beam filter systolic arrays.

Chapter 4 Under the existing technology operating frequencies of 200 MHz can be considered insufficient for a beamformer application. This is a clear disadvantage in the design described in chapter 3. As an extension, chapter 4 provides a mechanism to enhance the speed of operation of the systolic array based 2-D IIR filter up to 480 MHz. This was achieved by employing polyphase structures on the temporal feedback loop using LA optimization methods to decrease the critical path delay. This increased speed comes at the expense of higher hardware resource consumption to perform the additional required additions/multiplications. Thus we can conclude that polyphase structures for digital architectures can be an important concept which can be used to improve the performance of a conventional digital design to achieve high speeds overcoming the limitations in existing FPGA technology.

Chapter 5 we prove the successful realization of a systolic array based wideband beamformer that can operate at 1 GHz. However, during the research it was also noticed that this improvement comes with a huge increase in hardware resource consumption and power consumption when comparing with the 2-phase and single-phase designs. Moreover, it is evident that differential form version has far better gain in realization in comparison with the direct form beam filter design. This design can be of use as long as the application can tolerate this excessive resource requirement.

Chapter 6 introduces a method to derive a 3-D IIR frequency planar beam filter using the 2-D IIR beam filters discussed in previous chapters. The significance of this proposed technique is that the entire 3-D beam filter architecture incorporates

2-D beam filter modules. Moreover, it is important to note that this 3-D beam filter architecture can be used in many practical applications than 2-D beam filters because we live in a three dimensional space. However, there are limitations of this proposed beam filter when it comes to realization in existing hardware platforms. The demand for an excessive amount of chip area can be considered as one of the main disadvantages of this approach. The analysis of the proposed application clearly highlights the importance and novelty of this research. Apart from 3-D radar applications we believe that, this research can be applied for telescopes in radio astronomy to directionally enhance signals with wider bandwidth. Yet again, it is evident that ROACH-2 is an ideal hardware platform for high-level research. The downside is that excessive amount of hardware resource consumption and the cost incurred with RF front-end circuitry.

7.2 Future Work

There are numerous ways to expand research outlined in this thesis. Potential future extensions can be highlighted as follows,

1. Design and build the RF front-end consisting of the antenna array to receive signals operating at the designated frequency (100, 480 MHz etc.)
2. Build the prototype beamformer with the linear array RF front-ends for the ROACH-2 based real-time 2-D IIR beam filter using the methodology proposed.

3. Implement the digital design of polyphase architecture with 4-phases in ROACH-2 to further improve the speed of operation to reach the gigahertz range to be used in a more practical application potentially in radio astronomy.

4. Explore methods to address the disadvantages in polyphase structure designs of increased complexity and resource consumption using more efficient algorithms.

5. Research on methods to reduce the hardware foot print of the differential form 3-D IIR frequency planar beam filter.

6. Implement the 3-D IIR beam filter using multiple ROACH-2 based 2-D IIR beam filters since it can easily be interconnected through the high speed SFP+ 10 GbE interfaces ultimately leading to verify the feasibility of realization in the stated SPY-1B radar.

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