DESIGN OF A TEMPERATURE INDEPENDENT MOSFET-ONLY CURRENT REFERENCE

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Utthej Nukala

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DESIGN OF A TEMPERATURE INDEPENDENT MOSFET-ONLY CURRENT REFERENCE

Utthej Nukala

Thesis

Approved:

Co-Advisor
Dr. Joan E. Carletta

Co-Advisor
Dr. Robert Veillette

Committee Member
Dr. Kye-Shin Lee

Department Chair
Dr. Alex De Abreu-Garcia

Accepted:

Dean of the College
Dr. George K. Haritos

Dean of the Graduate School
Dr. George R. Newkome

Date

ABSTRACT

This thesis presents the design of a temperature-independent MOSFET-only current reference. A design procedure for the generation of a current reference using a MOSFET-only circuit is proposed. The design procedure is straightforward and the circuit is simpler than many other published approaches. The design consists of a simple current generation circuit with its transistors biased at their respective zero temperature coefficient (ZTC) points and two correction circuits that compensate for the temperature-induced current variations at the output. This current reference finds its place in potential applications that include digital-to-analog converters, analog-to-digital converters, phase locked loops, oscillators, analog buffers and operational amplifiers.

The transistor-level circuit for the generation of a 50µA current reference is designed according to the proposed design procedure and its functionality is verified by simulation. This circuit is implemented in a 0.5µm SOI process. This 50µA current reference circuit achieves a temperature coefficient of 5ppm/^{o}C over the operating temperature range of 27^{o}C to 125^{o}C, which is better than most published MOSFET-only current reference designs.

DEDICATION

Dedicated to my Parents and Sister.

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CHAPTER I

INTRODUCTION

1.1 Motivation

Reference circuits, whether providing reference voltages or currents, are some of the most important kinds of building blocks in analog and mixed-signal circuits. A reference circuit should operate independently of changes in the temperature and the power supply voltage. Many high-precision temperature-compensated and supply-voltage-insensitive reference circuits have been proposed in the literature over the last few decades [1-13]. Research on simple and reliable reference circuits has been continuously ongoing. Current references are more widely used than voltage references in complex analog circuits where long metal lines are used; current references have an advantage over voltage references in that they are not affected by voltage drops across the metal line [1].

Analog signals can be represented using either voltages or currents. The current-mode approach is chosen mainly for the implementation of analog circuits for the reason that many functions are easy to implement in current mode. For example, arithmetic operations such as addition, subtraction and scaling require operational amplifiers and resistors in voltage mode and hence voltage mode implementation of these operations

often consumes significant area and power. In contrast, these operations require only the use of current mirrors in a current mode approach. The current mode approach has an advantage that it requires less hardware than the voltage mode approach. It uses no operational amplifiers; further, it requires no resistors, which are difficult to implement accurately in integrated circuits. Hence, current-mode circuits are widely used, and thus current reference circuits are also widely used.

Current references are needed for many major building blocks in analog circuits, such as operational amplifiers, analog buffers, oscillators, phase locked loops, analog-to-digital converters and digital-to-analog converters [4]. The performance of these circuits depends upon the accuracy and stability of the bias currents used in them. A current reference circuit may be used to provide a bias current when high precision is required. The bias current provided by a current reference circuit ensures the stable and precise operation of the analog circuit in which it is used. Current references that are simple, efficient and easy to design are highly desired.

The most common technique used for the generation of a voltage or current reference is the bandgap reference technique. In this technique, the reference voltage or current is generated by combining the base-emitter voltage of a bipolar transistor V_{BE}, which has a negative temperature coefficient, with the difference between the base-emitter voltages of two bipolar transistors biased with unequal current densities ΔV_{BE}, which has a positive temperature coefficient. Some other techniques for reference generation have been proposed in the literature, based on the differences between depletion and enhancement MOSFETs [12], the thermal properties of MOSFETs biased in the weak inversion region [13], and the mutual compensation of the temperature

characteristics of threshold voltage and mobility [2, 4, 11]. A detailed description of these techniques is presented in Chapter II.

Some analog circuits are required to operate over extended temperature ranges. The temperature range of operation for a military application is -55^{o}C to +125^{o}C, for an industrial application is -40^{o}C to +85^{o}C and for a commercial application is 0^{o}C to +70^{o}C. Reference circuits must be designed so as to provide stable and reliable operation throughout the desired temperature range.

1.2 Goals of thesis

The major goal of this thesis is to design a simple, MOSFET-only current reference. The current reference circuit should not use any diodes and bipolar junction transistors (BJTs). Processes that are developed recently are mostly MOSFET processes, for the reason that fabrication of bipolar transistors is complex and they consume more power and occupy more area than MOSFETs [14]. The low cost of fabrication and the possibility of placing both analog and digital circuits on the same chip so as to improve the overall performance and reduce the cost of packaging make MOSFET technology attractive [15]. Although it is possible to use lateral BJTs in some MOSFET processes, inclusion of BJTs requires a more complex and costly fabrication process [15] and also these lateral BJTs are more sensitive to packaging stress and process variations [16]. Finally, current reference circuits using BJTs are generally complex and hence occupy a large area.

Many published current reference circuit designs are not MOSFET-only circuits; the designs use other components, such as resistors. The performance of these reference circuits depends on the quality of the implementation of the components; for example,

inaccuracy in the resistor value can significantly degrade the performance of the reference circuits. Hence the primary goal is to design a MOSFET-only circuit.

The current reference circuit should be simple and it should use only on-chip components, i.e., no external components are to be used. Some current reference designs in the literature use components like resistors that are external to the chip. This again increases the area of the circuit.

In this thesis, a current reference circuit was designed in a 0.5µm SOI process. The MOSFET models provided for the SOI process were characterized for the temperature range of 27^{o}C to 125^{o}C. The current reference circuit was designed to operate over this full temperature range, with a temperature coefficient of about 5ppm/^{o}C. A review of the literature found that there are only a few published designs that have a temperature coefficient less than 10ppm/^{o}C. To the best of our knowledge, the best temperature coefficient achieved with a published MOSFET-only circuit is 16ppm/^{o}C [10].

1.3 Summary of contribution

A procedure for the design of a current reference circuit is proposed and a 50µA current reference has been designed. The circuit is a simple, MOSFET-only circuit consisting of only twelve MOSFETs. The temperature coefficient obtained is 5ppm/^{o}C over the operating temperature range of 27^{o}C to 125^{o}C.

An important contribution of this thesis is a clear, step-by-step procedure for the current reference design. The circuit is designed based on the idea of biasing the current generating MOSFET at a particular voltage, which makes the MOSFET less sensitive to the changes in temperature. The reference current is generated in the current generation

circuit with the help of the bias voltage provided by the bias generation circuit. The behavior of the reference current over temperature is studied and the reference current is corrected for its temperature coefficient using the correction circuit and the Widlar current mirror circuit. A small signal analysis is performed on the current reference circuit to analyze the effect of power supply variations on the reference current. The circuit achieved a power supply rejection ratio (PSRR) of 84dB. Simulations were performed at all the four process corners to analyze the effect of process variations on the reference current and it was observed that the reference current is affected severely by process variations.

1.4 Organization of rest of thesis

The rest of the thesis is divided into four chapters. In Chapter II, background material is given and techniques and topologies for current reference circuits available in the literature are discussed in detail. In Chapter III, the design of a 50µA current reference using a basic MOSFET-only circuit that can be operated in the temperature range of 27^{o}C to 125^{o}C is discussed. The need for the addition of correction blocks is shown using simulation results. In Chapter IV, the design of a complete MOSFET-only current reference circuit is presented, and the improvement in performance of the circuit after the addition of correction blocks is discussed with the help of analysis and simulation results. In Chapter V, conclusions are drawn and possible future work is discussed in detail.

CHAPTER II

BACKGROUND AND RELATED WORK

In the first chapter, the importance of current references to the operation of analog and mixed-signal circuits was discussed. In this chapter, background needed to understand the proposed current reference circuit is given. In addition, existing current reference circuit design techniques and topologies are summarized.

Before getting into the details of existing current reference circuit design techniques, the temperature coefficient of a quantity is defined. The temperature coefficient of a quantity is the derivative of the quantity with respect to temperature. The temperature coefficient specifies whether that quantity increases or decreases with an increase in temperature, and how much. A quantity is said to have a positive temperature coefficient if the quantity increases with an increase in temperature. Similarly, a quantity is said to have a negative temperature coefficient if the quantity decreases with an increase in temperature.

2.1 Bandgap reference

The most common technique used for the generation of a current reference is the bandgap reference technique. The main idea here is that if two quantities that vary linearly with temperature and that have temperature coefficients (TCs) of opposite sign, are added with proper weighting, the resulting sum will have a zero TC.

The base-emitter voltage V_{BE} of a bipolar transistor or, more generally, the forward bias voltage of a pn-junction, exhibits a negative TC. Also, if two bipolar transistors are operated at unequal current densities, the difference between their base-emitter voltages ΔV_{BE} is directly proportional to the absolute temperature; i.e., ΔV_{BE} exhibits a positive TC [15]. A weighted sum of V_{BE} and ΔV_{BE} is the basis for the design of a temperature-insensitive voltage reference.

This bandgap voltage reference concept has given rise to new ideas that lead to the design of current references. Figure 2.1 shows the basic block diagram of a current reference. Two currents, one with a positive temperature coefficient and one with a negative temperature coefficient, are generated; they are added with proper weighting to obtain a temperature-insensitive reference current. The current having a positive temperature coefficient is termed as a proportional-to-absolute-temperature (PTAT) current, whereas the current having a negative temperature coefficient is termed as a complementary-to-absolute-temperature (CTAT) current. The weights are necessary because the PTAT and CTAT current magnitudes might not vary by the same amount with an increase in temperature. There are a number of ways to generate the PTAT and CTAT currents. Some of the designs reported in the literature are discussed in Section 2.3.

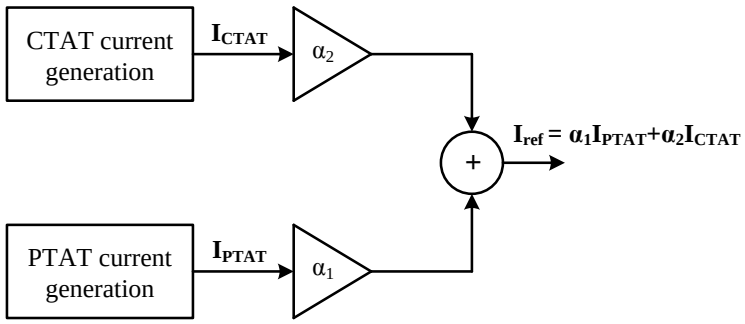

Figure 2.1 Basic block diagram of current reference circuit

2.2 ZTC point of a MOSFET

One of the most popular techniques used for current reference generation is the operation of a MOSFET near its Zero Temperature Coefficient (ZTC) point. A brief description of the ZTC point is presented in this section.

The concept of the ZTC point can be understood by considering the drain current of an NMOS transistor operating in the saturation region,

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_{tn})^2 \tag{2.1}$$

where

I_D is the drain current

μ_n is the charge carrier mobility

C_{ox} is the oxide capacitance

$\left(\frac{W}{L}\right)$ is the aspect ratio of the channel

V_{GS} is the gate-to-source voltage

V_{tn} is the threshold voltage

In Equation 2.1, the charge carrier mobility (μ_n) and the threshold voltage (V_{tn}) are the major temperature dependent parameters. Both these quantities decrease with an increase in temperature. However, they have an opposite effect on the drain current; i.e., with decrease in mobility the drain current decreases, and with decrease in threshold voltage the drain current increases. The ZTC point is the bias point at which there is a mutual compensation between the temperature effects on the mobility and the threshold voltage [11]. A transistor biased near its ZTC point has minimal variation in its saturation current over temperature.

The ZTC point of a transistor can be found experimentally by plotting its trans-conductance characteristics at different temperatures. All the curves intersect at about the

same point. This point of intersection is the ZTC point of the transistor. Figure 2.2 shows the transconductance characteristics for an NMOS transistor at different temperatures and it also shows the point of intersection of all these curves as the ZTC point. It can be observed that when a transistor is operated below the ZTC point, the current will have a positive temperature coefficient (the current increases with an increase in temperature) and the voltage will have a negative temperature coefficient (the voltage decreases with an increase in temperature). Similarly when a transistor is operated above the ZTC point, the current will have a negative temperature coefficient and the voltage will have a positive temperature coefficient.

In practice, the transconductance curves will not intersect at exactly a single point, because the temperature effects of mobility and threshold voltage do not cancel each other exactly at all temperatures for any given bias condition. Hence, there will be a small non-zero temperature coefficient even at the so-called ZTC point. Also, the ZTC point depends on the dimensions of the transistor as well as the drain-to-source voltage.

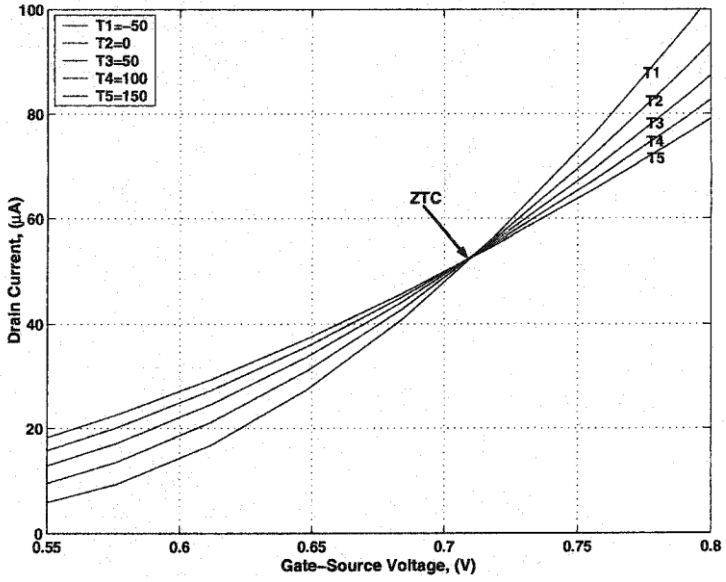

Figure 2.2 ZTC point of a transistor (from [11])

2.3 Literature review

A brief review of the current reference circuit designs reported in the literature is now presented. The current reference circuit designs can be classified into two categories: the designs that are based on the bandgap reference technique and the designs that are not based on the bandgap reference technique.

The designs presented in [1], [2], [3], [5] and [6] fall into the first category. They make use of either BJTs or diodes for implementing the bandgap reference technique. These designs first generate a voltage reference with some temperature coefficient and then, with the help of a resistor having a temperature coefficient of the opposite sign, convert the voltage into a current with a reduced temperature coefficient.

The designs presented in [4], [7], [8], [9] and [10] fall into the second category. The designs in [4] and [10] are based on the ZTC point of a MOSFET; currents with opposite temperature coefficients are obtained by biasing two MOSFETs, one above and one below their respective ZTC points. The weighted versions of these currents are used to obtain the current reference. The designs in [7] and [8] are based on generating two voltages or two currents having opposite temperature coefficients; these voltages or currents are weighted and added to get the final current reference. The design in [9] is based on the β-multiplier idea. This is an alternative way for the bandgap technique to generate PTAT and CTAT currents. Here weighted versions of the generated currents are added to obtain the current reference. Each of these designs is discussed in a little more detail in the following paragraphs. The sensitivity of the reference current to variations in temperature is calculated as

$$\text{ppm/}^{o}\text{C} = \frac{\Delta I_{max}}{I_{nominal}} \frac{10^6}{\Delta T}$$

where ΔI_{max} is the maximum variation in the current

In [1], a current reference circuit based on the bandgap reference technique was realized using the following components: MOSFETs, BJTs, on-chip resistors and an operational amplifier (OPAMP). The circuit achieves a reference current with a temperature coefficient of 50ppm/^{o}C over the temperature range of (0^{o}C, 110^{o}C). Three components are combined so as to ensure the temperature independence of the reference current in this circuit. The first is a base-emitter voltage V_{BE} with a negative TC. The second is a proportional-to-absolute temperature (PTAT) voltage. The third is the current through the on-chip resistors, which has a negative TC. The V_{BE} voltage and the PTAT voltage are added to reduce the TC of the reference current. However, their TC's do not cancel each other exactly. So, the current through the on-chip resistors is used to achieve better TC cancellation. N+ diffusion resistors without silicide were used here, since of all the available types of on-chip resistors they are least sensitive to process variations. This circuit requires a startup circuit to bring the transistors to the desired bias point upon power up.

The current reference circuit in [2] was also realized using MOSFETs, BJTs, resistors and an OPAMP. This current reference has a temperature coefficient of 6.9ppm/^{o}C over the temperature range of (-40^{o}C, 85^{o}C). This current reference was realized by adding a PTAT current and a CTAT current, both generated with the help of a bandgap reference circuit. The temperature coefficient of the reference voltage generated by the bandgap reference is negative. Also, the variation of this voltage is small in the working temperature range as the voltage was obtained by temperature coefficient compensation. This negative TC reference voltage is converted into current using a

voltage-to-current conversion circuit. The resistor used for the conversion is made of a special high-precision material, so that the resistor's TC is small and can be neglected. As a result the current obtained will also have a negative TC. In the same bandgap reference circuit, a positive TC current was produced by a PTAT current circuit. Then, an adder was used to add the weighted versions of the positive and negative TC currents to obtain the current reference. Like the circuit in [1], this approach requires a startup circuit.

In [3], a current reference circuit was realized using the following components: MOSFETs, BJTs, resistors and an OPAMP. The circuit realizes a temperature coefficient of 0.7ppm/^{o}C over the operating temperature range of (-20^{o}C, 150^{o}C). A high order curvature compensation technique for current reference generation was proposed in this work. The I-V characteristics of a MOSFET were exploited to achieve a current proportional to higher orders of temperature. With the help of a bandgap reference circuit, two currents, one proportional to temperature and one proportional to the square of the temperature, were generated. Also, two other currents, one inversely proportional to temperature and other inversely proportional to the square of temperature are generated with the help of another bandgap reference circuit. The PTAT currents were used to compensate the negative TC of the CTAT currents. Polysilicon resistors were used in this design since they have a small TC when compared to that of the current reference. As this design was also based on a bandgap reference technique, this also requires a startup circuit.

In [4], the circuit was realized using the following components: MOSFETs, capacitors, resistors and an OPAMP. This design realizes a current reference with a temperature coefficient of 46ppm/^{o}C over the temperature range of (-20^{o}C, 80^{o}C). This

design is different from the previously discussed designs in that it does not use the idea of a bandgap reference. The temperature and process-compensation were achieved by utilizing the Zero Temperature Coefficient (ZTC) bias point of a MOSFET. The design consists of a voltage reference circuit, a non-inverting voltage amplifier and an output transistor. The temperature compensation was performed by combining the voltage reference circuit, the non-inverting amplifier and the ZTC characteristics of the MOSFET. The voltage reference circuit generates a constant reference voltage V_{REF} that is based on the threshold voltage of a MOSFET at absolute zero temperature. The non-inverting voltage amplifier generates an appropriate bias voltage V_{OUT}, which is an amplified version of V_{REF}, at the gate of the output transistor. Finally, the output transistor generates reference current I_{REF} independent of temperature and process variation. Sub-threshold region operation was employed for all the transistors other than the output transistor.

In [5], a current reference circuit was realized using the following components: MOSFETs, diodes, resistors and an OPAMP. This design realizes a current reference with a temperature coefficient of 9.7ppm/^{o}C over a large temperature range of (-100^{o}C, 130^{o}C). This design proposed a second order temperature compensated current reference generation with a bandgap reference circuit as the core. Instead of bipolar transistors, diodes were used for the creation of a bandgap reference. This low-temperature coefficient current reference circuit adds scaled versions of three currents: one from a PTAT current source generator, the second from a first order curvature corrected current generator, and the third from a third order temperature varying current generator. The values for the weights were chosen such that the temperature coefficient of the current

reference is minimum over a large temperature range. Polysilicon resistors were used in this design because of their high resistance and low temperature coefficient.

In [6], a current reference circuit was realized using the following components: MOSFETs, resistors and lateral BJTs. This design realizes a current reference with a temperature coefficient of 600ppm/^{o}C over a large temperature range of (-20^{o}C, 100^{o}C). This design is a CMOS current reference that is constant over PVT (process, voltage and temperature) variations. The constant current reference is given by the drain current of a MOSFET. The current reference has been compensated for the power supply and temperature variations by the usage of a PTAT voltage reference in the generation of the current reference. Also, the current reference has been compensated for process variations by exploiting the physical relationship between k' ($\mu \cdot C_{ox}$) and V_T across various process corners. In this design the inverse relationship between k' and V_T was used to generate the current reference. The PTAT voltage required was obtained using lateral BJTs in a bandgap reference configuration.

In [7], a current reference circuit was realized using the following components: MOSFETs and resistors. This design realizes a current reference with a temperature coefficient of 130ppm/^{o}C with first-order temperature compensation and 28ppm/^{o}C with a second-order temperature compensation over a temperature range of (-30^{o}C, 100^{o}C). The design proposes a new compact temperature independent current reference with second-order temperature compensation. The circuit was realized with only five MOS transistors and two integrated resistors. First-order temperature compensation was achieved by designing the circuit such that the voltage drop across the resistor is given by the sum of two terms with different temperature coefficients. One term is related to the

overdrive voltages of the transistors and this has a positive temperature coefficient. The second term is the threshold voltage of the transistor and this has a negative temperature coefficient. Thus a first-order temperature-compensated current reference was achieved by properly choosing the ratio and sign of these terms by design. Second-order temperature compensation was achieved by employing a third, independent, temperature-dependent block. A MOS inverse Widlar current mirror that provides a temperature-dependent current ratio was employed to achieve second-order temperature compensation.

In [8], a current reference circuit was realized using only MOSFETs. This design realizes a current reference with a temperature coefficient of 180ppm/^{o}C over a temperature range of (0^{o}C, 100^{o}C). The temperature compensation circuit was implemented as an all-MOS temperature-compensated current reference. The current reference was realized by generating two opposite TC currents and by adding them. A CTAT current and a PTAT current were generated with two separate self-biased circuits. Then a computing circuit was used to add these two currents in weighted proportions to obtain a temperature compensated current reference. This current reference circuit has been combined with ring oscillator delay cells for controlling the characteristics of a voltage-controlled oscillator (VCO).

The current reference circuit in [9] was also realized using only MOSFETs. This design realizes a 230nA current reference with a temperature coefficient of 108ppm/^{o}C over a temperature range of (-20^{o}C, 100^{o}C). This design proposes a low-current current reference circuit suitable for power-aware LSI applications. The design consists of two self-biasing current generation sub-circuits that are based on β-multiplier circuits. The β-

multiplier circuit is an alternative way of generating PTAT or CTAT currents, without the use of bipolar transistors. These sub-circuits use MOS resistors with different bias voltages to generate two currents, one with a positive temperature coefficient and one with a negative temperature coefficient. The difference between these two current generation sub-circuits is in how they generate their respective bias voltages. For the sub-circuit generating a positive TC current, the bias voltage is generated by a diode-connected transistor operating in the strong-inversion region. For the sub-circuit generating a negative TC current, the bias voltage is generated by two diode-connected transistors in cascode connection, one operating in the strong-inversion region and the other operating in the sub-threshold region. The current adder circuit adds the two currents with opposite TCs to produce a current reference.

The current reference circuit in [10] was also realized using only MOSFETs. This design realizes a current reference with a temperature coefficient of 16ppm/^{o}C over a temperature range of (-10^{o}C, 100^{o}C), and is based on the Zero Temperature Coefficient (ZTC) point of a MOSFET. In this design, two different gate-to-source voltages located on the either side of the ZTC point are utilized for temperature compensation. This design consists of four sub-circuits: a bias circuit, a core circuit, an adder circuit and a mirror circuit. The bias circuit provides bias voltages to ensure that the MOSFETs will operate at the desired operating points. The core circuit generates two currents with opposite temperature coefficients. The adder circuit adds the two currents to generate a temperature invariant reference current. The mirror circuit is used for mirroring the reference current.

To summarize the current reference circuits present in the literature, their performance and characteristics are presented in tabular form in Table 2.1. Most of the

Table 2.1 Summary of current reference circuits present in the literature

Design	**Components Used for realization**	**Operating Temperature range (^{o}C)**	**Temperature Coefficient (ppm/^{o}C)**
[1]	MOS, BJT, R, OPAMP	(0, 110)	50
[2]	MOS, BJT, R, OPAMP	(-40, 85)	6.9
[3]	MOS, BJT, R, OPAMP	(-20, 150)	0.7
[4]	MOS, R, C, OPAMP	(-20, 80)	46
[5]	MOS, R, Diode, OPAMP	(-100, 130)	9.7
[6]	MOS, R, BJT	(-20, 100)	600
[7]	MOS, R	(-30, 100)	28
[8]	MOS	(0, 100)	180
[9]	MOS	(-20, 100)	108
[10]	MOS	(-10, 110)	16

designs in the literature [1], [2], [3], [5], [6] include bipolar junction transistors or diodes and so they are not suitable for a MOSFET-only design. Also, these circuits are usually very complex and therefore require a large area. All the designs [1]-[7] make use of resistors. In these designs the results strongly rely on the accuracy of resistors, which are often sensitive to process variations. Other designs [8]-[10], while realized with only MOSFETs, are complicated, require large areas, or have higher temperature coefficients.

In this thesis, a current reference has been generated using a MOSFET-only circuit. The circuit is simple and was realized using only 12 MOSFET transistors. The temperature-insensitive operation was achieved by using near-ZTC operation. First, a current has been generated by using a MOSFET biased near its ZTC operating point. The

bias voltage required is generated with the help of a diode-connected MOS resistive divider. A current reference of 50µA has been designed. This generated current exhibits some temperature coefficient, either positive or negative, depending upon the variation of the bias voltage. Here, the generated current exhibits a negative temperature coefficient of 164ppm/^{o}C. This temperature coefficient is compensated by generating another current having an opposite temperature coefficient with the help of some additional blocks and adding it to the previously generated current. This new circuit is called the complete current reference circuit. The reference current generated with the complete current reference circuit has a temperature coefficient of 5ppm/^{o}C over a temperature range of (27^{o}C, 125^{o}C), which is better than most of today's MOSFET-only current reference designs.

In this chapter, techniques used for current reference generation and various designs from the literature were presented. In the next chapter, the design of a 50µA (I_{ref}) basic MOSFET-only current reference circuit that can be operated up to 125^{o}C will be discussed in detail. With the help of the simulation results, the need for the additional correction circuits is shown. In Chapter IV, the design of a complete current reference circuit is presented.

CHAPTER III

DESIGN OF BASIC CURRENT REFERENCE CIRCUIT

In the previous two chapters, the need for a current reference as well as the techniques used for current reference generation were discussed. Also, various designs from the literature were presented. This chapter presents the design of a basic 50µA (I_{ref}) current reference using a MOSFET-only circuit that can be operated up to 125^{o}C. It achieves a negative temperature coefficient of 164ppm/^{o}C. The performance of the current reference circuit is further improved by adding some additional blocks to the basic circuit, which is discussed in detail in Chapter IV.

The basic current reference circuit consists of two parts as can be seen in Figure 3.1. The two parts are the bias generation circuit and the current generation circuit. The current generation circuit generates a reference current which varies somewhat with temperature. The bias generation circuit generates the bias voltage required to bias the current source transistor in the current generation circuit. The design of each block is discussed in detail. Figure 3.2 shows the circuit diagram of the basic MOSFET-only current reference circuit.

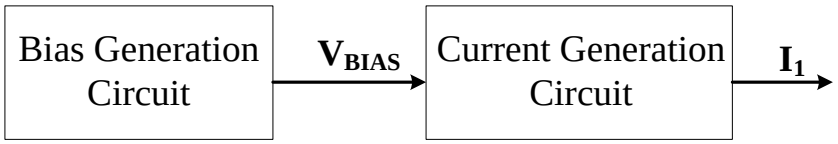

Figure 3.1 Block diagram of the basic MOSFET-only current reference circuit

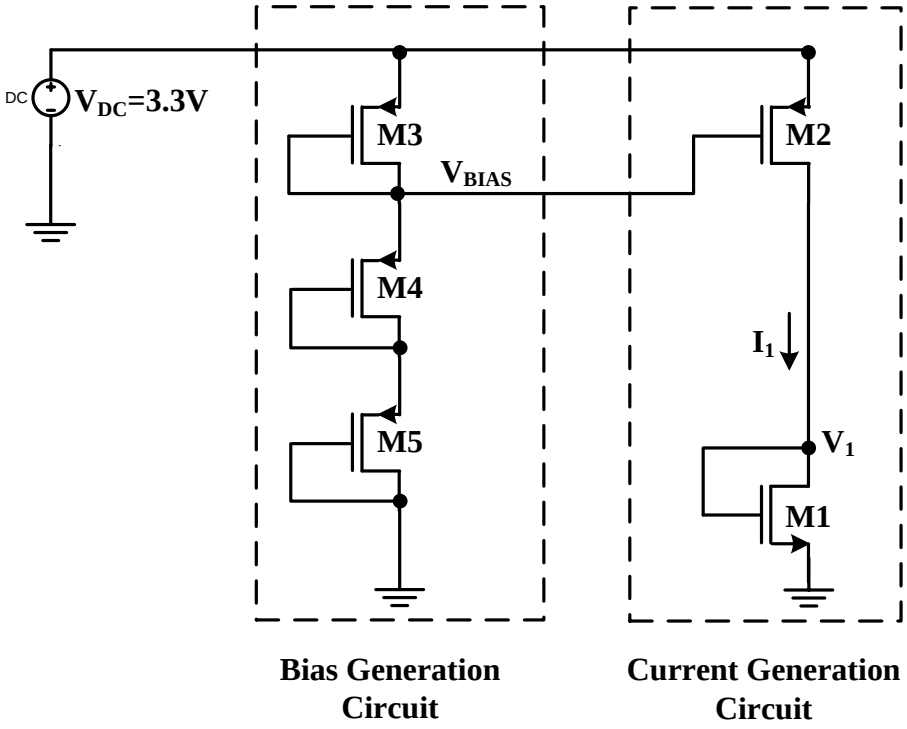

Figure 3. 2 Circuit diagram of the basic MOSFET-only current reference circuit

3.1 The current generation circuit

The current generation circuit is designed to produce a 50μA current that is invariant with temperature. At first, it is assumed that an ideal bias voltage V_{BIAS} is available; later, a circuit to create V_{BIAS} will be added.

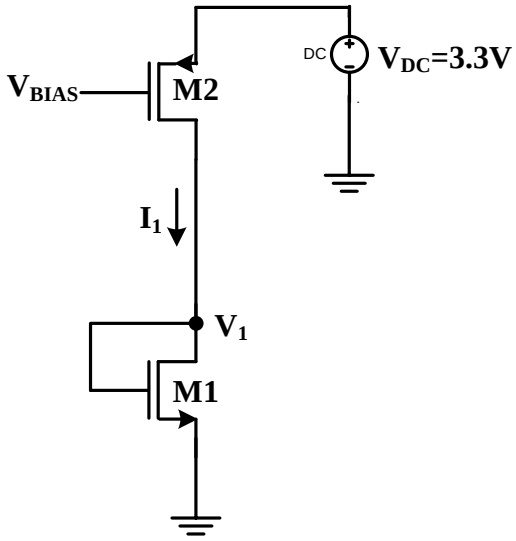

Figure 3.3 Circuit diagram of the current generation circuit

The circuit diagram of the current generation circuit is shown in Figure 3.3. It consists of two MOSFETs, both operating in the saturation region near their ZTC points. The PMOS transistor (transistor M2), can be considered to be a current source; it is placed at its ZTC point by controlling its gate voltage V_{BIAS}. The NMOS transistor (transistor M1), which is diode-connected to ensure its operation in saturation, is also biased at its ZTC point. This is achieved by sizing the transistors so that the voltage V_1 at their drains is the ZTC voltage of the NMOS transistor. A simulation was done of a single diode-connected NMOS transistor to establish the approximate location of its ZTC point in preparation for design of the current generation circuit. Figure 3.4 shows the transconductance characteristics of a diode-connected NMOS transistor with width 13.4μm and length 2μm. The same plot is shown on an expanded scale in Figure 3.5 for better visibility. The curves were plotted at 27^{o}C and 125^{o}C because those are the ends of the operating temperature range. It can also be observed from Figure 3.5 that the ZTC

point of a diode-connected NMOS transistor with width 13.4µm and length 2µm is 1.054V.

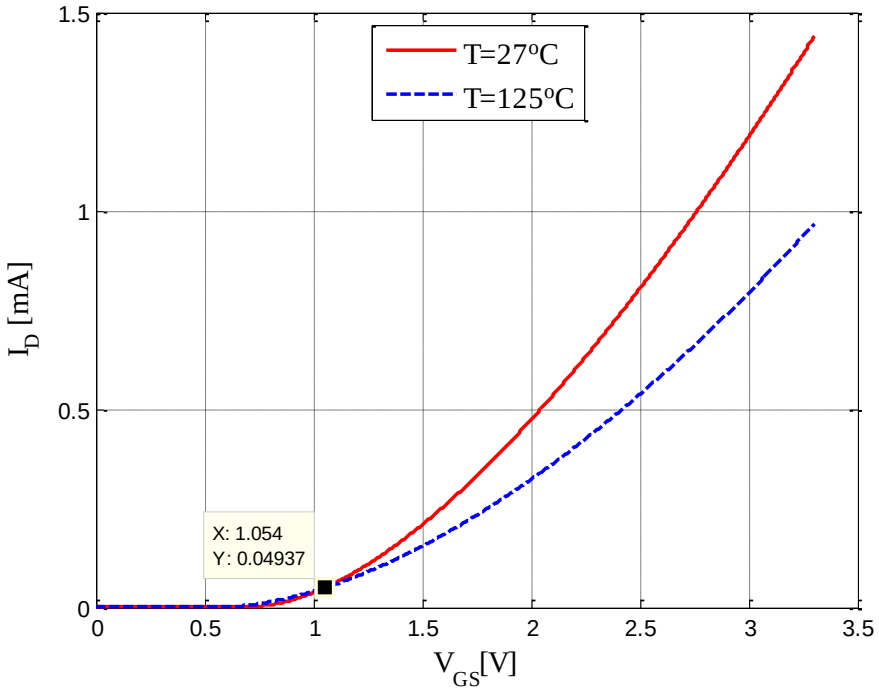

Figure 3.4 Transconductance characteristics of a diode-connected NMOS transistor having (W=13.4µm, L=2µm)

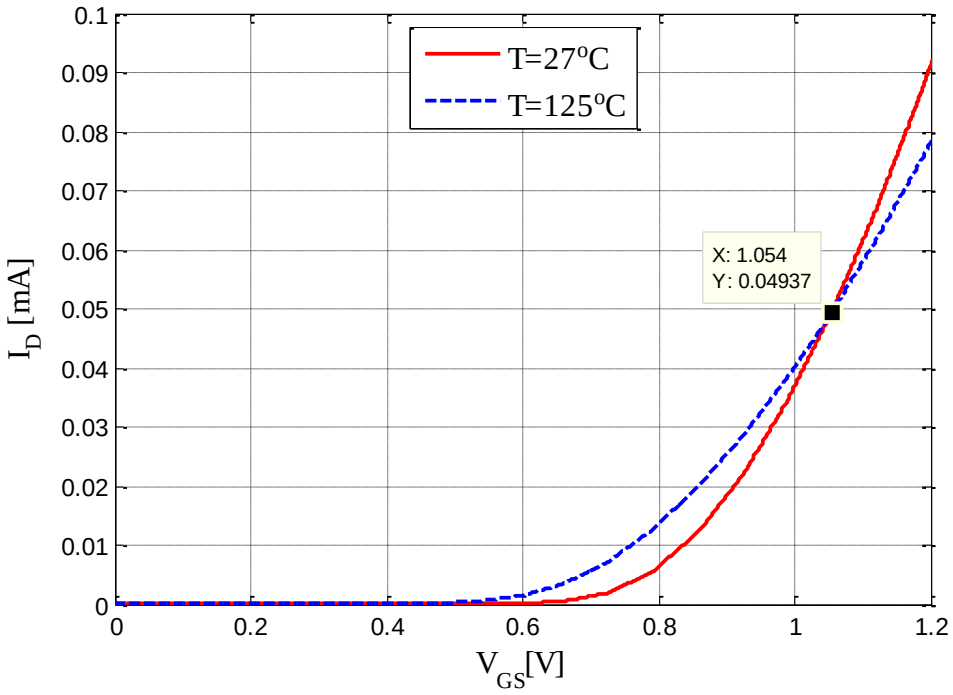

Figure 3.5 Transconductance characteristics of a diode-connected NMOS transistor having (W=13.4µm, L=2µm) (expanded scale)

For the design of the current generation circuit, the ZTC voltage of a diode-connected NMOS transistor with width 13.4µm and length 2µm is found from simulation to be 1.054V. The size of transistor M1 is chosen such that its drain current is 50µA when its $V_{GS}=V_{DS}$ is at the ZTC point of 1.054V. The simulation setup used to determine the sizing of the transistor M1 is shown in Figure 3.6. For a particular length of the transistor, the width is swept over a certain range and the I_D vs. V_{GS} characteristic is simulated. From this characteristic the size of the transistor M1 can be determined, by checking for what value of width the drain current equals 50µA. By repeating the simulation for different lengths, a set of possible sizes for transistor M1 is obtained; these sizes are shown in Table 3.1. Ideally, the ZTC voltage of a transistor is fixed with respect to the channel dimensions. In practice, however, the ZTC voltage varies as the channel length is

varied. Even though the variation is small, it is significant enough to change the bias conditions.

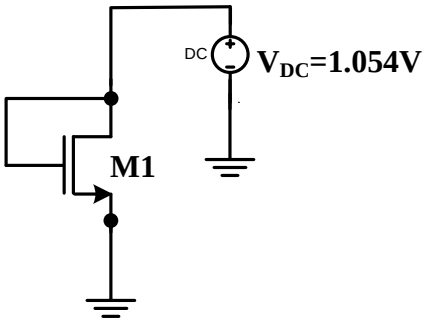

Figure 3.6 Simulation setup for determining the size of M1

Table 3.1 Set of possible dimensions (W/L) for transistor M1

M1	$\frac{6.1\mu}{1\mu}$	$\frac{\mathbf{13.4}\mu}{\mathbf{2}\mu}$	$\frac{21.3\mu}{3\mu}$	$\frac{29.7\mu}{4\mu}$

The transistor M2 in the current generation circuit in Figure 3.3 is also biased at its ZTC point so that the circuit produces a current that is constant over temperature. The ZTC voltage of a PMOS transistor with width 12.4µm and length 1µm is found to be 947mV from simulation. The size of transistor M2 is chosen so that its drain current is 50µA; at the same time, its $|V_{GS}|$ must be at its ZTC point of 947mV, and its drain voltage must be at the ZTC point of the NMOS transistor (1.054V). The simulation setup used to determine the size of transistor M2 is shown in Figure 3.7. A similar analysis as performed for transistor M1 was used for transistor M2 to determine its size. For a particular length of the transistor, the width is swept over a certain range and the I_D vs. V_{GS} characteristic is simulated. From this characteristic the size of the transistor M2 can

be determined, by checking for what value of width the drain current equals 50μA. By repeating the simulation for different lengths, a set of possible sizes for transistor M2 is obtained; these sizes are shown in Table 3.2. Now as the dimensions of the transistor M2 are varied, its bias conditions also vary but they remain close to the ZTC point of M2.

Table 3.2 Set of possible dimensions (W/L) for transistor M2

M2	$\frac{\mathbf{12.4\mu}}{\mathbf{1\mu}}$	$\frac{28.3\mu}{2\mu}$	$\frac{44.8\mu}{3\mu}$

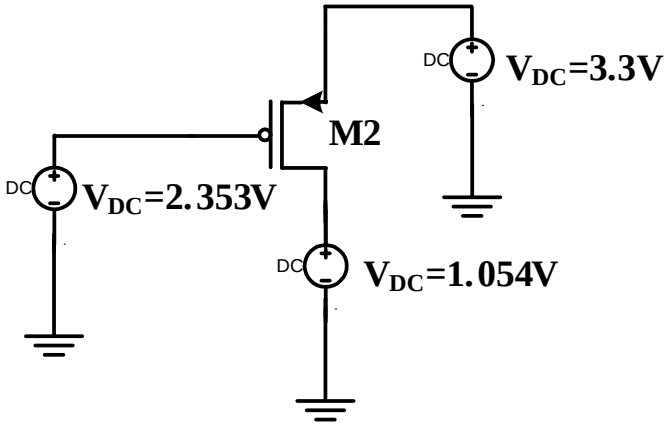

Figure 3.7 Simulation setup for determining the size of M2

Now that sets of possible sizes for both M1 and M2 are determined, one size among those in each set is to be chosen for each transistor. The exact ZTC point of a transistor varies slightly with its dimensions as well as with its drain-to-source voltage; hence, some combinations of sizes may set the two transistors more closely at their actual ZTC points. The set of sizes obtained are used for sizing the transistors M1 and M2 in the current generation circuit of Figure 3.3. An ideal V_{BIAS} is used for biasing the transistor M2 and the temperature is swept from 27^{o}C to 125^{o}C. Altogether, twelve different

combinations of sizes were tried. Table 3.3 shows the variations in current I_1 and voltage V_1 for all twelve combinations of sizes of transistors M1 and M2. The simulation results obtained for five of the combinations are shown in Figures 3.8 to 3.12.

Table 3.3 Variations in current I_1 and voltage V_1 for different sizes of M1 and M2

M1 / M2	6.1µm/1µm	13.4µm/2µm	21.3µm/3µm	29.7µm/4µm
12.4µm/1µm	ΔV= -14.98mV ΔI= -0.265µA	ΔV= -0.894mV ΔI= -0.305µA	ΔV= 1.36mV ΔI= -0.311µA	ΔV= 1.12mV ΔI= -0.310µA
28.3µm/2µm	ΔV= -27.93mV ΔI= -2.43µA	ΔV= -12.809mV ΔI= -2.454µA	ΔV= -10.347mV ΔI= -2.458µA	ΔV= -10.343mV ΔI= -2.45µA
44.8µm/3µm	ΔV= -31.16mV ΔI= -2.94µA	ΔV= -15.81mV ΔI= -2.96µA	ΔV= -13.26mV ΔI= -2.963µA	ΔV= -13.19mV ΔI= -2.9631µA

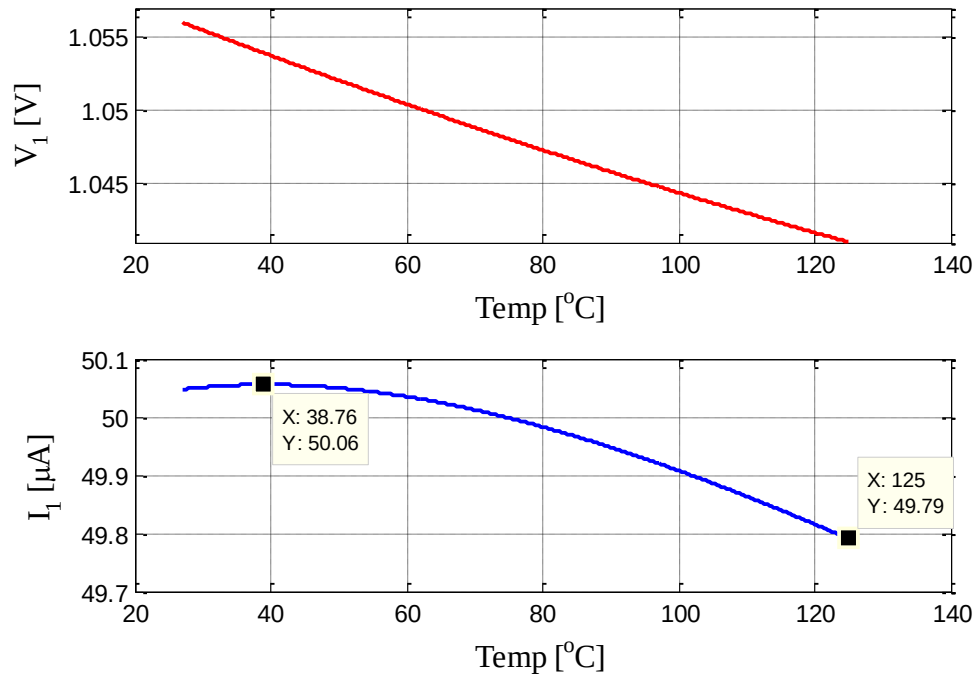

Figure 3.8 Current I_1 and voltage V_1 when M2 has (W=12.4µm, L=1µm) and M1 has (W=6.1µm, L=1µm) for current generation circuit with ideal bias voltage

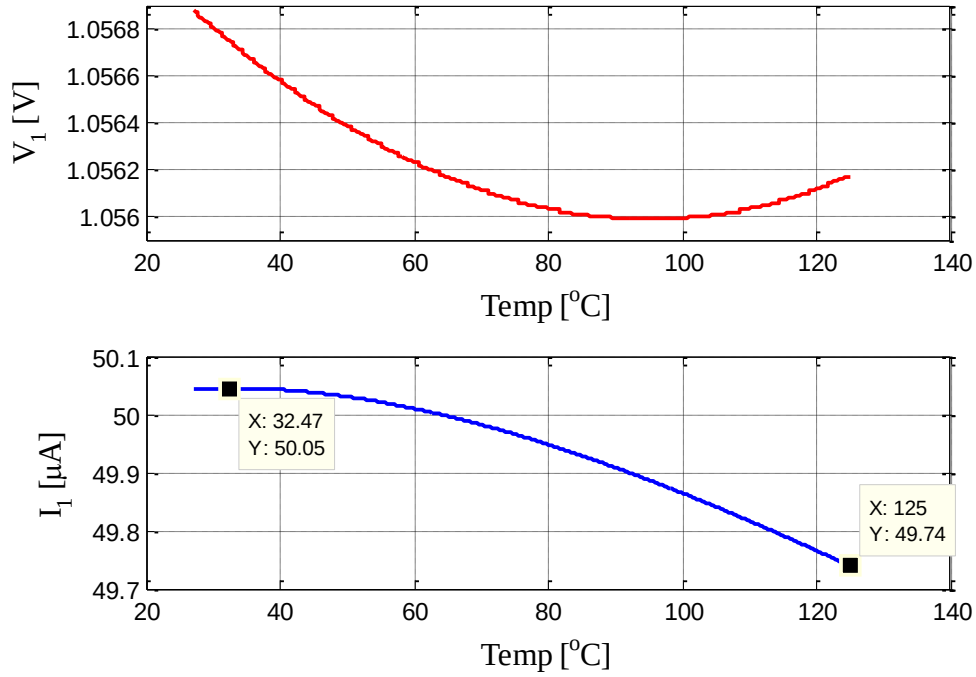

Figure 3.9 Current I_1 and voltage V_1 when M2 has (W=12.4µm, L=1µm) and M1 has (W=13.4µm, L=2µm) for current generation circuit with ideal bias voltage

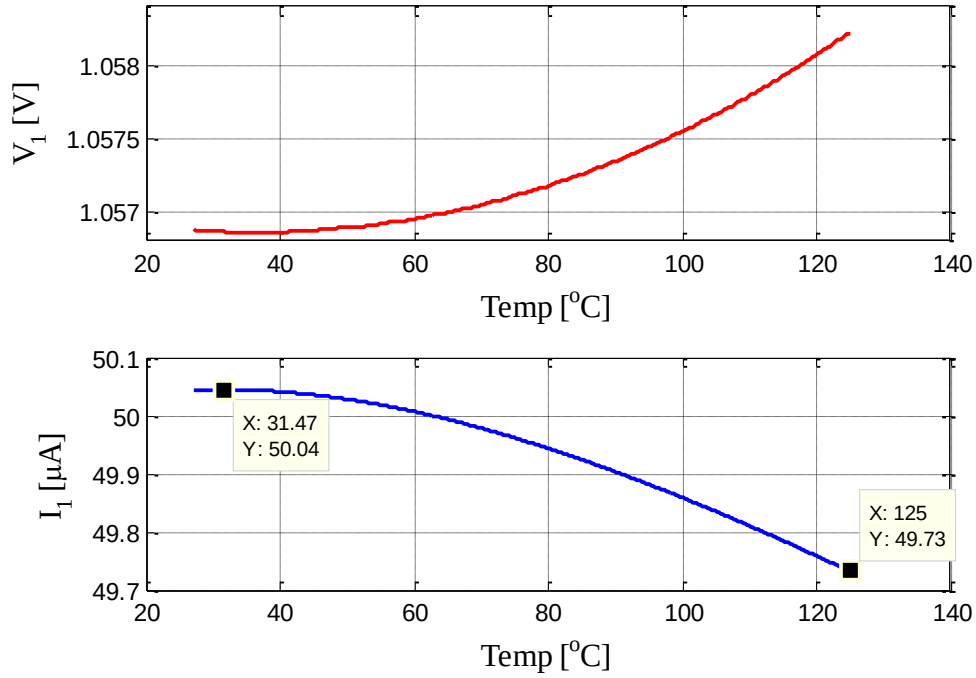

Figure 3.10 Current I_1 and voltage V_1 when M2 has (W=12.4µm, L=1µm) and M1 has (W=21.3µm, L=3µm) for current generation circuit with ideal bias voltage

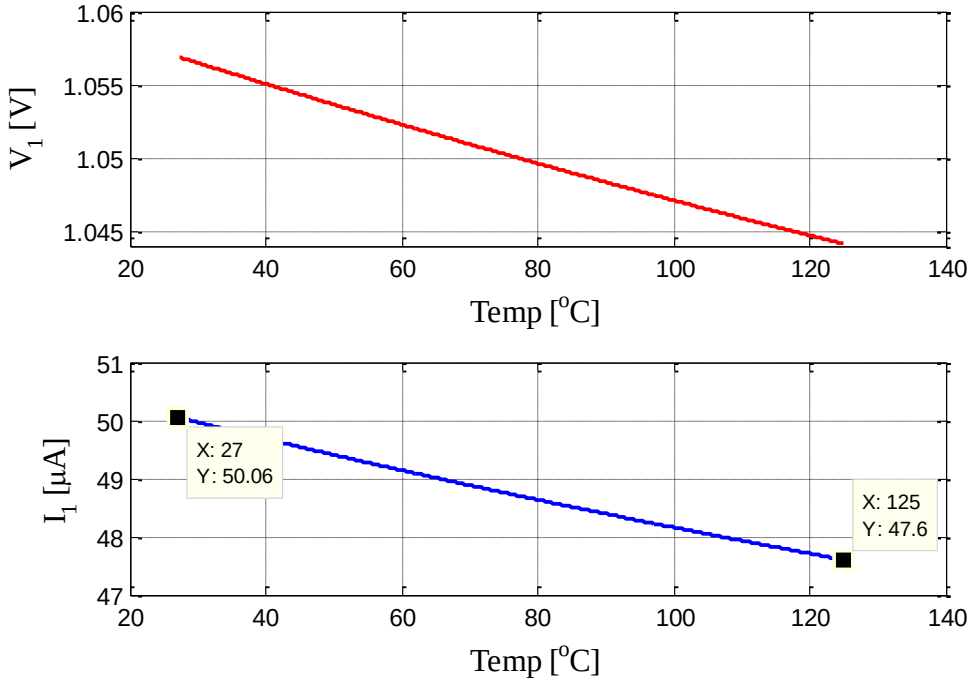

Figure 3.11 Current I_1 and voltage V_1 when M2 has (W=28.3µm, L=2µm) and M1 has (W=13.4µm, L=2µm) for current generation circuit with ideal bias voltage

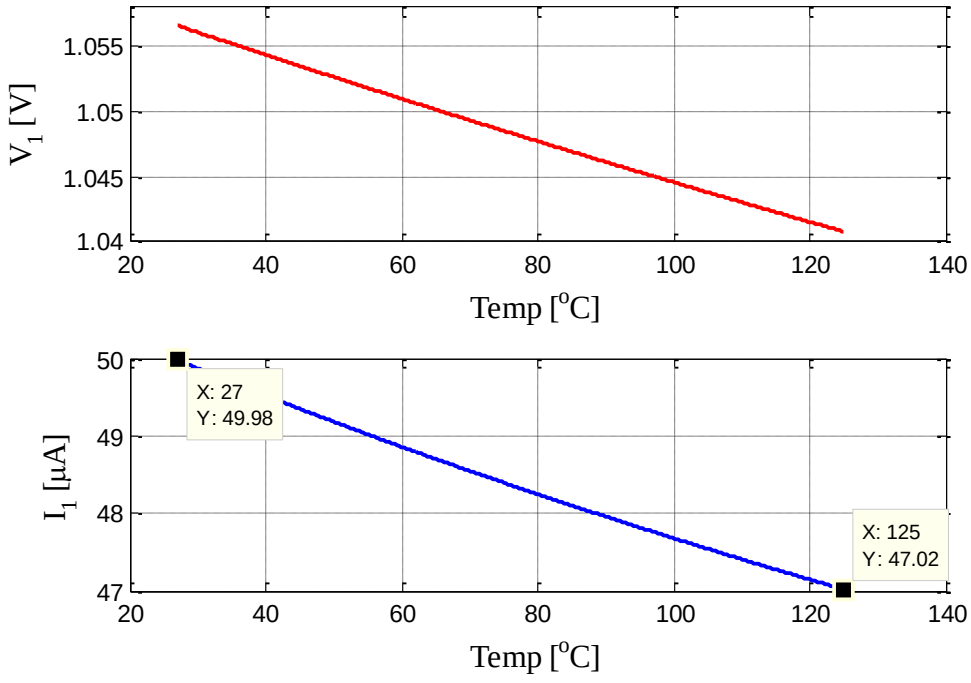

Figure 3.12 Current I_1 and voltage V_1 when M2 has (W=44.8µm, L=3µm) and M1 has (W=13.4µm, L=2µm) for current generation circuit with ideal bias voltage

From the plots, we can see how the current I_1 and voltage V_1 generated for different sizes of transistors M1 and M2 vary. In Figures 3.8, 3.9 and 3.10, the current characteristics are almost identical because M2 is the same for all the three cases; furthermore, M2 is near to its ZTC point and this leads to a small variation in I_1 over temperature. We can observe from the plots that of all the size combinations, the one shown in Figure 3.8, with M1 with width 6.1µm and length 1µm and M2 with width 12.4µm and length 1µm results in the least variation in current I_1 over the swept temperature range. However, the plot shown in Figure 3.9, with M1 with width 13.4µm and length 2µm and M2 with width 12.4µm and length 1µm has almost the same variation in current I_1 but a much less variation in voltage V_1; presumably, this is because the assumed ZTC voltages are a close match to the actual ZTC voltages for transistors of these sizes. Hence, these sizes used in Figure 3.9 were chosen for transistors M1 and M2 and these sizes are shown in Table 3.4. In the plots shown in Figure 3.11 and Figure 3.12, M1 has a width 13.4µm and length 2µm which biases M1 close to its ZTC but the variation in current I_1 and voltage V_1 are not small as M2 is not at its ZTC. Now, the design of the current generation circuit is complete. When used with an ideal bias voltage, the current generation circuit generates a current that ranges from 49.739µA to 50.045µA over the temperature range 27^{o}C to 125^{o}C, and so achieves a temperature coefficient of 62.34ppm/^{o}C.

Table 3.4 Dimensions chosen for transistors in current generation circuit

Transistor	Width(µm)	Length(µm)	No. of fingers
M1	13.4	2	1
M2	12.4	1	1

An important observation has to be made from Figures 3.8 to 3.12. It can be seen that even when the transistors are biased at their ZTC points with the use of an ideal bias voltage V_{BIAS}, there is some variation in the reference current generated over temperature. This variation is because of a previously mentioned fact: the mobility and threshold voltage temperature effects do not cancel each other exactly at all temperatures. This, and the fact that using a non-ideal voltage source to produce the bias voltage will cause the reference current to vary somewhat with temperature, will lead to the need for compensation circuitry, to be added in Chapter IV.

3.2 The bias generation circuit

In a practical implementation of the current reference circuit, it is not possible to use an ideal voltage source to produce the bias voltage for the current generation circuit; therefore, a bias generation circuit must be designed. This bias voltage should vary as little as possible with temperature. Since the ZTC voltage of the PMOS transistor in the current generation circuit is $|V_{GS}|$=947mV and the source voltage is V_S=3.3V, the bias voltage needed is V_{BIAS}=2.353V.

The circuit diagram of the bias generation circuit is shown in Figure 3.13. The bias generation circuit is a voltage divider circuit formed by three diode-connected PMOS transistors (M3, M4 and M5). The transistors were intentionally chosen to all be of the same type (PMOS); then, the characteristics of all the three transistors will vary the same way over process variations, and thus the bias voltage will not be significantly affected by the process variations. The number of transistors was chosen as three because the supply voltage is 3.3V and the bias voltage to be generated is 2.353V, which is close

to 2.2V (two-thirds of the supply voltage). If all the transistors were sized equally, the voltage obtained would be 2.2V; further, this voltage would be almost invariant with temperature because the characteristics of all three MOSFETs would vary similarly with temperature, and the variations would cancel out. To obtain a bias voltage of 2.353V, transistor M3 is made bigger than the other two. The characteristics of the transistors in the bias generation circuit are shown in Figure 3.14. It can be seen that the bias voltage is the point of intersection of the I_D vs. V_{GS} curves of M3 and M4, M5. The bias voltage has a variation of 2.5753mV when the temperature is swept from 27^{o}C to 125^{o}C.

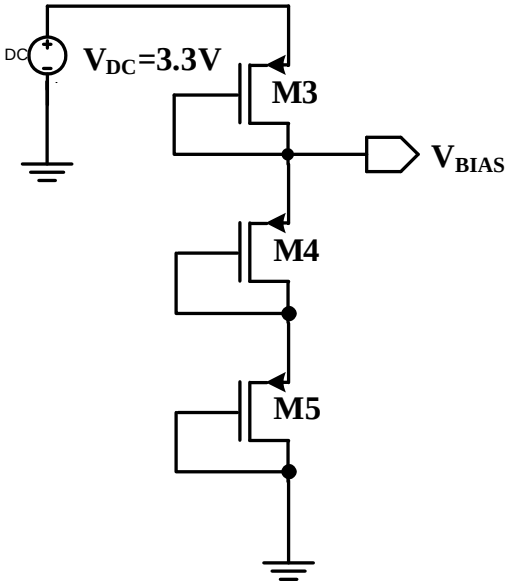

Figure 3.13 Circuit diagram of the bias generation circuit

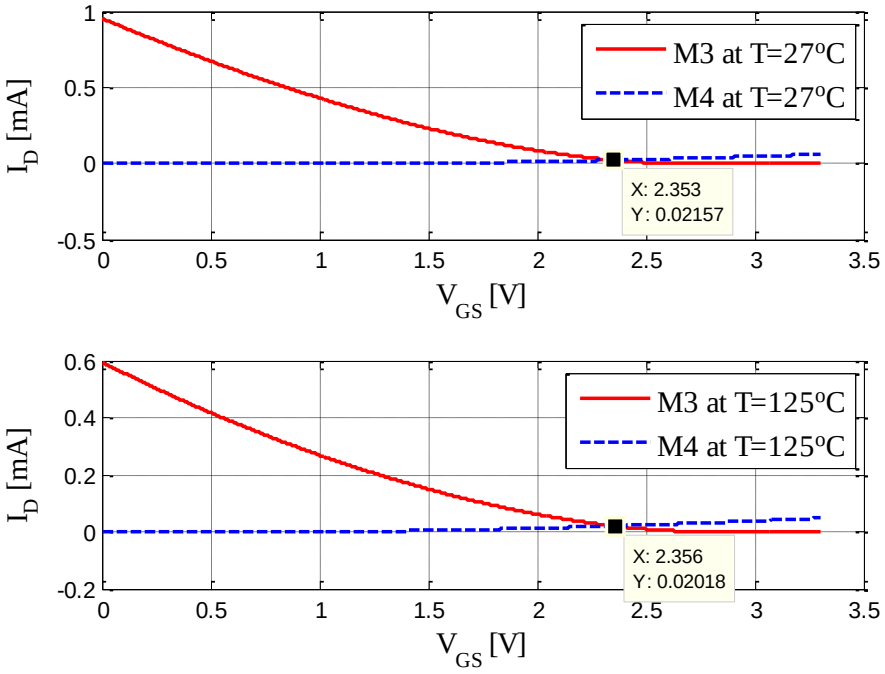

Figure 3.14 Characteristics of transistors in the bias generation circuit

Table 3.5 Dimensions of the transistors in bias generation circuit

Transistor	Width(µm)	Length(µm)	No. of fingers
M3	20.1	5.5	2
M4	1.2	0.5	1
M5	1.2	0.5	1

Table 3.5 gives the dimensions of the transistors chosen for the bias generation circuit. Transistors M4 and M5 are chosen with the default sizes. To obtain a voltage slightly greater than two-thirds of the power supply voltage, the resistance of the transistor M3 has to be decreased. We know that the resistance of a MOSFET is inversely proportional to the W/L ratio. Hence M3 is chosen to have a larger W/L ratio than transistors M4 and M5. A larger value of L was also used for M3 so that its aspect ratio could be chosen with a finer resolution. These particular W and L were chosen because going for still larger W and L did not show significant improvement in the V_{BIAS}.

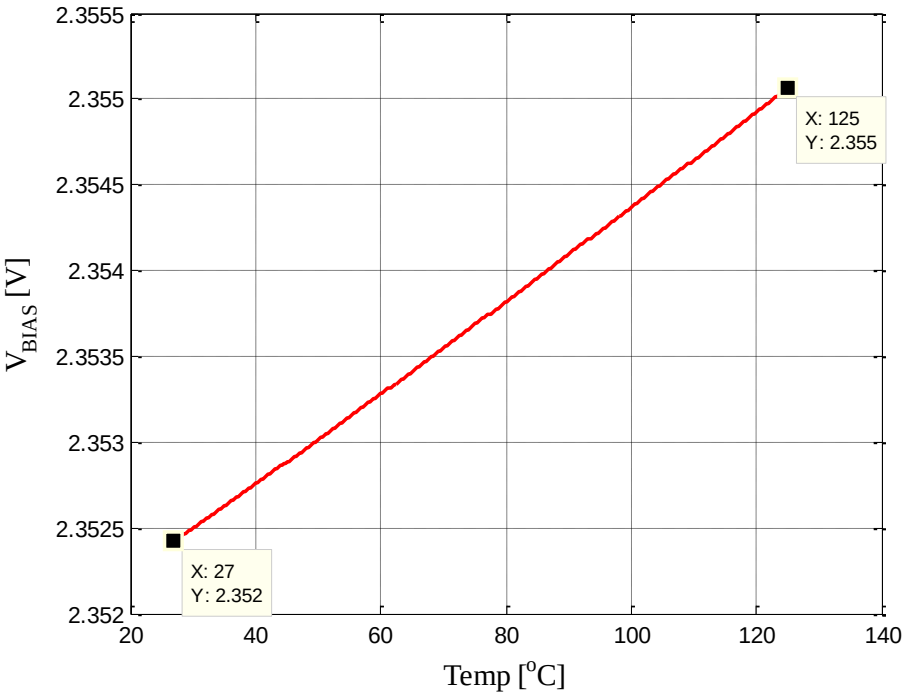

Figure 3.15 Variation in the non-ideal bias voltage over temperature

The current generated in the current generation circuit by using the bias voltage from the bias generation circuit will have some variation in it with respect to temperature. This is because the bias voltage itself has some variation in it and this causes a variation in the current generated. Figure 3.15 shows the variation in V_{BIAS} with temperature. It increases with an increase in temperature and has a variation of 2.5753mV when the temperature is swept from 27^{o}C to 125^{o}C.

Figure 3.16 shows the current I_1 and the voltage V_1 as they vary with temperature, with the bias voltage supplied by the bias generation circuit. The current I_1 has a variation of about 810nA over the temperature range 27^{o}C to 125^{o}C resulting in a negative temperature coefficient of 165.3 ppm/^{o}C. It was mentioned previously that the current reference circuit with an ideal bias voltage, produces a current having a variation of 305nA over the temperature range 27^{o}C to 125^{o}C, and so achieves a negative temperature

coefficient of 62.34ppm/^{o}C. It can be seen that after the addition of the bias generation circuit, the performance of the reference current was degraded. This is because of the 2.5mV variation in the bias voltage V_{BIAS} and the slight variation of the ZTC point. The bias voltage increases with an increase in the temperature. This causes a decrease in the gate-to-source voltage of the transistor M2. Therefore, the current I_1 has a negative temperature coefficient. To compensate for this variation, a correction circuit has to be designed.

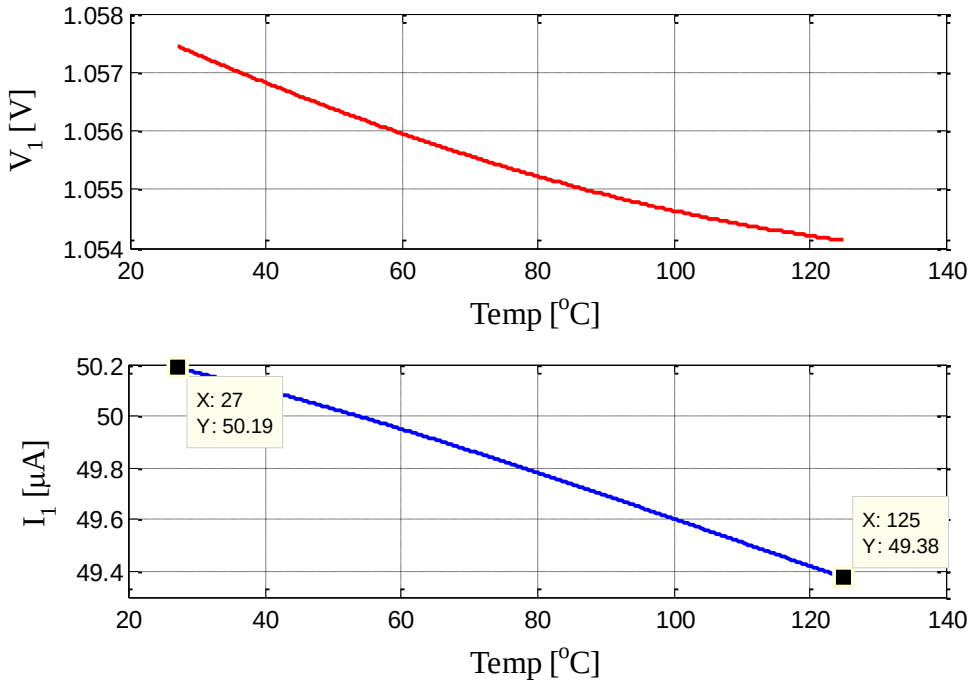

Figure 3.16 Current I_1 and voltage V_1 when M2 has (W=12.4µm, L=1µm) and M1 has (W=13.4µm, L=2µm) for current generation circuit with non-ideal bias voltage

The characteristic of the transistor M2 with the bias circuit driving its gate is plotted together with the characteristic of M1 in Figure 3.17. The point of intersection of the curves of transistors M1 and M2 determines the voltage V_1. It can be seen that the

voltage V_1 is at the desired ZTC voltage of the NMOS transistor and the current I_1 is close enough to the required value of 50µA.

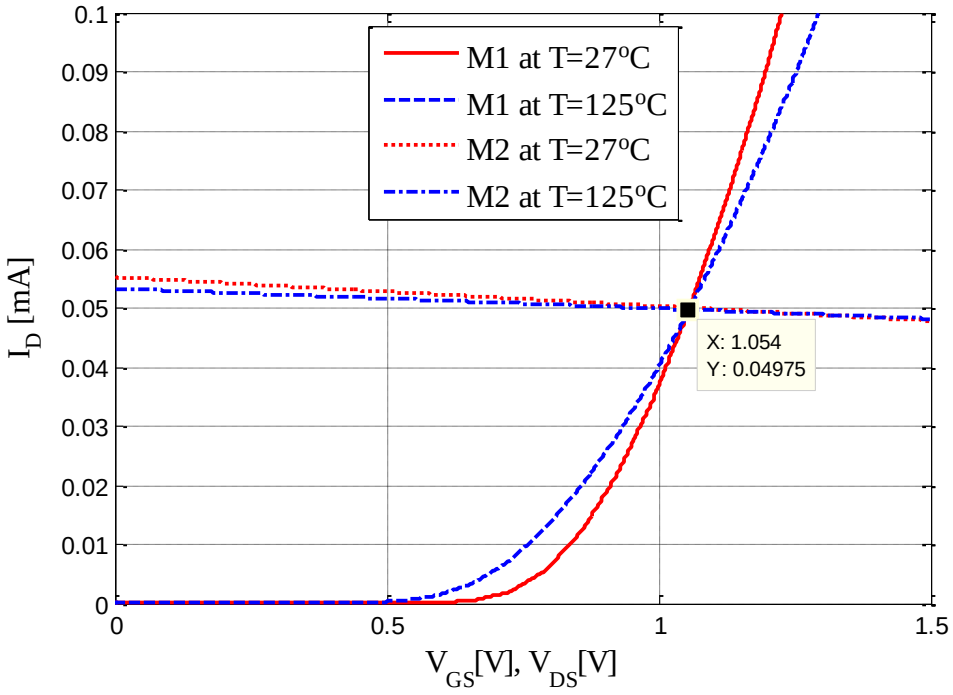

Figure 3.17 Characteristics of transistors M1 and M2

The design, simulation and performance of the basic MOSFET-only current reference circuit were presented. The current I_1 has a variation of about 165ppm/°C. In the next chapter, additional blocks will be added to the basic MOSFET-only current reference circuit to compensate for the changes in I_1 over temperature. There, the improved circuit, which is referred to as the complete MOSFET-only current reference circuit, is designed, and simulation results are discussed in detail.

CHAPTER IV

DESIGN OF COMPLETE CURRENT REFERENCE CIRCUIT

In the previous chapter the design of a basic MOSFET-only current reference circuit for generating a 50µA current reference I_1 was discussed. The basic circuit achieved a temperature coefficient of 165ppm/^{o}C. In this chapter, circuitry will be added to compensate for the variation in the reference current in the basic circuit. Two additional blocks, a correction circuit and a Widlar current mirror circuit, are added to the basic circuit. Finally, the results of the complete MOSFET-only current reference circuit are presented. Figures 4.1 and 4.2 show the block diagram and the circuit diagram of the complete MOSFET-only current reference circuit.

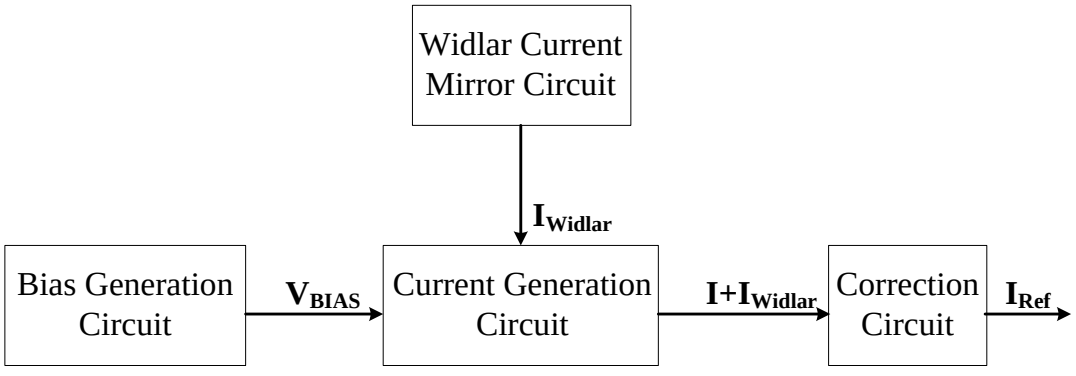

Figure 4.1 Block diagram of the complete current reference circuit

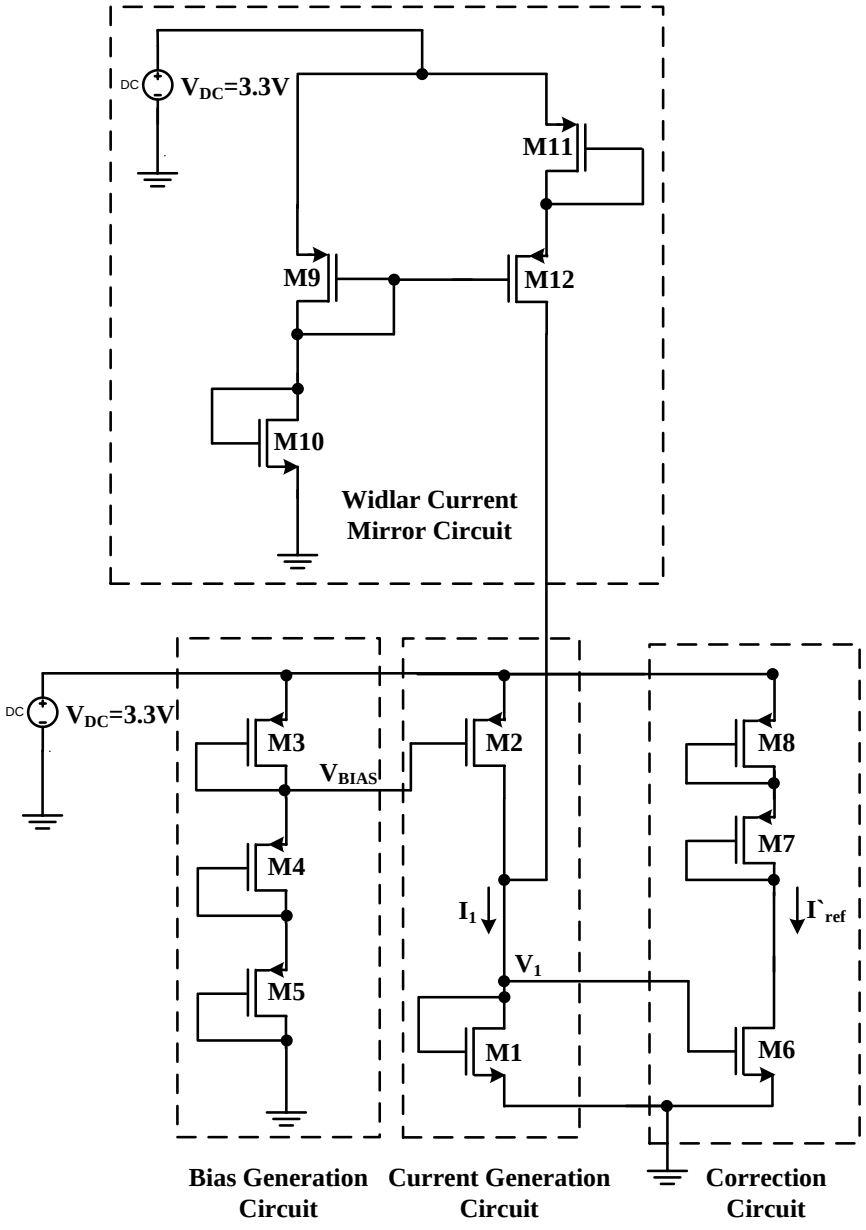

Figure 4.2 Circuit diagram of the complete MOSFET-only current reference circuit

4.1 The correction circuit

The circuit diagram of the correction circuit is shown in Figure 4.3. It consists of the three transistors M6, M7 and M8. The transistor M6 is a current mirror with respect to the transistor M1 in the current generation circuit. Both transistors M1 and M6 have the same gate voltage. However, M1 and M6 are not matched transistors; to reduce the effect of channel length modulation on the reference current, transistor M6 is made longer than M1, while having a W/L ratio that gives a current I_{ref} that matches current I_1. For a longer transistor the effect of channel length modulation will be less than that for a shorter transistor. Hence, to match I_{ref} to I_1, the ratio of W/L for M6 should be slightly larger than that of the shorter transistor M1. The transistor M6 not only mirrors the current I_1 but also helps in compensating for temperature variations in I_1, depending upon its dimensions. Because M6 has different dimensions than M1, it also has a slightly different ZTC point. As a result, M6 is biased slightly below its ZTC point, which tends to compensate for the negative TC of I_1.

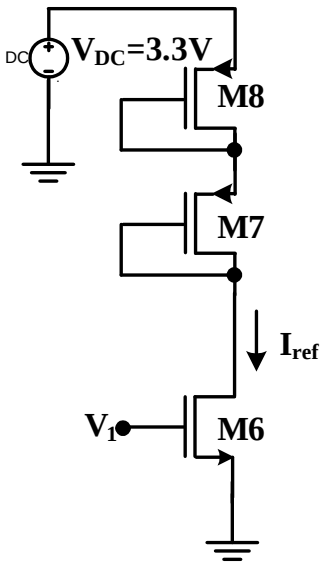

Figure 4.3 Circuit diagram of the correction circuit

As already mentioned, the current I_1 generated in the basic current generation circuit varies with respect to temperature. The current I_1 has a negative temperature coefficient, i.e., the current I_1 decreases with an increase in temperature. To counter this variation, the correction circuit is designed such that it introduces a positive temperature coefficient in the mirrored I_1 current. Hence the transistors M7 and M8 are designed such that the current through them has a temperature coefficient opposite to that of current I_1. For this case, the current through M7 and M8 should have a positive temperature coefficient to counter the variation in current I_1. To have a positive temperature coefficient for current, the transistors M7 and M8 have to be biased below their ZTC points. The transistors M7 and M8 are made wide because it is desired to operate the transistor pair far below their ZTC point to achieve high positive temperature coefficient. It would be possible to use a single transistor in place of the pair M7 and M8 to correct the temperature coefficient of the current I_1; however, a cascode is used to reduce the effect of load on the reference current when the reference current is mirrored outside of this circuit.

Table 4.1 shows the dimensions of the transistors in the correction circuit. Figure 4.4 shows the reference current before and after the addition of the correction circuit, i.e., the currents I_1 and I_{ref}. It can be seen that the variation in current has been reduced from 810nA to 80nA over the temperature range 27^oC to 125^oC with the addition of correction circuit. Before the addition of the correction circuit, it can be seen that the current I_1 has a linear negative temperature coefficient. The correction circuit tries to completely compensate for the negative temperature coefficient of the current I_1. However, the correction circuit compensates the variation in I_1 in a non-linear way and the resulting

current has a variation in the form of a parabola. With the correction circuit, the current reference circuit achieves a temperature coefficient of about 16 ppm/^{o}C.

Table 4.1 Dimensions of the transistors in correction circuit

Transistor	Width(μm)	Length(μm)	No. of fingers
M6	126	14.4	1
M7	20	1	8
M8	20	1	8

To verify that the chosen geometries place the transistors in the correction circuit at the desired operating point, the I-V characteristics of the transistors in the correction circuit are plotted. Figure 4.5 shows the I-V characteristics of the transistors in the correction circuit when transistor M6 is supplied with the voltage V_1 from the preceding current generation circuit. These were obtained by performing a dc sweep of the drain voltage of transistor M6 over the voltage range of 0V to 3.3V. It can be seen from the plots that the point of intersection of the NMOS and PMOS curves occurs below the ZTC point of the PMOS transistors, confirming the below-ZTC operation of M7 and M8 in the correction circuit. The same plots are shown on an expanded scale in Figure 4.6 for better visibility of the intersection points. It can be seen that the point of intersection of the curves of transistors M6 and M7 moves in a parabolic fashion as the temperature is increased.

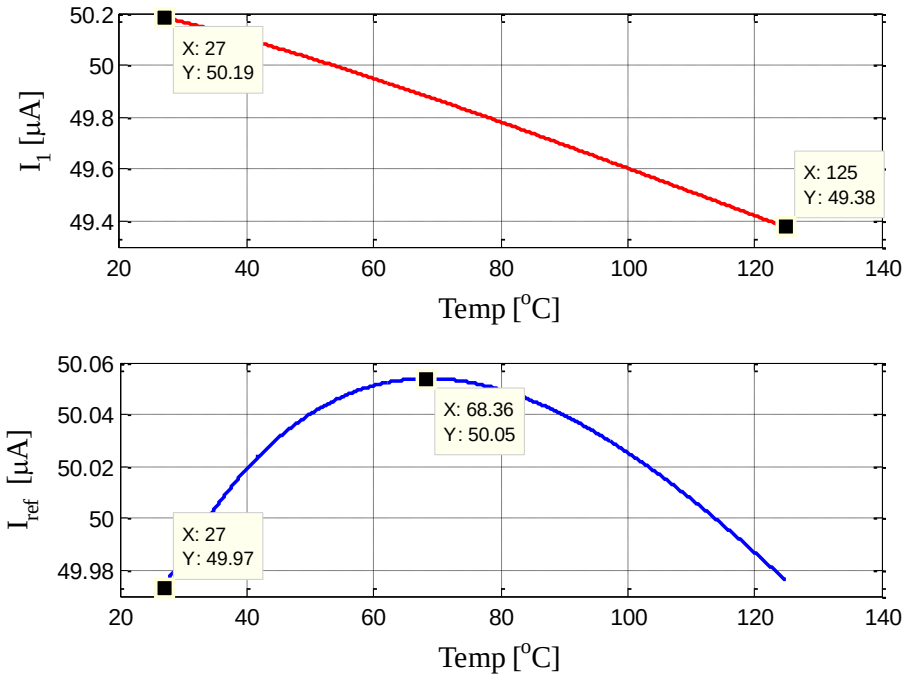

Figure 4.4 Reference current before and after correction

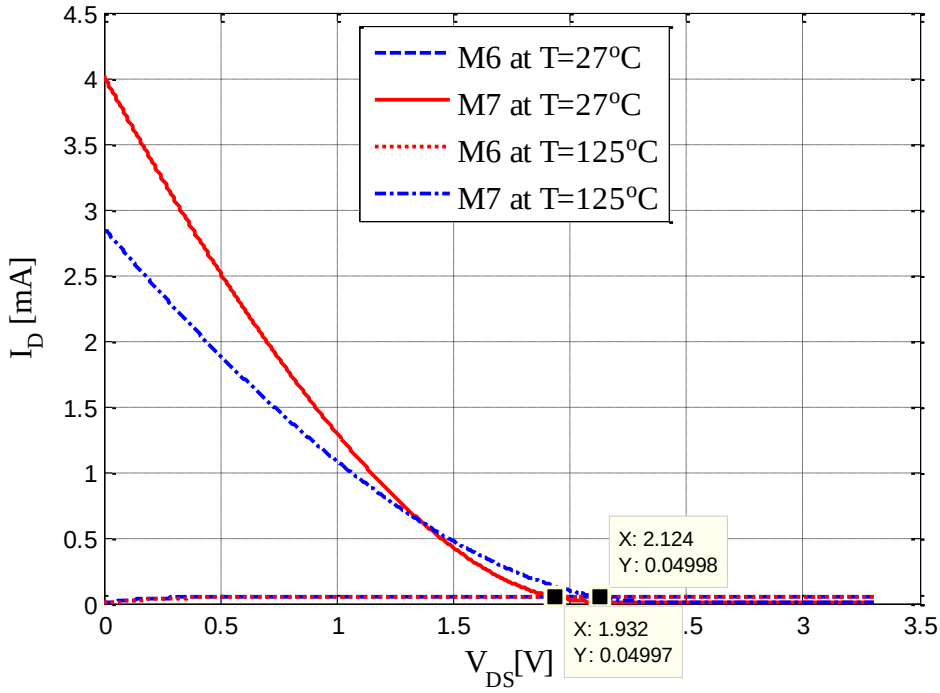

Figure 4.5 Characteristics of transistors in the correction circuit

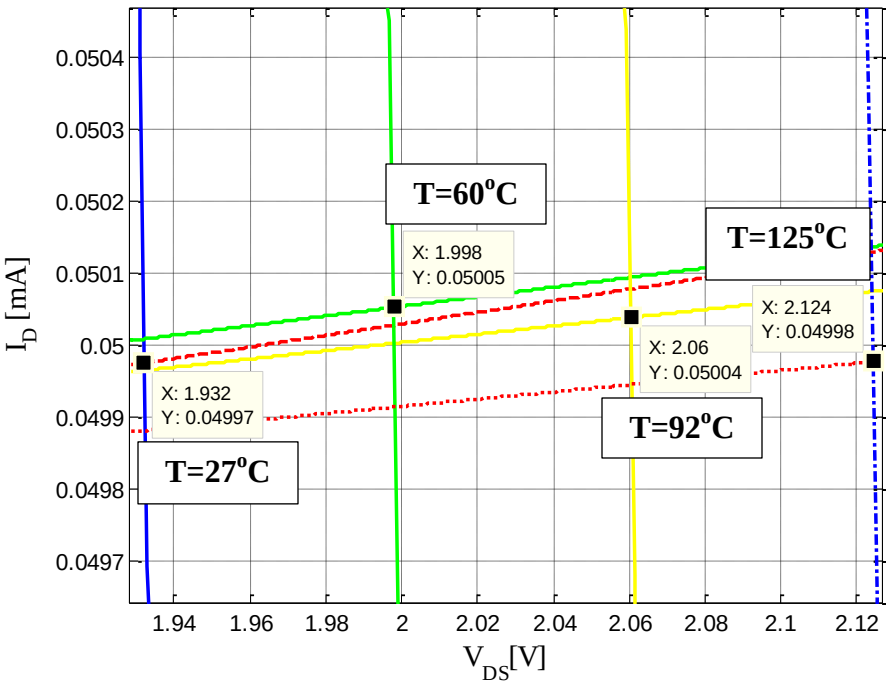

Figure 4.6 Characteristics of transistors in the correction circuit (expanded scale)

4.2 The Widlar current mirror circuit

The variation in the current is reduced to a large extent with the help of the correction circuit; however, the current I_{ref} still has some variation with temperature. This variation can be further reduced if we can reduce the variation in the current I_1 itself and then correct it using the correction circuit. The variation in the current I_1 is reduced with the help of a Widlar current mirror circuit [17], which is used to generate a small current that is added to I_1. As discussed earlier, the current I_1 has a negative temperature coefficient. The main idea here is to reduce this negative temperature coefficient of the current as much as possible by adding a current that has a positive temperature coefficient. This positive temperature coefficient current is generated using the Widlar current mirror circuit.

The circuit diagram of the Widlar current mirror is shown in Figure 4.7. It consists of the four transistors M9, M10, M11 and M12. It can be seen from the plot of the current I_1, shown in Figure 3.16 in Chapter III, that I_1 has a variation of around -800nA as the temperature is swept from 27°C to 125°C. Hence it was desired to generate a current I_{Widlar} with a positive temperature coefficient and a variation of +800nA over the temperature range of 27°C to 125°C. The circuit was designed such that the transistor M10 is operated above its ZTC point and the transistor M11 is operated below its ZTC point. Because both M9 and M10 are biased above their ZTC points, the current through the transistors M9 and M10 decreases with an increase in temperature. The gate voltage of transistor M9 is seen in simulation to increase slightly with an increase in the temperature.

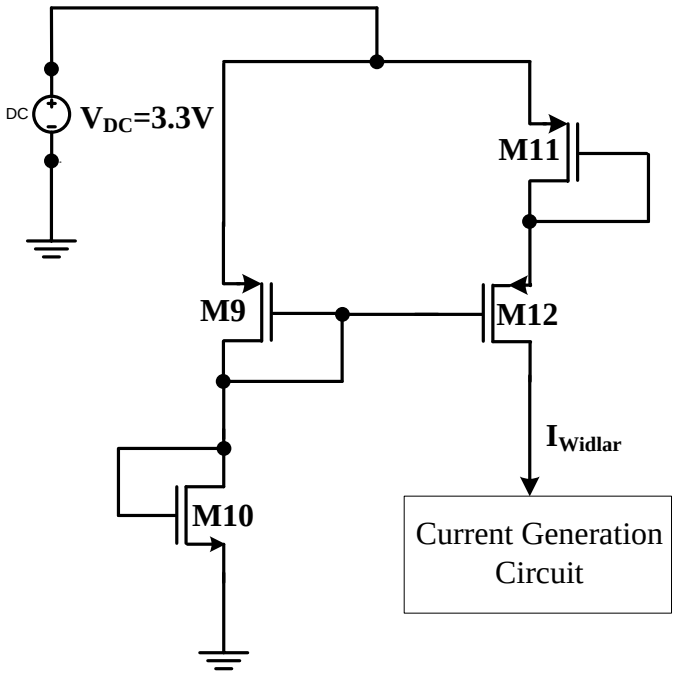

Figure 4.7 Circuit diagram of Widlar current mirror circuit

The source voltage of the transistor M12 increases slightly with an increase in temperature, leading to a slight decrease in the gate-to-source voltage $|V_{GS}|$ of transistor M11. This change has minimal effect on I_{Widlar}. The main temperature effect is an increase in I_{Widlar} with an increase in the temperature, as the transistor M11 is designed to operate below its ZTC point. The current I_{Widlar} generated here has a variation of only +755nA instead of the desired variation of +800nA because of the limitation in the resolution of the dimensions of the transistors. This current I_{Widlar} is added to the current I_1 and hence the resultant current I_1+I_{Widlar} has a variation of only -90nA.

The current I_1+I_{Widlar} is then corrected using the correction circuit as discussed previously. The only change to the correction circuit discussed in Section 4.1 is that the dimensions of the transistor M6 are now changed to W=58.4µm and L=7.4µm. This is because the variation in the current has already been reduced from 810nA to 90nA. The reference current $I`_{ref}$ with Widlar circuit after the correction has only +25nA variation over the temperature range of 27^{o}C to 125^{o}C; this corresponds to a temperature sensitivity of 5.078 ppm/^{o} C.

Table 4.2 Dimensions of the transistors in Widlar current mirror circuit

Transistor	Width(µm)	Length(µm)	No. of fingers
M9	1.2	2	1
M10	1.2	5	1
M11	1.2	0.9	1
M12	1.2	0.9	1

The design of a complete MOSFET-only current reference circuit has been discussed. The following figures show the simulation results of the current reference circuit after the addition of the Widlar current mirror circuit. Figure 4.8 shows the voltage

V_1 before and after the addition of the Widlar current mirror circuit. It can be seen that the variation in V_1 has reduced from 3.3mV to 1.8mV, because of the addition of the positive temperature coefficient current I_{Widlar} to the current I_1.

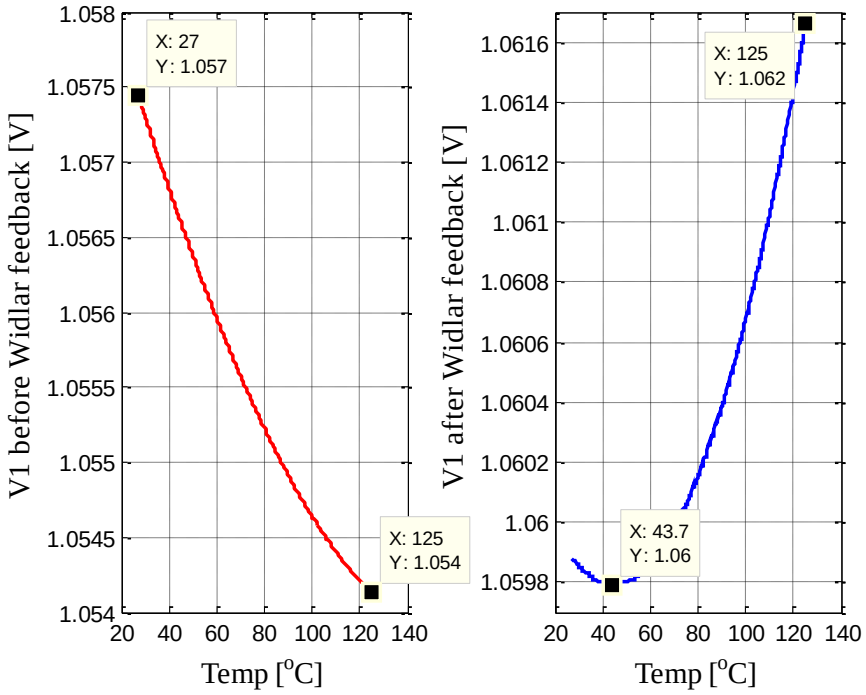

Figure 4.8 Voltage V_1 before and after adding Widlar circuit

Figure 4.9 shows the currents I_1, I_{Widlar} and I_1+I_{Widlar}. It can be seen that the current I_1 has a negative temperature coefficient and it has a variation of about 823nA. The current I_{Widlar} has a positive temperature coefficient and it has a variation of about 755nA. The resultant current I_1+I_{widlar} has a negative temperature coefficient and a reduced variation of only 90nA.

Figure 4.10 shows the currents I_1+I_{Widlar} and $I`_{ref}$. As discussed earlier, the current I_1+I_{Widlar} having a negative TC and a variation of 90nA is corrected with the help of a correction circuit. The resultant reference current has a variation of only +25nA over the

temperature range of 27^{o}C to 125^{o}C, which corresponds to a temperature sensitivity of 5.078 ppm/^{o} C.

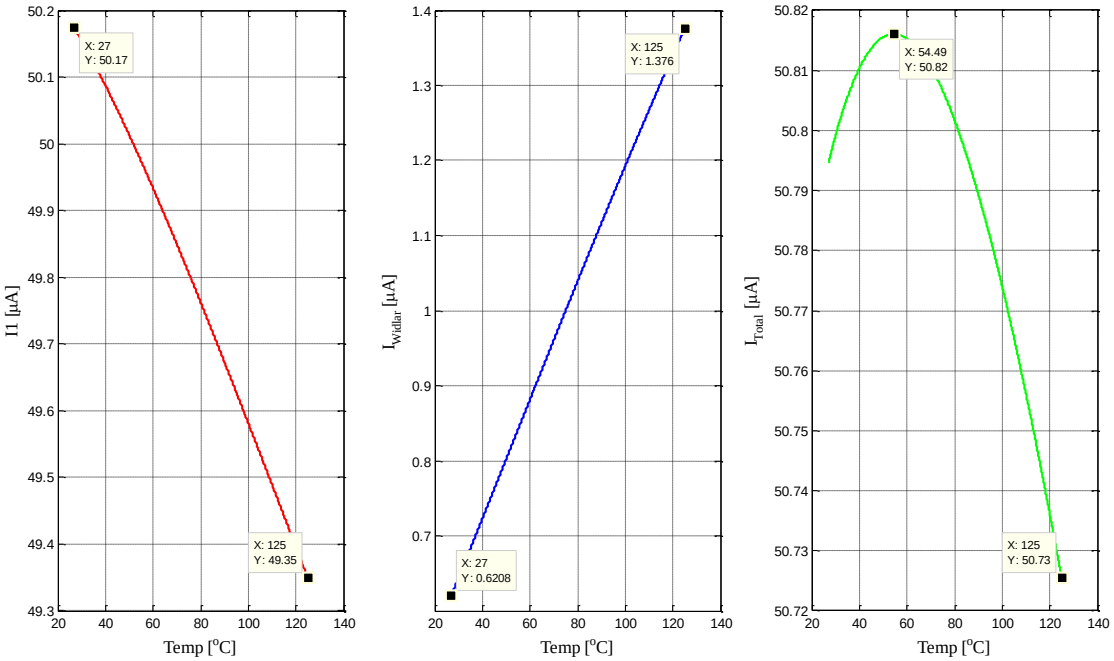

Figure 4.9 Currents with Widlar current mirror circuit

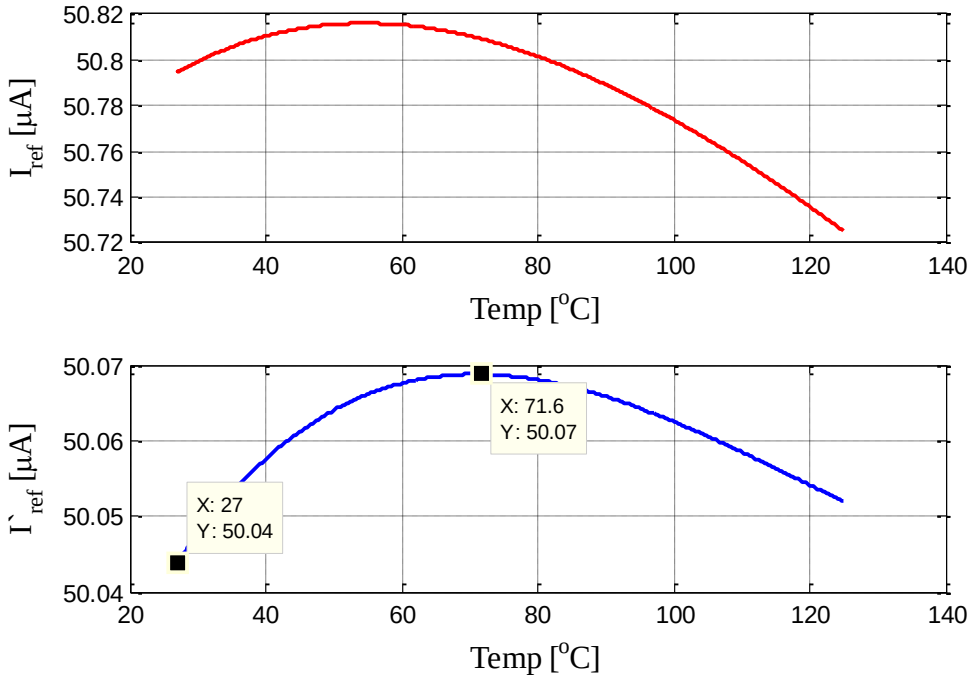

Figure 4.10 Reference current with Widlar circuit before and after correction

4.3 Analysis of sensitivity to power supply variations

A current reference should be insensitive to the variations in power supply voltage. However, in practice a current reference will have variations in it as the power supply voltage is varied. So, a small signal analysis is performed on the designed current reference circuit to analyze the effect of power supply variations on the reference current. Table 4.3 presents the transconductance ratios and the output resistances of the transistors in the complete current reference circuit of Figure 4.2. These values were determined from the simulations at the dc operating points of the transistors and are used in the small signal analysis.

Table 4.3 Transconductance ratios and output resistances of transistors in the complete current reference circuit

g_{m1}	247.8μA/V	r_{o1}	20.87kΩ
g_{m2}	252 μA/V	r_{o2}	44.65 kΩ
g_{m3}	124.2 μA/V	r_{o3}	44.02 kΩ
g_{m4}	61.56 μA/V	r_{o4}	54.64 kΩ
g_{m5}	61.56 μA/V	r_{o5}	54.64 kΩ
g_{m6}	275.4 μA/V	r_{o6}	38.56 kΩ
g_{m7}	779 μA/V	r_{o7}	13.69 kΩ
g_{m8}	779 μA/V	r_{o8}	13.69 kΩ
g_{m9}	21.8 μA/V	r_{o9}	141.4 kΩ
g_{m10}	16.1 μA/V	r_{o10}	177.7 kΩ
g_{m11}	8.6 μA/V	r_{o11}	1.18 kΩ
g_{m12}	8.8 μA/V	r_{o12}	2.42 kΩ

4.3.1 Small signal model of the basic current reference circuit

The small signal model of the basic current reference circuit in Figure 3.2 is shown in Figure 4.11. Analysis of the circuit yields the expression for current i_1 in terms of v_{dd}, assuming $g_{m4} = g_{m5}$, as

$$i_1 = \frac{g_{m1}}{1+g_{m1}r_{o2}}[1 + g_{m2}A_o r_{o2}]v_{dd} \quad (4.1)$$

where

g_{mi} is the transconductance of the transistor Mi

r_{oi} is the output resistance of the transistor Mi

$A_o = \frac{g_{m4}}{2g_{m3}+g_{m4}}$

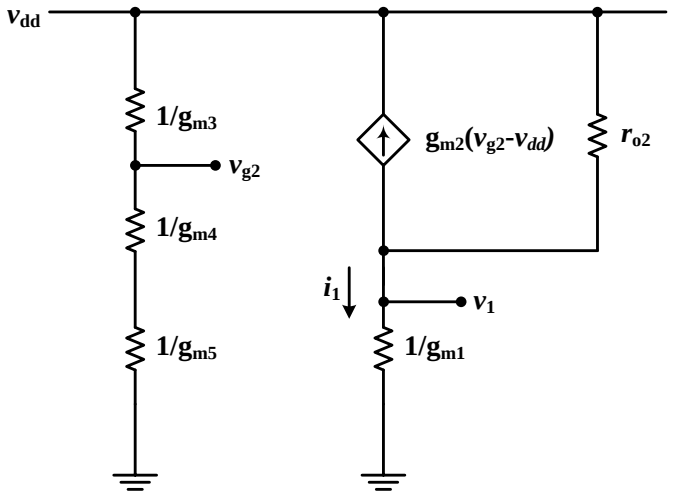

Figure 4.11 Small signal model of the basic current reference circuit

It can be seen from Equation 4.1 that the current i_1 is a constant multiple times the voltage v_{dd} and hence I_1 has a variation when the voltage V_{DD} is varied. The expression for i_1 shows the dependency of the reference current on the power supply voltage. By using the transconductance ratios and output resistances in Table 4.3, the dependency of

i_1 on v_{dd} is calculated as i_1= 66.29μA/V v_{dd}. In the following sections, a similar analysis is presented to show the effect of power supply voltage on the reference current as each additional block is added to the current reference circuit.

4.3.2 Small signal model of the basic current reference circuit with correction circuit

The small signal model of the basic current reference circuit with correction circuit is shown in Figure 4.12. Analysis of the circuit yields the expression for current i_{ref} in terms of v_{dd}, assuming g_{m4}=g_{m5} and g_{m7}=g_{m8}, as

$$i_{\text{ref}} = \frac{A_7}{r_{o6}} v_{dd} + \frac{g_{m6} A_7 (1+g_{m2} A_o r_{o2})}{1+g_{m1} r_{o2}} v_{dd} \qquad (4.2)$$

where

g_{mi} is the transconductance of the transistor Mi

r_{oi} is the output resistance of the transistor Mi

$A_o = \frac{g_{m4}}{2g_{m3}+g_{m4}}$; $A_7 = \frac{g_{m7} r_{o6}}{g_{m7} r_{o6}+2}$

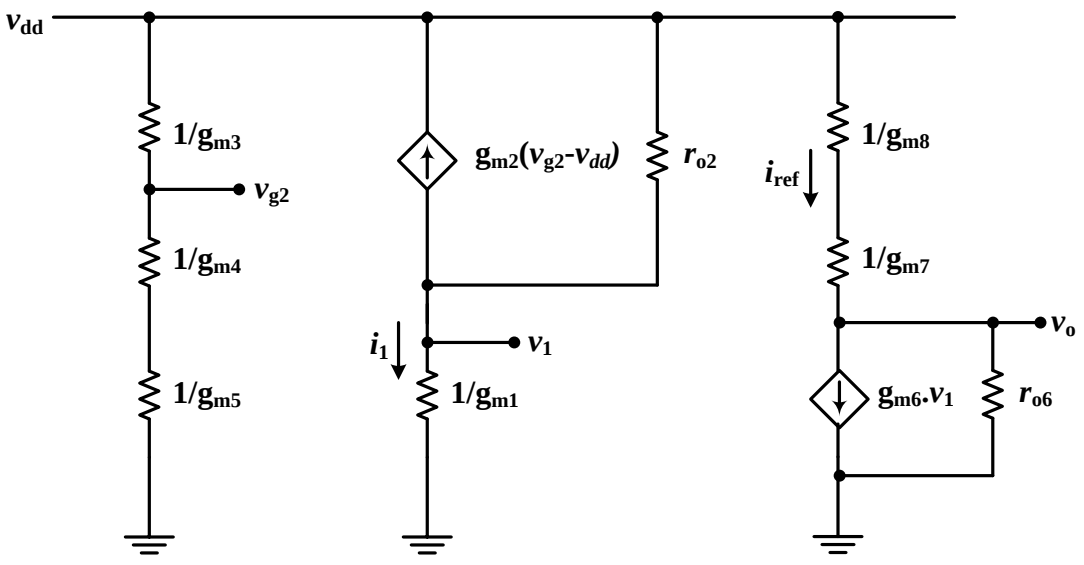

Figure 4.112 Small signal model of the basic current reference circuit with correction circuit

The expression for i_{ref} in Equation 4.2 is compared with the expression for i_1 in Equation 4.1, yielding

$$i_{\text{ref}} = \frac{A_7}{r_{o6}} v_{dd} + \frac{A_7 g_{m6}}{g_{m1}} i_1 \ . \tag{4.3}$$

It can be observed that i_{ref} is now the sum of two positive quantities. The second term of the expression is a quantity close to i_1 as the constant $\frac{A_7 g_{m6}}{g_{m1}}$=1.04 is close to 1. The first term adds a significant value to i_{ref}, because of the constant $\frac{A_7}{r_{o6}}$=24.31μA/V. The dependency of i_{ref} on v_{dd} is calculated as i_{ref} = 93.39μA/V v_{dd}. Hence, it can be observed from the expression that now the dependency of i_{ref} on v_{dd} has increased as the result of the addition of the correction circuit.

4.3.3 Small signal model of the complete current reference circuit

The small signal model of the complete current reference circuit in Figure 4.2 is shown in Figure 4.13. Analysis of the circuit yields the expression for current i'_{ref} in terms of v_{dd}, assuming g_{m4}=g_{m5} and g_{m7}=g_{m8}, as

$$i'_{\text{ref}} = \frac{A_7}{r_{o6}} v_{dd} + \frac{g_{m6} A_7 A_6 (1 + g_{m2} A_0 r_{oa} + A_3 g_{m12} r_{oa})}{1 - A_6 A_5 A_4 g_{m12} r_{oa}} v_{dd} \tag{4.4}$$

where

g_{mi} is the transconductance of the transistor Mi

r_{oi} is the output resistance of the transistor Mi

$$A_o = \frac{g_{m4}}{2g_{m3} + g_{m4}} \quad ; \quad A_1 = \frac{g_{m9}}{g_{m9} + g_{m10}} \quad ; \quad A_2 = \frac{g_{m11} r_{o12}}{g_{m11} r_{o12} + 1}$$

$$A_3 = \frac{A_2 - A_1}{1 + g_{m12} r_{o12} (1 - A_2)} \quad ; \quad A_4 = \frac{1 - A_2}{1 + g_{m12} r_{o12} (1 - A_2)} \quad ; \quad A_5 = \frac{g_{m11} r_{o12}}{g_{m11} r_{o12} + 1}$$

$$A_6 = \frac{1}{g_{m1} r_{oa} + 1} \quad ; \quad A_7 = \frac{g_{m7} r_{o6}}{g_{m7} r_{o6} + 2} \quad ; \quad r_{oa} = \left(\frac{1}{g_{m11}} + r_{o12} \right) || \, r_{o2}$$

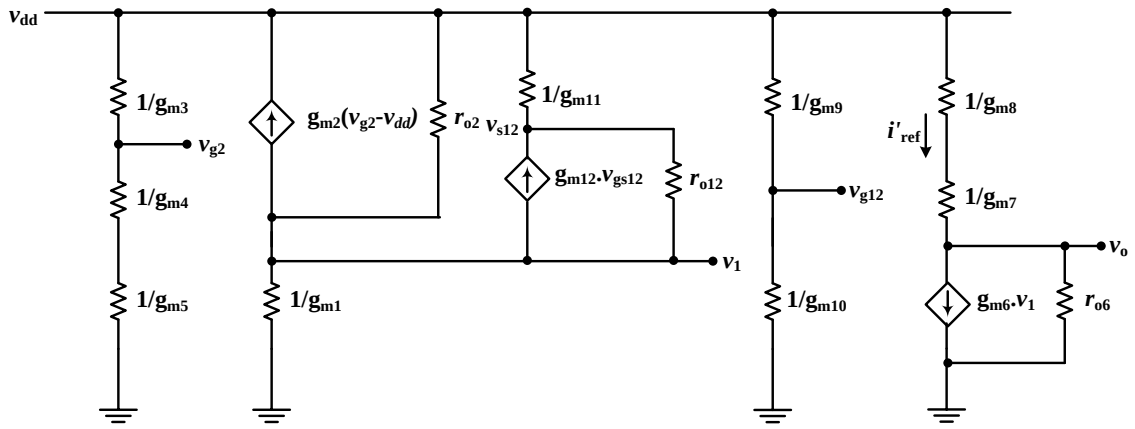

Figure 4.123 Small signal model of the complete current reference circuit

Equation 4.4 gives the final expression for i'_{ref} in terms of v_{dd}. The dependency of i'_{ref} on v_{dd} is calculated as $i'_{ref} = 95.05\mu A/V\ v_{dd}$. If we compare the Equations 4.2 and 4.4, it can be observed that only a small extra term is being added to the expression of i'_{ref}.

To complete the analysis and to get accurate numerical values, a simulation was done to quantify the dependence of the current I'_{ref} on variations in the power supply voltage V_{DD}. A transient simulation was performed to obtain the dc value of the change in the reference current for a 10% variation in the power supply voltage. Table 4.4 shows the comparison between the calculated and simulated values of the power supply rejection ratios. The values differ slightly because a linear model is considered in the small signal analysis, whereas the simulation is performed on the non-linear model.

An ac analysis is performed on the circuit in Figure 4.2 by including a sinusoidal source variation of 300mV peak value in V_{DD} and sweeping the frequency from 1Hz to 10MHz. Figure 4.14 shows the plot for power supply rejection and it can be observed from the plot that the circuit has a power supply rejection ratio (PSRR) of 84dB. The PSRR of this design is comparable to the PSRRs of the circuits given in [3] and [5],

which are 80dB and 97dB respectively. These dB quantities are calculated as $20 \times \log_{10}(\frac{i'_{ref}}{v_{dd}})$ where i'_{ref} is given in Amperes and v_{dd} in Volts.

Table 4.4 Comparison of the calculated and simulated power supply rejection ratios

Quantity	Calculated result	Simulation result
$\frac{i_1}{v_{dd}}$	66.29 μA/V	56.17 μA/V
$\frac{i_{ref}}{v_{dd}}$	93.39 μA/V	62.6 μA/V
$\frac{i`_{ref}}{v_{dd}}$	95.05 μA/V	64.7 μA/V

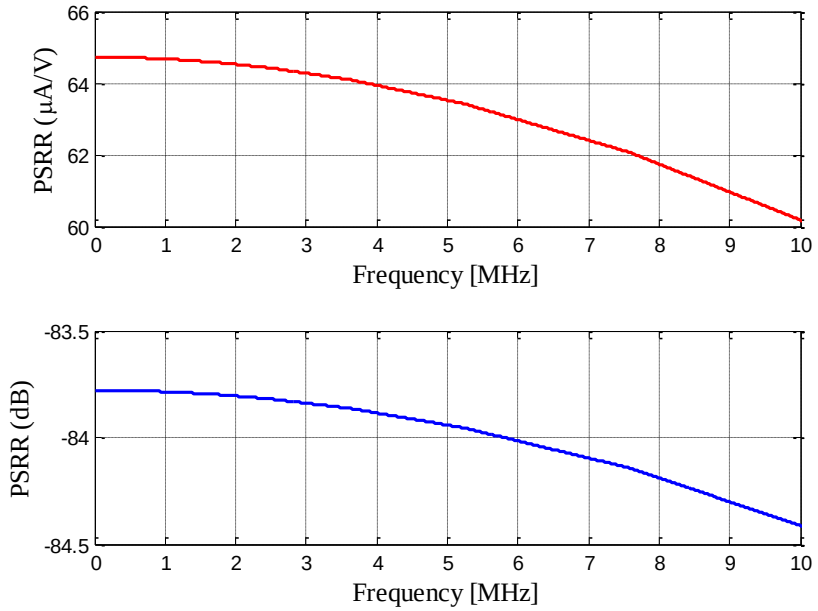

Figure 4.134 Power supply rejection ratio

4.4 Analysis of sensitivity to process variations

One of the important aspects that need to be considered is the sensitivity of the current reference to process variations. It is important because process variations cause a variation in the threshold voltage of the transistors and this variation in the threshold

voltage further causes a variation in the ZTC voltages of the transistors. As a result, the reference current varies with process variations.

The threshold voltage varies by as much as ±10% because of the process variations. This results in a variation of the ZTC voltages of the transistors. The values of the ZTC voltages of the NMOS and PMOS transistors for "slow" and "fast" process variations are shown in Table 4.5. It can be observed that the ZTC voltages vary by as much as 100mV because of the process variations.

Table 4.5 ZTC voltages of NMOS and PMOS transistors at different process corners

	Typical	Slow	Fast
NMOS (13.4µm/2µm)	(1.054V, 49.53µA)	(1.198V, 44.40µA)	(0.902V, 56.67µA)
PMOS (12.4µm/1µm)	(0.947V, 49.89µA)	(1.088V, 40.82µA)	(0.797V, 57.64µA)

Figures 4.15 to 4.18 show the reference current characteristic over temperature at the four process corners. It can be seen from the figures that the absolute value of the reference current is different from those at the nominal process corner. This variation in the reference current is because of the transistors M1 and M2 in the current generation circuit. Of these two, the major effect is because of the current source transistor M2. It becomes evident from the plots that when M2 is at a slow process corner the absolute value of the reference current drops to around 21µA and when M2 is at a fast process corner the absolute value of the reference current rises to around 92µA.

At the process corners the ZTC voltage of a transistor is different from its nominal value and hence the transistors in the current generation circuit are biased either below or above their respective ZTC points. Hence the amount of variation in reference current is

high. When M2 is at a slow process corner, it is biased below its ZTC voltage and hence it has a positive TC. Similarly, when M2 is at a fast process corner, it is biased above its ZTC voltage and hence it has a negative TC.

Sensitivity to process variations is a weakness of the design approach taken. As the reason for the poor performance of the current reference at the process corners is known, necessary action has to be taken so as to reduce the sensitivity of reference current to process variations. In general, a cascode process-insensitive bias mechanism [17] is considered to reduce the effect of process variations in current mirror circuits. However, this approach is not useful for current reference circuits, and so cannot be used to improve the proposed design. A compensation approach could possibly be developed that involves sensing the voltage V_1 and providing the required gate voltage to the transistor M6 depending upon the value of V_1 such that the reference current is less sensitive to process variations.

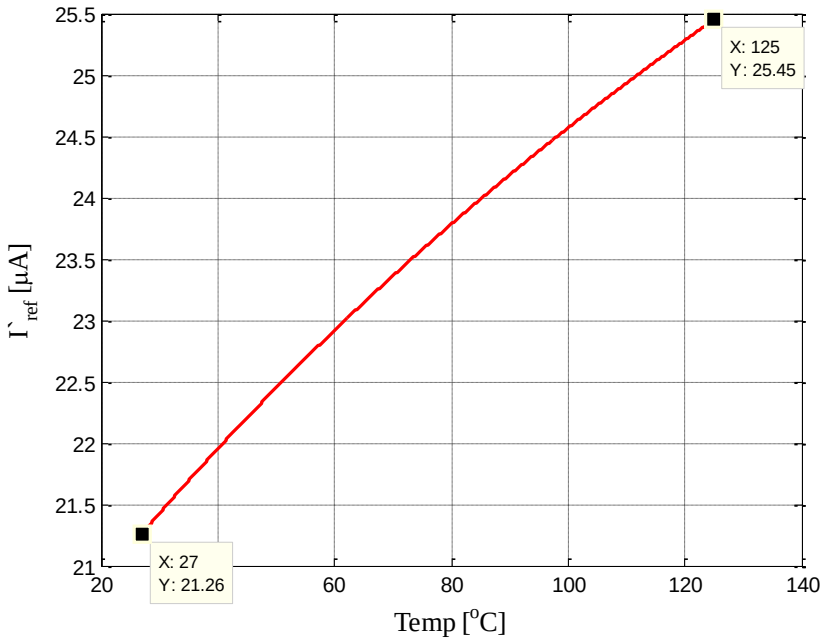

Figure 4.145 Reference current at slow-slow process corner

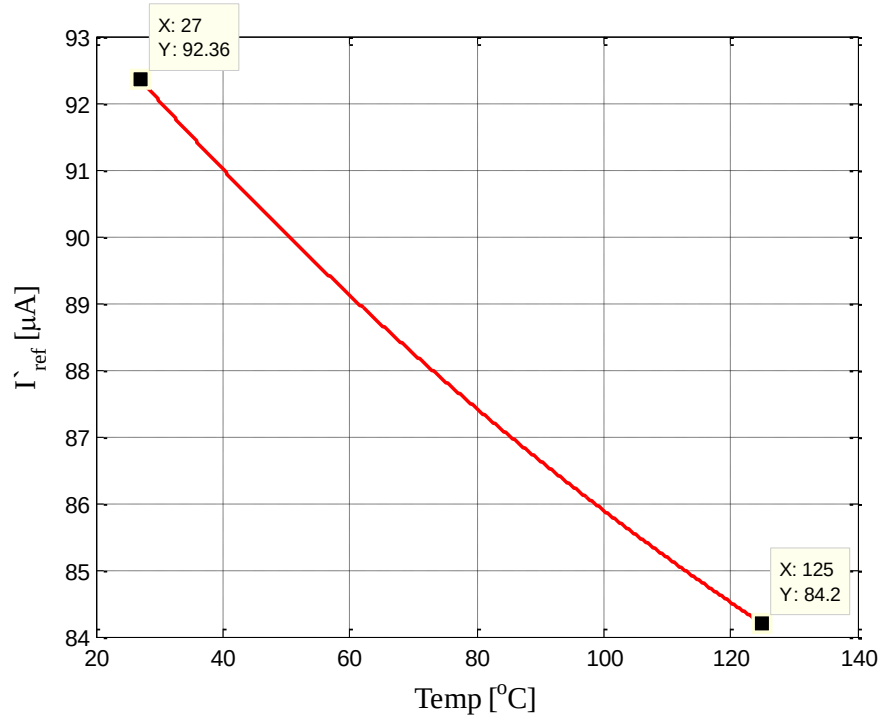

Figure 4.156 Reference current at slow-fast process corner

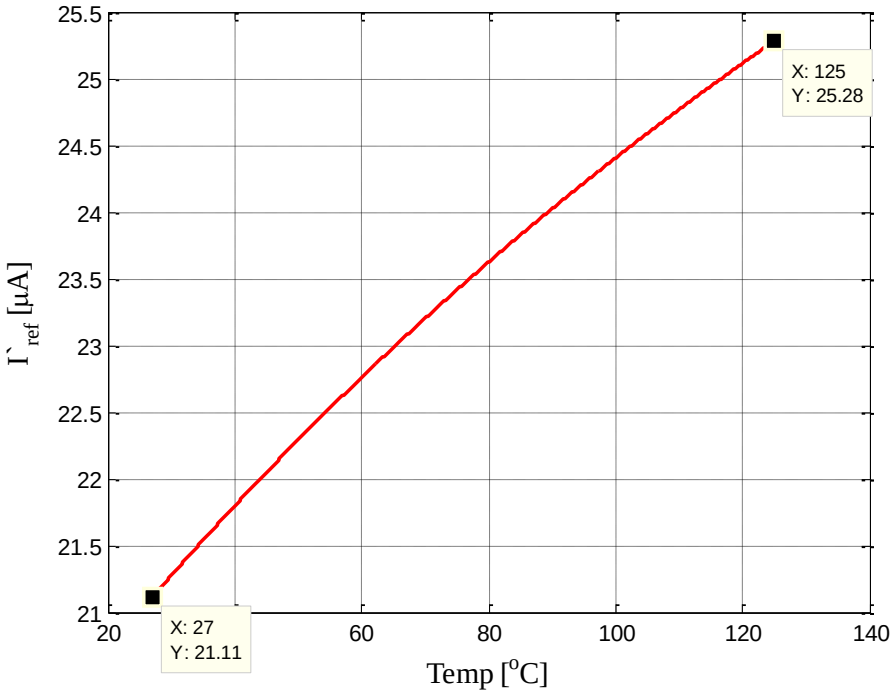

Figure 4.167 Reference current at fast-slow process corner

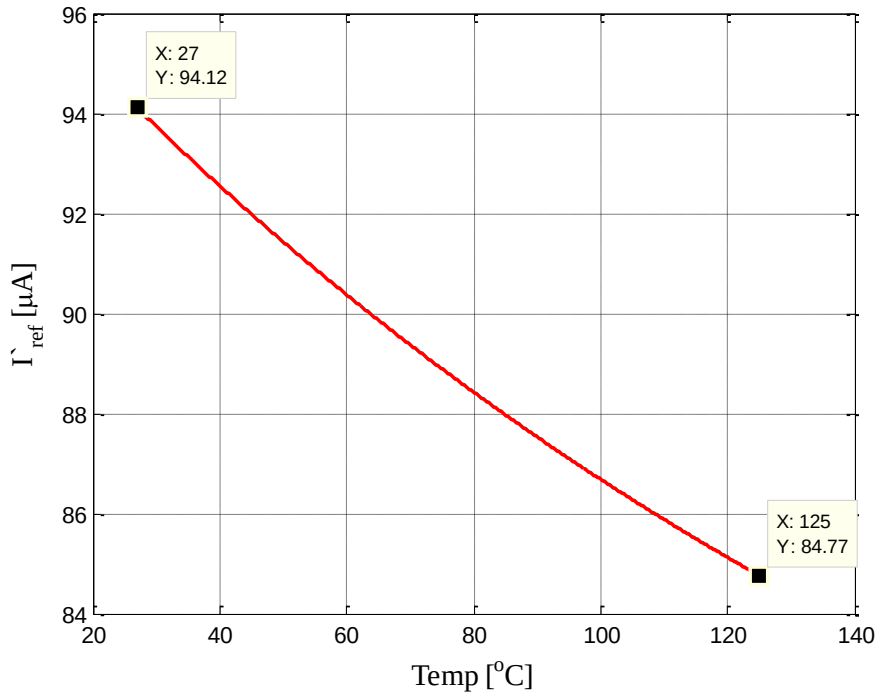

Figure 4.178 Reference current at fast-fast process corner

Now that the entire design of the current reference circuit is completed, a brief review of the design procedure is provided in this paragraph. First, the current generation circuit is designed by biasing the transistors at their respective ZTC points. Then the bias voltage required for biasing the current source transistor in the current generation circuit is generated with the bias generation circuit. Now, the behavior of the reference current from the basic current reference circuit over temperature has to be studied. Then, a correction circuit is designed to counter the effect of temperature on the reference current. Again the behavior of the reference current over temperature is studied. Now, to counter the remaining effect of temperature on the reference current, a Widlar current mirror circuit is added. This circuit is called the complete current reference circuit. Once again the behavior of the reference current over temperature is studied and the correction circuit

is slightly modified to minimize the effect of temperature on the reference current and it is observed that now the reference current has little variation over temperature.

The design of the complete MOSFET-only current reference circuit was discussed and the results of the MOSFET-only current reference circuit were presented in this chapter. In the next chapter, the conclusions derived as well as the possible future work will be discussed in detail.

CHAPTER V

CONCLUSIONS AND FUTURE WORK

5.1 Conclusions

A design procedure for the generation of a current reference using a MOSFET-only circuit is proposed. The straightforward design procedure and the simple circuit give this approach an advantage over others. Temperature insensitive operation is achieved by operating the transistors intentionally at, below, and above their respective Zero Temperature Coefficient (ZTC) points. The transistor-level circuit for the generation of a 50µA current reference is designed using the proposed design procedure, and its functionality is verified by simulation. This circuit is implemented in a 0.5µm SOI process. This 50µA current reference circuit achieves a temperature coefficient of 5ppm/^{o}C over the operating temperature range of 27^{o}C to 125^{o}C, which is better than most of today's MOSFET-only current reference designs. The proposed design procedure can be used for the generation of current references in the range of µA to mA.

5.2 Future work

Several aspects of the circuit could be considered in improving its performance further. The analysis shown in Chapters III and IV helps us in understanding the effect of

power supply variations on the reference current. Further study can be performed to more accurately analyze the effect of power supply variations on the performance of the circuit and any additional circuitry if needed have to be designed to overcome the effect of these variations.

Another aspect not addressed by the proposed design method is the performance of the circuit in the presence of process variations. Process-corner simulations have shown that the reference current is severely affected by the process variations. A compensation approach could possibly be developed that involves sensing the gate voltage of the transistor in current generation circuit and providing the required gate voltage to the transistor in the correction circuit depending upon the value of sensed voltage such that the reference current is less sensitive to process variations.

As a next step in the design flow, the layout of the proposed design can be sent to foundry for fabrication and can be tested for performance evaluation. This will help in further analyzing the effect of process variations and mismatch errors, which occur during fabrication, on the performance of the proposed design.

Finally, the performance of the circuit could be improved by replacing the simple bias generation circuit used here with a more sophisticated one. The bias generation circuit used in the design to generate the bias voltage for the current source transistor in the current generation circuit is shown to have a variation of 2.5mV in the bias voltage over a temperature range of 27^{o}C to 125^{o}C. A more sophisticated bias generation circuit whose output voltage does not vary as much with the temperature can be developed.

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