The Properties of SiC Barrier Diodes Fabricated with Ti Schottky Contacts

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Dr. Salvatore A. Sanders, Dean of Graduate Studies
ABSTRACT

Titanium (Ti) is a popular metal contact used in fabricating Schottky barrier diodes on silicon carbide (SiC) semiconductor. In this research, Ti/4H-SiC Schottky barrier diodes have been fabricated to investigate the effect of deposition temperature and annealing on the electrical characteristics of the fabricated devices. The parameters such as barrier height, ideality factor and on-resistance were determined from the current-voltage (I–V) and the capacitance–voltage (C–V) measurements at room temperature. The temperature-dependent electrical characteristics are realized by performing current-voltage-temperature (I-V-T) measurements. Furthermore, the material characterizations were performed using Auger Electron Spectroscopy (AES) and x-ray diffraction (XRD) measurements.

Thin films of Titanium (Ti) as Schottky contacts were deposited on n-type 4H-SiC substrate by magnetron sputtering at different temperatures form room temperature ~25 °C to 900 °C. In addition, thermal processing was performed by annealing at 500 °C in vacuum and argon environment up to 60 hours and characterized using I-V, C-V, and I-V-T measurements accordingly. The diodes with Ti deposited at 200 °C yield better devices with an average ideality factor of 1.04 and Schottky barrier height of 1.13 eV. The electrical properties shows that the deposition of Schottky contact should be at least below 700 °C and the Schottky contact should be annealed at 500 °C for 12-36 hours in order to obtain acceptable quality of Schottky diode. We believe that these variations in the electrical properties are due to the change in the quality of interfacial layer. The variations in physical/compositional properties of Ti/SiC interface has been investigated using Auger electron spectroscopy and x-ray diffraction, which reveled mainly two kinds of phases: Ti$_5$Si$_3$ and Ti$_3$SiC$_2$ formed at the interfacial layer.
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CHAPTER 1
SiC Properties and Summary of Current Processing Techniques

1.1 Introduction:

Silicon carbide (SiC), is one of the most prominent wide bandgap semiconductor materials known for high-temperature, high-power, high-frequency and high-radiation tolerance applications. SiC is a compound semiconductor made up of silicon and carbon. Although this material has been known for several decades, yet the semiconductor properties have been studied and implemented only in the past twenty years [1,2].

Presently, a majority of electronic applications like mobile phones, T.V., computers and several other integrated circuits are developed using silicon technology, which has limitations in the operating performance of electronic components at harsh environments and high-power applications. Silicon devices are not able to operate at temperatures above 250 °C whereas SiC devices are capable to operate from 350 °C to 600 °C junction temperature and can block voltages in the range of 300-1200 V. Theoretically such a potential led to the development of high-power and compact integrated circuit systems. Because of these superior qualities, SiC devices have a wide range of applications in power electronics like in automobile sector, information technology (IT) and consumer sector, aerospace applications, geothermal wells, oil and gas drilling, nuclear power instrumentation, space explorations and military applications. Wide range of power applications range of < 500 W to > 1 MW, at the low end the applications can be seen in computers, laptops, DC-DC converters etc. and at the high end it is grids and railway transmission. Currently SiC devices are being sold and are adopted gradually in the range between low and high power applications, i.e. for Hybrid Electric Vehicle (HEV) with different current ratings, these can be discrete devices like diodes and transistors which can further made into modules.

SiC Schottky diode is one of the most popular semiconductor devices and it is a basic building block of several electronic modules for example SBD’s are extensively used to build insulated-gate bipolar transistor (IGBT), power rectifiers and power factor correction circuits. Unlike p-n junction diode which depends on the barrier between the n-
type and p-type, Schottky diode depends on the barrier formed by the metal contact (or Schottky contact) and the semiconductor. Many SiC power devices are commercially available including Schottky barrier diode (or just Schottky diodes), junction gate field-effect transistor (JFETs or JUGFET), metal–oxide–semiconductor field-effect transistor (MOSFET) and metal–semiconductor field-effect transistor (MESFET) and are used in high-power switching applications. [3-4]

Titanium (Ti) is one of the most popular and widely used metals for Schottky contact because of its excellent adhesion on the surface of substrate (SiC) and lower specific contact resistance to the n-type material [5]. In this research, Ti/4H-SiC Schottky barrier diodes have been fabricated to investigate the effect of deposition temperature and annealing on the electrical characteristics of the fabricated devices. The processing techniques, results and analysis of this research work are discussed in the following chapters. Our group previously reported improvement of SiC Schottky diode by depositing various metal contacts at elevated temperature [6-8]. Improvements in the contacts were explained in terms of removal of unwanted oxides at the interface and the formation of silicide with higher work function.

1.2 History of SiC Development

Silicon carbide (SiC) is the only compound which is stable in Si-C equilibrium system and it is also known as carborundum. The natural form of SiC is called moissanite (a very rare mineral). This compound was first recognized by Jons Berzelius in the year 1824, he proposed the existence of chemical bond between Si and carbon. Later in 1885, Eugene Acheson introduced the growth of polycrystalline SiC, he was also the first to observe the silicide of carbon and he named the compound as SiC [9]. Since it is extremely rare to occur naturally, SiC was manufactured with several furnace techniques. Jan Antony Lely invented a new and better method for growing high quality crystals in 1955, since then SiC has become a popular semiconductor material for electronics; the first conference on SiC was held on 1958 in Boston. The major development of SiC was observed in 1978, the Lely technique was modified to use the seeded sublimation growth technique which made it possible to grow bulk crystal. Today SiC is produced in the same way as solid state
reaction between SiO\(_2\) (silicon dioxide) and carbon (petroleum coke) at high temperature in electrical furnaces [9, 10].

SiC based light emitting diodes (LED) were first introduced by H.J. Round in the year 1907 and thereafter several commercial SiC LED’s were produced, the first blue LED’s was fabricated in 1979. In 1990’s almost every basic electronic device was successfully demonstrated and the first commercial SiC devices made available were Schottky diodes and Metal Semiconductor Field Effect Transistors (MESFET). Later the SiC was used for high-power LED heat spreader and substrate for III – nitride based semiconductor devices (GaN LED’s) [10, 11].

1.3 Crystal Structure of SiC

As mentioned earlier Silicon Carbide (SiC) is a compound made up of silicon (Si) and carbon (C). Although there is a silicon in silicon carbide and silicon in elemental silicon the electrical, mechanical, and chemical properties are totally different. The basic structure of silicon carbide comprises Si (4 atoms) and C (1 atom) atoms tetrahedrally bonded, as shown in Fig. 1. The lattice constant \(a=3.08\) Å, is the distance between Si-Si atoms; the carbon atom is located at the center of tetrahedral structure bonding four Si atoms with an equidistance of 1.89 Å with each Si atom [1].

![Figure 1: Basic structure of silicon carbide.](image)

Silicon Carbide shows a special type of one-dimensional polymorphism called polytypism. This phenomenon exhibits a wide range of crystal structures of same compound called polytypes, but differ in their stacking sequence in a particular direction.
SiC can have endless number of polytypes, out of those only around 200 polytypes of SiC have been recognized and there are named based on their crystallographic structures like C-cubic, H-hexagonal, and R-rhombohedral. Some of common SiC polytypes consists of 3C, 2H, 4H, 6H, 8H, 9R, 10H, 14H, 15R, 19R, 20H, 21H, and 24R. Even though the bond lengths of each individual are closely identical, the symmetry of crystal depends on the stacking periodicity of tetrahedrally bonded Si-C bilayer [3]. The height ‘c’ of the cell varies with polytypes, for example the c/a ratio for 4H and 6H-SiC is 3.27 and 4.908 respectively.

![Figure 2: Crystal structure of SiC: (a) Wuirtzite structure and (b) Zinc blend structure](from ref 12 and 13).

The crystal structure of all the polytypes of SiC are either Wuirtzite (hexagonal) or zinc blend (cubic) structure, as shown in Fig.2. The only cubic SiC polytype (3C) has the zinc blend structure and it is classified as beta Silicon Carbide (β-SiC). The remaining polytypes (e.g. 2H, 4H, 6H, etc.) are known as alpha Silicon Carbide (α-SiC) and has the hexagonal crystal structure (Wurtzite). Si-C bilayer has only three possible orientated positions in its lattice and are denoted by A, B, C, using these notations the stacking periodicity of each polytype are identified. The bilayer sheet of Si and C atoms forms a plane known as basal plane, whereas the crystallographic c-axis direction, also called as the stacking-direction or [0001] direction as shown in Fig. 3, and also illustrates the crystal
structure and the stacking sequence of some of popular SiC polytypes. 2H-SiC has ABAB... stacking periodicity which is a true representation of Wurtzite structure. 4H-SiC composed of an equal number of hexagonal and cubic bonds and the sequence are denoted by ABCB whereas 6H-SiC consists of 1/3rd of hexagonal bonds and 2/3rd of cubic bonds, its stacking sequence is ABCACB [14]. Only 4H and 6H-SiC polytypes of SiC are commercially available in bulk crystal form. Each polytype has its own atomic environment and the impurities incorporation will have the relevant effects in the electronic transport properties of SiC.

Figure 3: Crystal structure and the stacking of SiC polytypes: a) Cubic 3C-SiC (Zinc blende structure), b) Hexagonal 4H-SiC (Wurtzite structure), c) Hexagonal 6H-SiC (Wurtzite structure) and d) Hexagonal 2H-SiC (Wurtzite structure) [from ref 14].

1.4 SiC Properties

SiC is a popular wide bandgap semiconductor material, as discussed earlier the electrical properties varies with the polytype structures. The properties are considered based on the device’s application. Wide bandgap semiconductors (SiC, GaN, diamond, and etc.) have higher bandgap energy (eV), that leads to higher breakdown electric field, so that helps the material to hold off high voltage, high temperature with low leakage current. It has very high chemical and mechanical inertness thus it can withstand extreme environments [15].
Bandgap is the energy difference between the top of the valance band and the bottom of conduction band in a crystalline semiconductor. As shown in Fig.4, the highest energy band that is filled with electrons is called valance band and the lowest unoccupied band is called conduction band. Semiconductor is neither a conductor nor insulator and the resistance of the semiconductor depends on how many electrons that are available in the conduction band so, the bandgap is the property, the energy required for an electron to excite from top of the valance band to the bottom of conduction band.

Table 1: Key electrical properties of SiC vs. Si, GaAs, GaN [from ref 15].

<table>
<thead>
<tr>
<th>Property</th>
<th>Si</th>
<th>GaAs</th>
<th>4H-SiC</th>
<th>6H-SiC</th>
<th>GaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandgap (E_g, eV)</td>
<td>1.12</td>
<td>1.4</td>
<td>3.26</td>
<td>3.02</td>
<td>3.4</td>
</tr>
<tr>
<td>Electron mobility (µ_n at 300K, cm^2/V-s)</td>
<td>1500</td>
<td>8500</td>
<td>800</td>
<td>470</td>
<td>900</td>
</tr>
<tr>
<td>Hole mobility (µ_p at 300K, cm^2/V-s)</td>
<td>450</td>
<td>400</td>
<td>115</td>
<td>101</td>
<td>50</td>
</tr>
<tr>
<td>Breakdown Elec Field (E_c, MV/cm)</td>
<td>0.3</td>
<td>0.4</td>
<td>3</td>
<td>3.2</td>
<td>3.3</td>
</tr>
<tr>
<td>Thermal Conductivity (Θ, W/cm °C)</td>
<td>1.5</td>
<td>0.5</td>
<td>3.7</td>
<td>4.9</td>
<td>1.3</td>
</tr>
<tr>
<td>Max. Operating temperature (°C)</td>
<td>300</td>
<td>400</td>
<td>1200</td>
<td>1000</td>
<td>600</td>
</tr>
<tr>
<td>Sat. electron drift velocity (V_s, 10^7 cm/s)</td>
<td>1</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>2.5</td>
</tr>
<tr>
<td>Dielectric constant (ɛ_r)</td>
<td>11.9</td>
<td>13.1</td>
<td>10.3</td>
<td>10.3</td>
<td>9</td>
</tr>
</tbody>
</table>

The important electrical properties of 4H-SiC along with some popular semiconductor device material are listed in Table 1. The bandgap of SiC varies from 3.0 to 3.2 eV depending upon the principle structure or polytype of the material and it is three times greater than Si (1.12 eV). Having wideband gap energy, SiC based devices can
sustain high temperature environment. As temperature increases more electron-hole pairs will be created due to thermal ionization and the material turns into intrinsic, hence the device fails, this is the limitation for Si devices at high temperatures. Depending on the doping the wide bandgap SiC material has an intrinsic temperature about 1000 °C. SiC has a high critical electric field for breakdown \( (E_{c,\text{SiC}} = 3 \text{ MV/cm}) \) which is ten times higher than silicon \( (E_{c,\text{Si}} = 0.3 \text{ MV/cm}) \). This property gives SiC the superior high breakdown voltage capability. Blocking voltage or break down voltage is the product of critical electrical field and width of the barrier of a device. So, SiC devices can block 10 times higher voltages than the Si devices.

Saturation drift velocity is the most important parameter for high-frequency devices. High saturation drift velocity leads to high channel current in the device. It is \( 2 \times 10^7 \text{ cm/s} \) in SiC which is twice the value of Si, hence SiC is a perfect semiconductor material for microwave devices like Schottky diodes, MESFET’s, MOSFET’s, etc. [16]. The dielectric constant of SiC is less among other semiconductor materials, which results in lower parasitic capacitance and makes the material more suitable for high-frequency applications. In addition, when high voltage and high current passing through the material, it generates heat and that heat produced needs to be dissipated, so the material must have high thermal conductivity. The thermal conductivity for 4H-SiC is two times greater than that of silicon and this quality can eliminate the need of heavy and bulky heat sinks and costly cooling systems [13].

1.5 Current Processing Techniques of SiC Devices

This section contains the details of processing techniques which are necessary to fabricate SiC based devices. The processing of SiC devices has widely developed since 1991 as the SiC substrates became commercially available.

1.5.1 SiC Bulk Growth

Production of good quality SiC bulk growth has been the most challenging problem restricting the usage of SiC for electronic applications. 6H and 4H-SiC bulk wafers are commercially available from Cree Research, Inc and ATMI. SiC sublimes rather instead of melting \( (2400 \text{ °C}) \) at fairly reachable pressure \( (10^{-2} \text{ bar}) \), it is impossible to be grown
through melt-growth seeded technique (technique applied to produced silicon wafers).
Modified seeded sublimation-growth method made it possible to grow large single crystal
of 4H-Silicon Carbide called ingot, that can be cut and polished to produce large amounts
of SiC wafer. The growth techniques involve heating SiC polycrystalline material at ~2400
°C condition to make the material sublime into vapor state and later condenses onto a cold
seed crystal of SiC. This process produces SiC single crystal into a cylindrical ingot or
boule, which grows longer at a rate of several of millimeter/hour. Generally, in this process
(0 0 0 1) is the preferred crystallographic c-axis orientation for SiC Bulk growth [17].
Various defects like micropipes, hillocks, hexagonal pits, screw dislocations, etc. found in
bulk SiC were issues that hindered the development of SiC based power devices and
integrated circuits [18]. Most of SiC electronics are not developed exactly on the surface
of sublimation grown wafer. However, the devices are fabricated on higher quality SiC
epitaxial layers, grown on top of sublimation grown substrate. There are several methods
to grow epitaxial layers such as Chemical Vapor Deposition (CVD), Molecular Beam
Epitaxy (MBE), Liquid Phase Epitaxy (LPE), etc. CVD is most commonly used method
for obtaining higher quality and throughput [19]. Typically, SiC epilayers are grown
through CVD process which are performed at temperatures between 1400 °C to 1600 °C
with pressures from 0.1 to 1 atm, that grows at a rate of few micrometer/hour [20]. CVD
process for SiC epilayer at much higher temperatures (~2000 °C) have also been reported
with higher rate of epilayer growth (hundreds of micrometer/hr) [21].

Homoepitaxial-growth, is a type of epitaxy implemented using only one material
so that the polytype of epilayer matches with polytype of substrate, step-controlled epitaxy
accomplishes this growth [22]. In this method, the grown epilayer is polished at certain
angles called off-axis angle or tilt angle (from 3-8°off with (0 0 1) of basal plane). Doping
SiC is also accomplish by using this method, whereby allowing nitrogen for n-type and
aluminum (triethyl- or trimethylaluminum) for p-type doping. Dopants such as boron and
phosphorous have also been used for p-type and n-type SiC epitaxial layer respectively.

1.5.2 Choice of SiC Polytype for Devices

4H and 6H-SiC substrates, popular among all SiC polytypes for electronic
applications, the only polytypes of SiC which can be grown in bulk form (wafers), whereas
3C-SiC is still developed on silicon substrate as a layer. The temperatures while processing are maintained below the melting point of silicon (1414 °C). 4H-SiC is widely chosen as device substrate over 6H-SiC because of its high mobility and shallower level with respect to the ionization energies of dopant as listed in Table 2 [23], which results in low on-resistance and higher current ability at a particular breakdown voltage. In addition, the higher conduction in the direction parallel to c-axis of crystallographic structure of 4H-SiC is the key reason to opt for 4H-SiC instead of 6H-SiC, and it is also favored for configuration of vertical power devices.

**Table 2:** Comparison between 4H- and 6H-SiC [from ref 23].

<table>
<thead>
<tr>
<th>Property</th>
<th>4H-SiC</th>
<th>6H-SiC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Energy Bandgap (eV)</td>
<td>3.2</td>
<td>3.0</td>
</tr>
<tr>
<td>Intrinsic Carrier-Concentration (cm⁻³)</td>
<td>10⁻⁷</td>
<td>10⁻⁵</td>
</tr>
<tr>
<td>Electro mobility at N_D=10¹⁶ (cm²/V-s)</td>
<td>⊥ c-axis: 800</td>
<td>⊥ c-axis: 600</td>
</tr>
<tr>
<td>Hole mobility at N_D=10¹⁶ (cm²/V-s)</td>
<td>115</td>
<td>90</td>
</tr>
<tr>
<td>Dopant Ionization Energy (MeV)</td>
<td>45</td>
<td>50</td>
</tr>
</tbody>
</table>

1.5.3 Doping

Methods used for doping SiC are controlled epitaxial doping and ion implantation. Conventional thermal diffusion method is not preferred for doping SiC because the process requires very high temperature (>1800 °C). Good diffusion coefficients, dopants-uniformity, less defects and controlled-doping of both epilayer and wafer (substrate) are critical for electronic device application. In the case of device, substrate with low resistivity are crucial for high-power electronics because it can lower the power-losses caused by contact-resistance and parasitic-substrate. Nitrogen for n-type and aluminum for p-type are commonly used dopants for doping SiC [3]. Site competition epitaxy is a popular epitaxy controlled doping method, quantity of the dopants into SiC crystal lattice are controlled by regulating the silicon and carbon source gases (eg. silane and propane) in processing reactor [24].

Generally selective region doping for 4H,6H-SiC is achieved by ion-implantation. Almost every SiC ion implantation process is performed at high temperature (500-800 °C)
along with patterned masking made up of high-temperature capable material. The impact of high energy ion damages the lattice structure of SiC substrate so, high-temperature annealing (1200-1800 °C) is performed after removal of mask to achieve activation of implanted dopants and to improve lattice healing [25]. Ion implantation at higher temperatures is preferred over room temperature ion-implantation because ion-implantation at lower temperatures leads to amorphized-materials.

1.5.4 Etching

Etching SiC single crystals by wet chemicals has proven to be challenging due to its chemical inertness (because of high bond strength) and also the metals (eg. Ni, Cr, Ti, Mo, W, etc.) used for mask are reactive with most chemicals. Therefore, dry etching is commonly preferred etching of SiC, Reactive Ion Etching (RIE), Inductively coupled etching (ICP) and Electron cyclotron resonance (ECR) are some of the techniques used for dry etching. RIE is most commonly used dry etching method (typically etch rates for 4H and 6H are of the order of 100’s of Ang/min.) whereas ICP and ECR are high-density plasma dry etching method (for higher SiC etch rate >1000 Ang/min) [26]. Most of RIE process involves fluorinated plasmas. Fluorinates gases (CF₄, NF₃, SF₆, CHF₃, etc.) mixed with O₂ have been implemented successfully for etching SiC [27, 28] along with etch masks (sacrificial layer) like metals to etch at desired surface of SiC substrate, the material for the etch mask is chosen as per the etch selectivity ratio [29]. Dry etching has also been carried out by using chlorine based gases (Cl₂, SiCl₄, etc.) with O₂.

1.5.5 Oxidation/Passivation

Most important property of SiC is that it is the only wideband semiconductor that can grow or get oxidized thermally at high temperature in oxygen to form Silicon dioxide (SiO₂) and this property leads way to fabricate electronic devices like MOS capacitors, metal oxide field effect transistor (MOSFET). Silicon dioxide is an insulator and act as a good quality barrier (mask), helps from diffusion of impurities in the semiconductor. In addition, SiO₂ also used as passivation layers to protect electronic devices from being exposed to the atmosphere and for packaging processes. Critical electric field of dielectric is a crucial parameter for passivation application. The main issues of reliability of an
insulator are high-temperature and high-radiation which may lead to reduction of critical field or increasing leakage current [30].

Oxidation of SiC may result in mixture of different oxide products consisting of carbon atoms and high defect density, which is undesirable. Achieving a good quality SiO₂/SiC interface layer (to avoid mixture of carbon into oxide) has proven to be challenging. The best way of passivation involves a post-oxidation annealing in nitric oxide (NO) followed by hydrogen (H₂). These gases decrease the defect density around the conduction band of SiC (4H-SiC) which is reported of the order of magnitude about 10^{12} eV⁻¹ cm⁻² (whereas for SiO₂/Si passivation interface is 10^{10} to 10^{11} eV⁻¹ cm⁻²) and mobility is 50 cm²/V-s⁻¹ [31].

1.5.6 Metal Contacts

Metal contacts are essential part of semiconductor devices. Metals are deposited to attain conduction with semiconductor or to achieve electrical interconnection among devices of same integrated circuit. Theoretically SiC devices can sustain at harsh environment (high-temperatures, high-radiations, etc.), however, this ability cannot be achieved unless the metal contacts do not fail at those conditions. Reliability and durability of the metal contacts are the main issues narrowing the possibility of operating electronics at high-temperatures. Depending on the process of metallization, contacts on semiconductor can be either rectifying or ohmic. Choosing a metal for rectifying contact will determine the barrier height of a Schottky diode and it is also very important for operating electronics at elevating temperatures. In addition, the quality of material surface and the type of metal-deposition are also crucial for device performance. The current flow mechanism of a Schottky contact and the metal used for 4H-SiC will be disused in Chapter 2.

Ohmic contacts (non-rectifying) of low resistivity are crucial for high-power, high-frequency and high-temperature applications. Usually, ohmic contacts are annealed after deposition to obtain as low contact resistance as possible. Specific contact resistance of 10⁻⁴ to 10⁻⁶ Ω cm has been reported for n-type 4H and 6H-SiC and 10⁻³ to 10⁻⁵ Ω cm for p-type [32-34].
CHAPTER 2
Silicon Carbide Schottky Barrier Diode

Silicon carbide based Schottky barrier diode (SBD) is the most important power device for its fast switching speed, low built-in voltage, large breakdown voltage and reliability in operating at elevated temperatures. These superior qualities potentially make SiC-SBD a perfect choice for applications like high-temperature, high-frequency and high-power. Because of its large bandgap, SiC-SBD’s have large turn-on voltage, at high current density (> 5000 A/cm²) and lower forward drop. However, SiC-SBD has high leakage current and high on-resistance compared to a silicon-pn junction diode at a particular voltage. Among all SiC devices, SiC-SBD is the most advanced power device in terms of development and is commercially available from 2001 with voltage range of 300-1700V by several companies [35]. It has been extensively used in power-electronic systems because of its low conduction losses and almost zero recovery time.

The Schottky diode (SBD) was named after Walter H. Schottky in the year 1938. However, the metal-semiconductor rectification was first observed by F. Braun in 1874 [35], his devices consisted of a metal point contacts to iron sulphide and lead sulphide semiconductors, these devices were used in radio wave detectors, which were later replaced by vacuum diodes in 1920s. The point contacted devices were used again during World War 2 for frequency converters and low-level microwave detectors. The point contact device technology was later examined by W. Schottky, he provided the theoretical aspects of the diode functionality. Since the point contact diodes are proven highly-unreliable, this contact was replaced by thin metallic film called planar contacts [36]. Thereafter the development in metal-semiconductor devices increased rapidly and several papers were published with variations of metals, semiconductors, and interfaces.

2.1 Schottky Contacts Used on SiC

Several metals were investigated by several authors as a Schottky contact on silicon carbide both unannealed and annealed. Table 3 illustrates the metals used on 4H-SiC polytype and their receptive barrier height ($\Phi_B$) and ideality factor. Many SiC Schottky
device prototypes have been made by researchers, yet the failure of metal contacts limiting the device lifetime to very few hours when they are operated at temperatures near to 600 °C. The contact failure was assumed to be caused by oxidation as the lifetime of the device improved to several hours when heated at 600 °C under vacuum [37].

Table 3: Schottky contacts on n-type 4H-SiC [from ref 38 and 39].

<table>
<thead>
<tr>
<th>4H-SiC face</th>
<th>Metal</th>
<th>SBH (eV)</th>
<th>Ideal Factor(n)</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>I-V</td>
<td>C-V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Si</td>
<td>Ti</td>
<td>0.56</td>
<td>1.26</td>
<td>As deposited</td>
</tr>
<tr>
<td>Si</td>
<td>Ti</td>
<td>0.91</td>
<td>1.10</td>
<td>RTA 300 °C/5min</td>
</tr>
<tr>
<td>Si</td>
<td>Ti</td>
<td>1.18</td>
<td>1.08</td>
<td>RTA 500 °C/5min</td>
</tr>
<tr>
<td>Si</td>
<td>Ti</td>
<td>1.19</td>
<td>1.23</td>
<td>RTA 700 °C/5min</td>
</tr>
<tr>
<td>Si</td>
<td>Ti</td>
<td>0.77</td>
<td>1.46</td>
<td>RTA 900 °C/5min</td>
</tr>
<tr>
<td>Si</td>
<td>Ti</td>
<td>0.95</td>
<td>1.17</td>
<td>1.02~0.20</td>
</tr>
<tr>
<td>C</td>
<td>Ti</td>
<td>1.16</td>
<td>1.30</td>
<td>1.02~0.20</td>
</tr>
<tr>
<td>Si</td>
<td>Ti</td>
<td>0.80</td>
<td>1.15</td>
<td>As deposited</td>
</tr>
<tr>
<td>Si</td>
<td>Ti/Au/Pt/Ti</td>
<td>1.17</td>
<td>1.09</td>
<td></td>
</tr>
<tr>
<td>Si</td>
<td>Ti</td>
<td>1.17</td>
<td>1.06</td>
<td></td>
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<td>1.22</td>
<td>1.23</td>
<td>1.05</td>
</tr>
<tr>
<td>Si</td>
<td>TiW</td>
<td>1.18</td>
<td>1.19</td>
<td>As deposited</td>
</tr>
<tr>
<td>Si</td>
<td>Ni₂Si</td>
<td>1.40</td>
<td>&lt;1.10</td>
<td></td>
</tr>
<tr>
<td>Si</td>
<td>Cu</td>
<td>1.60</td>
<td>&lt;1.10</td>
<td>As deposited</td>
</tr>
<tr>
<td>Si</td>
<td>Cu</td>
<td>1.80</td>
<td>&lt;1.10</td>
<td>500 °C/5min</td>
</tr>
<tr>
<td>Si</td>
<td>Au</td>
<td>1.73</td>
<td>1.85</td>
<td>1.02~0.20</td>
</tr>
<tr>
<td>C</td>
<td>Au</td>
<td>1.80</td>
<td>2.10</td>
<td>1.02~0.20</td>
</tr>
<tr>
<td>C</td>
<td>Au</td>
<td></td>
<td>1.59</td>
<td></td>
</tr>
<tr>
<td>Si</td>
<td>Ni</td>
<td>1.62</td>
<td>1.75</td>
<td>1.02~0.20</td>
</tr>
<tr>
<td>C</td>
<td>Ni</td>
<td>1.60</td>
<td>1.90</td>
<td>1.02~0.20</td>
</tr>
<tr>
<td>C</td>
<td>Ni</td>
<td></td>
<td>1.67</td>
<td></td>
</tr>
<tr>
<td>Si</td>
<td>Ni</td>
<td>1.30</td>
<td>1.21</td>
<td>1.07</td>
</tr>
<tr>
<td>Si</td>
<td>Ni</td>
<td>1.40</td>
<td>1.12</td>
<td>Measured at 20 °C</td>
</tr>
<tr>
<td>Si</td>
<td>Ni</td>
<td>1.50</td>
<td>1.12</td>
<td>Measured at 122 °C</td>
</tr>
<tr>
<td>Si</td>
<td>Ni</td>
<td>1.59</td>
<td>1.05</td>
<td>Measured at 225 °C</td>
</tr>
<tr>
<td>Si</td>
<td>Ni</td>
<td>1.35</td>
<td>1.05</td>
<td></td>
</tr>
<tr>
<td>Si</td>
<td>Ni</td>
<td>1.70</td>
<td>1.07</td>
<td></td>
</tr>
<tr>
<td>Si</td>
<td>Ni</td>
<td>1.63</td>
<td>1.10</td>
<td></td>
</tr>
<tr>
<td>Si</td>
<td>Ni</td>
<td>1.63</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Si</td>
<td>Pt</td>
<td>1.36</td>
<td>1.01</td>
<td></td>
</tr>
</tbody>
</table>
There are several factors like electro-migration, metal-contact interdiffusion, and oxidation which can lead to device failure at high temperatures. So, the reaction between metal-metal and metal-semiconductor are critical in the performance of Schottky contacts under harsh environments. The amount of research on metal failure mechanism in silicon carbide is little less compared to Si and other compound semiconductor (III-V) devices, especially in the case of high-temperature degradation studies. It has been stated that the choice of metal, SiC polytype and the annealing-temperature play a huge role in determine the Schottky barrier height ($\Phi_B$) [37].

In this study, Titanium (Ti) was used as a schottky contact on 4H-SiC. Even though there are several papers reported on metal/3C-SiC and 6H-SiC, there has been comparatively less research on metal/4H-SiC. Various metals like Pb, Au, Pt, W, Ti, Ni, etc., have been used for ohmic and Schottky contacts, out of which ‘Ni’ is commonly used for ohmic metal-contact. It behaves as a perfect (low contact resistance) ohmic contact after annealing at high-temperature. Ti is a popular Schottky contact because of its low barrier height which results in low forward-voltage drop ($V_F$) to decrease power-dissipation [38]

2.2 Theory of SBD Operation

As discussed in the section 1.5.2, 4H-SiC is widely used for electronic device application compared to 6H-SiC, therefore the semiconductor (substrate) for this study will be n-type doped 4H-SiC, Titanium is used as Schottky contact (metal). The potential barrier between metal-semiconductor junction can be realized using electron energy band diagram. Fig. 5 shows the energy band diagram of the metal and semiconductor which are aligned using same vacuum level. Vacuum level is the energy of free electron having zero-kinetic energy and it is used as the reference level [37, 40].

The metals are characterized by its work function ($\Phi_M$), the energy required to remove an electron from the fermi level of metal to the vacuum level. Similarly, ‘$\Phi_S$’ is the work function of semiconductor. Ideally, the metal contacts on semiconductor shows rectifying behavior if the metal work function is greater than work function of semiconductor ($\Phi_M > \Phi_S$) and if $\Phi_S > \Phi_M$ it behaves ohmic, which results in linear I-V characteristics. Because the semiconductor fermi level varies with the doping, a better way
of characterizing it is by using ‘\( \chi_s \)', the electron affinity. It is the energy difference between vacuum level and lower conduction band and it does not depend on doping the doping.

**Figure 5:** Energy band diagram of metal-semiconductor before contact.

The electron affinity (\( \chi_s \)) and the work function \( \Phi_M \) and \( \Phi_S \) are expressed in eV (electron volt). The value of electron affinity for SiC is 4.17 eV and the metal work function may differ depending on the intermetallic compound formed between the Schottky junction [14]. When the metal-semiconductor are brought in contact, the fermi level of both metal and semiconductor do not change immediately as shown in the Fig. 6. In addition, there will be a barrier formed in the junction called Schottky barrier height (SBH) which is also expressed in eV. It is the difference between the energy required for an electron to get free from the metal to the energy required for an electron to detach from the semiconductor, which is represented in the equation 2.1.

\[
\Phi_B = \Phi_M - \chi_S
\]  

(2.1)

After the contact formation, the M-S junction reaches thermal equilibrium i.e. the electrons from conduction band of semiconductor tend to move towards the metal until the fermi energy levels of both materials line up, because electrons in the semiconductor have higher energy compared to the electrons in metal. The electrons in the semiconductor lowers the energy band (bending) by shifting the junction as shown in the Fig. 7. When electrons move from semiconductor to metal it leaves a positive charged donor atom
behind, the region of semiconductor near metal becomes depleted (no free charged carriers) and makes the surface positive charged at interface so the electrons flow towards metal until it reaches the equilibrium between the diffusion electrons (semiconductor to metal) and the drift electrons (caused by ionized input atoms).

The built-in potential \( V_{BI} \) is the energy required by the carrier to cross the depletion region. In other words, it prevents from further carrier migration between the junction, \( V_{BI} \) is also known as equilibrium contact potential (forms when fermi energy levels lined up). \( V_{BI} \) in M-S junction is given by the equation 2.2.

\[
V_{BI} = \Phi_M - \Phi_S \tag{2.2}
\]

**Figure 6:** Energy band diagram of metal-semiconductor after contact and before equilibrium.
Width of depletion ‘W’ depends on the built-in potential, the doping concentration and the applied voltage. Since the depletion has very low charged carrier densities it behaves like insulator layer. The equation 2.3 gives the depletion width.

\[ W = \sqrt{\frac{2\varepsilon(V_{bi} - V_a)}{N_d}} \]  \hspace{1cm} (2.3)

where,

\( W \) = Width of the depletion region.
\( V_{bi} \) = Built-in potential
\( V_a \) = Applied Voltage
\( N_d \) = Doping Concentration
\( \varepsilon \) = Permittivity of substrate

After formation of depletion region, not many electrons have the energy to overcome the barrier to reach the metal. Depending on the biased voltage to the junction,
the barrier can either become lowered from semiconductor side or it can become enlarged. Fig. 8 shows the energy band diagram during forward bias (F.B) and reverse bias (R.B). When the diode is forward biased the depletion region becomes small and the electrons can cross over Schottky barrier to move towards the metal. The fermi level of the semiconductor rises with respect to the applied voltage ($V_a$) as shown in Fig. 8 (a). If the diode is reverse biased, the voltage applied strengthen the built-in potential and the depletion becomes wider with in the semiconductor therefore, the forward current goes to zero so in this case the fermi level of the semiconductor lowers with the applied voltage ($V_a$) as shown in Fig. 8 (b).

![Figure 8: Energy band diagram of M-S junction at (a) forward bias and (b) reverse bias.](image)

### 2.3 Current Transportation in Schottky Diode

The current across Schottky barrier diode occurs mainly because of majority charge carriers. There are three mechanisms by which the current transportation in metal/n-type semiconductor may occur, (1) Thermionic emission where, electrons flow over the barrier towards the metal as shown in Fig.9 (a). This occurs when the barrier is wide (due to low doping concentration), the only way for the electrons to pass through the barrier is to emit
over the potential barrier. Carrier migration in rectifying contact is mainly due to this mechanism. The width of the barrier depends on the doping concentration of the semiconductor. (2) Thermionic field emission occurs when semiconductor is medium doped, electrons tunnel through the thin barrier in the upper end of barrier as shown in Fig.9 (b). (3) Field emission (Quantum mechanical tunneling) through the energy barrier. This mechanism occurs when the material (semiconductor) is heavily doped, width of the energy barrier becomes so thin that the electrons start flowing through the barrier this phenomenon is called tunneling as shown in Fig.9 (c). This is the most important current transportation mechanism for ohmic contact [41].

![Figure 9: Conduction mechanisms for metal-semiconductor (n-type). (a) Thermionic emission; (b) thermionic-field emission; (c) field emission [from ref 41].](image)

Bethe has developed the theory for Thermionic emission, he proposed that the barrier height ($\Phi_B$) is much higher than $kT$, the formation of thermal equilibrium at junction will determines the emission and the equilibrium does not effect by the net current flow [37]. These assumptions create the barrier shape irrelevant and flow of current is controlled by the potential barrier height. So, the migration of electrons over the top of barrier results in current transportation. In this case, the diffusion and drift of charge carriers in the space charge region were neglected. The relation between current and voltage for thermionic emission is given by equation 2.4:
\[ I_F = A . A^* . T^2 e^{-q\Phi_B/kT} \left( e^{q(V_a-IR_S)/nkT} \right) \left( 1 - e^{-q(V_a-IR_S)/kT} \right) \] (2.4)

\[ I_F = I_0 \left( \frac{qV_a}{e^{nKT}} - 1 \right) \] (2.5a)

The reverse saturation current \( I_0 \) depends on the potential barrier height \( \Phi_B \) along with charge of electron and thermal voltage. Electrons in this case flow from metal to semiconductor.

\[ I_0 = A . A^* . T^2 e^{-q\Phi_B/kT} \] (2.5b)

Here \( I_F \) is the forward-current, \( A \) is the active-area of the metal contact on the semiconductor, \( T \) is the temperature of the material, \( \Phi_B \) is the barrier height between metal and semiconductor, \( V_a \) is the applied voltage (under high bias \( V_a >> 3kT/q \)), \( R_S \) is the series resistance, \( A^* \) is the Richardson’s constant for the material (a relation of current density and temperature), \( k \) is the Boltzmann constant and \( n \) is the ideality factor, the value \( n \) for an ideal diode is 1 but for a practical diodes it varies from 1-2. Under high bias and negligible series resistance the Eq. 2.5a can be simplified to Eq. 2.6.

\[ I_F = I_0 \left( \frac{qV_a}{e^{nKT}} \right) \] [if \( V >> 3kT \)] (2.6)

There are several factors of the material and the device fabrication which may cause a deviation from the performance of a device determined by the equation 2.4. Some of the factors like linearization and offset-potential caused by the resistance may vary the characteristics of an ideal diode. Whereas in R.B, a constant increase in current due to carrier generation is greater than the reverse saturation current \( I_0 \) and the current flow in reverse bias occurs because of avalanche and Zener breakdown. During reverse bias, the diode will be in high resistance mode although there are various mechanism which can generate current flow through it. Reverse breakdown voltage is an important aspect of a diode performance which occurs when the device is reverse biased and start conducting exponentially. There are two mechanisms which causes reverse-bias breakdown, 1) avalanche multiplication and 2) quantum mechanical tunneling. Neither of these two process will cause device failure. However, high-current due to breakdown voltage will increase the diode temperature this can be the cause of permanent device failure [42].
Avalanche-breakdown occurs due to impact ionization when large electrical-potential is applied to the diode, high-energy electrons pass over the barrier and promotes the formations of other electron-hole pair. Quantum mechanical tunneling which leads to Zener breakdown occurs when, the electrons flows through (penetrate) the potential barrier of depletion region. The breakdown voltage (or reverse blocking voltage) caused by these mechanisms can be determined by the equation 2.6. The reverse blocking voltage characteristics of a Schottky diode depends on the doping concentration ($N_D$) and breakdown electric-field ($E_c$) of the material (semiconductor).

$$ V_{RB} \approx \frac{\varepsilon_0 \varepsilon_m (E_c)^2}{2 q N_D} $$

(2.7)

The Schottky barrier diode in R.B results in large leakage current which increases with lowering of barrier height and increases with elevating temperature, this is because of electrical-field crowding at Schottky barrier edges.

![Figure 10: Schottky contact edge termination: a) Metal field plate structure, b) Diffused guard ring structure.](image)

The shape of metal-contact is the most important aspect which determines the electric-field intensity surrounding the Schottky contact. So, the breakdown voltage or blocking voltage can be increased by reducing the field intensity over the device. This can be done by improving the geometry of the metal contact and by implementing better edge-
termination methods. There are two most commonly used edge-termination methods for Schottky contacts which are shown in Fig. 10.

2.4 Parameter Extraction Through Electrical Characterization

In this study, the parameters of Schottky diodes, including barrier height $\Phi_B$, ideality factor $n$, on-resistance $R_{on}$, and capacitance ‘c’ were investigated using I-V and C-V measurements.

2.4.1 Current-Voltage (I-V) Characterization

As discussed in section 2.2 the current in Schottky barrier diode is due to thermionic emission of electrons over the potential barrier and the relation of current and applied voltage the relation.

$$I_F = I_0 \left( \frac{e^{qV_a}}{e^{nkT}} \right)$$

Where $I_0 = A \cdot A^* \cdot T^2 e^{-q\Phi_B/kT}$ (from eq. 2.5a and 2.5b)

By taking natural logs on both sides of the Eq. 2.5

$$\ln(I_F) = \ln(I_0) + \frac{q}{nkT} V_a$$

(2.8)

where, $\ln(I_0) = \ln(A \cdot A^* \cdot T^2) - \frac{q}{kT} \Phi_B$

(2.9)

From equations 2.7, a plot of $\ln(I_F)$ against $V_a$ gives a straight line whose slope is $q/nkT$ and $\ln(I_0)$ is the intercept which can be obtained by extrapolating the line to $V_a$ equals to zero. So, with this I-V characterization, by knowing $A^*$, Schottky contact cross section area $A$ and the temperature, the values of ideality factor ($n$) and barrier height ($\Phi_B$) can be determined [36].
2.4.2 On-Resistance ($R_{on}$)

The on-resistance the diode can be obtained by determining the series resistance ($R_s$). Assume $I_F$ as $I$ and $V_a$ as $V$ in the Eq. (2.4) for $V >> 3kT/q$ which gives.

\[
I = A \cdot A^* \cdot T^2 \left( e^{\frac{-q \Phi_B}{kT}} \right) \left( e^{\frac{q(V-I R_s)}{nkT}} \right)
\]  

(2.10)

By further simplification Eq. 2.10 gives

\[
I = \frac{1}{R_s} \left[ \frac{dV}{d(\ln(I))} \right] - \left( \frac{kT}{q} \right) \left( \frac{n}{R_s} \right)
\]  

(2.11)

a plot of $I$ against $dV/d[\ln(I)]$, gives a straight line whose reciprocal of slope gives the series resistance. Now by knowing $R_s$ and Schottky contact cross section area $A$. On-resistance can be determined by equation 2.12.

\[
R_{on} = R_s \times A
\]  

(2.12)

2.4.3 Capacitance–Voltage (C-V) Characterization

The structure of metal-semiconductor junction along with its depletion forms a capacitor, in which the voltage change across the metal-semiconductor junction leads to a change in depletion region width and this change is attained by the flow of charge carrier in the space-charge layer. The variations in the charge of depletion region gives rise to capacitance [36]. The Schottky diode capacitance is measured with reversed biased
voltage, when a voltage applied across the reversed biased diode, the capacitance is given by Eq. 2.13.

\[
C(V) = \frac{\varepsilon A}{W(V)} = A \sqrt{\frac{\varepsilon N_D}{2(V_{BI} - V_a)}}
\]

(2.13)

where \(W\) is the width of the depletion region, \(V_{BI}\) is the built-in potential, \(A\) is the Schottky contact cross section area, and \(N_D\) is the doping density of the material. A plot of \(1/C^2\) against \(V\) determines the \(V_{BI}\) and \(N_D\). The method used in the C-V measurements were obtained by superimposing an alternative-voltage of 10mV at 1MHz at DC reverse bias, the data further analyzed by the following relation.

\[
\left(\frac{A}{C}\right)^2 = \frac{2[V_{BI} - \frac{kT}{q}]}{qK_s\varepsilon_0 N_D} + \frac{2V}{qK_s\varepsilon_0 N_D}
\]

(2.14)

where \(A\) is the area, \(V_{BI}\) is the built-in potential, \(K_s\) is the dielectric constant of the semiconductor, \(N_D\) is the doping concentration of the semiconductor, \(k\) is the Boltzmann constant, \(T\) is the temperature, \(\varepsilon_0\) is the permittivity. A plot of \((A/C)^2\) against reverse-biased voltage \(V\) gives a straight line whose slope is \(2/q\varepsilon_0 N_D\) by which the value of \(N_D\) can be obtained. The intercept is equal to \(V_i = -V_{bi} + kT/q\), this will give the \(V_{bi}\) value. The SBH can be obtained by the following equation [36].

\[
\Phi_B = V_i + \left(\frac{kT}{q}\right) \left[1 + \ln\left(\frac{N_0}{N_D}\right)\right]
\]

(2.15)

The value of \(N_0\) is \(1.69 \times 10^{19}\) cm\(^{-3}\) used for effective density of state (4H-SiC) [36].
CHAPTER 3

Techniques Used for Schottky Diode Fabrication

This chapter presents the procedure for the processing techniques that were used to fabricate Ti-SiC Schottky barrier diodes, which includes the details of SiC semiconductor substrate, Schottky/ohmic contacts deposition and thermal treatment of the devices. In addition, the details of the instruments used for electrical and material characterization of the device are also included.

3.1 Sample Preparation

The Schottky barrier diodes were fabricated on n-type epitaxial 4H–SiC wafer (76.2 mm in diameter and 400 micrometers thick) with Si-face on the front side and carbon face on the back side, which was purchased from CREE Research Inc., for experiments, the wafer was sliced into segments of 0.5 × 0.5 cm$^2$ using diamond point scriber. The resistivity of the substrate was 0.015 - 0.028 Ω-cm. The wafer consists of two n-type epitaxial layers grown 4° off-axis with the basal plane having (0 0 0 1) orientation and with different carrier concentrations compared to highly doped substrate, first epitaxial layer was 0.5 µm-thick with carrier concentration of $\sim 1 \times 10^{18}$ cm$^{-3}$ and the second epitaxial layer was 11.67 µm-thick lightly doped having carrier concentration of $5.06 \times 10^{15}$ cm$^{-3}$. This epilayer was selected for depositing Schottky contact. Fig. 12 shows the structure of the SiC wafer.

<table>
<thead>
<tr>
<th>Layer</th>
<th>Thickness (µm)</th>
<th>Type</th>
<th>Carrier Concentration</th>
</tr>
</thead>
<tbody>
<tr>
<td>EP2</td>
<td>11.67</td>
<td>n$^-$</td>
<td>$\sim 5.06 \times 10^{15}$</td>
</tr>
<tr>
<td>EP1</td>
<td>0.5</td>
<td>n$^+$</td>
<td>$\sim 1 \times 10^{18}$</td>
</tr>
</tbody>
</table>

n$^+$ Heavily doped
4H-SiC Substrate

Figure 12: Structure of 4H-SiC substrate used in experiments.
The preparation of a semiconductor surface cleaning prior to metal-deposition is extremely important for the resulting Schottky/ohmic contacts properties. On top of the SiC epilayer there was a sacrificial SiO\textsubscript{2} protective layer grown, which helps in improving the surface morphology. There are several chemical mixture and process that can be followed for surface cleaning, Table 4 shows some of the chemicals used in wafer cleaning process [43]. In this work, the samples were cleaned by following standard RCA (Radio Corporation of America) cleaning-process [40]. Degreasing was the first step in cleaning the surfaces of the samples, which includes boiling in acetone for 3 mins, then boiling in IPA (isopropyl alcohol) for 3 mins and followed by rinsing in deionized water. Next, the samples were kept in BOE (Buffer Oxide Etchant - Ammonium Hydrogen Difluoride solution) for 3 mins to obtain SiO\textsubscript{2} free surface, sample were again rinsed in DI-water and dried using nitrogen gas.

**Table 4:** Chemicals/Mixtures used for cleaning SiC substrate and removal of SiO\textsubscript{2} [from ref 43].

<table>
<thead>
<tr>
<th>Chemicals - Mixtures</th>
<th>Temperature and Time</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>H\textsubscript{2}O: NH\textsubscript{4}OH: H\textsubscript{2}O\textsubscript{2} (5:1:1)</td>
<td>75 °C for 5 mins</td>
<td>RCA SC1</td>
</tr>
<tr>
<td>H\textsubscript{2}O: HCL: H\textsubscript{2}O\textsubscript{2} (5:1:1)</td>
<td>75 °C for 5 mins</td>
<td>RCA SC2</td>
</tr>
<tr>
<td>H\textsubscript{2}SO\textsubscript{4}: H\textsubscript{2}O\textsubscript{2} (2.5:1)</td>
<td>100 °C for 5 mins</td>
<td>Seven-up</td>
</tr>
<tr>
<td>H\textsubscript{2}O: HF: CH\textsubscript{3}CH(OH)CH\textsubscript{3} (100:3:1)</td>
<td>25 °C for 100 secs</td>
<td>IMEC</td>
</tr>
<tr>
<td>HCL: HNO\textsubscript{3} (3:1)</td>
<td>50 °C for 5 mins</td>
<td>Aqua Regia</td>
</tr>
<tr>
<td>HF: H\textsubscript{2}O (1:10)</td>
<td>25 °C</td>
<td>Dilute HF</td>
</tr>
<tr>
<td>HF: NH\textsubscript{4}F (1:7)</td>
<td>25 °C</td>
<td>BOE/BHF</td>
</tr>
</tbody>
</table>

**3.2 Schottky and Ohmic Contact Deposition**

Ohmic contacts were first deposited on highly doped surface of the sample (back side) which provides a low contact-resistance ohmic terminal. Samples were mounted inside the vacuum chamber immediately after surface cleaning so as to avoid any further formation of native oxide on the SiC surface. The contact-metals were sputter deposited using magnetron-sputtering. The sample holder with a film thickness monitor were placed 10 cm above the sputter guns and the holder can rotate mechanically to position the samples.
on a specific metal target gun. The deposition-process was carried out in a high vacuum chamber with a base pressure of $3.1 \times 10^{-7}$ Torr. Ar was used as the process gas with a flow rate of 10 SCCM (standard cubic centimeter per minute) with the chamber-pressure maintained at 10 mTorr during sputtering. Before deposition, two minutes pre-sputtering was allowed to clean the target material surface. The ohmic contact metal used for deposition are Titanium (Ti) and Nickel-Gallide (NiGa-an alloy of 90% Ni/10% Gallium), this metal combination as an ohmic contact was reported to be a perfect way in achieving low-resistance ohmic contact for 4H-SiC [44]. Titanium was first deposited for 13 mins with a current of 0.1 A to attain a thickness of 25 nm, NiGa is then deposited on top of Ti layer for 10 mins with a current of 0.1 A to reach the thickness of 65 nm and followed by another Ti layer of 10 nm. The deposited layer thickness was monitored in real-time using the film thickness monitor so to ensure the amount of metal that can be sputtered on to the substrate. After sputtering the ohmic metal contact, the samples were degreased again in acetone, isopropyl alcohol, and DI-water. Now the samples were annealed at high temperature 950 °C in N$_2$ environment for 2 minutes using rapid thermal processor (RTP) Fig. 13 shows the ohmic contact of a sample after annealing and RTP. N$_2$ was used as an inert-gas which helps in reducing the chance of metal oxidation at high-temperature annealing.

![Figure 13](image)

**Figure 13:** (a) Ohmic contact after annealing, (b) Rapid Thermal Processor (RTP).
To attain a good quality (low contact resistance) ohmic contact, the reaction between metal and SiC is essential to fully remove any effects of surface preparation. The ohmic contact formation mainly depends on metal reaction and the distribution of carbon during the surface reaction, high temperature annealing achieves this reaction by forming a Ni/Ti- silicide layer on SiC substrate.

After preparing the ohmic contact the final step for fabricating Schottky barrier diode is to deposit Schottky contacts on lightly doped epilayer of the substrate (front side). As discussed in section 2.1 Titanium (Ti) was used as Schottky contact in this work. Two sets of samples (each set contains six samples) were prepared to vary the thermal treatment process (after Schottky contacts deposition) for each set. Before sputtering, the sample surface (only front side) was cleaned again using BOE (Buffer Oxide Etchant) to remove any oxide layer which may formed during ohmic contact preparation, at the same time the ohmic metal contact was protected from the acids. Each sample was sputtered separately because the Schottky contacts were deposited at different temperatures, 28 °C, 200 °C, 400 °C, 500 °C, 700 °C, 900 °C. Since the temperature during sputtering is very high, photolithography technique was not used for patterning of the Schottky contact because photoresist is not capable of withstanding high temperatures. Therefore, a shadow mask is used during the deposition, which is placed on top of the sample.

**Figure 14:** (a) Shutter mask, (b) Heater with sample holder.
The shadow mask is made up of stainless-steel and it is perforated with ~ 0.5 mm diameter holes as shown in Fig. 14 (a), these perforated hole acts like an open window during the deposition so that the metal will sputter on the exposed surface of SiC substrate. The substrate was placed on the heater followed by the shutter mask on top of it as shown in the Fig. 14 (b) and mounted in the high vacuum deposition chamber.

The Schottky contacts were deposited with a base pressure of ~3.1×10^{-7} Torr, there is a small variation in the base pressure during the deposition of other samples but the value is of the order of 10^{-7} Torr. The first sample was deposited at room temperature ~ 28 °C, the temperature was monitored in real-time using thermocouple which is placed on the heater, while the temperature of the heater was controlled by an external power-controller (Powerstat – Variable autotransformer), the flow rate of Ar gas during sputtering was held at 10 SCCM with chamber-pressure of 10 mTorr, Ti was sputtered on the sample with current of 0.1 A for 100 minutes to reach the Schottky contact thickness of ~200 nanometers, the diameter of a Schottky contact is ~600 µm. Fig. 15 shows the image of Schottky contact on a sample which was capture by an optical microscope.

![Image of Schottky contacts after deposition](image_url)

**Figure 15:** Schottky contacts after deposition (600 µm in diameter).

As mentioned earlier, the Schottky contacts for other samples were deposited at different temperatures by varying the voltage-controller of the heater and the rest of deposition parameters were maintained to the same value for all the samples. Fig. 16 shows the schematic cross section of a 4H-SiC Schottky barrier diode.
Figure 16: Schematic cross-section of SBD.

Sputtering is most common technique used for depositing metals, in this work all deposition experiments were carried out in a magnetron-sputtering deposition chamber as shown in Fig. 17 (a). This system consists of a glass bell jar protected by a steel cage, vacuum pumps, temperature controller, DC/RF power supplies and three magnetron-sputtering guns as shown in Fig. 17(b).

Figure 17: (a) Sputter deposition chamber and (b) Magnetron-sputtering guns.
A magnetron-sputtering cathode consists of magnets under the target material which create a closed-static magnetic field pattern on top of the surface as shown in Fig. 18. This field controls the movement of secondary-electrons which are close to the target area to collimate the plasma. These secondary-electrons are captured by the magnetic-field and the motion of electrons are perpendicular to both electrical and magnetic field directions. The electrons lose their kinetic-energy when a collision occur with atoms of the processing gas, in this case Ar gas atoms which results in formation of high density plasma. The created ions will have high chance of collision with the cathode surface and improves the ionization efficiency [45]. In other words, this mechanism is based on bombardment of high energetic ions on the target material and eventually the atoms on the target surface eject and deposit on the substrate which leads to formation of thin-film coating.

![Magnetron Sputtering](image)

**Figure 18:** Magnetron sputtering [from ref 45].

### 3.3 Annealing:

After depositing Schottky contact on all samples at different temperatures, the samples were annealed at 500 °C for 60 hours in total and removed for characterization at interval of 12, 24, 36, 60 hours. As mentioned earlier two sets of samples were prepared, the samples were placed on the heater and there are mounted in the vacuum chamber. Set-1 samples were annealed in argon whereas set-2 samples were annealed in vacuum. The
reason for varying the deposition temperatures and annealing process was to investigate the variations of interfacial layer formation between the Schottky contact and 4H-SiC and to examine the performance of SBDs.

3.4 Methods Used for Electrical Characterization

This section gives the details of techniques and the instruments used for characterization of fabricated Schottky barrier diodes. Electrical characterization includes current-voltage (I-V), capacitance-voltage (C-V) and current-voltage-temperature (I-V-T) have been performed on the all samples.

3.4.1 I-V Measurements

The forward bias current-voltage (I-V) measurements were performed by using Keithley source meter (model 2400) which has a voltage range 5 µV to 20 V. The samples were attached to a copper plate using conductive sliver-paste (colloidal sliver liquid) as shown in Fig. 19 (a) so that the ohmic contact (back side of the substrate) of a sample is in contact with plate having a wire which is connected to negative terminal of the source meter. This copper plate with sample is placed in a probe station so that the probe is in contact with the Schottky metal on the substrate and it is connected to the positive terminal of the source meter as shown in Fig. 19 (b). A program file of LabVIEW software was used to control the source meter and to collect the data of I-V measurements. The forward bias voltage was varied from 0 to 2 volts with 300 data point and the respective current values were collected. The I-V measurement was performed on five different diodes of each sample. Fig. 20 (a) shows the source meter that was used in this work and Fig. 20 (b) shows the probe station used for I-V measurements.

After collecting the I-V measurements of as-deposited samples, the samples were removed from the copper plate and cleaned using acetone to remove the residual of the silver paste on the samples. The samples were then placed on the heater and mounted in the vacuum chamber for annealing. This process was repeated to perform forward-bias I-V measurements on samples after 12, 24, 36, 60 hours of annealing.
Figure 19: (a) Sample on a copper plate and (b) Test probe on a Schottky contact.

The I-V measurements were taken from same set of diodes of each sample after every interval of annealing so to maintain an accurate change in behavior comparison of a specific diode during the heat treatment. The data collected was analyzed using the thermionic equation to determine the barrier height, ideality factor, and on-resistance of the diodes.

Figure 20: (a) Keithley source-meter (2400) and (b) Probe station.
Reverse bias I-V measurements were performed to determine the breakdown voltage (blocking voltage) and reverse leakage current of the diodes. Keithley 2410 source-meter (voltage range is up to ± 1100 V and ± 1A) was used to take the reverse-bias measurements instead of 2400 because it has higher voltage range. The reverse bias was performed on several diodes on each sample by varying the reverse bias voltage from 0 volts to hundreds of volts until the diode breakdown occurs.

3.4.2 C-V measurement

C-V measurements were performed using Agilent precision LCR meter (model-E4980A), this LCR meter is connected to the computer using GPIB (General Purpose Interface Bus) cable and it is operated using a LabVIEW software program file. This meter has four output ports in which two probes from L\textsubscript{cur} and L\textsubscript{pot} ports (Low terminals) are connected together whereas the other two probes from H\textsubscript{cur} and H\textsubscript{pot} ports (High terminals) are connected together so that there are two main terminals formed one is low and other is high. The sample was placed on the copper plate using the silver paste. The copper plate was connected to the low terminal and the Schottky contact was connected using a needle probe and it is connected to the high terminal. As mentioned in section 2.4.3, by applying the reverse voltage the corresponding capacitance values from the diode were collected. The C-V measurements were done by covering the sample with an isolation container as shown in Fig. 21 (c), because the C-V measurements were very sensitive to the light and the ambient noise, i.e. the measurement shows a non-linear behavior if the sample is out of that isolated cage. These measurements were performed by superimposing an alternative-voltage of 10mV at a frequency of 1 MHz on the reverse DC bias which was varied from 0V to -5V and the corresponding capacitance values were recorded. Fig. 21 shows the LCR meter used in this work and the setup for C-V measurements.
3.4.3 I-V-T Measurement

Current-Voltage-Temperature (I-V-T) measurements were performed to investigate the diode performance of all samples with change in temperature. Unlike I-V measurement set up, the sample in this method was placed on a stainless-steel plate using silver paste and this plate is mounted on a ceramic heater. The temperature of the heater was controlled by a voltage-controller. The plate is connected to the negative terminal of the Keithley Source meter (model 2400) and the Schottky contact is connected using a needle probe, which is then connected to the positive terminal of the source meter so to perform forward-bias I-V-T characterization. A thermocouple was placed near the steel plate to measure the accurate temperature to which the diode is exposed. The measurements were performed by varying the voltage from 0 V to 2 V with 200 data point in that range and the corresponding current values were recorded, this process was repeated for every
25 °C rise in temperature, i.e. I-V measurement were performed with a rise in temperature of 25 °C from room temperature ~25 °C to 500 °C on diodes of all samples. Fig. 22 shows the setup used for I-V-T characterization.

**Figure 22: I-V-T Setup**

### 3.5 Material Characterization (XRD)

The material characterization of the Schottky contacts deposited at different temperatures has been evaluated by X-ray diffraction (XRD). These measurements were performed in 2θ geometry using Bruker X8 prospector (with micro source Cu radiation generator) to identify the composition of interfacial layers that are formed in between Schottky metal and 4H-SiC. The reason for using prospector instead of powder diffractometer is that the diameter of radiation beam of prospector is too small that it can be focused on each Schottky contact of the sample. The scans were performed on all samples from as deposited to 900 °C after 60 hours of annealing and scanned on four Schottky contacts of each sample to check the data consistency. Fig. 23 shows the instrument used for X-ray diffraction.
Figure 23: (a) Sample holder and (b) Bruker X8 Prospector.
CHAPTER 4
Results and Analysis

4.1 Results of Current-Voltage (I-V) Measurements

In this work, the Ti Schottky contacts were deposited at different temperatures (28 °C, 200 °C, 400 °C, 500 °C, 700 °C, and 900 °C). The I-V measurements were performed on all samples (two sets of samples) after deposition and after 12, 24, 36, 60 hours of annealing. Forward bias current-voltage results showed many interesting features. Some of the tested-diodes revealed very good linearity I-V characteristics as defined by thermionic-emission theory. However, other diodes on some samples showed tunneling mechanism which disturbed the linearity I-V behavior.

4.1.1 Forward bias I-V measurements

From Fig. 24 and 25 the I-V characteristic plots of diodes revealed that the turn-on voltage under forward bias varies with the deposition temperatures of Schottky contacts. The Schottky contacts deposited at lower temperatures had higher-turn on voltages and higher resistance when compared to the Schottky contacts deposited at higher temperature. The turn-on voltage was increased from room temperature deposited contact to 200 °C deposited contact and it started declining with increase in deposition temperature.

In Fig. 25, it is seen that the well behaved Schottky-contacts had a reasonable portion of linearity (up to six decades) whereas the linearity got distorted or disappears with increase in deposition temperatures. As discussed in section 2.4.1, the slopes and intercepts of the linear portion from the semilog I-V plots have been calculated. Using those values, the parameters like barrier heights and ideality factors are calculated, these parameters were collected after each interval of annealing (at 500 °C) to investigate the change in properties of Schottky barrier diodes with annealing time. In this study one set of samples annealed in Argon (Ar) and other set of samples annealed in vacuum. Table 5 and 6 shows the summary of data obtained from two sets of samples.
Figure 24: Plot of I-V on linear scale for the Ti Schottky contact deposited at 28 °C, 200 °C, 400 °C, 500 °C, 700 °C and 900 °C.
Figure 25: I-V plot for the Ti Schottky contact deposited at 28 °C, 200 °C, 400 °C, 500 °C, 700 °C and 900 °C.
Set-1: Samples annealed at 500 °C in argon

Figure 26: Change in barrier height and ideality factor with annealing time. (Samples annealed at 500 °C in argon).

Table 5: Change in barrier height (eV) and ideality factor with annealing time. (samples annealed at 500 °C in argon).

<table>
<thead>
<tr>
<th>Anneal Time (Hrs.)</th>
<th>28 °C</th>
<th>200 °C</th>
<th>400 °C</th>
<th>500 °C</th>
<th>700 °C</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>SBH</td>
<td>n</td>
<td>SBH</td>
<td>n</td>
<td>SBH</td>
</tr>
<tr>
<td>0</td>
<td>0.89</td>
<td>1.03</td>
<td>0.99</td>
<td>1.04</td>
<td>0.89</td>
</tr>
<tr>
<td>12</td>
<td>0.91</td>
<td>1.02</td>
<td>1.11</td>
<td>1.03</td>
<td>0.95</td>
</tr>
<tr>
<td>24</td>
<td>0.89</td>
<td>1.03</td>
<td>1.09</td>
<td>1.04</td>
<td>0.95</td>
</tr>
<tr>
<td>36</td>
<td>0.90</td>
<td>1.01</td>
<td>1.09</td>
<td>1.04</td>
<td>0.96</td>
</tr>
<tr>
<td>60</td>
<td>0.88</td>
<td>1.03</td>
<td>1.12</td>
<td>1.03</td>
<td>0.96</td>
</tr>
</tbody>
</table>
**Set-2:** Samples Annealed At 500 °C in vacuum

![Figure 27](image)

**Figure 27:** Change in barrier height and ideality factor with annealing time. (samples annealed at 500 °C in vacuum).

**Table 6:** Change in barrier height (eV) and ideality factor with annealing time. (samples annealed at 500 °C in vacuum).

<table>
<thead>
<tr>
<th>Anneal Time (Hrs.)</th>
<th>Schottky Contact Deposition Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>28 °C</td>
</tr>
<tr>
<td></td>
<td>SBH n</td>
</tr>
<tr>
<td>0</td>
<td>0.70</td>
</tr>
<tr>
<td>12</td>
<td>0.75</td>
</tr>
<tr>
<td>24</td>
<td>0.75</td>
</tr>
<tr>
<td>36</td>
<td>0.74</td>
</tr>
<tr>
<td>60</td>
<td>0.79</td>
</tr>
</tbody>
</table>

The results from set-1 and set-2 shows that the values of barrier height and the ideality factor of Schottky diodes are better for Argon annealed samples compared to
vacuum annealed samples. The values listed in Table 5 and 6 are the average values taken from five diodes of each sample so to verify the consistency in the data obtained. From Fig. 26, it can be seen that the values of barrier height and ideality factors are improving from 12-36 hours of annealing. Further annealing produces negligible change in the parameters started. Based on all the parameter values, it is clear that the Schottky contact deposited at 200 °C yields better Schottky barrier diodes.

4.1.2 Specific On-Resistance

The on-resistance ($R_{\text{on}}$) is a crucial parameter for better performance of a diode. In this work the on-resistance is determined by first obtaining series resistance ($R_s$) as mentioned in section 2.4.2. As shown in Fig. 28, a graph of $I$ vs $dV/d[\ln(I)]$ is plotted and the value from reciprocal of slope of linear region gives the series resistance ($R_s$) value, the on-resistance value is obtained by multiplying the $R_s$ with the cross-section area (A) of Schottky contact. Fig. 29 and Table shows the variations in the on-resistance value with the annealing time of two sets of samples.

**Figure 28:** A plot of $I$ versus $dV/d[\ln(I)]$ to determine the on-resistance.
Figure 29: Change in on-resistance with annealing time (samples annealed in argon and vacuum).

Table 7: Change in specific on-resistance $R_{on}$ (mΩ cm$^2$) with annealing time (samples annealed in argon).

<table>
<thead>
<tr>
<th>Anneal Time (Hrs.)</th>
<th>Schottky Contact Deposition Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>28 °C</td>
</tr>
<tr>
<td>0</td>
<td>46.94</td>
</tr>
<tr>
<td>12</td>
<td>40.78</td>
</tr>
<tr>
<td>24</td>
<td>57.53</td>
</tr>
<tr>
<td>36</td>
<td>50.69</td>
</tr>
<tr>
<td>60</td>
<td>46.82</td>
</tr>
</tbody>
</table>
Table 8: Change in specific on-resistance $R_{on}$ (mΩ cm$^2$) with annealing time (samples vacuum).

<table>
<thead>
<tr>
<th>Anneal Time (Hrs.)</th>
<th>Schottky Contact Deposition Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>28 °C</td>
</tr>
<tr>
<td>0</td>
<td>25.22</td>
</tr>
<tr>
<td>12</td>
<td>25.62</td>
</tr>
<tr>
<td>24</td>
<td>24.28</td>
</tr>
<tr>
<td>36</td>
<td>27.30</td>
</tr>
<tr>
<td>60</td>
<td>29.20</td>
</tr>
</tbody>
</table>

Fig. 29 and Table 8 shows that on-resistance values are low for diode annealed in vacuum compared to argon annealed samples. The on-resistance values tend to increase in between 12-36 hours of annealing but on further annealing the values are declining. Compared to all data the Schottky contact deposited at 400 °C and 500 °C have low on-resistance value.

4.1.3 Reverse bias I-V measurements

Reverse-bias I-V measurements were performed on samples which are annealed in Argon to find the reverse leakage current and the breakdown voltage. Reverse bias voltage is applied to at least four diodes in each sample until the device breakdown occurs. Fig. 30 shows that the reverse leakage current increases with increase in deposition temperature of Schottky contacts. Compared to all sample the Schottky contact deposited at 200 °C has the highest breakdown voltage of 850 V with a low leakage current of 0.5x10$^{-6}$ A at this bias voltage. Fig. 30 shows the reverse bias I-V Plots of samples, as most of the diode’s breakdown occurs near 450 V except 200 °C and 500 °C samples, so the reverse leakage current of all samples at 400 V are listed in Table 9.
Figure 30: Reverse leakage current at 400 V.

Table 9: Reverse leakage current at 400 V

<table>
<thead>
<tr>
<th>Schottky Deposition Temperature</th>
<th>leakage Current (A) at 400 V</th>
</tr>
</thead>
<tbody>
<tr>
<td>28 °C</td>
<td>-7.93 x 10^{-3} (at 300 V)</td>
</tr>
<tr>
<td>200 °C</td>
<td>-6.59 x 10^{-8}</td>
</tr>
<tr>
<td>400 °C</td>
<td>-1.17 x 10^{-6}</td>
</tr>
<tr>
<td>500 °C</td>
<td>-2.48 x 10^{-6}</td>
</tr>
<tr>
<td>700 °C</td>
<td>-3.89 x 10^{-5}</td>
</tr>
</tbody>
</table>
Figure 31: Reverse bias I-V plots of samples deposited at different temperature.
4.1.4 Current-Voltage-Temperature (I-V-T) measurement

In this study, current-voltage-temperature (I-V-T) measurements were performed on samples of two sets after annealing for 60 hours. The temperature was increased from room temperature to 500 °C with an increment of 25 °C upto 500 °C. This measurement was performed to investigate the performance of a device at higher temperatures. The diodes whose Schottky contacts deposited at 200 °C behaved very well by exhibiting linear I-V characteristics till 250 – 270 °C as described by thermionic emission. However, as the temperature increased the Schottky contacts started behaving like an ohmic contact. Since the diodes of 200 °C sample showed better performance compared to other samples the barrier height and ideality factor as a function of temperature were calculated.

Figure 32: I-V-T measurement of sample deposited at 28 °C and annealed at 500 °C in argon for 60 hrs.
Figure 33: I-V-T measurement of sample deposited at 200 °C and annealed at 500 °C in argon for 60 hrs.

Figure 34: I-V-T measurement of sample deposited at 500 °C and annealed at 500 °C in argon for 60 hrs.
Figure 35: I-V-T measurement of sample deposited at 700 °C and annealed at 500 °C in argon for 60 hrs.

Figure 36: I-V-T measurement of sample deposited at 900 °C and annealed at 500 °C in argon for 60 hrs.
Table 10: SBH and ideality factor as a function of temperature (200 °C annealed in Ar).

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>Barrier Height (eV)</th>
<th>Ideality Factor (n)</th>
</tr>
</thead>
<tbody>
<tr>
<td>25</td>
<td>1.08</td>
<td>1.05</td>
</tr>
<tr>
<td>50</td>
<td>1.01</td>
<td>1.11</td>
</tr>
<tr>
<td>75</td>
<td>0.93</td>
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<tr>
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<td>0.51</td>
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Figure 37: I-V-T measurements of sample 200 °C annealed in vacuum.
Table 11: I-V-T measurements of sample 200 °C annealed in vacuum.

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>Barrier Height (eV)</th>
<th>Ideality Factor (n)</th>
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<tr>
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<td>0.19</td>
</tr>
<tr>
<td>500</td>
<td>0.52</td>
<td>0.20</td>
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</table>
4.2 Capacitance-Voltage (C-V) measurements

The C-V measurements were performed on Ar and vacuum annealed samples after 60 hrs of annealing. As mentioned in the section 2.4.3, capacitance values were recorded under reverse bias voltage. A plot of \( (A/C)^2 \) against reverse-biased voltage \( V \) gives a straight line whose slope and the intercept values were calculated to determine the SBH and doping concentration. Fig. 34 shows the plot of C-V of samples which are annealed in argon and Fig. 35 shows the plot of \( 1/C^2 \) vs \( V \) of samples deposited at different temperature which shows the linearity of C-V measurement. Table 11 shows the doping concentration and the Schottky barrier height obtained from the slope and intercept values. the barrier height values obtained from C-V are greater than I-V measurement, this could be because of image force lowering and due to in homogeneities at metal-SiC interface [36]. The average doping concentration values from each sample were very close to the actual doping concentration value provided by the SiC substrate vendor which is \( 5.06 \times 10^{-15} \text{ cm}^3 \)

Table 12: Doping concentration and SBH obtained from C-V measurements.

<table>
<thead>
<tr>
<th>Schottky Dep. Temperature</th>
<th>Doping Concentration ( \left( N_d \right) \text{ cm}^{-3} )</th>
<th>Schottky Barrier Height (eV)</th>
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</thead>
<tbody>
<tr>
<td></td>
<td>Set-1</td>
<td>Set-2</td>
</tr>
<tr>
<td>28 °C</td>
<td>4.41E+15</td>
<td>4.25E+15</td>
</tr>
<tr>
<td>200 °C</td>
<td>4.11E+15</td>
<td>4.37E+15</td>
</tr>
<tr>
<td>400 °C</td>
<td>5.09E+15</td>
<td>4.49E+15</td>
</tr>
<tr>
<td>500 °C</td>
<td>6.75E+15</td>
<td>5.66E+15</td>
</tr>
<tr>
<td>700 °C</td>
<td>7.41E+15</td>
<td>ND</td>
</tr>
<tr>
<td>900 °C</td>
<td>7.31E+15</td>
<td>ND</td>
</tr>
</tbody>
</table>

Set-1: Samples annealed in argon.
Set-2: Samples annealed in vacuum.
ND- No data.
Figure 38: C-V plots of set-1 samples: (a) 28 °C (b) 200 °C (c) 400 °C (d) 500 °C (e) 700 °C (f) 900 °C.
4.3 X-ray Diffraction (XRD)

XRD measurements were performed on each sample, whose Ti Schottky metal contact were deposited at temperature 28C, 200C, 400C, 500C, 700C and 900C. The XRD scans were performed on four Schottky contacts of each sample to verify the consistency of the results. This method was performed to investigate the composition or the phase of the interfacial layer (silicides) formed in between the Ti/4H-SiC. Fig. 36 show the phases formed with respected to the deposition temperatures. The phases such as Ti$_5$Si$_3$, Ti$_3$SiC$_2$ were formed in the interfacial layer, results from published paper revels that there could be a TiC phase also formed in the samples but this might be dominated by the 4H-SiC peak intensity. Phases like Ti$_5$Si$_3$ and TiC are proven to be a good phase formation in the interfacial layer as these two phases have lower resistivity compared to Ti only [40]. In this study the intensities of phases formed increased with increase in deposition temperature of the Schottky contact samples.
Figure 40: X-ray diffraction spectra of Ti Schottky contacts deposited at 28 °C – 900 °C on 4H-SiC.
4.4 Auger Electron Spectroscopy (AES)

Two samples were prepared (Blanket pieces) for additional material characterization using auger electron spectroscopy (AES). Ti of 200 nm was deposited at 200 °C and 700 °C on the SiC substrates and annealed for 12hrs in Ar. AES was performed to investigate the depth profiling of concentration of elements at the interfacial region of Ti-SiC. The interfacial layer composition of Ti/SiC of both 200 °C and 700 °C samples were investigated. A positive argon ion beam was used for sputtering the surface to obtain auger electron spectrum at various depths. Sputtering and AES spectrum acquisition were conducted alternately.

From Fig. 37 and 38, AES results for the Ti-SiC interfacial layer of 200 °C sample shows that the atomic concentrations of carbon, oxygen, silicon, and Ti are 14.99 %, 52.26 %, 0.27 %, and 43.9%. From Fig. 39 and 40, the results for 700 °C sample shows that the atomic concentrations of carbon, oxygen, silicon, and Ti are 15.53 %, 42.99 %, 0.72 %, and 39.57 %. In contrast the oxygen and Titanium concentration at the interfacial layer of 200 °C sample is high compared to 700 °C sample. These results revealed that the interfacial region composition varied with the change in deposition temperature.

Figure 41: Auger electron spectrum of Ti/SiC:200 °C Sample.
Figure 42: AES depth profiling of Ti/SiC at 225 nm: 200 °C sample.

Figure 43: Auger electron spectrum of Ti/SiC:700 °C Sample.
Figure 44: AES depth profiling of Ti/SiC: 700 °C sample.
CHAPTER 5
Conclusion and Recommendation for Future Work

5.1 Conclusion

The influence of deposition temperature and annealing in the formation of Schottky contact on 4H-SiC was presented. Ti metal as a Schottky contact was deposited at different temperature ranging from ~25 °C to 900 °C and post deposition annealing at 500 °C was performed with two sets of samples one in argon environment and other is in vacuum for several hours to further improve the contact properties. The Schottky barrier diodes samples were characterized using current-voltage (I-V), capacitance-voltage (I-V), current-voltage-temperature (I-V-T), breakdown-voltage and x-ray diffraction (XRD) experiments. XRD was performed to investigate the formation phases in the interfacial layer between Ti (deposited at different temperature) and 4H-SiC. From the electrical characterizations, the barrier height, ideality factor, on-resistance, doping concentration, breakdown-voltage, and the respective interfacial composition were determined.

Schottky contacts deposited at 200 °C and annealed at 500 °C for 24 hours yield better Schottky barrier diodes with an optimum average barrier height of 1.13 eV and ideality factor of 1.04 obtained from forward bias current-voltage measurements. The diodes from same sample shows a low leakage current of 0.5 x 10⁻⁶ A at a reverse bias voltage of 850 V. the X-ray diffraction scans of the Ti/4H-SiC shows mainly two kinds of phases such as Ti₅Si₃ and Ti₃SiC₂ formed at interfacial layer.

5.2 Recommendation for future work

More analysis on processing techniques are recommended to enhance further improvements in the performance of Schottky barrier diodes. The turn-on voltage and on-resistance of the device can be further improved by investigating different cleaning processes on substrate surface. More accurate analysis using capacitance-voltage measurements are needed for this work. As mentioned the C-V measurements were performed after 60 hours of annealing so, to achieve a better understanding of variations in properties of SBD due to annealing time. The C-V measurements are needed to be performed after every interval of annealing.
The Schottky barrier diodes fabricated in this study can be further implemented into a temperature sensing applications for harsh-environments. The SBD whose Schottky contact was deposited at 200 °C exhibited a very good linearity in is forward bias I-V-T curve up to 300 °C with an optimum average barrier heights and ideality factors. So, a probe using Silicon carbide Schottky barrier diode as a temperature-sensor in the 20 °C - 300 °C range can be a further recommended work to analysis the efficiency of temperature sensor by investigating the sensitivity (change in voltage with respect to change in temperature at constant current) of the device.
APPENDICES

Appendix 1: Calculation of Barrier Height and Ideality Factor for the Schottky Contact Deposited at Room Temperature Using I-V Measurement.

The slope and intercept values were obtained from the linear portion from the semilog I-V plots. From those values and by using Eq. 2.8 the barrier height and ideality factor are calculated. Fig. 37 shows the ln(I)-V plot of sample whose Schottky contact (Ti) deposited at 28 °C. All the experimental data are analyzed using origin-pro.

![I-V plot of a diode, Ti deposited at 28 °C](image)

**Figure 45:** I-V plot of a diode, Ti deposited at 28 °C

From the linear fit, the intercept is -24.92 and slope is 37.74 and the radius of the particular diode is 0.03 cm.
Ideality factor, \( n = \frac{q}{kT} \times \frac{1}{\text{slope}} \)

\[ = \frac{(1.6 \times 10^{-19} \text{ C})}{(1.38 \times 10^{-23} \text{ J/K} \times 300 \text{K} \times 37.71)} \]

\[ = 1.02 \]

Barrier Height, \( \Phi_B = [\ln(AA^*T^2) - \text{intercept}] \frac{kT}{q} \)

\[ = \ln(2.83 \times 10^{-4} \text{cm}^2 \times 146 \text{cm}^{-2} \text{k}^{-2} \times 300^2 \text{k}^2) + 23.38) \]

\[ = 0.91 \text{ eV}. \]

**Appendix 2: Calculation of the Barrier Height and Doping Concentration for the Schottky Contact Deposited at Room Temperature Using C-V Measurement**

The barrier height and doping concentration values were determined from the intercept and slope of the C-V graph. Eq. 2.14 is used to find the barrier height and doping concentration. Fig. 38 shows the 1/c²-V plot of sample whose Schottky contact (Ti) deposited at 28 °C.

**Figure 46:** 1/C² -V plot of a diode, Ti deposited at 28 °C
Intercept and slope of Fig. 38 are 1.799E20 and -2.203E20 and the radius of the diode is 0.03 cm. A new slope is obtained by multiplying area$^2$ of the diode with the slope.

New slope = $A^2 \times$ slope

= -1.53E15

X-intercept = -(intercept/slope)

= -(1.799E20/(-2.203E20))

= 0.816

Doping Concentration, $N_D = \frac{-2}{(\text{newslope} \times q \times k \times \epsilon_0)}$

= -2 / (-1.5310^{15} \times (1.6 \times 9.7 \times 8.85 \times 10^{-33}))

= 9.47E15 cm$^{-3}$

Barrier Height, $\Phi_B = \text{X Intercept} + \left(\frac{kT}{q}\right) \left[1 + \left(\frac{N_o}{N_D}\right)\right]$  

= 0.81 + (3\times 1.38) / (1.6 \times 10^{-2}) \ln (1 + (1.69 \times 10^{19} / 1.51 \times 10^{16}))

= 1.03 eV.

Appendix 4: Calculation of Series Resistance for the Schottky Contact Deposited at Room Temperature.

Using the I-V data, we need to find the derivative of voltage and derivative of logarithmic current. After finding those values, we need to plot the current versus $dV/d[\ln(I)]$. Fig. 39 shows the linear fit for series resistance plot, for the sample whose Schottky contact (Ti) deposited at 28 °C.
Figure 47: I-[dV/d(ln(I))] plot, Ti deposited at 28 °C

From the above plot the reciprocal of slope gives the series resistance. If we multiply the series resistance with the area of the diode we will get specific on-resistance.

Series resistance = 1/slope
    = 1/ 0.059
    = 16.82 Ω

Specific on-resistance = area of the Schottky contact × series resistance
    = 0.00229 × 16.82
    = 38.53 mΩ-cm².
References


