RF CMOS Band Pass Filters with Wide Tuning Frequency, Controllable Pass Band and High Stopband Rejection: Using Passive and Active Inductors

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ABSTRACT


With the increasing demand for high performance RF front-end modules, like multimedia handset and base station devices accommodating multiple wireless standards (2G, 2.5G, 3G, WiMAX, and LTE). Multiple IF amplifiers, mixers, RF band pass filters (BPFs), modulators and demodulators are desired to be tunable to meet dynamic standards with different frequency bands. Tunable devices with wide tuning frequency range, tuning speed, high linearity, energy conservative, high pass band gain, high stop band rejection are the paramount components in the reconfigurable RF front-end systems.

In this dissertation, first a wide tuning passive inductor band pass filter (BPF) with steep roll-off high rejection and low noise figure is presented. The design feature of steep roll-off high stopband rejection (> 20 dB) and low noise figure (< 6 dB) provides a wide tuning frequency span (1-2.04 GHz) to accept desirable signals and reject close interfering signals. Next, a process variation aware design approach is proposed to verify robustness of the BPF after calibration from process variations. By operating in 1.04 GHz tuning frequency span the BPF achieves a stable center frequency, an average maximum deviation 1.16 dB on a nominal pass band gain of 55.6 dB, and an average maximum deviation 1.06 MHz on a nominal bandwidth of 12.3 MHz.
Next, a high inductance high Q factor floating CMOS RF active inductor (AI) is proposed, which uses a resistive feedback and a negative resistance block. By changing design parameters, an active inductor designed in 1.8 V 180 nanometer CMOS process achieves a tuning inductance range from 52 nH to 1,462 nH at 1.52 GHz and a maximum Q factor of 553k at 1.27 GHz. Its wide tunable frequency span can be increased to 3.09 GHz. Its power is below 7.59 mW.

Next, an AI driven BPF is proposed, which increases the BPF tuning frequency span from the original 1.04 GHz (1.0 - 2.04 GHz) to 2.1 GHz (1.0 - 3.1 GHz) while keeps a pass band gain (21.1 ~ 28.2 dB). The AI driven BPF achieves a low noise figure (1.81~5.42 dB), a power consumption of 18.6 mW, and a high stopband rejection of 28.9 dB. The AI driven BPF tuning frequency span can be further increased to 7.74 GHz (0.39 - 8.13 GHz) with a pass band gain of 8.14 dB.

Finally, a wide tuning inductorless BPF is proposed. The BPF has two tuning frequency spans: 1) a tuning frequency span of 1.33 GHz (0.74 - 2.07 GHz) while keeping a pass band gain (2.17 - 17.04 dB), a low noise figure (6.3 - 10.2 dB), and a power of 22.6 mW, and 2) a tuning frequency span of 1.26 GHz (1.15 - 2.41 GHz) while keeping a pass band gain (4.83 - 19.7 dB), a low noise figure (7.12 to 12.5 dB), and a power of 23.4 mW.
# Table of Contents

1 INTRODUCTION .................................................................................................................. 1  
   1.1 Background ............................................................................................................... 1  
   1.2 Motivation ............................................................................................................ 3  
   1.3 Dissertation organization ...................................................................................... 5  

2 CMOS PASSIVE BPF ARCHITECTURE AND PRINCIPLE OF OPERATIONS ..... 6  
   2.1 Theory overview ..................................................................................................... 6  
      2.1.1 Common source stage with source degeneration .............................................. 6  
      2.1.2 Common gate topology .................................................................................. 10  
   2.2 BPF Architecture .................................................................................................... 12  
   2.3 Principle of Operation ............................................................................................ 13  
      2.3.1 Stage I: transconductance amplifier ............................................................... 13  
      2.3.2 Stage II: transimpedance amplifier ............................................................... 17  

3 CMOS BPF DESIGN WITH FIXED CENTER FREQUENCY AND BANDWIDTH  
   24  
   3.1 Introduction ............................................................................................................ 24  
   3.2 Implementation of traditional BPF design ............................................................ 24  

4 CMOS PASSIVE TUNABLE BPF DESIGN ...................................................................... 29
4.1 Introduction .................................................................................................................. 29
4.2 Design algorithm of tunable BPF with specified center frequency and BW ..... 29
4.3 Example for designing tunable BPF given $f_c$ (1.7 GHz) and BW (12.4 MHz). 33
4.4 Simulation results considering process variation ......................................................... 35
4.5 BPF calibration after process variation ...................................................................... 36
4.6 Summary and comparison ........................................................................................ 37

5 HIGH INDUCTANCE, HIGH Q FACTOR FLOATING CMOS RF ACTIVE INDUCTOR ........................................................................................................................................ 40
5.1 Introduction .................................................................................................................. 40
5.2 Gyrator-C AI ............................................................................................................... 41
  5.2.1 Lossless Gyrator-C active inductors ................................................................. 41
  5.2.2 Lossy Gyrator-C active inductors ..................................................................... 44
  5.2.3 Transformation between series and parallel LC for Q enhancement .......... 47
5.3 Featured Parameters of active inductor ................................................................. 49
  5.3.1 Quality factor (Q) ......................................................................................... 51
5.4 CMOS Active inductor design implementation ......................................................... 56
  5.4.1 Basic gyrator-C active inductor ................................................................. 56
  5.4.2 CMOS implementation of negative shunt resistor ....................................... 60
  5.4.3 Self-resonant frequency boosted architecture of gyrator-C active inductor 62
  5.4.4 The proposed gyrator-C based active inductor .............................................. 67
5.5 Performance analysis.................................................................................................................. 72

5.5.1 Performance of active inductor without negative resistive (NR) block..... 72

5.5.2 Performance of Active inductor using negative resistive (NR) block ...... 73

6 CMOS ACTIVE INDUCTOR BASED TUNABLE BAND PASS FILTER .......... 76

6.1 Introduction ....................................................................................................................................... 76

6.2 Active drain inductor band pass filter ................................................................................................. 76

6.2.1 Design architecture ...................................................................................................................... 76

6.2.2 Simulation results and analysis ..................................................................................................... 80

6.2.3 Monte Carlo analysis for process variations .................................................................................... 85

6.3 Inductorless BPF ............................................................................................................................. 86

6.3.1 Design architecture ...................................................................................................................... 86

6.3.2 Simulation results and analysis ..................................................................................................... 87

6.3.3 Monte Carlo analysis considering process variation ................................................................. 93

6.4 Comparison and analysis .................................................................................................................. 94

7 CONCLUSION ....................................................................................................................................... 97

7.1 Summary .......................................................................................................................................... 97

7.2 Future Research .................................................................................................................................. 99

8 REFERENCE ......................................................................................................................................... 100
List of Figures

Fig. 1.1 An example of tunable BPF in receiver architecture........................................... 2

Fig. 2.1 Single stage Common source amplifier with source degeneration: (a) Schematic; (b) Small signal model when short the output to the ground........................................ 7

Fig. 2.2 Small signal model for the degenerated common source stage including channel length modulation and body effect when the output is connected to the ground .......... 9

Fig. 2.3 Common gate topology amplifier: (a) schematic; (b) small signal model .......... 11

Fig. 2.4 Schematic of Band-Pass Filter................................................................. 13

Fig. 2.5 Notch filter in stage I: (a) schematic; (b) equivalent model for common source topology with source degeneration ........................................................................ 14

Fig. 2.6 Small signal model for notch filter in stage I: (a) before equivalent (b) after equivalent .................................................................................................................. 15

Fig. 2.7 Notch filter in stage II: (a) schematic; (b) equivalent current divider model for common gate topology.................................................................................................. 17

Fig. 2.8 Stage II: (a) common gate topology; (b) equivalent small signal model.......... 18

Fig. 2.9 Frequency response of the proposed band pass filter (solid line: stage I, virtual line: stage II) .............................................................................................................. 22

Fig. 2.10 Example of frequency response of the proposed band pass filter (f_c = 1.7 GHz and BW = 12.4 MHz, stopband rejection = 27.4 dB) ...................................................... 22

Fig. 3.1 Flow chart of traditional double notch BPF design ................................................ 25

Fig. 3.2 Pseudo code of traditional double notch BPF design ........................................ 27
Fig. 4.1 Block diagram of process variation aware tunable BPF design ........................................... 30
Fig. 4.2 Process variation aware tunable BPF design approach .................................................... 32
Fig. 4.3 Pass band gain vs. bandwidth (1.0GHz≤f_c≤2.04GHz, and 5.5 MHz≤BW≤51.2 MHz, 45.2 dB≤gain≤65.1 dB) ......................................................................................................................... 34
Fig. 4.4 is the AC simulation waveform with channel length variation (+-10%), and more details tabulated in Table 4.3. .................................................................................................................................................. 35
Fig. 4.4 AC simulation results considering process variation ........................................................ 35
Fig. 4.5 A Performance case of the tunable BPF for 12.03 MHz≤BW≤12.71 MHz (1.0 GHz≤f_c≤2.04 GHz, 52.76 dB≤gain≤59.87 dB) ................................................................................................. 38
Fig. 4.6 Noise Figure measurement for different frequency......................................................... 39
Fig. 5.1 Lossless single-ended gyrator-C active inductors. ............................................................... 41
Fig. 5.2 Three basic transconductors: (a) common source transconductor; (b) common gate transconductor; (c) Common drain transconductor.................................................................................................. 42
Fig. 5.3 Two differential pair transconductors: (a) differential pair transconductor with ideal current source; (b) differential pair transconductor with current mirror......................... 43
Fig. 5.4 Lossy single ended gyrator-C active inductors: (a) block diagram; (b) equivalent RLC model.................................................................................................................................................. 44
Fig. 5.5 Transformation between RL series and RL parallel........................................................ 48
Fig. 5.6 Bode plots for the impedance of lossy gyrator-C active inductor .............................. 51
Fig. 5.7 The relationship between Q factor and working frequency of active inductor ... 54
Fig. 5.8 Q enhancement with a negative resistor .................................................................... 56
Fig. 5.9 Simplified schematic of the basic gyrator-C active inductor: (a) T_1 and T_2 
Implemented with NMOS and PMOS; (b) T_1 and T_2 Implemented with NMOS ............... 57
Fig. 5.10 Characteristic of negative resistor ................................................................. 61
Fig. 5.11 Single-ended negative resistor: (a) block (b) schematic ...................... 62
Fig. 5.12 NMOS implementation gyrator-C active inductor ................................. 63
Fig. 5.13 Small signal model of the NMOS implementation gyrator-C active inductor .. 63
Fig. 5.14 Equivalent parallel RLC model with series resistance $R_s$ ............... 65
Fig. 5.15 Proposed architecture of gyrator-C based active inductor (a) schematic (b) NR schematic, (c) AI symbol ................................................................. 67
Fig. 5.16 Proposed gyrator-C based active inductor (a) Small signal model; (b) RLC equivalent model; (c) AI symbol ................................................................. 68
Fig. 5.17 AI Inductance vs signal frequency for different $V_{la}$ ............................. 72
Fig. 5.18 Q factor and inductance of AI without NR ............................................. 73
Fig. 5.19 Q factor and inductance of AI using NR block ..................................... 74
Fig. 5.20 Inductance tuning range for different bias voltage $V_{la}$ ....................... 74
Fig. 6.1 Active drain inductor band pass filter ......................................................... 76
Fig. 6.2 Proposed architecture of active inductor (AI): (a) schematic of AI; (b) schematic of NR; (c) AI symbol ................................................................. 77
Fig. 6.3 A Performance of the tunable BPF without AI for 12.0 MHz ≤ $BW$ ≤ 12.7 Hz (1.0 GHz ≤ $f_C$ ≤ 2.04 GHz, 52.8 dB ≤ gain ≤ 59.9 dB) ........................................... 80
Fig. 6.4 A Performance of the tunable BPF with AI for 4.7 Hz ≤ $BW$ ≤ 83.2 MHz (0.39 GHz ≤ $f_C$ ≤ 8.1 GHz, 8.14 dB ≤ gain ≤ 22.5 dB) ........................................... 81
Fig. 6.5 Pass band gain vs. bandwidth (0.389 GHz ≤ $f_c$ ≤ 8.13 GHz, and 3.42 Hz ≤ $BW$ ≤ 95.7 MHz, 7.56 dB ≤ gain ≤ 28.2 dB) ......................................................... 83
Fig. 6.6 Noise figure measurement of AI driven BPF for different center frequencies ranging from 1.0 GHz to 3.09 GHz ................................................................. 83

Fig. 6.7 Inductorless band pass filter ................................................................................. 86

Fig. 6.8 block diagram for the active inductors ................................................................. 86

Fig. 6.9 Performance of the inductorless tunable BPF when sweeps bias voltage $V_{la1}$
from 1.34 to 1.8 volts and keeps $V_{dd}=1.8$ volts, $V_{dd1}=1.8$ volts, $V_{lb1}=1.05$ volts ...... 88

Fig. 6.10 Performance of the inductorless tunable BPF when sweep bias voltage $V_{lb1}$
from 0.77 to 1.4 volts and keeps $V_{dd}=1.8$ volts, $V_{dd1}=1.8$ volts, $V_{la1}=1.4$ volts ........ 89

Fig. 6.11 Performance of the inductorless tunable BPF when sweep bias voltage $V_{la1}$
(1.6 to 3.3 volts) and keeps $V_{dd}=3.3$ volts, $V_{dd1}=1.8$ volts, $V_{lb1}=1.4$ volts ............. 90

Fig. 6.12 Performance of the inductorless tunable BPF when sweep bias voltage $V_{lb1}$
from 0.6 to 3.2 volt and keeps $V_{dd}=3.3$ volts, $V_{dd1}=1.8$ volts, $V_{la1}=1.8$ volts.............. 91

Fig. 6.13 Noise figure measurements of different frequencies sweeping $V_{la1}$ and $V_{lb1}$
($V_{dd}=1.8$ volts, $V_{dd1}=1.8$ volts) .................................................................................. 91

Fig. 6.14 Noise figure measurements of different frequencies sweeping $V_{la1}$ and $V_{lb1}$
($V_{dd}=3.3$ volts, $V_{dd1}=1.8$ volts) .................................................................................. 92

Fig. 6.15 Noise Figure (NF) comparison among passive inductor BPF, active drain
inductor BPF and inductorless BPF .................................................................................... 95

Fig. 6.16 Tuning span comparison among different types of BPF. Note: BPF1 (passive
inductor BPF); BPF2-C1/C2 (active drain inductor BPF with different tuning span);
BPF3-C1 (inductorless BPF sweep $V_{la1}$); BPF3-C2 (inductorless BPF sweep $V_{lb1}$).... 96
Fig. 6.17 Passband gain comparison among different types of BPF. Note: BPF1 (passive inductor BPF); BPF2-C1/C2 (active drain inductor BPF with different tuning span); BPF3-C1 (inductorless BPF sweep Vla1); BPF3-C2 (inductorless BPF sweep Vlb1).... 96
List of Tables

Table 3.1 Transistor size information ................................................................. 27
Table 4.1 Initial design look-up table of inductors obtaining peak gain .................. 31
Table 4.2 Final transistor sizes and parameters based on the results from Chapter 3 ...... 34
Table 4.3 BPF $f_c$, $A_v$ and BW considering process variations ................................. 35
Table 4.4 Tunable BPF BW comparison with and without calibration after process
variants .................................................................................................................. 37
Table 4.5 Performance summary and comparisons ................................................... 38
Table 5.1 AI performance summary and comparison ................................................. 75
Table 6.1 BPF performance summary and comparison .............................................. 81
Table 6.2 Performance comparison of BPF w/o AI and BPF with AI ......................... 84
Table 6.3 Active drain inductor BPF $f_c$, $A_v$ and BW considering process variations ...... 85
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1 INTRODUCTION

1.1 Background

With the increasing demand for high performance RF front-end modules, like multimedia handset and base station devices accommodating multiple wireless standards (2G, 2.5G, 3G, WiMAX, Mobile WiMAX, LTE, and LTE-A). Multiple IF amplifiers, mixers, RF band pass filters (BPFs), modulators and demodulators are designed to be tunable so as to be more flexible and dynamic to meet these requirements since the standards work on different frequency bands. Adding another set of customized RF front-end devices would result in extra complexity and power consumption when mobile devices are upgraded to support future standards [1]. The power consumption prevents users from roaming freely among different networks if no effective measures are taken into the mobile device.

On the contrary, if reconfigurable handsets are used, it will minimize duplicated RF front-end components and hence reduce energy and cost in the market place. Other application such as cognitive radio in the TV-bands, narrow spectral holes may exist between strong incumbent TV transmitter signals [2]. Tunable band pass and band reject filters provide a good solution to pre-tune desired signals while reject interfering signals. In order to avoid blocking of the receiver it is desirable to reject the strong signals by using a filter of high linearity and high Q. For example, Q = 50 for 10
MHz bandwidth around a tunable frequency range of 500 MHz in reconfigurable RF applications.

Fig. 1.1 An example of tunable BPF in receiver architecture

Although off-chip mixers and passive IF amplifiers provide these properties, the proposed integrated CMOS alternatives with wide tunable center frequency and pass band are highly desirable for this solution will naturally reduce the Size, Weight and Power (SWaP) with all additional benefits this entails. To the same extent tunable power amplifiers, tunable antennas, tunable band pass filters, and tunable matching networks with wide tuning frequency range, tuning speed, high linearity, energy conservative, high gain are the paramount functions in reconfigurable RF front-end systems. For example, as shown in Fig. 1.1, a tunable band pass filter (TBPF) can function as a band pass filter (BPF) and an intermediate frequency filter (IF filter) in multiple RF channels. By tuning TBPF design parameters the TBPF can cope with mixer to operate in different RF frequency band.
1.2 Motivation

To design a wide tuning BPF in a reconfigurable RF front-end system, its tunable properties such as tunable frequency range, tunable gain, tunable center frequency, and even its relatively constant bandwidth and low noise figure while shifting the center frequency is desirable. A few of state-of-the-art techniques such as gm-C filters, Q enhanced LC filters, and N-path and pseudo N-path filters have been presented; however, these designs still have room to improve for a better band pass gain and noise figure, and a wider tuning frequency range [3-16]. The gm-C filters have the advantage of low power consumption, high frequency performance. Its weak linearity can be improved by applying linearization techniques such as resistive source degeneration, dynamic source degeneration, tunable feedback, and adaptive feedback, but its pass band gain is low or narrow tuning range [8-9]. The solution based on Q-enhanced LC band passed filter has high tuning center frequency but low band pass gain (-5 dB) and high noise figure (26.8 dB) [10]. Another Q-enhanced LC filter based design [11] was proposed for low power consumption, a relatively high frequency range of 400 MHz with a pass band gain of 23 dB. A design using high-Q N-path band pass filter was proposed [16] to achieve a wide tuning frequency range but its band pass gain is low. A novel inductor-less tunable switched-capacitor band pass filter based on N-path periodically time-variant network can operate in an ultra-wide bandwidth of 3-5 GHz but its band pass gain is low and noise figure is high [17].

The inductors play a key role in the double notch band pass filter design, since the filter is built by LC network. For the passive inductors, they take up too much silicon area and need special technology, like the thicker metal layers or a high resistivity substrate.
which results higher cost [18]. Once fabricated, the passive inductors are hard to be modified since their lack of tenability. In the fully integrated circuit design, Active Inductor (AI) in CMOS is an essential building block to function as traditional passive spiral inductor. In nowadays, the active inductors (AIs) are becoming more and more attractive in reconfigurable radio frequency front-end circuits, like the applications in band pass filters, low noise amplifier, and oscillators to support growing dynamic RF standards with different operating frequency band, since the first CMOS active inductor was proposed in 1996. These kinds of inductors overcome the shortages what the traditional passive inductors suffering: low quality factor, less tenability, and high chip area occupation. Gyrator-C architecture is a common topology to implement active inductors [19-20]; however, it has inherent weakness at low inductance-normally below 80 nH [21-23], low frequency range, and low Q factor. To increase inductance and Q factor of the gyrator-C AIs, feedback resistance [24-25] and new cascaded flipped architecture are applied [26] respectively. However, their Q factor is still not high enough to fit for the applications where high performance inductors are needed and noise figure is still high.

Hence, in this dissertation a new passive tunable BPF will be presented, which is tunable for wide tuning range, high band pass gain, low noise figure, and low power consumption. The algorithm of tunable BPF design will be also elaborately presented. The operation of this filter is inspired by a notch filter architecture [3]. The filter working in current mode is composed by two single stage filters using Q-enhanced LC resonator tanks to control the poles and zeros of the filter transfer function.
Besides, an active inductor implemented in CMOS technology, with enhanced inductance value, Q factor and inductance range will be presented in this dissertation. Then, an active inductor driven band pass filter will be proposed with relative high pass band gain, narrow pass band and wider frequency tuning range, and finally an inductorless tunable band pass filter with wide tuning range, comparable pass band gain and easy-to-tune by changing external bias voltage will be achieved. Monte Carlo simulations will be conducted to include process variations in the BPFs design, and the performances will be evaluated.

1.3 Dissertation organization

This dissertation is organized as follows. Chapter 1 introduces the background of tunable BPF and its state-of-arts design. Chapter 2 presents the passive BPF architecture and its principle of operation. Chapter 3 explains the design algorithm with fixed center frequency and band width (BW). Chapter 4 presents the design synthesis of BPF with tunable center frequency and BW, and conducts Monte Carlo analysis to account process variation. Chapter 5 presents implementation of high performance active inductor in CMOS technology and its analysis. Chapter 6 elaborates the design of CMOS active inductor driven and inductorless based tunable band pass filter. Chapter 7 summarizes the research work accomplished and future research.
2 CMOS PASSIVE BPF ARCHITECTURE AND PRINCIPLE OF OPERATIONS

2.1 Theory overview

2.1.1 Common source stage with source degeneration

In general, three types of amplifier configuration have been widely used in single stage amplifiers. They are common source stage, common gate stage, and common drain stage (also known as source follower). In accordance with different loads and the way of source connection, the single stage common source amplifier is classified to six types: common source stage with resistive load, common source stage with diode connected load, common source stage with current source load, common source stage with triode load, common source stage with resistive load, common source stage with source degeneration.

The configuration of common source stage with source degeneration has good linearity and is used in double notch filter design proposed in this dissertation. Hence, its operating principle is first discussed. Note that the square law dependency of the drain current with respect to the overdrive voltage \((V_{gs} - V_t)\) results in a bunch of nonlinearity, which can be alleviated by adding a resistor in series with the source terminal. The degeneration resistor is shown in Fig. 2.1, where an increase in \(V_{in}\) will result in an increase in \(I_D\) and also an increase in voltage drop across \(R_s\). Hence, the increase in \(V_{gs}\) is smaller than that.
Fig. 2.1 Single stage Common source amplifier with source degeneration: (a) Schematic; (b) Small signal model when short the output to the ground

of the original circuit without $R_s$. Therefore, $\nabla V_{gs}$ is a small fraction of $\nabla V_{in}$. Next, both large and small signal analysis are conducted. For the large signal analysis: we define the equivalent transconductance of the circuit as $G_m$, and assume $I_D = f(V_{GS})$, then,

$$G_m = \frac{\partial I_D}{\partial V_{in}} = \frac{\partial f}{\partial V_{GS}} \frac{\partial V_{GS}}{\partial V_{in}} \quad \text{(2.1)}$$

Considering $V_{GS} = V_{in} - I_D R_S$, and $\partial f/\partial V_{GS}$ is the transconductance of $T_1$, denoted as $g_m$, then $G_m$ is rewritten as,

$$G_m = (1 - R_S \frac{\partial I_D}{\partial V_{in}}) \frac{\partial f}{\partial V_{GS}} \quad \text{(2.2)}$$

$$= (1 - R_S G_m) g_m \quad \text{(2.3)}$$

Finally, $G_m$ can be expressed by
\[ G_m = \frac{g_m}{1+g_m R_S} \]  

(2.4)

For the small signal analysis: consider the small signal model in Fig. 2.1(b), the drain current is given by,

\[ I_D = g_m V_1 = g_m (V_{in} - I_D R_S) \]  

(2.5)

Then,

\[ I_D = G_m V_{in} = \frac{g_m V_{in}}{1+g_m R_S} \]  

(2.6)

For \( I_D = G_m v_{in} \), we get

\[ G_m = \frac{g_m}{1+g_m R_S} \]  

(2.7)

\[ = \frac{1}{1/g_m + R_S} \]  

(2.8)

This result for the equivalent transconductance is the same as the one obtained using large signal analysis. Therefore, without considering channel length modulation and body effect, the small signal voltage gain is given by

\[ A_v = -G_m R_D \]  

(2.9)

\[ = -\frac{g_m R_D}{1+g_m R_S} \]  

(2.10)

From Eq. (2.8), we observe that \( G_m \) becomes a weaker function of \( g_m \) when \( R_S \) increases, and so as the drain current. If \( R_S \gg 1/g_m \), then \( G_m \approx 1/R_S \), and \( \Delta I_D \approx \Delta V_{in}/R_S \), which indicates that most of the change in \( V_{in} \) appears across \( R_S \), and the drain current is a linear function of the input voltage.
In reality, the channel length modulation and body effect are considered. Fig. 2.2 depicts the equivalent small signal model for the source degenerated common source stage amplifier, considering the channel length modulation and body effect. It is realized that the current through $R_S$ equals $I_{out}$ when the output is connected to the ground. Hence, we get,

$$V_{in} = V_1 + I_{out}R_S$$  \hspace{1cm} (2.11)

$$I_{out} = g_mV_1 + g_{mb}V_{bs} + (0 - V_s)R_S$$  \hspace{1cm} (2.12)

$$= g_m(V_{in} - I_{out}R_S)R_S + g_{mb}(-I_{out}R_S) + (0 - I_{out}R_S)/r_{ds}$$  \hspace{1cm} (2.13)

Then the equivalent transconductance $G_m$ is given by
If $R_S \ll r_{ds}$ and the body effect is negligible, Eq. (2.15) can be simplified as Eq. (2.7).

2.1.2 Common gate topology

In the common gate configuration, the input signal is applied to the source terminal instead of the gate terminal like common source and common drain configurations. It takes the input signal at the source and generates the output signal at the drain. It has lower input impedance due to the body effect, which is covered in the following discussion. Meanwhile, the common gate configuration can transfer a low input impedance to a high output impedance and therefore avoid signal reflection in transmission line. The common gate configuration is used in double notch filter design proposed in this dissertation.

Fig 2.3 shows the schematic and small signal model of common gate configuration considering the channel length modulation and body effect, where $V_1 = -V_{in}, V_{bs} = V_1$ and the current through $r_{ds}$ is given by,

\begin{align*}
I_{r_{ds}} &= I_{in} + g_m V_1 + g_{mb} V_1 \\
&= I_{in} - (g_m + g_{mb})V_{in}
\end{align*}

Then, we get
\[ V_{in} = (I_{in} - (g_m + g_{mb})V_{in})r_{ds} + I_{in}R_D \]  

(2.18)

Hence, the input impedance from the source terminal is given by

\[ R_{in} = \frac{V_{in}}{I_{in}} = \frac{R_D + r_{ds}}{1 + (g_m + g_{mb})r_{ds}} \]  

(2.19)

Fig. 2.3 Common gate topology amplifier: (a) schematic; (b) small signal model

If \((g_m + g_{mb})r_{ds} \gg 1\), Eq. (2.19) is rewritten as,

\[ R_{in} \approx \frac{R_D}{(g_m + g_{mb})r_{ds}} + \frac{1}{g_m + g_{mb}} \]  

(2.20)

Note that if \(R_D\) is the resistor of an ideal current source, then input impedance will be infinite; if \(R_D\) small, the channel length modulation will be negligible, the drain to source resistance of \(m_1\) \(r_{ds}\) is infinite. Thus, Eq. (2.20) is simplified to

\[ R_{in} \approx \frac{1}{g_m + g_{mb}} \]  

(2.21)
If the body effect is neglected, the input impedance from the source of transistor $m_1$ is further simplified to

$$R_{in} \approx \frac{1}{g_m}$$ (2.22)

These analysis results will be used in the proposed double notch band pass filter design.

### 2.2 BPF Architecture

Based on the theory presented in the previous section, a double notch band pass filter is proposed. The proposed tunable band pass filter with differential cascade architecture is divided to two stages: the transconductance stage (stage I) and the transimpedance stage (Stage II). The transconductance stage converts input voltage $V_{INP}$ and $V_{INN}$ to output current $I_P$ and $I_N$ respectively, while the transimpedance stage converts input current $I_P$ and $I_N$ to output voltage $V_{OPP}$ and $V_{OPN}$ respectively, as shown in Fig. 2.4. Actually, the stage I is built by the common source topology with source degeneration ($T_1$ for one differential side and $T_2$ for the other differential side, the transistor $T_9$ and $T_{10}$ serve as source resistor of $T_1$ and $T_2$ respectively, $T_{11}$ and $T_{12}$ serve as the load of $T_1$ and $T_2$ respectively), while the stage II is built by the common gate topology ($T_{11}$ for one differential side and $T_{12}$ for the other differential side, the inputs to the source of $T_{11}$ and $T_{12}$ are the outputs of $T_1$ and $T_2$ from stage I).

$I_1, I_2$ and $I_3$ are the bias current to provide appropriate bias voltage for transistors $T_6, T_7, T_9, T_{10}, T_{16}$ and $T_{17}$. The transistor pairs $T_3/T_4$, and $T_{13}/T_{14}$ provide differential negative resistance for Q enhancement of the band pass filter. The operating principle in
detail will be discussed later. For convenient, we just discuss one differential side, e.g. Positive side ($T_1$ and $T_{11}$), since the other differential side has the same analysis.

![Schematic of Band-Pass Filter](image)

**Fig. 2.4 Schematic of Band-Pass Filter**

### 2.3 Principle of Operation

#### 2.3.1 Stage I: transconductance amplifier

To better introduce the principle of operation, the tunable BPF also called double notch filter composed by two single notch filters with LC parallel series resonant combination, as sketched in Fig. 2.5. The input LC impedance for parallel series resonant combination in stage I is expressed as $Z_{N1}$, and the input LC impedance for parallel series resonant combination in stage II is expressed as $Z_{N2}$, the impedance observing from the drain of transistor $T_9$ is $R_{o9}$. The input impedance looking into the source of transistor $T_{11}$
in the common gate topology of stage II is approximated as $1/g_{m11}$, the reason can be found in section 2.1.2. The output voltage of stage I is denoted as $v_X$. The equivalent small signal model is depicted in Fig. 2.5, where $I_P$ is the drain current of transistor $T_9$ after V-I conversion, $g_{m1}$ is the transconductance of transistor $T_1$ regarding the conversion from $v_{gs1}$ to $I_P$, $G_{m1}$ is the equivalent transconductance of transistor $T_1$ regarding the conversion from $v_{inp}$ to $I_P$. The input impedance $Z_{N1}$ is expressed as Eq. (2.23).

$$Z_{N1} = \frac{1+s^2L_{N1}(C_{N1}+C_{P1})}{SC_{N1}(1+s^2L_{N1}C_{P1})} \tag{2.23}$$

Similarly we get,

$$Z_{N2} = \frac{1+s^2L_{N2}(C_{N2}+C_{P2})}{SC_{N2}(1+s^2L_{N2}C_{P2})} \tag{2.24}$$

Fig. 2.5 Notch filter in stage I: (a) schematic; (b) equivalent model for common source topology with source degeneration
Considering the parallel series LC network, its parallel resonant frequency \( f_{p1} \) is higher than the zero frequency \( f_{z1} \), as shown below:

\[
f_{p1} = \frac{1}{2\pi \sqrt{L_{N1} C_{P1}}} \tag{2.25}
\]

\[
f_{z1} = \frac{1}{2\pi \sqrt{L_{N1} (C_{N1} + C_{P1})}} \tag{2.26}
\]

As shown in Fig. 2.5, the resistor \( 1/g_{m11} \) and the equivalent impedance \( Z_{N2} \) are in parallel, and the resistor \( R_{o9} \) and the equivalent impedance \( Z_{N2} \) are in parallel. In this way, Fig. 2.5(a) is simplified as Fig. 2.5(b), where

\[
R_D = \frac{1}{g_{m11}} // Z_{N2} \tag{2.27}
\]

\[
= \frac{Z_{N2}}{1 + g_{m11} Z_{N2}} \tag{2.28}
\]

\[
R_{S1} = R_{o9} // Z_{N1} \tag{2.29}
\]

Fig. 2.6 Small signal model for notch filter in stage I: (a) before equivalent (b) after equivalent
Where $R_{o9}$ is the resistance of current source ($T_9$), and it approaches infinite, thus we get

$$R_{S1} \approx Z_{N1} \quad (2.30)$$

Fig. 2.6(a) shows the small signal model of notch filter with before equivalent, since it is a model for common source topology with source degeneration, it can be simplified as the model sketched in Fig. 2.6(b) after equivalent. The equivalent transconductance $G_{m1}$ is given by (see Eq. 2.31)

$$G_{m1} = \frac{g_{m1}}{1 + g_{m1}Z_{N1}} \quad (2.31)$$

Hence, from Fig. 2.30(b), the output drain current $I_P$ is obtained,

$$I_P = G_{m1}V_{inp} = \frac{g_{m1}V_{inp}}{1 + g_{m1}Z_{N1}} \quad (2.32)$$

Similarly, we have

$$I_N = G_{m2}V_{inn} = \frac{g_{m2}V_{inn}}{1 + g_{m2}Z_{N}} \quad (2.33)$$

Considering $T_1$ and $T_2$ have the same dc current going through and have the same size, according to $g_{m1} = \sqrt{2I\beta}$, we get $g_{m1} = g_{m2} = g_m$. Hence, the output current $I_{op} (= I_P - I_N)$ of the transconductance stage is simply given by,

$$I_{op} = G_{m2}V_{in} = \frac{g_mV_{in}}{1 + g_mZ_{N1}} \quad (2.34)$$

Combine Eq. (2.30) and (2.32), the output voltage $v_X$ is given by,

$$v_X = -I_P R_D = -\frac{g_{m1}V_{inp}}{1 + g_{m1}Z_{N1}} \frac{Z_{N2}}{1 + g_{m11}Z_{N2}} \quad (2.35)$$
2.3.2 Stage II: transimpedance amplifier

As shown in Fig. 2.7(a), $I_D$ is the drain current serving as the driver of common gate amplifier, $I_N$ is the current feeding from the LC parallel series resonant combination, and $I_D$ is the current going through transistor $T_1$. Note that the impedance seen from the source of $T_{11}$ and the input impedance of the LC parallel series combination are in parallel, hence, apply current divider in Fig. 2.7(b), $I_D$ is given by,

$$I_D = \frac{Z_{N2}}{\frac{1}{g_{m11}} + Z_{N2}} I_P$$

Substitute Eq. (2.32) into (2.37), we get,

$$I_D = \frac{g_{m11} Z_{N2} + g_{m1} V_{in}}{1 + g_{m11} Z_{N2} + 1 + g_{m1} Z_{N1}}$$

$$I_D = -\frac{g_m V_{inp} Z_{N2}}{(1+g_{m1} Z_{N1})(1+g_{m2} Z_{N2})}$$

(2.36)
Then, the output for the positive side is obtained,

\[ V_{opp} = -I_D s L_D \]  \hfill (2.39)

\[ = - \frac{g_{m11} Z_{N2}}{1 + g_{m11} Z_{N2}} \frac{g_{m1} V_{inp}}{1 + g_{m1} Z_{N1}} s L_D \]  \hfill (2.40)

\[ = - \frac{sL_D g_m^2 Z_{N2} V_{inp}}{(1+g_m Z_{N2})(1+g_m Z_{N1})} \]  \hfill (2.41)

Similarly, we get the output for the negative side,

\[ V_{opn} = - \frac{sL_D g_m^2 Z_{N2} V_{inn}}{(1+g_m Z_{N2})(1+g_m Z_{N1})} \]  \hfill (2.42)

Assume \( V_{in} = V_{inp} - V_{inn} \), the differential output is given by,

\[ V_{op} = V_{opn} - V_{opp} \]  \hfill (2.43)

\[ = \frac{sL_D g_m^2 Z_{N2} V_{in}}{(1+g_m Z_{N2})(1+g_m Z_{N1})} \]  \hfill (2.44)

Fig. 2.8 Stage II: (a) common gate topology; (b) equivalent small signal model
The same result can be achieved by using the common gate topology with voltage input signal ($V_x$), as shown in Fig. 2.8(a). In accordance with the small signal model sketched in Fig. 2.8(b), without considering channel length modulation and body effect the output $V_{opp}$ is given by,

$$v_{opp} = sL_D I_x$$  \hspace{1cm} (2.45)

$$= -sL_D g_{m11} V_1$$  \hspace{1cm} (2.46)

$$= sL_D g_m V_x$$  \hspace{1cm} (2.47)

Substitute Eq. (2.36) to Eq. (2.47), we get,

$$v_{opp} = -\frac{sL_D g_m^2 V_{in}}{(1+g_m^2 Z_{N2})(1+g_m^2 Z_{N1})}$$  \hspace{1cm} (2.48)

According to the same procedures as discussed from Eq. (2.42) to Eq. (2.45), the final differential output $V_{op}$ of the double notch filter is derived,

$$v_{op} = \frac{sL_D g_m^2 V_{in}}{(1+g_m^2 Z_{N2})(1+g_m^2 Z_{N1})}$$  \hspace{1cm} (2.49)

Which gives the same output result as the one obtained using current divider technique.

The parallel series combination with different impedance value $L_{N2}$, $C_{N2}$, $C_{P2}$ is applied in the transimpedance stage. Hence, the input impedance of the second LC stage is given by,

$$Z_{N2} = \frac{1+s^2 L_{N2}(C_{N2}+C_{P2})}{s(C_{N2}+s^2 L_{N2} C_{P2})}$$  \hspace{1cm} (2.50)

The resonant frequencies are expressed as
\[ f_{P2} = \frac{1}{2\pi \sqrt{L_{N2} C_{P2}}} \]  
(2.51)

\[ f_{Z2} = \frac{1}{2\pi \sqrt{L_{N2} (C_{N2} + C_{P2})}} \]  
(2.52)

From Eq. (2.44), the differential output voltage \( v_{op} \) of the transimpedance filter stage is also written as,

\[ v_{op} = sL_D \frac{g_m Z_{N2}}{1 + g_m Z_{N2}} I_{op} \]  
(2.53)

When \( f = f_{Z1} \), \( Z_{N1} \) is nearly zero, and when \( f = f_{P1} \), \( Z_{N1} \) is infinite. Therefore, the output current \( I_{op} = I_P - I_N = \frac{g_m v_{IN}}{1 + g_m Z_{N1}} \) discussed in Eq. (2.34) can be approximated as

\[ I_{op} \approx \begin{cases} g_m v_{IN} & \text{when } f = f_{Z1} \\ 0 & \text{when } f = f_{P1} \end{cases} \]  
(2.54)

Similarly, \( Z_{N2} \) is nearly zero when \( f = f_{Z2} \), and \( Z_{N2} \) is infinite when \( f = f_{P2} \). Hence the differential output voltage in Eq. (2.53) is given by

\[ v_{op} \approx \begin{cases} 0 & \text{when } f = f_{Z2} \\ sL_D I_{op} & \text{when } f = f_{P2} \end{cases} \]  
(2.55)

It is observed from the Eqs. (2.23) and (2.24) that the transmission zero happens at \( f_{P1} \) in transconductance stage and happens at \( f_{Z2} \) in transimpedance stage. Meanwhile, the peak value happens at \( f_{Z1} \) in transconductance stage and at \( f_{P2} \) in transimpedance stage. Correspondingly, the peak conductance \( g_{m\max} \) and impedance \( Z_{\max} \) are achieved at \( f_{Z1} \) and \( f_{P2} \) respectively. For convenience, the final differential output (also calls overall transfer function) of the band pass filter in Eq. (2.49) is rewritten as,

\[ v_{op} = v_{IN} \frac{sL_D g_m^2 Z_{N2}}{(1 + g_m Z_{N1})(1 + g_m Z_{N2})} \]  
(2.56)
The peak output can be approximated as Eq. (2.57) when \( f \) equal to \( f_{Z1} \), and meanwhile \( f_{Z1} \) almost equal to \( f_{P2} \).

\[
v_{op} \approx \begin{cases} 
0 & \text{when } f = f_{P1} \text{ or } f_{Z2} \\
g_{max} Z_{max} v_{IN} & \text{when } f = f_{Z1} \approx f_{P2}
\end{cases}
\]  

(2.57)

Where \( g_{max} = I_{op}/v_{IN} \) and \( Z_{max} = \frac{v_{op}}{I_{op}} = sL_D \).

From Eq. (2.57) the peak gain happens at center frequency (the pole \( f_{P2} \) and the zero \( f_{Z1} \)). A wide tuning range is realized by changing \( L_{N1} \) and \( L_{N2} \). A high base band gain is achieved by maximizing \( g_{max} \) and \( Z_{max} \), which are determined by the Q factor of the inductors and by the location of the poles and zeros. The Q-factor of inductors is improved by using a cross-coupled transistor pair, creating negative impedance \(-1/g_m\) in parallel with the inductors. Hence, the Q factor can be increased by adjusting the size of transistors in the cross-coupled pair, since \( g_m = \sqrt{2I \mu_n w/L} \). The location of poles and zeros can be adjusted by varying \( C_N \) and \( C_P \).

The pole frequency is changed to slightly greater than the zero frequency by making \( C_{N1} \) much less than \( C_{P1} \) and making \( C_{N2} \) much less than \( C_{P2} \), and a steep roll-off filter is thus accomplished. Fig. 2.9 depicts the frequency response of proposed BPF in ideal case, where the solid line denotes the response from stage I, and the virtual line denotes the response from stage II. If the location of zero frequency from stage I is almost close to the the location of pole frequency from stage II (just means \( f_{P2} \approx f_{Z1} \)), the peak value will happen at the same location for stage I and II, hence the final output will be maximized. Fig. 2.10 demonstrates the example of frequency response of the proposed
BPF at $f_c = 1.7$ GHz and BW = 12.4 MHz. Its stopband rejection is 27.4 dB. Meanwhile, the middle band gain is maximized when $f_{p2} \approx f_{z1}$ by making $C_{N1} + C_{p1} \approx C_{p2}$.

Fig. 2.9 Frequency response of the proposed band pass filter (solid line: stage I, virtual line: stage II)

Fig. 2.10 Example of frequency response of the proposed band pass filter ($f_c = 1.7$ GHz and BW = 12.4 MHz, stopband rejection = 27.4 dB)
After specifically explain the principle of notch filter, the design for double notch filter will be presented in Chapter 3.
3 CMOS BPF DESIGN WITH FIXED CENTER FREQUENCY AND BANDWIDTH

3.1 Introduction

The theory of common source with source degeneration, common gate topology, the LC parallel series combination, and the overall operating principle of the double notch filter was presented in Chapter 2, which provides good guidance of the implementation in CMOS, like tells us the parameters to control the center frequency, the frequency range, the pass band gain or the band width, and etc. In digital circuits design, the methodologies and relative design tools have already been developed [27], the whole design can be completed by the automation tool. However, in analog circuit design, most of the designs are handled manually by analog design engineers, generated simplified circuit, eg, equivalent small signal model by hand calculation, then keep running spice simulator till meets the design objective. In this chapter, an intuition design procedure on how to achieve specified center frequency and band width for the double notch band pass filter is introduced.

3.2 Implementation of traditional BPF design

Fig. 3.1 depicts the traditional sizing approach of double notch BPF design with given power supply 1.8 V. Fig. 3.2 shows the pseudo code of traditional double notch BPF
At the very beginning, the DC power supply is denoted as $p_{w_0}$, while center frequency and band width is denoted as $f_{c_0}$ and $B_{W_0}$ respectively. Once identified it is
useful for the calculation of bias current I₁, I₂ and I₃ after distributing current for each branch. With the relationship of current mirror circuit, the current I₁ drives branch current I₆ and I₇; the current I₂ drives branch current I₉ and I₁₀; the current I₃ drives branch current I₁₆ and I₁₇. Note: Iᵣₓₓ is the current through the transistor Tᵣₓ. Normally, the driver current (I₁, I₂, I₃) is made by the tenth of its load current through transistor (T₆, T₇, T₉, T₁₀, T₁₆, T₁₇) for the concern of power consumption and driving ability.

---

**Given:** BPF (Fig. 2.4) with NMOS (T₁ to T₁₇), inductors (Lₙ₁, Lₙ₂, Lₜ), capacitors (Cₙ₁, Cₚ₁, Cₙ₂, and Cₚ₂), current sources (I₁, I₂, I₃), power (pw)
**Input:** Vᵢᵣn and Vᵢᵢp
**Objective:** BPF to meet a specified center frequency and bandwidth
**Output:** NMOS sizes, capacitors and inductors value

---

**Design approach: //BPF design to meet the specified center frequency and bandwidth//**
1: Specify DC power (pw₀), center frequency (f₀), bandwidth (BW₀);
2: Calculate I₁, I₂ and I₃ based on pw₀;
3: Set w₃, w₄, w₅ based on I₁, I₂ and I₃, and other transistors size;
4: Set initial value k₃(0), k₄(0) and k₅(0);
5: Given Cₙ₁, Cₚ₁, Cₙ₂, Cₚ₂, Lₙ₁, Lₙ₂ and Lₜ,
   - set Cₙ₁<<Cₚ₁ and Cₙ₂<<Cₚ₂ to make fₚ₁ a little greater than f₁ and make fₚ₂ a little greater than f₂;
   - set Cₚ₂≈Cₚ₁+Cₙ₁ to make fₚ₂≈f₂₁;
6: i=0
7: while (i<N) //Optimize k₃, k₄, k₅ in N iterations
8: {k₃(i)=k₃(0)+(k₃ₘₐₓ-k₃(0))*i/N;
   k₄(i)=k₄(0)+(k₄ₘₐₓ-k₄(0))*i/N;
9: do DC simulation;
10: if |pw - pw₀| / pw > 0.01 then i= i+1 and go to step 7;
11: else exit;
12: end if
13: adjust Cₙ₁, Cₚ₁, Cₙ₂, Cₚ₂, Lₙ₁, Lₙ₂;
14: do AC simulation; //find fₚ;
15: If |fₚ - f₀| / f₀ < 0.01 then go to step 17
16: else go to step 13
17: adjust Lₜ;
18: do AC simulation; //find BW
27

19: If $|BW - BW_0| / BW_0 < 0.01$ then exit;
20: else go to step 17
21: end if;

Fig. 3.2 Pseudo code of traditional double notch BPF design

The next step involves setting width and length for transistor $T_1$ to $T_{17}$ and coefficients $k_3$ to $k_5$ for current mirror load current through $T_3$, $T_4$, $T_5$ which is pre-calculated and as tabulated in Table 3.1. The width for $T_1$ and $T_2$ are assigned by the same variable $W_1$. The width for $T_3$ and $T_4$ is assigned by the same variable $W_6$. The widths for $T_5$, $T_6$ and $T_7$ are assigned by variable $W_4$, $k_4W_4$, $k_4W_4$ respectively. The widths for $T_8$, $T_9$ and $T_{10}$ are assigned by variable $W_3$, $k_3W_3$, $k_4W_3$ respectively. The width for $T_{11}$ and $T_{12}$ is assigned by the same variable $W_2$. The width for $T_{13}$ and $T_{14}$ is assigned by the same variable $W_7$. The widths for $T_{15}$, $T_{16}$ and $T_{17}$ are assigned by variable $W_5$, $k_5W_5$, $k_5W_5$ respectively. The initial value for $k_3$, $k_4$, $k_5$ is set to 10 and optimized after measuring the load current through transistor $(T_6$, $T_7$, $T_9$, $T_{10}$, $T_{16}$, $T_{17})$ is the tenth of its driver current $(I_1$, $I_2$, $I_3)$.

Table 3.1 Transistor size information

<table>
<thead>
<tr>
<th>Transistor</th>
<th>$m_1$</th>
<th>$m_2$</th>
<th>$m_3$</th>
<th>$m_4$</th>
<th>$m_5$</th>
<th>$m_6$</th>
<th>$m_7$</th>
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<tr>
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</tbody>
</table>

Using 180 nm CMOS process, the values for $C_{N1}$, $C_{N2}$, $C_{P1}$, $C_{P2}$, $L_{N1}$ and $L_{N2}$ are calculated based on Eqs. (2.25), (2.26), (2.51) and (2.52) after transistor sizes are given. Given $C_{N1} << C_{P1}$ and $C_{N2} << C_{P2}$, $f_{P1}$ and $f_{P2}$ are set a little greater than $f_{Z1}$ and $f_{Z2}$.
respectively. Also, set \( f_{Z_1} \approx f_{P_2} \). From the first four steps in Fig. 3.1, the initial parameter setting is established. It is now necessary to do a DC simulation to check if the power consumption meets the specified value. As shown in Fig. 3.1, the proportional coefficient \( k_3 \) to \( k_5 \) will be adjusted till power requirement is met. Next, do AC simulation to check if the center frequency \( f_c \) meets the requirement. The values of \( C_{N1} \), \( C_{N2} \), \( C_{P1} \), \( C_{P2} \), \( L_{N1} \), \( L_{N2} \), and \( L_D \) will be adjusted till reach the desirable \( f_c \). Finally, adjust the drain inductor \( L_D \) and redo the AC simulation till achieve specified band width.
4 CMOS PASSIVE TUNABLE BPF DESIGN

4.1 Introduction

The traditional design approach described in Chapter 3 is sequential and complex. Iterative loops for parameter setting are time consuming and results are impacted each other for many parameter settings for transistors, capacitors and inductors. After the final design is obtained it is optimized to meet unique specifications and is hard to be modified for other customer design. In this regard, a new design approach to make BPF tunable is proposed in this chapter, which storing designed circuit parameters in library for future use to improve design reusability and productivity.

4.2 Design algorithm of tunable BPF with specified center frequency and BW

To better explain the design algorithm for tunable center frequency with constant BW, the tunable BPF design is divided into three stages. Stage A is to meet the center frequency $f_c$. Stage B is to meet the BW. Stage C is to calibrate the BPF design to meet $f_c$ and BW after process variations. They are shown in Fig. 4.1. Fig. 4.2 depicts detailed design approach in the three stages and explains how to obtain design parameters for the tunable BPF. In stage A, it is desirable to narrow the range of design parameters, which are primarily related to the center frequency. By referring to a look-up table of inductors (Table 4.1), peak pass band gain and minimum BW for different center frequencies in a
wide tuning frequency range are obtained. These parameters are obtained by design approach in Fig. 4.1. Given $f_c$ to tunable BPF design, the first step is to find the adjacent center frequency (i.e., upper $f_{c2}$ and lower $f_{c1}$) from Table 4.1. Next, find the upper $L_{N12}$ and lower inductor $L_{N11}$ from $f_{c2}$ and $f_{c1}$ respectively. For example, if $f_c = 1.7$ GHz, then $f_{c1}$ is 1.58 GHz and $f_{c2}$ is 1.78 GHz. Also, $L_{N12} = 0.5$ nH and $L_{N11} = 0.4$ nH. Thereafter, set the initial value $L_D = L_{D2}$, $L_{N1} = L_{N2} = L_{N12}$. Calculate $C_{N1}$ to $C_{P2}$ value from equations in Chapter 2. Make $C_{P22} = 1.1C_{P2}$, $C_{P21} = 0.9C_{P2}$ and do AC simulation. $L_{N1}$ and $L_{N2}$ are the primary impact factors to determine the center frequency. If $|f - f_c| > \delta_1$ (i.e., 15 MHz), decreases $L_1$ and $L_2$ by $\Delta L_{N1} = (L_{N12} - L_{N11}) / M$ and then conduct AC simulation. Otherwise, decreases the second primary impact factor $C_{P2}$ by $\Delta C_{P2} = (C_{P22} - C_{P21}) / N$ until $|f - f_c| < \delta_2$ (i.e. 1 MHz). Then, go to stage B to meet the specified bandwidth, as shown in step 11-17 in Fig. 4.3. If $BW < BW_{\min}$, then $BW$ is out of design range. Otherwise, decrease $L_D$ by $\Delta L = (L_{D2} - L_{D1}) / P$ and do AC simulation till $|BW - BW_0| < \delta_3$ (i.e., 0.1 MHz).
Then, the specified BW is met. M, N and P are the number of repeats determined by the accuracy ($\delta_1, \delta_2, \delta_3$) in simulation.

Table 4.1 Initial design look-up table of inductors obtaining peak gain and minimum BW for different center frequencies

<table>
<thead>
<tr>
<th>$L_{N1}$ (nH)</th>
<th>$L_{N2}$ (nH)</th>
<th>$L_{D}$ (nH)</th>
<th>$f_c$ (GHz)</th>
<th>$BW_{min}$ (MHz)</th>
<th>Peak gain (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.30</td>
<td>1.30</td>
<td>281.0</td>
<td>1.00</td>
<td>5.34</td>
<td>65.3</td>
</tr>
<tr>
<td>1.10</td>
<td>1.10</td>
<td>269.4</td>
<td>1.07</td>
<td>5.47</td>
<td>69.3</td>
</tr>
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<td>1.00</td>
<td>1.00</td>
<td>210.0</td>
<td>1.15</td>
<td>5.85</td>
<td>68.3</td>
</tr>
<tr>
<td>0.90</td>
<td>0.90</td>
<td>196.0</td>
<td>1.20</td>
<td>6.33</td>
<td>64.7</td>
</tr>
<tr>
<td>0.80</td>
<td>0.80</td>
<td>183.0</td>
<td>1.26</td>
<td>6.14</td>
<td>67.8</td>
</tr>
<tr>
<td>0.70</td>
<td>0.70</td>
<td>169.0</td>
<td>1.35</td>
<td>6.87</td>
<td>66.2</td>
</tr>
<tr>
<td>0.60</td>
<td>0.60</td>
<td>164.0</td>
<td>1.45</td>
<td>7.17</td>
<td>66.3</td>
</tr>
<tr>
<td>0.50</td>
<td>0.50</td>
<td>136.0</td>
<td>1.58</td>
<td>7.79</td>
<td>66.1</td>
</tr>
<tr>
<td>0.40</td>
<td>0.40</td>
<td>118.0</td>
<td>1.78</td>
<td>8.92</td>
<td>65.0</td>
</tr>
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<td>0.30</td>
<td>0.30</td>
<td>93.00</td>
<td>2.04</td>
<td>9.91</td>
<td>64.9</td>
</tr>
<tr>
<td>0.20</td>
<td>0.20</td>
<td>55.00</td>
<td>2.51</td>
<td>12.4</td>
<td>63.6</td>
</tr>
<tr>
<td>0.10</td>
<td>0.10</td>
<td>27.50</td>
<td>3.55</td>
<td>16.6</td>
<td>63.1</td>
</tr>
<tr>
<td>0.05</td>
<td>0.05</td>
<td>14.20</td>
<td>5.01</td>
<td>21.4</td>
<td>62.9</td>
</tr>
</tbody>
</table>

Given: $f_c$, $BW_0$, and initial values of $L_{N1}$, $L_{N2}$, $L_{D}$.
Input: $V_{in}$ and $V_{in}$.
Objective: tunable BPF to meet $f_c$ and $BW_0$.
Output: $L_{N1}$, $L_{N2}$, $C_{P2}$.

Design approach: //Stage A to meet the specified $f_c$ (Step 1-10)//
1: Find the range of $f_c$ ($f_{c1} < f_c < f_{c2}$) in Table II;
2: Set initial values $L_{D}=L_{D2}$, $L_{N1}=L_{N2}=L_{N12}$, and set $C_{N1}$, $C_{N2}$, $C_{P1}$, $C_{P2}$, $\delta_1$, $\delta_2$, $\delta_3$, $M$, $N$, $P$, $Q$;
3: Repeat
4: do AC simulation;
5: decrease $L_{N1}=L_{N2}$ by $\Delta L_{N1}=(L_{N12}-L_{N11})/M$;
6: Until $|f-f_c|\leq \delta_1$;
7: Repeat
8: do AC simulation;
9: decrease $C_{P2}$ by $\Delta C = (C_{P22} - C_{P21})/N$;
10: Until $|f - f_c| < \delta_2$;

Design approach: //Stage B to meet the specified $BW_0$ (Step 11-17) //</br>
11: Find $f_c$ and its corresponding $BW_{\text{min}}$ in Table 4.1;
12: If $BW_0 < BW_{\text{min}}$ then break;
13: Else
14: Do {
15: decreases inductor $L_D$ by $\Delta L = (L_{D2} - L_{D1})/P$;
16: do AC simulation to find the bandwidth $BW$;
17: } While $|BW - BW_0| < \delta_3$;

Design approach: //Stage C to calibrate BPF design after considering process variations (Step 18-32)//</br>
18: Select N (i.e., N=100) cases of BPF designs with different $f_{c_0}$, $BW_0$ and $A_V$ after Stage A and B;
19: Perform Monte Carlo analysis to obtain $\mu$ and $\sigma$ for $BW$;
20: Compute $(BW - (\mu - \sigma))$; //calculate the BW deviation
21: Choose top 30% cases having the worst BW deviation and find their center frequency ($f_c$) and corresponding gain ($A_V$);
22: Compute the average of center frequency ($f_{\text{avg}}$) and gain deviation ($\Delta A_V$)
23: Compute $\Delta L_D$ from Eq. (17);
24: For $i \leftarrow 1$ to 30 //consider the top 30 cases
25: $L_{D,\text{new}}(i) = L_{D,\text{old}}(i) + \Delta L_D$;
26: do AC simulation;
27: if $BW_{\text{new}}(i) > BW_{\text{old}}(i)$ then set $BW(i) = BW_{\text{new}}(i)$;
28: else {$L_{D,\text{new}}(i) = L_{D,\text{old}}(i) - \Delta L_D$;
29: do AC simulation;
30: set $BW(i) = BW_{\text{new}}(i)$};
31: end if;
32: End for;

Fig. 4.4 Process variation aware tunable BPF design approach

\[ \Delta L_{N1} = \frac{L_{\text{larger}} - L_{\text{smaller}}}{\text{number of repeats}} = \frac{L_{N12} - L_{N11}}{M} \]  \hspace{1cm} (4.1) \]

\[ \Delta C_A = \frac{C_{\text{larger}} - C_{\text{smaller}}}{\text{number of repeats}} = \frac{C_{A2} - C_{A1}}{N} \]  \hspace{1cm} (4.2) \]

\[ \Delta L_D = \frac{L_{\text{larger}} - L_{\text{smaller}}}{\text{number of repeats}} = \frac{L_{D2} - L_{D1}}{P} \]  \hspace{1cm} (4.3) \]
4.3 Example for designing tunable BPF given $f_c$ (1.7 GHz) and BW (12.4 MHz)

Table 4.2 summarizes transistor sizes and parameter settings based on the design approach in Chapter 3. Prior to implement the tunable BPF design, the desirable center frequency $f_c$ (1.7 GHz) and BW (12.4 MHz) are specified. The number of repeats depends on the design accuracy $\delta_1$, $\delta_2$, $\delta_3$. For example, $\delta_1$, $\delta_2$, $\delta_3$ are given 15 MHz, 1 MHz and 0.1 MHz and the number of repeats M, N, P is 20, 40 and 25. As shown in Table 4.2, the center frequency $f_c$ (1.7 GHz) lies between $f_{c1}$ (1.58 GHz) and $f_{c2}$ (1.78 GHz), the corresponding inductor $L_D$ lies between $L_{D1}$ (136 nH) and $L_{D2}$ (118 nH), the inductor $L_{N1}$, $L_{N2}$ lies between $L_{N11}$ (0.4 nH) and $L_{N12}$ (0.5 nH). Therefore, set the initial value $L_D = L_{D2} = 136$ nH, $L_{N1} = L_{N2} = L_{N12} = 0.5$ nH, and $C_{N1} = 2$ pF, $C_{P1} = 18$ pF, $C_{N2} = 3$ pF, $C_{P2} = C_{N1} + C_{P1} = 20$ pF, $C_{P22} = 1.1C_{P2} = 22$ pF, $C_{P21} = 0.9C_{P2} = 18$ pF and do AC simulation. If $|f - f_0| > \delta_1 (> 15$ MHz), decreases $L_{N1}$ and $L_{N2}$ by $\Delta L = (L_{N12} - L_{N11}) / M = 0.005$ nH and then do AC simulation. Otherwise, decreases the second primary impact factor $C_{P2}$ by $\Delta C_{P2} = (C_{P22} - C_{P21}) / N = 0.1$ pF until $|f - f_c| < \delta_2 (< 1$MHz). After the specified $f_c$ is met the go to stage B to meet the specified BW = 12.4 MHz.

As shown in step 11-17 in Fig. 4.5, the first step is to find $f_c$ and its corresponding bandwidth ($BW_{\text{min}}$). If $BW < BW_{\text{min}}$ then BW is out of range. If $BW > BW_{\text{min}}$, decreases $L_D$ by $\Delta L = (L_{D2} - L_{D1}) / P = 0.84$ nH and run AC simulation. Repeat until $|BW - BW_0| < \delta_3 (< 0.1$ MHz). Then, $f_c$ (1.7 GHz) and BW (12.4 MHz) are met. The proposed BPF provides a high pass band gain between 45.2 to 65.1 dB and tunable pass band between 5.5 and 51.2 MHz while the center frequency is varied from 1.0 to 2.04 GHz, which is depicted in Fig. 4.6.
Fig. 4.7 Pass band gain vs. bandwidth (1.0GHz ≤ f_C ≤ 2.04GHz, and 5.5 MHz ≤ BW ≤ 51.2 MHz, 45.2 dB ≤ gain ≤ 65.1 dB)

Table 4.3 Final transistor sizes and parameters based on the results from Chapter 3

<table>
<thead>
<tr>
<th>T_1(um)</th>
<th>T_2(um)</th>
<th>T_3(um)</th>
<th>T_4(um)</th>
<th>T_5(um)</th>
<th>T_6(um)</th>
<th>T_7(um)</th>
<th>T_8(um)</th>
<th>T_9(um)</th>
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</thead>
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<tr>
<td>150</td>
<td>150</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>19</td>
<td>19</td>
<td>4</td>
<td>46.4</td>
</tr>
<tr>
<td>T_{10}(um)</td>
<td>T_{11}(um)</td>
<td>T_{12}(um)</td>
<td>T_{13}(um)</td>
<td>T_{14}(um)</td>
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<td>N</td>
<td>P</td>
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<td>δ_2</td>
<td>δ_3</td>
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<td>I_2(mA)</td>
<td>I_3(mA)</td>
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<td>0.1</td>
<td>50</td>
<td>300</td>
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</table>
4.4 Simulation results considering process variation

Fig. 4.8 is the AC simulation waveform with channel length variation (+10%), and more details tabulated in Table 4.3.

![Fig. 4.9 AC simulation results considering process variation](image)

Table 4.4 BPF $f_c$, $A_v$ and BW considering process variations

<table>
<thead>
<tr>
<th>fc after process</th>
<th>$f_c$ (min, max) (GHz)</th>
<th>$f_{ox}$ (min, max) (GHz)</th>
<th>$t_{ox}$ (min, max) (MHz)</th>
<th>$L_{eff}$ (min, max) (dB)</th>
<th>$t_{ox}$ (min, max) (MHz)</th>
<th>$A_v$ (min, max) (dB)</th>
<th>$L_{eff}$ (min, max) (MHz)</th>
<th>$t_{ox}$ (min, max) (MHz)</th>
<th>$A_v$ (min, max) (dB)</th>
<th>$L_{eff}$ (min, max) (MHz)</th>
<th>$t_{ox}$ (min, max) (MHz)</th>
<th>$A_v$ (min, max) (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nominal</td>
<td>(GHz)</td>
<td>(GHz)</td>
<td>(MHz)</td>
<td>(dB)</td>
<td>(MHz)</td>
<td>(dB)</td>
<td>(MHz)</td>
<td>(MHz)</td>
<td>(dB)</td>
<td>(MHz)</td>
<td>(MHz)</td>
<td>(dB)</td>
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<td>11.82, 12.4</td>
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<td>54.26, 55.5</td>
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<td>1.78, 1.78</td>
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<td>56.05, 57.1</td>
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<td>12.41, 12.9</td>
<td>12.67, 12.8</td>
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<td>2.04, 2.04</td>
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<td>59.79, 59.9</td>
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<td>0.66</td>
<td>0.76</td>
<td>0.33</td>
<td>1.06</td>
<td></td>
</tr>
</tbody>
</table>

Note: * AMD denotes average maximum deviation in comparison with its nominal value.
The performance of ten tunable BPF designs with the pass band nearly constant (12.1 - 12.6 MHz) is shown in Table 4.5. The bandwidth is 12.1 MHz, 12.3 MHz, 12.1 MHz, 12.1 MHz, 12.2 MHz, 12.3 MHz, 12.2 MHz, 12.4 MHz, 12.5 MHz, 12.6 MHz and 12.6 MHz, respectively. The center frequency is varied from 1.0 to 2.04 GHz: 1.0 GHz, 1.07 GHz, 1.15 GHz, 1.20 GHz, 1.26 GHz, 1.35 GHz, 1.45 GHz, 1.58 GHz, 1.78 GHz, and 2.04 GHz. The nominal pass band gain before considering process variations is between 53.4 and 59.9 dB. Considering process variations on $t_{ox}$, $L_{eff}$ and $v_t$ with a maximum 10% variation on its nominal value, the Monte Carlo simulation results show robustness of the BPF: zero deviation on center frequency. The average maximum deviation on pass band gain is 1.16 dB on a nominal pass band gain of 55.6 dB. And, the average maximum deviation on bandwidth is 1.06 MHz on a nominal bandwidth of 12.3 MHz.

4.5 BPF calibration after process variation

The BPF design calibration to meet the specified BW after process variation is presented in Stage C in Fig. 4.2. The initial step in stage C is to select N (i.e., N = 100) cases of different $f_c$, BW, $A_V$ and conduct Monte Carlo simulation to obtain BW’s mean ($\mu$) and standard deviation ($\sigma$). The top 30% design cases contributing to the worst deviation of (BW-(\mu-\sigma)) are selected to calculate the average center frequency ($f_{avg}$) and the corresponding gain deviation ($\Delta A_v$). Then, $\Delta L_D$ can be calculated from Eq. (4.3). Note: $\Delta L_D$ is used to calibrate $L_D$, which in turn calibrates BW. Finally, calibrated $L_D$ and calibrated BW for each case are obtained. Table 4.4 shows the tunable BPF BW comparison with and without calibration after process variations. Ten design cases of
center frequency varied from 1 to 2.04 GHz are compared. Their BW is close to 12.3 MHz. Considering the case example of $f_c = 1.35$ GHz and BW $=12.2$ MHz in Table 4.4, the bandwidth deviation BW-($\mu$-$\sigma$) before calibration is 0.88 MHz and after calibration is 0.42 MHz, which accounts for 52.3% improvement. Consider all 10 case examples, the average bandwidth deviation BW-($\mu$-$\sigma$) before calibration is 0.58 MHz and after calibration is 0.292 MHz, which accounts for 49.6% improvement.

Table 4.6 Tunable BPF BW comparison with and without calibration after process variations

<table>
<thead>
<tr>
<th>fc (GHz)</th>
<th>BW (MHz)</th>
<th>$\mu$-$\sigma$ (MHz)</th>
<th>BW-($\mu$-$\sigma$) (MHz)</th>
</tr>
</thead>
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<td>w/o calibration</td>
<td>w calibration</td>
<td>w/o calibration</td>
</tr>
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4.6 Summary and comparison

Fig. 4.10 depicts a performance case of the tunable BPF when the pass band is kept nearly constant (12.03 - 12.71 MHz). To a better understanding, five cases are presented. The center frequencies within the specified range from 1.0 GHz to 2.04 GHz are 1.0 GHz, 1.18 GHz, 1.58 GHz, 1.78 GHz and 2.04 GHz while the corresponding 3-dB BWs (denoted as dx)
Fig. 4.10 A Performance case of the tunable BPF for 12.03 MHz ≤ BW ≤ 12.71 MHz (1.0 GHz ≤ f_C ≤ 2.04 GHz, 52.76 dB ≤ gain ≤ 59.87 dB)

Table 4.7 Performance summary and comparisons

<table>
<thead>
<tr>
<th>CMOS technology (nm)</th>
<th>[5]</th>
<th>[7]</th>
<th>[17]</th>
<th>[16]</th>
<th>[12]</th>
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<td>BW (MHz)</td>
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<td>1.75-4.6</td>
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<td>2.5</td>
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<td>Freq tuning range (GHz)</td>
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<td>1.9-2.19</td>
<td>0.24-0.53</td>
<td>0.03</td>
<td>2.4-2.85</td>
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Note: * The noise figure is measured when pass band is kept nearly 12 MHz
as shown in Fig. 4.10 are 12.11 MHz, 12.03 MHz, 12.42 MHz, 12.71 MHz and 12.34 MHz, respectively. It is verified that the center frequency is tunable between 1.0 and 2.04 GHz while keep nearly constant pass band between 12.03 to 12.71 MHz. The pass band gain is between 52.76 and 59.87 dB.

Table 4.5 summarizes the performance of the proposed tunable BPF and that of other tunable RF band pass filters [5, 7, 9-14, 16, 17]. The BPF presented in this work achieves a wide tuning range from 1.0 to 2.04 GHz, a low noise figure range from 1.49 to 5.88 dB, as shown in Fig. 4.12, a low power consumption of 15 mW, and a high pass band gain from 45.2 to 65.1 dB.
5 HIGH INDUCTANCE, HIGH Q FACTOR FLOATING CMOS RF ACTIVE INDUCTOR

5.1 Introduction

Active inductors (AIs) are attractive in reconfigurable radio frequency front-end circuits whose applications in band pass filters, low noise amplifier, and oscillators have been supporting dynamic RF standards with different operating frequency band. The first CMOS AI was proposed in 1996. Since then, AI has tried to overcome the shortages of the traditional passive inductors: low Q factor, low tunability, and large area. Gyrator-C architecture was proposed to implement active inductors. However, it has inherent weakness at low inductance, low frequency range, and low Q factor. To increase inductance of the gyrator-C AI, a feedback resistance was introduced. To enhance Q factor, a cascaded flip architecture was proposed. However, their Q factors and noise figures still limit applications in reconfigurable radio frequency front-end.

In this chapter, the basic lossless gyrator-C AI block, lossy gyrator-C AI block, featured parameters of AI, negative resistor block, Q factor at the resonant frequency boosted technique, principle of operation, CMOS implementation are first discussed. Finally, a new CMOS AI using a resistive feedback and a negative resistance block is presented to enhance Q factor and equivalent inductance in a wide inductive frequency range.
5.2 Gyrator-C AI

5.2.1 Lossless Gyrator-C active inductors

A gyrator was firstly proposed in 1948 by Bernard D. H. Tellegen [30]. It is a passive, linear, lossless two-port network, comprised of resistor, capacitor, inductor, and transformer. The gyrator is built with transistors and OP amps using feedback. As shown in Fig. 5.1, two back-to-back transconductors function as a gyrator. Fig. 5.1(a) shows positive transconductance in the forward path and negative transconductance in the feedback path. Fig. 5.1(b) shows negative transconductance in the forward path and positive transconductance in the feedback path. If a gyrator port is connected to a capacitor, the gyrator is so called gyrator-C. Under the condition of infinite impedance of

![Image](image_url)

Fig. 5.1 Lossless single-ended gyrator-C active inductors.
both input/output transconductors in gyrator-C architecture and constant transconductance of the transconductors, the gyrator-C is assumed as lossless. For a better understanding, we first analyze the lossless gyrator-C architecture (Fig. 5.1 (a)). The admittance looking into $V_2$ port of the gyrator-C architecture can be written as

$$ Y = \frac{I_{in}}{V_2} = \frac{1}{s(C/G_{m1}G_{m2})} \tag{5.1} $$

Considering the admittance $Y$ of an inductor,

$$ Y = \frac{1}{j\omega L} = \frac{1}{sL} \tag{5.2} $$

So, the gyrator-C functions as a single-ended lossless inductor with its inductance as

$$ L = \frac{C}{G_{m1}G_{m2}} \tag{5.3} $$

Thus, the gyrator-C can be used to implement an inductor, which is so called gyrator-C active inductor. From Eq. (5.3), the inductance of gyrator-C active inductor is inversely

![Fig. 5.2 Three basic transconductors: (a) common source transconductor; (b) common gate transconductor; (c) Common drain transconductor.](image)
Two differential pair transconductors: (a) differential pair transconductor with ideal current source; (b) differential pair transconductor with current mirror proportional to $G_{m1}G_{m2}$ and is proportional to the load capacitance C. Also, the gyator-C active inductor is inductive over the entire frequency spectrum in this gyator-C architecture.

A desirable AI is to operate in a wide frequency span and consume low power and small area. For this reason, the transconductors in the gyator-C architecture will be implemented in an effective and simple structure. Three basic transconductors that have been used in implementation of the gyator-C AI are shown in Fig. 5.2. Two differential pair transconductors are shown in Fig. 5.3. Among these transconductors only the transconductance value of common source transconductor is negative; the rest ones are all positive. How to determine the sign of transconductance value? For example, for the common gate (Fig. 5.2(b)), increasing $v_{in}$ will decrease $i_D$ and therefore increase $i_o$ for $i_o = J - i_D$. Thus we call the common gate transconductor has a positive
transconductance. Similar analysis can be applied to the differential-pair transconductor (Fig. 5.3(a)). Increasing $v_{in}$ will increase $I_{D1}$ and therefore decrease $I_{D2}$ for $I_{D2} = J_3 - I_{D1}$. Finally, $i_o$ is increased for $i_o = J_2 - I_{D2}$. Therefore, the transconductance value of the differential pair transconductor is positive.

5.2.2 Lossy Gyrator-C active inductors

As discussed in the above section, the gyrator-C architecture is ideally lossless when both input and output impedance of the transconductors are infinite and the

![Diagram of Lossy Gyrator-C active inductors](image)

Fig. 5.4 Lossy single ended gyrator-C active inductors: (a) block diagram; (b) equivalent RLC model
transconductance of transconductors are kept constant. But in reality when AI is in use neither of the input nor the output impedance of the transconductor is infinity. The AI is not lossless, which restrict its inductive function in a certain frequency range. Fig. 5.4(a) shows the lossy gyrator-C architecture, where \( R_{o1} \) and \( R_{o2} \) are the total impedance seen from the nodes a and b.

\( R_{o1} \) in virtue of the finite input impedance of the transconductor 1, while \( R_{o2} \) in virtue of the finite input impedance of the transconductor 2. Fig. 5.4(b) is the RLC equivalent model of lossy gyrator-C architecture, where \( R_p \) is the parasitic parallel resistance, \( C_p \) is the parallel capacitance, \( R_s \) is the series resistance and \( L \) is the equivalent inductance of active inductor. To be simplified in mathematic analysis, the transconductance of the transconductors is assumed constant value. Applying KCL in node a and node b, we obtain,

Node a: \((sC_1 + 1/R_{o1})V_a - G_{m1}V_b = 0\) (5.4)

Node b: \(I_{in} + G_{m2}(0 - V_a) - (sC_2 + 1/R_{o2})V_a = 0\) (5.5)

Seen from the port 2 of the gyrator-C architecture, the admittance \( Y = I_{in}/V_b \). Combining Eq. 5.4 and 5.5, we obtain

\[
Y = sC_2 + \frac{1}{R_{o2}} + \frac{1}{s\sigma_{m1}\sigma_{m2}} + \frac{1}{\sigma_{m1}\sigma_{m2}R_{o1}}
\] (5.6)

Fig. 5.4(b) depicts the RLC parallel network. Its admittance \( Y' \) is written as,

\[
Y' = sC_p + \frac{1}{R_p} + \frac{1}{R_s+sL}
\] (5.7)

Fig. 5.4(b) is an equivalent model of Fig. 5.4(a), which means \( Y = Y' \). So,
From Eq. (5.8), $R_S$ is inversely proportional to $G_{m1}$, $G_{m2}$, and $R_{o1}$. From Eq. (5.9), $R_p$ is determined by $R_{o2}$ and $C_p$ is determined by $C_2$. It’s shown in Eq. (5.10) that the inductance of gyrator-C active inductor is independent from the input and output impedance of the transconductor. It is directly proportional to $C_1$ and inversely proportional to $G_{m1}$ and $G_{m2}$. From the above analysis, the small signal of the gyrator-C active inductor can be completely modeled by an equivalent parallel RLC in which the center frequency (resonant frequency of the active inductor), Q factor, and bandwidth can be analyzed. The Q factor is affected by the finite input and output impedance of the transconductors in the gyrator-C. Q-enhanced techniques are discussed in the following section.

The impedance $Z_{total}$ looking into the port b of RLC parallel circuit in Fig. 5.4(b) is given by,

$$Z_{total} = R_p // Z_{C_p} // (R_S + Z_L)$$

$$= \frac{R(Z_L+R_S)Z_{C_p}}{R(Z_L+R_S)+Z_{C_p}(Z_L+R_S)}$$

$$= \frac{R}{1\pm \frac{RR_S}{R_S^2+\omega_L^2} \pm \frac{jR}{R_S^2+\omega_L^2} \pm \frac{1}{R_S^2+\omega_L^2}}$$

$$= \frac{R}{\frac{R}{R_S^2+\omega_L^2} + \frac{1}{R_S^2+\omega_L^2}}$$

$$= \frac{1}{1 + \frac{R}{R_S^2+\omega_L^2}}$$ (5.11)
From Eq. (5.11), let the term \( \omega c (R_s^2 + \omega^2 L^2) - \omega L \) equal zero, the resonant frequency is obtained when \( \omega c (R_s^2 + \omega^2 L^2) - \omega L \) equals to zero.

\[
f_0 = \frac{1}{2\pi} \sqrt{\frac{1 - \frac{C_p R_s^2}{L C_p}}{L C_p}}
\] (5.12)

Combine Eq. (5.9), (5.10) and (5.12).

\[
f_0 = \frac{1}{2\pi} \sqrt{\frac{c_1 - c_2 R_s^2}{c_1^2 c_2}} \frac{1}{\sqrt{\frac{G_m G_m}{G_m G_m}}}
\] (5.13)

If \( R_s \) is small and negligible, Eq. (5.13) can be simplified as

\[
f_0 = \sqrt{\frac{1}{L C_p}} = \frac{1}{2\pi} \sqrt{\frac{G_m G_m}{c_1 c_2}}
\] (5.14)

Consider the cut off frequency \( \omega_{t1} \) and \( \omega_{t2} \) of the transconductors.

\[
\omega_{t1} = \frac{G_m}{c_1} ; \quad \omega_{t2} = \frac{G_m}{c_2}
\] (5.15)

The self-resonant frequency \( f_0 \) in Eq. (5.14) can be expressed as

\[
f_0 = \frac{1}{2\pi} \sqrt{\omega_{t1} \omega_{t2}}
\] (5.16)

From Eq. (5.16), the maximum operating frequency of an active inductor is the self-resonant frequency which is determined by the cut off frequency of the transconductors in the active inductor.

5.2.3 Transformation between series and parallel LC for Q enhancement
Considering transformation between series RL connection and parallel RL connection in RLC network, as shown in Fig. 5.5, the impedance of RL series branch equals to the impedance of RL parallel branch. Hence,

\[ \frac{j\omega L_p R_p}{R_p + j\omega L_p} = R_s + j\omega L_s \]  

Eq (5.17) can be written as

\[ R_s R_p - \omega^2 L_s R_p + j\omega L_p R_p + j\omega L_s R_p = j\omega L_p R_p \]  

(5.18)

Let the real part and imaginary part matched each other, we obtain

\[ R_s R_p - \omega^2 L_s R_p = 0 \]  

(5.19)

\[ L_p R_s + L_s R_p = L_p R_p \]  

(5.20)

Considering the Q factor in series LC branch,

\[ Q = \frac{\omega L_s}{R_s} \]  

(5.21)

Combining Eq. (5.19) and (5.20), we get
After understanding the operating principle of the active inductor, several featured parameters including working frequency range and quality factor to evaluate the performance of active inductor are presented in this section. The working frequency range and quality factor are discussed based on the theory and their enhancement techniques.

As discussed in section 5.2, the lossless gyrator-C active inductor operates as inductor in entire frequency band. And, the lossy gyrator-C active inductor is different, it operates as inductor only in certain range of frequency. In the following, the RLC model of active inductor is discussed to analyze AI working frequency range, and to achieve the range enlargement technique.

The total impedance \( Z_{total} \) looking into the input port of RLC parallel circuit (Fig. 5.4(b)) is given by,

\[
Z_{total} = R_p / \left( \frac{1}{Z_c} \right) / \left( (R_s + Z_L) \right)
\]

\[
= \frac{R_p(Z_L+R_s)Z_c}{R_p(Z_L+R_s)+Z_c(R_s+R_p)}
\]

\[
= \frac{R_p(sL+R_s)\frac{1}{sC_p}}{R_p(sL+R_s)+\frac{1}{sC_p}(R_s+R_p+sL)}
\]
\[
\frac{R_s}{C_p} L \frac{s^2 + s \left( \frac{1}{R_p C_p} + \frac{R_s}{L} \right) + \frac{R_p + R_s}{L R_p C_p}}{s^2 + s \left( \frac{1}{R_p C_p} + \frac{R_s}{L} \right) + \frac{R_p + R_s}{L R_p C_p}}
\]  

(5.24)

The pole resonant frequency of \( Z_{\text{total}} \) is

\[
f_p = \frac{1}{2\pi} \sqrt{\frac{R_p + R_s}{L R_p C_p}}
\]  

(5.25)

If \( R_p \gg R_s \), \( f_p \) is simplified as

\[
f_p \approx \sqrt{\frac{1}{L C_p}} = f_0
\]  

(5.26)

where \( f_0 \) is the self-resonant frequency of the active inductor. Meanwhile, the zero frequency for \( Z_{\text{total}} \) is

\[
f_z = \frac{R_s}{L} = \frac{1}{C_p R_{\text{on}}}
\]  

(5.27)

For a better understanding of the operating inductive frequency range, bode plots of \( Z_{\text{total}} \) is depicted in Fig. 5.6. It is observed that the gyrator-C is resistive when \( f < f_z \), inductive when \( f_z < f < f_0 \), and capacitive when \( f > f_0 \). Hence, the inductive frequency range upper bound is \( f_0 \) and lower bound is \( f_z \). From Eq. (5.14) and (5.27), the inductive range of gyrator-C is independent from the parallel resistor \( R_p \), but its lower bound is dependent of the series resistor \( R_s \). The upper bound frequency range of the active inductor is determined by the self-resonant frequency of the active inductor which is determined by cut-off frequency of the transconductors in the active inductor. Note that given an inductance value, minimizing the series resistance \( R_s \) or minimizing the parallel capacitor \( C_p \) can maximize the inductive frequency range.
5.3.1 Quality factor ($Q$)

In reality, real inductor unlike ideal inductor has internal resistance and its losses in RF applications. The quality factor $Q$ is a key factor in evaluating RF circuits. It is determined by the ratio of the net magnetic energy stored in the inductor to its ohmic loss in one oscillation cycle.

$$Q = 2\pi \times \frac{\text{Net magnetic energy stored}}{\text{Energy dissipated per oscillation cycle}}$$  \hspace{1cm} (5.28)

For a linear inductor, the complex power of active inductor can be written as

$$p(j\omega) = I(j\omega)V^*(j\omega) = Re(Z)|I(j\omega)|^2 + jIm(Z)|I(j\omega)|^2$$  \hspace{1cm} (5.29)
where \( \text{Re}(Z) \) and \( \text{Im}(Z) \) are the resistance and inductive reactance of the inductor, and \( V(j\omega) \) and \( I(j\omega) \) are the voltage across and the current through the inductor. The superscript * is the complex conjugation operator. The first term in Eq. (5.29) presents the net energy loss arising from the parasitic resistance of the inductor while the second term presents the magnetic energy stored in the inductor. Eq. (5.28) can be further expressed by

\[
Q = \frac{\text{Im}(Z)}{\text{Re}(Z)}
\]  

(5.30)

Note that \( Q \) of the linear inductor can be calculated from Eq. (5.3).

\[
L = \frac{C}{G_{m1} G_{m2}}
\]

The active inductor is almost linear when the voltages across it or the current through it is small. And, all transistors in AI operates in saturation. Eq. (5.24) can be rewritten as

\[
Z_{total} = \frac{R_p}{1 + \frac{R_p R_s}{R_s^2 + \omega^2 L^2}} + jR_p\omega c_p \left[ \frac{R_s^2 + \omega^2 L^2 - \omega L}{R_s^2 + \omega^2 L^2} \right]
\]  

(5.31)

Assume

\[
A = 1 + \frac{R_p R_s}{R_s^2 + \omega^2 L^2}
\]

\[
B = \frac{R_p \left( \omega c_p (R_s^2 + \omega^2 L^2) - \omega L \right)}{R_s^2 + \omega^2 L^2}
\]

Then, \( Z_{total} \) is simplified as

\[
Z_{total} = R_p \frac{1}{A + jB} = \frac{R_p}{A^2 + B^2} (A - jB)
\]  

(5.32)
According to Eq. (5.30),

\[
Q = \frac{-B}{A} = \frac{R_p \left[ \omega L - \omega C_p \left( R_s^2 + \omega^2 L^2 \right) \right]}{R_s^2 + \omega^2 L^2 + R_p R_s}
\]

\[
= \frac{R_p \left( \omega L - \omega C_p R_s^2 - \omega^3 L^2 C_p \right)}{R_s^2 + \omega^2 L^2 + R_p R_s}
\]

\[
= \frac{\omega L}{R_s} \frac{R_p}{R_p + R_s \left( 1 + \left( \frac{\omega L}{R_s} \right)^2 \right)} \left( 1 - \omega^2 C_p - \frac{C_p R_s^2}{L} \right) \quad (5.33)
\]

To find the working frequency range of active inductor, Eq. (5.33) can be expressed as the product of three terms \( Q_1, Q_2 \) and \( Q_3 \),

\[
Q = Q_1 Q_2 Q_3 \quad (5.34)
\]

where

\[
Q_1 = \frac{\omega L}{R_s} \quad (5.35)
\]

\[
Q_2 = \frac{R_p}{R_p + R_s \left( 1 + \left( \frac{\omega L}{R_s} \right)^2 \right)} \quad (5.36)
\]

\[
Q_3 = 1 - \omega^2 C_p - \frac{C_p R_s^2}{L} \quad (5.37)
\]

\( Q_1 \) is the Q factor of the active inductor at lower frequency, \( Q_2 \) is the Q factor considering effect of the finite output impedance, and \( Q_3 \) is the Q factor of the active inductor at high frequency and it approaches to zero when the working frequency approaches to the cut off frequency of the transconductors in the gyrator-C active inductor. Fig. 5.7 depicts the relationship between Q factors and working frequency of
the active inductor. It is observed that $Q_1$ dominates the total Q factor. $Q_2$ and $Q_3$ are negligible at low frequency range and become effective at high frequency range.

Fig. 5.7 The relationship between Q factor and working frequency of active inductor [31]

From Eq. (5.35),

$$Q_1 = \frac{\omega L}{R_s}$$

the series resistance $R_s$ should be made as small as possible in order to achieve high Q factor of the active inductor. To minimize $R_s$, based on Eq. (5.8),

$$R_s = \frac{1}{G_{m1} G_{m2} R_{o1}}$$

we can increases $G_{m1}$ and $G_{m2}$ or increase the output impedance $R_{o1}$. Other than this approach, we can cancel $R_s$ by connecting a shunt negative resistor.
Based on transformation between the series RL connection and the parallel RL connection in RLC network as discussed in section 5.2.3, let us analyze a Q enhancement technique using a shunt negative resistor, as sketched in Fig. 5.8. The relationship of R and L between the LC series branch and the LC parallel branch can be rewritten as follows,

\[ R_p = R_s (1 + Q^2) \]  \hspace{1cm} (5.38)

\[ L_p = L_s (1 + 1/Q^2) \]  \hspace{1cm} (5.39)

The total parasitic parallel resistance of the active inductor in Fig. 5.8(b) is,

\[ R_{\text{parasitic-total}} = \frac{R_p R_p'}{R_p + R_p'} \]  \hspace{1cm} (5.40)

And,

\[ R_{\text{total}} = \frac{R_{\text{parasitic-total}} R_{cp}}{R_{cp} + R_{\text{parasitic-total}}} \]  \hspace{1cm} (5.41)

It is observed that the effect of the both \( R_p \) and \( R_s \) can be removed if connect a negative resistor \( R_{cp} = -R_{\text{parasitic-total}} \) in parallel with \( C_p \), since the total resistance for RLC parallel circuit would be infinite. However, due to the variation of the resistor, it is difficult to make the value of negative resistor exactly equal to the total parasitic resistance. Hence, it is desirable to make a tunable negative resistor to approach an ideal cancellation. After compensation, the Q factor of active inductor can be expressed as

\[ Q|_{\omega=\omega_0} = \frac{R_p}{R_p'} / \frac{R_{cp}}{\sqrt{\frac{C_p C_{cp}}{\mu'}}} \]  \hspace{1cm} (5.42)
Note that $C_{cp}$ is the input capacitance of the negative resistor. In addition, $R_s$ and $R_p$ are frequency sensitive, which requires an appropriate negative resistor design to obtain an ideal resistive cancellation during the inductive frequency range of the active inductor. In reality, an ideal cancellation is difficult to obtain although in theory the negative resistor compensation technique can enhance the $Q$ factor of the spiral inductors. Only the major parasitic series resistance induced by the skin effect of spiral inductors is canceled out by the negative resistor.

![Diagram](image)

Fig. 5.8 Q enhancement with a negative resistor

5.4 CMOS Active inductor design implementation

5.4.1 Basic gyrator-C active inductor

Section 5.3 has discussed the basic operation of gyrator-C active inductor. In this section, the implementation of basic gyrator-C active inductor in CMOS technology will be presented. Fig. 5.9 shows the simplified schematic of the two basic gyrator-C active inductors. In Fig. 5.9(a), the active inductor built based on two transconductors: 1) positive transconductance (common-gate configured) and 2) negative transconductance
(common-source configured). In Fig. 5.9(b), the active inductor built based on two transconductors: 1) positive transconductance (common-drain configured) and 2) negative transconductance (common-source configured). A main difference between this two configurations is that the transistors of active inductor in Fig. 5.9(b) are all built by NMOS. In our design, we use the active inductor in Fig. 5.9(b) in high frequency applications. Note that all the transistors in these configurations operate in saturation.

Considering the lossy gyrator-C active inductor model presented in section 5.2.2, let

\[ R_{o2} \approx \frac{1}{g_{m1}}, \quad C_2 = C_{gs1}, \quad g_{m1} = g_{m1}, \quad g_{m2} = g_{m2}, \quad \text{and} \quad C_1 = C_{gs2}, \]

we obtain the parameters of the equivalent RLC model for the single ended gyrator-C active inductor.

\[ R_p = R_{o2} = \frac{1}{g_{m1}} \quad (5.43) \]
\[ C_p = C_2 = C_{gs1} \] (5.44)

\[ R_s = \frac{1}{R_{o1}g_{m1}g_{m2}} = \frac{1}{R_{o2}g_{m1}g_{m2}} \] (5.45)

\[ L = \frac{c_1}{g_{m1}g_{m2}} = \frac{c_{gs2}}{g_{m1}g_{m2}} \] (5.46)

where \( R_{o1} \) and \( R_{o2} \) are the output impedance of node 1 and 2, and \( g_{m1} \) and \( g_{m2} \) are the output transconductance of node 1 and 2. From Eq. (5.43) to (5.46), it is found that when the parasitic parallel resistance \( R_p \) is small, the Q factor of active inductor is small. Furthermore, if parasitic series resistance is large, the Q factor becomes smaller. Since \( R_p \) is small, the effect of parasitic series resistance is negligible in evaluating the Q factor of this basic active inductor. Reviewing Eq. (5.33),

\[ Q = \frac{\omega L}{R_s} \frac{R_p}{R_p + R_s \left( 1 + \left( \frac{\omega L}{R_s} \right)^2 \right)} \left( 1 - \omega^2 C_p - \frac{C_p R_p}{L} \right) \]

if \( R_s \) is small, the Q factor is mainly determined by \( R_p \) and given as,

\[ Q = \frac{R_p \omega L - R_p \omega^3 L^2 C_p}{\omega^2 L^2} \] (5.47)

Since \( \omega_0 = \frac{1}{LC_p} \),

\[ Q = \frac{R_p}{\omega L} \left\{ 1 - \left( \frac{\omega}{\omega_0} \right)^2 \right\} \] (5.48)

For the frequency below \( \omega_0 \), the Q factor is further simplified to,

\[ Q = \frac{R_p}{\omega L} = \frac{\omega r_2}{\omega} \] (5.49)
The self-resonant frequency of the active inductor can be obtained as,

\[
\omega_0 \approx \frac{1}{\sqrt{\mathcal{L}_c}} = \sqrt{\omega_{t1}\omega_{t2}}
\]  

(5.50)

where \(\omega_{t1} = \frac{g_{m1}}{C_{gs1}}\) and \(\omega_{t2} = \frac{g_{m2}}{C_{gs2}}\) are the cut off frequency of the transconductors. After combining Eq. (5.49) and (5.50), the Q factor of this active inductor at the self-resonant frequency is given by,

\[
Q|_{\omega=\omega_0} = \frac{\omega_{t2}}{\sqrt{\omega_{t1}}}
\]

(5.51)

The lower bound of the frequency range for the active inductor is obtained at the frequency when the impedance \(Z\) of the active inductor RLC model closes to zero. For this, Eq. (5.27) is rewritten as,

\[
\omega_z = \frac{1}{R_{o1}C_{gs2}}
\]

(5.52)

The working frequency range of the AI operating as an inductor is \([\omega_z, \omega_0]\), which was explained in section 5.3.1. In order to achieve a wider inductive range, \(\omega_z\) is minimized while \(\omega_0\) is maximized. In accordance with Eq. (5.49) and (5.52), we can either increase \(C_{gs2}\) or increase \(R_{o1}\) to obtain a lower \(\omega_z\). However, increasing \(C_{gs2}\) will result in a lower \(\omega_0\). Therefore, increasing \(R_{o1}\) to extend the inductive frequency range is preferred. Meanwhile, we also note that MOSFET has a small output resistance \((R_p = 1/g_{m1})\), which creates adverse impact for Q factor of the active inductor and can not be negligible. To remove the adverse impact of \(R_p\), one can connect \(R_p\) with a negative shunt resistor \((R_p' = -R_p)\) in parallel. Implementation of the negative shunt resistor in CMOS will be discussed in the following section.
From Eq. (5.45),

\[
R_s = \frac{1}{R_{o1}G_{m1}G_{m2}} = \frac{1}{R_{o1}g_{m1}g_{m2}}
\]

The adverse impact of \( R_s \) to the Q factor of active inductor is not negligible. Three approaches to minimize this impact: 1) using a high output impedance cascade architecture but it has a reduced signal swing, 2) using negative shunt resistor after transforming the series RL branch to the parallel RL branch in the RLC equivalent circuit of the active inductor. The transformed series resistor and inductor are \( R_p' = (1 + Q^2)R_s \) and \( L' = \left(1 + \frac{1}{Q^2}\right) L \), respectively. Then, the total parasitic parallel resistance of the active inductor is changed to \( R_{parasitic-total} = R_p'//R_p \). Hence, if connecting a negative resistor with resistance of \( -R_{parasitic-total} \) in parallel with the total equivalent parasitic resistor, an ideal resistive cancellation and high Q factor can be achieved.

### 5.4.2 CMOS implementation of negative shunt resistor

On the contrary to normal resistor, negative resistance (NR) is a behavior of circuit and device in which current and voltage are inversely proportional to each other. For power measurement, negative resistor produces power while positive resistor consumes power. Negative resistance is a special feature existing in nonlinear electronic devices such as Gunn diodes, tunnel diodes and gas discharge tubes.

In reality, negative resistor’s negative resistance occurs in certain range of current or voltage, as shown in Fig. 5.10. In general, two types of resistance are defined in these nonlinear devices: static and differential. Static resistance is the ratio of voltage to current while differential resistance is the ratio of a voltage change to the induced current change.
(also called negative differential resistance). The negative differential resistance has been used in amplifiers such as the transistors and operational amplifiers with positive feedback in application of active filters and oscillators.

![Characteristic of negative resistor](image)

**Fig. 5.10 Characteristic of negative resistor**

For simplicity, the negative differential resistance is called negative resistance in the following discussion. Fig. 5.11 shows the single ended negative resistor with positive feedback. It is observed: 1) this negative resistor can be implemented in CMOS technology and 2) a voltage increase in the gate of $T_1$ will lead to a voltage increase in the source of $T_2$, and 3) a voltage increase in the source of $T_2$ will lead to a voltage increase the drain of $T_2$. Hence, it creates a positive feedback using this architecture. Note that the transconductor based negative resistor should be synthesized as simple as possible in order to obtain a constant negative resistance within a maximal frequency span.
5.4.3 Self-resonant frequency boosted architecture of gyrator-C active inductor

In section 5.4.1, the positive transconductor in the forward path is implemented with NMOS while the negative transconductor in the feedback path is implemented with PMOS. This section presents an improved architecture for the gyrator-C active inductor. As shown in Fig. 5.12, all the transistors in the positive and negative transconductors are implemented with NMOS. The operating speed of NMOS implementation is faster than that of PMOS implementation.

To analyze operating principle of the active inductor quantitatively, the small signal model is depicted in Fig. 5.13. For a better analysis, several parameters are simplified, e.g., $c_1 = c_{gs1}$ in $T_1$, $c_2 = c_{gs2}$ of $T_2$, $g_1$ and $g_2$ are the reciprocal of the drain to source resistance dues to channel length modulation in $T_1$ and $T_2$; $g_{m1}$ and $g_{m2}$ are the transconductance of $T_1$ and $T_2$ respectively; $R_{f1}$ is the impedance of the current source $J_1$.
Fig. 5.12 NMOS implementation gyrator-C active inductor

Fig. 5.13 Small signal model of the NMOS implementation gyrator-C active inductor

\[ I_{in} \] is the input current seen from node 2; \( Y_{in} \) is the input admittance looking into node 2; \( I_a, I_b, I_c \) are the branches current, \( v_2 \) and \( v_1 \) are the voltage of node 1 and 2 respectively; \( v_2 \) also denotes \( v_{in} \). From Fig. 5.13,

\[ I_a = g_{m2}v_1 + v_2g_2 \]  \hspace{1cm} (5.53)

\[ I_b = I_a + (v_2-v_1)g_1 \]  \hspace{1cm} (5.54)
\[ I_c = I_b + g_{m1}v_2 \quad (5.55) \]

\[ I_{in} = I_c + v_2sc_1 \quad (5.56) \]

Note that \( J_1 \) is a current source and its resistance \( R_{j1} \) is very large. Hence,

\[ v_1 = (g_{m1}v_2 + (v_2 - v_1)g_1) \frac{1}{sc_2} \quad (5.57) \]

Combining Eqs. (5.53) to (5.56),

\[ v_1 = \frac{v_2(g_1+g_{m1})}{g_1+sc_2} \quad (5.58) \]

\[ I_{in} = v_2sc_1 + v_2g_2 + v_2g_1 + g_{m2}v_2 \frac{g_2(g_1+g_{m1})}{g_1+sc_2} + g_{m2} \frac{v_2(g_1+g_{m1})}{g_1+sc_2} \]

\[ = v_2sc_1 + v_2g_2 + \frac{v_2(g_1+g_{m1})}{g_1+sc_2} (g_{m2} + sc_2) \]

\[ = v_2sc_1 + v_2g_2 + \frac{v_2(g_1+g_{m1})}{g_1+sc_2} (g_{m2} - g_1 + g_1 + sc_2) \]

\[ = v_2sc_1 + v_2g_2 + v_2(g_1 + g_{m1}) \left( 1 + \frac{g_{m2}-g_1}{g_1+sc_2} \right) \]

\[ = v_2sc_1 + v_2(g_1 + g_2 + g_{m1}) + v_2(g_1 + g_{m1}) \frac{g_{m2}-g_1}{g_1+sc_2} \quad (5.59) \]

Since \( g_{m1}r_{ds1} \gg 1 \) and \( g_{m2}r_{ds2} \gg 1 \), then \( g_{m1} \gg g_1 \) and \( g_{m2} \gg g_2 \). Meanwhile, we also note that \( g_1 \) ad \( g_2 \) are comparable, then \( g_{m1} \gg g_2 \) and \( g_{m2} \gg g_1 \). Hence, Eq. (5.59) is simplified as

\[ I_{in} = v_2sc_1 + v_2g_{m1} + v_2g_{m1} \frac{g_{m2}}{g_1+sc_2} \]

\[ = v_2sc_1 + v_2g_{m1} + v_2 \frac{1}{g_{m1}g_{m2}} \frac{g_{m2}}{g_{m1}g_{m2} + s} \]
Finally, the admittance $Y_{in}$ is obtained,

$$Y_{in} = \frac{i_{in}}{v_{in}} = \frac{i_{in}}{v_2}$$

$$= s c_1 + g_2 + \frac{1}{g_{m1} g_{m2} + s g_{m1} g_{m2}} \cdot v_2$$

(5.61)

Comparing the admittance looking into the node 2 in Fig. 5.13 and Fig. 5.14, the parameters of small signal model of active inductor and equivalent parallel RLC model can be written as

$$R_p = \frac{1}{g_{m1}}$$

(5.62)

$$C_p = C_1 = C_{gs1}$$

(5.63)

$$R_s = \frac{g_1}{g_{m1} g_{m2}}$$

(5.64)

$$L = \frac{c_2}{g_{m1} g_{m2}} = \frac{C_{gs2}}{g_{m1} g_{m2}}$$

(5.65)

Fig. 5.14 Equivalent parallel RLC model with series resistance $R_s$
The effect of series resistance $R_s$ is negligible so the Q factor of the operating frequency range is improved and calculated with consideration of parallel resistance $R_p$. It is given by

$$Q \approx \frac{R_p}{\omega L} = \frac{\omega r}{\omega} = \frac{f_{t2}}{f}$$

(5.66)

The self-resonant frequency $f_0$ is expressed as

$$f_0 = \sqrt{f_{t1}f_{t2}}$$

(5.67)

Hence, we get the Q factor at the self-resonant frequency,

$$Q|_{f=f_0} = \frac{f_{t2}}{f_0} = \frac{f_{t2}}{\sqrt{f_{t1}f_{t2}}}$$

(5.68)

From Eq. (5.67), increasing self-resonant frequency can be realized by increasing both of cutoff frequency $f_{t1}$ and $f_{t2}$. Increasing the cutoff frequency $f_{t1}$ will lead to a lower Q factor at the frequency of $f_0$. Hence, in order to achieve high self-resonant frequency and the corresponding high Q factor, it is highly desirable to boost the cutoff frequency $f_{t2}$.

The Q enhancement gyrator-C active inductor can make this happen by injecting an additional current to the drain of $T_2$.

Considering Eq. (5.69) and (5.70), the cut off frequency $f_{t1}$ and $f_{t2}$ of the transconductors can be boosted by increasing the dc current of the transistors. As shown in Fig. 5.12, an additional current $J_2$ is attached to the drain of $T_2$, in this way, the transconductance $g_{m2}$ of $T_2$ is increased while the transconductance $g_{m1}$ of $T_1$ is unchanged once bias voltage $V_b$ is fixed. Hence, the cutoff frequency $f_{t2}$ is boosted without affecting $f_{t1}$. Finally, both of the self-resonant frequency and its corresponding Q
factor are boosted. In practical design, the current $f_2$ is provided by a current source realized by current mirror current source. This improved architecture of active inductor is also called current reuse gyrator-C active inductor.

$$f_{t1} = \frac{g_{m1}}{2\pi C_1}; f_{t2} = \frac{g_{m2}}{2\pi C_2}$$  \hspace{1cm} (5.69)

$$g_{m1} = \sqrt{2I_{ds1}\beta}; g_{m2} = \sqrt{2I_{ds2}\beta}$$  \hspace{1cm} (5.70)

5.4.4 The proposed gyrator-C based active inductor

The architecture discussed in the section 5.4.3 boosts the self-resonant frequency and the Q factor at the self-resonant frequency. However, its equivalent inductance is low and often cannot meet applications requiring high inductance. In this section a architecture of gyrator-C based active inductor for high inductance, high Q factor and

Fig. 5.15 Proposed architecture of gyrator-C based active inductor (a) schematic (b) NR schematic, (c) AI symbol
Fig. 5.16 Proposed gyrator-C based active inductor (a) Small signal model; (b) RLC equivalent model; (c) AI symbol

high self-resonant frequency is proposed. The gyrator-C based active inductor depicted in Fig. 5.15 uses Q enhancement technique by inserting negative resistive block, inductance boosted technique by adding feedback resistance, and self-resonant frequency boosted technique by inserting additional dc current source.

To analyze operating principle of the proposed active inductor quantitatively, the small signal model is depicted in Fig. 5.16. For a better analysis, several parameters are simplified, e.g., $c_1 = c_{gs1}$ of $T_1$, $c_2 = c_{gs2}$ of $T_2$, $c_3 = c_{gs3}$ of $T_3$, $g_1$, $g_2$ and $g_3$ are the reciprocal of the drain to source resistance dues to channel length modulation in $T_1$, $T_2$ and $T_3$; $g_{m1}$, $g_{m2}$ and $g_{m2}$ are the transconductance of $T_1$, $T_2$ and $T_3$; $g_4$ and $g_6$ are the conductance of the current source $T_4$ and $T_6$; $I_{in}$ is the input current seen from node 2; $Y_{in}$ is the input admittance looking into node 2; $I_a$, $I_b$, $I_c$ are the branches current; $v_1$ to $v_4$ are the voltage of node 1 to 4 respectively; $v_2$ also denotes $v_{in}$. From Fig. 5.16,
\[ I_a = g_6 v_4 + g_{m6} v_3 \] (5.72)
\[ I_b = (v_2 - v_4) g_4 - g_{m4} v_4 + (v_2 - v_1) g_3 \] (5.73)
\[ I_c = I_b + g_{m3} v_2 \] (5.74)
\[ I_{in} = I_c + v_2 s_c_3 \] (5.75)
\[ (v_2 - v_4) g_4 = g_{m4} v_4 + s c_4 v_4 + (g_6 + g_7) v_4 + g_{m6} v_3 \] (5.76)

Note that \( T_2 \) and \( T_6 \) serve as current source and both conductance \( g_2 \) and \( g_6 \) close to zero. Hence, the current goes through it is negligible.

\[ v_1 = ((v_2 - v_1) g_3 + g_{m3} v_2 - g_2 v_1) \left( \frac{1}{g_x} + \frac{1}{s c_6} \right) \] (5.77)

From Eq. (5.75) and (5.76), we get,

\[ v_1 = \frac{(s c_6 + g_x)(g_x + g_{m3})}{s c_6 g_x + s c_6 g_3 + g_3 g_x + g_2 (g_x + s c_6)} v_2 \] (5.78)
\[ v_3 = \frac{1}{s c_6} - \frac{1}{g_x} v_1 = \frac{g_x (g_3 + g_{m3})}{s c_6 g_x + s c_3 g_3 + g_3 g_x + g_2 (g_x + s c_6)} v_2 \] (5.79)
\[ v_4 = \frac{g_x v_1 - g_{m6} v_3}{g_4 + g_6 + g_7 + g_{m4} + s c_4} \] (5.80)

Finally, \( I_{in} \) can be rewritten as,

\[ I_{in} = s c_3 v_2 + g_{m3} v_2 + (v_2 - v_4) g_4 - g_{m4} v_4 + (v_2 - v_1) g_3 \]
\[ = s c_3 v_2 + (g_{m3} + g_4 + g_3) v_2 - (g_{m4} + g_4) v_4 - g_3 v_1 \] (5.81)

Hence, the admittance looking into the node 2 is given by

\[ Y_{in} = s c_3 + (g_{m3} + g_4 + g_3) v_2 - (g_{m4} + g_4) v_4 - g_3 v_1 \] (5.82)
Let \( Y = -(g_m^4 + g_4) v_4 - g_3 v_1 \), and \( Y = 1/Z \), then

\[
Y = \frac{\left(g_{m4} + g_4\right)(g_{m6} g_x (g_3 + g_m^3) - g_4 (s C_6 + g_x) (g_3 + g_m^3))}{(s C_6 g_x + s C_6 g_3 + g_3 g_x + g_2 (g_x + s C_6)) (g_4 + g_6 + g_7 + g_{m4} + s C_6)} \quad \frac{g_4 (s C_6 + g_x) (g_3 + g_m^3)}{s C_6 g_6 + s C_6 g_2 + g_3 g_x + g_2 (g_x + s C_6)}
\]

(5.83)

If the effect of channel length modulation is neglected, \( g_1 \) and \( g_2 \) approach to zero. Eq. (5.83) is then simplified to

\[
Y \approx \frac{g_x g_{m4} g_{m2} g_{m6}}{(s C_6 g_x + s C_6 g_2 + g_x g_2) (g_6 + g_7 + g_{m4} + s C_6)}
\]

(5.84)

Then the impedance \( Z \) is obtained,

\[
Z = \frac{(g_{m4} + g_6 + g_7) g_2 g_x + s^2 (C_4 C_2 (g_2 + g_x) + s (C_6 (g_6 + g_7 + g_{m4}) (g_2 + g_x) + g_2 g_x C_6))}{g_f g_{m1} g_{m2} g_{m3}}
\]

(5.85)

\[
= \frac{(g_{m4} + g_6 + g_7) g_2 g_x - \omega^2 (C_4 C_6 (g_2 + g_x) + j \omega (C_6 (g_6 + g_7 + g_{m4}) (g_2 + g_x) + g_2 g_x C_6))}{g_x g_{m4} g_{m3} g_{m6}}
\]

(5.86)

Let \( Z = r_s + j \omega L \). So,

\[
r_s = \frac{(g_{m4} + g_6 + g_7) g_2 g_x - \omega^2 (C_4 C_6 (g_2 + g_x))}{g_f g_{m1} g_{m2} g_{m3}}
\]

(5.87)

\[
L = \frac{(g_{m4} + g_6 + g_7) g_2 g_x - \omega^2 (C_4 C_6 (g_2 + g_x))}{g_x g_{m4} g_{m3} g_{m6}}
\]

(5.88)

Compare the admittance seen from the input terminal of the equivalent RLC network in Fig. 5.14. We get

\[
R_p = \frac{1}{g_{m3} + g_4 + g_3} \approx \frac{1}{g_{m3}}
\]

(5.89)

\[
C_p = C_4 = C_{gs4}
\]

(5.90)
Since

\[ g_{m6} = \beta (V_{gs6} - V_t) \]  

(5.91)

\[ V_{gs6} = V_{la} - V_{inDC} \]

(5.92)

Then,

\[ g_{m6} = \beta (V_{la} - V_{inDC} - V_t) \]

(5.93)

where \( g_{m6} \) is proportional to the \( V_{la} \). Combining Eq. (5.88) and (5.93), we obtain that the inductance \( L \) is inversely proportional to \( V_{la} \) and is expressed in Eq. (5.94) and verified by simulation, as shown in Fig. 5.17.

\[ L = f \left( \frac{1}{V_{la}} \right) \]

(5.94)

According to Eq. (5.82) and the equivalent RLC model in Figure 2(b);

\[ r_p = \frac{1}{(g_{ds6} + g_2)}; \quad C_p = C_{gs6} \]

(5.95)

The Q factor of the equivalent parallel RLC model in Fig. 16(b) is derived by

\[ Q = \frac{\omega L}{r_s} \frac{r_p}{r_p + \frac{r_s}{r_s + \omega^2 L}} \left( 1 - \frac{r_s^2 C_p}{L} - \omega^2 L C_p \right) \]

(5.96)

As shown in Eq. (5.88), the inductance of \( L \) is determined by \( g_{m2}, g_{m6}, g_{m7}, g_{ds7}, g_{ds3}, g_{ds6}, C_{gs2}, C_{gs4} \). The \( g_{ds6} \) and \( g_{ds7} \) introduced from the current mirror of \( T_7 \) and \( T_8 \) are added to \( g_{m4} \) and increase the total inductance. Meanwhile, the inductance is further increased after applying the feedback resistor \( R_x \).

From Eq. (5.96), the Q factor is proportional to \( r_p \), and \( r_p \) is inversely proportional to \( g_{ds6} + g_2 \). Thus, the Q factor is enhanced after the negative value of \( g_x \) is added to \( g_{ds6} \). In this AI circuit, all the transistors are biased in saturation region, and with the
adjustments of input bias voltages and transistors size, the Q factor and inductance of AI can be adjusted accordingly.

Fig. 5.17 AI Inductance vs signal frequency for different $V_{la}$

5.5 Performance analysis

5.5.1 Performance of active inductor without negative resistive (NR) block

The proposed AI is designed in CMOS 180 nm technology. As shown in Fig. 3, the relation of inductance without using NR verse signal frequency for different bias voltage $V_{b1}$ is presented. The equivalent inductance of AI without NR is tunable between 25 nH to 52 nH while $V_{b1}$ is changed from 1.628 V to 1.640 V. It is shown that the tuning frequency can be up to 3.1 GHz with respect to the change of $V_{b1}$. Fig. 4 depicts the frequency response of the proposed active inductor without NR. The inductive bandwidth
is 3.1 GHz, the peak inductance is 47 nH at the frequency ranges from 0 to 1.1 GHz, the maximum Q factor is 1.82 at 0.95 GHz, and the bandwidth of Q factor > 1.5 is 20 MHz.

![Graph](image)

Fig. 5.18 Q factor and inductance of AI without NR

5.5.2 Performance of Active inductor using negative resistive (NR) block

To better evaluate the contribution of negative resistive block, the performance of AI using NR is discussed. As shown in Fig. 5.19, the performance is much improved after adding negative resistive block compared with the performance with using negative resistive block, the peak Q factor of AI is 553k at 1.27 GHz for the bias voltage $V_{ib} = 1.629$. The inductive range is 1.89 GHz and peak inductance is 451 nH.

Fig. 5.20 shows the inductive tuning range with different bias voltage, where the bias voltage $V_{ib}$ is varied from 1.628 to 1.637 V, the inductance can be tuned from 52 to 1436 nH and reaches at its peak value at 1.52 GHz, and the maximum inductive frequency range reaches up to 2.16 GHz.
Fig. 5.19 Q factor and inductance of AI using NR block

Fig. 5.20 Inductance tuning range for different bias voltage $V_{la}$
Table 5.1 summarizes AI performance and comparison with [32, 33, 34]. All have wide inductive frequency range, 2.8 GHz [31], 3.52 GHz [32], 2.5 GHz [33], and 2.16 GHz [this work]. The proposed AI achieves the highest peak Q factor, 553k at 1.27 GHz and the highest inductance tuning range, from 52 to 1462 nH, and consumes the low power of 7.59 mW.

Table 5.1 AI performance summary and comparison

<table>
<thead>
<tr>
<th></th>
<th>[32]</th>
<th>[33]</th>
<th>[34]</th>
<th>This work</th>
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<td>2.16</td>
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<td>0.1-15 @</td>
<td>52-1462 @</td>
</tr>
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<td>(3GHz)</td>
<td>(1.4GHz)</td>
<td>(1.52GHz)</td>
</tr>
<tr>
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<td>16</td>
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<td>7.59</td>
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6 CMOS ACTIVE INDUCTOR BASED TUNABLE BAND PASS FILTER

6.1 Introduction

In this chapter, a wide tuning frequency BPF with high stopband rejection is first discussed and the design approach for controllable pass band and high pass band gain is presented, as also shown in my previous work [28-29]. A controllable calibration in the BPF to compensate process variation is proposed. Primitive measurement and performance analysis of band width, gain, noise figure, and power are further discussed.

6.2 Active drain inductor band pass filter

6.2.1 Design architecture

![Active drain inductor band pass filter](image)

Fig. 6.1 Active drain inductor band pass filter.
The proposed active inductor based band pass filter is shown in Fig. 6.1 where the differential cascade stage is divided into stages. In stage I, the input signals, \(V_{INP}\) and \(V_{INN}\), are transformed to two intermediate currents, \(I_P\) and \(I_N\). In stage II, \(I_P\) and \(I_N\) are transformed to the output signals, \(V_{OPP}\) and \(V_{OPN}\). The BPF is a type of double-notch filter [8] built by two filters in LC-series-parallel resonant connection. The module of active inductor (AI) (Fig. 5.15) and a voltage regulator (VR) are used in the stage II of BPF, and their physical connections are given as an example (Fig. 6.1). CMOS AI is to increase the frequency tuning range, reduce inductor loss and chip area while VR is to keep DC output of \(V_{opp}\) stable for DC bias voltage to the AI.

The input LC impedance for parallel series resonant combination in stage I and in stage II is expressed as \(Z_{N1}\), \(Z_{N2}\) respectively. The input impedance \(Z_{N1}\) is expressed in Eq. (6.1).

\[
Z_{N1} = \frac{1+s^2L_{N1}(C_{N1}+C_{P1})}{SC_{N1}(1+s^2L_{N1}C_{P1})}
\]  

(6.1)
Considering the parallel series LC network, its parallel resonant frequency $f_{p1}$ is a little bit higher than the zero frequency $f_{Z1}$,

$$f_{p1} = 0.5\pi^{-1}(L_{N1}C_{P1})^{-0.5} \quad (6.2)$$

$$f_{Z1} = 0.5\pi^{-1}(L_{N1}(C_{N1} + C_{P1}))^{-0.5} \quad (6.3)$$

For a better explanation, Eq. (2.34.) is rewritten as follows.

$$I_{op} = G_{m2}V_{in} = \frac{g_mV_{in}}{1 + g_mZ_{N1}} \quad (6.4)$$

The same LC parallel series combination with different impedance $L_{N2}$, $C_{N2}$, $C_{P2}$ is applied to the transimpedance stage. Hence, the input impedance of the second LC stage is given by

$$Z_{N2} = \frac{1 + s^2L_{N2}(C_{N2} + C_{P2})}{s(C_{N2} + s^2L_{N2}C_{P2})} \quad (6.5)$$

The two resonant frequencies are expressed by

$$f_{p2} = 0.5\pi^{-1}(L_{N2}C_{P2})^{-0.5} \quad (6.6)$$

$$f_{Z2} = 0.5\pi^{-1}(L_{N2}(C_{N2} + C_{P2}))^{-0.5} \quad (6.7)$$

The differential output voltage of the transimpedance filter stage is then expressed by

$$v_{op} = sL_D \frac{g_mZ_{N2}}{1 + g_mZ_{N2}}I_{op} \quad (6.8)$$

where $I_{op}$ equals to $g_mV_{in\text{n}}$. Similarly, the current $I_p$ can be expressed by replacing $v_{in\text{n}}$ with $v_{INP}$. The differential output current $I_{op}$ ($= I_p - I_N$) of the transconductance stage is simply obtained after replacing $v_{INP}$ with $v_{in}$ ($= v_{inp} - v_{in\text{n}}$). When $f = f_{Z1}$ then
\( Z_{N1} \approx 0 \). And, when \( f = f_{P1} \) then \( Z_{N1} \approx \infty \). Therefore, the output current \( I_{op} = I_p - I_N \) in Eq. (6.4) can be expressed as

\[
I_{op} \approx \begin{cases} 
  g_m v_{IN} & \text{when } f = f_{Z1} \\
  0 & \text{when } f = f_{P1}
\end{cases}
\]  

Similarly, \( Z_{N2} \approx 0 \) when \( f = f_{Z2} \). And, \( Z_{N2} \approx \infty \) when \( f = f_{P2} \). Hence the output voltage in Eq. (6.8) is given by

\[
v_{out} \approx \begin{cases} 
  0 & \text{when } f = f_{Z2} \\
  sL_D I_{op} & \text{when } f = f_{P2}
\end{cases}
\]  

It is observed from the Eqs. (6.1) and (6.5) that the transmission zero happens at \( f_{P1} \) in transconductance stage and happens at \( f_{Z2} \) in transimpedance stage. Meanwhile, the peak value happens at \( f_{Z1} \) in transconductance stage and happens at \( f_{P2} \) in transimpedance stage. Correspondingly, the peak conductance \( g_{\text{max}} \) and impedance \( Z_{\text{max}} \) are obtained at \( f_{Z1} \) and \( f_{P2} \). Finally, the overall transfer function of the BPF is obtained from Eq. (6.4) and (6.8).

\[
v_{out} = v_{IN} \frac{g_m^2 L_D Z_{N2}s}{(1+g_m Z_{N1})(1+g_m Z_{N2})}
\]  

The peak output can be expressed by Eq. (6.12) when \( f = f_{Z1} \) and \( f_{Z1} \approx f_{P2} \).

\[
v_{out} \approx \begin{cases} 
  0 & \text{when } f = f_{P1} \text{ or } f_{Z2} \\
  g_{\text{max}} Z_{\text{max}} v_{IN} & \text{when } f = f_{Z1} \approx f_{P2}
\end{cases}
\]  

where \( g_{\text{max}} = l_{out}/v_{IN} \) and \( Z_{\text{max}} = v_{out}/l_{out} = sL_D \).

Since \( L_D \) is inversely proportional to external bias voltage \( V_{b1} \), as discussed in Eq. (5.94), then the gain of band pass filter is expressed by Eq. (6.13).
Consequently, the bandwidth of band pass filter can also be tuned by adjusting the bias voltage of $V_{ia}$.

The design approach to a wide tuning BPF is divided into three stages. The first design stage is to meet the center frequency $f_c$. The second design stage is to meet the BW. The last stage is considering process variations by conducting Monte Carlo analysis to evaluate the robustness of design. All simulations are conducted in 1.8 V 180 nm CMOS process. The simulation result of bandwidth, pass band gain, and noise figure is depicted in Fig. 6.2-6.6.

6.2.2 Simulation results and analysis

![Simulation results and analysis](image)

Fig. 6.3 A Performance of the tunable BPF without AI for 12.0 MHz≤BW≤12.7 Hz (1.0 GHz≤fC≤2.04 GHz, 52.8 dB≤gain≤59.9 dB)
Fig. 6.4 A Performance of the tunable BPF with AI for 4.7 Hz ≤ BW ≤ 83.2 MHz (0.39 GHz ≤ f_c ≤ 8.1 GHz, 8.14 dB ≤ gain ≤ 22.5 dB)

Table 6.1 BPF performance summary and comparison

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<th>[5]</th>
<th>[7]</th>
<th>[17]</th>
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<th>[12]</th>
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<th>[11]</th>
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<th>This work with AI</th>
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<td>-2</td>
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<td>-2</td>
<td>6-14</td>
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<td>45.2-65.1</td>
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<td>3-5</td>
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<td>9</td>
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<td>6</td>
<td>15</td>
<td>1.49-5.88</td>
<td>1.81-5.42</td>
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<td></td>
</tr>
<tr>
<td>Power [mW]</td>
<td>16.2</td>
<td>43.2</td>
<td>12</td>
<td>7.6</td>
<td>5</td>
<td>63</td>
<td>120</td>
<td>15</td>
<td>17</td>
<td>15</td>
<td>18.6</td>
</tr>
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<td>Freq tuning range</td>
<td>0.05-0.85</td>
<td>1.77-1.86</td>
<td>0.1-1.0</td>
<td>0.05-0.3</td>
<td>1.93-2.19</td>
<td>0.24-0.53</td>
<td>0.03-0.12</td>
<td>2.45-2.85</td>
<td>2.0-2.06</td>
<td>1.0-2.04</td>
<td>1.0-3.1</td>
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<td>(GHz)</td>
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</tbody>
</table>

Note: * The noise figure of BPF with AI and BPF without AI are measured for the center frequency is varied from 1 GHz to 2.04 GHz, and from 1 GHz to 3.09 GHz, respectively.
Fig. 6.3 depicts performance of the BPF without AI when the pass band is kept nearly constant (12 MHz) in a wide tuning center frequency range (1-2 GHz). Five basis center frequencies, 1.0 GHz, 1.18 GHz, 1.58 GHz, 1.78 GHz and 2.04 GHz, are selected and plotted in Figure for evaluation. Fig. 6.3 also shows high stopband rejection with minimum stopband 24.8 dB. The BW of these five center frequency of BPF is nearly constant (12 MHz), 12.11, 12.03, 12.42, 12.71 and 12.34 MHz. The pass band gain is between 52.76 and 59.87 dB. Fig. 6.4 depicts performance of the BPF with AI when the pass band gain is from 8.14 dB to 23.3 dB, and the pass band range is from 4.7 MHz to 83.2 MHz in a wide tuning center frequency range (0.39-8.13 GHz). Nine basis center frequencies, 0.389, 0.501, 0.562, 0.645, 0.794, 1.12, 3.09, 5.01, 8.13 GHz, are selected and plotted. Fig. 6.4 also shows that high stopband rejection with minimum stopband 28.9 dB, and the bandwidth of these nine center frequencies of BPF with AI is 4.72, 5.81, 6.97, 7.59, 9.33, 12.3, 22.3, 62.1, 83.2 MHz respectively. Meanwhile, it is observed that the pass band gain is kept almost constant of 22.6 dB, the pass band is from 4.7 MHz to 22.3 MHz when tuning center frequency range is from 0.39 GHz to 3.09 GHz. Fig. 6.5 still depicts the relationship between pass band gain and bandwidth of AI driven BPF when the center frequency ranges from 0.389 GHz to 8.13 GHz. It is shown that the proposed AI driven BPF provides a pass band gain between 7.56 to 28.2 dB and tunable pass band between 3.42 and 95.7 MHz while the center frequency is varied from 0.389 to 8.13 GHz.

Table 6.1 summarizes the performance of the proposed BPF without AI, and other band pass filters [5, 7, 9-12, 14, 16, 17]. The BPFs presented from other articles they have narrow tuning range, low pass band gain and high noise figure.
Fig. 6.5 Pass band gain vs. bandwidth (0.389 GHz ≤ f_c ≤ 8.13 GHz, and 3.42 Hz ≤ BW ≤ 95.7 MHz, 7.56 dB ≤ gain ≤ 28.2 dB)

Fig. 6.6 Noise figure measurement of AI driven BPF for different center frequencies ranging from 1.0 GHz to 3.09 GHz
However, the BPF without AI presented in this work achieves good performance with wide tuning range from 1.0 to 2.04 GHz, a low power of 15 mW, and a high pass band gain from 45.2 to 65.1 dB, and low noise figure less than 6 dB. Table 6.2 tabulates the performance comparison for the proposed BPF without AI and BPF with AI. The AI driven BPF provided in this article obtains a pass band gain from 21.1 to 28.2 dB with frequency ranging from 1.0 to 3.09 GHz, while the same BPF without using AI achieves a higher pass band gain (45.2 ~ 65.1 dB). The AI driven BPF achieves a higher tuning range (1.0 ~ 3.1 GHz) than the BPF without AI (1.0 ~ 2.04 GHz) while keeps a fairly good pass band gain (21.1 ~ 28.2 dB), and its tuning range is further extended up to 7.74 GHz (0.39 GHz to 8.13 GHz) when the minimum pass band gain is reduced to 8.14 dB, an average power of 18.6 mW, and a high stopband rejection of 28.9 dB. The AI driven BPF achieves a low noise figure from 1.81 to 5.42 dB while the center frequency is varied from 1.0 to 3.09 Hz, as shown in Fig. 6.6. Besides, Table 6.2 also shows that the AI driven BPF achieves low noise figure ranging from 1.31 to 6.82 dB when center frequency changing from 0.389 to 8.13 GHz, the maximum Q factor reaches up to 138.5.

Table 6.2 Performance comparison of BPF w/o AI and BPF with AI

<table>
<thead>
<tr>
<th>Parameters</th>
<th>This work w/o AI</th>
<th>This work with AI</th>
</tr>
</thead>
<tbody>
<tr>
<td>Freq tuning range (GHz)</td>
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<td>0.389-3.09</td>
</tr>
<tr>
<td>Passband gain (dB)</td>
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<td>22.6</td>
</tr>
<tr>
<td>BW (MHz)</td>
<td>5.5-51.2</td>
<td>4.7-22.3</td>
</tr>
<tr>
<td>NF (dB)</td>
<td>1.49-5.88</td>
<td>1.81-6.82</td>
</tr>
<tr>
<td>Power [mW]</td>
<td>15</td>
<td>18.6</td>
</tr>
<tr>
<td>Minimum Q factor</td>
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<td>82.7-138.5</td>
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6.2.3 Monte Carlo analysis for process variations

Table 6.3 Active drain inductor BPF $f_c, A_v$, and BW considering process variations

<table>
<thead>
<tr>
<th>$f_c$ after process variation</th>
<th>$A_v$ after process variation</th>
<th>BW after process variation</th>
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</thead>
<tbody>
<tr>
<td>Nominal $(GHz)$</td>
<td>$t_{ox}$, $L_{eff}$, $V_{th}$</td>
<td>$t_{ox}$, $L_{eff}$, $V_{th}$</td>
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<td>Nominal $(GHz)$</td>
<td>$[\text{min, max}]$</td>
<td>$[\text{min, max}]$</td>
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<tr>
<td>$[\text{min, max}]$</td>
<td>$(GHz)$</td>
<td>$(GHz)$</td>
</tr>
<tr>
<td>$t_{ox}$, $L_{eff}$, $V_{th}$</td>
<td>$[\text{min, max}]$</td>
<td>$[\text{min, max}]$</td>
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<tr>
<td>$0.389$</td>
<td>0.389</td>
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</tr>
<tr>
<td>$0.501$</td>
<td>0.501</td>
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</tr>
<tr>
<td>$0.562$</td>
<td>0.562</td>
<td>0.562</td>
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<tr>
<td>$0.655$</td>
<td>0.655</td>
<td>0.655</td>
</tr>
<tr>
<td>$0.794$</td>
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<tr>
<td>$1.12$</td>
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<td>$3.09$</td>
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<td>$8.13$</td>
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</tr>
<tr>
<td>AMD</td>
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Note: * AMD denotes “average maximum deviation” in comparison with its nominal value. Nominal means the results were obtained without process variations.

The performance of nine tunable BPF designs with the pass band ranging from 4.72 to 83.2 MHz is shown in Table 6.3. The bandwidth is 4.72 MHz, 5.81 MHz, 6.97 MHz, 7.59 MHz, 9.33 MHz, 12.3 MHz, 22.3 MHz, 62.1 MHz, and 83.2 MHz, respectively. The center frequency is varied from 0.389 to 8.13 GHz: 0.389 GHz, 0.501 GHz, 0.562 GHz, 0.655 GHz, 0.794 GHz, 1.12 GHz, 3.09 GHz, 5.01 GHz, and 8.13 GHz. The nominal pass band gain before considering process variations is between 8.14 and 23.8 dB. Considering process variations on $t_{ox}$, $L_{eff}$ and $V_{th}$ with a maximum 10% variation on its nominal value, the Monte Carlo simulation results show robustness of the BPF: zero deviation on center frequency. The average maximum deviation on pass band gain is 0.86 dB on an average nominal pass band gain of 20.01 dB. And, the average maximum deviation on bandwidth is 1.73 MHz on an average nominal bandwidth of 23.8 MHz.
6.3 Inductorless BPF

6.3.1 Design architecture

The proposed inductorless band pass filter is shown in Fig. 6.7, where the differential cascade stage is divided into stages. In stage I, the input signals, $V_{INP}$ and $V_{INN}$, are transformed to two intermediate currents, $I_P$ and $I_N$. In stage II, $I_P$ and $I_N$ are transformed to the output signals, $V_{OPP}$ and $V_{OPN}$. The BPF is a type of double-notch filter [8] built by
two filters in LC-series-parallel resonant connection. All the inductors use in the double notch band pass filter sketched in Fig. 2.4 are replaced by active inductors. VR, VR \(_1\) and VR \(_2\) are the voltage regulator for AI\(_D\), AI\(_{N1}\) and AI\(_{N3}\) respectively, to provide a constant DC biasing voltage for the AIs in the BPF. AIs are used to increase the frequency tuning range, reduce inductor loss and chip area. Fig. 6.8 shows the block diagram of active inductors where the connections of bias voltages are: 1) \(V_a\) and \(V_b\) are the bias voltages for the drain active inductor (AI\(_D\)) to adjust inductance value, 2) \(V_c\) and \(V_d\) are the bias voltages for the negative resistive block in the AI to adjust Q factor, 3) \(V_{a1}\) and \(V_{b1}\) are the bias voltage for the active inductor (AI\(_{N1}\)) to adjust the inductance value, 4) \(V_{c1}\) and \(V_{d1}\) are the bias voltages for the negative resistive block in the AI to adjust Q factor, 5) \(V_{a2}\) and \(V_{b2}\) are the bias voltage for the active inductor (AI\(_{N2}\)) to adjust the inductance, and 6) \(V_{c2}\) and \(V_{d2}\) are the bias voltages for the negative resistive block in the AI to adjust Q factor. Note that different values of \(V_a\), \(V_b\), \(V_c\) and \(V_d\) produce different inductance value and Q factor.

### 6.3.2 Simulation results and analysis

Fig. 6.9 depicts performance of the inductorless tunable BPF when sweeps bias voltage \(V_{la1}\) from 1.34 to 1.8 volts and keeps \(V_{dd}=1.8\) volts, \(V_{dd1}=1.8\) volts, \(V_{lb1}=1.05\) volts. Ten basis center frequencies, 0.503, 0.527, 0.552, 0.568, 0.589, 0.612, 0.650, 0.699, 0.783 and 0.907 GHz are selected and plotted. It shows that the bandwidth of these ten center frequencies of BPF with AI is 228, 234, 262, 283, 307, 344, 396, 478, 618 and 877 MHz respectively. The simulation demonstrates that the pass band gain is from 0.31 dB to 5.32 dB, and the pass band range is from 228 MHz to 877 MHz in a tuning center frequency.
span 0.404 GHz (0.503-0.907 GHz). Note that the pass band gain is much reduced; the pass band is much increased while the center frequency tuning range is reduced when compared with the passive double notch band pass filter.

![Graph showing performance of the inductorless tunable BPF](image)

**Fig. 6.9** Performance of the inductorless tunable BPF when sweeps bias voltage $V_{ta1}$ from 1.34 to 1.8 volts and keeps $V_{da}=1.8$ volts, $V_{dd1}=1.8$ volts, $V_{lb1}=1.05$ volts

Fig. 6.10 depicts performance of the inductorless tunable BPF when sweep bias voltage $V_{lb1}$ from 0.6 to 3.2 volts, and keeps $V_{da}=1.8$ volts, $V_{dd1}=1.8$ volts, $V_{ta1}=1.4$ volts. Ten basis center frequencies 0.567, 0.603, 0.671, 0.746, 0.808, 0.872, 0.912, 0.950, 1.000 and 1.032 GHz are selected and plotted. It shows that the bandwidth of these ten center frequencies of BPF with AI is 1293, 1081, 895, 812, 800, 841, 911, 1052, 1250 and 1511 MHz respectively. The simulation demonstrates that the pass band gain is from 3.32 dB to 5.48 dB, and the pass band range is from 800 MHz to 1511 MHz in a tuning center
frequency span 0.46 GHz (0.57-1.03 GHz). Note that the pass band gain is much reduced compared with the one achieved using active drain inductor based band pass filter, the pass band is much increased while the center frequency tuning range is reduced when compared with the passive double notch band pass filter.

![Graph showing performance of the inductorless tunable BPF](image)

**Fig. 6.10** Performance of the inductorless tunable BPF when sweep bias voltage $V_{lb1}$ from 0.77 to 1.4 volts and keeps $V_{dd}=1.8$ volts, $V_{dd1}=1.8$ volts, $V_{la1}=1.4$ volts

Fig. 6.11 depicts performance of the inductorless tunable BPF when sweeps bias voltage $V_{la1}$ from 1.6 to 3.3 volts, and keeps $V_{dd}=3.3$ volts, $V_{dd1}=1.8$ volts, $V_{lb1}=1.4$ volts. Nine basis center frequencies, 0.74, 0.84, 1.11, 1.31, 1.56, 1.86, 2.01, 2.03 and 2.07 GHz are selected and plotted. It shows that the bandwidth of these nine center frequencies of BPF with AI is 339, 445, 698, 883, 1002, 1009, 1040, 1030 and 989 MHz respectively. The simulation demonstrates that the pass band gain is from 2.17 dB to 17.04 dB, and the pass band range is from 339 MHz to 1040 MHz in a wide tuning center frequency span.
1.33 GHz (from 0.74 to 2.07 GHz). Note that the pass band gain is comparable with the one achieved using active drain inductor based band pass filter, the pass band is much increased while the center frequency tuning range is a little higher when compared with the passive double notch band pass filter.

Fig. 6.11 Performance of the inductorless tunable BPF when sweep bias voltage $V_{lat1}$ (1.6 to 3.3 volts) and keeps $V_{dd}$=3.3 volts, $V_{dd1}$=1.8 volts, $V_{lb1}$=1.4 volts

Fig. 6.12 depicts performance of the inductorless tunable BPF when sweeps bias voltage $V_{lb1}$ from 0.6 to 3.2 volts, and keeps $V_{dd}$=3.3 volts, $V_{dd1}$=1.8 volts, $V_{la1}$=1.8 volts. Nine basis center frequencies, 1.148, 1.788, 1.930, 2.180, 2.280, 2.320, 2.370, 2.391, and 2.410 GHz are selected and plotted. It shows that the bandwidth of these nine center frequencies of BPF with AI is 3056, 2847, 1404, 1050, 992, 931, 865, 802 and 721 MHz respectively. The simulation demonstrates that the pass band gain is from 4.83 dB to 19.7 dB, and the pass band range is from 721 MHz to 3056 MHz in a wide tuning
Fig. 6.12 Performance of the inductorless tunable BPF when sweep bias voltage $V_{lb1}$ from 0.6 to 3.2 volt and keeps $V_{dd}=3.3$ volts, $V_{d1}=1.8$ volts, $V_{la1}=1.8$ volts.

Fig. 6.13 Noise figure measurements of different frequencies sweeping $V_{la1}$ and $V_{lb1}$ ($V_{dd}=1.8$ volts, $V_{d1}=1.8$ volts).
Fig. 6.14 Noise figure measurements of different frequencies sweeping $V_{la1}$ and $V_{lb1}$

\[ (V_{dd}=3.3\ \text{volts}, V_{dd1}=1.8\ \text{volts}) \]

center frequency span 1.26 GHz (1.15 - 2.41 GHz). Note that the pass band gain is comparable with the one achieved using active drain inductor based band pass filter, the pass band is much increased while the center frequency tuning range is a little higher when compared with the passive double notch band pass filter.

Keeping power supply \((V_{dd}=1.8\ \text{volts}, V_{dd1}=1.8\ \text{volts})\), Fig. 6.13 shows the noise figure changing from 12.9 to 19.5 dB at different frequencies when sweeping $V_{la1}$ and the noise figure from 12.4 to 14.3 dB when sweeping $V_{lb1}$. Keeping power supply \((V_{dd}=3.3\ \text{volts}, V_{dd1}=1.8\ \text{volts})\). Fig. 6.14 shows the noise figure changing from 7.12 to 12.5 dB at different frequencies when sweeping $V_{la1}$ and the noise figure from 6.3 to 10.2 dB when
It is observed that the inductorless band pass filter generates lower noise figure by sweeping $V_{la1}$ than sweeping $V_{lb1}$, regardless of power supply change. Meanwhile, it is also demonstrated that the inductorless band pass filter generates fairly low noise figure (<10.2 dB when center frequency tuning range is from 1.15 to 2.41 GHz), which is better than that of using single power supply.

### 6.3.3 Monte Carlo analysis considering process variation

Table 6.4 Inductorless BPF $f_c$, $A_v$ and BW considering process variations

<table>
<thead>
<tr>
<th>$f_c$ after process variation</th>
<th>$A_v$ after process variation</th>
<th>BW after process variation</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{ox}$</td>
<td>$L_{eff}$</td>
<td>$V_{th}$</td>
</tr>
<tr>
<td>(GHz)</td>
<td>(GHz)</td>
<td>(GHz)</td>
</tr>
<tr>
<td>Nominal</td>
<td>[min, max]</td>
<td>[min, max]</td>
</tr>
<tr>
<td>0.74</td>
<td>0.71, 0.77</td>
<td>0.71, 0.77</td>
</tr>
<tr>
<td>1.11</td>
<td>1.06, 1.15</td>
<td>1.05, 1.16</td>
</tr>
<tr>
<td>1.31</td>
<td>1.24, 1.36</td>
<td>1.24, 1.37</td>
</tr>
<tr>
<td>1.56</td>
<td>1.50, 1.67</td>
<td>1.50, 1.64</td>
</tr>
<tr>
<td>1.68</td>
<td>1.71, 1.92</td>
<td>1.71, 1.89</td>
</tr>
<tr>
<td>2.01</td>
<td>1.97, 2.10</td>
<td>1.98, 2.13</td>
</tr>
<tr>
<td>2.03</td>
<td>1.97, 2.06</td>
<td>1.95, 2.09</td>
</tr>
<tr>
<td>2.07</td>
<td>2.02, 2.09</td>
<td>1.95, 2.13</td>
</tr>
<tr>
<td>AMD(%)</td>
<td>4.19</td>
<td>5.09</td>
</tr>
</tbody>
</table>

Note: * AMD denotes “average maximum deviation in percentage” in comparison with its nominal value. Nominal means the results were obtained without process variations.

Table 6.4 tabulates the performance of nine inductorless tunable BPF designs with the pass band ranging from 339 to 1040 MHz. Note that these results are obtained with the case of sweeping $v_{la1}$. The bandwidth is 339 MHz, 445 MHz, 698 MHz, 883 MHz, 1002 MHz, 1009 MHz, 1040 MHz, 1030 MHz, and 989 MHz, respectively. The center frequency is varied from 0.74 to 2.07 GHz: 0.74 GHz, 0.84 GHz, 1.11 GHz, 1.31 GHz, 1.56 GHz, 1.86 GHz, 2.01 GHz, 2.03 GHz, and 2.07 GHz. The nominal pass band gain before considering process variations is between 2.17 and 17.02 dB. Considering process variations on $t_{ox}$, $L_{eff}$ and $v_{th}$ with a maximum 10% variation on its nominal value, the
Monte Carlo simulation results still show acceptable anti-process variation ability of the BPF: 5.71% deviation with respect to nominal center frequency. The average maximum deviation in percentage on pass band gain is 6.7% with respect to their nominal pass band gain. And, the average maximum deviation in percentage on bandwidth is 7.81% with respect to their nominal bandwidth.

6.4 Comparison and analysis

Fig. 6.15 depicts noise figure (NF) comparison among passive inductor BPF, active drain inductor BPF and inductorless BPF. It is shown that the passive inductor BPF has almost same NF (< 6 dB) as the active drain inductor BPF; the inductorless BPF has higher NF (< 12 dB) than the passive and active drain inductor BPF. Fig. 6.16 shows the tuning span comparison among passive inductor BPF, active drain inductor BPF and inductorless BPF. They are BPF1 (the passive inductor), BPF2-C1 (active drain inductor BPF with higher pass band gain), BPF2-C2 (active drain inductor BPF with lower pass band gain), BPF3-C1 (inductorless BPF with sweeping $V_{ia1}$ ) and BPF3-C2 (inductorless BPF with sweeping $V_{lb1}$ ). We find that the tuning span between passive inductor BPF and inductorless BPF are pretty close (around 1 GHz). The tuning span of active drain inductor BPF is much increased to 7.74 GHz, which is much higher than the passive inductor BPF and inductorless BPF. Furthermore, the maximum and minimum pass band gains of each BPF are depicted in Fig. 6.17. The passive inductor BPF achieves the highest pass band gain from 52.8 dB to 59.9 dB. The active drain inductor BPF with lower tuning span but achieves almost constant pass band gain of 22.4 dB. The active drain inductor BPF with higher tuning span achieves a low minimum pass band gain of
8.14 dB. The inductorless BPF with sweeping $V_{la1}$ and $V_{lb1}$ has a low minimum pass band gain of 2.17 dB but their maximum pass band gain of 19.5 dB, which is comparable with the active drain inductor BPF.

![Fig. 6.15 Noise Figure (NF) comparison among passive inductor BPF, active drain inductor BPF and inductorless BPF](image)

In summary, among the three types of band pass filter, each one of them has their advantages and disadvantages: the passive inductor based BPF has highest pass band gain, low noise figure but has narrower tuning span. The active drain inductor based BPF has widest tuning span, and relatively lower pass band gain. The inductorless based BPF takes much smaller chip area, has easier-to-tune but has relatively narrower tuning span, lower pass band gain, a higher noise figure.
Fig. 6.16 Tuning span comparison among different types of BPF. Note: BPF1 (passive inductor BPF); BPF2-C1/C2 (active drain inductor BPF with different tuning span); BPF3-C1 (inductorless BPF sweep $V_{t1}$); BPF3-C2 (inductorless BPF sweep $V_{t2}$)

Fig. 6.17 Passband gain comparison among different types of BPF. Note: BPF1 (passive inductor BPF); BPF2-C1/C2 (active drain inductor BPF with different tuning span); BPF3-C1 (inductorless BPF sweep $V_{t1}$); BPF3-C2 (inductorless BPF sweep $V_{t2}$)
7 CONCLUSION

7.1 Summary

In this dissertation, an efficient tuning algorithm to optimize design parameters of a RF passive inductor based band pass filter for tunable center frequency in a wide frequency span (e.g., 1 GHz) was first presented. The measured results in TSMC 180 nm CMOS technology show that when the central frequency was varied from 1.0 to 2.04 GHz and the pass band was kept nearly constant 12 MHz, the tunable BPF had a high pass band gain (52.76 to 59.87 dB), a low noise figure (1.49 to 5.88 dB) and a low power (15 mW). The narrow bandwidth with steep roll-off can block adjacent interferers in saw less GPS receiver. The pass band is also tunable, which can be varied from 5.5 MHz to 51.2 MHz with pass band gain varied from 65.1 to 45.2 dB while its center frequency is swept from 1.0 to 2.04 GHz.

Next, to design an active inductor based BPF, a high inductance floating CMOS RF active inductor with high Q factor is proposed, which uses resistive feedback and negative resistance block (NR). Changing design parameters, an active inductor for a tuning inductance range from 52 nH to 1462 nH at frequency of 1.52 GHz, and a maximum Q factor of 553k at frequency of 1.27 GHz is designed in 1.8 V 180 nanometer TSMC CMOS process. Its inductive range can be up to 3.09 GHz. The inductor also achieves low power consumption of 2.8 mW.
An active drain inductor based BPF was designed. This BPF includes passive and active inductors. The design analysis results show that when the central frequency was swept from 0.39 to 3.09 GHz and the pass band was varied from 10.1 to 56.2 MHz, the tunable BPF achieved an almost constant high pass band gain (21.1 - 22.5 dB), a low noise figure (1.81 - 5.42 dB) and a low power (18.6 mW). Its center frequency tuning range could be extended up to 7.74 GHz (0.39 - 8.13 GHz) when the pass band was varied from 10.1 to 83.2 MHz and the pass band gain is from 8.14 to 22.5 dB.

After analyzing the CMOS circuit model for active inductor, an inductorless based BPF (fully CMOS integrated) was presented. Its tunable capability is achieved by controlling bias voltages $V_{ta1}$ and $V_{tb1}$. The simulation results of BPF with sweeping $V_{ta1}$ show that when the central frequency was changed from 0.74 to 2.07 GHz and the pass band was from 339 MHz to 1040 MHz, the tunable BPF had pass band gain (2.17 to 17.04 dB), a low noise figure (6.3 to 10.2 dB) and a low power (22.6 mW). The simulation results of BPF with sweeping $V_{tb1}$ show that the center frequency tuning range was from 1.15 to 2.41 GHz, the pass band was from 721 to 3056 MHz, and the pass band gain was from 4.83 to 19.7 dB.

Monte Carlo process variations by altering gate oxide thickness ($t_{ox}$), the threshold voltage ($V_{th}$) and transistor length in Gauss distribution to test the performance of tunable passive inductor BPF, active drain inductor BPF and inductorless BPF, and achieved acceptable results was conducted. Meanwhile, the functional verification of the three types of tunable BPF was also proved. The synthesis of the whole design was elaborately presented. Monte Carlo process variation analysis in design synthesis to optimize the
tunable BPF circuit parameters for best performance in a wide tuning frequency range and pass-band bandwidth was discussed.

7.2 Future Research

My future research will study design approaches to improve tunable capability of passive and active inductor based double notch band pass filters. A robust wide tuning inductive AI and its applications in designing wide tuning inductorless BPF will be studied. Techniques to improve pass band gain, dynamic pass band will be studied. Designing high performance active capacitor and integration to CMOS fully integrated RF double notch band pass filter to meet robust needs of reconfigurable RF will be studied.
8 REFERENCE


[24] Hsiao, C-C., Kuo, C-W., Ho, C-C., Chan, Y-J., “Improved quality-factor of 0.18-um CMOS active inductor by a feedback resistance design,” IEEE Microwave and Wireless Components Letters, VOL. 12, NO. 12, pp. 467-469, December 2002


