Wide Tuning Range I/Q DCO VCO and A High Resolution PFD implementation in CMOS 90 nm Technology

A thesis submitted in partial fulfilment of the requirements for the degree of Master of Science in Electrical Engineering

By

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B.Tech., Jawaharlal Nehru Technological University, 2013.

2015
Wright State University
I HEREBY RECOMMEND THAT THE THESIS PREPARED UNDER MY SUPERVISION BY Eswar Raju Suraparaju ENTITLED Wide Tuning Range I/Q DCO VCO and A High Resolution PFD implementation in CMOS 90 nm Technology BE ACCEPTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF Master of Science in Electrical Engineering.

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ABSTRACT

Suraparaju, Eswar Raju M.S.E.E., Department of Electrical Engineering, Wright State University, 2015. Wide Tuning Range I/Q DCO VCO and A High Resolution PFD implementation in CMOS 90 nm Technology

This thesis presents wide tuning range in-phase and quad-phase (I/Q) output digital control oscillator (DCO) and voltage control oscillator (VCO) and a simple high performance phase frequency detector (PFD) in 90 nm CMOS technology with 1.2 V power supply. The designed I/Q output DCO has an operating frequency range from 1.1-8.2 GHz with high resolution and wide linearity by using a novel skew delay structure. At 2.02GHz oscillation frequency, the measured phase noise of I/Q output DCO is -90.43dBc/Hz at an offset of 1 MHz offset and has 5 mW of power dissipation. A complementary series coupled quadrature VCO (S-QVCO) is also implemented with measured phase noise of -114.1 dBC/Hz at an offset of 1 MHz from 3.5 GHz center frequency. The operating range of the designed S-QVCO is 3.05-4.62 GHz and has 2.6 mW power dissipation. A simple high resolution novel PFD is designed for high frequency signal detection and low jitter phase locked loop applications. The proposed PFD design can operate over a wide range of frequencies from 10 kHz to 6 GHz and can detect phase differences for inputs as small as 125 fs for all frequencies of operation and for all process corners.
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Dedicated to my family and friends
1. INTRODUCTION

Phase Locked Loops (PLLs) have a wide range of applications in various areas and have prominent importance in today’s communication. PLLs are widely used in radio frequency (RF) circuits, clock and data recovery systems, analog-to-digital converters (ADCs), computers, amplitude modulated radio receivers, demodulators, and frequency synthesizers. In the early 20th century, PLLs were used for the first time in the synchronization of vertical and horizontal scans of television. The first PLL ICs were built by using purely analog components. High performance PLL design specifications were achieved by recent advancements in integrated circuit design techniques. Today PLL circuits are being integrated as a part of a larger circuit on a single chip.

In general PLLs are implemented by using analog LC components because of their low phase noise performance, but their tuning range is less when compared to some other types of PLL designs. Analog PLLs suffer from high noise due to process voltage and temperature variations (PVT) and variations in the layout. Furthermore, analog PLLs requires redesigning if the IC feature size is changed. Several advancements in recent years have taken place to allow fully digital controllable phase locked loops to overcome the disadvantages of analog PLLs. Digital phase locked loops have high noise immunity and better tolerance to PVT and bias variations when compared to analog PLLs. One of the most important critical performance parameters of a PLL is the phase noise. Developing PLLs with low power dissipation and low phase noise is became challenging. In addition,
large tuning range, fine frequency resolution and fast locking time are also desirable for a high frequency PLLs.

A phase locked loop is a closed loop control system that generates an output signal whose phase and frequency is analogous to the phase and frequency of the input reference signal. The feedback signal of a PLL comes from either an oscillator or a frequency divider circuit. Typical analog PLLs have five building blocks. These are

1) A phase frequency detector (PFD),
2) A charge Pump (CP),
3) A low pass loop filter (LPF),
4) A voltage control oscillator (VCO)
5) A frequency divider.

In the following Fig.1, the conventional block diagram of an analog PLL as described above is shown.

Fig. 1. Block diagram of an analog PLL
Fully digital PLLs are the exact digital versions of the analog PLL counterpart’s in operation. Fully digital PLLs are also known as All Digital Phase Locked Loops (ADPLLs). Here mainly Charge Pump, Loop filter and Voltage control oscillator of an analog PLL are replaced with a digital integrator, a digital filter and a Digital Control Oscillator (DCO). Digital Control Oscillators (DCOs) cannot generate continuous frequency of oscillations, whereas Voltage Control Oscillator which uses analog components produce continuous oscillation frequencies. To overcome this, a very high resolution DCO is required. The general block diagram of a fully digital PLL is shown below in Fig. 2.

![Block diagram of a fully digital PLL](image)

**Fig. 2.** Block diagram of a fully digital PLL

The study of In-phase and Quadrature phase signal generation techniques has acquired prominent importance as they are becoming essential for the implementation of image-rejection transceivers and also for up and down conversion of signal. Therefore a low phase noise, low power dissipation, wide tuning range and very high resolution In-phase and Quadrature phase oscillator outputs are required.
Phase frequency detectors are also playing a crucial role in calculating the performance of a PLL system. Some of the performance characteristics of a PFD are dead-zone, frequency of operation and power dissipation. Dead zone errors and output glitches of a PFDs will introduce jitters in the PLL system. Therefore, PFDs with no output glitches and dead zone errors are preferred.

Due to the reasons explained above, I/Q phase output oscillators with low phase noise and low power consumption, and PFDs with no dead zone errors and output glitches are required. The previous works in [10-13] presents CMOS ring oscillators having I/Q phase outputs. The design analysis for dual-delay path CMOS ring oscillators was performed in [12]. Papers [14-25] introduce various Q-VCOs with low-phase noise performance. Paper [18] introduced a parallel coupled Q-VCO for the first time. The phase noise of parallel coupled Q-VCO was improved in papers [17-20].

Papers [27-31] show various PFD design implementations. The conventional PFD design is presented in paper [27]. A dead zone error of 15 ps is designed in paper [3]. Paper [29] proposed a new PFD design to minimize the dead zone error to near 750 fs.

This chapter talks about various techniques for generating multi-phase signals and also phase frequency detectors (PFDs) that are commonly used in PLL systems. The goal of this research is to design and develop a high performance In-Phase and Quadrature Phase Outputs for both DCO, VCO and also a simple high performance phase frequency detector for a PLL operating at very high frequencies.
1.1 Objective

The main objective of thesis is to design a high frequency wide tuning range I/Q phase output DCO and VCO with low phase noise, and a simple phase frequency detector with a dead zone error of near zero. A new PFD design architecture and a skew delay cell is proposed in this work. The design goals of this thesis, was achieved with the designed skew delay cell in DCO and opting complimentary series coupling method for VCOs. The dead zone error of PFD is minimized to near zero by using the proposed novel PFD architecture.

1.2 Multi-Phase Signal Generation Techniques

This section overviews the design methodologies to generate quadrature outputs. The most widely used design techniques for quadrature output signal generation are phase shifters, ring oscillators and frequency dividers and LC VCOs [1]. The design constraints of each method are also discussed in this section.

1.2.1 Passive Phase Shifting

The common method used for generating multiphase outputs from a single input reference signal is by using passive RC and CR networks. A combination of low-pass and high-pass RC filter circuit is shown in Fig. 3. This combination of RC-CR circuits can produce quadrature output signals from a single sinusoidal input reference signal. It produce 90 degrees phase shift between the outputs always regardless of the frequency of operation of the input reference signal. This circuit has a drawback of amplitude mismatching where the amplitudes of the generated signals are equal only at the cut-off
frequencies of the filters. The quadrature accuracy also get into effect due to mismatches between the elements of the RC and CR filters.

![RC and CR phase shifter circuit](image)

**Fig. 3.** RC and CR phase shifter circuit

### 1.2.2 Ring Oscillators

Ring oscillators are widely used for generating multi-phase clock outputs. The minimum number of stages required to produce oscillation in ring oscillators is three. Conventional ring oscillators comprises of an odd number of inverter stages. Ring oscillators have also the tendency to produce oscillations with even number of stages if conventional inverter delay elements in ring oscillator are replaced with other delay cells. Most commonly used delay cells in ring oscillators for generating multi-phase outputs are
skew delay cells and differential dual delay cells. The following Fig. 4 shows the typical ring oscillator structure with n number of stages.

![Ring Oscillator Diagram]

Fig. 4. Conventional ring oscillator circuit

\[ F_{osc} = \frac{1}{2dn} \]

(1.1)

As shown in Fig. 4, d is the propagation delay of each stage, \( \theta_1 \), \( \theta_2 \), \( \theta_3 \) and \( \theta_n \) are the phased outputs at stage1, stage2 and stage3 and stage n respectively, n is the number of stages. The cell delay and number of stages of a ring oscillator plays an important role as it determines the oscillation frequency. In order to generate more phased outputs, more inverters are need to be added. This results in high oscillation time period and less oscillation frequency. The usage of ring oscillator structures is also reduced in wireless systems due to their high phase noise value. The ring oscillators have high phase noise when compared to LC VCO oscillators for a given power constraint.

1.2.3 Multi-Phase Signal Generation using Divide-by-N

The commonly used design for generating quadrature outputs is by using frequency dividers. D flip-flops can act as a frequency divider by 2 circuit when the inverted output of D flip-flop is connected to the data D input of it. The generation of quadrature output by
using D flip-flop is shown in Fig. 5. Here the in-phase and out phase of a clock signal operating at a frequency of 2f is used to obtain in-phase and quad–phase outputs at a frequency f. The same method can be extended for generating N number of phases, by using a frequency divider of N. The drawback of using this method is, the input frequency is getting divided by N in generating N phased outputs. The power dissipation is also getting more, because it is high operating frequency. It offers a better phase noise compared to poly-phase filters because it avoids usage of lossy passive networks.

Fig. 5. Quadrature phase generation using divide-by-2

1.2.4 Generation of Quadrature Outputs using LC VCOs

The most attractive design approach for generating quadrature outputs is by using LC voltage control oscillators (VCOs). LC VCOs exhibit a very good phase noise performance provided by either a good on-chip inductor or an off-chip inductor with high Q value. LC VCOs can produce quadrature outputs by coupling two symmetrical LC VCO tanks to each other. The tuning range of LC VCOs is less when compared to other types of
oscillators. The detail operation and generation of Quadrature LC VCO (QVCO) is discussed in chapter 3.

1.3 Phase Frequency Detector

Phase frequency detectors (PFDs) are one of the key sub-circuit of PLLs. The main function of this PFDs is to compare the phase and frequency difference between the input signals and output the phase and frequency difference of them.

Analog phase detectors can be implemented by using a simple mixer or a multiplier as shown in Fig. 6. Compared to the digital counterparts analog phase detector operate at high frequencies, and inputs can be sinusoidal. The design complexity of analog phase detectors is huge compared to the digital phase detectors. Analog phase detectors also requires large circuit area and power consumption.

Fig. 6. Multiplier based Phase detector

Here $X_1(t)$ and $X_2(t)$ are the two inputs of multiplier and $X_3(t)$ is the multiplier output. The output of this multiplier needs to be passed to a LPF in order to obtain the phase difference between the inputs.
Some of the widely used digital phase and frequency detector circuits for detecting the phase and frequency difference between the two signals are listed below.

1. EX-OR gate
2. Phase Frequency Detector using D-flip flops
3. JK flip-flop

The following Fig. 7, shows the ideal characteristics of a PFD. As shown in Fig. 7, $\theta_d$ is the phase difference between the input reference signal to divider feedback signal of a PLL. The ideal characteristic curve passes through origin and have positive slope for the positive difference of $\theta_d$ and negative slope for the negative difference value of $\theta_d$. The positive difference value indicates the reference input signal is leading the divider feedback signal and negative difference value refers to the lagging of reference signal with respect to the divider signal.

![Fig. 7. Ideal characteristics of a Phase frequency detector](image)
1.4 Thesis Organization

This thesis is structured as follows. Chapter 2 introduces the operation of the skew delay cell and the novel DCO architecture with the proposed skew delay cell. Chapter 3 explains the various methods used for improving the performance of the quadrature LC VCO. Chapter 4 introduces the different types of PFD and a simple high performance novel architecture of the PFD. Chapter 5 concludes the work and future work, and followed by references in Chapter 6.
2. A wide tuning range I/Q phase output DCO

Digital Control Oscillators (DCOs) are the most critical and important building blocks of the ADPLLs. ADPLLs are robust to PVT variations and they are replacing the present analog PLLs. ADPLLs also have full digital control over the frequency range, fast frequency locking and good stability compared to the analog PLLs [2]. Many applications require in-phase (I) and quadrature (Q) phase output clock signals for up and down conversion with low phase noise, low power consumption, and wide tuning range specification [3].

Most of the digital control oscillator designs use ring structure because of its easy frequency controlling feature and simple design structure. In ring oscillators, the structure of each stage is similar to the others. The oscillation frequency of a three stage ring oscillator is shown in Fig. 8 and is estimated by using Eq. (2.1).

![Diagram of a conventional three stage static CMOS ring oscillator](image)

\[ F_{osc} = \frac{1}{2(t1+t2+t3)} = \frac{1}{2T} \]  

(2.1)

As shown in Fig. 8, t1, t2, t3 are the propagation delays of stage1, stage2 and stage3, and T is the total propagation delay of the three stage inverter ring oscillator. In general,
an odd number of inverter stages are needed to generate oscillation in a ring oscillator. Multi-phase outputs can be generated by using even number of stages. The cell delay and the number of stages of a ring oscillator plays an important role as they determines the oscillation frequency. In order to obtain more phased outputs, more inverters are need to be added, which results in high oscillation time period and less oscillation frequency.

The stage delay of the ring oscillator can be reduced by using skewed delay cells in a ring oscillator [4]. Most of the CMOS ring oscillators produce in-phase and Quadrature phase outputs by using four input differential delay latch cell with voltage control input which is used for analog PLL. This voltage control oscillator is more sensitive to the PVT variations and tuning range of it is also reducing when the technology is getting scaled down. Considering all the design constraints, a novel skewed digital delay cell is proposed and designed in this work for obtaining high operating frequencies and wide tuning range with low power consumption.

2.1 Operation of the skew delay cell

A new skewed delay cell is proposed in this work for achieving higher operating frequency and wide tuning range. The schematic of the proposed skewed delay cell is shown in Fig. 9 [5]. The delay of the conventional skewed delay cell and the static CMOS inverter cell can be reduced as follows. NMOS and PMOS transistors with negative delayed input are added in parallel to the pull-down and pull-up networks of the static CMOS inverter, respectively as shown in Fig. 9.
In Fig. 9, the input \(in\) is applied to PMOS P1 and NMOS N1 transistors and they act as the static CMOS inverter. The \(in'\) input signal is the skewed delay signal or negative delayed signal is used to reduce the propagation delays of both rising and falling transition time, resulting minimized cell delay.

The transition operation of the static CMOS cell and proposed skew delay cell is shown in Fig. 10, where \(in\) is the input signal and \(in'\) is the skewed delay signal; the Conventional is the output of the conventional static CMOS inverter and Proposed is the output for the proposed cell. When input \(in\) is making low-high transition, N2 is turned on.
prior to N1 transistor with the help of \textit{in'} input goes to high ahead of \textit{in}, this reduces the output high-low transition delay. Similarly in case of the high-low input transition, the P2 turns on prior to the P1 transistor with the help of \textit{in'} input goes to low before \textit{in}, leading to the reduction in the low-high output transition delay. Therefore the total transition time of the proposed design is less than the conventional static CMOS design.

Fig. 10. Transition operation of the conventional static CMOS cell and Proposed Skew delay cell
2.2 Four stage ring oscillator with I and Q output

Fig. 11. Four stage ring oscillator having I-Q outputs

Combine four proposed skewed delay cells in Fig. 9 to build a four stage ring oscillator with I-Q as shown in Fig. 11. In Fig. 11, the bold lines represents main loop and the dotted lines represents the skewed delay input connections. The output of each stage is connected to the input of next stage and to the skewed delayed input of the stage after next. This connections make the delay cells to produce four 90 degrees phase shifted output signals, Q+, I-, Q- and I+ i.e. 90, 180, 270 and 360 degrees respectively.

2.3 Operation of the skew delay cell

Various techniques are used for controlling the oscillating frequency of a DCO. Some of the widely used techniques are changing the driving strength by using fixed capacitance loading, stage selective ring oscillator technique, and also by load capacitance tuning with shunt capacitances [6],[7].
2.3.1 **Drive strength controlling using the fixed capacitive load**

In this technique the delay of the inverter cell is controlled by switching either of the parallel connected NMOS or PMOS transistors. The NMOS and PMOS transistors are connected in parallel to the conventional inverter delay cell as shown in Fig. 12. The widths for NMOS and PMOS transistors are assigned in linear increasing fashion. When all the transistors are turned ON the drive strength of the cell is increased and makes the delay of inverter cell to be minimum. Similarly in order to increase the delay of the inverter cell the more number of NMOS and PMOS transistors are need be tuned OFF.

![Diagram](image)

*Fig. 12. Drive strength controlling using fixed capacitive load*
2.3.2 **Shunt capacitance control technique**

Shunt capacitive technique is used for varying the frequency of an oscillator. In this technique the delay of a cell is varied by adding capacitances to the load. The effective load capacitance of a cell can be controlled by using digital control switches. The maximum frequency of operation can be obtained with a small capacitive load and minimum frequency of operation can be obtained with large effective capacitive load. There is a tradeoff in the DCO design between operating range and the maximum frequency of operation. In order to obtain large tuning range the number of capacitive load switches need to be increased. This results in higher power consumption and also decreases the maximum frequency of operation. As shown in Fig. 13, the delay of the cell is controlled with shunt capacitances by using digital switches. Here the drain and source of a MOSFET is connected to ground to act as a capacitor.

![Shunt capacitive controlling technique](image)

*Fig. 13. Shunt capacitive controlling technique*
2.3.3 Stage selective frequency controlling technique

As the delay of a ring oscillator depend on the number of stages. Therefore the frequency of oscillation can be increased or decreased by selecting the number of stages. As the number of stages in a ring oscillator increases the total time period of oscillation also get increased. This decreases the frequency of oscillation as the period of oscillation is increased.

The selection of the stages in a ring oscillator can be performed by using a multiplexer and selection signals. Other techniques such as switches could be used. In a switch method the capacitive loads are different at different stages. Whereas multiplexer provides fixed load capacitance for every ring oscillator path. This technique has poor frequency resolution when compared to the above mentioned controlling techniques. As shown in Fig. 14, multiplexer is used for selecting the number of stages of a ring oscillator.

![Fig. 14. Stage selective frequency controlling technique](image)
2.4 14-bit Digital control delay cell

As the drive strength controlled technique has better controlling feature compare to others, the designed 14-bit DCO use a fixed capacitive load NMOS drive strength controlled technique to control the oscillation frequency. Here the capacitive load of each delay cell in the ring oscillator is made constant and the driving strength of the delay cell is controlled with the help of 14 digital control input pins. The schematic of delay cell 1 that is used in the four stage ring oscillator design is shown in Fig. 15.

![Schematic of the delay cell 1 of a ring oscillator](image)

Fig. 15. Schematic of the delay cell 1 of a ring oscillator shown in Fig. 11

As seen in Fig. 15, 14-bit digital input pins are given to the NMOS transistors having widths that increase linearly to the digital input pins. The minimum width of the transistor is connected to the smallest numbered digital input pin and maximum width of
the transistor is connected to the largest number digital input pin. The width of the transistor is inversely proportional to resistance of the transistor. When the digital inputs are made high, the NMOS transistors present in the pull-down ladder network is turned on. This minimizes the resistance of the pull down network. The driving strength of the cell becomes larger and drives maximum current into it, resulting in less delay for the cell. Similarly when the digital inputs are made low, the delay of the cell increases resulting in low frequency of oscillations. The oscillation period generated by DCO is TDCO, and is a function of the digital input bits given in [8].

\[
R \propto \frac{1}{W} \tag{2.2}
\]

\[
T_{\text{constant}} = R \cdot C \tag{2.3}
\]

\[
T_{\text{DCO}} = f (d_{n-1} \cdot 2^{n-1} + d_{n-2} \cdot 2^{n-2} + \ldots \ldots + d_1 \cdot 2^1 + d_0 \cdot 2^0) \tag{2.4}
\]

Here R is the channel on resistance and W is the width of the transistor, C is the load capacitance and TDCO is the period of oscillation.

2.5 Simulation Results

The 14-bit digital control oscillator is implemented in CMOS 90 nm technology with 1.2 V voltage supply as seen in Fig. 16. The schematic simulation results show that the designed DCO has a frequency tuning range from 1.1-8.2GHz with a tuning range of 7.1GHz (87%).
Fig. 16. Full schematic of the designed 14-bit DCO

The following Table 1 shows the variation of DCO frequency for different combinations of digital control pins.

<table>
<thead>
<tr>
<th>Control bits</th>
<th>Frequency (GHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>14-13 12-9 8-5 4-1</td>
<td></td>
</tr>
<tr>
<td>0 0 0 0</td>
<td>1.1</td>
</tr>
<tr>
<td>0 0 0 3</td>
<td>1.33</td>
</tr>
<tr>
<td>0 0 0 F</td>
<td>1.78</td>
</tr>
<tr>
<td>0 0 1 D</td>
<td>2.03</td>
</tr>
<tr>
<td>0 0 2 F</td>
<td>2.32</td>
</tr>
<tr>
<td>0 0 5 7</td>
<td>2.68</td>
</tr>
<tr>
<td>0 0 C 6</td>
<td>2.77</td>
</tr>
<tr>
<td>0 0 7 C</td>
<td>3.22</td>
</tr>
<tr>
<td>0 0 B A</td>
<td>3.53</td>
</tr>
<tr>
<td>0 0 F D</td>
<td>4.21</td>
</tr>
<tr>
<td>0 1 7 8</td>
<td>4.47</td>
</tr>
<tr>
<td>0 1 E C</td>
<td>5.03</td>
</tr>
<tr>
<td>0 6 0 7</td>
<td>5.92</td>
</tr>
<tr>
<td>0 9 C 3</td>
<td>6.57</td>
</tr>
<tr>
<td>0 A E 7</td>
<td>6.82</td>
</tr>
<tr>
<td>0 F C 3</td>
<td>7.33</td>
</tr>
<tr>
<td>1 F C 3</td>
<td>7.63</td>
</tr>
<tr>
<td>3 D 1 F</td>
<td>8.2</td>
</tr>
</tbody>
</table>

Table 1. Frequency of oscillation for different control input pins
As seen from the above Table 1, the designed DCO operates from 1.1 GHz- 8.2 GHz with a tuning range of 7.1 GHz by varying 14 digital control pins.

The following Fig. 17, shows the relation between the control word and the output oscillation frequency. From Fig. 17, it can be clearly deduced that with the increase in the control bits from [0000H-3FFFH] the output frequency of the DCO is increased from 1.1-8.2GHz. The power consumption of the circuit also get increased because of the increase of driving current in the pull down network and oscillation frequency.

![Fig. 17. Variation of DCO frequency with control word](image)

The resolution of the DCO is 433.3 KHz and it is calculated by using Eq. (2.5), where MSB is the highest oscillation frequency and LSB is the lowest oscillation frequency.
Phase noise of the simulated design is shown in Fig. 18. The phase noise of the DCO is -90.43dBc/Hz at 1MHz offset and -117.64dBc/Hz at 10MHz offset frequency with the carrier frequency of 2.02 GHz and consumes 5 mW power.

\[ Resolution = \frac{MSB-LSB}{Total\ Control\ words} \]  \hspace{1cm} (2.5)

Fig. 18. Phase noise performance of the designed DCO

The Figure of Merit (FoM) of the designed DCO is -156.8dBc/Hz at 10 MHz offset frequency, which is calculated from a widely used [9] Eq. (2.6).

\[ FoM = L\{f_{offset}\} - 20\ log\left(\frac{f_o}{f_{offset}}\right) + 10\ log\left(\frac{P_{DC}}{1\ mW}\right) \]  \hspace{1cm} (2.6)
Here FoM is the Figure of merit, \( f_{\text{offset}} \) is the measured phase noise at offset \( \Delta f \), 
fo is the oscillation frequency and \( P_{\text{DC}} \) is the power dissipation in mW.

The performance comparison with other DCOs and VCOs with I/Q outputs is shown in Table 2 below:

<table>
<thead>
<tr>
<th>Ref</th>
<th>Technology</th>
<th>Supply voltage</th>
<th>Output frequency</th>
<th>Phase noise (dBc/Hz)</th>
<th>Pdiss (mW)</th>
<th>FoM (dBc/Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>This work</td>
<td>90 nm</td>
<td>1.2 v</td>
<td>1.1-8.2GHz</td>
<td>-90.4@1 MHz</td>
<td>5</td>
<td>-156.8</td>
</tr>
<tr>
<td>[10]</td>
<td>600 nm</td>
<td>2.5 v</td>
<td>900 MHz</td>
<td>-105.5@600 KHz</td>
<td>15.4</td>
<td>-157.1</td>
</tr>
<tr>
<td>[11]</td>
<td>180 nm</td>
<td>2 v</td>
<td>630 MHz</td>
<td>-108</td>
<td>22</td>
<td>-150.6</td>
</tr>
<tr>
<td>[12]</td>
<td>180 nm</td>
<td>1.8 v</td>
<td>1861 MHz</td>
<td>-102</td>
<td>13</td>
<td>-156.3</td>
</tr>
<tr>
<td>[13]</td>
<td>600 nm</td>
<td>3 v</td>
<td>900 MHz</td>
<td>-117@600KHz</td>
<td>30</td>
<td>-165.7</td>
</tr>
</tbody>
</table>

Table 2. Performance comparison with other DCOs and VCOs with I/Q outputs

The final design of the DCO is also verified for process variation by doing Monte Carlo simulation with random sampling method for 10 points. The following figure Fig. 19, shows the Monte Carlo simulation outputs for in-phase and quadrature phase for 10 points. The frequency of designed DCO is varied for different process corners. The simulation results verify that the design is robust to process variations. As shown in Fig. 19, the outputs are able to produce output for all the 10 iterations and shows good phase accuracy between the in-phase and quadrature phase outputs. The designed DCO has a phase error value less than 1.5\(^0\) between the in-phase and quadrature phase outputs.
The final output waveforms of the designed DCO at 5GHz oscillation frequency is shown in the following Fig. 20. The four outputs of the designed DCO are phase shifted by 90 degrees each.
Fig. 20. Final simulated output result of the designed DCO with I/Q outputs

Here the In-phase and Quadrature Phase are labeled as I+ (0°), Q+ (90°), I- (180°), and Q- (270°). The maximum phase error of the designed DCO is less than 1.5 degrees over the complete tuning range.

The period of oscillation is constant from one cycle to the other cycle in an ideal oscillator. But in practice, the period of oscillation vary from cycle to cycle due to some noise variations. The undesired deviation of the oscillation period of a signal from its nominal period is called jitter. The root mean square (RMS) jitter is defined as the RMS value of period deviations for infinite number of cycles. Whereas the difference between the maximum and minimum value of period deviation is called as peak-peak jitter [14].

The following Fig. 21 shows the eye-diagram of the designed DCO output when operating at 5.32 GHz. Here the simulation time is elapsed for 1000 cycles and the delay is measured at 50% of voltage level for the rising edge to determine the output signal stability. Each and every cycle of the DCO output is overlapped on one clock period, and
the difference between the maximum and minimum deviation gives peak-to-peak jitter value. The peak-to-peak jitter value of the designed DCO when operating at 5.32 GHz oscillating frequency is 1.46 ps.

Fig. 21. Eye-diagram of the designed DCO when operating at 5.32 GHz

2.6 Summary

A new skewed digital delay cell is designed for high speed oscillation frequencies in ring oscillator which is suitable for generating multiphase output signals. The circuit designed generates very high speed oscillation frequencies compared to the conventional multi-phase oscillation circuits that are currently used. Key highlights of the circuit such as wide tuning range; and low power with multiphase outputs makes it an excellent source for very high speed communication systems.
3. Quadrature LC VCO

Voltage control oscillators are one of the most critical and important building blocks of an analog PLLs. Voltage control oscillators offers very good phase noise performance when compared to other digital control oscillators. LC VCO’s consume less power compared to DCOs in designing an oscillator having low phase noise value. The frequency of oscillation in LC oscillator depends mainly on the values of L and C.

The frequency of oscillation can be controlled by varying the values of L and C. The variation of inductance (L) for controlling the frequency of oscillation is difficult, because it is difficult to vary the size of an inductor in order to obtain different L values. Also inductors consume a lot of area in LC oscillators. The best way to tune the frequency of LC oscillators is with the help of variable capacitors. The maximum frequency of oscillation is obtained for small values of L and C in LC oscillators, because it needs less time in transferring stored energy from capacitor (electro-potential energy) to inductor (magnetic energy) and vice-versa. A low phase noise LC VCO can be designed with high Q value of an on-chip or off-chip inductors.

\[ F_{osc} = \frac{1}{2\pi\sqrt{LC}} \]  

(3.1)

Multi-phase signal generation is extensively used in high speed wireless and wire-line communication systems. There exist a tradeoff between phase noise and phase error in designing multi-phase VCOs. Phase noise plays an important role in wireless communication.
3.1 Phase Noise

The output spectrum of an ideal frequency synthesizer should be a single tone at the desired frequency of oscillation. Random variations in amplitude and phase values of a signal from the desired values supply energy to the side bands of the operating oscillation frequency. Undesirable sidebands are created when the side band energy is mixed with the modulated baseband signal or RF received signal. Some of the key parameters indicating the performance of a frequency synthesizer are phase noise and spurious tones. The ideal equation for a pure sinusoidal signal is given by Eq. (3.2).

\[ V(t) = V_0 \cos (2\pi f_0 t) \quad (3.2) \]

Where \( V_0 \) is the amplitude and \( f_0 \) is the frequency of a pure sinusoidal signal. The waveform of a pure sinusoidal signal deviates due to amplitude and phase fluctuations. The equation for a deviated signal is given by Eq. (3.3).

\[ V(t) = (V_0 + v(t)) \cos (2\pi f_0 t + \phi(t)) \quad (3.3) \]

Where \( v(t) \) and \( \phi(t) \) represents amplitude and phase deviations from ideal sinusoidal signal. Amplitude variations of a signal can be eliminated or reduced greatly by proper designing of oscillators. The elimination of phase fluctuation is became a challenging task in designing a high frequency synthesizers and designers are putting much effort in reducing this phase fluctuations.

If the RMS (root-mean Square) value of \( \phi(t) \) is much smaller than 1 radian, then the above Eq. (3.3) after ignoring amplitude variations is given by Eq. (3.4).

\[ V(t) = (V_0 + v(t)) \cos (2\pi f_0 t + \phi(t)) = V_0 \cos (2\pi f_0 t) - \phi(t) V_0 \sin (2\pi f_0 t) \quad (3.4) \]
The power spectral density of Eq. (3.4) is given by Eq. (3.5).

\[ S_V(f) = V_0^2/2[\delta(f-f_0) + S_\delta(f-f_0)] \]  

(3.5)

The above Eq. (3.5), contains the carrier power at frequency \( f_0 \) and phase noise at an offset frequency \( \Delta f = f - f_0 \). The following Fig. 22, shows the defining of phase noise. The phase noise \( L\{\Delta f\} \) of a single-sideband (SSB) can be defined as the ratio of noise power having in 1 Hz bandwidth at an offset frequency \( \Delta f \) from the carrier frequency to the power of a carrier frequency. The equation for phase noise is given by Eq. (3.6).

Fig. 22. Defining phase noise spectrum
\[ L\{\Delta f\} = 10\log \left( \frac{P_{\text{noise}(f_0+\Delta f)}}{P_{\text{carrier}}} \right) \]  
(3.6)

Here \( P_{\text{noise}}(f_0+\Delta f) \) is the noise power present in 1Hz bandwidth from a carrier frequency \( f_0 \) at an offset frequency of \( \Delta f \), \( P_{\text{carrier}} \) is the carrier frequency power [15].

### 3.2 Phase error

Multi-phase output signals are used for up and down conversion of a signal. Therefore good phase accuracy is needed between the phased output signals. Due to mismatches in phase and amplitudes of multi-phase signals corrupt the up and down converted signals. The main reason for having phase error in multi-phase is due to device mismatches. In general, the relative phase difference between In-phase (I) and Quad phase (Q) of the signals of a quadrature output oscillator design deviates from 90°.

Let
\[ V_I(t) = V_m(I) \cos (\omega t + \theta(I)) \]  
(3.7)
\[ V_Q(t) = V_m(Q) \cos (\omega t + \theta(Q)) \]  
(3.8)

\[ \theta(Q) - \theta(I) = \pi/2 + \alpha \]  
(3.9)

Here \( \omega \) is frequency of oscillation and \( \alpha \) is the phase deviation amount from quadrature signal.

### 3.3 Differential LC VCO

In order to obtain stringent phase noise performance for cellular and wireless communication devices etc. LC oscillators are preferred. In an ideal LC tank oscillators
there are no losses associated with L and C components. But in reality the on chip inductors have finite losses with them. If $R_s$ is the series resistance of an inductor (L), the value of $R_s$ depends on the value of $Q$ and is shown in following Eq. (3.10).

$$R_s = \left( \frac{L}{\omega} \right) \frac{1}{Q} \quad (3.10)$$

LC tanks offers a low inductive losses for high values of $Q$. If energy is injected into the lossy LC tank, it will try to oscillate and get damped down exponentially because of its lossy components. The series inductive loss resistance and other capacitive losses can converted into parallel resistance ($R_p$). Now in order to obtain sustain oscillations a negative resistance need to be added in parallel to the lossy LC tank.

In general active devices are used to overcome the energy loss in LC tanks. The following Fig. 24, shows the two cross coupled NMOS transistors and equivalent circuit of cross coupled pair. The equivalent resistance for the following circuit is given by
Fig. 24. (a) NMOS cross-coupled pair (b) Equivalent circuit of a cross coupled pair

\[ \frac{V_x}{I_x} = -\frac{2}{g_m} \quad (3.11) \]

As we are connecting negative resistance in parallel to the lossy resistive LC tank, the value of the negative resistance should be less than the effective \( R_p \) value for obtaining stable oscilltion. Therefore the condition for obtaining oscillation for a LC core VCO is given by Eq. (3.12).

\[ R_p > \frac{2}{g_m} \quad (3.12) \]

The three design topologies of cross-coupled LC VCO structures that are commonly seen are complementary cross-coupled, N-MOS only, and PMOS-only.
3.4 Quadrature LC VCOs

In general, phase shift networks are used to generate multi-phase output signals from a single reference input signal. As the frequency of oscillation changes integrated phase shifters suffers from amplitude variation and phase errors between the quadrature outputs.

Efforts have been made to generate the quadrature output signals from LC oscillators because of their good phase noise performance. The generation of quadrature outputs can be done by proper coupling of two identical differential LC VCOs. The following Fig. 25, shows that the combination of direct connection and inverting (cross) connection makes the two VCOs to oscillate in quadrature [16].

![Fig. 25 Block diagram of a QVCO](image)

3.5 Types of Q-VCOs

Some of the commonly used design topologies of Q-VCOs are parallel coupled QVCO (P-VCO), series-coupled QVCO (S-QVCO) and transformer coupled QVCO. The topology types are defined based on the connection of coupling transistors in the VCOs. In this chapter P-QVCO and S-QVCO design topologies are discussed.
The two important performance parameters of Q-VCOs are phase noise and phase error. In general, they are not independent of one another. Phase noise and phase error values in P-QVCO are mainly depend on the value of $\alpha$. Where $\alpha$ is defined as the ratio of the width of coupled transistor to the width of switching transistors.

$$\alpha = \frac{W_{cpl}}{W_{sw}} \quad (3.13)$$

The phase noise is inversely proportional to $\alpha$, whereas phase error is directly proportional of $\alpha$. The low phase noise was achieved for the value of $\alpha = 1/3$, through the original value of $\alpha$ is unity [17]. Therefore we can improve the phase noise in P-QVCO by scarifying phase error. Whereas in S-QVCO the phase error is independent on the value of $\alpha$. This allows us the flexibility in choosing the value of $\alpha$ for low phase noise.

### 3.5.1 Parallel coupled Q-VCO

The parallel coupling method for generating the quadrature outputs proposed by Roffougaran [18] and is shown in the following Fig. 26. Here the coupling between the two VCOs is applied by placing transistors $M_{cpl}$, in parallel to the switch transistors $M_{sw}$. The parallel coupled quadrature VCO (P-QVCO) outputs four quadrature signals showing low amplitude and phase errors. Phase shifters were introduced between the cascaded LC resonators [19], [20] of a P-QVCO to improve the phase noise, but they resulted design complexities and also increased power consumption.
3.5.2 Series coupled Q-VCO

The other design methodology used for generation of quadrature outputs by using coupled of LC VCO is series-coupling. The schematic of the S-QVCO is shown in the following Fig. 27. Here the coupling transistor \( M_{cpl} \) is connected in series with the switch transistor \( M_{sw} \), rather in parallel. As the parallel coupling in the P-QVCO degrading the phase noise performance, the series coupling i.e. cascode like fashion was done to improve the phase noise. The flicker noise is less in S-QVCO because of the operation of cross-coupled switches in triode region for most of the oscillation time period [21].
3.6 Complimentary series coupled QVCO

In general complementary LC VCOs are preferred for low power and large output voltage swing. Complimentary LC VCOs consume less power because they produce negative resistance value two times larger than PMOS and NMOS-only LC VCOs for a particular bias current value. Complimentary VCO also helps in improving the switching of cross-coupling pair [17]. It also has better rise and fall times, which improves the up conversion 1/f noise.

Based on the advantages of series coupled Q-VCO design topology and complimentary LC VCO design topology, a complimentary series coupled Q-VCO is opted and designed. The schematic of the designed complimentary series coupled Q-VCO is shown in the following Fig. 28.
Here the two complimentary LC VCOs are coupled in series to obtain In-phase and Quad-phase outputs. The generated output pin names are assigned as 0, 90, 180, and 270. Vbias pin is used for controlling the capacitance value of circuit.

N-cap MOSFET capacitors are used in this design because of their large capacitive tuning range compared P-cap. Also N-cap takes less area compared to the P-cap. The capacitance value is tuned by varying control voltage (Vbias). The frequency of oscillation decreases by increasing the Vbias because of the increase in capacitance value with respect to the Vbias.
3.7 Simulation Results

The complementary series coupled Q-VCO has been designed and simulated using CMOS 90 nm technology with voltage supply of 1.2 V. The designed VCO has a frequency tuning range 1.57 GHz, while maintaining low phase noise over the complete range. The following Fig. 29, shows the frequency variation with control voltage.

Fig. 29. Voltage vs Frequency curve for the designed S-QVCO

As shown in Fig. 29, for a Vbias of 0V the circuit oscillates at maximum frequency of 4.62 GHz and for a Vbias of 1.2V the circuit oscillates at minimum frequency of 3.05 GHz.

The following Fig. 30, depicts the phase noise performance of the designed complementary series coupled Q-VCO. For an oscillating frequency of 3.5 GHz the circuit
has a phase noise of -114.1 dBc/Hz at an offset of 1 MHz and -134.9 dBc/Hz at an offset of 10 MHz.

![Graph showing phase noise performance of designed S-QVCO](image)

**Fig. 30. Phase noise performance of designed S-QVCO**

The Figure of Merit (FoM) of the designed S-QVCO is -180.8 dBc/Hz at 1 MHz offset frequency, which is calculated from a widely used [9] Eq. (2.6).

\[
FoM = L\{f_{offset}\} - 20 \log\left(\frac{f_o}{f_{offset}}\right) + 10 \log\left(\frac{P_{DC}}{1\ mW}\right) \quad (2.6)
\]
The performance comparison with other quadrature VCOs (Q-VCOs) is shown in Table 3 below.

<table>
<thead>
<tr>
<th>Ref</th>
<th>Technology</th>
<th>Supply voltage</th>
<th>Output frequency (GHz)</th>
<th>Phase noise (dBc/Hz)</th>
<th>Pdiss (mW)</th>
<th>FoM (dBc/Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>This work</td>
<td>90 nm</td>
<td>1.2 v</td>
<td>3.05-4.62</td>
<td>-114.1 @ 1 MHz</td>
<td>2.6</td>
<td>-180.8</td>
</tr>
<tr>
<td>[22]</td>
<td>180 nm</td>
<td>1.7 v</td>
<td>4.12 -4.89</td>
<td>-115.06</td>
<td>8.6</td>
<td>-180.5</td>
</tr>
<tr>
<td>[23]</td>
<td>90 nm</td>
<td>1.0 v</td>
<td>4.88-5.15</td>
<td>-103</td>
<td>2.8</td>
<td>-173</td>
</tr>
<tr>
<td>[24]</td>
<td>350 nm</td>
<td>3.3 v</td>
<td>900 MHz</td>
<td>-101.4 @ 600KHz</td>
<td>9.8</td>
<td>-155</td>
</tr>
</tbody>
</table>

Table 3. Performance comparison with other Q-VCOs

The final design of the complimentary S-QVCO is also verified for process variation by doing Monte Carlo simulation with random sampling method for 10 points. The following figure Fig. 31, shows the Monte Carlo simulation output results for 0 degrees and 90 degrees for 10 points. The frequency of designed S-QVCO is varied for different process corners. The simulation results verify that the design is not completely robust to process variations. As shown in Fig. 31, the designed S-QVCO generate outputs for only 9 iterations out of 10 iterations and shows good phase accuracy between the in-phase and quadrature phase outputs. The designed DCO has a phase error value less than 2° between the in-phase and quadrature phase outputs.
Fig. 31. Monte Carlo simulation results of the designed S-QVCO with I/Q outputs for 10 points

The final output waveforms of the designed complimentary S-QVCO at 4GHz oscillation frequency is shown in the following Fig. 32. The four outputs of the designed S-QVCO are phase shifted by 90 degrees each.
Fig. 32. Output waveforms of the designed S-QVCO

Here the In-phase and Quadrature Phase outputs are labeled as I+ (0\degree), Q+ (90\degree), I-(180\degree), and Q- (270\degree). The maximum phase error of the designed complimentary S-QVCO is less than 2 degrees over the complete tuning range.

Performance comparison between the designed I/Q DCO and S-QVCO is shown in the following Table 4 below.

<table>
<thead>
<tr>
<th>Ref</th>
<th>Technology</th>
<th>Supply voltage</th>
<th>Output frequency (GHz)</th>
<th>Phase noise (dBc/Hz)</th>
<th>Phase error</th>
<th>Pdiss (mW)</th>
<th>FoM (dBc/Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DCO</td>
<td>90 nm</td>
<td>1.2 v</td>
<td>1.1-8.02</td>
<td>-90.4@1 MHz</td>
<td>&lt; 1.5\degree</td>
<td>5</td>
<td>-156.8</td>
</tr>
<tr>
<td>S-QVCO</td>
<td>90 nm</td>
<td>1.2 v</td>
<td>3.05-4.62</td>
<td>-114.1@1 MHz</td>
<td>&lt; 2\degree</td>
<td>2.6</td>
<td>-180.8</td>
</tr>
</tbody>
</table>

Table 4. Performance comparison between the designed I/Q DCO and S-QVCO
As seen from the Table 4 above, the designed DCO has very wide tuning range and less phase error compared to the S-QVCO. Whereas S-QVCO has better phase noise performance and FoM compared to the designed DCO.

3.8 Summary

A complimentary series coupled Q-VCO design topology is opted for this design due to its low power consumption and, low phase noise performance parameters. The circuit designed generates I/Q phase outputs with large tuning range, low phase noise and, low power dissipation. Therefore the designed S-QVCO can be used for low power and low phase noise oscillator applications.
4. Phase Frequency Detector

Phase frequency detectors (PFDs) are widely used in micro-electronic circuit designs including phase locked loops (PLLs), radars, and interferometers. A PFD is a key sub-circuit to the operation of a PLL. The purpose of a PFD is to compare the two periodic input signals and generate output pulses indicative of the phase and frequency difference of the two periodic input signals [25].

4.1 Types of phase and frequency detectors

Several phase and frequency detectors have been proposed by researchers over the years. Mixers or analog multipliers are used as analog phase detectors, but they are limited due to large size and power. Digital phase and frequency detector circuits have overcome the disadvantages of analog phase detectors and they are widely used. Some of the performance parameters of a PFD are simplicity, power and accuracy. Among the various designs the most commonly used phase detectors that are widely used in PLLs are

- EXOR Phase Detector
- JK flip-flop
- Phase-Frequency detector

An EXOR phase detector is normally a basic EX-OR logic gate. The XOR gate results the phase difference between them only if the duty cycle of the input signals are 50%. Edge triggered JK flip-flop can be used as phase frequency detector based on the principle one to charge, and other to discharge. It is used often, when active charge pump is suggested [26].
Phase frequency detector (PFD) is chosen to be best among all of the above because of its performance and ease of use and design. Conventional PFDs are designed by using D flip-flops with a reset path as feedback loop. The circuit block diagram of a conventional PFD using D flip-flops is shown in the following Fig. 33.

![Fig. 33. Schematic of a conventional PFD](image)

Here it uses two D-Flip-flops and an AND gate to function as PFD. In the Fig. 33 shown above, the D- inputs of both the flip-flops are connected to ‘VDD’. The clock input of both flip-flops are triggered separately using reference and the divider frequency clocks respectively. The output of AND gate is connected CLR pin of the D-flip-flops.
These flip-flops are asynchronous clear flip-flops. Therefore when the output of AND is logic high, it clears the outputs of the flip-flops to logic zero irrespective of clock and data input of the d-flip-flop. The outputs of this PFD are UP and DN.

The maximum possible output states that the PFD can be placed are 4 they are

- $UP = 0, DN = 0$
- $UP = 0, DN = 1$
- $UP = 1, DN = 0$
- $UP = 1, DN = 1$

The state $UP=1$ and $DN=1$ is omitted, as we using an AND gate for clearing the outputs to logic low. Therefore, we left with only 3 states are shown below.

- $UP = 0, DN = 0$  \{state 0\}
- $UP = 1, DN = 0$  \{state 1\}
- $UP = 0, DN = 1$  \{state 2\}

The minimum number of flip-flops required for implanting 3 states is 3. The following Fig. 34, shows the finite state machine of the phase frequency detector by using state transition table. State 0 indicates $UP=0$ $DN=0$, State 1 indicates to $UP=1$ $DN=0$ and State 2 corresponds to $UP=0$ $DN=1$. 


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Fig. 34. FSM of a conventional PFD

The following Figs. 35, 36 and 37 shows the outputs for all the possible states. Fig. 35 shows the output for state 0, Fig. 36 shows the output for state 2 and, Fig. 37 shows the output for state 1.
Fig. 35. When \( f_{\text{REF}} \) and \( f_{\text{DIV}} \) are in Phase

Fig. 36. When \( f_{\text{REF}} \) is lagging \( f_{\text{DIV}} \)
This conventional PFD has the drawbacks of high power consumption, large dead zone, limited operating speed, and undesired output glitches [27]. Improved design topologies manage to reduce dead-zone errors [3] to 15 ps and attempt to simplify design circuitry. Pass transistor-based logic PFD [28] designs try to minimize the number of transistors to improve performance benchmarks, but such designs are subjected to output

Fig. 37. When $f_{\text{REF}}$ is leading $f_{\text{DIV}}$
voltage drops and performance is affected greatly by adding output load capacitance. An alternative flip-flop-based design [29] has been proposed to reduce the dead-zone error to near 750 fs, but it has a drawback of large power consumption and moderate operating frequency due to its circuit complexity and long critical path. The dead zone is defined as the minimum bound of phase error where PFD is unable to detect the difference in input phase and is shown in Fig. 38. Therefore, the dead zone plays an important role in the operation of a PFD since dead-zone errors introduce jitter to PLL devices [30].

In this chapter, a new design topology without any feedback path is presented to improve dead zone of the PFD while simplifying the design to reduce power consumption. The proposed PFD design accepts two input phase differences over the complete range \([0, 2\pi]\). The output glitches are completely removed and this PFD can drive large capacitive loads without affecting its normal operation. Dead-zone error of the PFD design is reduced to almost zero by removing the reset path.

Fig. 38. Characteristics of PFD with dead-zone
4.3 Proposed PFD design architecture

Three stages are used to implement this PFD design [31], as shown in Fig. 38. To avoid the usage of D flip-flops, two narrow pulse generator circuits are used in the proposed PFD to detect rising edges. Stage 1 is used to generate narrow pulses at the rising edges of the two inputs, ‘REF’ and ‘DIV’. In stage 2, tri-state logic-based architecture is used to distinguish the phase and frequency differences of the two input signals. The tri-state logic circuits are controlled by the pulses generated in the first stage. A pull down circuit is implemented in the third stage to make sure the two outputs ‘UP’ and ‘DN’ are not logically high at the same time. Inverters at the end of the third-stage buffer the output signals to achieve a full voltage swing for the outputs of the PFD and to enhance the driving capability. As seen in Fig. 39, neither latches nor D flip-flops is used in this design, and the reset feedback path delay from output to input is removed completely, which helps in obtaining very high resolution and high speed. The detailed operating principles of this proposed PFD design is discussed in the following section.

4.4 Proposed PFD design circuit operation

The full schematic of the proposed PFD design architecture with three stages is shown in Fig. 39. The PFD in Fig. 39, is designed to measure phase difference between rising edges only by using 16 inverters, two NAND gates, and two tri-state-based logic components. On each rising edge, the first stage produces a narrow falling pulse followed by a narrow rising pulse after a delay produced by the three inverters. The timing of these pulses can be seen in Fig. 40. The pulse generator circuitry is implemented by a three inverter delay path and one NAND gate for both ‘REF’ and ‘DIV’ input signals as shown
in Fig. 39. The rising and falling pulse width is determined by the time propagation delay of the inverter path and NAND gate.

Fig. 39. Proposed PFD design
In the second stage of the design, the rising edge of the ‘DIV’ signal is given as an input to the gates of transistors T1 and T4 and used as enable input for the tri-state logic block. The falling pulse of the ‘REF’ signal is fed to transistor T2 and the ‘DIV’ signal is connected to the gate of T3 transistor. When the falling pulse of ‘REF’ pulse is active low, T2 is turned ON and produces an active high output at node ‘X’, if the rising edge of ‘DIV’ signal is already at active low as shown in Fig. 40. A high output at node ‘X’ indicates that the ‘REF’ signal rises ahead of the ‘DIV’ signal. When the rising pulse of ‘DIV’ input signal is high, transistors T3 and T4 are turned ON and the voltage at node ‘X’ is forced to
active low. Similar operation takes place when ‘DIV’ signal rises ahead of ‘REF’ signal. NMOS transistors, T9 and T10 are added to prevent both outputs being high simultaneously.

As seen in Fig. 39, T10 is used to pull node ‘Y’ down when the input signal ‘REF’ leads ‘DIV’ and T9 is used to pull node ‘X’ down when ‘DIV’ leads ‘REF’. The output waveforms for each node and the connections of the proposed design in Fig. 39 are shown in Fig. 40, for the ‘REF’ input signal both leading and lagging behind the ‘DIV’ input signal. The narrow pulses generated by the first stage have a minimum sufficient width such that the logic in the second stage can process the pulses. The pulse width of node ‘X’ which is equivalent to the width of the ‘UP’ signal is logically high from the falling edge of the ‘REF’ input signal to the rising edge of the ‘DIV’ input signal. Similarly, the pulse width of the ‘DN’ signal is logically high from the falling edge of the ‘DIV’ input signal to the rising edge of the ‘REF’ input signal.

The resolution of the design is dependent on the inverter stage delay that produces the rising pulses from the falling pulses. If the delay between the rising and falling is set by a single inverter delay instead of three, the second stage is unable to produce a logical high output if the difference between the input signals of the PFD is too small. Thus, in order to obtain very high resolution and high speed of operation, three-stage inverter delay is necessary. Process variation can affect the propagation delay of the inverters in the PFD, which affect the widths of the rising and falling narrow pulses. These changes affect the output pulse widths of ‘UP’ and ‘DN’ pulse widths. The effects of process variation are discussed in final design performance section.
4.5 Simulation Results

The resulting output waveform of the PFD design is shown in Fig. 41 when the input phase difference is at the edge of the dead zone. When the ‘REF’ input signal leads the ‘DIV’ input signal by 125 fs, the output signal ‘UP’ goes logic high, whereas the ‘DN’ signal remains at logic zero, thereby producing single-ended outputs for the PFD design.

Fig. 41. Output response of proposed PFD for 125 fs input phase difference with ‘REF’ leading ‘DIV’
The output pulse width of the proposed PFD design is measured by varying the phase difference between input signals as shown in Fig. 42. The pulse width increases exponentially for phase differences below 4 ps and exhibits a linear response for input phase differences >4 ps. The PFD output pulse width is 29.54 ps at the edge of the dead zone when the input phase difference is 125 fs.

Fig. 42. Output pulse width against input phase difference for proposed PFD tested with input frequency of 166 MHz
The final design is also verified for process variation by doing Monte Carlo simulation with random sampling method for 20 points with ‘REF’ both leading and lagging ‘DIV’. The simulation results verify that the design is robust to process variations. As shown in Fig. 43, with 125 fs of ‘REF’ lagging ‘DIV’, the ‘DN’ outputs are able to catch all the 20 pulses and ‘UP’ remains logic zero. The ‘UP’ and ‘DN’ pulse widths change by <15% from the nominal value over the 20 iterations that spanned the process corners.

Fig. 43. Monte Carlo simulation results for 20 iterations of proposed PFD
4.6 Summary

The proposed CMOS PFD design accepts the complete range of input phase differences [0, 2π] while avoiding glitches at the outputs. The PFD operates over a frequency range from 10 KHz to 6 GHz with a minimal critical path delay and no reset path architecture. This proposed PFD consumes low power due to its simple design structure, produces single-ended outputs, and has a near-zero dead-zone error. The proposed design can be used for wideband frequency signal detection applications and for implementation in PLLs.
5. Conclusion and Future work

5.1 Conclusion

In this thesis a wide tuning range In-phase and quadrature phase output DCO, a complimentary series coupled Q-VCO, and a simple very high performance phase frequency detector (PFD) are designed in 90 nm CMOS technology with 1.2 V power supply. The contribution to this thesis work is listed below.

- The proposed I/Q output DCO design operates in the frequency range of 1.1-8.2GHz. The designed ring oscillator with digital control inputs attains high oscillation frequencies by applying negative delay inputs to the transistors in parallel to the conventional static CMOS inverter. The stage delay of the ring oscillator with the proposed design is less than the conventional static CMOS inverter and the skewed delay inverter cell. At 2.02GHz oscillation frequency, the measured phase noise is -90.43dBc/Hz at an offset of 1 MHz and -117.64dBc/Hz at an offset of 10MHz and consumed 5 mW of power dissipation.

- Complimentary series coupled Q-VCO structure is opted in this work for low phase noise and wide tuning range. The designed complimentary S-QVCO has a power consumption of 2.6 mW, phase noise value of -114.1 dBc/Hz at 1 MHz offset, and a tuning range of 34%. Therefore the designed S-QVCO can be used for low power and low phase noise oscillator applications.

- The proposed CMOS PFD design accepts the complete range of input phase differences [0, 2π] while avoiding glitches at the outputs. The designed PFD completely removes unwanted output glitches, accepts inputs with a large
difference in frequency, and also has the ability to drive a large capacitive load with minimal impact on performance. The PFD operates over a frequency range from 10 KHz to 6 GHz. Simulation results indicate that the proposed design can operate over a wide range of frequencies from 10 kHz to 6 GHz and can detect phase differences for inputs as small as 125 fs for all frequencies of operation and for all process corners. The simulated power consumption is 75 μW at 166.6 MHz with an input phase difference of 125 fs. The proposed design can be used for wideband frequency signal detection applications and for implementation in PLLs.

5.2 Future Work

Design modifications need to be performed to improve the phase noise performance of quadrature DCO while maintaining low power consumption. The phase noise and phase error of the designed S-QVCO can be further improved to find better applications. Finally, the designed PFD and quadrature output oscillators are need to be placed in a PLL system to verify the overall performance.
6. References


