MODELING AND MINIMIZATION OF
INTEGRATED CIRCUIT PACKAGING PARASITICS AT RADIO FREQUENCIES

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requirements for the degree of
Doctor of Philosophy

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ABSTRACT

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Many integrated circuits are connected to their packaging pins through bondwires. Due to the low cost of bondwires, there is interest in extending operating frequencies or negating their effects in order to keep the price of packaged integrated circuits as low as possible. Bondwires function as lumped circuits consisting of inductors, capacitors, and resistors which can be modeled based on wire geometry. Knowing this, models can be created which approximate the effects of bondwires. With the knowledge of these models, compensation techniques can be implemented which will match the bondwire impedance to the signal line impedance. The effects of these elements on circuit operation is apparent on both signal and power lines to devices.

This dissertation is going to present

1. A bondwire model based on physical characteristics of interconnections including neighboring wires. The model is tested against data from fabricated test fixtures, and results compared to those produced by current software.
2. A compensation method for performance degradation caused by bondwires at radio frequencies. Test fixtures implementing these methods are fabricated and checked with results compared to predictions.
3. A method of component stacking which can be used to attach passive components directly to IC die.
   a. Use above method to improve power distribution network (PDN) performance. Theoretical results are compared to measured test fixture results.
   b. Use above method to improve performance of off device filters through Q-factor improvement. Improvement verified through test and analysis of a physical test fixture.
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1 Introduction and Background

1.1 Introduction

Modern high performance electronic systems generally consist of several packaged integrated circuits mounted on a printed circuit carrier board which serves to interconnect signals and as an interface to the “outside” world. As switching frequencies increase in integrated circuits device packaging parasitics have an increasing effect on the device’s performance. Compensating for or eliminating these parasitic circuit elements is an area of active research and the area in which this project will focus. Of particular interest is the performance of the bondwire which has a lower cost per pin than the competing flip chip attachment technology. Bondwires are conductors used to attach an integrated circuit’s (IC) input output (IO) ring to circuitry outside of the IC. At high frequencies undesired inductances and capacitances are introduced into the operating circuit through the physical geometries of the bondwire. This dissertation investigates several methods of avoiding and compensating for these unwanted elements for various cases of circuit operation.
Several means of bondwire compensation are covered in this dissertation. First, a novel method of modeling the bondwire is introduced in chapter 3. This provides a model of the bondwire to be used in subsequent sections. Next, a novel bondwire compensation network is introduced and analyzed in chapter 4. The final two chapters involve eliminating bondwires from critical circuit IO by directly attaching passive components to a die for power decoupling and RF filtering applications. To provide a sufficient background, each level of interconnection for a system involving packaged ICs will be further discussed in detail.

1.2 Background

1.2.1 Printed Circuit Board

The printed circuit board (PCB) is a set of one or more dielectric and copper layers pressed together to form interconnections between electronic devices. The simplest type of board is a single layer variety with a layer of copper etched onto an insulating layer. Components are either mounted on the surface of the copper which is called surface mount technology (SMT) or the board is drilled and has leaded components mounted through the board in the drilled holes called through hole mounting. SMT is currently the dominant technology as parts are easier to place and smaller than traditional through hole components. Once components are placed they are soldered to the PCB to form an electrical bond with the copper. Multilayer boards are made possible through the use of vias which are drilled holes through the board connecting one or more layers together. Vias must be plated to provide proper conductivity.
As board complexity increases so do the available options and cost. Smaller and more complicated via structures are possible such as blind, which only are visible on one side of the PCB, and buried which are fully embedded into the board and stitch together internal layers. PCBs may be made of a ridged or flexible material with a variety of different characteristics. Controlled impedances are possible on a PCB with using properly designed geometries. Several different types of transmission lines are possible on the surface or internal to a PCB. These complex requirements for PCBs have primarily been driven by advances in integrated circuit technology which require many more interconnections than discrete components. High speed devices both digital and analog can also have signal integrity requirements which involve careful considerations of parasitic elements which can become influential at high frequencies. An example of a simple, multilayer board with multiple structures is shown in Figure 1.2.1.1.

![Example PCB Structures](image)

**Figure 1.2.1.1. Example PCB Structures [1]**
1.2.2 Transistor Technology

The first transistor was invented in the 1947 at Bell Laboratories in Murray-Hill, New Jersey. The team that invented the point contact transistor was Shockley, Bardeen, and Brattain with the team assembled by Jack Kelly [2]. The research was started out of Kelly’s vision of a replacement for vacuum tubes and relays which were slow and unreliable and he believed would limit telephone communications advancements. The team experimented with silicon and germanium primarily and demonstrated the first transistor in December of 1947, two and a half years after beginning work. An image of the device is shown in Figure 1.2.2.1. After the invention of the point contact transistor, Shockley focused his efforts on the formation of p-n junction theory resulting in the junction transistor which would be later chosen over the point contact transistor for commercial development. The junction transistor, later improved and called the bipolar junction transistor (BJT) did not, however come to be the dominant integrated circuit transistor technology. That slot would be filled by the metal oxide semiconductor field effect transistor (MOSFET) which was not the performance leader between the two technologies, but was the smaller of the two [3].
In 1957 Jack Kilby of Texas Instruments developed the first integrated circuit (IC) which consisted of a Texas Instruments mesa transistor, a capacitor, and a resistor all connected with a discrete wire connection. This rudimentary device is shown in Figure 1.2.2.1. Later at Fairchild Semiconductor, a planar process was developed by Hean Hoerni and used by Bob Noyce to create an IC using deposited metal connections [6]. A few years later, in 1965 Gordon Moore, co-founder of Intel predicted an exponential increase in transistor density in his paper *Cramming more components into integrated circuits* [7]. This prediction has continued to generally remain true through today despite obstacles in the path of integration and predictions to the contrary [6]. Figure 1.2.2.2 illustrates this trend of increasing complexity as a simple logarithmic plot of transistor count on a microprocessor versus year as well as key enabling technologies for higher transistor density.
Figure 1.2.2.2. Transistor Densities with Enabling Technologies [8]

Integrated circuits have special handling and assembly requirements and therefore must be packaged before being placed onto a PCB.

1.2.3 Integrated Circuit Packaging

After a die has been fabricated it is placed in a package which is friendly to the assembly of the final product. A number of different packages exist based on various assembly methods and integrated circuit configurations. The basic functions of the package are to provide a mechanical fixture for the IC to inhabit while providing protection from the environment and electrical bonding to the carrier substrate, which is usually a PCB. In the relatively distant past, ceramic flat packages and later DIP (dual inline package) were the package of choice, but as IC complexities increased, so did the requirements for low loss, high IO packages. With the adoption of surface mount technology (SMT) devices, the packages decreased in size – with small outline integrated
circuit (SOIC) and the tighter pitched small outline package (SOP) becoming DIP replacements. Later, quad flat pack (QFP) and quad flat no-lead (QFN) became available which sported higher pin counts and pins around the periphery of a square package allowing for more IO to be run out of the IC. Even more complex packaging includes the ball grid array (BGA) which consists of a die on a multilayer passive substrate with solder balls on the bottom. Examples of these packages are shown in Figure 1.2.3.1. The substrate routes signals from the die to the solder balls which connect to the carrier PCB through a reflow solder process. On the opposite end of the packaging spectrum is the chip scale package (CSP) which may be up to 1.2 times the size of the die [9] and finally the wafer scale package (WSP) which is a wafer that is mounted directly to the carrier via solder balls similar to how a flip chip die may be mounted to a substrate and placed in a BGA package.

![Image of IC Packaging](image)

**Figure 1.2.3.1. IC Packaging [10]**

Direct chip attach (DCA), COB, and WSP are all similar technologies in that the wafer is attached to the board; however the differences are in the electrical connections and assembly methods. DCA and COB involve the device being placed pad up similar to how it is placed in a package. The footprint on the PCB has a number of copper pads surrounding the die which are then wire bonded. Finally, an epoxy is poured over the
device which serves to secure the device and bondwires to the PCB as well as a barrier to the environment. A WSP however is not actually a package, but a die with solder balls on the bottom which is attached to the PCB in a manner similar to a BGA – the reflow process.

In general IC packages have two levels of interconnection – level 1 and level 2. The level 1 interconnect is the interconnection between the chip and the package, in the case of a QFP package, for example this would be the bondwire. The level 2 interconnect is the connection from the package to the PCB. For the QFP example this would be the pins on the QFP package.

1.2.4 Bringing it all Together

When combining the packaged IC and the PCB, there are a number of parasitic factors the IC designer and the PCB designer must take into account for a high performance circuit to behave properly or at all. In Figure 1.2.4.1 below an electrical model of a typical PCB with attached IC in a quad flat pack (QFP) package is shown with parasitic elements identified. From left to right is the chip IO, the wire from the chip to the substrate, the trace in the package, the lead on the package and finally contact with the PCB. Note that there are a number of interacting mutual inductances \( M \), mutual capacitances \( C_M \), as well as self inductances \( L_s \) and resistances \( R \). Before even getting to the board, RF and high speed signals have a number of issues to deal with. The case of a wire bonded chip in a BGA package is shown in Figure 1.2.4.2 which also shows a physical representation of these parasitics.
1.2.5 Measurement and Analysis Theory

Throughout this dissertation, scattering parameters (s-parameters) are used as a method of measuring and quantifying signal performance. S-parameters quantify signal transmissions and reflections in a network consisting of one or more ports. The most common measurements used in this dissertation are $S_{11}$ and $S_{21}$. $S_{11}$ is the measurement of the amount of energy reflected back from an input port while $S_{21}$ is the gain through the network. $S_{11}$ is an indicator of the input return loss of the network, which is a measurement of how well the network’s impedance is matched to the source’s
impedance. A graphical representation of a two port device with its s-parameters indicated is shown in Figure 1.2.5.1.

![Graphical representation of s-parameter measurements.](image)

**Figure 1.2.5.1. Graphical representation of s-parameter measurements.**

A vector network analyzer (VNA) is a device used to measure s-parameters. The VNA operates by sweeping a carrier wave (CW) signal out through one port and measuring the resulting signal through a second port or the generating port. To use a VNA, the device must first be calibrated with known standards. This calibration is performed using the cabling setup the user will use during the test. In this way, the cabling and interconnections from the VNA to the test fixture are included in the calibration. Figure 1.2.5.2 shows the internal components in a VNA and their signal paths.
1.2.6 Test Fixture Fabrication

In this work, physical test fixtures are fabricated in order to verify simulation results. The method of fabrication used is PCB milling. PCB milling is a subtractive process which uses a milling head with controllable X, Y, and Z axis to remove copper from a copper clad substrate. The general steps of the milling process are shown in Figure 1.2.6.1 as well as the resulting test fixture. Test fixtures are hand assembled and soldered using traditional solder techniques. The artwork for the milling machine is created using Agilent ADS to produce Gerber photoplots which are interpreted by the milling machine software to create the instructions for the PCB mill.
Figure 1.2.6.1. PCB Milling process. Bare board (a) is run through the mill (b) and the test fixture (c) is created by soldering the resulting PCB.

1.3 Chapter Summary

This chapter contains the background information necessary for someone familiar to the field to understand this work. This included an overview of PCB, IC, and IC packaging technology. Also introduced were s-parameters as well as the fabrication process that is used throughout this work to create test fixtures. The next chapter outlines the objectives of this project.
2 Organization & Objectives

2.1 Organization of Dissertation

This dissertation is organized into a number of chapters. The first chapter is the introduction. The second chapter is this outline of the dissertation’s organization as well as a listing of its objectives. The third chapter covers the bondwire model developed over the course of the research. This model and its values are used in subsequent sections. Chapter four details a new impedance matching circuit which improves bondwire performance. Chapter five details a method to eliminate the bondwire by directly attaching decoupling capacitors to an IC die. This is shown to improve performance of a system’s power distribution network (PDN). The sixth chapter again directly attaches passive components to an IC, however this is used to increase passive filter performance. Chapter seven is an outline of the contributions of this work as well as a listing of development that can be done in the future. Chapter eight is an appendix containing a listing of the MATLAB code developed during the course of this project.
2.2 Objectives of Dissertation

2.2.1 Bondwire Modeling

The first objective of this dissertation is to create a new bondwire model based on the physical characteristics of the wires, including:

- Develop lumped element model for bondwires of various shapes and configurations
  - Curved wires
  - Wires with angles to ground plane
  - Arbitrary number of wires
  - Wires at angles to each other
- Model implementable in standard circuit simulators
- Test model against physical test fixture and leading simulation software
- Use test results to verify model performance
- Create a model that is not a black box
  - Makes compensation for the wire possible in objective 2

2.2.2 Bondwire Compensation

The second objective is to develop a compensation method for performance degradation caused by bondwires through the use of impedance matching techniques, specifically:

- Develop a compensation method for performance degradation caused by bondwires at RF through the use of impedance matching techniques
• The method presented is adjustable post fabrication
• Test compensation on physical test fixture and leading simulation software
• Demonstrate performance improvement at RF

2.2.3 Power Distribution Network Improvement

The third objective is a new method of component stacking which can be used to attach capacitors directly to IC die improving distribution network (PDN) performance. Parts of this objective include:

• Develop PDN improvement method useful for improving PDN noise in the 1-100 MHz frequency range through passive capacitor stacking
• Test improvement with physical test fixture and software models
• Demonstrate improvement with test results

2.2.4 Filter Improvement

The fourth objective uses the passive attach method to enhance performance of filters through Q-factor improvement. Each portion of the objective will be met as follows:

• Develop a method of inductor attachment which allows for a high Q-factor inductor to be attached directly to a die, circumventing bondwires and avoiding the use of low-Q integrated inductors
• Method eliminates the need for complicated structures, exotic materials, or interconnecting bondwires to improve inductor performance
• Test improvement with physical test fixture and software models
• Demonstrate improvement with test results
3 Bondwire Modeling

3.1 Motivation

Much work in modeling the effects of packaging has taken place the RF domain. Bond wires have been included in the design, modeling, and fabrication of an LNA operating at up to 9GHz [14]. Studies into the effects of the board bond process into silicon have been carried out to varying success [15].

Parasitic modeling at the package level has been an active area of interest as well. Some research has been done extracting models of bond wires in QFN packages [16] as well as with QFP [11] and BGA packages [17]. A 40Gb/s BGA package has been constructed, verified, and compared to a non-optimized package [12]. The authors of the BGA study used bondwires but carefully placed signal return paths, selected high performance dielectric for the substrate, and properly modeled bondwire geometry which all contributed to success.

Some more recent work on reducing package parasitics appears in literature regarding WSPs. Some effort has been put into studies which minimize effects of packaging in the WSP. One of the advantages of WSP is the ability to embed passives such as inductors and antennas into the WSP which are traditionally difficult to fabricate on integrated
circuit die in any technology due to the inherent size requirements [18]. A properly designed substrate has also been demonstrated to be able to minimize crosstalk in the chip by providing isolation [18].

3.2 Bondwire Model

Bondwires are regularly used to attach integrated circuit (IC) electrical signals with off die destinations. A typical bondwire array is a set of round conductors adjacent to each other conducting signals or power between a die and its carrier. Due to fanout limitations, these conductors may not be perfect parallel structures with constant height which can complicate predicting their impact on a circuit with one size fits all equations. As a demonstration of this non-uniformity a cutaway view of an IC die in a quad flat no lead (QFN) package is shown in Figure 1.2.4.2.

In addition to being part of a package interconnect, bondwires can also be used as part of device circuitry. Devices such as transformers [19], active baluns [20], and clock sources [21] have been proposed using bondwires. These circuit implementations also highlight the need for accurate bondwire models.

Given that bondwires are used as part of circuits and interconnects, modeling and simulation of bondwire effects on performance is an important part of designing high frequency integrated circuits. If an IC uses bondwires as part of the package, the bondwire can affect the circuit operation. Modeling the full interconnection allows the designer to offset the effects of the bondwires, predict final circuit operation, and find optimal wire geometries which will have the smallest impact on circuit operation. As
bondwires provide a low cost package bonding solution when compared to flip chip [22]. There is interest in pushing bondwires to ever higher frequencies [12]. To do this, accurate models are needed. Finite-difference time-domain (FDTD) [23], physics based [24], and electromagnetic (EM) [25] modeling are filling the need. These approaches in [23] [24] [25] rely on advanced software or a full EM simulator, whereas the presented algorithm in this chapter can be run using any scripting language and implemented with a SPICE simulator. The technique in this dissertation takes traditional inductance and capacitance equations and applies them to a selectable number of small slices of the wire set which is uniquely modeled in order to approximate complex geometry. The results are then applied as lumped elements in a circuit simulator. Being a lumped model, this work’s method can be inserted a schematic and used with the simulation of the IC being designed. Two examples are provided in this work: a circular bondwire, and polygonal bondwire. The use of arbitrarily small slices facilitates more accurate modeling of realistic bondwire geometries compared to bondwire models in software packages such as Agilent ADS.

![Figure 2.2.4.1. Bondwire 3-dimensional view in QFN package (top removed).](image)
3.3 Bondwire Theory

Bondwire interconnects can be modeled using traditional wire inductor techniques. In order to properly model the wires several parasitic elements must be identified, which include: self inductance, $L$; mutual inductance, $L_m$; self capacitance, $C$; mutual capacitance, $C_m$; input output pad capacitance, $C_{io}$; and resistance, $R$. Self inductance is the inductance of the wire itself, whereas mutual inductance is the inductance between adjacent wires. Self capacitance is the capacitance between the wire and ground plane, while mutual capacitance is the capacitance between two wires. $C_{io}$ is the capacitance created by the IO pads of the die and its carrier where the bondwires are connected. Resistance is simply the resistance of the wire which is affected by the skin depth of the wire. Skin depth is the depth that current is carried in wires which becomes more shallow as frequency increases. In the following sections these six element values will be calculated and the full model will be presented, but first a discussion of known ignored effects will be presented as well as an explanation for their omission.

3.3.1 Neglected Effects

One electrical effect present but negligible at the scales of bondwires is current crowding. Current crowding is the tendency for currents in a conductor to have an increased density near a bend or neck down, and is more prevalent around acute wire bends. The skin effect takes into account some of the resistance influenced by current crowding. In order to check the effects of corner crowding, a model was generated in ADS and simulated with the Momentum Microwave field solver. The physical representation of the model is shown in Figure 3.3.1.1. In the model, three bondwires
with a radius of 37.5 μm and length of 3.14 mm were used. One wire was flat, one had an edge 500 μm in height along its line, and the third had an edge 1 mm in height along its line. All were suspended 5 cm above the ground substrate to minimize the effect of the wire height differences due to the added angle. Simulation results show that even at the angle of 90 degrees, the effects of the current crowding are less than 0.5 dB. Results are shown in Figure 3.3.1.2.

![Image](image1.png)

*Figure 3.3.1.1. Three bondwires used to simulated current crowding.*

![Image](image2.png)

*Figure 3.3.1.2. Current crowding effect on bondwire modeling.*
The second minimal effect is contact resistance, which is the resistance between the bondwire and its IO pad. The wire attachment method discussed in this dissertation is a tin-lead solder method with a resistivity of approximately $1.5 \times 10^{-7} \, \Omega \cdot m$. Given the spacing between the copper bondwire with a radius of $37.5 \, \mu m$ of and the IO pad is less than $100 \, \mu m$, the contact resistance is no greater than $3.4 \, m\Omega$. To test the assumption the additional resistance is negligible, a simulation was put together with three circuits: a transmission line of $4 \, cm$, a transmission line of $4 \, cm$ bisected with a $3.4 \, m\Omega$ resistor, and a transmission line of $4 \, cm$ bisected by a $10 \, m\Omega$ resistor. All cases showed near identical performance in the simulation results, which are given in Figure 3.3.1.3.

![Figure 3.3.1.3. Effects of small resistances on a transmission line.](image)

### 3.3.2 Bondwire Model Values

Bondwire models are based on the following physical measurements as shown in Figure 3.3.2.1: separation distance, $d$; wire radius, $r$; wire length, $l$; separation angle, $\alpha$; and height above ground plane, $h$. 

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3.3.3 Value Derivation

The starting point of the new bondwire models are classic inductance and capacitance equations [26] [27] [28].

The self inductance for straight wire is defined as
where $\mu_0$ is the permeability in a vacuum ($4\pi \times 10^{-7}$ H/m), $h$ is the height above the substrate, $r$ is the wire radius, and $\mu_r$ is the relative permeability (dimensionless).

The mutual inductance for straight wire pair is defined as

$$L_m = \frac{l\mu_r\mu_0}{4\pi} \ln\left(1 + \left(\frac{2h}{d}\right)^2\right)$$  \hspace{1cm} (3.3-2)

where $d$ is the distance between wires.

The mutual capacitance for a straight wire pair over ground is

$$C_m = \frac{l\pi\varepsilon_0\varepsilon_{r(\text{eff})} \ln\left[1 + \left(\frac{2h}{d}\right)^2\right]}{\ln\left(\frac{2h}{r}\right)^2}$$  \hspace{1cm} (3.3-3)

where $\varepsilon_0$ is the permittivity of free space ($10^{-9}/36\pi$ [F/m]) and $\varepsilon_{r(\text{eff})}$ is the relative dielectric constant of the dielectric material.

The self capacitance for a straight wire over a ground is expressed as
Equations (5-7) remain constant through the geometry calculations but are necessary to complete the model.

The skin depth of a round inductor is defined as

\[ \delta = \frac{1}{\sqrt{\pi \sigma f \mu_0}} \]  

(3.3-5)

where \( \sigma \) is the conductivity of the wire used and \( f \) is the frequency of the signal.

The resistance of the wire for both cases including skin effect is

\[ R = \frac{4l}{\pi \sigma (2r)^2} \left[ 0.25 \frac{d}{\delta} + .2654 \right]. \]  

(3.3-6)

The capacitance of the pads connecting the bondwires to the fixture is

\[ C_{io} = \varepsilon_0 \varepsilon_{r(\text{eff})} A/t \]  

(3.3-7)

where \( A \) is the IO pad area overlapping the ground plane and \( t \) is the dielectric thickness.
The new solutions for the bondwire parameters for each wire involve sectioning the bondwire into $n$ discrete parts and solving $(3.3-1)-(3.3-4)$ for each part. The values are summed to create the new bondwire values which reflect the wire geometry. Figure 3.3.3.1 shows a graphical representation of this slicing for a particular step on a semicircular shaped wire. The left side shows the angle $\rho$ between a slice and the dielectric. This angle is the same as the angle between the slice and the ground plane. The length of a slice, $l'$ and height of a slice, $h'$ for 10 slices on a side is also shown. As an example of a finer model, the right side of Figure 3.3.3.1 shows the same for 100 slices on a side, resulting in 200 total for the semicircle. A small slice size (large $n$) leads to a more accurate result as it will better track the actual wire geometry. The space between the bondwires and the ground plane is a dielectric layer with a thickness of $t$.

![Diagram of sliced semi-circular bondwire](image)

*Figure 3.3.3.1. Approximation of sliced semi-circular bondwire.*
The slice size of the wire is

\[ l' = \frac{l}{n} \]  \hspace{1cm} (3.3-8)

where \( l \) is the wire length and \( n \) is the number of slices desired.

Each wire is assumed to be a perfect semi-circle with a radius of \( h \) (the height above the dielectric). Each slice of the bondwire has a height of \( h' \)

\[ h' = |\sin(\rho)|h + t. \]  \hspace{1cm} (3.3-9)

Inductance calculations requiring permeability \( (\mu) \) and capacitance calculations requiring permittivity \( (\varepsilon) \) will be affected by the ratio of the relative height of the two dielectrics involved in the model. The first dielectric above the ground plane is the substrate dielectric and above that the second dielectric, air. Air envelopes the bondwires.

The ratio for relative permeability is

\[ \mu'_r = \mu_1 \left( \frac{h_1}{h_2} \right) + \mu_2 \left( 1 - \frac{h_1}{h_2} \right) \]  \hspace{1cm} (3.3-10)

where \( \mu_1 \) is the permeability of the dielectric material immediately above the ground plane and \( \mu_2 \) is the permeability of the second material. \( h_1 \) is the height of the dielectric immediately above the ground plane; \( h_2 \) is the height of the second material.
The ratio for effective permittivity is

\[ \varepsilon'_{\text{eff}} = \varepsilon_1 \left( \frac{h_1}{h_2} \right) + \varepsilon_2 \left( 1 - \frac{h_1}{h_2} \right). \]  

(3.3-11)

In most cases, the permittivity of a dielectric material will be 1 or very close to 1.

By using the height of the semicircle, \( h \) the actual circumference of the circle is not directly used as the semi-circle is composed of \( \pi \) radians. In this numerical solution, each step increases \( \rho \) by the slice size (\( \Delta \)) which drives the solution and sums the wire length which is half of the circle’s circumference. Note that \( n \) cannot result in a slice size smaller than the diameter of the wire.

The increment of \( \rho \) for each slice of the wire is

\[ \Delta = \frac{\pi}{n} \]  

(3.3-12)

Each adjacent wire is at an angle, \( \alpha \) to the other wires which affects the separation distance of that slice. For straight wires, \( \alpha = \pi \) and \( d' \) is \( d \). Adjacent wire slices are

separated by

\[ d' = \rho \times 10^{-3} \tan \alpha + d. \]  

(3.3-13)
Now that the parameters for each slice have been defined, substitute these values to (3.3-1)-(3.3-4) to create the parameters for each bondwire.

Applying substitutions to (3.3-1) yields an inductance of

\[
L = \frac{l' \mu' \mu_0}{2\pi} \ln \left(\frac{2h'}{r}\right). \tag{3.3-14}
\]

Applying substitutions to (3.3-2) yields a mutual inductance of

\[
L_m = \frac{l' \mu' \mu_0}{4\pi} \ln \left(1 + \left[\frac{2h'}{d'}\right]^2\right). \tag{3.3-15}
\]

Applying substitutions to (3.3-3) yields a mutual capacitance of

\[
C_m = \frac{l' \pi \varepsilon_0 \varepsilon_r(\text{eff}) \ln \left[1 + \left(\frac{2h'}{d'}\right)^2\right]}{\ln \left(\frac{2h'}{r}\right)^2}. \tag{3.3-16}
\]

Applying substitutions to (3.3-4) yields a capacitance of

\[
C = \frac{l' 2\pi \varepsilon_0 \varepsilon_r(\text{eff})}{\ln \left(\frac{2h'}{r}\right)}. \tag{3.3-17}
\]
The number of slices is limited by (3.3-14) as $2h'$ must be greater than $r$ for a valid solution. For the most accurate solution $n$ should be maximized according to the limitation presented in (3.3-14). Therefore, restrict $r$ as follows

$$2 \sin \left( \frac{\pi}{n} \right) h > r.$$  
(3.3-18)

which produces the inequality

$$n > \frac{\pi}{\sin^{-1} \left( \frac{r}{2h} \right)}.$$  
(3.3-19)

The next step in creating the model is to apply these equations to find the component values for the model.

### 3.4 Applying the Numerical Solution

#### 3.4.1 Algorithm

Equations (3.3-5)-(3.3-19) can be combined with bondwire physical parameters to create the model. The physical values used in this dissertation are given in Table 3.4.1. These values represent a theoretical bondwire from a chip to a substrate such as in a ball grid array (BGA) package. $L$, $L_m$, $C$, and $C_m$ are found by looping $\rho$ from $\Delta$ to $\Delta - \pi$ in increments of $\Delta$. In each loop iteration, first $d'$ and $h'$ are found then $h'$ is used to update
the permeability for inductance values and permittivity for capacitance values; finally the
value is summed for each loop iteration starting with an initial value of 0 and all
substitutions included. Figure 3.4.1.1 shows the algorithm flow chart for a single
bondwire parameter.

Table 3.4.1. Bondwire parameter calculation values.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$l$</td>
<td>3.14 mm</td>
<td>Length of bond wire</td>
</tr>
<tr>
<td>$\sigma$</td>
<td>5.8x10$^7$ S/m</td>
<td>Bondwire conductivity</td>
</tr>
<tr>
<td>$r$</td>
<td>37.5 μm</td>
<td>Radius of bond wire</td>
</tr>
<tr>
<td>$d$</td>
<td>1.52 mm</td>
<td>Distance of wire separation</td>
</tr>
<tr>
<td>$\alpha$</td>
<td>10 degrees</td>
<td>Separation angle of wires</td>
</tr>
<tr>
<td>$h$</td>
<td>1.57 mm</td>
<td>Wire height</td>
</tr>
<tr>
<td>$A$</td>
<td>.25 mm$^2$</td>
<td>IO pad area</td>
</tr>
<tr>
<td>$t$</td>
<td>508 μm</td>
<td>Dielectric thickness</td>
</tr>
<tr>
<td>$\varepsilon$</td>
<td>3.48</td>
<td>Dielectric constant of dielectric</td>
</tr>
<tr>
<td>$\mu$</td>
<td>1</td>
<td>Dielectric material permeability</td>
</tr>
<tr>
<td>$f$</td>
<td>Swept 1-10GHz</td>
<td>Test frequency</td>
</tr>
<tr>
<td>$n$</td>
<td>22</td>
<td>Number of slices used in algorithm</td>
</tr>
</tbody>
</table>

Figure 3.4.1.1. Algorithm flow chart.

3.4.2 Algorithm Results

The values given in Table 3.4.1 combined with the algorithm from the previous
section result in the bondwire parameters given in Table 3.4.2. The values in Table 3.4.2
show that the bondwire itself has a significant inductance and that the mutual capacitance between wires decreases with distance. Since the resistance of the wire is based on the skin effect, it varies with frequency. These values are then used to create circuit model.

The schematic representation of the model is given in Figure 3.4.2.1. In Figure 3.4.2.1 $L_1$-$L_3$ are the three bondwire inductances obtained from (3.3-14), while $L_{m1}$ and $L_{m2}$ are the mutual inductances from (3.3-15). $C_{s1}$-$C_{s3}$ are the three self capacitances of the bondwires from (3.3-16). $C_{m1}$ and $C_{m2}$ are the mutual capacitances between the signal wire and its neighbors from (3.3-17), and $C_{io1}$-$C_{io6}$ are the IO pad capacitances from (3.3-7). $L_{m3}$ is the inductance between wire1 and wire3 while $C_{m3}$ is the capacitance between wire1 and wire3; these values are omitted in this test as the outside wires are grounded in the test fixture to limit measurements to a two port network.

Figure 3.4.2.1. Final schematic for three bondwire model.
Table 3.4.2. Bondwire model values.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Calculated Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_{self}$</td>
<td>2.87 nH</td>
<td>Bond wire inductance</td>
</tr>
<tr>
<td>$r$</td>
<td>Varies with $f$</td>
<td>Bond wire resistance</td>
</tr>
<tr>
<td>$L_{m0}$</td>
<td>0.522 nH</td>
<td>Mutual inductance to first neighbor (symmetrical)</td>
</tr>
<tr>
<td>$L_{m1}$</td>
<td>0.314 nH</td>
<td>Mutual inductance to next neighbor (symmetrical; 5 wire model only)</td>
</tr>
<tr>
<td>$C_{self}$</td>
<td>101 fF</td>
<td>Bond wire capacitance</td>
</tr>
<tr>
<td>$C_{m0}$</td>
<td>11 fF</td>
<td>Mutual capacitance to first neighbor (symmetrical)</td>
</tr>
<tr>
<td>$C_{m1}$</td>
<td>5.81 fF</td>
<td>Mutual capacitance to next neighbor (symmetrical; 5 wire model only)</td>
</tr>
<tr>
<td>$C_{io}$</td>
<td>17.4 fF</td>
<td>IO pad capacitance</td>
</tr>
</tbody>
</table>

The progression of this algorithm for the self inductance value of the bondwire is shown in Figure 3.4.2.2. The Y-axis represents inductance while the X-axis represents the angle of the wire being computed ($\rho$). This angle determines the height of the wire. Four series are plotted. $L_{cum}$ is the cumulative inductance of the wire while $L_{ind}$ is the inductance of the individual wire slices. The $L_{m0}$ and $L_{m1}$ are the cumulative and individual values for the mutual inductance respectively. It can be seen in Figure 3.4.2.2 that the largest increases happen at the max height above the ground plane, $\rho = \pi/2 = 1.57$. 

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3.5 Bondwire Testing

3.5.1 Test Setup

A bondwire test fixture was created to test the models in a physical environment. The fixture was designed in Agilent ADS and then milled using a PCB milling machine on a 2-layer piece of Rogers 4350B low loss dielectric material. The test fixture has four test circuits: two three wire and two five wire circuits. The center wire is the signal wire and the other wires are attached to ground. The signal wire is attached to SMA.
connectors via a 50 Ω microstrip line. The final test fixture which measures approximately 46 mm x 20 mm is shown in Figure 3.5.1.1.

Figure 3.5.1.1. Test fixture with three and five wire assemblies.

3.5.2 Experimental Results

S-parameter measurements were run with each 3 and 5 wire test fixture connected to an Agilent E8362B VNA and a 10GHz frequency sweep was taken. The test fixture attached to the VNA is shown in Figure 3.5.2.1. The results of the two test fixtures were averaged together to create the final test fixture measurement values. The same averaging was done for the two five wire test fixtures. For comparison to the proposed numerical
model, two other widely used models are used to obtain results for the same three and five wire test fixtures. An Agilent ADS 2011.01 bondwire model using the software’s PBOND (Philips-TU Delft) component is used as a reference benchmark. The PBOND model has a maximum of six geometric points for creating an approximate semi-circle bondwire. This reference model is based on Neumann’s inductance equations and partial inductance [29]. A second benchmark model is from the ADS 2011.01 Momentum 3D field solver. The solver’s physical model for the 5 wire fixture is given in Figure 3.5.2.2.

![Figure 3.5.2.1. Test fixture attached to VNA.](image)

Figure 3.5.2.1. Test fixture attached to VNA.

Figure 3.5.2.3 shows the s-parameter plots for the three wire network. $S_{11}$ represents the energy reflected back into the input port from the network. As expected, at lower frequencies the return loss is lower. $S_{21}$ is the attenuation the network suffers at each frequency. Measurements for the three wire network can be seen in Figure 3.5.2.3 in
solid green. For each measurement the numerical model (pink dash) better tracks the measurement than either the PBOND (double dash blue) or Momentum (solid orange) model.

Plots in Figure 3.5.2.4 are s-parameters for the five wire network. For the $S_{11}$ measurement the numerical model has a higher estimate which tracks the result very well. Both the PBOND and Momentum models appear lower than the measurement. For the $S_{21}$ case, the numerical model better agrees with the measurements as it has a lower loss than either the PBOND or Momentum models.

Results were analyzed and compared using mean absolute error (MAE) and root mean squared error (RMSE). Table 3.5.1 and Table 3.5.2 have the MAE and RMSE results for the three and five wire test fixtures, respectively. MAE was computed by averaging the absolute value of the delta between the measured results and predicted results for each point. The RMSE was computed by squaring the difference between the measured points for that frequency. These were then averaged to obtain the mean square error (MSE) which was square rooted to produce the RMSE for that series. For all cases, the proposed model has a lower error computation than either of the benchmarks as shown in Table 3.5.1 and Table 3.5.2.
Table 3.5.1. MAE test fixture measurements.

<table>
<thead>
<tr>
<th>Fixture Type</th>
<th>ADS PBOND</th>
<th>Numerical Model</th>
<th>ADS Momentum</th>
<th>Parameter</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Three wire</td>
<td>1.053</td>
<td>0.546</td>
<td>1.299</td>
<td>S(1,1)</td>
<td>dB</td>
</tr>
<tr>
<td>Three wire</td>
<td>0.989</td>
<td>0.681</td>
<td>1.130</td>
<td>S(2,1)</td>
<td>dB</td>
</tr>
<tr>
<td>Five wire</td>
<td>0.657</td>
<td>0.538</td>
<td>1.097</td>
<td>S(1,1)</td>
<td>dB</td>
</tr>
<tr>
<td>Five wire</td>
<td>0.770</td>
<td>0.643</td>
<td>0.856</td>
<td>S(2,1)</td>
<td>dB</td>
</tr>
</tbody>
</table>

Table 3.5.2. RMSE test fixture measurements.

<table>
<thead>
<tr>
<th>Fixture Type</th>
<th>ADS PBOND</th>
<th>Numerical Model</th>
<th>ADS Momentum</th>
<th>Parameter</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Three wire</td>
<td>1.214</td>
<td>0.709</td>
<td>1.328</td>
<td>S(1,1)</td>
<td>dB</td>
</tr>
<tr>
<td>Three wire</td>
<td>1.328</td>
<td>0.962</td>
<td>1.572</td>
<td>S(2,1)</td>
<td>dB</td>
</tr>
<tr>
<td>Five wire</td>
<td>0.832</td>
<td>0.633</td>
<td>1.391</td>
<td>S(1,1)</td>
<td>dB</td>
</tr>
<tr>
<td>Five wire</td>
<td>1.064</td>
<td>0.871</td>
<td>1.213</td>
<td>S(2,1)</td>
<td>dB</td>
</tr>
</tbody>
</table>

Figure 3.5.2.2. ADS Momentum five wire model.
Figure 3.5.2.3. S-parameters for three wire networks (a) $S(1,1)$ and (b) $S(2,1)$. 
Figure 3.5.2.4. S-parameters for five wire networks (a) $S(1,1)$ and (b) $S(2,1)$.

Plots of relative errors between the fixture simulations and measurements are shown in Figure 3.5.2.5(a), (b) and Figure 3.5.2.6(a), (b). A perfect match would be a
horizontal line across 1 on the Y-axis. As the proposed model has lower error counts than the two benchmarks the proposed model tends to be more centered around the horizontal ‘1’ when compared with the other models as shown in Figure 3.5.2.5 (a).

![Figure 3.5.2.5. Three wire relative error for (a) S(1,1) and (b) S(2,1).](image)
These results show that the proposed model slicing solutions produce a result that is valid and agrees with measurements. In the next section, a second model will be produced using the numerical method and tested against ADS bondwire models.

Figure 3.5.2.6. Five wire relative error for (a) S(1,1) and (b) S(2,1).
3.6 Further Geometries

3.6.1 ADS BONDW Parameterized Shape

ADS includes several bondwire shape models which can be used in circuit simulations. One of these is the BONDW shape [29] which is shown in Figure 3.6.1.1. It can be seen this shape is comprised of two triangles and a straight inductor. Knowing these geometries, useful equations can be developed and the slicing method of wire modeling applied. The parameters for each triangle can be found and summed together with the straight wire to produce an accurate representation of a bondwire network.

![Figure 3.6.1.1. ADS BONDW bondwire shape [29].](image)

3.6.2 BONDW Shape Equations

The BONDW shape is comprised of two fundamental elements: a straight wire and triangle. The straight wire equations are already defined in (3.3-1)-(3.3-4). The triangular equations require the use of the slicing method used in section 3.4 which will be applied to each of the two triangles separately. The broken down shape is given in Figure 3.6.2.1.
Instead of walking along the unit circle as was the case for circular wires, for the triangles, the algorithm walks along the triangles’ hypotenuse whose length, *hyp* can be found with the Pythagorean theorem. The position on the hypotenuse will be called *ρ*, and the angle of the triangle relative to the ground plane is *θ*. As a reference, a triangle with *n*=10 is shown in Figure 3.6.2.2.

**Figure 3.6.2.1. BONDW shape with elementary elements highlighted.**
The slice size, $l'$, can be found by

$$l' = \frac{h_{\text{yp}}}{n}$$  \hspace{1cm} (3.6-1)

where $n$ is the number of slices.

The height of each slice

$$h'' = \sin \theta \left( \rho - \frac{l'}{2} \right).$$  \hspace{1cm} (3.6-2)

The overall height of each slice is

$$h' = h'' + t.$$  \hspace{1cm} (3.6-3)

The number of slices should be restricted such that

$$h'' > 2r$$  \hspace{1cm} (3.6-4)

or
\[ h'' > \sin \theta \left( \rho - 2 \frac{h_{yp}}{n} \right). \quad (3.6-5) \]

For the angular wires, the distance of wire separation is

\[ d' = \rho \tan(\alpha) + d \quad (3.6-6) \]

Where \( d \) is the separation between adjacent wire segments.

To realize the final equations for the angled wires, use eq. (3.3-14)-(3.3-17) with
(3.6-1)-(3.6-6). The modified algorithm for the triangular wire sequence is shown in Figure 3.6.2.3.

**Figure 3.6.2.3. Bondwire computation algorithm for wires at an angle to ground.**

After finding the parameter value of each segment type, the values are summed to create the mode for the whole wire network. The model used is the same as Figure 3.4.2.1.

### 3.6.3 BONDW Shape Bondwire Calculations

Bondwire shape parameters are given in Table 3.6.1. A pictorial representation of the measurements can be found in Figure 3.6.1.1.
Table 3.6.1. Bondwire Shape Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$r$</td>
<td>31.8 μm</td>
<td>Bondwire radius</td>
</tr>
<tr>
<td>Gap</td>
<td>1000 μm</td>
<td>Linear distance covered by wire</td>
</tr>
<tr>
<td>StartH</td>
<td>508 μm</td>
<td>Height of wire attach first point</td>
</tr>
<tr>
<td>MaxH</td>
<td>1508 μm</td>
<td>Max height of wire</td>
</tr>
<tr>
<td>Tilt</td>
<td>200 μm</td>
<td>Base of first triangular segment</td>
</tr>
<tr>
<td>Stretch</td>
<td>200 μm</td>
<td>Length of parallel segment</td>
</tr>
<tr>
<td>StopH</td>
<td>508 μm</td>
<td>Height of wire attach second point</td>
</tr>
<tr>
<td>FlipX</td>
<td>1</td>
<td>X geometry not flipped</td>
</tr>
<tr>
<td>$\alpha$</td>
<td>15°</td>
<td>Separation angle of wires</td>
</tr>
<tr>
<td>$d$</td>
<td>200 μm</td>
<td>Distance of wire separation</td>
</tr>
<tr>
<td>$t$</td>
<td>508 μm</td>
<td>Dielectric thickness</td>
</tr>
<tr>
<td>$\varepsilon$</td>
<td>3.48</td>
<td>Dielectric constant of dielectric</td>
</tr>
<tr>
<td>$\mu$</td>
<td>1</td>
<td>Dielectric material permeability</td>
</tr>
<tr>
<td>$f$</td>
<td>Swept 1-10GHz</td>
<td>Test frequency</td>
</tr>
<tr>
<td>$n$</td>
<td>14</td>
<td>Number of slices per angled wire</td>
</tr>
</tbody>
</table>

After running the algorithm, the resulting parameters were used with Agilent ADS to generate s-parameter data. The parameter data is shown in Table 3.6.2; the s-parameter results are given in Figure 3.6.3.2. The ADS 3D model for use in Momentum is displayed in Figure 3.6.3.1. Note that in the 3D model, the initial spacing between bondwires is 200 μm.

S-parameter results shown in Figure 3.6.3.2 show a close correlation between the BONDW shape model, which uses the PBOND equations, the numerical model presented in this dissertation, and the Momentum field solver model. The numerical model correlates closer to the Momentum results than the PBOND based model.
Table 3.6.2. Bondwire Model Values

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Calculated Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_{self}$</td>
<td>1.98 nH</td>
<td>Bond wire inductance</td>
</tr>
<tr>
<td>$r$</td>
<td>Varies with $f$</td>
<td>Bond wire resistance</td>
</tr>
<tr>
<td>$L_{m0}$</td>
<td>.86 nH</td>
<td>Mutual inductance to first neighbor</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(symmetrical)</td>
</tr>
<tr>
<td>$C_{self}$</td>
<td>90 fF</td>
<td>Bond wire capacitance</td>
</tr>
<tr>
<td>$C_{m0}$</td>
<td>40 fF</td>
<td>Mutual capacitance to first neighbor</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(symmetrical)</td>
</tr>
</tbody>
</table>

Figure 3.6.3.1. ADS 3-dimensional model of the BONDW test.
Figure 3.6.3.2. S-Parameter plots with numerical and ADS models.
3.7 Design Example

A significant advantage of the proposed bondwire model is the ability to insert the model into an RF circuit to facilitate the extraction of a simulation netlist that includes the bondwire model parameters. A previously designed on chip CMOS RF amplifier for driving off chip 50 Ω loads is used to illustrate the use of the bondwire model. The amplifier was designed with a 90 nm CMOS process and Cadence ADE is used to simulate the performance. The on chip amplifier is coupled to an off chip 50 Ω load (measurement instrument or signal chain device) with a single bondwire as shown in Figure 3.6.3.1(a). Figure 3.6.3.1(b) shows the case for no bondwire. Table 3.7.1 gives the bondwire parameters used for the evaluation. Two wire lengths are used: 1 mm and 0.5 mm.

Figure 3.6.3.1. Power amplifier test diagram (a) with bondwires and (b) without bondwires.
Table 3.7.1. Bondwire Parameter Values.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>(l)</td>
<td>1 mm, 0.5 mm</td>
<td>Length of each bondwire</td>
</tr>
<tr>
<td>(\sigma)</td>
<td>5.8x10^7 S/m</td>
<td>Bondwire conductivity</td>
</tr>
<tr>
<td>(r)</td>
<td>37.5 (\mu)m</td>
<td>Radius of bond wire</td>
</tr>
<tr>
<td>(h)</td>
<td>0.5 mm</td>
<td>Wire height</td>
</tr>
<tr>
<td>(A_{\text{die}})</td>
<td>.0056 mm^2</td>
<td>Die IO pad area</td>
</tr>
<tr>
<td>(A_{\text{sub}})</td>
<td>.25 mm^2</td>
<td>Substrate IO pad area</td>
</tr>
<tr>
<td>(t)</td>
<td>508 (\mu)m</td>
<td>Substrate Dielectric thickness</td>
</tr>
<tr>
<td>(\varepsilon)</td>
<td>3.48</td>
<td>Dielectric constant of dielectric</td>
</tr>
<tr>
<td>(\mu)</td>
<td>1</td>
<td>Dielectric material permeability</td>
</tr>
<tr>
<td>(R)</td>
<td>10 m(\Omega)</td>
<td>Resistance (skin effect @9GHz)</td>
</tr>
<tr>
<td>(f)</td>
<td>Swept 1-10 GHz</td>
<td>Test frequency</td>
</tr>
<tr>
<td>(n)</td>
<td>12</td>
<td>Number of slices used in algorithm</td>
</tr>
<tr>
<td>(L)</td>
<td>9.10 nH</td>
<td>1mm Bond wire inductance</td>
</tr>
<tr>
<td>(C_s)</td>
<td>32 fF</td>
<td>1mm Bond wire capacitance</td>
</tr>
<tr>
<td>(L)</td>
<td>.455 nH</td>
<td>0.5mm Bond wire inductance</td>
</tr>
<tr>
<td>(C_s)</td>
<td>16 fF</td>
<td>0.5mm Bond wire capacitance</td>
</tr>
<tr>
<td>(C_{\text{io2}})</td>
<td>.391 fF</td>
<td>Die IO pad capacitance</td>
</tr>
<tr>
<td>(C_{\text{io1}})</td>
<td>17.4 fF</td>
<td>Substrate IO pad capacitance</td>
</tr>
</tbody>
</table>

3.7.1 Amplifier Performance With and Without Bondwires

The device was simulated in order to show the AC frequency response with output bondwires of 1 mm and 0.5 mm length as well as a case with no bondwires. The simulation results in Figure 3.7.1.1(a) and Figure 3.7.1.1(b) show the gain and phase at the load as a function of frequency, respectively. It can be seen that above 1 GHz both the gain and phase are affected by the presence of the bondwires, and the effect increases with frequency. The phase margin (phase where gain crosses zero dB) should be above 50° for a stable amplifier. Figure 3.7.1.1 (a) and (b) show the amplifier without the bondwire has a phase margin of 52°, while the phase margin decreases to 26° and 10° considering the effects of the 0.5 mm and 1 mm bondwires, respectively. The results
indicate that a stability issue with the amplifier design should be addressed after considering the bondwires. This example illustrates the importance of considering bondwire effects at RF frequencies and the ease of using the proposed bondwire model with state of the art circuit design tools.

Figure 3.7.1.1. Power amplifier characteristics with bondwire comparison: (a) voltage gain and (b) phase.
3.8 Chapter Summary

In this chapter, a technique for modeling bondwires of arbitrary geometries is presented. The model is based on a numerical solution for each lumped element of a bondwire model including inductance, mutual inductance, capacitance, mutual capacitance, resistance, and IO pad capacitance. It can be run using any scripting language and implemented with a SPICE simulator. Three bondwire and five bondwire network measurement results show this proposed numerical bondwire model can track the measured bondwire s-parameter responses of $S_{11}$ and $S_{21}$ up to 10 GHz well. For all measured parameters, the modeling results using our proposed method have a lower MAE and RMSE than either benchmark model. This straightforward technique is applicable to bondwires of any size providing the geometry is known and can be predicted with geometric equations. This technique requires no proprietary software to implement as its estimations result in a lumped element network which can be used by most circuit simulators. In order to demonstrate the model’s usefulness and compatibility with circuit design tools, a test case of a power amplifier coupled with bondwire outputs was analyzed in the frequency domain.
4 Bondwire Compensation

4.1 Introduction

Bondwires are regularly used to attach integrated circuit (IC) electrical signals with off die destinations. As a bondwire is a conductor with limited (if any) geometry control it will have an undesired impedance. If a wire with an arbitrary geometry is to interface to a controlled impedance line a discontinuity will result. The method presented in this dissertation is a means of compensating for the impedance mismatch between the bondwire and the transmission line. As a demonstration of bondwires in a signal chain a cutaway view of two ICs on a printed circuit board (PCB) is shown in Figure 3.7.1.1. In this view with the two packages shown, the signal lines on the ball grid array (BGA) package and the PCB have controlled impedances. These are interconnected with vias, solderballs, and pins to the quad flat no lead (QFN) package. Of these structures, the bondwire has the longest electrical length of the uncontrolled impedance structures making it a prime target for improvement. In a system there may be several such interconnections with the bondwires affecting the signal at each transition. The impact of bondwires will be shown later in this dissertation to be severe with $S_{21}$ losses greater than
3 dB above 4 GHz. As a solution to this loss, this dissertation presents a circuit to be implemented as part of a packaged device’s input output (IO) path. This circuit uses the bondwire’s inductance combined with other lumped elements to create an impedance matching network. This network negates the effect of the transmission line discontinuity caused by the bondwire connection reducing loss by 3.7 dB at 6 GHz.

Pushing the limits of high frequency signals over bondwires is an active area of interest. The results obtained by groups focusing on wideband frequency applications are presented in [30] [31] [32], which model a test design featuring a bond wire acting as a transmission line leading from a PCB to the RF IC. These techniques require a custom layout of the bondwire to obtain the desired bondwire transmission line characteristics. Static and dynamic capacitors have been integrated into substrates to decrease the inductance of bondwires and improve signal transmission from 1 to 3 GHz [33], but this was only tested in simulation. Other approaches optimize wire bond points on the package [34] [12] through manipulating the package pinout. While these pinout changes improve device performance, the solution presented in this dissertation can be used with any pinout. Yet another solution adds a microelectromechanical systems (MEMs) switch device using inductors and capacitors to create a match [35]. The MEMs technique requires special placement of the device which may not be compatible with all packaging technologies.
Figure 3.7.1.1. Bondwires used in a signal chain.

This dissertation presents two lumped element networks as ways to improve bondwire performance through impedance matching. One method adds a series capacitor to the bondwire’s intrinsic inductance resulting in a narrowband frequency performance enhancement. The second method implements a shunt capacitor and series inductor with the bondwire’s inductance in order to obtain a broadband performance increase. Both networks have been tested to reduce loss in the bondwire extending signal transmission capabilities of the signal chain to more than 5.5 GHz. This method has a distinct advantage over some of the previously mentioned attempts in that it may be implemented after device fabrication with discrete elements attached to the package or PCB carrier per design requirements. It may also be implemented with variable capacitors on die adding to its flexibility. The objective of this chapter is to explore and demonstrate a network that improves device performance through transmission line impedance matching. Most analysis in this dissertation is performed using scattering parameters (s-parameters)
which are a form of electrical network analysis commonly used for analyzing RF packaging and interconnections [36] [37] [38].

4.2 Transmission Line Matching

4.2.1 Series LC Network Theory

Bondwires can present an impedance discontinuity which will result in reflections on the transmission lines. These reflections cause ringing and reduce the power delivered to the load. In a perfectly matched system the load impedance matches the source impedance resulting in no ringing and maximum power transfer.

The characteristics of a bondwire inductor in series with a compensation capacitor are reviewed here to form a basis for a more detailed analysis in a later section. The inductor will act as an approximation of a bondwire without the self capacitance, \( C_s \), or resistance, \( R \). The self capacitance and resistance will be included later in this dissertation during the detailed modeling and testing of the compensation networks. This topology has the side effect of creating a direct current (DC) block on the signal line which may affect other aspects of the design. Since many designs require DC blocks on their high frequency ports, this will generally not be a problem. The proposed network with the additional compensation capacitor is shown in Figure 4.2.1.1.
4.2.2 Resonant Circuit

As the $R$ value will tend to be small for the bondwire, the $L$ and $C_{\text{comp}}$ values are used to compute the parameters for the resonant circuit. When this circuit is in resonance, its impedance will be near zero resulting in a source seeing the impedance caused by $R_L$ only and not the bondwire in series with $R_L$. Without the compensation capacitor, the network impedance will simply increase with frequency. For this impedance minimization approach, the $C_s$ can be ignored as well. The results are impacted little by this capacitance which will be considered later in this dissertation in the LCL tee network.

The fundamental angular frequency of the resonant circuit is

$$\omega_0 = \frac{1}{\sqrt{LC}}$$  \hspace{1cm} (4.2-1)

The impedance of the resonant circuit as a function of angular frequency is
The impedance of an inductor is

\[ Z_{IND} = j\omega L. \tag{4.2-3} \]

As real and complex impedances are present, from \( R \) and \( L \) respectively, use (4.2-4) to combine real and imaginary impedances to find the absolute impedance

\[ Z_{ABS} = \sqrt{im^2 + re^2} \tag{4.2-4} \]

where \( im \) is the imaginary component of the impedance and \( re \) is the real component of the impedance.

A plot of the impedance of a bondwire vs. the impedance of a compensated bondwire is shown in Figure 4.2.2.1, where the uncompensated network plot represents a bondwire only without a compensation capacitor. The bondwire is modeled as a 1.0 nH inductor. The compensated network plot represents the same 1.0 nH bondwire, but compensated with a series 0.6 pF capacitor as shown in Figure 4.2.1.1. As can be seen, for lower frequencies the compensated LC network has a high impedance value, but for higher frequencies this is decreased. Above 4.5 GHz, the compensated network
impedance becomes closer to the source impedance of 50 Ω than uncompensated, which will result in better power transfer to the load.

4.2.3 Impedance Mismatches

In RF design, impedance matching matters. In high frequency circuits there is a driver with a source impedance ($Z_S$) which drives a load with a specific load impedance ($Z_L$). If these impedances are mismatched, energy is lost during transmission which is undesirable. This lost energy is the ratio of the voltage reflected back to the source, $V_{reflected}$, to the voltage delivered to the load, $V_{incident}$, and is called mismatch loss.

The mismatch loss in dB can be found in (4.2-5)

$$ML_{dB} = \log_{10}(1 - \rho^2).$$  \hspace{1cm} (4.2-5)
where $\rho$ is the magnitude of $\Gamma$ and $\Gamma$ is the reflection coefficient, given in (12)

$$\Gamma = \frac{V_{\text{reflected}}}{V_{\text{incident}}} = \frac{Z_L - Z_S}{Z_L + Z_S}. \quad (4.2-6)$$

Comparing a compensated bondwire represented by a 1.0 nH inductor and 0.6 pF compensation capacitor against a 1.0 nH uncompensated bondwire in Figure 4.2.3.1 it can be seen that the mismatch loss decreases at higher frequencies for the network. This plot is based on $50 \, \Omega \, Z_S$ and $Z_L$. A lower mismatch loss implies more power is transferred to the load and less is lost due to reflections. The mismatch loss curves in Figure 4.2.3.1 agree with the curves found in Figure 4.2.3.1. Above 4.5 GHz the compensated network has less mismatch loss representing more power being transferred to the load.

![Mismatch loss compensated and uncompensated networks](image)

*Figure 4.2.3.1. Mismatch loss compensated and uncompensated networks.*

Reviewing (4.2-5) and (4.2-6) it can be seen that the mismatch loss in a network is greatest when there is a short in the load impedance ($Z_L = 0$) or when the load
impedance is open \((Z_L = \infty)\). A plot of the mismatch loss in a 50 Ω system is shown in Figure 4.2.3.2. From this plot it can be observed that as \(Z_L\) strays from 50 Ω, the loss increases. This increase will become important in later sections when comparing the input impedance of a network vs. its frequency responses.

![Mismatch loss in a 50 Ω system.](image)

**Figure 4.2.3.2. Mismatch loss in a 50 Ω system.**

The return loss of the network is a ratio of the incident power to the reflected power \([39]\). This is represented in dB by

\[
RL_{dB} = -20 \times log_{10}(\rho).
\]  

(4.2-7)

Return loss is a measurement of how well impedances are matched in the system. A larger return loss indicates better matching. A return loss plot with a compensated
bondwire and uncompensated bondwire is shown in Figure 4.2.3.3. As seen in Figure 4.2.3.3 it is apparent that at frequencies higher than 4.5 GHz the incident power of the compensated network is greater than the uncompensated network. The asymptote represents the point of maximum power transfer to the load. The peak return loss at 6.5 GHz indicates the compensated network is resonating.

![Graph showing network and inductor return loss](image)

**Figure 4.2.3.3. Network and inductor return loss.**

S-parameters are used throughout this dissertation during analysis. $S_{11}$ is equivalent to the input complex reflection coefficient and $S_{21}$ is the forward complex transmission coefficient. $S_{11}$ and $S_{21}$ are determined by measuring the magnitude and phase of the incident, reflected, and transmitted signals when the output is terminated in a load that is perfectly matched to the source. The relationship to the magnitude of $S_{11}$ to the return loss is

$$S_{11} = -\text{RL}_{dB}. \quad \text{(4.2-8)}$$
The magnitude of $S_{21}$ is calculated by

$$S_{21} = 20 \cdot \log_{10}(V_{out}/V_{in}). \quad (4.2-9)$$

$S_{11}$ and $S_{21}$ are plotted in Figure 4.2.3.4. For both $S_{11}$ and $S_{21}$, improvement can be seen for the compensated network at frequencies above 4.5 GHz. These results correspond to the improvement previously seen for mismatch loss and return loss.

![Graph showing S-parameter comparison for compensated and uncompensated cases: (a) $S_{11}$ and (b) $S_{21}$.](image)

**Figure 4.2.3.4. S-parameter comparison for compensated and uncompensated cases:**

(a) $S_{11}$ and (b) $S_{21}$.

### 4.3 Tee Network Bondwire Compensation

The tee network was chosen for its simplicity, ease of calculation, and the fact that broadband and narrowband matching profiles could be achieved. Figure 4.2.3.1 shows two different tee network configurations. Configuration (a) is the LCL tee network and configuration (b) is the LCC network. In each network, the first inductor ($L_{BW}$) represents
the inductance caused by the bondwire while \( R \) is the bondwire’s resistance. The shunt capacitor \( (C_{TEE} \text{ and } C_{TEE1}) \), series capacitor \( (C_{TEE2}) \), and series inductor \( L_{TEE} \) are the additional elements added in the tee method. The bondwire’s self capacitance can be absorbed into \( C_{TEE} \) or \( C_{TEE1} \) in order to make a more accurate model.

\[
\begin{align*}
\text{(a)} \\
\text{(b)}
\end{align*}
\]

*Figure 4.2.3.1. Tee networks (a) LCL and (b) LCC.*

### 4.3.1 Tee Network Equations

As the tee network is a series of lumped elements connected to a two-port network, ABCD parameters are created for convenient use in analyzing cascaded networks of lumped elements. The ABCD parameters will then be converted to \( Z \)-parameters and finally to \( s \)-parameters for visually analyzing the circuit responses.

In a cascaded network, transmission parameters can be used to compute a single equivalent series network by multiplying network matrices together [40]. These matrix
multiplications must happen in the reverse order of the series of components of the network.

In general an ABCD network is written as

\[
\begin{bmatrix}
A & B \\
C & D
\end{bmatrix}.
\]

Generally for ease of computation and display, inverse ABCD networks are used, where the inverse matrix \( b \) of \( a \) is

\[
b = [a]^{-1}.
\]

The series resistor *inverse* ABCD network is

\[
b_3 = \begin{bmatrix} 1 & -R \\ 0 & 1 \end{bmatrix}.
\]

The series inductor *inverse* ABCD network is

\[
b_2 = \begin{bmatrix} 1 & -j\omega L \\ 0 & 1 \end{bmatrix}.
\]

The shunt capacitor *inverse* ABCD network is
\[ b_1 = \begin{bmatrix} 1 & 0 \\ -j\omega C & 1 \end{bmatrix}. \] (4.3-5)

The series capacitor inverse ABCD network is

\[ b_0 = \begin{bmatrix} 1 & -1 \\ 0 & 1 \end{bmatrix}. \] (4.3-6)

The test networks used in this study are connected to their source and load via series 50 Ω microstrip transmission lines (mlines). The basic transmission line unit is given in Figure 4.3.1.1 which represents a unit length section of the line.

![Basic transmission line unit](image)

**Figure 4.3.1.1. Basic transmission line unit.**

The values of the lumped elements of the transmission line are estimated as follows.

The capacitance per meter is
where \( H \) is the dielectric thickness, \( W \) is the mline width and \( T \) is the mline thickness.

The inductance per unit meter is

\[
L_{TL} = Z_0^2 \cdot C_{TL}
\]  

(4.3-8)

where \( Z_0 \) is the characteristic impedance of the line.

The transmission line ABCD parameter is

\[
a_4 = \begin{bmatrix}
\cosh(Y \cdot l) & Z_0 \sinh(Y \cdot l) \\
\sinh(Y \cdot l) & \cosh(Y \cdot l)
\end{bmatrix}
\]  

(4.3-9)

where \( l \) is the length of the transmission line in meters and

\[
Y = \sqrt{(R_{TL} + j\omega L_{TL})(j\omega C_{TL})}
\]  

(4.3-10)

assuming the mline’s conductance (\( G \)) is negligible. The resistance is based on (11) and (12) but for a rectangular cross section.

Finally, the ABCD parameter is inverted for the combination of the elements.
The ABCD parameters for the LCL tee are

\[
\begin{align*}
\mathbf{b}_4 &= [\mathbf{a}_4]^{-1}. \\
\mathbf{ABCD}_{LCL} &= [\mathbf{b}_4 \mathbf{b}_2 \mathbf{b}_1 \mathbf{b}_3 \mathbf{b}_4]^{-1}. 
\end{align*}
\]  

The completed LCL test network with ABCD parameter elements is given in Figure 4.3.1.2. Note that the input and output impedance are not explicitly modeled as separate lumped elements and the inverse ABCD parameters will vary with device value.

The ABCD parameters for the LCC tee are

\[
\begin{align*}
\mathbf{ABCD}_{LCC} &= [\mathbf{b}_4 \mathbf{b}_0 \mathbf{b}_1 \mathbf{b}_2 \mathbf{b}_3 \mathbf{b}_4]^{-1}. 
\end{align*}
\]  

Figure 4.3.1.2. LCL Lumped element test network.
ABCD parameters can be converted between Z and s-parameters [41]. ABCD parameters break out such that

\[ z_{11} = \frac{A}{C}, \]  
\[ z_{12} = \frac{A \cdot D - B \cdot C}{C}, \]  
\[ z_{21} = \frac{1}{C}, \]  
and

\[ z_{22} = \frac{D}{C}. \]

Z-parameters can then be transferred into s-parameters using the following sets of equations

\[ s_{22} = \frac{(z_{11} + Z_0)(z_{22} - Z_0) - (z_{12} \cdot z_{21})}{\Delta s}, \]
and

\[ S_{22} = \frac{(z_{11} - Z_0)(z_{22} + Z_0) - (z_{12} * z_{21})}{\Delta s} \]  

(4.3-21)

where

\[ \Delta s = (z_{11} + Z_0)(z_{22} + Z_0) - (z_{12} * z_{21}) \]  

(4.3-22)

and \( Z_0 \) is the characteristic impedance of the test ports.

With the Z-parameters the input impedance of the network can be figured by

\[ Z_{in} = z_{11} - \frac{(z_{12} * z_{21})}{(z_{22} + Z_L)} \]  

(4.3-23)

70
where \( Z_L \) is the load impedance of the network.

### 4.3.2 Tee Network Calculations

The parameters for bondwire and the mlines are derived by using equations in the previous section and chapter. Table 4.3.1 lists the lumped element properties and derived parameter values.

#### Table 4.3.1. Bondwire parameter calculation values.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>( l )</td>
<td>3.14 mm</td>
<td>Length of bond wire</td>
</tr>
<tr>
<td>( \sigma )</td>
<td>5.8x107 S/m</td>
<td>Bondwire conductivity</td>
</tr>
<tr>
<td>( r )</td>
<td>37.5( \mu )m</td>
<td>Radius of bond wire</td>
</tr>
<tr>
<td>( h )</td>
<td>1.0 mm</td>
<td>Wire height</td>
</tr>
<tr>
<td>( A )</td>
<td>.25 mm(^2)</td>
<td>IO pad area</td>
</tr>
<tr>
<td>( t )</td>
<td>508 ( \mu )m</td>
<td>Dielectric thickness</td>
</tr>
<tr>
<td>( \varepsilon )</td>
<td>3.48</td>
<td>Dielectric constant of dielectric</td>
</tr>
<tr>
<td>( \mu )</td>
<td>1</td>
<td>Dielectric material permeability</td>
</tr>
<tr>
<td>( f )</td>
<td>Swept 1-10 GHz</td>
<td>Test frequency</td>
</tr>
<tr>
<td>( L_{\text{self}} )</td>
<td>2.9 nH</td>
<td>Bond wire inductance</td>
</tr>
<tr>
<td>( r )</td>
<td>10 m( \Omega )</td>
<td>Bond wire resistance</td>
</tr>
<tr>
<td>( C_{\text{self}} )</td>
<td>100 fF</td>
<td>Bond wire capacitance</td>
</tr>
<tr>
<td>( C_{\text{TL}} )</td>
<td>109pF</td>
<td>Capacitance per unit length</td>
</tr>
<tr>
<td>( L_{\text{TL}} )</td>
<td>273 pH</td>
<td>Mline inductance per unit length</td>
</tr>
<tr>
<td>( R_{\text{TL}} )</td>
<td>Varies with ( f )</td>
<td>Mline resistance per unit length</td>
</tr>
<tr>
<td>( Z_0 )</td>
<td>50 ( \Omega )</td>
<td>Mline characteristic impedance</td>
</tr>
<tr>
<td>( L )</td>
<td>9.7 mm</td>
<td>Mline length</td>
</tr>
<tr>
<td>( W )</td>
<td>1.09 mm</td>
<td>Mline width</td>
</tr>
<tr>
<td>( T )</td>
<td>.04 mm</td>
<td>Mline thickness</td>
</tr>
<tr>
<td>( H )</td>
<td>.51 mm</td>
<td>Dielectric thickness</td>
</tr>
</tbody>
</table>

### 4.3.3 Tee Network Impedance Check

The impedance seen by the source is \( Z_{\text{in}} \) which will determine how much power is transferred to the load. This can be used to estimate the attenuation caused by the network for each tee type. Unfortunately the impedance for these networks is complex. This
makes it difficult to plot and interpret the network $Z_{in}$. Mismatch loss measurements take into account complex impedances and give an indication of how a network will perform. The mismatch loss plot for a LCL network including the transmission lines at input and output in Figure 4.3.3.1 reveals that for the 0.3 pF, 0.5 pF and 0.7 pF networks a lower mismatch loss is expected below 9.5 GHz, 6.5 GHz, and 5.0 GHz, respectively. The bandwidth of the network will be tested in the next section to verify these simulation results with the experimental results from the proposed model. As can be seen in Figure 4.3.3.1, the 0.3 pF, 0.5 and 0.7 pF capacitance value provide a lower loss solution than the 0.1 pF capacitor or the uncompensated bondwire. This shows that tuneable capacitor would be appropriate to use as it could be varied based on final bondwire lumped element values.
Figure 4.3.3.1. *LCL tee network mismatch loss with varying CTEE.*

The mismatch loss of the LCC tee for various compensation values based on the proposed model is shown in Figure 4.3.3.2. This plot illustrates the peaking nature of the network as the impedance is only well matched for the specific frequencies where the compensated networks have a lower loss than the uncompensated networks. These points will be reflected in the $S_{11}$ and $S_{21}$ plots of the network in the next section which show where the least loss is present. The peaks are at 4.2 GHz, 4.9 GHz, 5.5 GHz, and 6.8 GHz for 0.4 pF, 0.3 pF, 0.2 pF, and 0.1 pF compensation values, respectively. The smaller the value of $C_{COMP}$ used, the higher the peaking frequency and the narrower the passband. Again, this demonstrates that a tuneable capacitor would be useful for tuning response to a specific frequency based on the bondwire lumped element values.
As mismatch loss translates directly into loss and reflections in a network, the mismatch loss will be reflected in s-parameter measurements. A 1.0 dB increase in mismatch loss will add 1.0 dB to the reflection measurement of $S_{11}$ and a 1.0 dB decrease in the gain through the network’s $S_{21}$ measurement. For this reason, it is important to minimize mismatch loss, but in reality physical systems will have some mismatch loss present.

**Figure 4.3.3.2. LCC tee network mismatch loss with varying CTEE.**
4.4 Tee Network Test Results

4.5 Test Fixture

A bondwire test fixture was created to test the models in a physical environment. The fixture was designed in Agilent ADS and then milled using a PCB milling machine on a 2-layer piece of Rogers 4350B low loss dielectric material. The test fixture has a number of test circuits to allow the characterization of several circuits in a single test session and three of these are shown in Figure 4.3.3.1. The signal wire is attached to SMA connectors via a 9.7 mm 50 Ω microstrip line. In between each line is a 3.14 mm bondwire and compensation capacitor.
4.5.1 LCL Tee Network Test Results

The tee networks were built using the same test fixture type shown in Figure 4.3.3.1. Tests were conducted with two compensation networks: the first with a $L_{TEE}$ of 1.0 nH and a $C_{TEE}$ of 0.3 pF and the second with a $L_{TEE}$ of 1.0 nH and a $C_{TEE}$ of 0.5 pF. The goal of this design was to achieve a wideband compensation which is shown in Figure 4.5.1.1 and Figure 4.5.1.2 through $S_{11}$ and $S_{21}$, respectively. The $S_{11}$ plot in Figure
4.5.1.1 shows the ratio of the voltage reflected to the voltage incident at the input port of the network. The lower frequencies have a small amount of reflected energy, but as frequency increases, the reflected energy increases. The measured results show a several dB offset in reflected voltage for the lower frequencies between the uncompensated and compensated networks. The $S_{21}$ plot in Figure 4.5.1.2 shows the gain through the network. The passband for the 0.3 pF network compared to an uncompensated wire starts improving around 2.0 GHz and continues until 6.5 GHz where it crosses the uncompensated network’s measurement. The passband for the 0.5 pF network starts at 2.0 GHz and continues to 5.5 GHz where it crosses the uncompensated measurement.

The tradeoff with this technique is a steep rolloff around at the end of the passband for each solution. The line marked “1.0 dB Drop” will be considered in a later section when quantifying the improvement of this network. The network becomes what is effectively a low pass filter, increasing the gain through the network at low frequencies and reducing it at high frequencies.
Figure 4.5.1.1. Measured $S_{11}$ for LCL tee network.

Figure 4.5.1.2. Measured $S_{21}$ for LCL tee network.
The network performance can be predicted from the mismatch loss plot of Figure 4.2.3.2. The low amount of loss present in Figure 4.2.3.2 at lower frequencies results in a very low $S_{11}$, meaning more energy is transferred to the load. The slow slope and low mismatch loss below 5.0 GHz can be seen in $S_{21}$ with the $S_{21}$ gains not decreasing at a great rate until the mismatch losses begin to exponentially increase. The test results agree with the modeling predictions for frequencies below 6.0 GHz using a $C_{\text{comp}}$ value of 0.3 pF. Results are also in agreement for the 0.5 pF model for frequencies below 5.0 GHz.

### 4.5.2 LCC Network Test Results

The tested LCC network assumes the shunt capacitor is the bondwire’s $C_s$. This model is based on the equations presented in section 4.3.1 and uses the same test fixture type as the LCL network. Test results for $S_{11}$ and $S_{21}$ for this network are given in Figure 4.5.2.1 and Figure 4.5.2.2. It can be seen from Figure 4.5.2.1 that the reflections in the network will be reduced at several peak locations for the compensated networks whereas the uncompensated network has the least reflected energy at low frequencies and the reflections increase with frequency. From Figure 4.5.2.2, which shows the gain through the network, it can be observed that the smaller compensation capacitor values shift the optimum gain point of the network to a lower frequency. Knowing these peaks and a target frequency, a variable capacitor on die or a fixed capacitor on the package or PCB could be used to tune the response to a specific frequency.

Both Figure 4.5.2.1 and Figure 4.5.2.2 show the ABCD parameter model is a more accurate approximation of the response of the network than the simpler LC network presented in a previous section. Comparing calculated to measured results, it is seen that
the LCC model does approximate the $S_{11}$ inflection point for the reflected power in a very frequency accurate manner. The amplitude of the reflection, however is underestimated. The LC model (labeled as “Calculated LC w/0.2 pF”) misses the frequency and amplitude measurements. Gain through the circuit shown in Figure 4.5.2.2 is accurately modeled for the LCC case. Given that capacitor tolerance for these values are 0.1 pF, the LCC estimations fall well within the device tolerance. The LC model, while frequency accurate, does not approximate the gain with great accuracy. The LC model overestimates the effectiveness of the compensation creating a lossless network. However, this model can be used as a starting point for choosing values for the LCC networks.
Figure 4.5.2.1. Measured $S_{11}$ for LCC tee network.
Figure 4.5.2.2. Measured $S_{21}$ for LCC tee network.

We can use the mismatch loss plotted in Figure 4.2.3.2 to predict the results of the LCC network. As can be seen in Figure 4.2.3.2, the mismatch loss is a parabola which indicates lower loss at certain peaks. For the $S_{11}$ measurements, these lower mismatch loss peaks result in lower levels of $S_{11}$ reflections. For the $S_{21}$ measurements, the low peaks in Figure 4.2.3.2 indicate more energy is passed to the load.

4.5.3 Test Results Analysis

The test results are summarized in Table 4.5.1 for LCL networks, where the broadband cutoff is the point where the gain through the network drops by 1.0 dB. In the LCL results table, it can be observed that the LCL offers a broadband advantage of 3 dB
over an uncompensated network up to 5.5 GHz. Graphically this is shown in Figure 4.5.3.1 where the gains from each compensation network are given. The area labeled “Common gain” is the gain overlap from both networks compared to the uncompensated wire. The labeled regions of “0.5 pF Gain” and “0.3 pF Gain” are the gain provided by their respective compensation solutions. It can be seen from this plot that both compensation networks provide an improvement over an uncompensated wire.

\[ \text{Table 4.5.1. LCL Network Test Values} \]

<table>
<thead>
<tr>
<th>Broadband Cutoff</th>
<th>Compensated Gain @ Cutoff</th>
<th>Uncompensated Gain @ Cutoff</th>
<th>LTEE</th>
<th>CTEE</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.4 GHz</td>
<td>-1 dB</td>
<td>-4 dB</td>
<td>1.0 nH</td>
<td>0.5 pF</td>
</tr>
<tr>
<td>5.5 GHz</td>
<td>-1 dB</td>
<td>-4 dB</td>
<td>1.0 nH</td>
<td>0.3 pF</td>
</tr>
</tbody>
</table>

\[ \text{Figure 4.5.3.1. LCL } S_{21}\text{ gain.}\]
Table 4.5.2 illustrates the test results for the LCC network. In Table 4.5.2 the LCC network’s gain is given at its peak frequency as well as the uncompensated network’s gain at the peak frequency. The difference between these values is the gain advantage the compensation network provides. Gains of 2-3.8 dB are achieved over the frequencies selected with the max gain happening at the highest frequencies. Figure 4.5.3.2 is given to better illustrate the gain from the compensation networks. In Figure 4.5.3.2 network capacitance measured $S_{21}$ values for 0.1 pF and 0.2 pF are plotted to compare their performance to an uncompensated wire. The “Common gain” highlight is the gain achieved using either compensation value in the network. Each capacitor value has its own gain highlighted as well. Figure 4.5.3.2 shows the compensation network improvements offered over an uncompensated bondwire.

Comparing LCC and LCL networks, it can be concluded that the LCL network is a better fit for systems operating at multiple frequencies up to 6.0 GHz. In contrast, the LCC network can improve system $S_{11}$ and $S_{21}$ performance in specific frequency bands from 3.0 GHz to 10.0 GHz.

Table 4.5.2. LCC Network Test Values

<table>
<thead>
<tr>
<th>Peak Frequency</th>
<th>Gain @ Peak Frequency</th>
<th>Uncompensated Gain @ Peak</th>
<th>CTEE2</th>
<th>CTEE1</th>
</tr>
</thead>
<tbody>
<tr>
<td>6 GHz</td>
<td>-0.8 dB</td>
<td>-5.5 dB</td>
<td>0.1 pF</td>
<td>140 fF</td>
</tr>
<tr>
<td>5 GHz</td>
<td>-0.7 dB</td>
<td>-4.5 dB</td>
<td>0.2 pF</td>
<td>140 fF</td>
</tr>
<tr>
<td>4.5 GHz</td>
<td>-0.6 dB</td>
<td>-3.5 dB</td>
<td>0.3 pF</td>
<td>140 fF</td>
</tr>
<tr>
<td>3.3 GHz</td>
<td>-0.5 dB</td>
<td>-2.5 dB</td>
<td>0.4 pF</td>
<td>140 fF</td>
</tr>
</tbody>
</table>
4.6 Applications

This technique can be used for many combinations of bondwire sizes and compensation capacitors. This provides a way for custom matching an RF component to an application after fabrication. A component such as an amplifier can be left uncompensated at lower frequencies if that area of response is desired but if higher frequency operation is desired a compensation capacitor could be inserted into the package in order to improve performance. This could also be done using an integrated switch and capacitor network in the IC to choose specific capacitances or integrated, variable capacitors that could be tuned for certain frequencies. A plot of the compensation curves given in Figure 4.5.3.1 and Figure 4.5.3.2 illustrates this concept.
From these plots it can be seen a reasonable wideband solution can be assembled from multiple narrowband solutions. The LCL tee compensation is another option with a wider bandwidth, but lower overall frequency and steep roll off.

4.7 Chapter Summary

In this chapter a method for improving bondwire interconnections in RF ICs was introduced. The methods used are tee LCC and LCL networks which reduce the impedance mismatch caused by bondwires. The theory and models of the interconnects were introduced and measurements taken to validate the approach. The method can be used post fabrication and installed into the device packaging in order to tune devices after characterization. For the narrow bandwidth network, a 4 dB improvement was demonstrated at 6 GHz while the wideband network demonstrated a 4 dB gain improvement at 5.5 GHz.
5 Power Integrity
Improvement Through
Direct Die Attach

5.1 Power Integrity Introduction

Power integrity affects high frequency circuit operation. The power distribution network (PDN) is the network of power supplies and parasitics affecting power delivery to devices requiring power. This is shown in Figure 4.5.3.1 for various sources of inductance and resistance in an electrical system. This can happen both with and without a bondwire attached device as the connections to power are effectively through small inductors. Local power noise is generated on a chip when the current draw requirements of a device exceed the power locally available causing a transient droop on the power supply rail. Other sources of noise include power supply switching noise [42], and high frequency digital circuits. This unwanted noise is typically mitigated by using decoupling capacitors, which act as a noise filter on a power rail [43]. The capacitors can be integrated onto the chip, the package, and the package carrier – typically a printed circuit board (PCB) [44] [45] [46] [47].
The size of the decoupling capacitor is one of the primary factors in determining which frequencies it will filter. The available capacitor values are limited by the location of the capacitors. PCB mounted capacitors may vary in size from 0.1 pF to 1,000 µF, however the effectiveness of the smaller capacitors will be reduced by parasitics between the chip and the board. On-package decoupling is limited to smaller capacitors, but some of the parasitics between the PCB and package may be eliminated allowing for higher frequencies to be filtered. On-chip decoupling capacitors are integrated into the IC’s substrate and limited to values less than 100 pF [48] [49]. On-die decoupling, which this work introduces has the capacitors stacked onto the integrated circuit die eliminating parasitics caused by both the packaging and PCB resulting in frequency coverage not possible by on-chip decoupling alone.

The decoupling approach this chapter introduces involves the attachment of discrete capacitors to the top of an IC die on standard IO pads. These additional capacitors filter signals from 100 kHz to 100 MHz. For example, 10,000 pF devices are available in 380 x 380 µm (0101) packaging. Several larger 600x300 µm (0201) packages fit on a 2 mm x 2 mm die as shown in Figure 4.5.3.2. Figure 4.5.3.3 shows the
additional capacitors as well as the other sources of non-ideality in power distribution system. These devices would electrically connect to the IC power rails through large input/output (IO) pads on the top of the die. Capacitor values up to 1 µF are available in the 0201 package. These devices electrically connect to the IC power rails through input/output (IO) pads on top of the die.

![Figure 4.5.3.2. Isometric of decoupling capacitors on die.](image-url)
Figure 4.5.3.3. Sideview showing decoupling on package, die, and PCB levels.

Capacitor attachment can be performed before the die is electrically connected to pins during packaging. High viscosity conductive materials exist, which may be applied to the IO pads via standard SMT solder stencil technology such as Epoxy Tech E4110-PFC [50]. After the material is stenciled onto the IO pads, the capacitors would be placed and the die baked allowing the adhesive to dry forming an electrical and mechanical bond between the capacitor leads and the die. Bondwires would then be attached or the die attached to its carrier using flip chip technology. Alternatively, after the die is connected to the package each lead of the capacitor could be dipped into the adhesive and then placed onto the IO pads of the die.

As electronic devices increase in complexity and speed, PDN improvement is an active area of interest. Recent advances include on-package decoupling [51] [45], on-chip decoupling through integrated capacitors [51], the use of decoupling capacitors in
through silicon vias (TSVs) in 3D package stacking [52], and precision decoupling capacitor simulation and placement both on the package and the board [53] [54]. The proposed approach in this dissertation requires no extra die real-estate, extra package complexity, or board PDN simulation software unlike the previous proposed approaches. It also improves the PDN performance better than what could be achieved through board-level or package level decoupling alone. The proposed approach is designed to be used with current decoupling strategies using capacitors on the board, package, and in-chip in order to improve PDN performance while saving package and board real-estate. The approach can be applied after fabrication if the proper IO pads are included in the design as capacitors may be added to the die or their values changed after device characterization.

The objective of the proposed approach is to facilitate the use of large capacitors that perform as if they are on-chip. This effectively combines the capability to incorporate the small on-chip integrated capacitors with the on-die capacitors to permit increased noise reduction for selected frequencies as dictated by the application.

5.2 Sources of PDN Non-Ideality

5.2.1 Bondwires

One source of PDN inductance is packaging bondwires. Of primary concern in this chapter are the self inductance, $L_s$ and the resistance, $R$ of the bondwire. As shown previously, a 1.0 mm bondwire with a 0.25 µm radius has an inductance of 0.9 nH while a 3.0 mm bondwire of the same diameter may have a 2.9 nH inductance. Both of these
inductance values will affect the PDN’s performance as power and/or return currents will have to traverse the bondwires.

### 5.2.2 Capacitors

Real-world capacitors have an inherent resistance and inductance. These are called equivalent series resistance (*ESR*) and equivalent series inductance (*ESL*) [55] [56]. Figure 5.2.2.1 shows the comparison of an ideal capacitor vs. a “real world” model including *ESR* and *ESL*. These parasitics affect the ability of a capacitor to react to changes of current at frequencies above 0 Hz. Example *ESR* curves for multiple packages are shown in Figure 5.2.2.2. From this graph it can be seen the smaller 0201 package has a lower impedance at higher frequencies than larger packages. Figure 5.2.2.2 shows the impedance of various capacitor values in 0201 packaging emphasizing that lower value capacitors cover higher frequencies. Figure 5.2.2.3 compares multiple capacitor values against inductance. Smaller values have a lower inductance at low frequencies. Figure 5.2.2.4 illustrates the resistance curves of the 0201 sized capacitors. The lower capacitance values have a lower resistance. As the figure of merit for capacitors vary with both physical size, capacitance, and frequency multiple decoupling caps must be used to cover all frequency bands of interest.
Figure 5.2.2.1. Capacitor models: (a) ideal capacitor, (b) real capacitor.

Figure 5.2.2.2. Impedance curves for various capacitor package sizes.
Figure 5.2.2.3. Impedance curve for 0201 size capacitors of varying sizes.

Figure 5.2.2.4. Inductance curves for 0201 size capacitors of varying sizes.
Figure 5.2.2.5. Resistance curves for 0201 size capacitors of varying sizes.

Recognizing that capacitors are not simply a purely capacitive element, we can begin to generate more accurate models to understand their behavior.

The resonant frequency of a capacitor is given by

\[
    f_0 = \frac{1}{2\pi} \left( \frac{1}{\sqrt{C \times ESL}} \right). \tag{5.2-1}
\]

above this resonant frequency, the capacitor will behave as an inductor [57].

The impedance of a capacitor is found by

\[
    Z = ESR + \frac{1}{j2\pi fC} + j2\pi f ESL \tag{5.2-2}
\]

where \( f \) is the test frequency [58].
In order to apply (5.2-1) and (5.2-2) to select proper capacitors the switching noise of the PDN needs to be determined as a function of PDN impedance. The switching noise is estimated by

\[ V_{\text{noise}}(t) = L_{PDN} \frac{dI(t)}{dt} \approx L_{PDN} \frac{(I_{\text{max}} - I_{\text{min}})}{tr} \]  \hspace{1cm} (5.2-3)

where \( tr \) is the waveform rise time, \( I_{\text{max}} \) is the maximum amplitude of the current waveform and \( I_{\text{min}} \) is the minimum of the current waveform.

The goal of the PDN is to have an impedance low enough to satisfy the power requirements of the circuit being designed. Other drivers of the PDN impedance are the power plane of the board, package, and chip. The final PDN impedance is the sum of the impedances of the board, package, and chip

\[ Z = Z_{\text{BRD}} + Z_{\text{PKG}} + Z_{\text{CHIP}}. \]  \hspace{1cm} (5.2-4)

The target PDN impedance is

\[ Z_{\text{target}} = \frac{V_{dd} \times \text{tolerance}}{I_{\text{max}} - I_{\text{min}}} \]  \hspace{1cm} (5.2-5)

where \( V_{dd} \) is the supply voltage, the tolerance is the voltage ripple tolerance. The tolerance is determined by the target device, but is usually 5-10%. 

(5.2-5) transforms into

\[ Z_{\text{target}} = \frac{L_{PDN}}{tr} \]  \hspace{1cm} (5.2-6)

where \( tr \) is the risetime.
5.2.3 Conductors and Planes

A third source of system imperfection is conductors and planes present in the various stages of interconnect. The PCB has plane layers which conduct power to the ICs from on board power supplies. These plane layers are also present in BGA packaging and ICs. The plane layers have a resistance and inductance which will cause non-ideality.

5.2.4 PDN Model

Accounting for bondwires, capacitors, and power planes a model can be created which represents the various elements of the PDN. This is given in Figure 5.2.4.1 which illustrates both board and package parasitics being bypassed by the newly added on die decoupling solution as well as the on-chip decoupling. From this model it can be seen on-die decoupling bypasses the package and board parasitics, only being affected by the power distribution network of the chip itself.

![Figure 5.2.4.1. PDN Model incorporating decoupling capacitors.]

5.2.5 Example Decoupling Design

Selecting capacitors for a PDN is based on target impedance. Using (5.2-4) with a $V_{dd}$ of 1 V, a tolerance of 10%, $I_{min}$ of 15 A and an $I_{max}$ of 25 A, a $Z_{target}$ of 0.1 $\Omega$ is
reached. The values of $I_{\min}$, $I_{\max}$, and $V_{dd}$ were taken from a 100,000 flip flop gate array presented and analyzed in [59] to provide a typical IC example. On certain designs, this target may only be present at certain frequencies due to noise at a specific frequency, such as noise caused by an on board clock where many transistors must switch at the same frequency. This knowledge can be used to target frequencies for a specific impedance minimum. The minimum impedance point of a capacitor can be estimated by using (5.2-1). A 68 nF capacitor with a 50 mΩ $ESR$ and an $ESL$ of 200 pH would produce a device with an impedance minimum at 11 MHz. Equation (5.2-2) tells us that device would have an impedance of 50 mΩ as the $ESR$ of the capacitor will dominate the impedance value at the resonant frequency. A 1 µF capacitor with similar parasitics would have an impedance minimum at 43 MHz.

Three networks were created in Agilent ADS and simulated. The capacitor models used were provided by TDK. The schematic diagram for this simulation is given in Figure 5.2.5.1. A network with 1 µF and 68 nF on-die decoupling capacitors was tested, as well as a network with 1 µF and 68 nF off die decoupling capacitors. Each of these two networks had a 10 µF bulk capacitor located off die. A third network with a single 10 µF bulk capacitor off die was also simulated as an additional comparison point. A plot of the three simulated networks is given in Figure 5.2.5.2. From Figure 5.2.5.2, it can be seen the only network that meets the 0.1-Ω target impedance is the network with the capacitors located on die. Knowing the operating characteristics of the design, the 7 mΩ violation at 3 MHz can be evaluated to see if it will impact circuit operation. Minimal improvement is exhibited by the off-die capacitors.
The peaking value on the 1 µF, 68 nF on-die curve is explained by the fact that with any two impedance zeros, a pole must occur. The peak can be reduced by adding series resistance to the capacitors or slightly deviating capacitors from the values used to reduce the zeros [60] [61].

*Figure 5.2.5.1. PDN test diagram.*
5.3 PDN Testing

5.3.1 Measurement Theory

Measuring PDNs can be difficult due to the low impedances involved. An accurate method of measurement involves using a two port vector network analyzer (VNA) using one port to drive the device under test (DUT), in this case the PDN, and the port other to measure the PDN’s impedance as shown in Figure 5.3.1.1. The s-parameter measurements taken can then be transformed into the measured impedance using (5.3-1) [62].

Figure 5.2.5.2. PDN Decoupling Simulated Results.
\[ Z_{DUT} = \frac{-25(S_{21})}{(S_{21} - 1)} \]  

(5.3-1)

**Figure 5.3.1.1. Test schematic. Ports outside of dotted line are VNA ports.**

5.3.2 Test Fixture

In order to test the effects of on-die decoupling, a test fixture has been developed to take measurements of a physical system. The fixture was designed to test the effects of bondwires between the power and ground planes as would be found in typical IC packaging. Test circuits were created, visible in Figure 5.3.2.1. The on-die circuit, Figure 5.3.2.1(a) has a 1 nF and a 68 nF 0201 size capacitors on-die, and an 0805 size 10 µF capacitor off-die. The package level circuit shown in Figure 5.3.2.1(b) has the 1 nF and 68 nF capacitors off -die as well as a 10 µF capacitor. The artwork for a single layout is given in Figure 5.3.2.2.
Figure 5.3.2.1. Three test fixtures with integrated decoupling capacitor fixture (a), off die decoupling capacitors (b), bulk decoupling capacitor only (c).
The test fixture was fabricated on a single sided FR-4 PCB. Bondwires of 3.1mm were used and the fixture was measured through SMA connectors. The schematic of the test fixture is shown in Figure 5.3.2.3. Each fixture was cut from the same PCB artwork resulting in identical trace layouts. The decoupling capacitors were populated differently to represent two scenarios: on chip decoupling with a single bulk capacitor and off chip decoupling with a single bulk capacitor.
5.3.3 Impedance Test Setup

The test was performed using an Agilent E5061B vector network analyzer (VNA). Sweeps were done on a log scale from 100 kHz to 1 GHz. A photograph of the test setup is given in Figure 5.3.3.1. The results were saved as Touchstone format and exported to Matlab for analysis.
5.3.4 Impedance Test Results

The test results from the VNA are plotted in Figure 5.3.3.1. From the tests, it can be seen that the on-die decoupling has a lower impedance curve than the off chip decoupling schemes. The on-die decoupling solution stays below 1 Ω for the entire swept frequency range. In contrast the off die decoupling solution cross the 1 Ω mark at 30 MHz.
5.3.5 Noise Test Setup

To show the effects of the decoupling capacitor configurations at eliminating on-die noise, testing at select frequencies was performed. In the test, the test fixtures were connected to an Agilent N9301A signal generator and Tektronix DPO71254C oscilloscope in parallel. The signal generator’s 50 Ω output was set to 20.0 dBm and the resulting waveforms were recorded on the oscilloscope. 60 s of persistence was used on the waveform to ensure the minimum and maximum values over a given time were recorded. The waveform was sampled at 1.25 GS/s. The maximum peak to peak swings
of these waveforms is given in Table 5.3.1. The RF source represents noise on the power plane which could be caused by noisy circuits such as switching power supplies or digital clocks. From Table 5.3.1, it is observed that the on-die noise tracks the predictions from the impedance test. The on-die decoupling solution offers noise improvements across the tested bands.

Table 5.3.1. Transient test values with 2 dBm input

<table>
<thead>
<tr>
<th>Frequency</th>
<th>Noise w/on die decoupling (mV)</th>
<th>Noise w/off die decoupling (mV)</th>
<th>Noise improvement on die vs. off die (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100 kHz</td>
<td>126</td>
<td>176</td>
<td>40</td>
</tr>
<tr>
<td>1 MHz</td>
<td>61</td>
<td>133</td>
<td>118</td>
</tr>
<tr>
<td>10 MHz</td>
<td>65</td>
<td>317</td>
<td>388</td>
</tr>
<tr>
<td>100 MHz</td>
<td>180</td>
<td>914</td>
<td>408</td>
</tr>
</tbody>
</table>

As a further method of analysis, a spectrum analyzer was used in conjunction with a signal generator. Each instrument was connected to a port on the test fixture. The signal generator’s 50 Ω output was set to sweep points between 1 MHz and 100 MHz for 10 ms at 0.0 dBm. The spectrum analyzer captured the peaks of the output as the signal generator performed the sweep. This output is shown in Figure 5.3.5.1. As predicted by the impedance sweep, the 68 nF on die decoupling solution shows 30 dB of attenuation for the duration of the sweep (1 MHz to 100 MHz) with the off die solution providing the same performance only to 30 MHz. If input frequency was considered power supply noise, this plot represents the power supply rejection ratio, which is a measurement of the rejection of power supply noise on a circuit’s output.
5.4 Chapter Conclusion

In this chapter, a power supply decoupling solution for ICs was introduced, which attaches large decoupling capacitors directly to an IC die. The attachment of these capacitors increases noise reduction in certain frequency bands not covered by on-chip, on-package, or PCB level decoupling solutions. Bondwire effects on IC power supplies were discussed as well as PDN theory and a true capacitor model was introduced. A test fixture was designed, fabricated, and measured demonstrating two decoupling solutions: on-die and on-package. The on-die solution met or out-performed the on-package solution reducing PDN noise for frequencies from 100 kHz to 100 MHz. At 100 MHz, a 408% reduction in noise was realized. Across all test frequencies, a 40% minimum
improvement was observed. Compared to other decoupling solutions, the on-die decoupling capacitors provide a lower impedance and a larger capacitance than previously achievable by avoiding packaging interconnects and providing a large capacitance value close to the IC’s power rails.
6 Filter Improvement Through Direct Die Attach

6.1 LC Filter Introduction

Inductors and capacitors are commonly used in RF circuits such as low noise amplifiers (LNAs), power amplifiers, and voltage controlled oscillators (VCOs) to create a bandpass filter known as an LC tank. The Q-factor of the inductor will determine the filter’s bandwidth as the inductor generally has the lowest Q in the system. A higher Q means a tighter bandwidth with higher output power while a lower Q implies a wider bandwidth over lower output power. Production integrated inductors have a limited Q factor as shown in Figure 5.3.5.1 which is representative of 4.5nH inductors buried in a 10-Ω-cm silicon substrate. In contrast to integrated inductors which exist as part of the die, ceramic multilayer surface mount inductors and capacitors are commonly available in a package 600um x 300um in size. This package will comfortably fit onto the top passivation layer of a 2mm x 2mm die saving die real-estate while increasing device performance. Though these devices have been integrated into SiP circuits in the past, the SiP still must contend with packaging parasitics such as bond wires. Performance plots of
such surface mount devices are given in Figure 5.3.5.2 and Figure 5.3.5.3. A diagram of a die with two such devices attached is shown in Figure 4.5.3.2. From these figures it is apparent that a predictable inductance and Q factor are available for lower inductance external devices up to 3GHz. In the next few sections, the integrated inductor will be introduced, LC filter theory presented, simulations presented which will take into account the effects bondwires can have on an LC tank, and physical measurements taken to verify assumptions regarding the performance of on-die LC tanks.

![Typical Integrated Inductor Q-Factor](image1.png)

**Figure 5.3.5.1 – Typical Integrated Inductor Q-Factor [63]**

![Commercial Ceramic Inductor Performance Characteristics](image2.png)

**Figure 5.3.5.2 - Commercial Ceramic Inductor Performance Characteristics [64]**
6.1.1 Integrated Inductors

The traditional integrated inductor is a 2D conductor structure with a geometry that creates a known inductance. This can be commonly found in the form of a spiral [65] as shown in Figure 6.1.1.1. In traditional Si fabrication situations, the inductor is limited by its series resistance, which is a result of the metal used which is typically Al [66]. Two ways to avoid this are by going off-chip using a SiP technique [67] [68] as shown in Figure 6.1.1.4 or changing the metal used to create the inductor. Other, more exotic structures are available as well such as the recessed 3D solenoid inductor [69] shown in Figure 6.1.1.2 and the external solenoid inductor [70] in Figure 6.1.1.3 are silicon compatible but cannot be manufactured with traditional (non-MEMS) processing steps.
Figure 6.1.1.1 - Conventional Spiral Inductor [65]

Figure 6.1.1.2 - Recessed Solenoid Type Inductors (Cu) [69]

SEM images of three types of solenoid inductors in straight layout. Type (a) is a 8.5-turn compact inductor with 15-μm copper wire width. Type (b) is an 11.5-turn inductor with 25-μm copper strip width. Type (c) is a 31-turn inductor with three straight solenoids serial connected (15-μm copper width).

SEM images of three curve layout solenoid inductors (all with 15-μm copper width). Type (d) is a 31-turn serpentine inductor. Type (e) is a 31-turn quadrate ring inductor. Type (f) is a 16-turn circular inductor.
Figure 6.1.1.3 - 20 Turn Cu Solenoid Inductor [70]

Figure 6.1.1.4 - Wi-Fi Sip with Integrated Passive Components [67]
In order to illustrate the improvement possible with an external inductor, a survey of literature concerning integrated passive conductors is given in Table 6.1.1.

**Table 6.1.1 - Integrated Inductor Comparison**

<table>
<thead>
<tr>
<th>Source</th>
<th>Inductance (nH)</th>
<th>Peak Q</th>
<th>Q Frequency (GHz)</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>[71]</td>
<td>1.5</td>
<td>16</td>
<td>5.45</td>
<td>Model, spiral</td>
</tr>
<tr>
<td>[71]</td>
<td>2.0</td>
<td>14</td>
<td>5.45</td>
<td>Model, spiral</td>
</tr>
<tr>
<td>[71]</td>
<td>2.75</td>
<td>12</td>
<td>5.45</td>
<td>Model, spiral</td>
</tr>
<tr>
<td>[70]</td>
<td>2.67</td>
<td>16.7</td>
<td>2.4</td>
<td>De-embedded on Si, solenoid</td>
</tr>
<tr>
<td>[70]</td>
<td>2.67</td>
<td>24.2</td>
<td>6.0</td>
<td>De-embedded on glass, solenoid</td>
</tr>
<tr>
<td>[72]</td>
<td>5</td>
<td>9.5</td>
<td>2.4</td>
<td>Model, 160um radius</td>
</tr>
<tr>
<td>[72]</td>
<td>5</td>
<td>19</td>
<td>2.4</td>
<td>Model, 220um radius</td>
</tr>
<tr>
<td>[70]</td>
<td>2.78</td>
<td>30</td>
<td>4.5</td>
<td>Type a*</td>
</tr>
<tr>
<td>[70]</td>
<td>2.6</td>
<td>52.3</td>
<td>5.5</td>
<td>Type b*</td>
</tr>
<tr>
<td>[70]</td>
<td>7</td>
<td>16.4</td>
<td>3.0</td>
<td>Type c*</td>
</tr>
<tr>
<td>[70]</td>
<td>5.9</td>
<td>24.9</td>
<td>3.2</td>
<td>Type f*</td>
</tr>
<tr>
<td>[73]</td>
<td>1.6</td>
<td>19.8</td>
<td>2.6</td>
<td>Solenoid on Si</td>
</tr>
<tr>
<td>[74]</td>
<td>1.8</td>
<td>10</td>
<td>3.0</td>
<td>Spiral on 3um Oxide</td>
</tr>
<tr>
<td>[75]</td>
<td>2</td>
<td>14</td>
<td>2-15</td>
<td>Spiral w/Cu conductor</td>
</tr>
<tr>
<td>[75]</td>
<td>2</td>
<td>11.5</td>
<td>2-15</td>
<td>Spiral w/Al conductor</td>
</tr>
<tr>
<td>[64]</td>
<td>2.7</td>
<td>40</td>
<td>3.0</td>
<td>Ceramic inductor only</td>
</tr>
<tr>
<td>[64]</td>
<td>1</td>
<td>48</td>
<td>3.0</td>
<td>Ceramic inductor only</td>
</tr>
</tbody>
</table>

*Reference Figure 6.1.1.2*

As can be seen in the table of inductors, large Q values are difficult to achieve using standard integrated spiral inductors. One must use an exotic process to achieve a Q much above 15. In order to overcome this physical limitation, it is proposed to directly attach an inductor and capacitor to a chip in order to create circuits which require a high Q factor for operation. This configuration is possible even in situations where the device being designed cannot be placed into a package with an inductor on a carrier substrate.
such as in the case of a QFN or QFP package. In the next section the LC tank will be presented.

### 6.1.2 LC Passive Filter Modeling

Many RF circuits use an inductor and capacitor together resonating in parallel to form an LC tank. The Q factor of the inductor in the tank’s resonant circuit determines the bandwidth of the filter and the resulting output power. This selectivity also impacts the noise figure among other RF figures of merit. Two LC tanks are given: one is the on-die tank and the other is the off-chip tank which must run through bondwires as shown in Figure 6.1.2.1. Modeling equations are based on [76]. Attention will be paid to the performance of the resonant circuit which acts as a bandpass filter.

![LC Filter Test Setup](image)

**Figure 6.1.2.1 – LC Filter Test Setup**

The resonant frequency \( \omega_0 \) of the LC tank is

\[
\omega_0 = \frac{1}{\sqrt{LC}}
\]  

(6.1-1)
where \( L \) is the inductance of the inductor in and \( C \) is the capacitance of the capacitor.

The characteristic impedance of the circuit is

\[
Z_0 = \sqrt{\frac{L}{C}} = \omega_0 L = \frac{1}{\omega_0 C}
\]

(6.1-2)

And the loaded quality factor \((Q_L)\)

\[
Q_L = 2\pi \frac{\text{maximum energy stored at } f_0}{\text{total energy lost per cycle at } f_0} = 2\pi \frac{[W_L(\omega_0 t) + w_C(\omega_0 t)]_{\text{max}}}{\rho_0 T}
\]

(6.1-3)

The instantaneous energy in the capacitor is

\[
w_C(\omega_0 t) = \frac{1}{2} C v_o^2 = \frac{1}{2} CV_m^2 \sin^2 \omega_0 t
\]

(6.1-4)

where \( v_o \) is the AC output voltage, \( I_m \) is the AC output current amplitude, and \( V_m \) is the output voltage amplitude.

The instantaneous energy in the inductor is

\[
w_L(\omega_0 t) = \frac{1}{2} L i_L^2 = \frac{1}{2} LI_m^2 \cos^2 \omega_0 t = \frac{1}{2} L \left( \frac{V_m}{\omega_0 L} \right)^2 \cos^2 \omega_0 t
\]

\[
= \frac{1}{2} CV_m^2 \cos^2 \omega_0 t
\]

(6.1-5)

Therefore

\[
Q_L = 2\pi \frac{\frac{1}{2} CV_m^2 (\sin^2 \omega_0 t + \cos^2 \omega_0 t)}{V_m^2 / 2Rf_0} = \omega_0 CR = \frac{R}{Z_0} = \frac{R}{\omega_0 L}.
\]

(6.1-6)
As can be seen in the resulting equation (6.1-6), the driving factors of the tank’s loaded quality factor are the frequency, inductance, and load resistance. The actual Q factor for the tank however will be determined by the lowest Q in the system, which is generally the inductor. In the case of the off-chip tank, the bondwire could have a detrimental effect on the Q if its R and L are not accounted for.

The inductor’s effective Q factor \( Q_{eff} \) is the degree the inductor deviates from an ideal component and is given by [77]:

\[
Q_{eff} = \frac{Im[Z_{in}]}{Re[Z_{in}]} = \frac{X}{R} = \frac{\omega L_e}{R}
\]  

(6.1-7)

where \( L_e \) is the effective inductance of the inductor, which is generally greater than the nominal specified value below the inductor’s self-resonance frequency [78]. The self-resonance frequency is the frequency at which the inductive reactance and the parasitic capacitive reactance become equal and opposite in sign. Beyond this point the inductor becomes capacitive. From (6.1-7) this is when \( Q_{eff} \) is equal to 0.

To compute the effect the Q-factor has on the bandwidth of the operation of the Class A amplifier, continue solving after (6.1-6) as follows:

The phasor of the output voltage is

\[
V_o = -ZI_s = -\frac{I_s}{Y}
\]  

(6.1-8)

where \( I_s \) is the current provided by the power supply.

The admittance of the circuit is

118
\[ Y = \frac{I_d}{V_o} = \frac{1}{R} + j \left( \omega C - \frac{1}{\omega L} \right) = \frac{1}{R} \left[ 1 + jQ_L \left( \frac{\omega}{\omega_0} - \frac{\omega_0}{\omega} \right) \right] = |Y|e^{j\phi_y} \] (6.1-9)

with
\[ |Y| = \frac{1}{R} \sqrt{1 + Q_L^2 \left( \frac{\omega}{\omega_0} - \frac{\omega_0}{\omega} \right)^2} \] (6.1-10)

and
\[ \phi_y = \frac{1}{R} \arctan \left[ Q_L \left( \frac{\omega}{\omega_0} - \frac{\omega_0}{\omega} \right) \right]. \] (6.1-11)

The impedance of the circuit is
\[ Z = \frac{1}{Y} = \frac{V_o}{I_d} = \frac{1}{R} + j \left( \omega C - \frac{1}{\omega L} \right)^{-1} = \frac{1}{R} \left[ 1 + jQ_L \left( \frac{\omega}{\omega_0} - \frac{\omega_0}{\omega} \right) \right]^{-1} = |Z|e^{j\phi_z} \] (6.1-12)

where
\[ |Z| = \frac{R}{1 + Q_L^2 \left( \frac{\omega}{\omega_0} - \frac{\omega_0}{\omega} \right)^2} \] (6.1-13)

and
\[ \phi_z = -\arctan \left[ Q_L \left( \frac{\omega}{\omega_0} - \frac{\omega_0}{\omega} \right) \right]. \] (6.1-14)

The normalized input impedance \( \frac{|Z|}{R} \) and phase \( \phi_Z \) will determine the 3 dB point, which is
\[
\frac{|Z|}{R} = \frac{1}{\sqrt{2}}
\]  

(6.1-15)

giving

\[
Q_L \left( \frac{\omega}{\omega_0} - \frac{\omega_0}{\omega} \right) = -1
\]  

(6.1-16)

and

\[
Q_L \left( \frac{\omega}{\omega_0} - \frac{\omega_0}{\omega} \right) = 1.
\]  

(6.1-17)

the lower 3 dB frequency is

\[
f_L = f_0 \left[ \sqrt{1 + \left( \frac{1}{2Q_L} \right)^2} - \frac{1}{2Q_L} \right]
\]  

(6.1-18)

and the upper 3 dB frequency is

\[
f_H = f_0 \left[ \sqrt{1 + \left( \frac{1}{2Q_L} \right)^2} + \frac{1}{2Q_L} \right].
\]  

(6.1-19)

so the 3 dB bandwidth of the LC tank is:

\[
BW = f_H - f_L = \frac{f_0}{Q_L}.
\]  

(6.1-20)

Taking equations (6.1-13) and (6.1-14) and plotting them yields the curved graphs of the normalized magnitude of the impedance and the phase of the input frequency respectively. These can be viewed in for various Q’s in Figure 6.1.2.2. In the impedance graph, the reference impedance is 50\(\Omega\).
It can be seen from (6.1-20) that the Q-factor of the resonant circuit which is driven by the Q-factor of the inductor will determine the bandwidth, and therefore selectivity of the filter. This will impact the noise figure of the circuit as the more selective the circuit, the fewer undesired signals will be driven onto the load.

### 6.1.3 LC Passive Filter Simulation

To determine how Q-factors and bondwires affect circuit operation various simulations are given with Q factors varying from 1, 9, 17, 25, and 33 both with and without bondwires. The Q of 9 is representative of what can be found currently in an integrated inductor (Table 6.1.1) while the Q of 25 and 33 can be found in an off chip inductor (Figure 5.3.5.2). The bondwire used was an ADS model which was a free-
floating bondwire (not above a plane) of 12.5 μm radius and 2 mm length. The bondwires were attached between the output voltage and ground nodes of the LC tank. The attachment through ground was due to the fact that on any setup there would be an interconnect between the ground of the on-die circuit and the off-chip tank. The filter was designed for operation at 2 GHz.

Figure 6.1.3.1 shows an AC sweep of the filter’s output at 2 GHz. The higher the Q, the higher the peak of the output amplitude and the more narrow the bandwidth. The on-die configuration with a Q of 37 has a 3 dB bandwidth of approximately 450 MHz while the off-die configuration has a bandwidth of around 520 MHz. The on-die filter has a symmetrical bandwidth while the devices attached with bondwires have an asymmetrical bandwidth with a low slope on the low frequency side and a high slope on the high frequency side. Since the goal of a band pass filter is to pass frequencies in a certain band while attenuating others, the high Q on-die devices are the preferred solution for these simulations.
Figure 6.1.3.1 - Effect of Q Factor on AC Peaking

Figure 6.1.3.2 shows the Q values vs. noise figure. The noise figure decreases with the higher Q values which is expected. The external circuit also exhibits a noise figure spike in frequencies above 2 GHz. At the frequency of interest, the best noise figure achieved is through the high-Q on-die inductor.
Figure 6.1.3.2 - Filter Figure with Various Q Values

The transient simulation results in Figure 6.1.3.3 show once again that the Q results in a higher signal on the output of the filter at 2GHz. As expected, the bondwire attached tank has a slightly lower amplitude than the on-die tank.
6.2 Physical Testing

6.2.1 Test Fixture & Setup

To test the direct attach approach of circuit attachment, a test fixture was made with the filter DUT. For the filter, a 5.0 pF capacitor and 0.4 nH inductor (TDK part number MLG0603SON4CT) were used. The inductor has a minimum Q of 34 at 2.4 GHz [64]. This filter was simulated with TDK inductor and capacitor models to peak at 2.74 GHz. The actual peak frequency was calculated to be 3.56 GHz using (6.1-1), however the
parasitics in the capacitor and inductor affect the final filter frequency. These parasitics are accounted for in the TDK model. See section 5.1 for more information on capacitor modeling. A photograph of the test fixture is shown in Figure 6.2.1.1. The fixture was attached to a 2 port Agilent E8362 VNA and a frequency sweep performed as shown in Figure 6.2.1.2.

![LC Filter test fixture](image)

*Figure 6.2.1.1. LC Filter test fixture.*
To analyze the performance of the tank, it needs a some benchmark performance references. First, to verify the proper peaking frequency, the TDK reference model was created. The TDK reference was used to verify the correct position of the LC tank’s peak frequency. Second, as a comparison, an ideal tank model was created which uses an ideal inductor with adjustable Q-factor and ideal capacitor. Before simulation, the capacitor’s value was adjusted to 8.3 pF in order to provide the proper peaking frequency for the ideal tank. The circuit with adjustable Q-factor allows a rough estimation of integrated inductors with various Q’s such as those listed in Table 6.1.1. The ADS circuit used, which applies to both references is shown in Figure 6.2.2.1.

Figure 6.2.1.2. Filter test fixture setup with VNA.

6.2.2 Test Results
The circuit was simulated through AC analysis. The test data was s2p Touchstone data format which ADS readily accepts and uses for simulation. The output of the two models and the test fixture is shown in Figure 6.2.2.2. Figure 6.2.2.2 (a) shows the broadband sweep while Figure 6.2.2.2 (b) shows the zoom in of the peaking area. Figure 6.2.2.2 reveals the measured results have tighter rolloffs than either of the references, which according to (6.1-20) results in a better $Q$-factor for that LC tank. Test results with a several $Q$-factors for the tank inductor are given in Table 6.2.1. From Table 6.2.1 it can be seen that the LC test fixture exhibits a higher LC $Q$ than either the ideal model or the TDK based model. $Q$-value calculations in Table 6.2.1 are based on (6.1-20) and taken from waveform measurement at the -3 dB dropoff point from the peak $f_c$ of the tank being analyzed.
Figure 6.2.2.2. LC Tank test results (a) broadband and (b) narrowband detail.
### Table 6.2.1. LC Tank Fixture Test Results.

<table>
<thead>
<tr>
<th>Device</th>
<th>Bandwidth (MHz)</th>
<th>Tank Q-Factor</th>
<th>Peak Frequency (GHz)</th>
<th>Magnitude at Peak (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test fixture</td>
<td>472</td>
<td>5.84</td>
<td>2.76</td>
<td>-6.92</td>
</tr>
<tr>
<td>ADS Sim w/ TDK Models</td>
<td>502</td>
<td>5.46</td>
<td>2.74</td>
<td>-8.42</td>
</tr>
<tr>
<td>ADS Sim w/ideal models (Q=5)</td>
<td>791</td>
<td>3.5</td>
<td>2.77</td>
<td>-6.28</td>
</tr>
<tr>
<td>ADS Sim w/ideal models (Q=15)</td>
<td>779</td>
<td>3.55</td>
<td>2.76</td>
<td>-6.13</td>
</tr>
<tr>
<td>ADS Sim w/ideal models (Q=25)</td>
<td>773</td>
<td>3.57</td>
<td>2.76</td>
<td>-6.10</td>
</tr>
<tr>
<td>ADS Sim w/ideal models (Q=50)</td>
<td>773</td>
<td>3.57</td>
<td>2.76</td>
<td>-6.08</td>
</tr>
</tbody>
</table>

### 6.3 Chapter Summary

In this chapter, a concept for directly attaching a high Q-factor passive inductor to an IC die is presented. Using this technique, a higher Q inductor can be realized than can be done through traditional fabrication methods. A test LC tank was fabricated and tested using a high-Q inductor and the results compared to simulated inductors with lower Q-factors. The on-die solution is shown to have a higher LC Q-factor than the competing simulated models which are representative of what integrated inductor technology is currently available on the commercial market.
7 Summary, Contributions, and Future Work

7.1 Summary

This research has focused on making improvements to and overcoming the limitations of bondwire interconnections in IC packaging. In order to provide background information a summary of IC, packaging, and PCB technology was presented as well as an overview of some of the measurement techniques used throughout this work. In addition to the background information, four chapters are present which contain the contributions of this dissertation.

7.2 Contributions

7.2.1 Bondwire Modeling

Given that bondwires are used as part of circuits and interconnects, modeling and simulation of bondwire effects on performance is an important part of designing high frequency integrated circuits. If an IC uses bondwires as part of the package, the bondwire can affect the device’s operation. Modeling the full interconnection allows the
designer to offset the effects of the bondwires, predict final circuit operation, and find optimal wire geometries which will have the smallest impact on circuit operation.

Specifically, these are the contributions of the first objective:

- Developed lumped element model for bondwires of various shapes and configurations
  - Curved wires
  - Wires with angles to ground plane
  - Arbitrary number of wires
  - Wires at angles to each other
- Model implementable in standard circuit simulators
- Model proved to have lower error measurements than ADS PBOND and Momentum software models
- Model is not a “black box”
  - Makes compensation for the wire possible in objective 2
  - Lumped element output more versatile than “black box” output of some high end simulators

7.2.2 Bondwire Compensation

If a wire with an arbitrary geometry is to interface to a controlled impedance line a discontinuity will result. The method presented in this dissertation is a means of compensating for the impedance mismatch between the bondwire and the transmission line. The impact of bondwires can be severe and $S_{21}$ losses of greater than 3 dB above 4
GHz are demonstrated in this document. As a solution to this loss, this dissertation presents a circuit to be implemented as part of a packaged device’s input output (IO) path. This circuit uses the bondwire’s inductance combined with other lumped elements to create an impedance matching network.

The contributions of the second objective are as follows:

- Developed a compensation method for performance degradation caused by bondwires at RF through the use of impedance matching techniques
- Current techniques require a custom layout of the bondwire to obtain the desired bondwire transmission line characteristics
- Static and dynamic capacitors have been proposed, but not implemented
- The method presented may be adjusted post fabrication
- Demonstrated performance improvement up to 5.5 GHz

7.2.3 PDN Improvement

The PDN of a system can influence key performance parameters of devices present. High speed clocks and switching regulators can cause unwanted noise on a PDN, resulting in degraded device performance.

The contributions of objective 3 are as follows:

- Developed PDN improvement method useful for the 1-100 MHz domain through passive capacitor stacking
- Method shown to improve rejection of noise from 10-100MHz by 30 dBm
Currently off-package decoupling has limited effectiveness above 10’s of MHz

On-chip decoupling has smaller devices and therefore is limited to frequencies above 100 MHz

7.2.4 Filter Improvement

Inductors and capacitors are commonly used in RF circuits such as low noise amplifiers (LNAs), power amplifiers, and voltage controlled oscillators (VCOs) to create a bandpass filter known as an LC tank. The Q-factor of the inductor will determine the filter’s bandwidth as the inductor generally has the lowest Q in the system. In contrast to integrated inductors which exist as part of the die, surface mount inductors are commonly available in a package that will comfortably fit onto the top of a die. Attaching the inductor to the die saves real-estate while increasing device performance.

The contributions of the fourth objective are:

- Developed a method of inductor attachment which allows for a high Q-factor inductor to be attached directly to a die, circumventing bondwires and avoiding the use of low-Q integrated inductors
- This approach eliminates the need for complicated structures, exotic materials, or interconnecting bondwires to improve inductor performance
- Used to provide superior Q-factor inductor(s) when compared to integrated or off chip inductor solutions
  - Traditional integrated inductors have Q’ in the range of 15
SMT inductors can have Q’s above 50

7.3 Future Work

7.3.1 Bondwire Modeling

The bondwire models presented in this work cover several shapes, but only one is validated in test. A second test fixture implementing the PBONDW shape could be fabricated and tested. In addition to testing the second shape, a test case where cross talk between signal lines is modeled and tested would be of great benefit. This can be performed with a VNA and checked with Agilent ADS or similar software. Instead of the aggressor wires being attached to ground on the fixture, they would need to be attached to a transmission line and SMA connector. Two port measurements may be used to check induced signals between adjacent wires. Test fixtures that create bondwires on the scale of a typical wire bond BGA package could also be created to further validate the models.

7.3.2 Bondwire Compensation

The bondwire compensation techniques mentioned in this dissertation have several areas of improvement available. Further measurements involving bit error rate testing (BERT) and associated measurements could be taken to further validate bondwire improvement. IC scale test fixtures could be fabricated in order to validate the size scalability of the technique.

7.3.3 PDN Improvement

The PDN improvement approach has several open areas of improvement. First a means of manufacturing the completed IC with attached capacitors in an automated
fashion could be devised. The PDN could also be tested on a fabricated IC that would likely be affected by a degraded PDN such as an ADC or DAC. These types of devices can be quantified by their estimated number of bits (ENOB) which would give the tester an idea of the improvement gained by the additional PDN decoupling.

7.3.4 Filter Improvement

Filter improvement can be tested by designing and fabricating a device that supports the filter components attached to the die as well as to IO pads leading to an off-die set of filter components. Like the PDN improvement method, the filter improvement approach also needs a method of repeated manufacturing if it is to leave the realm of hand assembled, low-volume specialty parts. The approach also needs further verification through simulation of an active circuit which uses either an on-die inductor or an integrated inductor.
8 Appendix: MATLAB Code

8.1 Introduction

This section contains a printout of the major Matlab code developed during the course of this project. This may be used to replicate results listed in this document. The code is divided into sections by the application and the function or script name.

8.2 Bondwire Modeling

These functions were used to generate the bondwire models used in this dissertation.

8.2.1 Circular Bondwire Calculator

Used to generate lumped element values for the circular bondwires.

```matlab
clear
disp('Circular bondwire calculator original soln');
neigh = 1;
n=22;
for n=12:1:12;
    % microns to meters
    len = 3.14e-3
    rad =31.8e-6;
    alpha=15;
    % convert angles to radians
    alpha = alpha/180 * pi;
    distance = 1.524e-3;
    s = distance;
    delta = pi/(n); % step size
```
height = 1e-3; %height (1mm)
%disp( ['Wire height: ' num2str(height) ' (m) Length: ' num2str(len) ' (m) ']);
%disp(['ro delta is: ' num2str(delta) ' with ' num2str(n) ' slices']);
lenprime=len/(n); %slice size
hrogers = 508e-6; %Rogers 4030b dielectric height
erogers = 4; %Rogers 4030b dielectric constant
c = 2.997935e8;
%urogers = 1/(erogers*c); %Rogers permeability
urogers = 1; %Rogers RELATIVE permeability
ur = 1;
eair = 1; uair = 4*pi*1e-7; %air permeability
u0 = 4*pi*1e-7; %permeability of free space
e0 = 1e-9/(36*pi); %dielectric constant of q in a vacuum
A = 1e-3 * 1e-3; %IO pad size in square m
%disp( ['number of slices:' num2str(n)]);
L = 0;
templen = 0;
tempdelt = 0;
iter = 0;
for ro=delta/2:delta:(pi);
    if ( abs(ro-pi/2) < .001 )
        h = height;
        FF = hrogers/(h + hrogers);
        %ur = (urogers*(FF) + uair*(1-FF))/u0;
        mu = (u0*ur)/(2*pi);
        current = mu*log((2*(h + hrogers))/rad)*lenprime;
    elseif ( ro == 0 || ro == pi )
        h = 0;
        FF = hrogers/(h + hrogers);
        %ur = (urogers*(FF) + uair*(1-FF))/u0;
        mu = (u0*ur)/(2*pi);
        current = mu*log((2*(h + hrogers))/rad)*lenprime;
    else
        h = sin(ro)*height;
        FF = hrogers/(h + hrogers);
        %ur = (urogers*(FF) + uair*(1-FF))/u0;
        mu = (u0*ur)/(2*pi);
        current = mu*log((2*(abs(tan(ro))*h + hrogers))/rad)*lenprime;
    end;
    %disp( [num2str( mu ) ' ' num2str(FF) ' ' num2str(ur )]);
    templen = templen + lenprime;
    L = L + current;
%disp([ num2str(iter) ' ro ' num2str(ro) ' height ' num2str(h) ' current ' num2str(current) ' : ' num2str(L) ' H : ' num2str(ur) ' corrected ur']);
iter = iter + 1;
if (2*abs(sin(pi/n))*(h)) < rad
    disp('Warning: 2h is smaller than wire radius - results may not be correct');
end;
disp(['L for bond wire w/mixed dielectric: ' num2str(L) ' H' ' number of slices:' num2str(n)]);
s = distance;
for i=0:neigh;
    lm = 0;
    for ro=delta/2:delta:(pi);
        sep = tan(alpha)*ro*1e-3 + s;
        if(abs(ro-pi/2) < .00001)
            h = height;%h is hypotenuse (1mm ht)
            FF = hrogers/(h + hrogers);
            %ur = (urogers*(FF) + uair*(1-FF))/u0;
            mu = (u0*ur)/(4*pi);
            current = mu*log(1 + (2*(h + hrogers)/(sep))^2)*lenprime;
        elseif(ro == 0 || ro == pi)
            h = 0;%h is hypotenuse (1mm ht)
            FF = hrogers/(h + hrogers);
            %ur = (urogers*(FF) + uair*(1-FF))/u0;
            mu = (u0*ur)/(4*pi);
            current = mu*log(1 + (2*(h + hrogers)/(sep))^2)*lenprime;
        else
            h = sin(ro)*height;%h is hypotenuse (1mm ht)
            FF = hrogers/(h + hrogers);
            %ur = (urogers*(FF) + uair*(1-FF))/u0;
            mu = (u0*ur)/(4*pi);
            current = mu*log(1 + (2*(abs(tan(ro))*h + hrogers)/(sep))^2)*lenprime;
        end;
        lm = lm + current;
    end;
s = s + distance;
disp(['Lm for neighbor ' num2str(i) ' with distance ' num2str(s - distance) ' : ' num2str(lm) ' H' ' sep:' num2str(sep)]);
end;
C = 0;
for ro=delta/2:delta:(pi);
    if(abs(ro-pi/2) < .00001)
        h = height;
FF = hrogers/(h + hrogers);
er = (erogers*(FF) + eair*(1-FF));
current = (2*pi*e0*er)/log(2*(h + hrogers)/rad)*lenprime;
elseif( ro == 0 || ro == pi )
h = 0;
FF = hrogers/(h + hrogers);
er = (erogers*(FF) + eair*(1-FF));
current = (2*pi*e0*er)/log(2*(h + hrogers)/rad)*lenprime;
else
h = sin(ro)*height;
FF = hrogers/(h + hrogers);
er = (erogers*(FF) + eair*(1-FF));
current = (2*pi*e0*er)/log(2*(abs(tan(ro))*h + hrogers)/rad)*lenprime;
end ;
%disp( num2str(current));
end;
C = C + current;
end;
disp( ['C for bond wire: ' num2str(C) ' F']);

s = distance;%wire pitch (increments in loop)
for i=0:neigh;
    Cm = 0;
    sep = ro*1e-3*tan(alpha)*2/pi + s;
    for ro=delta/2:delta:(pi);
        sep = tan(alpha)*ro*1e-3 + s;
        if( abs(ro-pi/2) < .00001 )
            h = height;
            FF = hrogers/(h + hrogers);
            er = (erogers*(FF) + eair*(1-FF));
            current = (pi*e0*er*log(1+(2*(h + hrogers)/(sep))^2))/(log(2*(h + hrogers)/rad)^2)*lenprime;
            elseif( ro == 0 || ro == pi )
                h = 0;
                FF = hrogers/(h + hrogers);
                er = (erogers*(FF) + eair*(1-FF));
                current = (pi*e0*er*log(1+(2*(h + hrogers)/(sep))^2))/(log(2*(h + hrogers)/rad)^2)*lenprime;
            else
                h = sin(ro)*height;
                FF = hrogers/(h + hrogers);
                er = (erogers*(FF) + eair*(1-FF));
                current = (pi*e0*er*log(1+(2*(abs(tan(ro))*h + hrogers)/(sep))^2))/(log(2*(abs(tan(ro))*h + hrogers)/rad)^2)*lenprime;
            end;
        Cm = Cm + current;
    %disp( ['Cm for neighbor ' num2str(i) ' with distance ' num2str(s - distance) ' : ' num2str(Cm) ' pF'] );
    end;
s = s + distance;
disp( ['Cm for neighbor ' num2str(i) ' with distance ' num2str(s - distance) ' : ' num2str(Cm) ' F'] );
8.2.2 BONDW Calculator

Generates values for lumped elements used in the PBOND model.

clc;
clear;
disp('Triangle bondwire calculator');

%constants
hrogers = 508e-6; %Rogers 4030b dielectric height
erogers = 4; %Rogers 4030b dielectric constant
e0 = 1e-9/(36*pi); %dielectric constant of q in a vacuum
t = hrogers;
x1 = 0;
y1 = 0;
x2 = 200e-6;
y2 = 1e-3;
x3 = 400e-6;
y3 = 1e-3;
x4 = 1e-3;
y4 = 0;

neigh = 4; %#neighbors (symmetrical)
n=14; %#segments
rad =3.8e-6; %wire radius
alpha=15; %separation angle (degrees)
alpha = alpha/180 * pi; %convert angles to radians
distance = 200e-6; %initial separation distance between wires (start)

% make picture
xplot = [x1,x2,x3,x4];
yplot = [y1,y2,y3,y4];
plot(xplot,yplot, 'r', 'LineWidth', 2);
hold on;
% if neighbors
angle = alpha;
for j=1:neigh;
    zplot = [distance*j,distance*j+tan(angle)*x2,distance*j+tan(angle)*x3,distance*j+tan(angle)*x4,];
    plot3(xplot,yplot,zplot, 'b', 'LineWidth', 2);
    plot3(xplot,yplot,-zplot, 'b', 'LineWidth', 2);
    angle = angle + alpha;
end
plot([0,x4],[-t,-t],'k');
axis([x1-1e-3 x4+1e-3 y1-1e-3 y3+1e-3]);

az = 180;
el = -60;
view(az, el);

A = 1e-3 * 1e-3; % IO pad size in square m

% first triangle
[L1,Lm1,C1,Cm1] = angle_calc(x1, x2, y1, y2, neigh, alpha, distance, rad,n);
% second triangle (or straight line)
[L2,Lm2,C2,Cm2] = angle_calc(x2, x3, y2, y3, neigh, alpha, distance, rad,n);
% third triangle (reversed)
[L3,Lm3,C3,Cm3] = angle_calc(x3, x4, y3, y4, neigh, alpha, distance, rad,n);
% total all stuff
\[
\begin{align*}
L &= L_1 + L_2 + L_3; \\
L_m &= L_{m1} + L_{m2} + L_{m3}; \\
C &= C_1 + C_2 + C_3; \\
C_m &= C_{m1} + C_{m2} + C_{m3}; \\
\end{align*}
\]

\[
\text{disp( } ['L: ' num2str(L) ' H'])\;
\text{for } j=1:n;\;
\quad \text{disp([ 'Lm: ' num2str(j) ': ' num2str(Lm(j)) ' H'])};\;
\text{end}\;
\text{disp(num2str(L1))}\;
\text{disp(num2str(L2))}\;
\text{disp(num2str(L3))}\;
\text{disp( } ['C: ' num2str(C) ' F'])\;
\text{for } j=1:n;\;
\quad \text{disp([ 'Cm' num2str(j) ': ' num2str(Cm(j)) ' F'])};\;
\text{end}\;
\]

\[
\text{Cio} = \text{erogers}\text{e0}\text{A}/\text{hrogers};
\]

\[
\text{disp( } ['C for IO pad: ' num2str(Cio) ' F'])\;
\]

#### 8.2.3 Angled Wire Calculator

Generates lumped element values for wires at an angle of a ground plane.

\[
\%\text{Angled bondwire calculations...}
\text{function } [L,Lm,C,Cm] = \text{angle_calc}(x1, x2, y1, y2, neigh, alpha, distance, rad,n)\;
\%\text{constants}
\text{hrogers} = 508e-6; \%\text{Rogers 4030b dielectric height}
\text{erogers} = 4; \%\text{Rogers 4030b dielectric constant}
\text{c} = 2.997935e8;
\%\text{urogers} = 1/(erogers*c);\%\text{Rogers permeability}
\text{urogers} = 1; \%\text{Rogers RELATIVE permeability (same as air...)}
\text{ur} = 1;
\text{eair} = 1;
\text{uair} = 4*pi*1e-7; \%\text{air permeability}
\text{u0} = 4*pi*1e-7; \%\text{permeability of free space}
\text{e0} = 1e-9/(36*pi); \%\text{dielectric constant of q in a vacuum}
\]

\[
\begin{align*}
L &= 0; \\
C &= 0; \\
L_m &= \text{zeros}(\text{neigh}); \\
C_m &= \text{zeros}(\text{neigh}); \\
\text{if ( } y2 < y1 \text{ )}\;
\quad \text{temp} = y2; \\
\quad y2 = y1; \\
\end{align*}
\]

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\[ y_1 = \text{temp}; \]

\[
\text{end;}
\]

\[
\text{for } j=0:\text{neigh;}
\]
\[
\text{for } i=1:1:n;
\]
\[
\text{hyp} = \sqrt{(x_2-x_1)^2+(y_2-y_1)^2};
\]
\[
\text{lprime} = \text{hyp}/n;
\]
\[
\text{ro} = i*\text{lprime}-1/2*\text{lprime};
\]
\[
\text{theta} = \arctan((y_2-y_1)/(x_2-x_1));
\]
\[
\text{h} = \sin(\text{theta})*(\text{ro});
\]
\[
\text{sep} = \tan(\alpha)*(\text{ro})+(\text{distance}*j);
\]
\[
\% \text{L calculations...}
\]
\[
\text{FF} = \text{hrogers}/(h + \text{hrogers});
\]
\[
\text{ur} = (\text{urogers}*(\text{FF}) + \text{uair}*(1-\text{FF}))/\text{u0;}
\]
\[
\text{if}(j == 0) \% \text{primary wire}
\]
\[
\text{mu} = (\text{u0} * \text{ur})/(2*\pi);
\]
\[
\text{if} ( (y_2 - y_1) < \text{rad} )
\]
\[
\text{L} = \text{mu*log}(2*(y_1+\text{hrogers})/\text{rad})*(x_2-x_1);
\]
\[
\% \text{disp}(['L for line: ' num2str(L) ' H']);
\]
\[
\text{else}
\]
\[
\text{current} = \text{mu*log(2*(h+\text{hrogers})/\text{rad})*lprime;}
\]
\[
\text{L} = \text{L} + \text{current;}
\]
\[
\text{end}
\]
\[
\text{end}
\]
\[
\text{else} \% \text{neighbors } (\text{lm})
\]
\[
\text{mu} = (\text{u0} * \text{ur})/(4*\pi);
\]
\[
\text{if} ( (y_2 - y_1) < \text{rad} )
\]
\[
\text{Lm(j)} = \text{mu*log}(1 + (2*(y_1 + \text{hrogers})/(\text{sep}))^2)*(x_2-x_1);
\]
\[
\text{else}
\]
\[
\text{current} = \text{mu*log(1 + (2*(h + \text{hrogers})/(\text{sep}))^2)*lprime;}
\]
\[
\text{Lm(j)} = \text{Lm(j)} + \text{current;}
\]
\[
\text{end}
\]
\[
\text{end}
\]
\[
\% \text{C calculations}
\]
\[
\text{er} = (\text{erogers}*(\text{FF}) + \text{eair}*(1-\text{FF}));
\]
\[
\text{if}(j == 0)
\]
\[
\text{if} ( (y_2 - y_1) < \text{rad} )
\]
\[
\text{C} = (2*\pi*\text{e0})*\text{er}/\log(2*(y_1 + \text{hrogers})/\text{rad})*(x_2-x_1);
\]
\[
\text{else}
\]
\[
\text{current} = (2*\pi*\text{e0})*\text{er}/\log(2*(h + \text{hrogers})/\text{rad})*\text{lprime;}
\]
\[
\text{C} = \text{C} + \text{current;}
\]
\[
\text{end}
\]
\[
\text{else}
\]
\[
\text{if} ( (y_2 - y_1) < \text{rad} )
\]
\[
\text{Cm(j)} = (\pi*\text{e0})*\text{er}*(\log(1+(2*(y_1 + \text{hrogers})/\text{sep})^2))/(\log(2*(y_1 + \text{hrogers})/\text{rad})^2)*(x_2-x_1);
\]
\[
\text{else}
\]
\[
\text{end}
\]
current = (pi*e0*er*log(1+(2*(h + hrogers)/sep)^2))/(log(2*(h + hrogers)/rad)^2)*lprime;
Cm(j) = Cm(j) + current;
end;
%disp(["Sep ", num2str(sep), ", ", num2str(j), ", ", current ", num2str(current), ", cm ", num2str(Cm(j))]);
end;
end;
%disp(num2str(h/2));
if ( (h/2) < rad ) 
if ( (rad - y1) > rad )
disp('Warning: h/2 is smaller than wire radius - results may not be correct');
end;
end;
disp(["C ", num2str(C), ", Cm ", num2str(Cm(1))]);
end;

8.3 Bondwire Compensation

The code in this section was used to create

8.3.1 LCC Model Creator and Plotter

This script creates a model for the LCC compensation and plots results including external test results.

c1c;
calculations_lc;
x_lc = x;
clear x mldb;
%clear;
start = .1;
inc = .1;
final = 10;
count = 1;
c = .2; %capacitance in pF
l = 1; %inductance in nH
cs = 1e-13; %self capacitance
rwire = .01; %bondwire self resistance
dpath = 'C:\data';
for k = start:inc:final
f = k*1e9;
w = 2*pi*f*1;
zs = 50;
z0 = 50;
% R
b0 = [1, -rwire; 0, 1];
% L1
l1 = 2.9e-9;
b1 = [1, -w*l1; 0 1];
% C shunt (cs)
c1 = cs;
b2 = [1,0;-w*c1,1];
% C2 series
C2 = c*1e-12;
b3 = [1,1/(-w*c2);0,1];

Z0=z0;
% R = 1.68e-8/(.036e-3*1.09e-3); % no skin effect (RDC=p*1/A)
% with skin effect....
ro = 1.68e-8;
sigma = (1/ro);
u0=pi*4e-7;
skin_d=1/sqrt(pi*sigma*0.999994*f*u0);
skin_a=(.036e-3 + 1.09e-3)*skin_d*2;
if (skin_a > .036e-3*1.09e-3)
    R = 1.68e-8/(.036e-3*1.09e-3); % no skin effect (RDC=p*1/A)
else
    R=ro/(skin_a);
end;

 _microstrip
% http://www.ece.rutgers.edu/~orfanidi/ewa/ch10.pdf   p.417
C = 1.09e-10;
length_cable = 9.7e-3; % 9.7mm
ww=f.*2.*pi;
L=Z0^2*C; % inductance per meter
Gamma= sqrt((R+1i.*ww.*L).*(1i.*ww.*C)); % Gamma assuming G=0
Z0=sqrt((R+1i.*ww.*L)./(1i.*ww.*C)); % Complex Z0
% Now fill in the matrix equations
A=cosh(gamma.*length_cable);
B=Z0.*sinh(gamma.*length_cable);
C=1./Z0.*sinh(gamma.*length_cable);
D=cosh(gamma.*length_cable);
b4 = inv([ A, B;C,D]);
DL=inv(b4*b3*b2*b1*b0*b4);
% DL=inv((b3*b2*b1*b0));
% Now to Z-parameters
A = DL(1,1);
B = DL(1,2);
C = DL(2,1);
D = DL(2,2);

z11 = A/C;
z12 = (A*D-B*C)/C;
z21 = 1/C;
z22 = D/C;

zin = z11 - (z12*z21)/(z22 + z1);
zout = z22 - (z12*z21)/(z11 + zs);
points(count) = abs(zin);
pointsout(count) = abs(zout);

ds = (z11 +z0)*(z22+z0)-(z12*z21);
s22(count) = ((z11+z0)*(z22-z0)-(z12*z21))/ds;
s21(count) = 2*z0*z21/ds;
s12(count) = 2*z0*z12/ds;
s11(count) = ((z11-z0)*(z22+z0)-z12*z21)/ds;

count = count + 1;
end

zsmat = repmat(zs,1,count-1);
x = start*1e9:inc*1e9:final*1e9;
figure('Color',[1 1 1]);
%subplot(2,2,1);
plot(x,abs(points));
hold on;
plot(x,zsmat,':k');
title('LCC Tee Network Zin vs. Frequency');
ylabel('Impedance (Magnitude)');
xlabel('Frequency (Hz)');
axis([.1e9 10e9 0 150]);
legend('Calculated', 'Zs', 'Location', 'SE');
hold off;

%bsx fun is funky...
for k=1:count-1
    gamma(k) = (points(k) - zsmat)/(points(k) + zsmat);
end

for k=1:count-1
    mldb(k) = -10*log10(1-abs(gamma(k))^2);
end
%figure(2);
%subplot(2,2,2); plot(x,mldb);
title('LCC Tee MisMatch Loss vs. Frequency');
ylabel('Mismatch Loss (dB)');
xlabel('Frequency (Hz)');

%----------------------------------------------------------

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%%%S11
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% for k=1:count-1
%     s11(k) = 20*log10(abs(gamma(k)));
%     s11(k) = 20*log10(gamma(k));
%     s11(k) = 20*log10(abs(s11(k)));
% end;
% subplot(2,2,3);
% subplot([dpath,'\PhD\test results\2013-02-20\1.s2p'], '-rx', 1, 1);
% subplot([dpath,'\PhD\test results\2013-02-20\3.s2p'], '-b', 1, 1);
% subplot([dpath,'\PhD\test results\2013-02-20\4.s2p'], '-g', 1, 1);
% subplot([dpath,'\PhD\test results\2013-02-20\5.s2p'], '-m', 1, 1);
% subplot([dpath,'\PhD\test results\2013-02-20\6.s2p'], '-k', 1, 1);
% plot(x,20*log10(abs(s11)), ':k');
% plot(x_lc,s11_lc, '-r');
% legend('0.1pF Measured', '0.2pF Measured', '0.3pF Measured', '0.4pF Measured', 'Uncompensated Measured', ['Calculated LCC w/ num2str(c) ' 'pF'], ['Calculated LC w/ num2str(c) ' 'pF'],'Location', 'SE');
% title('S11');
% ylabel('S11 (dB)');
% xlabel('Frequency (Hz)');
% hold off;
% axis([1e9 10e9 -25 0]);

%%%S21
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% for k=1:count-1
%     s21(k) = 20*log10(1-abs(gamma(k)));
%     s21(k) = 20*log10(abs(s21(k)));
% end
% subplot(2,2,4);
s2p_plot([dpath,'\PhD\test results\2013-02-20\1.s2p'], '-rx', 2, 1);
hold on;
s2p_plot([dpath,'\PhD\test results\2013-02-20\3.s2p'], '-b', 2, 1);
s2p_plot([dpath,'\PhD\test results\2013-02-20\4.s2p'], '-g', 2, 1);
s2p_plot([dpath,'\PhD\test results\2013-02-20\5.s2p'], '-m', 2, 1);
s2p_plot([dpath,'\PhD\test results\2013-02-20\6.s2p'], '-k', 2, 1);
plot(x,20*log10(abs(s21)), ':k');
plot(x_lc,s21_lc, '-r');
legend('0.1pF Measured', '0.2pF Measured', '0.3pF Measured', '0.4pF Measured', 'Uncompensated Measured', ['Calculated LCC w/ num2str(c) ' 'pF'], ['Calculated LC w/ num2str(c) ' 'pF'],'Location', 'SE');
title('S21');
ylabel('S21 (dB)');
xlabel('Frequency (GHz)');
hold off;
axis([1e9 10e9 -10 0]);
8.3.2 LCL Model Creator and Plotter

This script creates a model for the LCL compensation and plots results including external

clc;
clear;
start = .1;
inc = .1;
final = 7.5;
count = 1;
c = .5; % capacitance in pF
rwire = .01;
l = 1; % inductance in nH
l1 = 2.9e-9; % bondwire inductance in nH
cs = 1e-13; % self capacitance
dpath = 'C:\data';

for k = start:inc:final
f = k*1e9;
w = 2*pi*f*1i;
z1 = 50;
zs = 50;
z0 = 50;

% R
b0 = [1, -rwire; 0, 1];
% L1
b1 = [1, -w*l1; 0, 1];
% C
cl = c*1e-12+cs;
% L2
b2 = [1,0;-w*c1,1];
% L3
l2 = 1*1e-9;
bb3 = [1, -w*l2; 0, 1];

% R = 1.68e-8/(.036e-3*1.09e-3); % no skin effect (RDC=p*l/A)
% with skin effect....
ro = 1.68e-8;
sigma = (1/ro);
u0=pi*4e-7;
skin_d=1/sqrt(pi*sigma*0.999994*f*u0);
skin_a=(.036e-3 + 1.09e-3)*skin_d*2;
if(skin_a > .036e-3*1.09e-3)
    R = 1.68e-8/(.036e-3*1.09e-3); % no skin effect (RDC=p*l/A)
else
    R=ro/(skin_a);
end;
Z_cable=47.5;
C_cable = 1.068e-10;
length_cable = 9.7e-3; % 9.7mm
ww=f.*Z.*pi;
\begin{verbatim}
L_cable = 2 * cable^{2} * C_cable; \hspace{1em} \text{inductance per meter}
\gamma = \sqrt{(R + 1i.*\omega.*L_cable) \cdot (1i.*\omega.*C_cable)}; \hspace{1em} % Gamma assuming \( G = 0 \)
Z_0 = \sqrt{(R + 1i.*\omega.*L_cable) / (1i.*\omega.*C_cable)}; \hspace{1em} % Complex

\text{Now fill in the matrix equations}
A = \cosh(\gamma \cdot \text{length}_\text{cable});
B = Z_0 \cdot \sinh(\gamma \cdot \text{length}_\text{cable});
C = 1 / Z_0 \cdot \sinh(\gamma \cdot \text{length}_\text{cable});
D = \cosh(\gamma \cdot \text{length}_\text{cable});
b_4 = \text{inv}([A, B; C, D]);
\% b_1 = [1, -50; 0, 1];
DL = \text{inv}(b_4 \cdot b_3 \cdot b_2 \cdot b_1 \cdot b_4);

\% now to \( Z \)-parameters
A = DL(1,1);
B = DL(1,2);
C = DL(2,1);
D = DL(2,2);

z_{11} = A / C;
z_{12} = (A \cdot D - B \cdot C) / C;
z_{21} = 1 / C;
z_{22} = D / C;

zin = z_{11} - (z_{12} \cdot z_{21}) / (z_{22} + z_1);
zout = z_{22} - (z_{12} \cdot z_{21}) / (z_{11} + z_{2});
points(count) = \text{abs}(zin);
pouts(count) = \text{abs}(zout);

ds = (z_{11} + z_0) \cdot (z_{22} + z_0) - (z_{12} \cdot z_{21});
s_{22}(count) = ((z_{11} + z_0) \cdot (z_{22} - z_0) - (z_{12} \cdot z_{21})) / ds;

s_{21}(count) = 2 \cdot z_0 \cdot z_{21} / ds;
\% s_{21}(count) \cdot zin / (z_0 + zin);
s_{12}(count) = 2 \cdot z_0 \cdot z_{12} / ds;
\% s_{12}(count) = ((z_{11} - z_0) \cdot (z_{22} + z_0) - z_{12} \cdot z_{21}) / ds;
\% s_{11}(count) = ((A+B) / 50-C*50-D) / ((A+B) / 50+C*50+D)
s_{11}(count) = (zin-50) / (zin+50);

\text{count} = \text{count} + 1;
end

\% 0.3pF capacitor
\text{count} = 1;
c = .3;
for \text{k} = \text{start} : \text{inc} : \text{final}
f = k*1e9;
w = 2*\pi*f*1i;
z_1 = 50;
z_2 = 50;
\end{verbatim}
\( z_0 = 50; \)
\( \%R \)
\( b_0 = [1, -\text{rwire}; 0, 1]; \)
\( \%L_1 \)
\( b_1 = [1, -w*11; 0, 1]; \)
\( \%C \)
\( c_1 = c*1e-12+cs; \)
\( b_2 = [1, 0; -w*c1, 1]; \)
\( \%L_2 \)
\( l_2 = 1*1e-9; \)
\( b_3 = [1, -w*12; 0, 1]; \)
\[ \]
\( \%R = 1.68e-8/(.036e-3*1.09e-3); \) \( \% \) no skin effect \( (\text{RDC}=p*l/A) \)
\( \% \) with skin effect....
\( \rho_0 = 1.68e-8; \)
\( \sigma = 1/\rho_0; \)
\( u_0 = \pi*4e-7; \)
\( \text{skin}_d = 1/\sqrt{\pi*\sigma*0.999994*f*u_0}; \)
\( \text{skin}_a = (0.036e-3 + 1.09e-3)*\text{skin}_d*2; \)
\( \text{if} \) \( \text{skin}_a < 0.036e-3*1.09e-3) \)
\( R = 1.68e-8/(.036e-3*1.09e-3); \) \( \% \) no skin effect \( (\text{RDC}=p*l/A) \)
\( \text{else} \)
\( R = \rho_0/\text{skin}_a; \)
\( \text{end}; \)
\( \% \) http://www.technick.net/public/code/cp_dpage.php?aiocp_dp=util_pcb_imp
\( \_ \) microstrip
\( Z_{\text{cable}} = 47.5; \)
\( C_{\text{cable}} = 1.068e-10; \)
\( \text{length}_{\text{cable}} = 9.7e-3; \) \( 9.7 \) mm
\( \omega_f = f.*2.*\pi; \)
\( L_{\text{cable}} = Z_{\text{cable}}^2*C_{\text{cable}}; \) \( \% \) inductance per meter
\( \gamma = \sqrt{((R+1i.*\omega_f.*L_{\text{cable}}).*(1i.*\omega_f.*C_{\text{cable}}))}; \) \( \% \) Gamma
\( \text{assuming} \) \( G=0 \)
\( Z_0 = \sqrt{(R+1i.*\omega_f.*L_{\text{cable}})./(1i.*\omega_f.*C_{\text{cable}})}; \) \( \% \) Complex
\( Z_0 \)
\( \% \) Now fill in the matrix equations
\( A = \cosh(\gamma.*\text{length}_{\text{cable}}); \)
\( B = Z_0.*\sinh(\gamma.*\text{length}_{\text{cable}}); \)
\( C = 1./Z_0.*\sinh(\gamma.*\text{length}_{\text{cable}}); \)
\( D = \cosh(\gamma.*\text{length}_{\text{cable}}); \)
\( b_4 = \text{inv}([A, B; C, D]); \)
\( % b_1 = [1, -0; -1/50, 1]; \)
\( \text{DL} = \text{inv}(b_4*b_3*b_2*b_1*b_0*b_4); \)
\( \% \) now to \( Z\)-parameters
\( A = \text{DL}(1, 1); \)
\( B = \text{DL}(1, 2); \)
\( C = \text{DL}(2, 1); \)
\( D = \text{DL}(2, 2); \)
\( z_{11} = A/C; \)
\( z_{12} = (A*D-B*C)/C; \)
\[ z_{21} = \frac{1}{C}; \]
\[ z_{22} = \frac{D}{C}; \]
\[ z_{\text{in}} = z_{11} - \frac{z_{12}z_{21}}{z_{22} + z_{\text{in}}}; \]
\[ z_{\text{out}} = z_{22} - \frac{z_{12}z_{21}}{z_{11} + z_{\text{out}}}; \]
\[ \text{points}_3(\text{count}) = \text{abs}(z_{\text{in}}); \]
\[ \text{points}_{\text{out}}(\text{count}) = \text{abs}(z_{\text{out}}); \]
\[ ds = (z_{11} + z_{0}) (z_{22} + z_{0}) - (z_{12}z_{21}); \]
\[ s_{22,3}(\text{count}) = \frac{(z_{11}z_{0}) (z_{22} - z_{0}) - (z_{12}z_{21})}{ds}; \]
\[ s_{21,3}(\text{count}) = \frac{2z_{0}z_{21}}{ds}; \]
\[ s_{12,3}(\text{count}) = \frac{2z_{0}z_{12}}{ds}; \]
\[ s_{11,3}(\text{count}) = \frac{(z_{11} - z_{0})(z_{22} + z_{0}) - z_{12}z_{21}}{ds}; \]
\[ \text{count} = \text{count} + 1; \]

%%uncompensated
\[ \text{count} = 1; \]
\[ \text{for } k = \text{start:inc:final} \]
\[ f = k \times 1e9; \]
\[ w = 2 \times \pi \times f \times 1i; \]
\[ z_{1} = 50; \]
\[ z_{s} = 50; \]
\[ z_{0} = 50; \]
\[ % \text{R} \]
\[ b_{0} = [1, -\text{rwire}; 0, 1]; \]
\[ % \text{L} \]
\[ b_{1} = [1, -w \times 1i; 0 1]; \]
\[ % \text{C} \]
\[ c_{1} = \text{cs}; \]
\[ b_{2} = [1,0;-w \times c_{1},1]; \]
\[ \]
\[ % R = 1.68e-8/(.036e-3*1.09e-3); \text{ no skin effect (RDC=p*l/A)} \]
\[ % \text{with skin effect....} \]
\[ \text{ro} = 1.68e-8; \]
\[ \sigma = (1/\text{ro}); \]
\[ u_{0} = \pi \times 4e-7; \]
\[ \text{skin}_{\text{d}} = 1/\sqrt{\pi \times \sigma \times 0.999994 \times f \times u_{0}}; \]
\[ \text{skin}_{\text{a}} = (0.036e-3 + 1.09e-3) \times \text{skin}_{\text{d}} \times 2; \]
\[ \text{if}(\text{skin}_{\text{a}} < 0.036e-3*1.09e-3) \]
\[ R = 1.68e-8/(.036e-3*1.09e-3); \text{ no skin effect (RDC=p*l/A)} \]
\[ \text{else} \]
\[ R = \text{ro}/(\text{skin}_{\text{a}}); \]
\[ \text{end}; \]
\[ \text{http://www.technick.net/public/code/cp_dpage.php?aiocp_dp=util_pcb_imp_mic ostrip} \]
\[ Z_{\text{cable}}=47.5; \]
\[ C_{\text{cable}} = 1.068e-10; \]
\[ \text{length}_{\text{cable}} = 9.7e-3; \text{ 9.7mm} \]
\[ \text{ww} = f \cdot 2 \cdot \pi; \]
\[ L_{\text{cable}} = Z_{\text{cable}} \cdot 2 \cdot C_{\text{cable}}; \quad \text{inductance per meter} \]
\[ \gamma = \sqrt{(R + 1i \cdot \text{ww} \cdot L_{\text{cable}}) \cdot (1i \cdot \text{ww} \cdot C_{\text{cable}})}; \quad \text{%Gamma} \]
assuming G=0
\[ Z_0 = \sqrt{(R + 1i \cdot \text{ww} \cdot L_{\text{cable}}) \cdot (1i \cdot \text{ww} \cdot C_{\text{cable}})}; \quad \text{%Complex} \]
\[ Z_0 \]
%Now fill in the matrix equations
\[ A = \cosh(\gamma \cdot \text{length}_\text{cable}); \]
\[ B = Z_0 \cdot \sinh(\gamma \cdot \text{length}_\text{cable}); \]
\[ C = 1 / Z_0 \cdot \sinh(\gamma \cdot \text{length}_\text{cable}); \]
\[ D = \cosh(\gamma \cdot \text{length}_\text{cable}); \]
%RL
%\[ b_0 = \begin{bmatrix} 1 & 0 \\ -1/50 & 1 \end{bmatrix}; \]
\[ b_4 = \text{inv}(\begin{bmatrix} A & B \\ C & D \end{bmatrix}); \]
\[ D_L = \text{inv}(b_4 \cdot b_2 \cdot b_1 \cdot b_0 \cdot b_4); \]
%now to Z-parameters
\[ A = D_L(1,1); \]
\[ B = D_L(1,2); \]
\[ C = D_L(2,1); \]
\[ D = D_L(2,2); \]
\[ z_{11} = A / C; \]
\[ z_{12} = (A \cdot D - B \cdot C) / C; \]
\[ z_{21} = 1 / C; \]
\[ z_{22} = D / C; \]
\[ z_{\text{in}} = z_{11} - (z_{12} \cdot z_{21}) / (z_{22} + z_{11}); \]
\[ z_{\text{out}} = z_{22} - (z_{12} \cdot z_{21}) / (z_{11} + z_{21}); \]
\[ \text{points}_{\text{uc}}(\text{count}) = \text{abs}(z_{\text{in}}); \]
\[ \text{points}_{\text{out}}(\text{uc})(\text{count}) = \text{abs}(z_{\text{out}}); \]
\[ d_s = (z_{11} + z_{0}) \cdot (z_{22} + z_{0}) - (z_{12} \cdot z_{21}); \]
\[ s_{22}_{\text{uc}}(\text{count}) = \frac{(z_{11} + z_{0}) \cdot (z_{22} + z_{0}) - (z_{12} \cdot z_{21})}{d_s}; \]
\[ s_{21}_{\text{uc}}(\text{count}) = \frac{z_{22} \cdot z_{21}}{d_s}; \]
\[ s_{12}_{\text{uc}}(\text{count}) = \frac{z_{12} \cdot z_{0}}{d_s}; \]
\[ s_{11}_{\text{uc}}(\text{count}) = \frac{(z_{11} - z_{0}) \cdot (z_{22} + z_{0}) - z_{12} \cdot z_{21}}{d_s}; \]
\[ \text{count} = \text{count} + 1; \]
end
zsmat = repmat(zs,1,count-1);
x = start*1e9:inc*1e9:final*1e9;
figure('Color',[1 1 1]);
subplot(2,2,1);
plot(x,abs(points));
hold on;
plot(x,abs(points_3), '-r');
plot(x,abs(points_{uc}), '-m');
plot(x,zsmat, ':k');
title('Tee Network Zin vs. Frequency');
ylabel('Impedance (Magnitude)');
xlabel('Frequency (Hz)');
axis([.1e9 final*1e9 0 150]);
legend('0.5 pF', '0.3 pF', 'Uncomp', 'Zs', 'Location', 'SE');
hold off;

%bsx fun is funky...
for k=1:count-1
    gamma(k) = (points(k) - zsmat)/(points(k) + zsmat);
gamma_3(k) = (points_3(k) - zsmat)/(points_3(k) + zsmat);
gamma_uc(k) = (points_uc(k) - zsmat)/(points_uc(k) + zsmat);
end

for k=1:count-1
    mldb(k) = -10*log10(1-abs(gamma(k))^2);
mldb_3(k) = -10*log10(1-abs(gamma_3(k))^2);
mldb_uc(k) = -10*log10(1-abs(gamma_uc(k))^2);
end

%figure(2);
subplot(2,2,2); plot(x,mldb);
hold on;
subplot(2,2,2); plot(x,mldb_3, '-r');
subplot(2,2,2); plot(x,mldb_uc, '-m');
legend('0.5 pF', '0.3 pF', 'Uncomp', 'Zs', 'Location', 'NW');
title('Tee MisMatch Loss vs. Frequency');
ylabel('Mismatch Loss (dB)');
xlabel('Frequency (Hz)');
axis([.1e9 final*1e9 0 15]);
title('S11');
ylabel('S11 (dB)');
xlabel('Frequency (GHz)');
hold off;
axis([.1e9 final*1e9 -10 0]);

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%S21
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% for k=1:count-1
%   s21(k) = 20*log10(1-abs(gamma(k)));
%   %s21(k) = 20*log10(abs(s21(k)));
% end
subplot(2,2,4);
s2p_plot([dpath '\PhD\test results\2013-02-20\18.s2p'], '-rx', 2, 1);
hold on;
s2p_plot([dpath '\PhD\test results\2013-02-20\19.s2p'], '-bx', 2, 1);
s2p_plot([dpath '\PhD\test results\2013-02-20\6.s2p'], ':k', 2, 1);
plot(x,20*log10(abs(s21)));
plot(x,20*log10(abs(s21_3)), '-r');
line = repmat(-1,1,count-1);
plot(x,line, '-m');
title('S21');
ylabel('S21 (dB)');
xlabel('Frequency (GHz)');
hold off;
axis([.1e9 final*1e9 -10 0]);

8.4 Plotting and Data Manipulation

These functions were used to plot and interpret results in all sections.

8.4.1 Impedance Analyzer

Drives the impedance plotter multiple times in order to plot multiple impedances

dpath = 'C:\data';
figure('Color',[1 1 1]);
z_plot_width([dpath, '\PhD\test results\2013-06-21\1.S2P'], 'DB','-m',1);
hold on;
z_plot_width([dpath, '\PhD\test results\2013-06-21\2.S2P'], 'DB',':r',2);
legend('On-die decoupling 1 uF, 68 nF', 'Off-die decoupling 1 uF, 68 nF', 'Location', 'NW');
title('PDN Impedance');
ylabel('Z (\Omega)');
xlabel('Frequency (Hz)');
axis([1e5 1e8 0 10]);

8.4.2 S2P Plotter

Plots touchstone files

%s2p plotter
% takes filename and generates plot (to 10GHz)
% second argument is a string for the plot options
% third and fourth arguments are the ports (p1=1, p2=1 means s11)
% this is fragile and non-optimized
function s2p_plot(filename, plot_options, p1, p2)

%%%%%%%%%%%%%%%%%%%%%%%%%%
%%% Import and format data
%%%%%%%%%%%%%%%%%%%%%%%%%%
[freq, s11, s21] = s2p_import(filename);

% remove anything >10GHz
freq([freq(1:end,1)>10e9,:]=[];
[row,~] = size(freq);

[r,~] = size(s21);
while r > row
    s11(r,:) = [];
    s21(r,:) = [];
    [r,c] = size(s21);
end

if p1 == 1 && p2 == 1
    plot(freq,smooth(s11,10,'moving'),plot_options);
else if p1 == 2 && p2 ==1
    plot(freq,smooth(s21,10,'moving'),plot_options);
end

end

8.4.3 S2P Importer

This is used to import s2p (touchstone) files
8.4.4 Impedance Plotter

This is used to import an s2p (touchstone) file and plot the results as the magnitude of impedance on a log scale.

% s2p plotter
% takes filename and generates plot (to 10GHz)
% second argument is a string for the plot options
% third and fourth arguments are the ports (p1=1, p2=1 means s11)
% this is fragile and non-optimized
function z_plot_width(filename, type, plot_options, lineWidth)

  %%%%%%%%%%%%%%%%%%%%%%%%%%%
  % Import and format data
  %%%%%%%%%%%%%%%%%%%%%%%%%%%
  [freq, s11, s21] = s2p_import_z(filename);

  % remove anything >10GHz
  freq(freq([freq(1:end,1)>10e9],:)=[];
  [row,~] = size(freq);

  %...
[r,~] = size(s21);
while r > row
    s11(r,:) = [];
    s21(r,:) = [];
    [r,c] = size(s21);
end
if strcmp(type,'DB')
    s21=10.^((s21)./20);
end;
output=-25.*s21./(s21-1);
loglog(freq,output,plot_options,
       'LineWidth', lineWidth);
set(gca,'XGrid','On');
set(gca,'YGrid','On');

8.4.5 Spectrum Analyzer Plotter

This is used to import and plot results from Tektronix Spectrum Analyzers

% formatting note: remove 'Hz' from rows 41 and 41 (0 indexed)
dpath = 'C:\data';
scale = 1;
spacing = 1e-2;
smoothing = 15;
fileName = [dpath,'\PhD\test results\2013-06-22\1.csv' ];
num_points = csvread(fileName,40,1,[40 1 40 1]);
start = csvread(fileName,41,1,[41 1 41 1]);
stop = csvread(fileName,42,1,[42 1 42 1]);
Ch1 = csvread(fileName,43,0,[43 0 num_points+42 0]);
fileName = [dpath,'\PhD\test results\2013-06-22\2.csv' ];
Ch2 = csvread(fileName,43,0,[43 0 num_points+42 0]);
points(1) = start;
delta = (stop-start)/num_points;
for k=2:num_points
    points(k) = points(k-1) + delta;
end
figure('Color',[1 1 1]);
hold off;
semilogx(points,smooth(Ch1,100,'moving'), 'r');
hold on;
semilogx(points,smooth(Ch2,100,'moving'), '-k');
legend('On Die Decoupling', 'Off Die Decoupling', 'Location', 'NW');
ylabel('Output (dBm)');
xlabel('Frequency (Hz)');
set(gca,'XGrid','On');
set(gca,'YGrid','On');
axis([1e6 100e6 -50 -20]);
9 References

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