WIDEBAND, HIGH DATA RATE KU-BAND MODULATOR DRIVER AMPLIFIER
FOR HIGH RELIABILITY SPACEBORNE APPLICATIONS

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By

JEREMY DALE GASSMANN
B.S., University of Cincinnati, 2002

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Wright State University
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I HEREBY RECOMMEND THAT THE THESIS PREPARED UNDER MY SUPERVISION BY Jeremy Dale Gassmann ENTITLED Wideband, High Data Rate Ku-Band Modulator Driver Amplifier for High Reliability Spaceborne Applications BE ACCEPTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF Master of Science in Engineering

Marian K. Kazimierczuk, Ph.D.
Thesis Director

Kefu Xue, Ph.D.
Department Chair

Committee on Final Examination

Marian K. Kazimierczuk, Ph.D.

Ronald Riechers, Ph.D.

Saiyu Ren, Ph.D.

John A. Bantle, Ph.D.
Vice President for Research and Graduate Studies and Interim Dean for Graduate Studies
ABSTRACT

Wideband, High Data Rate Ku-Band Modulator Driver Amplifier for High Reliability Spaceborne Applications.

The increased demand for high resolution satellite imagery for government, military, and commercial applications is driving the need for high data rate, millimeter-wave transmission systems to relay imagery information to a ground-based end user. An important aspect of this system which interfaces digital information to the RF domain is the modulator driver. The current trend in miniaturization of electronics leaves systems more vulnerable to single-event radiation effects in spaceborne applications. In an effort to overcome this deficiency, a wideband, high data rate modulator driver circuit has been designed, built, and tested using only high reliability space rated electronic components. To ensure operation over a wide range of frequencies, a wide bandwidth driver amplifier is needed to deliver a high speed, low bit-error rate signal. This thesis work presents the optimum circuit design to achieve these goals and demonstrates the performance of the driver in a relevant subsystem-level test setup.
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1. INTRODUCTION

1.1. Objectives

Satellite imaging technology used to gather imagery data of the Earth is gaining popularity in a number of scientific, commercial, and military applications. Applications for this technology range from the study of the health of vegetation to the study and analysis of soil moisture and human impact upon the environment. This increased demand for high resolution imagery is the main driver for the need of high data rate, millimeter-wave transmission systems to relay the large volumes of imagery information to the end user. A key system interface that is needed to meet this increased demand for high resolution satellite imagery is a high speed, wideband modulator driver. This driver is a critical interface between the digital and RF domains of a modulator system and provides the means for the collected data to be transmitted between a satellite and a ground station on earth.

The inherent need for a modulator driver sub-circuit in a high data rate, millimeter-wave transmitter application is derived from the necessity to interface a digital subsystem with an analog/radio frequency (RF) subsystem. The modulator driver is required to accept a digital data signal with a format such as current-mode logic (CML) and deliver a current-driven signal to the input of the modulator. Specifically for this work, the CML inputs to the modulator driver come from a high-speed, D-flip flop integrated circuit with a 1200 mV$_{pp}$ differential, voltage-driven output. The Ku-Band modulator has a 50-ohm input interface.
which requires a single-ended, current driven waveform to properly modulate the RF carrier for a Quadrature Phase Shift Keyed (QPSK) system. A notional block diagram of the system architecture is shown in Figure 1.1-1. This interface is a critical component to help keep bit error rate (BER) low which helps reduce the required output power for the transmitter and loosens the requirements on the forward error correction scheme on the digital data, which reduces coding overhead and improves spectral efficiency.

Figure 1.1-1: System Block Diagram

The uniqueness of this specific driver interface lies mainly in the environment in which it will be used. Being a space-based platform in a satellite imaging system requires that it meet the stringent operating environment conditions found in space including radiation effects, drastic temperature extremes, potentially very long mission life in excess of fifteen (15) years, and extremely high reliability requirements which result from the fact that electronics in space cannot be serviced if it is determined that electrical performance has been compromised.
These constraints eliminate several available components for use in this circuit mainly due to the sensitivity of the associated active components. In addition to this, the high data rates required to meet the continually increasing user demands of space-based imaging adds to the challenge of this design. The coding and encryption algorithms that generate the data to be transmitted also necessitate that the driver operate over a wide bandwidth to capture bit streams ranging from the maximum of the clock rate down to a bit stream with a pre-defined minimum transition density.

1.2. Literature Review

Throughout the research and design phase of this work, many similar modulator driver technologies were reviewed to develop the high reliability, wideband modulator driver. All of the commercially available modulator drivers found were monolithic integrated circuits that typically operated at data rates up into the 10 Giga-bit per Second (GBPS) and higher range. Many of these modulators that are available commercially are also geared toward optical modulators which have a high voltage drive requirement and can operate at very high data rates up to 40 GBPS. Of the surveyed modulator drivers, a company called Picosecond Pulse Labs offers a driver circuit, model 5865, which operates at 12.5 GBPS with a maximum root-mean-square (RMS) jitter of 1.5 ps. This driver has a gain of greater than 24 dB over the 12.5 GHz bandwidth and can accept an input voltage amplitude of 1.5 V. (Picosecond Pulse Labs, 2004) An eye diagram of this driver operating at 10.66 GBPS is shown in Figure 1.2-1.
Figure 1.2-1: Eye Diagram for Picosecond Pulse Labs Modulator Driver

Another commercially available modulator driver is the EMY1441HI manufactured by Eudyna Devices Incorporated. This integrated circuit operates at a maximum data rate of 11.3 GBPS and has a maximum RMS jitter of 3.5 ps. This driver outputs a constant current in proportion to the input voltage to the circuit. The maximum output current at room temperature is 60 mA and the maximum input voltage to the driver is 1 V pp. (Eudyna Devices Incorporated, 2006) An eye diagram of this driver operating at 10 GBPS is shown in Figure 1.2-2.
A final modulator driver that was surveyed for this work was a TriQuint Semiconductor microwave monolithic integrated circuit (MMIC) model TGA4832. This modulator driver circuit has a bandwidth of 35 GHz and a small signal gain of greater than 12 dB across this bandwidth. The RMS jitter of this driver is a very low 1 ps at a data rate of 40 GBPS. (TriQuint Semiconductor, 2009) An eye diagram of this driver operating at 40 GBPS is shown in Figure 1.2-3.
Current commercially available modulator drivers offer very high data rate operation, exceptionally low jitter, and high gain. However, none of these commercial modulators is rated for space applications. While Triquint Semiconductor does offer space rated components, they come only in a die form without a package, making it harder to implement in a system using printed wiring boards. Other attributes that are common with commercially available drivers are the high gain and very wide bandwidths. For the application that this work is trying to address, these otherwise desirable attributes actually do not meet the requirements of the system. The modulator that the driver will be interfaced with is sensitive to the drive level being delivered to it, so lower gain is needed to avoid damaging the modulator. Also, the operating environment places bandwidth restrictions on the transmitter, so bandwidth limiting is needed to avoid exceeding the constraints of the environment.

Figure 1.2-3: Eye Diagram for TriQuint Modulator Driver
1.3. Introduction to Digital Modulators

With the digital age in full force it is clear where the demand for digital communications over wireless channels came from. The benefits of being able to eliminate the need for high speed digital-to-analog and analog-to-digital components are the savings on cost and power and reduced complexity. Digital communications are also more immune to the effects of distortion and signal interference than their analog counterparts. (Sklar, 1988, p. 3) Today’s digital modulation technology comes in two main types similar to analog modulation: phase/frequency modulation and amplitude modulation. In digital amplitude modulation or amplitude shift keying (ASK), the carrier signal is amplified in discrete steps to represent the digital word to be transmitted. The simplest case is with a binary bit sequence and is also called On-Off Keying (OOK). In this method, the presence of the carrier signal is one state and the absence of the carrier is the other state.

More typically used in today’s digital communications systems are the frequency/phase based digital modulation. Frequency-based digital modulation, called frequency shift keying (FSK), utilizes steps in the carrier frequency to represent the digital signal. FSK modulators are more complex and less bandwidth efficient than an OOK modulator. Phase-based digital modulation, called phase shift keying (PSK), is a more widely used digital communication technique compared to the ones discussed above. In PSK, the phase of the carrier signal is stepped in discrete levels to represent the digital signal. For instance, the phase in binary PSK is shifted by 180° between states while in
quaternary PSK (QPSK or 4PSK), the phase is shifted in 90° increments for each of the 2-bit phase states. Both FSK and PSK modulation can be categorized as an In-Phase/Quadrature (I/Q) modulation format that is widely used in communication systems. An I/Q modulator receives separate and unique I and Q bit streams that steer the RF waveform of two mixers that are driven with an RF local oscillator with a 90° phase shift between the mixers, see Figure 1.3-1.

![I/Q Modulator Diagram](image)

**Figure 1.3-1: I/Q Modulator**

I/Q modulation is a form of bandwidth efficient modulation. This type of modulation relies on using multiple states represented as shifts in amplitude, phase, or both to increase the data throughput instead of using a higher data rate. Modulation formats such as QPSK, 8-PSK, and quadrature amplitude...
modulation (QAM) are all included in bandwidth efficient modulation. In QPSK or any M-ary PSK modulation, the data stream is encoded in the phase of the carrier. For 8-PSK, the 3-bit wide data is represented into 8 phase states: 0°, 45°, 90°, 135°, 180°, 225°, 270°, 315°, and 360°. (Langton, 2005) If the data rate was 100 MBPS, the occupied bandwidth would only be 66.6 MHz in an 8-PSK system as opposed to the full 200 MHz bandwidth that a BPSK system would occupy. In a modulation scheme such as 16-QAM, the data bits are represented in both phase and amplitude. A 16-QAM modulator can be represented by 2 QPSK modulators of differing amplitudes that are combined into one output. The combining of two QPSK modulators yields a total of 4 bits of data at a time. Using the same 100 MBPS input data stream into a 16-QAM modulator, the occupied bandwidth would only be 50 MHz.

While one of the great benefits of bandwidth efficient modulation is the fact that a great deal of information can be sent at high data rates down a bandlimited channel, one major drawback to this category of modulation is the increased probability of error. This is due to the decreased distance between the constellation points in the signal space of the higher order demodulated signal. Reduced minimum distance between adjacent symbols in the signal space leads to higher probability of bit error. As the points move closer to each other, the decision regions become smaller and the effects of noise on the system become enhanced, causing bit error probability to increase. This must be compensated for by any combination of forward error correction or increased transmit power and the tradeoff between wasted bandwidth and wasted power must be made.
1.4. Important Modulator Performance Parameters

The main parameters that are important in making digital modulators operate correctly with the given system constraints include data rate and occupied bandwidth, error vector magnitude (amplitude and phase error), bit error rate (BER), and carrier rejection. (Agilent Technologies, 2001) The combination of these metrics defines how well the modulator will deliver the digital data in terms of speed, power, and error.

The first major parameter of a digital modulator is the maximum data rate. This parameter quantifies how fast a data stream can be modulated and transmitted across a channel. The primary limitation to maximum data rate from a hardware perspective is the speed with which the internal diodes of the modulator can be fully turned on and off. Another major limitation is the amount of bandwidth available in the channel that is being used for wireless data transmission. This is because the data rate effectively spreads the spectrum of a continuous wave carrier signal in proportion to the speed of the data coming in. This can be better illustrated in Figure 1.4-1 showing the downconverted spectrum of a 2 GBPS QPSK modulator. From this figure we see that the null-to-null bandwidth of this spectrum is 2 GHz centered about an intermediate frequency (IF) of 2 GHz. This corresponds to the symbol rate of 1 Giga-symbol per second (GSPS) and the first nulls occurring at 1 GHz above and below the carrier. The side lobes are each half the width of the main lobe at 1 GHz. In this figure, the x-axis represents the frequency of the downconverted modulated carrier and the y-axis represents the power level.
The next important parameter to help determine the performance of a digital modulator is error vector magnitude (EVM). EVM can best be explained by referring to an I/Q constellation diagram like Figure 1.4-2 and an EVM pictorial like Figure 1.4-3. The I/Q constellation shows the four states of a demodulated QPSK signal and the trajectories that they take to switch between states. In a perfect QPSK system, the four states would have precise equidistant locations in the constellation and the trajectory going from each state would all overlap. The EVM pictorial shows a comparison of the location of the ideal state on a constellation and a possible real-world state location. EVM quantifies the relative error of the demodulated magnitude and phase of the received signal compared with the ideal phase and amplitude.
The bit error rate (BER) that a demodulated signal will produce compared to the signal that was sent is closely related to the EVM of the demodulated signal. The BER of a demodulated signal is simply the percentage of errors in a bit stream relative to the total number of bits in the stream. This metric is a function of the
energy per bit to noise power spectral density ratio \( (E_b/N_0) \) of the system. The \( E_b/N_0 \) of a communication system is a function of transmitted signal energy, the amount of noise and interference in the transmission medium, intersymbol interference, and the noise induced by the receiver. A popular method of estimating the BER of a communication system is to use a BER vs. \( E_b/N_0 \) curve as shown in Figure 1.4-4. (Pillai, 2008) Given a specific modulation format and \( E_b/N_0 \), a predicted value for BER can be found on this graph.

![Bit Error rate vs Eb/No for various modulation schemes](image)

**Figure 1.4-4: BER vs \( E_b/N_0 \)**

The final performance parameter to be discussed is the carrier rejection of the modulator. This parameter gives an indication of the relative phase and amplitude imbalances of the I and Q data as well as the balance of the internal mixers of the modulator. In a perfectly balanced modulator system, the carrier is completely suppressed in the modulated spectrum because the I and Q signals...
have equal amplitudes and are 180° out of phase from each other and perfectly cancel one another. When the phase and amplitude of the I and Q signals become unbalanced, the carrier signal begins to increase in amplitude. (Mini-Circuits, 1999) Looking at Figure 1.4-1, the carrier rejection can be viewed as the power level of the carrier signal relative to the peak power level of the modulated spectrum. In this figure, the level of the carrier cannot be seen. To view the carrier signal within the modulated signal, the frequency span of the spectrum analyzer must be very small to essentially zoom in on the carrier signal.
2. THEORY OF OPERATION

2.1. Digital Modulators

Digital modulation is a technique employed for the purpose of transmitting information across a wireless channel in a format that is conducive for this task. Transmitting data wirelessly across a span of many miles requires the use of a high frequency sinusoidal electrical signal because the signal attenuating properties of earth’s atmosphere at high frequencies is much lower compared with frequencies in the audible range, for example. Modulation involves the modifying of a high frequency signal called the carrier frequency by changing its amplitude, frequency, phase, or a combination of these parameters. The mathematical form of an arbitrarily modulated carrier signal is shown in Equation 1.1.

\[ A(t) \cos(\omega_0 t + \varphi(t)) \]  

(1.1)

In this equation, \( \omega_0 \) is the radian frequency of the carrier signal, \( t \) is time, and \( A(t) \) is a time varying amplitude which would be used in ASK or OOK modulation as previously discussed. The function \( \varphi(t) \) represents the time varying phase of the carrier signal. This time varying phase component can be used to vary the phase of the carrier signal such as QPSK modulation or it can be used to vary the frequency component of the carrier signal such as in FSK modulation.

Now that it is understood how modulation is mathematically expressed, the implementation of a modulator using electronic components can now be
discussed. To illustrate this, the physical implementation of a QPSK modulator and a 16-QAM modulator will be discussed.

The implementation of QPSK modulation utilizes the basic configuration of an I/Q modulator as discussed in section 1.2. The basic block diagram is repeated below in Figure 2.1-1.

\[
\frac{1}{\sqrt{2}} \cos(\omega_0 t + \pi/4) \\
\frac{1}{\sqrt{2}} \sin(\omega_0 t + \pi/4)
\]

\[d_i(t)\]
\[d_q(t)\]

RF Out

\[\text{RF Out}\]

\[\text{Figure 2.1-1: QPSK Modulator}\]

The heart of a basic I/Q modulator is the mixer. A common mixer type used in RF communication systems is the double balanced mixer. This mixer type will be
used to discuss the theory of operation of both the QPSK and 16-QAM modulation scheme. A typical double balanced mixer is shown in Figure 2.1-2.

![Double Balanced Mixer Diagram](image)

**Figure 2.1-2: Double Balanced Mixer**

In a QPSK modulator, two of these mixers are required to properly output a QPSK waveform. One mixer is used to modulate all of the in-phase (I) data and the other mixer is used to modulate all of the quadrature (Q) data. Once both of the I and Q channels have been modulated onto an RF carrier, they are summed together with an RF power combiner where the full QPSK waveform is made available for transmission.

When a double balanced mixer is configured for use in a modulator, the LO port becomes the input for the RF carrier signal, the IF port becomes the input for the digital data signals, and the RF port becomes the output for the modulated RF signal. When the IF port is fed with a digital I/Q signal that is conditioned properly to fully turn the internal diodes of the mixer on and off, the mixer acts like an RF switch. When one pair of diodes is on, the RF carrier signal is steered along that
conductive path in the diode bridge. When the other pair of diodes is on, the RF carrier is steered along this other conductive path in the diode bridge.

For the case when the I/Q signal going into the IF port is positive, diodes 1 and 4 are on and diodes 2 and 3 are off. This only allows the RF carrier to flow through the top part of the LO transformer, then through diode 1 to the RF/IF transformer from the top to the bottom, through diode 4, and finally back through the bottom part of the LO transformer. For the case when the I/Q signal going into the IF port is negative, diodes 1 and 4 are now off and diodes 2 and 3 are now on. This only allows the RF carrier to flow through the top part of the LO transformer, then through diode 2 to the RF/IF transformer from the bottom to the top, through diode 3, and finally back through the bottom part of the LO transformer. The main difference between these two possible signal paths is their relative phase to one another. The center-tapped LO transformer outputs the RF carrier signal 180° out of phase on the bottom leg compared to the top leg. So when a digital signal in conditioned and directed into the IF port, the 1’s and 0’s modulate the phase of the RF carrier by 180°. The RF carrier then has either a 0° phase shift or a 180° phase shift.

The second mixer that makes up the QPSK modulator behaves the same exact way as the first mixer with one slight difference. The second mixer is driven with an RF carrier signal that is 90° out of phase in relation to the first mixer. Now the RF carrier in the second mixer is switched between either a 90° phase shift or a 270° phase shift. The outputs of the two mixers are then combined via an RF power combiner. The resulting output waveform will be the RF carrier that has
either a $45^\circ$ phase shift, a $135^\circ$ phase shift, a $225^\circ$ phase shift, or a $315^\circ$ phase shift as shown in Figure 2.1-3

![QPSK Constellation Diagram](image)

**Figure 2.1-3: QPSK Constellation**

Now that the operation of a QPSK modulator has been described, the physical implementation of a 16-QAM modulator which is based on a QPSK modulator is addressed. A functional block diagram for a 16-QAM modulator is shown in Figure 2.1-4.
A 16-QAM modulator is comprised of two QPSK modulators, a power splitter and power combiner, and an attenuator. The theory of operation of a 16-QAM modulator follows after the QPSK modulator that was discussed above. The QPSK modulators behave the same as already discussed. The first power splitter is used to divide the RF carrier signal power equally between the two QPSK modulators. They both receive equal amplitudes and phases of the RF carrier. The output of each QPSK modulator is a phase modulated RF carrier signal both having equal amplitudes and phases. For 16-QAM to operate as designed, the two QPSK signals need to be offset in amplitude. This is done through an attenuator that reduces the amplitude of just one QPSK signal. These unequal signals are then combined with a power combiner and a 16-QAM output signal is produced. To describe mathematically the output signal of the 16-QAM modulator, Figure 2.1-5 will be used as an illustration.
This figure is a 16-QAM constellation diagram that shows graphically where the signal states lie in the I/Q signal space. It can be seen from the diagram on the right that it looks like there are four QPSK signals in each quadrant in the I/Q signal space. This is simply the vector summation of two equal phase but unequal amplitude QPSK modulators. The resultant RF sinusoid that is produced in a 16-QAM modulator can also be taken from Figure 2.1-5. It can be analytically seen from this figure, that there are four separate amplitudes that are created in this type of modulator and twelve separate phase states. So at any instant in time, the output waveform will take on one of four amplitude states and one of twelve phase states.

2.2. Modulator Driver Interface

The modulator driver interface bridges the gap between the digital interface circuitry that contains the information to be transmitted and the RF transmitter which modulates the information onto an RF carrier signal for transmission over
very long distances to be recovered as the original information that was sent. The successful operation of any I/Q modulator depends on the quality of this interface. If the interface circuitry distorts the digital signal or introduces noise or harmonics, the performance of the modulator suffers and the quality of the received signal will be degraded. The modulator driver interface provides two essential characteristics to the modulator system. First, it provides a high current output to the internal diodes of the modulator to ensure that the diodes are completely turned on. Second, the modulator driver provides a bandwidth limiting effect on the digital signal which shapes the square wave pulse at the highest frequencies into more rounded signals. Since a digital square wave signal at a given frequency requires multiple harmonics to represent the square shape of the signal, limiting the bandwidth tends to round off the edges of the square wave. This is important in systems that require strict bandwidth limitations to keep interference down for nearby systems and manifests itself into lower sideband levels of the modulated RF spectrum.

The modulator driver can best be categorized as a wideband RF amplifier. The main subcircuits of this wideband amplifier are the input matching network, the output matching network, the stability network, the bias network, and the active device, as depicted in Figure 2.2-1.
Starting at the device and working outward, the gate and drain bias networks, in the case of a field effect transistor (FET), are encountered first. The main purpose of these networks is to allow the DC biasing voltages for the transistor to reach the device, while at the same time preventing the high frequency signals from entering the power supplies that are generating the DC voltages. This high frequency rejection is required for reasons of keeping electromagnetic interference down so other electronics in the system are not adversely affected. The bias networks are essentially low pass networks with a very low cutoff frequency. Another important aspect of the bias network is its loading effect on the transistor. The selection of the first elements nearest to the device is critical for proper operation of the circuit. More detail regarding this will be given in the design section.

Working farther away from the device, the next subcircuit is the stability network. The stability network’s sole purpose is to increase the margin of stability of the active device in the amplifier. RF transistors are prone to oscillation if a certain
range of impedances (real and reactive) are presented to the device. In an effort to reduce or even eliminate the range of impedances that can cause this instability, a stability network is inserted typically at the input of the device and sometimes at the output to desensitize the subcircuit to the various impedances that will be presented by the matching networks discussed next and on the input and output ports of the modulator driver.

Finally, located farthest from the active device are the matching networks. There is one network to match the input of the device and one network to match the output of the device. They both have the same function, however they may look different due to the fact that the input and output impedances looking into an active device are typically different. When matching an RF transistor, the key is to transform the impedance seen at the device to the characteristic impedance of the system that the amplifier is connected to, typically 50 Ω in RF communications. When the amplifier impedance is matched to the system impedance, then maximum power transfer is accomplished and the circuit is optimized.
3. DEVICE TECHNOLOGY

3.1. Device Parameters

The core building block for the modulator driver circuit is the active device technology. Without the active device, signal amplification would not be possible. In selecting the active device that would suit the application of the wideband modulator driver, there are several key parameters that need to be identified so that the correct device is selected to ensure all of the performance requirements are met. The important device parameters that were considered for this circuit were output power, maximum transition frequency, small signal gain, reliability, and radiation hardness.

The output power that the device is capable of producing is important in determining if the device is suitable for an application. For the modulator driver circuit, the required power that the modulator wants to see is within the 0 dBm to +10 dBm range. Also required for this application is that the transistor is operated in the linear power range without any gain compression. Given these criteria, a device capable of producing at least 20 dBm of output power at the highest frequency of operation was deemed adequate for the application.

This leads into the next important parameter, the maximum transition frequency. This metric is simply the maximum frequency component that the active device can transition from the input to the output. This is used to determine the highest frequency that can be passed through a transistor. The highest frequency that
the modulator driver could see is a 1 GHz square wave. Being a square wave as opposed to a sine wave means that multiple harmonics of the square wave frequency are needed to represent the square wave and thus the maximum frequency will be on the order of three to five times the maximum frequency for a proper square wave. So a 1 GHz square wave can be represented with a 3 to 5 GHz sinusoid. Given these criteria, a device with at least 10 dB of gain at 10 GHz is required to cleanly output a square wave at 1 GHz to the modulator.

Concerning the gain of the RF transistor, the available output power of the digital circuitry that feeds the modulator driver and the required input power to the modulator needs to be considered. The required input power to the modulator was already discussed in the section on output power and was up to 10 dBm. The output power of the digital circuitry with a current mode logic CML signal is on the order of 0 dBm. In order to produce the required power to the modulator, a transistor with a small signal gain of at least 10 dB is required at the maximum frequency found in the section on transition frequency.

The final set of criteria that needs to be analyzed is the reliability and radiation hardness of the devices. The main driver for these requirements is the application where this driver circuit will be used, namely in space. When operating in space, there are very harsh conditions that the active devices are exposed to such as temperature extremes and high radiation environments, not to mention the harsh vibrations that the electronics will experience being transported into space on a launch vehicle. Also under consideration is the total operating time that the transistor will see during the life of the mission. Inserted in
a platform that is transferring information all of the time will require a transistor with a high mean time to failure (MTTF). Now having all of these requirements factored in, an optimal device technology can be selected.

3.2. Device Classification
There are many different types of RF devices available for signal amplification ranging from Silicon bipolar junction transistors to Gallium Arsenide field effect transistors to Indium Gallium Arsenide pseudomorphic high electron mobility transistors (pHEMT). Two important things to consider when choosing a device type is the operational frequency and output power capability. For the modulator driver application the combination of power and frequency allows any of these device types to be used.

To take another step forward in choosing an appropriate device technology, the noise performance of the device is important in this application since the system has a requirement for low BER performance and a reduction of noise in the system will improve this. It turns out that the pHEMT and FET have very good noise performance at the frequencies of interest. (Vendelin, Pavio, & Rohde, 1992) Of these two technologies, the pHEMT has slightly better noise performance than the FET.

Finally, the most critical design requirement is the device immunity to radiation effects. Being a space borne application, the exposure to radiation that the active devices experience is quite high. FET and HEMT technologies naturally have a high degree of immunity to different radiation effects compared to bipolar
technology. Putting all of these device requirements together to find the optimal device technology that meets the requirements of the system, a millimeter-wave AlGaAs/InGaAs pHEMT from Microwave Technologies was chosen as the core of the modulator driver circuit. The device chosen was the PH-9 pHEMT. (Microwave Technology, Inc., 2006) This device offers 10 dB of small signal gain at 12 GHz providing sufficient gain at the frequency of operation of the modulator driver. It has a typical output power of +27 dBm at 12 GHz allowing for operation in the linear region of the power curve. The pHEMT devices in the same category offer noise figures on the order of about 2 dB. The long term reliability of these devices is quite long having an MTTF of $10^6$ hours or 114 years at a junction temperature of 150 °C. The combination of all of these parameters makes this device the top candidate for the modulator driver design.

3.3. Device Model

Now that the specific device has been identified, an electrical model of the characteristics of the device needs to be either obtained or generated to aid in the modulator driver design. From the manufacturer’s website, S-parameters are included for the specific device chosen and a linear circuit model is included for a similar device (Microwave Technology, Inc., 2006). Since the S-parameters for the device used in this design range from 1 GHz up to 26 GHz and the driver design occupies the range of frequencies at and below 1 GHz, a linear model had to be created. The model created that matches the frequency response of the S-parameters can then be used to predict the behavior of the model below 1 GHz.
AWR’s Microwave Office is the CAD software that was used to develop the transistor model for this effort as well as the actual modulator driver design. The topology for the model that was used in the design is shown in Figure 3.3-1.

![Figure 3.3-1: Linear Transistor Model](image)

The model consists of a generic linear FET model that is depicted in Figure 3.3-2, along with the parasitic inductance and resistance of the device package for the gate, drain, and source.
This model was then fit to the S-parameters given by the manufacturer over the frequency range of 1 GHz to 12 GHz since the higher frequencies are of less significance in the driver design. The resulting response of the transistor model versus the S-parameters is depicted in Figure 3.3-3, Figure 3.3-4, and Figure 3.3-5. As can be seen from these figures, the modeled transistor fits the measured S-parameters given by the manufacturer to within a very low error. The confidence that the model will accurately predict the response of the modulator driver at lower frequencies is therefore quite high.
Figure 3.3-3: Modeled Versus Measured Source and Load Gamma
Figure 3.3-4: Modeled Versus Measured Forward Transmission
Figure 3.3-5: Modeled Versus Measured Reverse Transmission
4. MODULATOR DRIVER DESIGN

Now that the basic requirements for the wideband modulator driver have been established and the device technology has been chosen, the details for the design of the modulator driver is discussed. First, the full requirements for the modulator driver need to be established in order to proceed with the detailed design. Table 4-1 shows the important parameters needed to design the modulator driver and meet the requirements of the high data rate modulator system.

Table 4-1: Modulator Driver Requirements

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Requirement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandwidth</td>
<td>10 MHz – 1.5 GHz</td>
</tr>
<tr>
<td>Gain</td>
<td>Greater than 10 dB</td>
</tr>
<tr>
<td>Input and Output Return Loss</td>
<td>Less than -10 dB</td>
</tr>
<tr>
<td>RMS Jitter</td>
<td>Less than 10 ps</td>
</tr>
<tr>
<td>Error Vector Magnitude</td>
<td>Less than 10%</td>
</tr>
</tbody>
</table>

When designing an active RF circuit, the scattering parameters or S-parameters of the device over a range of frequencies are often used to understand and predict the behavior of the active circuit over a range of impedances. S-
parameters quantify how RF energy propagates through a multi-port network and can be understood as the ratio of the voltage out to the voltage in. (P-N Designs, Inc., 2009) They can also be used to determine circuit stability and can even be used to produce eye diagrams and predict jitter performance. Figure 4-1 depicts the S-parameters of the chosen device obtained from the device model developed previously. Figure 4-2 shows the relative stability of the unmatched device over the entire frequency band with the condition for stability identified by the blue cross-hashed line.

![Driver LS Analysis Smith](image)

**Figure 4-1: S-parameters of Device**
Figure 4-2: Stability of Device

Now that the device response is fully characterized, the design of the modulator driver circuit can proceed. The driver circuit is implemented using surface mount resistors, capacitors, and inductors and the components are routed on a microstrip substrate using Rogers 4003 substrate material. This material has a dielectric constant of 3.38 and has a thickness of 20 mils between the bottom ground plane and the top signal plane. Where a low resistance and low inductance electrical connection to the ground plane is required on the top layer, epoxy filled electrically conductive vias are used. However, the source leads of the active device are directly connected to the ground plane using small wires. This was needed to provide a very low resistance and inductance path to ground for the stable operation of the device. SMA connectors are used to interface the modulator driver circuit to the adjacent circuitry in the modulator system. The
subcircuits of the modulator driver have been partitioned by function and are thus labeled the Bias Network, the Stability Network, and the Input and Output Matching Networks. The function and design of each subcircuit are described in the sections to follow.

4.1. Bias Network Design

The first step in designing an amplifier circuit is to design the DC bias networks. These networks provide the device with DC voltage for the gate and drain while simultaneously rejecting high frequency signals at the power supplies. Concurrently the bias networks need to be designed such that they do not load the device with impedances that would cause instabilities. In fact, the bias networks can be used to partially add stability margin to the active device. In their basic form, these networks are a low pass filter with a very low cutoff frequency when viewed from the device to the power supply. Figure 4.1-1 shows a schematic of the modulator driver with the bias networks highlighted in orange.
Figure 4.1-1: Modulator Driver Schematic with Bias Networks Highlighted

As can be derived from the schematic, the bias network is an eighth order lowpass filter design. The reason for the complexity of this bias network is because of the very wide bandwidth of the modulator driver design. In a typical microwave amplifier with a reasonable 10% bandwidth, a simple quarter-wave transmission line with a low operating frequency impedance shunt capacitor to ground and series inductor would take care of most microwave frequencies trying to pass through to the power supplies. However, for a wide bandwidth design, multiple microwave frequency filtering stages are required; otherwise the bias network would detrimentally load the active device in the passband of the amplifier.
The first elements in the bias networks are the resistors that are connected directly to the gate and drain of the devices. Placing resistors in close proximity to the devices offers a termination path for high frequency instabilities which helps stabilize the amplifier. The magnitude of the gate resistor in the bias network is several hundred ohms while the resistor in the drain bias network is only a few ohms. The gate of the transistor can afford to have a high value resistor in the DC bias path since the DC current into the gate is typically very low and the gate side of the device is a large source of transistor instability. The drain, however, should have less than 10 to 20 ohms of resistance in the bias network so that a large voltage drop is not induced in the drain path and so that variations in drain bias current does not modulate the drain bias voltage during large RF voltage swings. In power amplifiers, large drain resistance also has a negative effect on the power-added efficiency of the amplifier and the amount of drain resistance has to be even lower.

The next component in the gate and drain bias networks is a low value microwave inductor that has a resonant frequency well above the highest frequency of the amplifier. The magnitude of this inductor is only a few nano-Henries. This offers an impedance of a couple tens of ohms at the highest frequency and impedes the flow of high frequency signals. Following the inductor is a shunt capacitor to ground. To avoid any resonances in the passband of the amplifier, a relatively large value capacitor was used on the order of about 1500 pF. This presents a low impedance path to ground for any high frequency signals that make it past the resistor and inductor. Also to note is the resistor that is
placed in the path of the capacitor to ground. This resistor is needed to add a real component to the high reactance of the capacitor so that any resonances with the combination of the inductor and capacitor are de-queued.

Continuing on down, the inductance values get larger and larger as well as the capacitance values. Each inductor going down the bias network impedes the transmission of frequencies lower than the inductor before it and each capacitor going down the bias network shunts the energy of frequencies lower than the capacitor before it until the network has eliminated all potential frequencies that might be generated by the active device. Figure 4.1-2 shows the simulated forward transmission response of the gate and drain bias networks in the direction from the transistor to the power supplies.
Figure 4.1-2: Gate and Drain Bias Network Forward Transmission Response

The S-parameters of the device with the bias networks included are shown in Figure 4.1-3. These are the parameters that will be used to match the device to a 50 ohm system as well as make the device unconditionally stable. The stability parameters known as $\mu$-factors are shown in Figure 4.1-4. More details about stability will be given in the next section.
Figure 4.1-3: S-parameters of Device with Bias Network Included
4.2. Stability Network Design

The stability network of a microwave amplifier is a special network that is used to significantly reduce the range of termination impedances that would cause instabilities to be induced in the amplifier. Typical stability network topologies that are used in microwave amplifier design include shunt resistive loading which was incorporated in the bias network design with the inclusion of the first resistor, capacitor, and inductor combination inserted close to the device. Another type of stability network that is widely used is the parallel RC network inserted serially with the gate of the transistor. This acts as a resistive high pass network and helps relieve the transistor from low frequency instabilities while still maintaining a low resistance path to the gate for frequencies in the passband of the amplifier.
At very low frequencies, the capacitor acts as a high impedance compared to the resistor, so any low frequency feedback signals will have to pass through a resistor to continue to support oscillations. At frequencies in the passband and above, most of the microwave energy is passed through the capacitor which is now a low impedance path to the gate and allows the desired frequencies to pass through. Since microwave transistors typically have high gain at low frequencies and then roll off as the frequency increases, reducing low frequency gain significantly helps alleviate instability problems in microwave amplifiers. Figure 4.2-1 shows a schematic of the modulator driver with the stability network highlighted in green.

Figure 4.2-1: Modulator Driver Schematic with Stability Network Highlighted
When analyzing the stability of an amplifier, there are several different simulation techniques that can be used to measure the relative stability of the amplifier. Among these methods are using the K and B1 factors, μ and μ-prime factors, and a simulation measurement tool known as the gamma probe. Using the K and B1 factors to ascertain stability performance of an amplifier is a widely accepted method that ensures unconditional stability given that the requirements are met. While this method is a good approach, the amplifiers tend to be over stabilized and consequently yields lower gain performance of the amplifier.

At the other end of the spectrum, the gamma probe offers a unique stability analysis technique that delivers accurate stability predictions while not over stabilizing the amplifier and affecting the performance. The gamma probe actually measures the gamma coefficients at the device and if the reflection coefficients go above unity or 0 dB, an unstable load impedance on the Smith chart is found. Since this method is using the device as the reference plane, the true stability can be determined and the amount of stabilization can be relaxed.

Finally, the μ factors which is the method chosen for this work, offers a similar result to the K and B1 method but offers a less confusing criteria and also has the advantage of being usable with multistage designs where K and B1 cannot. (Pozar, 1998, pp. 612-617) The necessary and sufficient conditions for unconditional stability are that both the source and load μ factors be greater than 1 at all frequencies. Figure 4.2-2 shows the new S-parameters that will be used to match the network to the 50 ohm system impedance and Figure 4.2-3 shows
the stability performance of the amplifier after the insertion of the stability network.

Figure 4.2-2: S-parameters of Device with Stability Network Included
4.3. Input and Output Matching Networks

The final step in the modulator driver design is the design of the input and output matching networks that will transform the impedance of the current network which includes the device, bias network, and stability network to the required 50 ohm impedance imposed by the system. Also included in the matching networks are DC blocking capacitors to keep DC voltages out of the digital circuitry feeding the modulator driver and out of the modulator itself. Referencing the Smith chart in Figure 4.2-2, the goal of the input and output matching networks is to move the impedances looking into the ports of the network displayed in the red and blue traces to the center of the chart which is the 50 ohm point. When the impedance of the network matches the impedance of the system, maximum power is
transferred and there are no signals that are reflected back. Figure 4.3-1 shows the schematic of the modulator driver with the input and output matching networks highlighted in blue.

**Figure 4.3-1: Modulator Driver Schematic with Matching Networks Highlighted**

As can be seen from Figure 4.2-2, the output matching network appears to already be matched quite well. As mentioned, the output matching network includes a series capacitor to isolate the DC voltage to the drain of the device. It also includes a series resistor, capacitor, and inductor shunting the output of the driver. This was included to shape the gain of the driver so that there is high frequency roll off. This is helps keep the sidelobe levels of the RF output spectrum of the modulator as low as possible.
Again, referring to Figure 4.2-2, it is clearly seen that the input of the network is not ideally matched to the 50 ohm characteristic system impedance. It was found that a series resistor-inductor circuit shunted at the input was all that was needed to bring the low frequency match closer to the center of the Smith chart. The final S-parameter response of the modulator driver is shown in Figure 4.3-2. The stability analysis of the modulator driver is shown in Figure 4.3-3 and suggests unconditional stability from 10 kHz up to 26 GHz.

Figure 4.3-2: S-parameters of Modulator Driver Circuit
Figure 4.3-3: Stability of the Modulator Driver Circuit

The final response showing the small signal gain, input return loss, and output return loss of the modulator driver circuit is shown in Figure 4.3-4.
**Figure 4.3-4: Full Small Signal Response of the Modulator Driver Circuit**

Figure 4.3-5 and Figure 4.3-6 below show the layout of the modulator driver circuit and a photograph of the built hardware as tested in the remainder of this work.
Figure 4.3-5: Modulator Driver Circuit Layout

Figure 4.3-6: Modulator Driver Circuit Hardware
Once this circuit was fully assembled, several tests on the circuit alone were completed as well as testing of the circuit in an actual modulation subsystem. The results of the stand-alone testing and the performance of the modulator driver implemented in a QPSK modulator are presented in the next section.
5. MEASURED RESULTS OF THE MODULATOR DRIVER

5.1. Modulator Driver Measurements

Once the modulator driver circuit was designed and the circuit built, the next step was to quantify the performance of the circuit and compare its performance to the predicted simulations. The first measurement that was made on the modulator driver was done using an Agilent ENA Series network analyzer, model E5071C (Agilent Technologies, 2009) to determine the frequency response of the circuit. Small signal gain and input and output return loss were measured on the network analyzer and imported into Microwave Office for comparison of measured versus simulated results. Figure 5.1-1 shows the measured versus simulated small signal gain and input and output return loss of the modulator driver. In this figure, the data points with circles represent the simulated data and the data points with squares represent the measured data.
Figure 5.1-1: Measured versus Simulated Gain and Return Loss of the Modulator Driver (Circles indicate simulated, squares indicate measured)

As can be seen from the figure, there is some error between the measured and simulated frequency response of the modulator driver but both maintain the same overall shape of the frequency response. In some areas, the gain is less than the simulator predicted and in other areas it is more. Also, some of the locations of good matching to a 50 ohm system are offset in frequency. These variations are largely due to the effect of the microstrip substrate on the active device. Also, the S-parameters given by the device manufacturer were taken on an actual wafer full of these devices and packaging parasitics were modeled and added to the overall transistor model which could add to the error. A more rigorous approach would have been to mount the devices to the intended circuit substrate and characterize it as it will be implemented. However, for the requirements of this
work, the modulator driver needed to operate up to 1.5 GHz. The error between measured versus simulated up to this frequency is actually quite low with the exception of a couple of decibels of gain difference.

The next stand-alone testing on the modulator driver circuit were the construction of an eye diagram and the resulting output pulse shape when driven with a square wave signal at various fixed data rates. The data source used to drive the modulator driver circuit with digital data was a serial data analyzer called a BERTScope with model number 12500A (SyntheSys Research, Inc., 2010). This unit is designed to test the signal integrity of digital systems by measuring signal jitter, bit error rate, and even constructing eye diagrams. An eye diagram can best be described as the output waveform histogram of a pseudo-random bit sequence (PRBS). The eye diagram compiles and overlays multiple patterns into one waveform that is the width of the least significant bit. (Foster, 2004)

For the modulator driver eye diagram test, the input and output capabilities of the BERTScope are used to test the signal integrity of the output of the driver, but when analyzing the output pulse shape of the modulator driver or the performance of the driver in a modulated system, the outputs of the BERTScope are used only to provide digital waveforms to the driver. A block diagram of the test setup to measure the eye diagram and the output pulse shape is in Figure 5.1-2.
In the configuration of the system that the modulator driver will be inserted into, the driver is being driven by a D-flip flop integrated circuit. To establish a baseline for the analysis of the modulator driver, the D-flip flop has been analyzed using the BERTScope to measure the jitter at the output of the flip flop as well as to generate an eye diagram. The eye diagram for the D-flip flop is shown in Figure 5.1-3.
The RMS jitter of the D-flip flop is 2.8 ps and the rise and fall times are 22.9 ps. Now that a baseline has been established, the measured eye diagram for the modulator driver fed by the D-flip flop and the eye diagram simulated with Microwave Office without the D-flip flop is now shown in Figure 5.1-4.
Figure 5.1-4: Modulator Driver Eye Diagram Fed by D-Flip Flop (Left) and Simulated without D-Flip Flop (Right)

The measured eye diagram looks very similar in shape to the simulated eye diagram in the figure. It can be seen that the jitter and rise and fall time performance has been degraded some by the addition of the modulator driver. The measured RMS jitter of the modulator driver with the D-flip flop is 9.2 ps and the rise and fall time of the combined components is 160 ps. This gives an RMS jitter of the driver by itself of just 6.4 ps. Simulated jitter without the D-flip flop is 3.9 ps. The increased jitter and rise and fall times are tradeoffs that must be made to give the QPSK modulator the correct drive signal. The significant increase of the rise and fall times of the digital waveforms is attributed to the bandwidth limiting effect that the driver imposed on the system and is desirable for systems that have very strict bandwidth requirements. This increase in rise and fall times is only a small percentage of the bit period of the data waveforms input to the system and does not significantly affect the BER of modulator.
Now that the eye diagram has been described and the performance of the driver with a random bit sequence shown, the performance of the driver with a fixed frequency square wave can be discussed. In this measurement scenario, the BERTScope is being used solely as a source for the square wave signal for the modulator driver and a Tektronix high speed digital storage oscilloscope with model number TDS6124C (Tektronix, Inc., 2009) is being used to capture the output waveforms. Refer to Figure 5.1-2 for the output pulse shape measurement setup. Figure 5.1-5 shows the measured versus simulated output pulse shape of a 1 GHz square wave input to the modulator driver.

![Driver LS Analysis Tuned](image)

**Figure 5.1-5: Measured (Left) versus Simulated (Right) Modulator Driver Output Pulse Shape at 1 GHz without D-Flip Flop**

The waveforms shown in Figure 5.1-5 have very similar characteristics and the output has the shape of a rounded square wave at the maximum data rate that the modulator drivers will be operated. This is a good indication that the modulator driver will be able to sufficiently turn on the internal diodes of a modulator at the highest data rate required for this work. At the other end of the frequency range that represents the associated frequency of the data rate
divided by the longest consecutive sequence of 1’s or 0’s, Figure 5.1-6 shows the measured versus simulated performance of the modulator driver with a 12.5 MHz square wave.

![Graph showing measured and simulated performance](image)

**Figure 5.1-6: Measured (Left) versus Simulated (Right) Modulator Driver Output Pulse Shape at 12.5 MHz without D-Flip Flop**

This figure also shows a very similar waveform shape between the measured and simulated modulator driver. At the low end of the bandwidth of the modulator driver, the shape of the output pulse has a slope associated with it. This is due to the large DC blocking capacitors that are a part of the input and output matching networks. These large capacitors were needed because of the wide bandwidth of the modulator driver circuit. To compensate for this slope by decreasing the capacitance of the DC blocking capacitors, the gain and return losses of the driver over the required bandwidth become non-optimal. For the function that the modulator driver performs in a modulator system, this artifact does not noticeably affect the performance of the modulator as the waveform remains above the turn on characteristics of the internal diodes of the modulator.
5.2. Circuit Implementation in a Ku-Band QPSK Modulator

Now that the signal integrity of the modulator driver has been established, the attention is now focused on the performance of the modulator driver when interfaced with a 2 GBPS Ku-Band QPSK modulator. The first analysis that can be done on a modulated RF signal is to measure the RF spectrum. The output RF spectrum of the modulator is measured with a spectrum analyzer as shown in the test setup of Figure 5.2-1. To operate the QPSK modulator, two modulator drivers were built to ascertain the performance of the modulator drivers in an applicable system.

![Figure 5.2-1: RF Output Spectrum Measurement Block Diagram](image)

The output RF spectrum of the Ku-Band QPSK modulator operating at a data rate of 2 GBPS is shown in Figure 5.2-2.
Figure 5.2-2: Modulated RF Spectrum

Important information can be obtained from the modulated RF spectrum. The main attribute that can be measured from the modulated spectrum is the RF carrier rejection. Looking at Figure 5.2-2 as a reference, a modulator with poor carrier suppression would manifest itself as a spurious signal at the center frequency of the modulated spectrum rising above the main lobe. As discussed before, the amount of carrier suppression of a modulator gives an indication as to the amplitude and phase balance of the internal mixers of the modulator. This measurement only gives an indication of the performance of the modulator system. To actually determine the amplitude and phase imbalance performance of the modulated system, the signal must be demodulated and mapped to the I/Q plane as will be discussed next.
As a way to complete the analysis of the performance of the modulator driver in a modulated system, a very high speed oscilloscope is used to demodulate the modulated waveform and produce a QPSK constellation, the reconstructed I/Q data waveforms, and some basic measurements such as EVM, phase and magnitude error, and modulation error rate (MER). The test setup for this set of measurements is shown in Figure 5.2-3.

Figure 5.2-3: Demodulated Analysis Measurement Block Diagram

In this test setup, the Ku-Band modulated signal is downconverted to an intermediate frequency (IF) of 2 GHz for post processing of the signal by the high speed oscilloscope. The post processing done by the oscilloscope takes the
downconverted modulated carrier signal and produces an I/Q signal constellation diagram, the recovered I and Q data signals, and even constructs the spectrum of the IF signal. In addition to this, the high speed oscilloscope can measure the EVM, the phase and magnitude error, and can compute the modulation error rate (MER). Figure 5.2-4 shows the constructed I/Q signal constellation diagram with state trajectories of the demodulated waveform of the QPSK modulator system with the modulator driver.

![Constellation Diagram](image)

**Figure 5.2-4: 2 GBPS QPSK Modulator I/Q Constellation Diagram**

This figure shows the magnitude and angle of the demodulated signal in pink and the signal trajectories from state to state in yellow. The points on the constellation are relatively tight in their spacing and there are no stray points in the signal space. This shows that the modulator is shifting the phase of the carrier signal very well and with little variation in the phase and amplitude of the modulated...
signal. To go a step further, Figure 5.2-5 shows the recovered I and Q eye diagram after demodulation.

![Demodulated I/Q Eye Diagram](image)

**Figure 5.2-5: Demodulated I/Q Eye Diagram**

Comparing this figure to Figure 5.1-4 it can be seen that the width of the eye has been reduced, but the jitter of the eye looks nearly the same. The reduction in width is an artifact of the bandwidth limiting effect that the modulator driver has on the system and manifests itself in slower rise and fall times of the waveform. The bandwidth limitation of the mixer used to downconvert the modulated signal also adds to this reduction in eye width. The amplitude of the I and Q data signals is sufficient to produce the correct digital representation of the signal after it is demodulated as was portrayed in Figure 5.2-4. Finally, Figure 5.2-6 shows
the measurements and calculated results of the demodulated signal found by the post processing of the RF waveform by the high speed oscilloscope.

![Table of Modulator Performance Metrics](image)

**Figure 5.2-6: Measured and Calculated Modulator Performance Metrics**

An EVM of 11.8%, phase error of 6°, and magnitude error of 5.5% while not quite adequate in low data rate systems, is in the moderate performance range for a high data rate, Ku-band system operating in a harsh space environment. The modulator that was used to determine the capabilities of the modulator driver was not a commercial part but an engineering unit that was designed specifically for this program and still needs to be optimized for peak performance. Therefore the modulation metrics presented here are not solely tied to the performance of the modulator driver but are a part of all of the pieces of the modulation system. These metrics are included only to serve as a data point to show that the modulator driver is indeed operating correctly and also to be a benchmark for future iterations of the modulation system.
6. CONCLUSIONS AND FUTURE WORK

6.1. Conclusion

The design, simulation, fabrication, and measurement of a wideband modulator driver for high data rate communications applications in a space environment have been presented. The uniqueness of this work lies in the requirements of the operating environment of the modulator driver and surrounding circuitry, namely that the active device is required to be able to operate reliably in a high radiation environment. Another factor driving the need for a discrete circuit design is the specific bandwidth restrictions required by the modulator system at the 2 GBPS data rate. A wideband modulator driver was successfully designed and built to meet the requirements for a 2 GBPS QPSK modulator operating in the Ku-Band of frequencies. When interfaced with the modulator, the EVM performance of the driver and modulator was 11.8% with associated phase and magnitude error of 6° and 5.5%, respectively. This performance is quite modest given the data rate and carrier frequency of the modulator system. The jitter performance of the modulator driver itself was a low 6.4 ps which is excellent. Overall, the wideband modulator driver delivers good performance relative to commercially available integrated circuit drivers and has the characteristics to operate with high reliability in a space environment.
6.2. Future Work

As previously discussed the modulator driver circuit while operating sufficiently for the given application, still has room for improvement and expanded functionality. Some areas for improvement would be in the phase and magnitude error performance of the modulator driver which directly affects the EVM performance. The jitter performance of the driver could be improved by using a low phase noise pHEMT that Microwave Technology, Incorporated manufactures and this could improve the phase error performance significantly. More effort could also be taken to improve the gain flatness over the bandwidth and specifically, the low frequency performance could be adjusted to produce flat pulses instead of sloped pulses. This would help improve the magnitude error performance of the driver circuit. The combination of these two areas of improvement could significantly increase the EVM performance of the modulation system used to exercise the performance of the modulator driver.

Another area for future work could be to make this a DC coupled instead of AC coupled modulator driver. The current design was configured as an AC coupled driver for ease of bias voltage selection for the active device. More complicated topologies could be adopted to allow for a DC coupled design. This would be advantageous during the testing and fine tuning stage of the modulation system. This would also allow for more flexibility with various encoding and/or encrypting algorithms that could possibly have longer strings of 1’s or 0’s. In addition, the modulator driver could operate at lower data rates while it is currently fixed at 2 GBPS.
A final avenue for future expandability of the current design is to provide a means for control of the output amplitude for use in multilevel modulation schemes such as 16-QAM. The driver circuit as currently designed can respond to an extent to a multilevel signal, but the gain of the amplifier is not tunable. To successfully operate the driver in a multilevel modulation system, the output would need to be tunable during the adjustment and alignment stage of the modulation system. Linear modulators typically have a small linear range of drive levels that will result in an amplitude varying output. Given this, a means to vary the gain of the drive circuitry is necessary to deliver high performance multilevel modulation signals.
Bibliography


http://www.microwaves101.com/encyclopedia/sparameters.cfm


