Design of Pulse Output Direct Digital Synthesizer with an Analog Filter Bank

A thesis submitted in partial fulfilment of the requirements for the degree of Master of Science in Engineering

by

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B.Tech., Jawaharlal Nehru Technological University, 2005

2008
Wright State University
WRIGHT STATE UNIVERSITY
SCHOOL OF GRADUATE STUDIES

June 19, 2008

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SUPERVISION BY Aditya Pothuri ENTITLED Design of Pulse Output Direct Digital
Synthesizer with an Analog Filter Bank BE ACCEPTED IN PARTIAL FULFILLMENT
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Abstract


Over the past two decades frequency synthesizer has progressed from a relatively crystal bank synthesizer to multi-loop phase locked loops. But in recent years direct digital synthesizers (DDS) have witnessed an increase in demand over their analog counterparts. The DDS offers a wide range of advantages over phase locked loops such as high frequency range, fast switching response, and sub-hertz frequency resolution. However, the conventional DDS suffers limitations due to its architecture involving digital-to-analog converter (DAC) and read-only-memory (ROM) with respect to high clock speeds.

The Pulse Output Direct Digital Synthesizer (PODDS) presented in this thesis eliminates the necessity for a DAC and ROM, and replaces the phase conversion block present in the conventional DDS with an Analog filter bank to generate the sine wave. The PODDS operates at a frequency of 2.25GHz, with a 16-b phase accumulator designed using carry look-ahead adder. The analog filter bank was designed using an array of low-pass Chebyshev filters. A frequency range of 1.1 MHz – 1.125GHz was achieved with average power consumption of 83mW.
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<table>
<thead>
<tr>
<th>Acronym</th>
<th>Description</th>
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<tbody>
<tr>
<td>DDS</td>
<td>Direct Digital frequency Synthesizer</td>
</tr>
<tr>
<td>PLL</td>
<td>Phase Locked Loop</td>
</tr>
<tr>
<td>DAC</td>
<td>Digital to Analog Converter</td>
</tr>
<tr>
<td>AFB</td>
<td>Analog Filter Bank</td>
</tr>
<tr>
<td>PODDS</td>
<td>Pulse Output Direct Digital frequency Synthesizer</td>
</tr>
<tr>
<td>ROM</td>
<td>Read Only Memory</td>
</tr>
<tr>
<td>LUT</td>
<td>Look Up Tables</td>
</tr>
</tbody>
</table>
Acknowledgement

I would like to first thank Dr. Siferd for giving me this opportunity and his guidance through out my thesis and also Dr. Henry Chen and Dr. Marian Kazmeirczuk for being on my Thesis Defense committee. I like to thank my parents and family for their continuous moral support through out my graduate studies with out whom this was not possible. Finally I would like to thank my friends for their help and standing by my side through some tough times and encouraging me and also to people who ever involved directly or indirectly in completing this work.
1. Introduction

1.1 Background

In the last 20 years, frequency synthesis has progressed from relatively a theoretical crystal bank synthesizer to the modern multi-loop phase-locked loop systems. Recent years have witnessed an increasing interest in Direct digital frequency synthesizers because of the bulky analog devices which have been dominating frequency synthesis for years. Analog techniques use bulky devices such as inductors, capacitors, quartz crystals and etc. With today’s technology, direct digital synthesizer (DDS) systems are becoming an alternative to analog based techniques because of their accuracy, precision and fast frequency hoping.

Direct digital synthesis has been described in the literature as early as 1970’s for generating audio signals but has been considered as a low-speed technique because most of its performance was based on the Digital-to-Analog converter (DAC). In its early developmental stage the attainable output frequency was only a few MHz but with the advancement in available logic ICs and semiconductor technology the performance of the DDS has improved immensely. Today there are capable of generating output frequencies in the range of few hundred MHz to GHz and are being used in communication systems.
Various designs of DDS are available today in the market designed on the basic principle of conventional DDS. A conventional DDS consists of a Phase accumulator, digital-analog converter (DAC) and a low-pass filter. The DAC consists of a sine ROM (read-only memory) and a Look up table (LUT). The performance of the DDS is mostly limited by the performance of the DAC. Many techniques have been suggested to improve the performance of the DDS such as a ROM-less DDS which employ computational methods such as CORDIC algorithms [2], Taylor series and parabolic approximation [4].

Whatever method is used the number of bits coming out of the phase accumulator has a direct influence on the size and complexity of sine wave mapping. For example if a 32-bit phase accumulator is being used and a 12 bit DAC, the size of the ROM would be $2^{32} \times 12$ bits. As such ROMs’ are power hungry devices the amount of power dissipation would be huge making the device in applicable for use. To counter this limitation number of output bits to the ROM is truncated to reduce the Rom size which in turn results in precision loss and these will appear as spurious frequencies on the output spectrum.

For signal synthesis DDS has become the preferred technique over its analog counterpart. The main advantages of DDS are precision, fast switching capability, sub-Hertz resolution, less susceptibility to aging and temperature changes. Ideally a DDS would achieve optimal values for all the 3 performance techniques [7] i.e., high accuracy, low-power and high-speed but practically only 2 metrics can be met. To increase the
accuracy, higher precision of N (number of bits), Q, and M (resolution of DAC) are required. Increasing the hardware complexity of the phase accumulator, phase- to-amplitude converter and the DAC these metrics can be met but at cost of increased power consumption and a slower clock frequency.

Using high-speed optimization techniques such as Pipelining, a high clock frequency is achievable while maintaining high accuracy, but power consumption has to be sacrificed due to higher complexity of the circuit. Conversely if low-power techniques are employed for high accuracy circuits then an optimal speed may not be achieved. Low-power and high frequency are possible but would require low-precision arithmetic components sacrificing accuracy.

Since only two optimal characteristics can be achieved it becomes of utmost important to understand the requirement of the target application. One of the popular target applications of a DDS are expected to be portable – wireless and satellite communications, which would require a DDS with low-power consumption and high accuracy.

Chapter 2 gives an overview of different types of frequency synthesizers such as Phase locked loops (PLL), Direct Analog synthesizers (DAS), Direct Digital Synthesizers (DDS) and Hybrid frequency synthesizers. This chapter also lists the limitations of Analog techniques compared to Digital techniques. We also discuss about Modulation techniques where DDS plays a vital role.
Chapter 3 gives the motivation behind this thesis and also discusses in detail the design of the Pulse output Direct Digital Synthesizer (PODDS) and Analog Filter Bank (AFB) [21]. It also talks about the differences between a conventional DDS and this work. In chapter 3, we also see the limitations in a conventional DDS caused by Digital to Analog Converter (DAC) and Read only Memory (ROM) in terms of Clock speed, Frequency range and Power.

Chapter 4 of this thesis gives a summary of results and compares this work with other previous works and also talks about future work and things that can be done to improve the PODDS.
2. Direct Digital Synthesizer

2.1 Introduction

An electronic device that accepts some reference frequency and then generates a frequency range as commanded by a control word or method, whereby the stability, accuracy and spectral purity of the output correlates with the performance of the input reference such a device is called as “Frequency synthesizer”. The quality of the device depends upon several performance factors such as the spectral purity, accuracy, Switching speed, and Phase noise and frequency range.

In the last two decades, frequency synthesizer has evolved from mainly analog to a mix of analog, radio-frequency (RF), digital and Digital signal processing (DSP) techniques. In general there are 3 major techniques to implement the function of Frequency synthesis:

1. Phase locked loop (PLL)
2. Direct Analog synthesizer (DAS)
3. Direct digital synthesizer (DDS).

2.1.1 Phase Locked Loops (PLL)

PLL is the technology of choice for generating radio frequency and microwave frequencies for radio applications. PLL, also known as Indirect synthesis, is a negative feedback loop structure that locks the phase of the output signal after division to the reference. Synthesis is simple because the variable counter (divider) N allows the generation of many frequencies F by changing the division ratio N.
\[ F = NF_r \] where \( F = \) output / desired frequency, \( F_r = \) reference frequency (2.1)

Changing \( N \) is made easy by the use of dual modulus devices, capable of dividing by two ratios.

From the above architecture of PLL, we observe that it is made of number of components. These blocks include a Reference Signal \( F_r \), that is derived from a crystal oscillator, a Phase frequency detector (PFD), a low pass filter (LPF), a voltage controlled oscillator (VCO) and a frequency divider \( N \), where \( N \) is an integer. We see in the architecture that the VCO output is fed back to the frequency divider, and comparison is done between the output signal and the VCO reference signal through the use of phase-frequency detector. As the output drifts the error signals are produced which then send correction commands to the VCO, which responds accordingly. Error detection and correction occur in the phase-frequency detector, which adds phase noise close to the carrier, though a PLL can outperform direct synthesis at larger offsets. Even with using
aggressive VCO pre-tuning techniques it’s difficult to achieve fast switching and fine steps degrade phase noise.

2.1.2 Direct Analog Synthesizer

This method, the first used to be in Frequency synthesis, derives the signals directly from the reference as compared to PLL, which it does indirectly. Direct analog uses building blocks such as Comb generators, mix and filter and dividers as the main tools. Many direct analog synthesizers use similar repeating blocks for for resolution. These blocks usually generate a 10 MHz band in the ultrahigh frequency (UHF) range, in 1 MHz steps, and after division they are used as an input to the next stage. Every stage divides by 10, thereby increasing the resolution. Most analog synthesizers traditionally use binary coded decimal (BCD) for control. This is losing importance because a computer controls all modern applications. One advantage of the direct analog synthesizers are signals are clean because they are derived directly from the crystal, however the complexity is high which comes at a high price. The other advantage of this synthesizer is the ability of rapid frequency range, the pure output spectrum, similar to the reference source and excellent phase noise because of direct process. However, the numbers of components are large making it a bulky, power hungry and expensive device.
2.1.3 Direct Digital Synthesizer

Direct digital synthesis is a Digital signal processing method [3] that generates and manipulates the signal in the numbers (digital) domain and eventually converts to its analog form via digital to analog converter (DAC).

Now we study in detail the operation of a conventional DDS. A DDS in its simplest form is a clock-dividing counter which generates a digitized ramp waveform. This ramp waveform is converted to a sine wave representation and subsequently translated to the analog domain by the DAC and subsequent filtering of the signal can be used to remove high frequency components.

The direct digital synthesizer (DDS) is shown in a simplified form in the figure 2.3. The direct digital synthesizer (DDS) or numerical controlled oscillator (NCO), are used to name this circuit. The DDS mainly consists of the following basic blocks; a Phase accumulator (PA), a phase to amplitude converter, a digital to analog converter (DAC)
and a low pass filter (LPF). The phase accumulator consists of a j-bit full adder and a j-bit phase register which stores a digital phase increment word. The digital input phase increment word is given one j-bit input of the full adder and the other j-bit input to the full adder is fed back from the phase register [8]. At every clock pulse this data is added to the data previously held in the phase register. The phase increment word represents a phase angle step that is added to the previous value at each \( 1/f_{clk} \) seconds to produce a linearly increasing digital value. The phase value is generated using the modulo \( 2^j \) overflowing property of a j-bit phase accumulator. The rate of the overflow is the output frequency.

\[
F_{out} = \Delta P f_{clk} / 2^j \quad \text{for all } F_{out} \leq f_{clk} / 2
\]  

(2.2)

Where \( F_{out} \) is the output frequency of the DDS, \( \Delta P \) is the phase increment word or also sometimes referred to as Frequency control word (FCW) or the tuning word; \( j \) is the number of the bits in the phase accumulator. The frequency resolution is found by setting \( \Delta P = 1 \). So the resolution is given by

\[
F_{out} = f_{clk} / 2^j
\]  

(2.3)

The read only memory (ROM) used in the phase – to-amplitude converter block is a sine look up table.

The output of the phase accumulator is fed to the ROM, which is a phase address. The ROM converts the digital value of this address to its corresponding sine value. In an ideal case with no phase and amplitude quantization the output sequence of the table is given by
\[ \sin \left( \frac{2\pi \text{P}(n)}{2^j} \right) \quad (2.4) \]

Where \( \text{P}(n) \) is a \( j \)-bit phase register value at the \( n \)th clock period.

The numerical period of the phase accumulator output sequence is defined as the minimum value of \( \text{P}_e \). For which \( \text{P}(n) = \text{P}(n + \text{P}_e) \). Numerical period in clock cycles is given by

\[ \text{P}_e = \frac{2^j}{\text{GCD}(\Delta \text{P}, 2^j)} \quad (2.5) \]

The numerical period of the sequence generated by the phase accumulator is same as that of the samples from Rom.

The output of the ROM is fed to the Digital – to – Analog converter (DAC) which converts the digital signal to quantized analog sine waves. To produce a sine wave having a fixed frequency, a constant value (Tuning word) is added to the phase accumulator with each clock cycle.

The output of the DAC contains high frequency components which may reduce the purity and the accuracy of the desired signal.

Therefore the performance and the choice of the filter play a pivotal role in elimination of these high frequency components to produce a error free and pure sine wave.
Fig 2.3 Basic architecture and Signal Flow of Direct Digital Synthesizer [1]

Let us consider an example which explains the concept of sine wave generation. We consider five bit input to the accumulator out of which the 3 MSBs are used to address an 8x8 ROM. For every complete clock cycle the address at the Rom is latched. For every clock cycle, the output of the accumulator corresponds to a unique address in the ROM. The value at this address is the output of the DAC. The output of the DAC is then fed to a low pass filter (LPF).

The accumulator is capable of generating 32 unique addresses since the bits are truncated and only 3 MSBs are considered only 8 unique addresses are created. Thus the values stored in the ROM correspond to one complete clock cycle.

To show a working example, consider the clock frequency $F_{\text{clk}}$ is 32 Hz. Let the Frequency control word (FCW) be 1. So after every clock cycle the values in the phase register is incremented by 1 and this process is continued until the adder overflows and all the values are set to zero.
<table>
<thead>
<tr>
<th>accumulator output</th>
<th>ROM Address</th>
<th>Phase angle generated</th>
<th>Contents of the ROM</th>
</tr>
</thead>
<tbody>
<tr>
<td>00000</td>
<td>000</td>
<td>0</td>
<td>10000000</td>
</tr>
<tr>
<td>00001</td>
<td>000</td>
<td>0</td>
<td>10000000</td>
</tr>
<tr>
<td>00010</td>
<td>000</td>
<td>0</td>
<td>10000000</td>
</tr>
<tr>
<td>00011</td>
<td>000</td>
<td>0</td>
<td>10000000</td>
</tr>
<tr>
<td>00100</td>
<td>001</td>
<td>45</td>
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<td>00101</td>
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</tr>
<tr>
<td>11111</td>
<td>111</td>
<td>315</td>
<td>00100110</td>
</tr>
</tbody>
</table>
The clock frequency of the synthesizer is mostly limited by the access time of the ROM and also the maximum operating frequency of analog components is much less when compared to digital. So to overcome these aforementioned limitations many Direct Digital synthesizers have been developed by eliminating the use of DAC and ROM [9]-[12].

### 2.2 Modulation Techniques Using DDS

In communication, modulation is the process of varying a periodic waveform in order to use that signal to convey a message. Normally a high frequency sinusoid waveform is used as the carrier signal. The three key parameters of a sine wave are its frequency, phase and amplitude.

Modulation techniques are classified as

- Digital modulation
- Analog modulation
- Digital baseband modulation
- Pulse modulation

#### 2.2.1 Analog modulation

In analog modulation, the modulation is applied continuously in response to the analog information signal. Commons methods of analog modulation are Amplitude modulation, Frequency modulation and phase modulation.
2.2.1.1 Amplitude Modulation

Amplitude modulation (AM) is a technique used in electronic communication, most commonly for transmitting information via a radio carrier wave. AM works by varying the strength of the transmitted signal in relation to the information being sent. Using a DDS Amplitude modulation can be implemented by adding a multiplier in between ROM and the DAC as shown in Fig 2.4.[16]

![Fig 2.4 Amplitude Modulation using DDS](image)

2.2.1.2 Frequency Modulation

Frequency modulation (FM) conveys information over a carrier wave by varying its frequency (contrast this with amplitude modulation, in which the amplitude of the carrier is varied while its frequency remains constant. For a special sub-set of frequency modulation, linear FM, or linear FM Chirp, the DDS has shown itself to be a viable
alternative to the existing (and limited) techniques used in the past such as voltage swept VCO's and fixed SAW devices. FM chirp modulation is used in advanced radar, anti-jam electronic warfare, and similar system architectures. Chirp signals have been traditionally complex to generate. VCOs have problems in linearity and total accuracy. Such systems had to be liberalized as well as kept at constant temperature and continuously calibrated. This makes the hardware complex and expensive. Linear FM is much more complex to generate in the analog domain.

Fig 2.5 Frequency Modulation using DDS [16]

2.3 Advanced DDS systems

DDS systems have good resolution, high-speed frequency switching speed and low power consumption when compared to its analog counter parts such as Phase locked loop (PLL) or Direct Analog Synthesizer (DAS). However they are limited by their spurious response and to an extent by their bandwidth and operating frequency which depends on the ROM access time. Direct analog synthesizers on the other hand provide very fast switching speed ranging from micro-to nano-seconds and its ability to generate very low phase noise output because of components like mixers employed in their design[15].
But the main limitation of this device is low frequency coverage and step size. Frequency coverage can be decreased but at the cost of increased circuitry. A solution to this would be employing a DDS to increase the minimum step size required. In Fig 2.5 we see how DDS is employed in a Analog synthesizer.

![Diagram of DDS employed in Analog synthesizer](image)

**Fig 2.6 Direct analog synthesizer using DDS at the Input [15]**

In chapter 3, we discuss in detail the design of PODDS and AFB. We talk about different components and their designs used to implement the frequency synthesizer. We also discuss about pipelining the Phase accumulator and its advantages and limitations. In chapter 3 we present the design of Analog filter bank which comprises of Chebyshev filters and how this AFB replaces a DAC and ROM present in a conventional DDS.
Chapter 4 of this work gives an overview of this work and discusses about various results obtained from this work and does a comparison with previous works and also talks about future work and improvements that can be done.
3. Design Methodology and Sub-system Design

3.1 Motivation

The main objective behind this work was to design and develop a frequency synthesizer which can clock in GHz and generate a wide frequency coverage ranging from MHz to GHz. A conventional DDS is limited by the speed at which it can clock and the frequency range it can generate. The main cause for this is the DAC and the ROM blocks present in a conventional DDS. To design a high speed conventional DDS, one would require a high resolution DAC and ROM, but has to compromise the area and the power which are key requirements in present world. With the fast evolution of wireless communication, where Small area and low power consumption and high speeds are key statistics; a need for such a device is enormous.

The main motivation for this work was to overcome the above mentioned limitations and to design a device which can operate at GHz frequency and consume low power and also give the user a wide frequency range to choose from. In this work we implement a PODDS and an AFB which eliminates the need for a DAC and ROM. In this work we intend to operate the device at 2.25GHz and generate a frequency range of 1.1MHz – 1.125GHz.
3.2 Introduction

The primary architecture of this design combines a Pulse output DDS (PODDS) with an Analog filter Bank (AFB) as shown in figure below to form a PODDS/AFB signal generator[21].

Fig 3.1 Pulse output Direct Digital Synthesizer/Analog Filter Bank (PODDS/AFB) Signal Generator

The DDS mentioned above consists of the followings core blocks.

- Phase accumulator
- De-Multiplexer
- Analog filter bank
- Analog multiplexer
The phase accumulator is essentially the same design as for the conventional DDS, with a digital accumulator that generates a digital ramp signal with a slope that is proportional to the j bit frequency select input. However, in this case the output is a pulse signal with a frequency that can be selected to be in the range of 1 MHz to 1.125 GHz. We used a 2.25 GHz clock as the system clock. After startup the time for switching frequencies will be tens of nanoseconds which will be determined by the number of pipelines in the phase accumulator and the delay of the De-multiplexer, Analog Filters, and Analog Multiplexer. The j-bit frequency select input to the phase accumulator will be 16 bits wide, so combining this with the 2.25 GHz clock the frequency resolution was found to be less than 0.034 MHz.

The frequency resolution (Δf) is found by setting Δp=1.

\[ \Delta f = \frac{f_{clk}}{2^j} \quad (3.1) \]

The pulse output of the phase accumulator is just the most significant bit of the accumulator output.

### 3.3 Phase Accumulator

The Phase accumulator consists of a phase register and an Adder. In this thesis a 16 bit Carry look ahead adder is implemented as fast switching between the frequencies is desired. In order to make the design work at 2.25GHz minimal pipelining is implemented to reduce the delay and the carry between the pipelining stages is latched. Discussed below is the architecture of the carry look ahead adder implemented in this thesis.
3.3.1 Carry Look Ahead adder.

The 16 bit accumulator is composed of 4 4 bit carry look ahead adders [13]. A Ripple carry adder is much slower when compared to a Carry look ahead adder. The carry has to ripple through successive stages making it undesirable when optimal speed is a performance parameter. In a carry look ahead adder, the carry look ahead logic will determine whether it will generate or propagate a carry. So when the actual addition is performed there is no ripple effect of the carry. The propagate and the generate functions can be determined by

\[
\text{Propagate } P = A + B \quad (3.3)
\]

\[
\text{Generate } G = A \cdot B \quad (3.4)
\]
The 1 bit adder can be cascaded to design a 4 bit Carry look ahead adder with necessary Carry look ahead logic \cite{13}

\[
C_{o,k} = G_k + P_k \left( G_{k-1} + P_{k-1}(\ldots+P_1(G_0 + P_0C_{i,0})) \right) \quad (3.5)
\]

This equation can be used to implement an N-bit adder. For every bit, the carry and sum outputs are independent of the previous bit. Thus the ripple effect has been effectively eliminated.

Shown below is the schematic of a 4 bit Carry Look ahead logic.
The Carry look ahead logic for this 4 bit adder was derived from the equation 3.5 and was found to be:

\[
\begin{align*}
C_1 &= P_0 \cdot C_0 + G_0 \\
C_2 &= G_1 + P_1 G_0 + P_1 P_0 C_0 \\
C_3 &= G_2 + G_2 P_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_0 \\
C_4 &= G_3 + G_3 P_2 + P_3 P_2 P_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_1 C_0
\end{align*}
\]

For any larger circuits, \(N>4\) the circuitry becomes complicated and fan-in problems arise because some gated would require more than 6 inputs.
The heart of the system is the phase accumulator whose contents are updated every clock cycle. Each time the phase accumulator is updated, the digital number stored, is added to the number in the phase accumulator register. Ideally a phase accumulator designed using a fully pipelined architecture [8] is preferred to avoid the delay in the outputs. For this design we would require 4 pipeline stages. Each pipelining level consists of 5 4-bit registers and a 4-bit carry look ahead adder. The number of d-flip flops requires for each pipeline is determined by the formula [8]

\[ (B \times (P^2 + P)) + P - 1 \]  \hspace{2cm} (3.2)

Where B is the number of bits per pipeline stage and P is the number of pipeline stages.
In total our design we need 83 D-flip flops. But in this designed we preferred a simple architecture for phase accumulator shown below is the architecture of the phase accumulator.

Fig 3.5 Schematic of 16 bit Phase accumulator

As against 295 D flip flops we require only 37 D flip flops which would decrease the amount of power dissipated considerably and also since there is no memory involved in this architecture as against a conventional DDS the switching between the frequencies has to be fast enough. Choosing a pipelined architecture would reduce the delay but
would be limited by the speed of switching between the frequencies. As an alternative we used a simple architecture for faster switching. The total average power dissipation is found to be only 25mW where as for Pipelined architecture it was found to be 50mW. Shown below are the simulation results for a phase accumulator operating at 2.25GHz. In fig 3.6 we see that the phase accumulator is able to generate a 1.12GHz frequency phase number as it was intended.

![Simulation results of Phase accumulator for input 1000 0000 0000 0000 (1.12GHz)](image)

Fig 3.6 Simulation results of Phase accumulator for input 1000 0000 0000 0000 (1.12GHz)

In fig 3.7 we see that it can generate a frequency as low as 4.4 MHz from these Simulations we observe that the phase accumulator is able to generate frequencies in the range of MHz- GHz.
Even though this we only require the MSB bit of the phase accumulator for generating the required frequency, this architecture can also be used for a conventional DDS.

3.4 De-Multiplexer.

The MSB bit of the Phase accumulator the phase and frequency information of the frequency control word (FCW) that is being given as an input to generate certain required frequency. This MSB is fed to a De-multiplexer as an input. At the output of the multiplexer is an Analog Filter bank. The multiplexer presents the input on its output bits. Depending upon the MSB bit frequency and the Frequency Control word (FCW) the input goes to the appropriate filter.
For example, if the FCW is 0100 0000 0000 0000. According to the tuning equation the required output should be 560MHz. So the de-multiplexer chooses the appropriate low-pass filter for the pulse output from the bank of Analog filters.

Fig 3.8 Schematic of 1:16 De-multiplexer
Fig 3.9 Schematic of 1:32 De-multiplexer

3.5 Analog Filter Bank.

The conventional DDS uses a phase amplitude converter (ROM) and a DAC to produce a sampled data sine wave output which is then filtered to remove harmonics to obtain a sine wave with the required spectral purity. The proposed architecture in this work eliminates the phase amplitude converter and DAC by incorporating an Analog Filter bank with a number of sharp cut off frequency low pass filters. The pulse wave output of the phase accumulator theoretically is composed of the fundamental sine wave and odd harmonics (3, 5, 7,). In a non-ideal implementation, there would also be even harmonics (2, 4, 6,) with less power than the odd harmonics, but which must be suppressed if only the fundamental is to remain at the output of the filter.
A pulse wave output of the phase accumulator can be expressed in a Fourier series. For a square wave with fundamental frequency $f_0$ and amplitude $A$ the Fourier series can be expressed as

$$4A/\pi \left( \sin(2\pi f_0 t) + 1/3 \sin(3\pi f_0 t) + 1/5 \sin(5\pi f_0 t) + 1/7 \sin(7\pi f_0 t) + \ldots \right)$$

From the series expansion above the square wave of frequency $f$ will become a sine wave of frequency $f$ if the higher harmonics are filtered out. So the main objective is an architecture which rejects the third and higher order harmonics.

### 3.5.1 Chebyshev Filter

We implemented the analog filter bank using chebyshev-I filter. Although Butterworth filters possess a monotonic response, they constrain other filter shape parameters like transition steepness, and out-of-band rejection. The response of butter worth filters is based on the minimization of error in the entire pass band, resulting in equi ripples or pass band ripples with equal amplitude. The greater the ripple amplitude allowed, the steeper the transition roll off. The chebyshev filters are also known as “Equiripple” or “Minimax” filters because of their characteristics.

The gain or the amplitude response of a chebyshev type I filter is given

$$G_n(\omega) = |H_n(j\omega)| = \frac{1}{\sqrt{1 + \epsilon^2 T_n^2 \left( \frac{\omega}{\omega_0} \right)}}$$

(3.6)

Where $\epsilon$ is the ripple factor, $\omega_0$ is the cut off frequency and $T_n(\cdot)$ is a Chebyshev polynomial of the $n$th order.
The pass band exhibits equi ripple behavior, with the ripple determined by the ripple factor $\varepsilon$.

\[ \text{Ripple in dB} = 20 \log_{10} \frac{1}{\sqrt{1 + \varepsilon^2}} \]  

(3.7)

The chebyshev response has the fastest rate of phase change.

The ABF is implemented with Low Pass Filters (LPFs) with bandwidths [0-1.5 MHz], [0-1.5*1.5 MHz], [0-1.5*1.5 MHz], [0-1.5*1.5 MHz]..., [0-1.5*1.5 MHz]. As seen from
fig 3.1 the Analog Filter Bank (AFB) would require 20 analog chebyshev low pass filters to cover the required frequency range. When outputs are required in the 1-1.5 MHz range, the pulse wave from the phase accumulator with the desired frequency would be routed to the top analog filter (LPF1) with a pass band of 0 to 1.5 MHz. The transition region to stop band is sharp enough to suppress the 2nd, 3rd, and higher order harmonics so the analog output would be a sine wave with spurs less than -40 dBc as required by the specification stated earlier. If an output is required in the 1.5 MHz to 2.25 MHz, then the pulse wave from the phase accumulator would be routed to the second filter with a pass band of 0 to 2.25 MHz.

Shown below in fig 3.9 is the schematic of a ninth order Chebyshev filter designed using only passive RLC components. The initial design of the filter was obtained based upon theoretical calculations and then iteratively changing those values to obtain the required cut off frequencies.

Fig 3.11 schematic of 9th order Chebyshev LPF, Pass Band 0 – 1.5 MHz

The frequency response was obtained using cadence analog environment tools and is shown in fig 3.11. From the fig 3.12 we observe that there is a sharp cutoff at 1.5 MHz frequency and the required pass band is obtained and the transition to the stop band is relatively sharp over 40 dB suppression of the 2 MHz 2nd harmonic.
A transient simulation was performed using cadence tools to obtain the output wave form as function of time with the pulse input. This result is shown in fig 3.13, where it is noted that the output is a sine wave with an amplitude of about half of the pulse wave input due to the filter design which incorporated a 50 ohm resistance at the input and the output.
A spectral purity analysis was performed on the filter and from fig 3.14, it seen that the Spurs are less than -58 dBC for the 1MHz output of the LPF filter with a pass band 0-1.5 MHz.

A similar transient analysis was performed on 1.4GHz filter output with 1.12GHz pulse wave input to obtain an output waveform as function of time with pulse wave input. This result is shown in fig 3.16.

Fig 3.14 FFT of 1.5 MHz Filter output with 1 MHz pulse wave input spurs <-58dBC

Fig 3.15 Schematic of Ninth order Chebyshev Filter pass band 0-1.4 GHz
A fast Fourier transform (FFT) performed on the simulated 1.12 GHz output of the filter to determine the harmonic spurs that are present in the output are shown in fig 3.17 below.
3.6 Digital Buffer

A digital buffer was also designed to drive the output of the de-multiplexer. The De-mux output is fed to the Analog filter bank. So it is very difficult for the output to drive the filter as they have high input capacitance. To be able to drive such high capacitances a buffer with multiple stages has been designed.

![Fig 3.17 Schematic of a digital Buffer](image-url)
This design was tested using cadence analog environment tools. It was tested with loads ranging up to 25pf.

Shown below in fig 3.18 and fig 3.19 are the transient response of the filters with loads 20pf and 15pf respectively.

![Fig 3.18 Transient Response of Digital Buffer with load 8pf](image)
3.6 Analog Multiplexer

The output of the Analog filter Bank is fed to a Multiplexer. Since the output of AFB is analog in nature i.e., a sine wave an analog multiplexer [14] is employed. The analog multiplexer is designed using transmission gates, NAND gates and Inverters. Shown below in Fig 3.14 is a 2:1 analog multiplexer.
But a 16:1 Analog multiplexer was designed by cascading 4 4:1 Analog multiplexers. In fig 3.21 we see the design of 4:1 Analog multiplexer and in fig 3.22 the transient response of the multiplexer.
In chapter 4 we discuss the various results obtained from the proposed PODDS and compare these results with the previous work and also verify whether the proposed frequency range was generated.
4. Simulations and Results

4.1 Results

Fig 4.1 shows the frequency generated by the Pulse output DDS for input 1000 0000 0000 0000 (1.1GHz)

![Simulation results of the Pulse output DDS for a Frequency Control word 0100 0000 0000 0000 (16384) and an output frequency of 560MHz](image)

A frequency control word of decimal equivalent 16384 (0100 0000 0000 0000) is given as an input to the Phase accumulator. At the output of the phase accumulator a phase number equivalent to the input is generated. This number is then routed to the Analog filter bank via the demultiplexer. Since the filter has high input capacitance, the load in the output signal of the phase accumulator is very high. To drive such a high load a
digital buffer is introduced. From the above figure it is clearly seen that a sine wave is generated corresponding to the control word value. The sine wave generated in this particular case is of 560MHz frequency.

The average power dissipated from the whole system is calculated to be 50.06mW out of which 25mW is contributed by the phase accumulator alone.

![Average power output of Pulse output DDS](chart.png)

**Fig 4.2 Average power dissipated from Pulse output DDS**

In fig 4.1, we have seen that for an output frequency of value 560MHz, the average power was found to be 50mW (see fig 4.2). When the PODDS was simulated for a maximum output frequency of value 1.12GHz the average power was found to 83mW.
Fig 4.3 Sine wave output of the PODDS with frequency value of 750 MHz

The table below shows the phase values and their corresponding frequencies

<table>
<thead>
<tr>
<th>Phase value</th>
<th>Output Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>32786</td>
<td>1.12GHz</td>
</tr>
<tr>
<td>8192</td>
<td>280MHz</td>
</tr>
<tr>
<td>2560</td>
<td>158MHz</td>
</tr>
<tr>
<td>1024</td>
<td>35MHz</td>
</tr>
<tr>
<td>32</td>
<td>1.1MHz</td>
</tr>
</tbody>
</table>
4.2 Summary

Technology: 0.18µm TSMC technology

Input clock: 2.25GHz

Number of input bits: 16

Output Frequency range: 1.1MHz – 1.125GHz

Average power: 83mW@ 1.12GHz

Minimum output frequency: 1.1MHz

Maximum output frequency generated: 1.125GHz

4.3 Comparisons

Table 4.2 comparisons between different DDS ICs[20]

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>.5µm CMOS</td>
<td>.8µm CMOS</td>
<td>.6µm CMOS</td>
<td>.18µm CMOS</td>
<td>.18µm CMOS</td>
</tr>
<tr>
<td>Max clock frequency</td>
<td>.23 @ 3.3 V</td>
<td>.03 @ 3.3 V</td>
<td>0.2 @ 3.3 V</td>
<td>1.25 @ 1.8 V</td>
<td><a href="mailto:2.25@1.8V">2.25@1.8V</a></td>
</tr>
<tr>
<td>(GHz)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Amplitude resolution</td>
<td>11</td>
<td>9</td>
<td>10</td>
<td>10</td>
<td>16</td>
</tr>
<tr>
<td>(bits)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power dissipation</td>
<td>92 mW @ 3.3 V</td>
<td>9.5mW @ 1.8 V</td>
<td>1.82 W @ 3.3 V</td>
<td>.43 W @ 1.8 V</td>
<td><a href="mailto:83mW@1.8V">83mW@1.8V</a></td>
</tr>
<tr>
<td>Transistor Count</td>
<td>-</td>
<td>-</td>
<td>430 000</td>
<td>18 700</td>
<td>-</td>
</tr>
<tr>
<td>Output Frequency Range</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>1MHz-312.5GHz</td>
<td>1.1MHz-1.125GHz</td>
</tr>
</tbody>
</table>
5. Conclusions and Future work

The Pulse output Direct Digital Synthesizer implemented in this operates at 2.25 GHz and has a 16 bit Phase accumulator and an Analog Filter Bank. The frequency range obtained was found to be 1.1MHz to 1.12GHz and the average power was found to be 83mW.

In this design the maximum frequency generated was found to be 1.125GHZ which is half the input clock frequency as compared to previous work (20) where it was only 0.25% of the input clock.

The maximum frequency that can be generated can be increased by increasing the input clock frequency which would require a much faster adder than implemented in this work and also the frequency resolution can be increased by increasing the input bits.
References


16. Technical Staff, Osicom technologies Inc, “A basic tutorial”.


Appendix

Fig A-1 Two input AND gate
Fig A-2 Two input XOR gate

Fig A-3 Two input OR gate

Fig A-4 Edge Triggered D flip flop
Fig A-5 Three input AND gate
Fig A-6 Three input OR gate
Fig A-7 Two input Demultiplexer

Fig A-8 Four input Demultiplexer