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Tunable All Electric Spin Polarizer

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Abstract

To realize the full potential of spin-based devices, ways must be found to inject, manipulate, and detect the spin of the electron by purely electrical means. In the past, our group has shown that a quantum point contact (QPC) with lateral spin orbit coupling (LSOC) can be used to create a strongly spin-polarized current by purely electrical means; that is in the absence of any applied magnetic fields. The LSOC results from the lateral in-plane electric field created by the confining potential in QPCs with in-plane side gates (SGs). Strongly spin-polarized currents can be generated by tuning the asymmetric bias voltages on the side gates. A conductance anomaly in the form of a plateau at conductance \( G \approx 0.5G_0 \) (where \( G_0 = 2e^2/h \)) was observed in the ballistic conductance of a QPC based in the absence of magnetic field – which was established to be a signature of complete spin polarization. A Non-Equilibrium Green’s Function (NEGF) analysis was used to model a small QPC and three ingredients were found to be essential to generate a strong spin polarization: (1) LSOC, (2) an asymmetric lateral confinement, and (3) a strong electron-electron (e-e) interaction. Our group has also shown that electric control of spin polarization of a QPC can be achieved for different materials (InAs and GaAs), electron mobility, heterostructure design, QPC dimensions and strength of LSOC.

Some of the previous experimental and theoretical results have also found the presence of other conductance anomalies (i.e., at values different from 0.5 \( G_0 \)) and the main reason for these occurrences was shown to be due to the influence of surface roughness scattering. In this thesis, we address the important technological challenge to better control the location of the conductance anomalies in QPCs and create a tunable all-electric spin polarizer based on a QPC with four gates,
i.e., with two in-plane SGs in series. In this device, the first pair of SGs, near the source, is asymmetrically biased to create spin polarization in the QPC channel. The second set of gates, near the drain, is symmetrically biased and that bias is varied to maximize the amount of spin polarization in the channel. We have fabricated several InAs based QPCs with four SGs and have shown that some of the experimental results were in qualitative agreement with our NEGF simulations. Our main finding is that the range of common mode bias on the first set of gates over which maximum spin polarization can be achieved is much broader for the four gate structure compared with the case of a single pair of in-plane SGs.

In addition, we have observed both *hysteresis* and *negative differential regions* in the conductance of the device for specific biasing conditions. We believe these results are evidence of Coulomb and Spin Blockade effects on the conductance of these structures, features which cannot be explained within the context of a NEGF approach and require a many-body approach to the description of carrier transport. Our studies suggest that the study of spin valve structures composed of a quantum dot or wire coupled to the source and drain via asymmetrically biased QPCs should open a new area in the field of spintronics. With an asymmetric bias on the gates of the two QPCs, their spin filtering, when combined with Coulomb blockaded transport through the active channel, should lead to spin-blockaded transport through the spin valve. When operated close to threshold, all electrical spin valves could be used to investigate new many-body effects, such as electrically controlled spontaneous spin polarization, Wigner crystallization and formation of spin lattices in nanoscale devices, which are burgeoning fields of spintronics research.
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List of Contents

1. Introduction to Spintronics................................................................. 1
   1.1 Overview.......................................................................................... 1
   1.2 Spintronics....................................................................................... 3
   1.3 The Datta-Das SpinFET................................................................. 5
   1.4 Why all electric spintronics?......................................................... 8
   1.5 Mesoscopic systems..................................................................... 9
   1.6 Quantized Conductance in Quantum Point Contacts (QPCs) ....... 10
   1.7 Spin Orbit Coupling (SOC)........................................................... 16
      1.7.1 Rashba SOC............................................................................ 17
      1.7.2 Dresselhaus SOC................................................................. 19
      1.7.3 Lateral Spin Orbit Coupling (LSOC)...................................... 21
   1.8 Spin relaxation mechanisms in 1D system.................................... 23
   1.9 Thesis Outline.............................................................................. 25

2. Background......................................................................................... 30
   2.1 Review of Previous Work............................................................. 30
   2.2 Spin Polarization Due to LSOC.................................................... 30
   2.3 Influence of Surface Scattering..................................................... 33
   2.4 QPC with two pairs of in-plane side gates.................................... 42

3. Device Fabrication and Characterization.......................................... 45
   3.1 Introduction.................................................................................... 45
   3.2 Molecular Beam Epitaxy (MBE)..................................................... 46
   3.3 InAs/InGaAs/InAlAs heterostructure........................................... 49
   3.4 Device Fabrication and Processing Steps.................................... 52
      3.4.1 Pre-Process Cleaning............................................................ 53
      3.4.2 Defining the QPC using E-beam Lithography....................... 54
      3.4.3 Photolithography................................................................. 59
      3.4.4 Metal contact deposition and patterning.............................. 64
      3.4.5 Annealing.............................................................................. 65
List of Figures

Fig 1.1: Schematic of the Stern-Gerlach experiment. The beam of silver ions from the effusion cell is focused into a narrow beam and passes through a non-homogeneous magnetic field. The beam is deflected in either direction depending on the orientation of the spin. The figure on the right shows the cross sectional view of the magnet. The shape of the magnet used in the experiments gives rise to a non-homogeneous field between the poles............................................ 2

Fig 1.2: Number of transistor per dollar at various technology nodes. ......................... 4

Fig 1.3: Schematic of the Datta-Das spin-FET. The source and drain contacts are assumed to be half-metallic contacts (ideal ferromagnets) carrying only one type of spins. In the channel, there is a precession of the injected spins due to the effective magnetic field associated with the gate controlled spin-orbit coupling in the channel, referred to as Rashba spin orbit coupling…. 7

Fig 1.4: Formation of a two-dimensional electron gas (2DEG) of an AlGaAs/GaAs hetero-interface. Z is the direction of growth of the heterostructure............................................. 12

Fig 1.5: Schematic illustrations of (a) QPC constriction created by two surface gates (upper gate - UG and lower gate - LG) deposited on the surface of a semiconductor heterojunction (b) AlGaAs/GaAs heterostructure with 2DEG at the interface depleted by surface Schottky gates to create a one dimensional electron gas (1DEG) system. (c) Energy subbands in a 1DEG as a result of quantum confinement produced by the top surface gates. ............................................. 12

Fig 1.6: Experimental observation of conduction quantization in a split gated QPC as a function of voltage applied to the top gates. ................................................................. 16

Fig. 1.7: Illustration of Zeeman spin splitting in presence of an external magnetic field of intensity B; g is the gyromagnetic factor of the semiconductor and $\mu_B$ is the Bohr magneton......... 17
Fig. 1.8: Zeeman spin splitting of the first quantized plateau in presence of an external magnetic field B. The appearance of the 0.5\(G_0\) conductance plateau indicates that the spin degeneracy is lifted.

Fig. 1.9: Energy dispersion relations in a 1D semiconducting channel as a result of RSOC as used in Datta-Das in their proposal of the first SpinFET.

Fig. 1.10: (a) Schematic of a 1D quantum wire, the direction of current flow is indicated by the arrow. (b) The confining potential along the y-direction which is perpendicular to the motion of the electrons (along x-direction). In presence of LSOC, this leads to the accumulation of electrons with opposite spin along the edges of the wire.

Fig 1.11: An Atomic Force Microscope image of a QPC with two in-plane side gates designated as G1 and G2.

Fig 1.12: (a) Linear conductance in units of \(G_0\) \((2e^2/h)\) of a QPC measured at both gate symmetric (S) and asymmetric (AS) bias condition. The plot for AS shows a conductance plateau near 0.5\(G_0\). The bias asymmetry between the two side gates is 7.5V. The sweep voltage is superimposed on the potentials \(V_{G1}\) and \(V_{G2}\) applied to the gates to create the asymmetry. \(V_G\) is the common sweep voltage applied simultaneously to both side gates (the plots were smoothened using 5 point averaging method) [31] (b) Plot of conductance of another QPC (in units of \(2e^2/h\)) as a function of the common sweep voltage \(V_G\). The potential applied to gate G2 is fixed at -1.0V. The leftmost curve corresponds to the actual conductance data for the symmetric case, i.e., with only the common sweep voltage \(V_G\) applied to the two gates. The other plots have been shifted to the right for clarity. From left to right, the potentials on gate G1 are equal to 0, 0.4, 0.8, 1.2, 1.6, 2.0, 2.4, 2.8, 3.2, 3.6, 4.0, 4.4, 4.8 and 5.2V, respectively [48]. In Fig.1.12 (b) the conductance anomaly is below 0.5\(G_0\).

Fig. 1.13: Schematic of proposed four-gate QPC device to achieve better control of spin polarization. S and D denotes the source and the drain contacts, respectively. In this thesis, we
study the conductance of this QPC as a function of the potential on the left ($G_1$, $G_2$) and right ($G_3$, $G_4$) pairs of in-plane SGs.

Fig. 2.1: (a) Scanning electron micrograph of a side-gated InAs QPC. Dark areas represent isolation trenches. Arrows schematically show spin orientations of incoming and outgoing (polarized) electrons. Electrons travel along x-axis. UG and LG are the in-plane SGs. (b) Potential profile in the channel region of the QPC calculated using NEGF simulations.

Fig. 2.2: (a) Schematic representation of the transverse confining potential profile of a side-gated QPC. I and II represent the two edges of the QPC channel. $B_{SO}$ is the effective magnetic field induced by LSOC. Blue (dashed) and yellow curves correspond to the symmetric and asymmetric bias between the two SGs, respectively.

Fig 2.3: Linear conductance in units of $2e^2/h$ of a QPC measured for both symmetric (S) and asymmetric (AS) bias between the two SGs. The plot for AS shows the 0.5 plateau. Here, $V_G$ is common sweep voltage applied simultaneously to both SGs.

Fig 2.4: Schematic of the QPC configuration used in the NEGF simulations. The width and length of the narrow portion of the QPC is equal to $w_2$ and $l_2$, respectively. In the simulations, the dimensions used were $w_2$, $l_2$, $w_1$, $l_1 = 16, 32, 48, and 64$ nm, respectively. The impurity locations 1,2,3,4,5 correspond to the coordinates $y_1 = w_1/2$ and $x_1 = 16, 24, 32, 40, and 48$ nm, respectively.

Fig. 2.5: Conductance as a function of $V_{sweep}$ for a QPC containing an impurity (either attractive (positive) or repulsive (negative)) at location 3 in Fig.2.4. Also shown for comparison are the results with no impurity (0 meV) in the channel.

Fig. 2.6: A three-dimensional AFM image of a QPC with two in-plane gates (G1 and G2), fabricated using a chemical wet etching technique. The current flows in the x-direction. An asymmetric LSOC is generated using an asymmetric bias between the two SGs generating an electric field in the y-direction. As seen in the figure, the side walls of the QPC are rather ragged, most likely due to the wet etching process used to define the trenches. Surface scattering from this
roughness plays a critical role in the observation of the anomalous conductance plateau ($G < 2e^2/h$).

Fig. 2.7: The conductance of an InAs QPC (in units of $2e^2/h$) measured as a function of the common sweep voltage $V_G$ applied to the in-plane gates, at $T=4.2$ K [34, 48]. The sweep voltage $V_G$ is superimposed on initial potentials $V_{G1}$ and $V_{G2}$ applied to the gates to create an asymmetry. The left-most curve shows the actual conductance data for the symmetric case; i.e., with only the common sweep voltage $V_G$ applied to the gates. The other curves have been shifted to the right for clarity. Thus, from left to right, the initial potential $V_{G2}$ applied to gate G2 is fixed at -2.0V and the initial potential $V_{G1}$ on gate G1 is equal to 0.0, -0.1, -0.3, -0.6, -0.9, -1.2, -1.5, -1.8, -2.0, -2.3, -2.6, -2.9, -3.1, -3.4, -3.7, -4.0, -4.5, -5.0, -5.5 and -6.5 V, respectively. ……………………

Fig. 2.8: Illustration of the conduction band energy profile between the two SGs, along a line through the middle of the QPC and perpendicular to the direction of current flow. The numbers 1, 2, 3 represent dangling bonds on either side of the channel. $E_f$ is the Fermi level of the source contact. Figures (a) and (b) show the conduction profile for opposite polarities of the potential between the two SGs [48]. …………………………………………………………………………

Fig 2.9: (a) Atomic force micrograph of 4-gate QPC device. (b) Schematic of four-gate QPC device denoting the two sets of in-plane SGs. S and D denotes the source and the drain contacts, respectively. In the actual structure shown on the left, the separation $x$ between the two sets of in-plane split gates is 200 nm, the width of the narrow portion of the QPC is 275 nm, and the length of both sets of split gates is 600 nm………………………………………………………………………

Fig. 3.1: A schematic diagram of a MBE system showing its different components………

Fig 3.2: Knusen Cell……………………………………………………………………………………………

Fig. 3.3: InAs/InGaAs heterostructure……………………………………………………………………

Fig 3.4: InAs/InGaAs heterostructure band diagram………………………………………………

Fig 3.5: Quantized energy levels inside the potential well…………………………………………

Fig 3.6: The spin speed versus film thickness curves for different Anisole content………
Fig. 3.7: Raith 150 e-beam lithography system available in UC Cleanroom

Fig 3.8: Schematic of e-beam exposure system.

Fig 3.9: Screen shot of exposure parameter calculation in the Raith software.

Fig 3.10: E-beam CAD design for Four gate QPC.

Fig 3.11: Photolithography using positive (left) and negative (right) photoresist.

Fig 3.12: Spin speed curves.

Fig 3.13: A Karl Suss MJB3 Mask Aligner.

Fig 3.14: KLA TENCOR P-15 Profilometer.

Fig 3.15: On the left - Photomask for patterning isolation trenches. On the right - Photomask for patterning ohmic contacts.

Fig 3.16: Metal contacts with bonding wires.

Fig 3.17: Schematic diagram of an AFM showing the different components.

Fig 3.18: NCS15/AIBS tip and tip specifications.

Fig. 3.19: A Veeco Dimension 3100 Model of AFM used in this work [82].

Fig 3.20: AFM scan of a typical QPC device showing trench width, channel width and trench depth of a QPC along with the spacing between the two sets of in-plane SGs.

Fig 3.21: Tempress 1713-10C wafer scriber.

Fig. 3.22: A wire bonded device.

Fig. 3.23: L-He Dewar used for low temperature measurement.

Fig 3.24: (a) Picture of the sample holder section of the DR probe insert showing the chip being held by the chip holder socket. (b) The far end of the DR probe insert with its main components marked.
Fig. 3.2: (a) Typical schematic of a QPC device with four in-plane side gates. The source and drain are designated as ‘S’ and ‘D’. G1 and G2 represent the gates of QPC1 and G3 and G4 are the gates for QPC2.

Fig 3.2: An AFM image of the QPC device showing the channel region and the side gates. Dark red areas are the isolation trenches cut by e-beam lithography and wet etching technique to define the SGs.

Fig 3.2: Circuit used to measure the conductance of each of the QPCs of the device.

Fig 4.1: 3D AFM image of the QPC with two sets of in-plane SGs.

Fig 4.2: Proposed four-gate QPC device. In the simulations, the potential on the two side gates close to the source was set equal to \( V_{\text{sg1}} = -0.2 \, \text{V} + V_{\text{sweep}} \), \( V_{\text{sg2}} = +0.2 \, \text{V} + V_{\text{sweep}} \), \( V_s = 0.0 \), and \( V_d = 0.3 \, \text{mV} \). The potential on the two SGs next to the drain was kept the same at a fixed value. The current flows in the x-direction.

Fig. 4.3: Conductance versus \( V_{\text{sweep}} \) of a four-gate QPC with the following parameters: \( w_1 = 48 \, \text{nm}, \, l_1 = 80 \, \text{nm}, \, w_2 = 16 \, \text{nm}, \, l_2 = 22 \, \text{nm}, \, d = 4 \, \text{nm} \). \( G_T \) is the total conductance and \( G_{\text{up}} \) and \( G_{\text{down}} \) the contributions from the up spin and down spin electrons. The biases on the gates are set to be \( V_{G_1} = -0.2 + V_{\text{sweep}} \), \( V_{G_2} = +0.2 + V_{\text{sweep}} \), and \( V_{G_3} = V_{G_4} = 0.0 \, \text{V} \). Also shown for comparison is \( G_T \) for a QPC with only two gates, with the same bias but for \( l_2 = 22 \) and 48 nm.

Fig. 4.4: Total conductance versus \( V_{\text{sweep}} \) of a four-QPC with the following parameters: \( w_1 = 48 \, \text{nm}, \, l_1 = 80 \, \text{nm}, \, w_2 = 16 \, \text{nm}, \, l_2 = 22 \, \text{nm}, \, d = 4 \, \text{nm} \). The biases on the gates close to the source are set as follows: \( V_{G_1} = -0.2 + V_{\text{sweep}} \), \( V_{G_2} = +0.2 + V_{\text{sweep}} \). The biases on the two gates close to the drain are set equal: \( V_{G_3} = V_{G_4} = 0.0, -0.1, \) and -0.2V, respectively. All calculations were performed using \( V_S = 0.0, \, V_d = 0.3 \, \text{mV} \) and \( T = 4.2\, \text{K} \).

Fig. 4.5: Spin conductance polarization \( \alpha = (G_{\text{up}} - G_{\text{down}})/(G_{\text{up}} + G_{\text{down}}) \) versus \( V_{\text{sweep}} \) of a four-gate QPC with the following parameters: \( w_1 = 48 \, \text{nm}, \, l_1 = 80 \, \text{nm}, \, w_2 = 16 \, \text{nm}, \, l_2 = 22 \, \text{nm}, \, d = 4 \, \text{nm} \). The different curves correspond to the biasing conditions \( V_{G_1} = -0.2 + V_{\text{sweep}} \), \( V_{G_2} = +0.2 + V_{\text{sweep}} \) for a QPC with a single set of in-plane gates and a length of the narrow portion of the QPC equal
to $2l_2 + d = 48\text{nm}$. The following parameters were used $V_S = 0.0$, $V_d = 0.3 \text{ mV}$ and $T = 4.2K$.

Fig. 4.6: Conductance of four gate InAs QPC device shown in Fig. 4.1 for $V_{G1} = -1.0 + V_{\text{sweep}}$ and $V_{G2} = 0.0 + V_{\text{sweep}}$ for different values of the same potential applied to gates 3 and 4 as shown in the inset. Measurements were taken at $T = 4.2K$. The voltages $V_{G3}$ and $V_{G4}$ are identical. No common sweep voltage is added to these two gates. The leftmost curves are the actual conductance data for $V_{G3} = V_{G4} = -2.8 \text{ V}$, all the other curves have been shifted to the right for clarity.

Fig. 4.7: Conductance of four gate QPC device shown in Fig. 4.1 with $V_{G1} = -0.4 + V_{\text{sweep}}$ and $V_{G2} = -0.7 + V_{\text{sweep}}$ for different values of the potential applied to gates 3 and 4 as shown in the inset. Measurements were taken at $T = 4.2K$. The voltage $V_{G3}$ is varied from $-0.3\text{V}$ to $-1.7\text{V}$ (from left to right) in steps of $-0.1\text{V}$. $V_{G4}$ is held constant at $-0.3\text{V}$. The leftmost curves are the actual conductance data for $V_{G3} = V_{G4} = -2.8 \text{ V}$, all the other curves have been shifted to the right for clarity.

Fig. 4.8: Conductance of four gate QPC device shown in Fig. 4.1 for $V_{G1} = -0.4 + V_{\text{sweep}}$ and $V_{G2} = -0.7 + V_{\text{sweep}}$ for different values of the potential applied to gates 3 and 4 as shown in the inset. Measurements were taken at $T=4.2K$. The voltage $V_{G3}$ is varied from $-1.7\text{V}$ to $-0.3\text{V}$ (from left to right) in steps of $0.1\text{V}$. $V_{G4}$ is held constant at $-0.3\text{V}$.

Fig. 4.9: Conductance of four gate QPC device shown in Fig. 4.1 for $V_{G1} = -0.4 + V_{\text{sweep}}$ and $V_{G2} = -0.7 + V_{\text{sweep}}$ for different values of the potential applied to gates 3 and 4 as shown in the inset. Measurements were taken at $T=4.2K$. The voltage $V_{G4}$ was varied from $-0.3\text{V}$ to $-1.7\text{V}$ (from left to right) in steps of $-0.1\text{V}$. $V_{G3}$ was held constant at $-0.3\text{V}$.

Fig. 4.10: Conductance of four gate QPC device shown in Fig. 4.1 for $V_{G1} = -0.4 + V_{\text{sweep}}$ and $V_{G2} = -0.7 + V_{\text{sweep}}$ for different values of the potential applied to gates 3 and 4 as shown in the inset. Measurements were taken at $T=4.2K$. The voltage $V_{G4}$ was varied from $-1.7\text{V}$ to $-0.3\text{V}$ (from left to right) in steps of $0.1\text{V}$. $V_{G3}$ was held constant at $-0.3\text{V}$. 

Fig. 4.11: Conductance of four gate QPC device shown in Fig. 4.1 for $V_{G1} = -0.4 + V_{\text{sweep}}$ and $V_{G2} = -0.7 + V_{\text{sweep}}$ for different values of the potential applied to gates 3 and 4 as shown in the inset. Measurements were taken at $T=4.2K$. The voltage $V_{G4}$ was varied from $-1.7\text{V}$ to $-0.3\text{V}$ (from left to right) in steps of $0.1\text{V}$. $V_{G3}$ was held constant at $-0.3\text{V}$.
Fig. 4.11(a): Conductance vs $V_{\text{sweep}}$ for $V_{G1} = -1.0 + V_{\text{sweep}}$ and $V_{G2} = 0.0 + V_{\text{sweep}}$. The second set of gates is biased symmetrically with a negative bias $V_{G3} = V_{G4} = -3.5$ V. No sweep voltage is superimposed on gates 3 and 4. All measurements were taken at $T = 4.2$K.............. 93

Fig. 4.11(b): Conductance vs $V_{\text{sweep}}$ for $V_{G1} = -1.0 + V_{\text{sweep}}$ and $V_{G2} = 0.0 + V_{\text{sweep}}$. The second set of gates is biased symmetrically with a high negative bias $V_{G3} = V_{G4} = -4.0$ V. No sweep voltage is superimposed on gates 3 and 4. All measurements were taken at $T = 4.2$K.............. 94

Fig. 4.11(c): Conductance vs $V_{\text{sweep}}$ for $V_{G1} = -1.0 + V_{\text{sweep}}$ and $V_{G2} = 0.0 + V_{\text{sweep}}$. The second set of gates is biased symmetrically with a high negative bias $V_{G3} = V_{G4} = -4.5$ V. No sweep voltage is superimposed on gates 3 and 4. All measurements were taken at $T = 4.2$K.............. 94

Fig. 4.12 (a): Schematic of QPC with a pair of in-plane SGs with gate contacts $G_1$, $G_2$, $G_3$, and $G_4$. (b) Energy levels corresponding to single electron picture of carrier transport through four gate QPC device. (c) Coulomb blockade picture of carrier transport through the four gate QPC device. $E_F$ is the Fermi level across the entire structure and is assumed to be constant since the source and drain potential is small................................................................. 98

Fig. 4.13(a): Conductance vs $V_{\text{sweep}}$ for $V_{G1} = 0.0 + V_{\text{sweep}}$ and $V_{G2} = 0.0 + V_{\text{sweep}}$. The second set of gates is biased symmetrically with a high negative bias $V_{G3} = V_{G4} = -4.1$ V. No sweep voltage is superimposed on gates 3 and 4. All measurements were taken at $T = 4.2$K.............. 101

Fig. 4.13(b): Conductance vs $V_{\text{sweep}}$ for $V_{G1} = 0.0 + V_{\text{sweep}}$ and $V_{G2} = 0.0 + V_{\text{sweep}}$. The second set of gates is biased symmetrically with a high negative bias $V_{G3} = V_{G4} = -4.2$ V. No sweep voltage is superimposed on gates 3 and 4. All measurements were taken at $T = 4.2$K.............. 102

Fig. 4.13(c): Conductance vs $V_{\text{sweep}}$ for $V_{G1} = 0.0 + V_{\text{sweep}}$ and $V_{G2} = 0.0 + V_{\text{sweep}}$. The second set of gates is biased symmetrically with a high negative bias $V_{G3} = V_{G4} = -4.3$ V. No sweep voltage is superimposed on gates 3 and 4. All measurements were taken at $T = 4.2$K.............. 102

Fig. 4.13(d): Conductance vs $V_{\text{sweep}}$ for $V_{G1} = 0.0 + V_{\text{sweep}}$ and $V_{G2} = 0.0 + V_{\text{sweep}}$. The second set of gates is biased symmetrically with a high negative bias $V_{G3} = V_{G4} = -4.35$ V. No sweep voltage is superimposed on gates 3 and 4. All measurements were taken at $T = 4.2$K.............. 103
Fig. 4.13(e): Conductance vs $V_{\text{sweep}}$ for $V_{G1} = 0.0 + V_{\text{sweep}}$ and $V_{G2} = 0.0 + V_{\text{sweep}}$. The second set of gates is biased symmetrically with a high negative bias $V_{G3} = V_{G4} = -4.4$ V. No sweep voltage is superimposed on gates 3 and 4. All measurements were taken at $T = 4.2$K.

Fig 5.1: SEM image of a dual QPC spin valve recently fabricated in our lab. The length of the middle section is roughly 1 micron. Spin precession in the central portion of the spin valve is controlled by LSOC in that region. The central portion of the spin valve must be much smaller than the spin diffusion length in the semiconducting channel.
Chapter 1

Introduction to Spintronics

1.1 Overview

In 1922, the famous Stern-Gerlach experiment was performed by Otto Stern and Walther Gerlach in Frankfurt, Germany. At the time of the experiment the idea of spin had not been developed and the experiment was conducted to study the space quantization as predicted by Bohr. The idea that an electron has spin, in addition to the charge, was first proposed by Ralph de Laer Kronig in 1925 and was further developed by Uhlenbeck and Goudsmit in 1926 [1, 2]. The schematic of the experimental set up used for the Stern-Gerlach is shown in Fig 1.1. Depending on the orientation of the spin, the beam of silver ions emanating through the small hole in a heated cavity was found to be deflected in opposite directions, after passing through the poles of the magnet with a non-homogeneous magnetic field. It took another five years to establish that deflection of the beam in presence of an external magnetic field was due to spin splitting in the non-homogeneous magnetic field. The Stern-Gerlach experiment remains one of the most fundamental experiments in the history of spintronics. By the middle of the 20th century, it was realized that spin plays a very important role in explaining magnetism and since 1988, the spin properties of an electron have been investigated for practical applications in electronics. This new area of research is referred to as “Spintronics”.

1
Fig 1.1: Schematic of the Stern-Gerlach experiment. The beam of silver ions from the effusion cell is focused into a narrow beam and passes through a non-homogeneous magnetic field. The beam is deflected in either direction depending on the orientation of the spin. The figure on the right shows the cross sectional view of the magnet. The shape of the magnet used in the experiments gives rise to a non-homogeneous field between the poles.
In agreement with Gordon Moore’s prediction in 1965, the density of transistors in a semiconductor chip has increased ever since in a geometric progression, roughly doubling every 18 months. A projected density of $10^{13}$ transistors per cm$^2$ is anticipated by 2017 with device dimensions in the nanoscale range. In the past decade, keeping up with Moore’s prediction has raised several challenges [3]. The biggest problem facing the semiconductor industry is that the on-chip heat sinking technology has lagged behind Moore’s prediction, projecting chip meltdown within a few generations of modern integrated circuits. This doomsday has been dubbed the *Red Brick Wall* by the International Technology Roadmap for Semiconductors. The upmost challenge is to find alternatives to the current semiconductor technology which would lead to a drastic reduction in energy dissipation during device operation.

1.2 Spintronics

As device dimensions shrink, quantum effects play a more dominant role in device performance which opens the possibility of developing new class of devices based on fundamentally different operating principles. It is expected that spintronics would provide a breakthrough in application of new quantum devices and circuits with applications ranging from quantum information processing to quantum computing [4, 5, 6]. Research in spintronics has rapidly progressed since the discovery of the giant magnetoresistance (GMR) effect by Albert Fert and Peter Grünberg in the late 1980s revolutionized the storage industry and has since led researchers to develop spin based logic devices for better functional integration of both logic and storage on the same chip [7,8]. GMR is the first and best example of an important application of the field of spintronics.
Numerous semiconductor spintronic devices have been proposed since then such as spin-MOSFET [9, 10], the spin Lifetime Transistor [11-13], the Spin Bipolar Transistor [14] and the most widely known Spin Field Effect Transistor (SpinFET) pioneered by Supriyo Datta and Biswajit Das [15].
1.3 The Datta-Das SpinFET

Hereafter we analyze the spin based device proposed by Datta and Das in 1990 which is considered as the archetype of many spin based transistors [15]. The schematic of the device is shown in Fig 1.3. The proposed structure uses ferromagnetic (FM) contacts for injection and detection of spin. Electrons are injected into the channel from the ferromagnetic source with a definite spin, which depends on the spin polarization in the FM contacts. This can only be achieved with ideal half-metallic contacts which are an area of intensive research. Assuming that the spin polarization in the FM source is along the x-direction, the electrons are injected as shown in Fig. 1.3. At the drain end, the electron’s transmission probability depends on the relative alignment of its spin with the drain’s magnetization. By controlling the amount of spin precession in the semiconducting channel with a gate voltage, the relative spin alignment at the drain end can be modulated allowing a fine tuning of the source-to-drain current. This realizes the basic “transistor” action. Because of this attribute, the Datta-Das device came to be known as the ballistic spin field effect transistor (SpinFET). When the gate voltage is turned on, it leads to a $y$-directed electrical field which controls Rashba spin-orbit coupling (RSOC) in the channel. A quantitative discussion for the Datta-Das SpinFET is as follows. The gate voltage $V_G$ controls the spin precession of the electron as it goes from the source contact to the drain contact. The spin orbital Hamiltonian for Rashba spin orbital coupling (RSOC) is given by [16];

$$H_{RSOC} = q\beta\sigma \cdot \hat{k}_s \times \vec{E}_y,$$  \hspace{1cm} (1.1)

where $\beta$ is the intrinsic SOC parameter, $\sigma$ is the vector of Pauli spin matrices, $\vec{E}_y$ is the $y$-directed gate electric field.

Following the derivation of [16], we define the effective magnetic field $\vec{B}_{RSOC}$,
\[ B_{RSOC} = \left[ \frac{2m^*a_{46}}{g\mu_B h} \right] E_y k_F \]  \hspace{1cm} (1.2)

where \( g \) is the Lande factor, \( m^* \) is the effective mass for electron in the channel, \( k_F \) is the Fermi wave vector in the x-direction. The effective magnetic field \( B_{RSOC} \) is along the z-axis and it causes the electrons to execute a Larmor precession in the x-y plane as they travel from the source to drain. The coefficient \( a_{46} \) is a material constant which depends on the bandgap, \( E_g \) and the spin-orbit split-off energy in the valence band \( \Delta_s \). For GaAs, \( a_{46} \) is \( 10^{-38} \text{ C-m}^2 \) [16].

\[
a_{46} = \frac{\pi e h^2}{m^*} \frac{\Delta_s (\Delta_s + 2E_g)}{E_g (\Delta_s + E_g)(2\Delta_s + 3E_g)} m^* \] \hspace{1cm} (1.3)

The angular frequency of the Larmor precession [17] is given by

\[
\Omega = \frac{d\phi}{dt} = \frac{g\mu_B B_{Rashba}}{h} \] \hspace{1cm} (1.4)

Therefore the spatial rate of precession along the semiconducting channel is given by

\[
\frac{d\phi}{dx} = \frac{d\phi}{dt} \frac{dt}{dx} = \frac{d\phi}{dt} \frac{1}{v_x} = \frac{2a_{46}m^*}{\hbar^2} E_y v_x, \] \hspace{1cm} (1.5)

\[
\phi = \left[ \frac{2a_{46}m^*}{\hbar^2} E_y \right] L, \] \hspace{1cm} (1.6)
Fig 1.3: Schematic of the Datta-Das spin-FET [15]. The source and drain contacts are assumed to be half-metallic contacts (ideal ferromagnets) carrying only one type of spins. In the channel, there is a precession of the injected spins due to the effective magnetic field associated with the gate controlled spin-orbit coupling in the channel, referred to as Rashba spin orbit coupling.

It must be pointed out that the device proposed by Datta-Das has severe practical limitations with regards to miniaturization, including susceptibility to Hall voltages induced by stray magnetic fields [9], conductivity mismatch between the contacts and semiconducting channel, and other fabrication complexities. This is because the proposed structure used FM electrodes for injection and detection of the spin polarized current through the device.
To overcome the limitations due to the FM electrodes, intense research is being pursued to control the creation, detection and manipulation of the spin-polarized current by purely electrical means [4, 17, 18, 19]. Spin-orbital coupling (SOC), which couples the spin of the electron with its orbital motion, has been considered as a possible mechanism by which all-electric spintronics could be realized. In addition to the tuning of the RSOC which arises due to the asymmetry in the lateral confining potential of a two-dimensional (2D) system [20, 21] discussed above, recent research has focused on control of lateral spin-orbit coupling which arises from an in-plane electric field resulting from the lateral confining potential of a quantum wire [22-24].

1.4 Why all-electric spintronics?

Research in semiconductor based spintronics has not kept up with the rapid progress in metallic spintronics which has been exceptionally rapid by historic standards, with revolutionary commercial devices available within ten years from the discovery of the GMR effect. Magnetic random access memory (MRAM), hard disk read/write heads based on this effect are testimony to the great success enjoyed by metallic spintronic devices [25]. However, as mentioned earlier, using FM contacts has inherent disadvantages. Because of the use of metal contacts and their bulky size, the memory unit cannot be directly integrated onto the logic unit.

The logic operations are currently performed with charge based devices. The presence or absence of charge is interpreted as logic level high and low respectively. For example, in case of a CMOS transistor the ‘ON’ state is defined by the channel being charged and thus conducting and the ‘OFF’ state is defined by the channel having no charge, and hence non-conducting. In other words, to switch the device from one state to another can be analogous to the process of moving charge from one well to another with the two wells being separated by a barrier - the barrier being
adjustable. It has been shown that the minimum switching energy, for an adiabatic system, to move from one state to another, as given by Landauer, is $E_{\text{bit}} = k_B T \ln 2 \sim 23 \text{ meV}$ [26]. It is estimated that the projected gate switching energy in 2018 for low power CMOS with a 10 nm gate width is 15 eV, i.e., three orders of magnitude larger than the theoretical minimum [27]. If spin based devices are used, none of the operations involving the change of logic level require raising or lowering of barriers and the task will simply be accomplished by applying an external or an effective magnetic field which will rotate the spin by 180°. It is thus expected that spin based devices will avoid the fundamental limit barrier that besieges the charge based devices. The RSOC based Datta-Das SpinFET was first such attempt towards realizing the spin analogue of the standard charge based MOS device. Other, albeit lesser known efforts have been made based of Dresselhaus Spin Orbital Coupling (DSOC), Spin Hall effect (SHE) and the one proposed by our group based on Lateral spin orbital coupling (LSOC) [28 - 35].

1.5 Mesoscopic Systems

Mesoscopic systems are those that have dimensions between atomic and macroscopic scale. These have dimensions are smaller than the de Broglie wavelength, the mean free path and the phase relaxation length. The devices fabricated in this thesis are all with dimensions that smaller than above mentioned lengths and hence qualify as mesoscopic systems. In this regime the wave nature of the electrons comes into prominence and hence as expected quantum effects dominate which are not observed in macroscopic devices. The relatively long mean free path implies that the electrons can pass through the entire length of the conductor without scattering, i.e., ballistically. The phase relaxation length is generally longer than the mean free path since when a particle loses its energy it also loses its momentum.
We know that the number of electrons is related to the Fermi wavenumber, \( k_F \), by

\[
n = \frac{k_F}{2\pi}
\]  

(1.7)

And the Fermi wavelength and velocity are given by

\[
v_F = \frac{\hbar}{m^*} \sqrt{2\pi n}
\]

(1.8)

\[
\lambda_F = \frac{2\pi}{\sqrt{n}}
\]

(1.9)

For our InAs sample, \( n_{2D} = 1.2 \times 10^{12}/\text{cm}^2 \) and the mobility \( \mu = 10^5 \text{ cm}^2/\text{V-s} \) [31] and the effective mass in case of InAs is \( m^* = 0.023m_e \), and \( m_e \) is free electron mass, \( 9.1 \times 10^{-31} \text{ kg} \).

Therefore from Eq. (1.8), \( v_F = 13821.013 \text{ cm/s} \). The mean free path is given by

\[
l = v_F \frac{m\mu}{e}
\]

(1.10)

From Eq. (1.10), in InAs based devices, \( l = 1.8 \mu \text{m} \) which is larger than the channel length (typically around 900nm to 1 \( \mu \text{m} \)) of the quantum point contact (QPC) devices to be used in this thesis to implement an all-electric spin polarizer. Hence, our devices satisfy the conditions that qualify them for being treated as mesoscopic systems.

### 1.6 Quantized Conductance in Quantum Point Contacts (QPCs)

In mesoscopic systems, quantum mechanical effects dominate and it becomes increasingly difficult to answer simple questions like what represents a resistance using classical theory. A QPC is the simplest mesoscopic device that directly shows quantum mechanical properties. It consists of a very short quantum wire or constriction. It is usually made by depositing a pair of surface gates (Schottky or metal) over a two dimensional electron gas (2DEG) like the one that exists at the interface of a semiconductor heterostructure (Fig. 1.4). Over the years there
have been many reports on the fabrication and characterization of top gated QPCs (shown in Fig. 1.5(b)) and side gated QPCs (which we will discuss further in chapter 2).

In 1988, two groups, one led by D.A. Wharam at Cambridge [37] and another led by B.J. van Wees at Delft [38] were the first to experimentally measure the conductance of a QPC in the ballistic regime of operation. They used a 2DEG at a heterointerface of an GaAs/AlGaAs heterostructure as shown in Fig. 1.4.

Figures 1.5(a) and 1.5(b) show a schematic illustration of a top gated QPC. A negative bias on the two gates repels the electrons in the 2DEG under the gate area creating a short conduction channel or a constriction. The width of the channel so formed can be controlled by application of suitable biasing voltage on the gates.

Despite being referred to as "point" contact, fabricated QPCs have a finite length ranging from a few ~ 100 nm to a few microns. As indicated in Fig 1.5(c), the band structure of 1D system consists of a number of 1D sub-bands with energy $E_1, E_2, E_3, \ldots$ (if the confinement is approximated by a particle in a box). The energies of the subband bottoms are given by

$$E_n = \left( \frac{\pi^2 \hbar^2}{2m} \right) \frac{n^2}{w^2} \quad \text{with} \quad n = 1,2,3, \ldots$$

Referring to Fig. 1.5(c), $E_F$ is the Fermi level and $k$ is the vector describing the propagation along the QPC channel. Only the energy levels that are below the Fermi energy level contribute to conduction. At 0 °K, the conduction of such a system is given by the Landauer formula

$$G = \frac{2e^2}{h} \sum_{n,m=1}^{N} |t_{mn}|^2$$

(1.12)
Fig 1.4: Formation of a two-dimensional electron gas (2DEG) of an AlGaAs/GaAs hetero-interface. Z is the direction of growth of the heterostructure.

Fig 1.5: Schematic illustrations of (a) QPC constriction created by two surface gates (upper gate - UG and lower gate - LG) deposited on the surface of a semiconductor heterojunction (b) AlGaAs/GaAs heterostructure with 2DEG at the interface depleted by surface Schottky gates to create a one dimensional electron gas (1DEG) system. (c) Energy subbands in a 1DEG as a result of quantum confinement produced by the top surface gates.
where $N$ represents the number of subbands below the Fermi level, i.e., the number of transverse modes available for conduction and $|t_{mn}|^2$ are the transmission coefficients between the subbands along the QPC channel. However, if the mean free length is longer than the length of the QPC channel, ballistic transport prevails, there is transmission between subbands and $|t_{nn}|^2 = 1$, for all subbands below the Fermi level. As a result, in the case of ballistic transport, the conductance through the QPC is given by

$$G = \frac{2e^2}{h} N = G_0 N$$

(1.13)

where $N$ is the largest integer for which $E_n$ is below $E_F$.

Therefore, at very low temperature, the QPC conductance is predicted to be quantized in multiples of a fundamental unit of conductance, $G_0 = 2e^2/h$, equal to $7.748 \times 10^{-5}$ S.

Figure 1.6 shows the QPC conduction as a function of gate voltage as was first reported by B. J. Wan Vees et al [38]. In order to observe the steps in conductance, measurements were performed at sufficiently low temperature so that the thermal energy $k_B T$ is smaller than the energy separation between the subbands. Figure 1.6 shows that change of about 0.1V is needed on the top gates to progressively align the energy subbands in the narrow portion of the QPC with the Fermi level in the contacts. Typical energy separation between subbands is just a few meV and the much larger change in potential needed on the gate to shift the energy levels is due to the separation of the 2DEG (several nm) from the top surface.
Fig 1.6: Experimental observation of conduction quantization in a split gated QPC as a function of voltage applied to the top gates [38].

The factor of 2 on the right hand side of Eq. (1.13) is to account for the spin degeneracy of the subbands. The spin degeneracy can be lifted by application of magnetic field. In this case, the conductance is predicted to be quantized at integral values of 0.5\(G_0\) and can only be observed with sufficiently high magnetic fields and low temperatures. The occurrence of 0.5\(G_0\) plateau in the conductance of a QPC is therefore an indirect evidence of complete spin polarization in the channel. Figure 1.7 shows the spin splitting and hence the lifting of spin degeneracy by application of an external magnetic field. These results were obtained for AlGaAs/GaAs QPC device fabricated by a former student in our group [31]. The spin splitting energy in presence of a magnetic field \(B\) is given by

\[
\Delta E = g\mu_B B 
\]  
(1.14)
where $g$ is the gyromagnetic or Lande ratio and $\mu_B$ is the Bohr magneton.

The splitting of an energy level in presence of a magnetic field is known as **Zeeman Effect**. The splitting energy is proportional to the strength of the magnetic field. Figure 1.7 shows the schematic representation of the spin splitting of an energy level due to Zeeman Effect.

![Zeeman spin splitting](image)

Fig. 1.7: Illustration of Zeeman spin splitting in presence of an external magnetic field of intensity $B$; $g$ is the gyromagnetic factor of the semiconductor and $\mu_B$ is the Bohr magneton.
1.7 Spin Orbital Coupling (SOC)

A successful implementation of an all-electric SpinFET requires means for creating, manipulating and detecting spin polarized currents. The electric control of Spin Orbital Coupling (SOC) in semiconductors is a possible mechanism for achieving these goals.

The Hamiltonian for spin-orbit coupling is given by [31]

\[ H_{so} = \lambda \vec{\sigma} \cdot (\vec{k} \times \vec{V}) \] (1.15)

where, \( \lambda = \frac{\hbar^2}{4m_o c^2} = 3.7 \times 10^{-6} \text{ A}^2 \) is called the spin orbital coupling parameter (here, \( m_o \) is the free electron mass and \( c \) is the speed of light in vacuum). \( \vec{\sigma} = (\sigma_x, \sigma_y, \sigma_z) \) represents the Pauli spin matrices, \( \vec{k} = \frac{\vec{p}}{\hbar} \) and \( \vec{V} \) is the electrostatic potential.

Fig. 1.8: Zeeman spin splitting of the first quantized plateau in presence of an external magnetic field \( B \). The appearance of the 0.5\( G_0 \) conductance plateau indicates that the spin degeneracy is lifted. [31]
In the original formalism (for an electron in an atom) the energy gap (the Dirac gap) between an electron’s positive and negative energy plays a role in determining the magnitude of the SOC; it has to be relatively small for SOC to be large. In the case of semiconductors, the Dirac gap is replaced by the bandgap of the semiconductor. This is on the order of 1 eV or less in III-V semiconductors. In InAs-based materials, where both the band gap and the electron effective mass are small (~ 0.36 eV and 0.023\(m_0\), respectively) there can be very large spin-orbit coupling. This is why InAs-based quantum wells are thought to have interesting spin-dependent properties and explains why we have selected InAs as a material of choice in our experiments.

There are three types of SOC that are prominent in QPC systems: Rashba, Dresselhaus and Lateral SOC. We briefly describe each mechanisms in the next sections.

### 1.7.1 Rashba SOC

This spin-orbit interaction is the basis of the Datta-Das spin based transistor discussed in section 1.3. In this section, we analyze in more detail its influence on spin transport through the structure shown in Fig. 1.3. From Eq. (1.15), we see that the SOC Hamiltonian \(H_{so}\) depends on the gradient of the electrostatic potential \(V\). This potential could be internal, for example due to presence of impurities or defects, or it could be due to an externally applied potential. One possible potential arises due to the structural inversion asymmetry (SIA) in the confining potential of the 2DEG which produces an electric field that is perpendicular to the plane of the 2DEG, i.e., in the direction of growth of the heterostructure. This was first studied by E. I. Rashba in 1960 in an asymmetrically grown QW structure with an asymmetry in the barrier height of the two sides of the well, causing a gradient in the potential [20, 21]. The electrons moving in the well see this
electric field as an effective magnetic field that lies in the plane of the 2DEG, perpendicular to the electric field. The interaction of this effective magnetic field with the electron motion results in SOC. This effective magnetic field is responsible for spin splitting and lifting of the spin degeneracy. This SOC is referred to as Rashba Spin Orbit Coupling (RSOC).

The effective Hamiltonian describing RSOC in a 2 DEG is given by [20],

$$H_{Rashba} = \alpha (\vec{k} \times \hat{z}) \cdot \vec{\sigma}$$  \hspace{1cm} (1.16)

Leading to an energy dispersion relations of the spin split subbands in the well given by

$$E(k) = \frac{\hbar^2}{2m^*} k^2 \pm \alpha k$$  \hspace{1cm} (1.17)

where, $\alpha$ is a constant defined by $\alpha = \alpha^* |e|E$, and $\alpha^*$ is the Rashba SOC parameter, which is proportional to the strength of the electric field [20]. The value of $\alpha$ can be tuned externally by applying a gate voltage. The Rashba electric field points in the direction of growth of the asymmetric heterostructure. The energy dispersion curve for spin-up and spin-down electrons in case of RSOC is shown in Fig 1.9. Electrons with opposite spins travel with different Fermi velocities because of the difference in their $k$ vector at the Fermi level. The two different wave vectors correspond to two electron gases, i.e., one for up spin electron gas and one for down spin electron gas, with slightly different carrier concentrations and can be seen in the beating pattern of the Shubnikov-de Hass (SdH) oscillations [33, 34]. The RSOC can be tailored by introducing either internal (asymmetric confinement of the 2DEG in a heterostructure) or external electric fields.
Unlike Zeeman splitting, Rashba spin splitting does not result in a net magnetization of the 2DEG system as its Hamiltonian ($H_{\text{Rashba}}$) has time-reversal invariance and therefore no common spin quantization axis is available for its spin eigenstates.

Numerous efforts have been made to manipulate the electron spin in 2DEG systems by controlling the RSOC [15, 16]. A successful experimental demonstration would pave the way for realization of the Datta-Das Spin-FET [16]. To date, there has been only one reported implementation of the Datta-Das SpinFET, a claim that was recently challenged [39].

![Energy dispersion relations](image)

Fig. 1.9: Energy dispersion relations in a 1D semiconducting channel as a result of RSOC as used in Datta-Das in their proposal of the first SpinFET [15].

### 1.7.2 Dresselhaus SOC

Time and space inversion symmetry lead to the following properties for the energy dispersion relationships in semiconductors such as Si or Ge:
Time inversion symmetry: \[ E_\uparrow (k) = E_\downarrow (-k), \]  

Space inversion symmetry: \[ E_\uparrow (k) = E_\uparrow (-k) \]  

where, \( k \) is the wavevector and \( \uparrow \) and \( \downarrow \) denote the spin-up and spin-down electron states.

Combining both time and space inversion symmetry leads to the following spin degeneracy of the energy dispersion relations, i.e.,

\[ E_\uparrow (k) = E_\downarrow (k) \]  

The above relation is valid in semiconductors such as Si and Ge. In semiconductors like InAs, GaAs which lack an inversion center and the spin degeneracy is lifted for a non-zero \( k \), i.e,

\[ E_\uparrow (k) \neq E_\downarrow (k). \]  

The DSOC Hamiltonian is given by

\[ H_{DSOC} = \beta (k_x \sigma_x, -k_x \sigma_x) \]  

It can be shown that the parameter \( \beta \) is inversely proportional to the width of the quantum well. DSOC has been experimentally observed in InSb and GaAs (110) [40, 41]. The DSOC is a strong function of the crystallographic direction and can be minimized along specific directions. The optimal directions for GaAs and InAs have been shown to be [1 2 0] and [1 0 0], respectively [33].

III-V semiconductors have a zinc-blende crystal structure and lack inversion symmetry. The SOC due to bulk inversion asymmetry (BIA) is referred to as Dresselhaus Spin Orbit Coupling (DSOC) as it was first studied by Dresselhaus in 1955 [30].
1.7.3 Lateral Spin-Orbit Coupling

Recently, Lateral Spin Orbit Coupling (LSOC), associated with transport in quantum wires, was theoretically predicted by three groups – K. Hattori et al., Y. Xing et al. and Y. Jiang et al. [22-24]. LSOC can occur in a 1D quantum wire where the current flows along the wire (used as positive $x$-direction) and the electrons are confined in the direction perpendicular to the current flow ($y$-direction hereafter). A 1D quantum wire can be realized by applying a confining potential $V$ along the $y$-axis to a 2DEG system lying in the $xy$-plane as shown in Fig. 1.10(a). The potential is nearly constant in the central part of the wire, but rises steeply near the edges as shown in Fig 1.10(b). This leads to a transverse electric field, $E = -\nabla V$, perpendicular to the direction of current flow and pointing towards the edges. The moving electrons will respond to this electric field as if there was an effective magnetic field pointing along the $z$-direction. This effective magnetic field ($B_{SO}$) will lead to spin-orbit coupling. Since the origin of this SOC is the lateral electric field that is near the edges of the wire, it is referred to as LSOC and is clearly different from the RSOC originating from an electric field due to the asymmetric confinement of a quantum well structure, as discussed earlier.

The LSOC Hamiltonian is given by [21]

$$H_{SO} = -\frac{\hbar^2}{2m^*c^2}\sigma_z k \frac{d}{dy} U(y)$$

(1.23)

where $U(y)$ is the lateral confining potential in the QPC channel

For electrons moving in the $+k_x$ direction in the 1D channel, Eq. (1.23) shows that the effective potential is lower for the spin-down electrons ($\sigma_z = -1$) than for the spin-up electrons ($\sigma_z = +1$) and the opposite is true on the other side of the channel. This causes a spin imbalance and results in accumulations of opposite spins on the two edges of the wire [22-24]. For electrons
travelling in \(-k_x\) direction the sign of spin accumulation is reversed. With a small bias applied along the direction of the current and at a sufficiently low temperature, the contribution from electrons travelling from right to left can be neglected. As a result, a lateral confining potential can cause opposite spin accumulation along the two sides of the 1D quantum wire. However, because of the symmetry of the effective field on both sides of the wire, there is no net spin polarization and resulting spin-polarized current in these 1D systems [22-24]. To investigate the possibility of a net spin polarization in 1D quantum wires, one must first assess the sources of spin dephasing, i.e., the sources of spin decoherence in such systems.

Fig 1.10: (a) Schematic of a 1D quantum wire, the direction of current flow is indicated by the arrow. (b) The confining potential along the y-direction which is perpendicular to the motion of the electrons (along x-direction). In presence of LSOC, this leads to the accumulation of electrons with opposite spin along the edges of the wire. [31]
1.8 Spin Relaxation Mechanisms in 1D systems

Spin relaxation and spin dephasing are processes that lead to the loss of spin polarization of the injected spin current and are thus of great importance for spin based devices. What makes spin a viable option for encoding information is the fact that non-equilibrium electronic spin in metals and semiconductors has a relative long relaxation time (typically a few nanoseconds). For optimal device design, it is important to look into the spin relaxation and dephasing mechanisms.

There are four mechanisms for spin relaxation that are relevant for metals and semiconductors: the Elliott-Yafet, D’yakonov-Perel’, Bir-Aronov-Pikus, and the hyperfine-interaction mechanisms [42-45]. For III-V devices, the first two are dominant. Bir-Aronov-Pikus (BAP) mechanism occurs in hole (p-doped) systems and arises because of the local magnetic field created by the electron-hole exchange interaction – since we will be using n-doped heterostructures, we will not discuss BAP mechanism here. Hyperfine interaction is of importance in systems with atoms having large nuclear moments and can be neglected in III-V semiconductors. In III-V semiconductors with lack of inversion symmetry, the Elliott-Yafet (EY) mechanism leads to electron spins relaxation due to the mixture of the wavefunctions associated with opposite-spin states as a result of the spin-orbit coupling induced by momentum scattering from ions and phonons. The spin-orbit coupling by itself does not lead to spin relaxation. However, in combination with momentum scattering, the spin-up and spin-down states can couple and lead to spin relaxation. Scattering from ions is dominant at low temperatures and phonon scattering dominates at higher temperature [42]. The D’yakonov-Perel’ (DP) mechanism is another mechanism important in III-V semiconductors because this is responsible for spin dephasing in solids without a center of symmetry. The lack of symmetry in the lattice results in the electrons feeling an effective magnetic field, due to spin orbit interactions, as it moves through the lattice. Thus at every instance along the lattice, the electron's
spin changes in a random manner leading to spin decoherence. One of the main advantages of using a 1D system is the limitation on the available k space for propagation. Additionally, in a 1D system, the propagation vector k is essentially unidirectional which also means that the spin quantization axis is well defined. Both these contribute to the suppression of EY and DP spin dephasing mechanisms. Based on these results we opted to explore 1D system to achieve all electric control of the amount of spin polarization. Furthermore, to reduce the effects of both elastic and inelastic scattering the dimensions of the 1D wire in the direction of current should be smaller than the mean free path and the spin coherence length L. The devices reported all have dimensions smaller than above mentioned lengths and hence qualify as 1D system. In this regime the wave nature of the electrons comes into prominence and hence as expected quantum effects dominate which are not observed for macroscopic devices. A classic example of quantum mechanical effect is the quantization of the conductance in sufficiently small 1D quantum wires. The relatively long mean free path implies that the electrons can pass through the entire length of the conductor without scattering, i.e., ballistically, while the long phase relaxation length lets us assume that transport is coherent through the sample. As shown earlier, in the InAs based heterostructures to be used to fabricate our devices, \( l = 1.8 \mu m \) which is larger than the channel length of our QPC devices, which is typically around 900 nm to 1 \( \mu m \). Hence our devices satisfy the conditions that qualify them as 1D systems. A relatively short QPC, operating at a relatively low temperature and with a single subband participating in current flow, is therefore an ideal 1D system to explore for the generation of spin-polarized currents based on appropriate tuning of LSOC.
1.9 Thesis outline

Over the last six years, our group demonstrated experimentally that it is possible to have almost complete spin polarization in a QPC -- a short quantum wire between two large electron reservoirs -- in presence of LSOC and if the lateral confining potential is highly asymmetric [31,32,47-49]. It was the first experimental demonstration that a spin-polarized current can be achieved by purely electric means in a QPC in the presence of LSOC. Figure 1.11 shows an atomic force microscope image of single QPC devices with side gates G1 and G2, the arrow indicates the direction of electron flow.

Fig 1.11: An Atomic Force Microscope image of a QPC with two in-plane side gates designated as G1 and G2.

Figure 1.12(a) shows the first successful demonstration of spin polarization in a QPC using LSOC by Debray et al. [31] in the study which showed the appearance and evolution of a 0.5G0 conductance plateau in an In0.52Al0.48As/InAs QPC. However, the work of Dr. Das (a former Ph.D
student in our lab) led to the observation of other conductance anomalies (i.e., at values different from 0.5$G_0$ but below the first conductance plateau $G_0$) that depended strongly on the QPC dimensions (length and width) and the polarity of the offset bias between the two side gates. P. Das showed that the conductance anomalies are extremely sensitive to defects (surface roughness and impurity/dangling bond scattering) generated during the etching process that forms the QPC side walls [47, 48]. However, it was observed that the anomalous plateaus were quite robust and extended over a maximum range of nearly 1 V for the common sweep voltage applied to the two gates. Some of the experimental results of P. Das are summarized in Fig. 1.12(b). Fig 1.12(b) shows the linear conductance $G = I/V$ of the channel measured for different $(V_{G1} - V_{G2})$ values as a function of a common sweep voltage, $V_G$, using a four-probe AC technique with a drive frequency of 17 Hz and a drain-source drive voltage of 100 μV at 4.2 K.

In order to be able to realize a practical working spin based device, it is important to address the important technological challenge of controlling the location of the conductance anomalies in QPCs. To achieve this goal, a new QPC structure is investigated in this thesis with two pairs of in-plane SGs to create a **tunable all-electric spin polarizer**. The schematic of the proposed device is shown in Fig. 1.13. This work, shows that the first pair of SGs near the source can be asymmetrically biased to create spin polarization in the QPC channel. The second set of gates, near the drain, can then be symmetrically biased to maximize the amount of spin polarization in the channel. Several InAs based QPC devices of this type with four SGs have been fabricated and found to have conductance characteristics in qualitative agreement with predictions based on a Non-Equilibrium Green’s Function (NEGF) approach developed by a former Ph.D., Dr. Junjun Wan [35]. The main finding, as reported in this thesis, is that the range of common mode sweep voltage applied on the first set of gates over which maximum spin polarization can be achieved is
much broader for the four gate structure proposed in this thesis compared with the case of a single pair of in-plane SGs.

![Graph](image1)

![Graph](image2)

Fig 1.12: (a) Linear conductance in units of $G_0$ $(2e^2/h)$ of a QPC measured at both gate symmetric (S) and asymmetric (AS) bias condition. The plot for AS shows a conductance plateau near $0.5G_0$. The bias asymmetry between the two side gates is 7.5V. The sweep voltage is superimposed on the potentials $V_{G1}$ and $V_{G2}$ applied to the gates to create the asymmetry. $V_G$ is the common sweep voltage applied simultaneously to both side gates (the plots were smoothened using 5 point averaging method) [31] (b) Plot of conductance of another QPC (in units of $2e^2/h$) as a function of the common sweep voltage $V_G$. The potential applied to gate $G_2$ is fixed at -1.0V. The leftmost curve corresponds to the actual conductance data for the symmetric case, i.e., with only the common sweep voltage $V_G$ applied to the two gates. The other plots have been shifted to the right for clarity. From left to right, the potentials on gate G1 are equal to 0, 0.4, 0.8, 1.2, 1.6, 2.0, 2.4, 2.8, 3.2, 3.6, 4.0, 4.4, 4.8 and 5.2V, respectively [48]. In Fig.1.12 (b) the conductance anomaly is below $0.5G_0$. 
In addition, we have observed both *hysteresis* and *negative differential regions* in the conductance of the device for specific biasing conditions which could not be explained using the Non Equilibrium Green Function (NEGF) approach. In this case, we have developed a simple many-body approach to carrier transport through the four gate QPC device based on the onset of Coulomb and Spin blockade regime of operation.

![Schematic of proposed four-gate QPC device](image)

**Fig 1.13:** Schematic of proposed four-gate QPC device to achieve better control of spin polarization. S and D denotes the source and the drain contacts, respectively. In this thesis, we study the conductance of this QPC as a function of the potential on the left (G₁, G₂) and right (G₃, G₄) pairs of in-plane SGs.

The outline of this thesis is as follows:

(a) Chapter 2 discusses in more details the conditions necessary for the onset of spin polarization in asymmetrically biased QPCs in the presence of LSOC based on NEGF simulations of the conductance through the device. Some of the previous experimental results by P. Das on the observation of conductance anomalies in QPC devices are analyzed. Further, the incentive and
principle of operation of the proposed four gate QPC device shown in Fig. 1.13 as an all-electric spin polarizer is detailed.

(b) Chapter 3 describes the device fabrication sequence of the four gate QPC devices and gives an overview of our conductance measurement setup.

(c) Chapter 4 present NEGF simulations of the four gate QC device illustrating the tunability of the $0.5G_0$ conductance plateau for various biasing conditions applied to the two pairs of SGs. Next, conductance measurements in qualitative agreement with our NEGF results when the right portion of the QPC device is not operated too close to its threshold for conduction are presented. When the device is close to its threshold, hysteresis and the equidistant peaks in the conductance curves are observed which are attributed to the onset of Coulomb/Spin blockade regime of operation of the device for which a simple model of the four gate QPC in qualitative agreement with the experimental results is presented.

(d) Chapter 5 proposes extension of our work towards the realization of an all-electric spin valve, i.e., the first realization of an all-electric SpinFET along the lines of the spin transistor envisioned by Datta and Das [15].
Chapter 2

Background

2.1 Review of Previous Work

In chapter 1, we gave a brief perspective of the field of spintronics. We discussed the Datta-Das SpinFET which was proposed based on a gate voltage control of the RSOC to control the spin precession in the channel. We also discussed other SOC mechanisms with special emphasis on LSOC that we have exploited to achieve spin polarization in our QPC devices.

In this chapter we give a brief overview of the extensive work on InAs single QPC devices performed by previous students in our group and which forms the basis of our work [31, 33, 34]. In the past, our group has extensively studied the appearance and evolution of the 0.5 conductance plateau and other conductance anomalies in QPC with LSOC and demonstrated the influence of dangling bonds and surface roughness scattering on their appearance and location [34, 48, 49]. Here, we will qualitatively explain the significance of the half integer plateaus and how we intend to exploit the spontaneous spin polarization previously observed in the QPCs to realize the all-electric spin polarizer described at the end of the previous chapter.

2.2 Spin Polarization Due to LSOC

In chapter 1, we gave an overview of LSOC and how it lifts the spin degeneracy. Here, we will take a closer look at it with respect to our QPC devices. Figure 2.1(a) shows a scanning electron
micrograph of a QPC device with two in-plane SGs, these are indicated as upper gate (UG) and lower gate (LG). The gradient of the lateral confining potential, \( U(y) \), along the side walls of the QPC result in a transverse in-plane electric field \( E \). Figure 2.1(b) shows the profile of the confining potential, which drops rapidly as we move away from the walls of the QPC. Figure 2.2 (a) shows the direction of the electric field experienced by an electron moving perpendicularly out of the plane of the page. Due to LSOC, an electron moving with wave vector \( \mathbf{k} \) sees this as an effective magnetic field.

The effective magnetic field \( \mathbf{B}_{\text{so}} \) is given by

\[
\mathbf{B}_{\text{so}} = \beta (\mathbf{k}_x \times \nabla U(y))
\]

(2.1)

where \( \beta \) is the intrinsic SOC parameter of the channel material. For the case of InAs, \( \beta \) is 5 Å\(^2\) [31].

LSOC is clearly different from Rashba SOC, which arises from the electric field due to the asymmetry in the confining potential of a quantum well (QW) structure and is along the direction of growth of the heterostructure. The electric field responsible for inducing RSOC is perpendicular to the 2DEG plane (or device plane), whereas the electric field responsible for LSOC lies in the plane of the 2DEG.

Recent theoretical work reported that LSOC can induce an accumulation of opposite spins on the edges of a quantum wire [22-24]. But, none predicted a net spin polarization that might generate a spin-polarized current. Figure 2.2(a) and (b) illustrate the two cases where symmetric and asymmetric potential applied across the gates UG and LG cause spin polarization in the channel. When the potential along the side walls is symmetric (Fig 2.2(a)), though the electrons experience an effective magnetic field, \( \mathbf{B}_{\text{so}} \), the latter is of equal magnitude on the sidewalls and
merely causes opposite spin accumulation along the side walls of the QPC [22-24]. Thus though we can obtain local spin polarization this way, the net polarization in the channel is zero (Fig. 2.2(a)). However, if a small asymmetry $\Delta V_{sg}$ is applied across the gates $UG$ and $LG$, the potential profile in the channel region changes to that shown in Fig. 2.2(b). The electrons now experience a slightly different $B_{so}$ depending on their spin state which in turn creates a small imbalance in the net spin of electrons in the channel. As was shown previously by Junjun Wan, this initial imbalance is enhanced due to the repulsive e-e interaction in the channel region [32, 35]. As a result of the strong electron-electron interaction, Junjun Wan has shown that the up spin electrons experience an energy barrier that is proportional to the population of spin down electrons in the channel and vice versa. This feedback mechanism when calculated self-consistently through a solution of Poisson equation to include space-charge effects leads to a large spin imbalance in the device [22-24, 35].

Our group has previously modeled a QPC using a NEGF approach to carrier transport [32]. This technique is summarized in appendix A. NEGF simulations have indicated that three conditions are essential to obtain spin polarization in QPC with in-plane SG: (a) an asymmetric lateral confinement, (b) LSOC induced by the lateral confining potential of the QPC and, (c) a strong electron-electron interaction. When the confinement is made asymmetric ($V_{UG} - V_{LG} \neq 0 V$) by tuning the SG voltages $V_{UG}$ and $V_{LG}$ (Fig. 2.7(b)), either the up spin electrons on the left edge dominates the down spin electrons on the right edge or vice-versa resulting in a spin imbalance and a net polarization. The spin polarization is responsible for a conductance plateau near $0.5G_o$ as shown in Fig. 2.3, referred to hereafter as the $0.5G_o$ plateau or the $0.5$ conductance anomaly.
2.3 Influence of Surface Scattering

For more than a decade, there have been many experimental reports of anomalies in the quantized conductance of quantum point contacts (QPCs). These anomalies appear at non-integer multiples of $G_0 = (2e^2/h)$, and include the observation of anomalous conductance plateaus that range from $0.4G_0$ and $0.7G_0$ [31, 50-59]. Even though the occurrence of these anomalies is still a highly debated issue, the emerging consensus is that the conductance anomalies are evidence of the onset of spin polarization in the channel of the QPC [31, 50-59], the detailed physics of which are unsettled.
Fig. 2.2: (a) Schematic representation of the transverse confining potential profile of a side-gated QPC. I and II represent the two edges of the QPC channel. $B_{SO}$ is the effective magnetic field induced by LSOC. Blue (dashed) and yellow curves correspond to the symmetric and asymmetric bias between the two SGs, respectively [32].

Fig 2.3: Linear conductance in units of $2e^2/h$ of a QPC measured for both symmetric (S) and asymmetric (AS) bias between the two SGs. The plot for AS shows the 0.5 plateau. Here, $V_G$ is common sweep voltage applied simultaneously to both SGs [31].
Experimental as well as theoretical models have shown that the number and location of the conductance anomalies can be further tuned by deliberately introducing a broken symmetry in the electrostatic confinement in the narrow portion of the QPC [60, 61]. Recently, it was reported that in presence of an asymmetric lateral confinement potential due to the bias applied between the two split gates, the impurity potential in a QPC changes drastically and this has been shown to strongly affect the location of the conductance anomalies [62].

In our group, Debray et al. reported for the first time that the lateral spin orbit coupling (LSOC), resulting from the lateral in-plane electric field of the confining potential of a QPC with in-plane SGs, can be used to create a strongly spin-polarized current by purely electrical means in the absence of any applied magnetic field [31].

P. Das, a former group member, has studied the appearance and evolution of several anomalous (i.e., $G < 2e^2/h$) conductance plateaus in an In$_{0.52}$Al$_{0.48}$As/InAs QPC. The number and location of the anomalous conductance plateaus strongly depend on the polarity of the offset bias. The anomalous plateaus were found to appear only over an intermediate range of offset bias of several volts. They are quite robust, being observed over a maximum range of nearly 1 V for the common sweep voltage applied to the two gates. These results were interpreted as evidence for the sensitivity of the QPC spin polarization to defects (surface roughness and impurity (dangling bond) scattering) generated during the etching process that forms the QPC side walls. Thus, the location and the strength of the 0.5 structure varies depending on the location as well as the strength of the defects, traps or surface states that may be inherently present in the heterostructure or may be introduced during the fabrication process [34]. Conductance measurements showed evidence of
surface scattering, due to surface roughness and dangling bonds on the side walls of the narrow portion of the QPC.

Further, this observation was supported by applying a magnetic field perpendicular to the QPC plane [47]. The NEGF simulations performed on a simple model of a QPC channel with dangling bonds (modeled as impurities – see Appendix-1 for details) in the channel, as shown in Fig. 2.4, produce conductance anomalies which were found to be in qualitative agreement with experiments reproducing conductance anomalies at values different from $0.5G_0$, as shown in Fig. 2.5 [63]. The NEGF analysis further showed that the QPC spin conductance polarization can still be fairly large even in the presence of such impurities [63].

Fig 2.4: Schematic of the QPC configuration used in the NEGF simulations. The width and length of the narrow portion of the QPC is equal to $w_2$ and $l_2$, respectively. In the simulations, the dimensions used were $w_2$, $l_2$, $w_1$, $l_1 = 16$, 32, 48, and 64 nm, respectively. The impurity locations 1, 2, 3 correspond to the coordinates $y_1 = w_1/2$ and $x_1 = 16$, 24, 32, respectively [63].
Figure 2.6 shows the three dimensional AFM image of the QPC that was used to study the effect of scattering centers on the location of the 0.5\(G_0\) structure. As can be seen in the figure, the side walls of the QPC are rather ragged (especially in the region around the constriction), a result of the wet-etching process used to define the trenches. One of the main challenges of the wet etching process is avoiding surface states and roughness in the channel side walls which can cause carrier depletion and degradation of carrier mobility [64-66]. Therefore, surface scattering is, in part, due to the roughness of the side walls which causes variations in the potential profile in the narrow portion of the QPC.

![Graph showing conductance as a function of V_sweep](image)

Fig. 2.5: Conductance as a function of \(V_{\text{sweep}}\) for a QPC containing an impurity (either attractive (positive) or repulsive (negative)) at location 3 in Fig.2.4. Also shown for comparison are the results with no impurity (0 meV) in the channel [63]
Fig. 2.6: A three-dimensional AFM image of a QPC with two in-plane gates (G1 and G2), fabricated using a chemical wet etching technique. The current flows in the x-direction. An asymmetric LSOC is generated using an asymmetric bias between the two SGs generating an electric field in the y-direction. As seen in the figure, the side walls of the QPC are rather ragged, most likely due to the wet etching process used to define the trenches. Surface scattering from this roughness plays a critical role in the observation of the anomalous conductance plateau ($G < 2e^2/h$) [34].

Additional surface scattering may be expected due to the presence of dangling bonds on the QPC walls. In QPC experiments, the charge state of dangling bonds as well as any other impurity is often affected during sample handling and may be affected by processes such as temperature cycling. This typically leads to markedly different conductance traces for identical biasing conditions. We observed this in the conductance of our InAs-based QPCs when the sample was brought to room temperature between low temperature measurements (at 4.2 K). Thermal cycling is expected to change the charge state of dangling bonds formed on the side walls of the QPC during etching [34].
Results from temperature (4.2 K) conductance measurements made using an InAs QPC device are shown in Fig. 2.7. The in-plane SGs, G1 and G2, were defined using e-beam lithography and wet etching techniques. DC voltages \( V_{G1} \) and \( V_{G2} \), applied to gate G1 and G2, respectively, create an asymmetric potential profile in the narrowest part of the QPC. The asymmetry in the bias potential, \( \Delta V_G = V_{G1} - V_{G2} \) creates spin polarization in the channel, as described earlier. The linear conductance in the QPC channel, \( G = \frac{I}{V} \), was recorded as a function of a common sweep voltage, \( V_G \), applied to the two gates, in addition to the potentials \( V_{G1} \) and \( V_{G2} \), with the current flowing in the x-direction. For all values of \( \Delta V_G \), the gates were found to be non-leaking.

Figure 2.7 shows the conductance of the QPC as a function of the sweep voltage \( V_G \) for different asymmetric biases (\( \Delta V_G = V_{G1} - V_{G2} \)) between the SGs. The left-most curve shows the conductance for the symmetric case (\( V_{G1} = V_{G2} = 0 \text{V} \)), i.e., with only the common sweep voltage \( V_G \) applied to the gates. For the other curves, from left to right, the potential \( V_{G2} \) applied to gate G2 is fixed at -2.0V and the potential \( V_{G1} \) on gate G1 is varied from -0.1 to -6.5 V, the latter corresponding to a large asymmetry between the two gates. As can be seen from Fig. 2.7, an anomalous plateau, seen around 0.4\( G_0 \), only appears for an intermediate range of bias \( \Delta V_G \). Interestingly, it appears over a maximum sweep voltage (\( V_G \)) range of nearly 1 V.

The application of a negative potentials \( V_{G1} \) and \( V_{G2} \) on the two SGs tends to push the electrons away from the side walls and reduces the effects of surface roughness scattering. However, the latter cannot be completely avoided. Since surface roughness and dangling bonds have a significant effect on the conductance of the channel, thermal cycling will result in a large change to the conductance, which we observed. Furthermore, the application of an asymmetric offset bias affects the charge state of dangling bonds as their energy levels are pushed up or down with reference to the Fermi levels in the QPC contacts. This is illustrated in Fig.2.8. Since the
surface roughness and the number of dangling bonds is different on the two side walls, this will lead to some level of asymmetry in the electrostatic potential in the narrow portion of the QPC, which is reflected in the conductance measurements [34,48].

Fig. 2.7: The conductance of an InAs QPC (in units of $2e^2/h$) measured as a function of the common sweep voltage $V_G$ applied to the in-plane gates, at $T=4.2$ K [34, 48]. The sweep voltage $V_G$ is superimposed on initial potentials $V_{G1}$ and $V_{G2}$ applied to the gates to create an asymmetry. The left-most curve shows the actual conductance data for the symmetric case; i.e., with only the common sweep voltage $V_G$ applied to the gates. The other curves have been shifted to the right for clarity. Thus, from left to right, the initial potential $V_{G2}$ applied to gate G2 is fixed at -2.0V and the initial potential $V_{G1}$ on gate G1 is equal to 0.0, -0.1, -0.3, -0.6, -0.9, -1.2, -1.5, -1.8, -2.0, -2.3, -2.6, -2.9, -3.1, -3.4, -3.7, -4.0, -4.5, -5.0, -5.5 and -6.5 V, respectively.
Fig. 2.8: Illustration of the conduction band energy profile between the two SGs, along a line through the middle of the QPC and perpendicular to the direction of current flow. The numbers 1, 2, 3 represent dangling bonds on either side of the channel. $E_F$ is the Fermi level of the source contact. Figures (a) and (b) show the conduction profile for opposite polarities of the potential between the two SGs [48].

The results shown in Fig. 2.7 are in qualitative agreement with the NEGF simulations shown in Fig.2.5, i.e., the location of the conductance anomalies (i.e. observed below $G_0$) is dependent on the impurities/dangling bonds or surface imperfections (surface roughness scattering) that may be inherently present in the heterostructure or may be induced during the device fabrication steps. In order to realize practical working devices, ways must be found to control and manipulate the spin in a much more reliable way. The goal of this thesis is to show
that a QPC with two pairs of in-plane SGs can act as a tunable spin polarizer. The incentive for the proposed device is describe next.

2.4 QPC with two pairs of in-plane SGs.

As discussed in section 2.3, prior conductance measurements on a QPC with two in plane SGs offered valuable insights into the spin polarization mechanism of the QPC. However, as discussed in section 2.3, the spin polarization was found to be strongly influenced by the presence of impurities as well as dangling bonds. As a result, fine tuning of the 0.5 conductance plateau, which may be needed for realizing practical spintronic devices, is not possible using a QPC device with a pair of SGs that we have explored so far.

In order to obtain a better control over the spin polarization in the channel, the structure shown in Fig 2.9 (b) was proposed, i.e., a QPC with two pairs of in plane SGs. Figure 2.9 (a) shows the AFM image of one such device fabricated in our lab. NEGF simulations have outlined three conditions that were discussed in section 2.2 which are fundamental for the realization of complete spin polarization in a QPC. By using the new QPC design proposed here (Fig. 2.9(b)), by appropriately biasing the second set of SGs, we believe that we not only enhance the electron-electron interaction which will lead to a robust polarization plateau but we would also be able to use the second pair of SGs to tune this plateau. In this thesis, we have investigated thoroughly the conductance of structures similar to the one shown in Fig. 2.9.
Fig 2.9: (a) Atomic force micrograph of 4-gate QPC device. (b) Schematic of four-gate QPC device denoting the two sets of in-plane SGs. S and D denotes the source and the drain contacts, respectively. In the actual structure shown on the left, the separation x between the two sets of in-plane split gates is 200 nm, the width of the narrow portion of the QPC is 275 nm, and the length of both sets of split gates is 600 nm.

An asymmetric bias ($V_{G1} \neq V_{G2}$) was applied between the two gates nearest the source to create spin polarization in the channel. An additional common mode bias $V_{sweep}$ was added to both of these gates. The second set of gates, close to the drain, was biased at the same potential $V_{g3} = V_{g4}$ with no additional sweep voltage applied to these gates. The conductance was then measured versus $V_{sweep}$ for different values of $V_{g3} = V_{g4}$. The measurements were repeated with an asymmetric bias on the second set of SGs – which are nearer to the drain. The influence on the 0.5 structure due to the potential on the second set of gates was then recorded in order to realize a non-local control of spin polarization in a QPC. Chapter 4 describes the result of NEGF simulations of a QPC structure with two pairs of in-plane SGs (Fig. 2.9(b)). In chapter 4, the conductance measurements on four gate InAs QPC devices performed at $T = 4.2K$ for a wide variety of biasing
conditions on the SGs is also reported. But first, we describe in the next chapter the different processing steps needed to fabricate the proposal all-electric spin polarizer.
Chapter 3

Device Fabrication and Characterization

3.1 Introduction

The remarkable progress in science of microfabrication in the last 30 years has enabled the fabrication of very complex devices which has in turn enabled experimentally validating various quantum mechanical phenomena such as quantized conduction, spin Hall effect, etc., as well as to discover new quantum phenomena such as the fractional quantum spin Hall effect which was unexpectedly discovered in 1982. One of the most critical components required to observe these quantum mechanical effects is the availability of very high quality heterostructures. Molecular Beam Epitaxial (MBE) is a growth technique used to grow the heterostructure wafers used for device fabrication. Although the basic process of MBE, ultrahigh vacuum evaporation, had been in practice long before, it was not until the works of J.R. Arthur and A.Y. Cho, in the late 1960s at Bell Telephone Laboratories, that a fundamental understanding of the process as applied to compound semiconductor growth evolved [68]. The main advantage of MBE lies in the atomic level resolution it offers thereby enabling precise control of layer thicknesses. In our work, we have used a custom designed high mobility InAs/InGaAs-based symmetric heterostructure that was grown by Intelligent Epitaxy Technology, Inc. Since we want a long spin coherence length in our samples, it is important that these structures be defect free so as to minimize scattering due to defects, impurities, etc. In this chapter, we will take a look at MBE growth technique and then go into the details of each of the QPC device fabrication procedures starting from sample cleaning to
lithography, followed by etching, forming ohmic contact regions using metal anneal, characterizing the device using atomic force microscopy and finally packaging which includes scribing, gluing and bonding the device. In addition, we will also discuss the basic measurement techniques for QPC devices with four in-plane SGs.

3.2 Molecular Beam Epitaxy (MBE)

The word “epitaxy” comes from Greek and means an ordered arrangement. In semiconductor processing, it means an ordered arrangement of atoms on a substrate. MBE is an advanced ultra-high vacuum growth method (base pressure $10^{-13}$ bar) to make complex compound semiconductor heterostructures with great precision (< 0.01 nanometer) and purity (>99.99999%). These materials are layered one on top of the other to form high quality wafers which are widely used in semiconductor devices such as transistors, light emitting diodes and lasers. MBE is one of the most sophisticated techniques for epitaxial growth of several crystalline semiconductor layers on top of one another, with atomic layer precision.

MBE is done inside an ultrahigh vacuum chamber. Figure 3.1 shows the schematic representation of the important components of a MBE system. The solid source materials are placed in effusion cells, called Kundsen cells (shown in Fig. 3.2), which have a very small orifice at one of the end and the other end is used for refilling the material to be evaporated. This reduces the chances of contamination as well as the need to break the vacuum while loading material. The design of the Kundsen cell provides an angular distribution of atoms or molecules in a beam. The substrate is heated to the necessary temperature and, when needed, can be continuously rotated to improve the growth homogeneity. The heating of the substrate provides energy to the molecules in the epitaxial layer to rearrange themselves once they reach the substrate. However excessive
heating of the substrate may cause reduction in the sticking coefficient of the material which can lead to the reduction in growth rate above a certain temperature [68].

Fig. 3.1: A schematic diagram of a MBE system showing its different components [68].

The operation of MBE can be divided into two steps. In the first step the solid source materials, the constituent elements of the material to be grown, are placed in the evaporation cells. Each material is evaporated and directed toward the hot substrate. Particles within a beam do not react or collide with one another. To have such a molecular flow, the mean free path of the particles
has to be greater than the geometrical size of the chamber. An ultrahigh vacuum environment ensures the ballistic nature of the beam. The heated substrate is rotated to ensure a uniform deposition rate across it.

In the second step, the evaporated atoms from the different Kundsen cells are deposited to form the layers on the hot substrate. Prior to the start of the growth process, the substrate is cleaned, loaded through a load lock, and is appropriately placed so that an optimum flow of materials emanated from the Kundsen cells reach the surface. The as-deposited film profile depends on the deposition rate, substrate rotation, surface temperature, surface material, and crystallographic orientation. During deposition ultrahigh vacuum of $10^{-11}$ Torr is maintained in the chamber using a cryopump.

The deposited thin film profile can be accurately analyzed using in situ reflection high energy electron diffraction (RHEED) technique. The RHEED pattern generated can be observed on the screen. As growth begins, initially the intensity begins to reduce and then increases as as a
continuous monolayer is formed. The intensity of the RHEED pattern starts oscillating as successive layers are deposited. When a monolayer growth is completed the pattern returns to the initial intensity. Each peak represents the forming of a new monolayer. Since the degree of order is at a maximum once a new monolayer has been formed, the spots in the diffraction pattern have maximum intensity since the maximum number of diffraction centers of the new layer contribute to the diffracted beam. The overall intensity of the oscillations however drops as more layers are grown. This is because the electron beam is initially focused with respect to the original surface and it gets out of focus as more layers are grown [62].

3.3 InAs/InGaAs/InAlAs heterostructure

Figure 3.3 shows the heterostructure of the wafer use for QPC fabrication in this thesis. A 2DEG system formed using an InAs/InGaAs quantum well (QW) is selectively etched to fabricate a 1D channel. In this heterostructure, a thin layer of InAs, which has a low bandgap around 0.36 eV is sandwiched between two layers of InGaAs with a relatively large bandgap of about 0.76 eV, thus forming the QW structure. Figure 3.4 shows the band diagram of the heterostructure. The formation of a QW at the interface traps the electrons whose motion is now restricted along the growth direction (z), but they are free to move along the x and y direction. Since the electrons in the quantum well are free only to move in the x-y plane, such a system is called a two-dimensional electron gas, referred to as 2DEG hereafter. The symmetry of the layers that are adjacent to the 2DEG, along the growth direction, enables us to minimize the Rashba component of the spin orbit interaction. By ensuring the growth of the wafer along the [1 0 0] direction, we have also ensured that the Dresselhaus SOC is minimum.
The heterostructure is grown on an InP substrate which is semi-insulating. A 300nm $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ layer is deposited using MBE which forms the buffer layer and helps in lattice matching the supply layer. The supply layer is Si doped $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ which is about 7nm thick. The Si acts as an n-type dopant in InAlAs material system. Fig 3.3 shows the detailed layer structure. The QW consists of a few monolayers of InAs (3.5 nm). A 2 nm InAs cap layer is deposited to prevent oxidation of the aluminium in the underlying layers. The oxidation of underlying layer is found to induce defects and traps and is responsible for pinning the Fermi level.

Fig. 3.3: InAs/InGaAs heterostructure
In a quantum well shown above, the electrons are free to move in the x-y plane, therefore, the total energy of an electron in each subband is given by:

\[
E_n(k_x, k_y) = E_n + \frac{\hbar^2}{2m} (k_x^2 + k_y^2)
\]  

(3.1)

where, \(E_n\) is given by the Eq. (3.1) and \(k = (k_x^2 + k_y^2)^{1/2}\) is the wave-vector in the (x,y) plane. \(k_x, k_y\) and \(n\) are the three quantum numbers needed to label the states.

For the case of 1D potential well, the energy levels are given by
\[ E_n = \frac{\hbar^2 \pi^2}{2m^*l^2} n^2 \] (3.2)

Where \( n (=1, 2, 3, \ldots) \) is the quantum number associated with different energy levels, \( a \) is the width of the 1D potential well, \( m^* \) the effective mass of electron in the well. Figure 3.5 shows the discrete energy levels in the 1D quantum well.

![Quantized energy levels inside the potential well](image)

**Fig 3.5: Quantized energy levels inside the potential well**

### 3.4 Device Fabrication and Processing Steps

The important steps involved in fabricating a QPC device with four in-plane SGs are

1. Pre-process cleaning.
2. Defining the QPC using e-beam lithography
3. Photolithography to write the isolation trenches followed by defining the ohmic regions
4. Deposition of ohmics contacts, followed by metal lift-off.
5. Atomic force microscopy to check different features of the as-prepared four gate QPC device.

6. Annealing of ohmic contacts.

7. Scribing, gluing and bonding.

8. Conductance measurements.

Except for the Atomic Force Microscopy, scribing and bonding steps, all the other steps were done in the clean room available in the College of Engineering and Applied Sciences.

### 3.4.1 Pre-process cleaning

A 5 mm × 5 mm wafer chip is diced from a two-inch circular wafer using a wafer scribe. The first cleaning step is called solvent cleaning during which the chip is soaked in hot (~ 60°C) acetone, methanol and isopropanol (IPA) for about 10 minutes each. At the end of the solvent cleaning process, the chip is blow dried with dry N₂. Since a thin layer of organic solvents may still be present on the surface, these organics are ashed off the surface using reactive ion etching in oxygen plasma for 40 sec. Though this process burns off any organic solvent traces that may have been on the chip due to the solvent cleaning, the oxygen plasma treatment tends to causes surface oxidation which can be a problem when making electrical contact with the chip later and hence the pre-etched in 18% HCl for 5 minutes. The chip is then rinsed under running DI water for at least 2 mins. This rinsing under running DI water is very important since any remnant acid has been found to “pit” the surface. The chip is blow dried dry N₂ and heated on a hotplate at 185°C for 5 min. This heating step helps drive off any residual moisture that may be present on the surface. Next, an e-beam resist - poly methyl methacrylate (PMMA) is spun on the wafer at 5000 rpm for 60 sec which gives us a thickness of around 50 nm [70]. After spinning coating the PMMA,
the chip surface is examined under a high resolution optical microscope to make sure that the PMMA is uniformly coated and no residual dust particles are on the chip. The entire cleaning steps are done in the cleanroom environment.

![Graph: Spin speed versus film thickness curves for different Anisole contents](image)

**Fig 3.6:** The spin speed versus film thickness curves for different Anisole contents [70].

### 3.4.2 Defining the QPC using e-beam lithography

The dimensions of a typically QPC are around a few hundred nanometers and at such dimensions, precise control becomes difficult. One of the widely used tools for fabricating nanoscale devices is Electron Beam Lithography (EBL) which offers a resolution limit down to few tens of nanometers and is therefore a widely used tool in nanoscale research. It also allows in situ monitoring of the wafer surface using Scanning Electron Microscopy (SEM) control.
Recently, efforts are on to make viable switching devices with dimensions down to the molecular level. Figure 3.8 shows a photograph of the Raith 150 e-beam writer that we use in the Engineering Research Center Clean Room located at the University of Cincinnati. The Raith 150 system is kept in a gold room in class 10 cleanroom.

Fig. 3.7: Raith 150 e-beam lithography system available in UC Cleanroom [71]

Fig 3.8: Schematic of e-beam exposure system [72]
In a typical e-beam writer an electron beam, with a Gaussian energy distribution profile, scans over the resist coated sample and defines the desired pattern by using the high energy electron beam to break the bonds in the resist. The electron beam is generated from a tungsten filament with very high aspect ratio and accelerated with a high voltage that is typically defined by the user. We use 10kV accelerating voltage. Figure 3.8 shows the typical block diagram of EBL system. Several sets of electromagnetic lenses collimate the accelerated beam of electrons and the beam properties are checked by burning smallest dimension “dots” on the sample. The sharpness of these dots gives us a qualitative estimate of our focusing and alignment.

The electrons in the beam impinge onto the samples and are scattered back from the sample into the collector which is kept at a slightly positive potential to attract the electrons. These electrons typically are incident on a phosphor coated plate inside the collector where they give out energy in the form of light which can be further amplified using a photomultiplier set up. Two kinds of scattering phenomena are observed for electrons penetrating the resist layer – first, forward scattering - a small scattering angle and inelastic in nature which creates secondary electrons with a few eV of energy. Second, large angle scattering and elastic in nature. These electrons when coming back into the resist layer, produce more secondary electrons. In both processes the secondary electrons are responsible for breaking/weakening the polymer crosslink of PMMA.

The design of the desired pattern is made using built-in CAD tools in the Raith software. A number of fine adjustments need to be made before we write the pattern. There are two work stations, called Raith and Leo, interfaced to the Raith machine [71]. They are converted to machine readable data through a “GDSII” file. The Leo site is for viewing the SEM image of the sample under the electron gun. A joystick helps the user move the sample stage in the horizontal plane (x-
y plane). The working distance is controlled from the Leo site. The Raith 150 EBL provides an electron beam with accelerating voltages from 0-30 kV. A 10 kV beam is used throughout our work. After loading the sample and measuring the beam current in the faraday cup, a sharp spot is burned on the sample by adjusting the working distance. A 20 nm size sharp round spot indicates a reasonably well focused beam. Also, a set of UV-global coordinates are defined to locate a point on the sample surface.

Once good focusing is reached, one needs to fix a proper dose of electrons. Dose is a measure of amount of electrons hitting the resist surface per unit area per unit time. Typical doses are in the range of 5 nA/cm$^2$ for very fine structures to 250 μA/cm$^2$ for large area structures. We have chosen a dose of 65 μA/cm$^2$ for our e-beam lithography.

![Exposure Parameter Calculation](image)

**Fig 3.9:** Screen shot of exposure parameter calculation in the Raith software

The dose is calculated using the following relation

\[
Area \ Dose = \frac{Beam \ Current \ \ast \ Area \ Dwell \ Time}{(Area \ Step \ Size)^2}
\]
Figure 3.10: The CAD file used for all the QPC with four in-plane SGs that we have fabricated in this thesis.

Once the design is written on the resist coated chip, the chip is then developed in a developing solution consisting of 1:1 methyl iso-butyl ketone and Iso-propyl alcohol (IPA) for 65 secs. The chip is then post backed on a hot plate at a temperature of 115 °C for 5 mins and then cooled down for 10 mins. Next, wet chemical etching is used to etch the exposed area. The etchant comprises of 15 ml Acetic acid, 20 ml hydrogen peroxide and 125 ml water. The etchant must contain an oxidizing agent and be free from any metallic cations to avoid ionic contamination of the etched surface. This can result in unwanted surface leakage current in the device [73]. The etchant works by first oxidizing the surface and then dissolving the oxide, thereby removing some of the underlying atoms of the semiconductor. Hydrogen peroxide is an oxidizing agent; acetic acid dissolves the resulting oxide. Typical etching rates observed using this recipe are 2 nm/sec – 4 nm/sec. Since our 2DEG is located approximately 22 nm below the surface and we have to ensure that we have to go below this to effectively etch and isolate the 2DEG in the QPC constriction, we etch for 25 secs. Deionized water is used as an etch stop. After etching, the chip is soaked in
acetone for stripping the PMMA resist. Heating the acetone to about 50 °C is found to give a more effective strip. Once the resist is removed, the chip is rinsed in IPA and blow dried in Nitrogen. The chip is then ready for patterning the isolation trenches and ohmics using photolithography.

3.4.3 Photolithography

The word lithography comes from the Greek word "lithos", meaning stones, and "graphia", meaning to write. When taken together, it means writing on stones. In the case of semiconductor lithography, which is referred to as photolithography our stones are semiconductor wafers and our patterns are written with a photo sensitive polymer called a photoresist. In modern fabrication, in order to build the complex structures that make up a transistor and interconnects that connects these billions of transistors, photolithography and etch pattern transfer process is repeated at least 30 times or more to make one modern day processor. Each pattern being printed on the wafer is aligned to the previously formed patterns and slowly the conductors, insulators, and selectively doped regions are built up to form the final device. Thus, photolithography is a very important process in semiconductor device fabrication.

Substrate preparation is intended to improve the adhesion of the photoresist material to the substrate. A hot acetone strip process done at the end of the e-beam etch step ensures that the chip surface is clean. Substrate contamination can take the form of particulates or a film and can be either organic or inorganic. Particulates result in defects in the final resist pattern, whereas film contamination can cause poor adhesion and subsequent loss of line width control and hence the whole process is done in a clean room environment.

There are two types of photoresist: positive and negative. For positive resists, the resist, is exposed to UV light wherever the underlying material is to be removed. In these resists, exposure
to the UV light changes the chemical structure of the resist, typically by breaking long polymer bonds, so that it becomes more soluble in the developer. The exposed resist is then washed away by the developer solution, leaving windows of the bare underlying material. In other words, "whatever shows, goes." The mask, therefore, contains an exact copy of the pattern which is to remain on the wafer.

Negative resists behave in just the opposite manner. Exposure to the UV light causes the negative resist to become polymerized, i.e., crosslink, and therefore it is more difficult to dissolve. The negative resist remains on the surface wherever it is exposed, and the developer solution

Fig 3.11: Photolithography using positive (left) and negative (right) photoresist. [73]
removes only the unexposed portions. Masks used for negative photoresists, therefore, contain the inverse of the pattern to be transferred. Figure 3.11 shows the pattern differences generated from the use of positive and negative resist.

Negative resists were popular in the early history of integrated circuit patterning, however positive resists offer better control over small geometry. We use positive resist – Shipley 1818 – for our photolithography process.

The clean and dried chip is placed onto a spincoater and a positive resist – Shipley 1818 – is spin coated over the chip at 4000 rpm for 60 sec to obtain a 1.5 μm thick layer of resist. A thick layer of resist is preferred since it facilitates easier liftoff. Figure 3.12 gives the thickness vs. spin speed curve for different resists including S1818.

The spin coated chip is placed on a hot plate at 115°C for 60 sec to drive out any remaining solvents from the photoresist and to ensure good adhesion of the resist to the chip. The chip is then ready for patterning by exposure to UV light through the photomask. A Karl Suss MJB3 Mask Alighner system which uses mercury arc lamp with a UV light of 365 nm wavelength is used for photolithography. We use soft contact lithography which gives us a resolution of 1.0 – 2.0 μm. The chip is exposed to UV light for 11 secs and then developed for 60 secs in a developing solution which comprises of a 1:5 solution of deionized water and 351 solution. The exposed regions are dissolved in the developing solution, the isolation trenches are etched using the same etching recipe that we used for the e-beam etch, the only difference being the etch time which is 65 secs.
Fig 3.12: Spin speed curves [74]

Fig.3.13: A Karl Suss MJB3 Mask Aligner [64].
Once the isolation trenches are etched, the chip is thoroughly cleaned using acetone, methanol and IPA to strip the photoresist. The chip is then blow dried using dry N\textsubscript{2} gas. Next, the etch depth is measured using KLA TENCOR P-15 Profilometer shown in Fig. 3.14. For InAs heterostructure, shown in Fig. 3.3, the 2DEG is located about 22 nm below the surface and is about 3.5 nm hence the isolation trench should be at least 26 nm deep to ensure complete isolation of the 2DEG from the rest of the chip.

Fig 3.14: KLA TENCOR P-15 Profilometer [75]

The next is to pattern the ohmic contacts. The clean dry chip is loaded onto a spin coater and a S1818 resist layer is coated using the same parameters that we used for defining the isolation trenches followed by exposure to define the ohmic contact openings. After exposure, the chip is dipped in chlorobenzene for 90 secs and then baked in the oven set at 90 °C for 180 secs. This step is necessary in order to obtain good, clean liftoff [76, 77].
3.4.4 **Metal contact deposition and patterning.**

Metal contacts are placed on the surface on the chip by thermal or e-beam evaporation. These are also referred to as bonding pads and are used to bond the chip onto the chip carrier. The metal deposition process is carried out in the closed chamber of a high vacuum (~2×10⁻⁶ Torr) evaporation system - Cooke vacuum Products, CVE-600-EB-FR-S-DC. Our system is equipped with both e-beam and thermal evaporation techniques. A well-researched ohmic contact recipe consist of Ni as a wetting agent for an Au-Ge alloy system. The three layers: Ni (12 nm), Ge (20 nm) and Au (200 nm) can be deposited sequentially. We deposit Ni and Ge by e-beam evaporation and Au by resistive heating. Typical deposition rates for Ni and Ge are 1 Å/sec to 2 Å/sec and Au at 5 Å/sec. The whole deposition is done in a single run without breaking the high vacuum. After the deposition is complete the chamber is allowed to cool down for 15 mins and is then vented with dry nitrogen for a few minutes and the sample is unloaded and carefully placed in the chip carrier. At this stage, the metal covers the entire area of the chip. The next processing step is lift-
off which is a fairly simple process. After depositing the metal, the sample is kept submerged in hot (~50°C) acetone for a few hours. The acetone strips the photoresist and along with it the overlying metal layer leaving only the ohmics on the sample surface. The metal contacts after lift-off can be seen in Fig. 3.16.

![Fig 3.16: Metal contacts with bonding wires](image)

### 3.4.5 Annealing

After the ohmic contact deposition and lift-off, the sample is annealed. It is done using a rapid thermal annealing set-up. We use AG associates, Heatpulse 210T Rapid Thermal Annealing (RTA) system for annealing our samples. The process consists of heating the chip in N₂
environment at 350 °C for 120 sec. RTA helps in alloy formation (Au-Ge) and diffusion of germanium into the 2DEG to create good ohmics. The diffused Germanium (into the wafer) acts as a dopant. The nickel acts as a wetting agent which prevents Au-Ge from coalescing on the surface during evaporation. The annealing process must be carefully optimized since under heating will lead to germanium not diffusing all the way through and over annealing will cause Nickel to diffuse to the 2DEG along with the Germanium and lead to higher resistance values in either case for the contacts [78].

3.4.6 Atomic Force Microscopy

Atomic force microscopy (AFM) is used to image the surface topography on a sub-micron scale. The atomic force microscope is a combination of the principles of the scanning tunneling microscope and the stylus profilometer and was invented by Binnig, Quate and Gerber in 1986 [79]. A schematic diagram is shown in Fig. 3.17. The technique involves the use of a shaped tip with an approximate radius of 10-20 nm. A feedback mechanism (not shown in the figure) is used that measures the tip’s interaction with the surface. Depending on the mode of operation, the tip may either be <10 nm above the surface to be scanned or oscillate up and down 100 nm to 200 nm above the sample surface. The basic principle involved is the same, while scanning across the sample; the tip height variation is recorded to produce a topographic image of the surface. The tip is positioned at the end of a diving-board-shaped cantilever beam. The attractive and repulsive forces between the tip and the sample surface deflect the cantilever beam. A laser beam, reflected from the tip of the cantilever, captures the magnitude of deflection. The plot of laser deflection as a function of tip position reproduces the topography of the sample surface.
Fig 3.17: Schematic diagram of an AFM showing the different components [80].

The AFM has three different modes of operation: contact, non-contact and tapping. In the contact mode the tip always remains at a fixed distance from the surface and it is almost always used when the force between the tip and the sample is repulsive. To boost the signal, low stiffness cantilevers are used. This mode is good only for solid samples and usually not preferred since there is always a possibility of the sample being contaminated or damaged if the tip contacts and scans along the surface due to attractive forces developing between the tip and the sample. Moreover, at ambient temperatures, most samples develop a liquid meniscus which can be a problem in contact mode of operation. The preferred mode therefore for our samples is the tapping mode, also known as the AC mode. In tapping mode, the cantilever is driven by a small piezoelectric element mounted in the AFM tip holder. By passing an electric current through this piezoelectric element, the tip is made to oscillate up and down near its resonance frequency. The frequency of oscillation is around
the resonant frequency of the tip. As the tip is brought close to the sample surface, Van der Waal forces, or dipole-dipole interactions, electrostatic forces, etc. cause the amplitude of this oscillation to decrease as the tip gets closer to the sample. In the non-contact mode, the tip does not touch the sample surface. The cantilever oscillates at an amplitude typically a few hundred nanometers. For our scans, we use a NCS15/AlBS tip made by Mikromasch. Figure 3.18 shows a sketch of the tip and its detailed specifications.

A Veeco Dimension 3100 AFM shown in Fig. 3.19 is used to get a three dimensional image scan of the QPCs. Analysis of an AFM scan provides information about the etch depth, the spacing between the two QPCs and width of the QPC channel region as well as its length. Figure 3.20 shows a typical AFM scan analysis of a QPC device along with different dimensions of the channel width, spacing, etc.

![NCS15/AlBS tip and tip specifications](image)

<table>
<thead>
<tr>
<th>Cantilever</th>
<th>Resonance Frequency, kHz</th>
<th>Force Constant, N/m</th>
<th>Length l ± 5, µm</th>
<th>Width w ± 3, µm</th>
<th>Thickness t ± 0.5, µm</th>
</tr>
</thead>
<tbody>
<tr>
<td>15 Series</td>
<td>265 (min), 325 (typ), 410 (max)</td>
<td>20 (min), 40 (typ), 80 (max)</td>
<td>125</td>
<td>30</td>
<td>4.0</td>
</tr>
</tbody>
</table>

Fig 3.18: NCS15/AlBS tip and tip specifications [81].
Fig. 3.19: A Veeco Dimension 3100 Model of AFM used in this work [82].

Fig. 3.20: AFM scan of a typical QPC device showing trench width, channel width and trench depth of a QPC along with the spacing between the two sets of in-plane SGs.
3.4.7 Packaging

Once we have accurately measured the device dimensions via AFM, the next step is to scribe the chip and bond the individual devices so that they could be easily loaded for measurement. We refer to scribing, mounting and bonding as packaging and is the last step of the device fabrication process. Each chip that we process has four QPC devices typically with different dimensions. We identify the devices by appropriate markers on the chip that we make using a diamond scribing pen before we begin fabrication. The wafers are diced using Tempress 1713-10C wafer scriber is shown in Fig. 3.21. The individual devices are mounted on to a chip carrier, using General Electric (GE) varnish. The devices are bonded to the chip carrier using Kullicke and Soffa model 4123 wedge bonder. To avoid the need for heating, we use gold pads and 25 mil diameter aluminum wires. The bonded chip carrier is then mounted on to the cryogenic insert for measurements. Figure 3.22 shows a complete bonded device.
3.5 Conductance Measurement

Once the sample is bonded, it is gently placed into the chip holder socket that is located in the sample holder section of the Dilution Refrigerator (DR) probe as shown in Fig 3.24. The probe with the QPC device mounted in it was inserted slowly into the dewar to avoid sudden thermal shocks. The LHe dewar is shown in Fig 3.23. The outer jacket of the dewar is pumped (to about 2 x 10^{-6} Torr) before transferring helium to ensure insulation from the outside atmosphere.
In order to minimize the LHe loss, we first precool the Dewar to 77K using liquid N\textsubscript{2} and let it sit for about 30mins before pumping it out and purging the system with Helium gas. Once the system has been purged of all nitrogen, we introduce LHe into the system. Typically our Dewar system, shown in Fig 3.23, holds 90 liters of LHe which lasts for about 8 days and gives us sufficient time to do our measurement before a refill is needed.

![Fig 3.24](image)

**Fig 3.24:** (a) Picture of the sample holder section of the DR probe insert showing the chip being held by the chip holder socket located at one end of the DR probe. (b) The far end of the DR probe insert with its main components indicated.

After that the electrical connections to the probe are made using coaxial cables, the gates are checked for leakage as well as the quality of ohmic contacts is verified. The detailed process of checking the gate leakage and the ohmic quality can be found elsewhere [34].
The contact resistance of the ohmics was measured using a four-probe measurement set up. Typically the contact resistance is less that 3KΩ in case of InAs QPCs. The left QPC and the right QPC (Fig. 3.25) of the QPC with four in-plane SGs were checked this way.

Fig. 3.25: (a) Typical schematic of a QPC device with four in-plane SGs. The source and drain are designated as ‘S’ and ‘D’. G1 and G2 represent the gates of QPC1 and G3 and G4 are the gates for QPC2.
Fig 3.26: An AFM image of the QPC device showing the channel region and the SGs. Dark red areas are the isolation trenches cut by e-beam lithography and wet etching technique to define the side-gates.

The low temperature conductance measurements were made using standard lock-in techniques. Figure 3.27 shows the circuit that was typically used to measure each of the four gate QPC devices. The major components are AMETEK Model 5210 dual-phase lock-in amplifiers, a Keithly 2000 multimeter, an Agilent 33220A function generator, and an Agilent E 3642A DC power supply. A custom made battery power supply was used to apply a no-noise DC bias voltages to the side-gates. Our experience with fabricating single QPC InAs devices guided us in determining the best dimensions for each of the QPCs. The two channel regions, in the four gate QPC, had widths ranging from 200 nm to 275 nm, and lengths of the order of 500 nm each. The spacing between the two adjacent pairs of gates was approximately 300nm (Fig. 3.26). The effective width and the carrier density in the channel are fine-tuned by the bias voltages on the two
side-gates. Since we are interested in the fundamental transport mode, a large 1D sub band separation is desired and this can be achieved in QPCs with small channel widths.

Since there is very little surface depletion at the InAs 2DEG/vacuum interface, typically, at 4.2 K the channel is found to be conducting for QPCs with even a very narrow channel width. This makes it easier to make measurements with InAs as compared to GaAs based devices [49].

The conductance of each QPC was measured as a function of gate voltage on each of the pair of SGs. The basic idea is to record the current $I$ that flows through the channel region due the application of a 17 Hz 100 μV AC signal between the source and the drain contacts and the voltage drop $V$ in the channel region. The linear conductance was calculated by dividing the current by the voltage ($G = I/V$). In order to avoid electron heating, it is important that the drain source voltage $V_{DS}$ be much less than $kT/q$ at the measurement temperature. The current and voltage were measured at 17 Hz using two synchronized lock-in amplifiers. The data points were collected by a computer using LabVIEW which interfaces with the different input and output components of our circuit. All measurements were carried out at $T= 4.2$ K and inside a Faraday cage.

The electrostatic dimensions of the QPC channel were changed by applying bias voltages to the metallic in-plane SGs (G1, G2 or G3, G4), depleting the channel near the side walls of the QPC. The detailed measurement set up is as shown in Fig 3.27. At the start of the experiment, to characterize the individual QPCs battery operated DC voltage sources were used to apply constant voltages, $V_{G1}$ and $V_{G2}$, to the two gates of left QPC while keeping the gates of the right QPC, $V_{G3}$ and $V_{G4}$, grounded. In addition to the DC bias, a sweep voltage $V_{sweep}$ was applied to the first pair of SGs (G1 and G2). The linear conductance ($G = I/V$) of the channel was measured for different $\Delta V_G = V_{G1} - V_{G2}$ as a function of $V_{sweep}$, with a drain-source voltage of 100 μV and a set of curves was obtained for different values of symmetric potential on G3 and G4.
Fig 3.27: Circuit used to measure the conductance of each of the QPCs of the device.

Next, with the same setup, an asymmetric potential, $\Delta V_G = V_{G3} - V_{G4}$ was applied between the two SGs on the right and the influence of this bias on the spin polarization generated by the first pair of gates was observed. The conductance of the first QPC was then recorded as a function of a common sweep voltage, $V_{\text{sweep}}$, applied to the two gates on the left (in addition to the potentials $V_{G1}$ and $V_{G2}$ which create the asymmetry), with the current flowing in the $x$-direction (Fig. 3.27). The linear conductance $G = I/V$ of the channel was measured for different $\Delta V_G$ as a function of $V_{\text{sweep}}$, with a drain-source drive voltage of 100 $\mu$V. The value of the gate voltages corresponding to the maximum width of the 0.5 conductance plateau was noted.
Typically, each of the conductance curves was cycled a few times until the subsequent curves were reproducible. This was done to minimize contributions from the movement of impurities (that are present at the vacuum/2DEG interface) to the net conductance of the QPC. Once the QPCs were characterized, conductance measurements using four different biasing conditions on the four SGs were performed on these devices as described in the next chapter.
Chapter 4
Experimental Results and Conclusion

4.1 Introduction

First we describe the results of NEGF simulations of the QPC with four in-plane side gates (SGs) proposed in this thesis to assess its potential as a tunable all electric spin polarizer. Next we report our experimental results for low temperature, low noise, and conductance measurements on these new QPC devices. In order to control the amount of spin polarization through the four gate QPC devices, two sets of biasing conditions were investigated. In the first set of experiments, the first set of gates near the source contact is asymmetrically biased to create strong spin polarization in its channel. A symmetric bias is applied on the second set of gates near the drain contact to study the effect of this bias on the spin polarization. In the second set of experiments, we investigated the influence of an asymmetric bias of both polarities of the applied voltage on the second set of gates near the drain on the amount of spin polarization as created by the first set of gates near the source. When the second half of the QPC is operated close to threshold, we have observed unexpected hysteresis and negative differential resistance in the conductance measurements which we conjecture are signatures of Coulomb and Spin blockaded transport through the devices. These features cannot be explained within the context of NEGF approach used in this thesis.

4.2 QPC with two sets of in-plane side gates

In light of the experimental and theoretical results that we have obtained previously it seems imperative to find a way to control and finely tune the location of a conductance anomaly
to achieve this spin conductance polarization over a broader range of gate biases for a specific QPC [33, 34, 35]. Our proposed new QPC device consists of a QPC with two sets of in-plane SGs. A schematic of the device was shown in Fig 3.24. A 3D AFM image of a fabricated device is shown in Fig. 4.1 in which the isolation trenches can be clearly seen. The source (S), drain (D) and the four in-plane SGs (G1, G2, G3, G4) are clearly labeled. In Fig.4.1, the width of each of the four gates of the QPC was about 350 nm with a 275 nm spacing between the two sets. The width of the channel was kept the same as that of the single QPC devices fabricated, i.e., about 300 nm.

Fig 4.1: 3D AFM image of the QPC with two sets of in-plane SGs.

4.3 NEGF simulations of four gate QPC devices

For the theoretical analysis of the device, we use the NEGF approach developed by a former Ph.D student, Junjun Wan [35]. All dimensions of the QPC are defined with reference to Fig 4.2. In simulation, the device dimensions are about a factor of ten smaller than the actual device to keep the computation time for convergence of NEGF simulations reasonable (a few days for some simulations).
In this structure, a bias asymmetry \( V_{G1} - V_{G2} \) is applied between the two leftmost gates (nearest the source) to create spin polarization in the channel. An additional common-mode bias \( V_{\text{sweep}} \) is applied to both those gates. The second set of gates, closest to the drain, and separated by a gap ‘d’ from the first set, is biased at a fixed symmetric potential \( V_{G3} = V_{G4} \). The latter was varied to control the amount of depletion in region II of the QPC. In the numerical examples, an InAs QPC was considered and its conductance was calculated using the NEGF approach described in refs. [32, 67]. This approach is briefly summarized in appendix I. It was found that the second set of gates has a profound effect on the spin polarization of the QPC. As shown below, it is observed that the range of \( V_{\text{sweep}} \) over which the spin polarization \( \alpha = \frac{G_{\text{up}} - G_{\text{down}}}{G_{\text{up}} + G_{\text{down}}} \) is appreciable, is much larger for the four gate structure than a comparable QPC with only two gates, i.e., a device with a length \( = 2l_2 + d \) and one gate at potential \( V_{G1} + V_{\text{sweep}} \) and the other gate at potential \( V_{G2} + V_{\text{sweep}} \).

![Diagram of four-gate QPC device](image)

**Fig. 4.2:** Proposed four-gate QPC device. In the simulations, the potential on the two side gates close to the source was set equal to \( V_{\text{sg1}} = -0.2 \, \text{V} + V_{\text{sweep}} \), \( V_{\text{sg2}} = +0.2 + V_{\text{sweep}} \), \( V_s = 0.0 \), and \( V_d = 0.3 \, \text{mV} \). The potential on the two SGs next to the drain was kept the same at a fixed value. The current flows in the x-direction [83].
The NEGF simulations were performed on the four-gate InAs QPC with the parameters shown in Fig. 4.2. The effective mass in the InAs channel was set equal to $0.023m_0$ and all calculations were performed at 4.2 $K$. Figure 4.3 shows the conductance versus $V_{\text{sweep}}$ of the four gate QPC, where $G_T$ is the total conductance and $G_{\text{up}}$ and $G_{\text{down}}$ the contributions from the up spin and down spin electrons, respectively. The initial biases on the gates are $V_{G1} = -0.2 \ V + V_{\text{sweep}}$, $V_{G2} = +0.2 \ V + V_{\text{sweep}}$, and $V_{G3} = V_{G2} = 0.0 \ V$. Figure 4.3 shows a conductance anomaly around 0.5 $G_0$ (the oscillations are due to multiple reflections at the ends of the QPC) [83]. It is a signature of spin polarization in the channel as $G_{\text{up}}$ is much larger than $G_{\text{down}}$ over the range of $V_{\text{sweep}}$ from -0.2 $V$ to 0$V$ where the conductance anomaly appears. For an equivalent single-gate QPC, with length $2l_2+d=48$nm, and the same bias conditions on $V_{G1}$ and $V_{G2}$, the range of $V_{\text{sweep}}$ over which $G_{\text{down}} \neq G_{\text{up}}$ was found to be -0.1$V$ to 0$V$, half the range for the four gate QPC. For a QPC with length $l_2=22$ nm, and the same bias conditions we found $G_{\text{down}} = G_{\text{up}}$ for all $V_{\text{sweep}}$ and there is no spin polarization in the channel.

Figure 4.4 is a plot of the total conductance versus $V_{\text{sweep}}$ of the four gate QPC described above with $V_{G1} = -0.2 + V_{\text{sweep}}$, $V_{G2} = +0.2 + V_{\text{sweep}}$. The three different curves are for the bias on the two gates closest to the drain being equal to $V_{G3} = V_{G4} = 0.0 \ V$, -0.1 $V$, and -0.2$V$. These curves show that the conductance anomaly can be fine-tuned by varying the negative potential on gates 3 and 4. The range of $V_{\text{sweep}}$ over which the conductance anomaly appears also strongly depends on the negative bias on gates 3 and 4. This is best illustrated by plotting the spin conductance polarization $\alpha$ corresponding to the three curves shown in Fig. 4.4. Figure 4.5 shows that the range of $V_{\text{sweep}}$ over which the spin polarization ($\alpha$) is different from zero increases from 0.2 to 0.5 $V$ when to $V_{G3} = V_{G4}$ is changed from 0.0$V$ to -0.2$V$. The maximum value of $\alpha$ was found to be nearly the same (~97%) for $V_{G3} = V_{G4}$ equal to 0.0 $V$, -0.1 $V$, and -0.2$V$. At the value
of $V_{\text{sweep}}$ corresponding to $\alpha_{\text{max}}$, the total charge density over the first half of the four gate QPC (region I in Fig. 4.2) was found equal to 0.14, 0.17, and $0.23 \times 10^{12}$ cm$^{-2}$.

A qualitative explanation for these results is as follows. The negative bias on gates 3 and 4 creates a potential barrier to electrons flowing through the first portion of the QPC. This enhances space-charge effects in the left half of the QPC closer to the source, leading to an increase in the e-e interaction, one of the ingredients needed for enhanced spin polarization in the channel [32]. This enhanced space charge control of the spin polarization effect can be viewed as a proximity effect in which the electrostatic potential of gates 3 and 4 affects the conduction band profile in region I including the potential walls between the QPC channel and etched regions. This affects the amount of LSOC whose strength is proportional to the slopes of the QPC walls. As a result, the proximity of gates 3 and 4 allows for fine tuning the amount of spin polarization in the overall structure.

Figure 4.6 shows the experimental results in qualitative agreement with the NEGF results. The conductance plots were obtained using the procedure described in the next section.
Fig. 4.3: Conductance versus $V_{\text{sweep}}$ of a four gate QPC with the following parameters: $w_1 = 48$ nm, $l_1 = 80$ nm, $w_2 = 16$ nm, $l_2 = 22$ nm, $d = 4$ nm. $G_T$ is the total conductance and $G_{\text{up}}$ and $G_{\text{down}}$ the contributions from the up spin and down spin electrons. The biases on the gates are set to be $V_{G_1} = -0.2 + V_{\text{sweep}}$, $V_{G_2} = +0.2 + V_{\text{sweep}}$, and $V_{G_3} = V_{G_4} = 0.0$ V. Also shown for comparison is $G_T$ for a QPC with only two gates, with the same bias but for $l_2 = 22$ and 48 nm.
Fig. 4.4: Total conductance versus $V_{\text{sweep}}$ of a four-QPC with the following parameters: $w_1 = 48$ nm, $l_1 = 80$ nm, $w_2 = 16$ nm, $l_2 = 22$ nm, $d = 4$ nm. The biases on the gates close to the source are set as follows: $V_{G1} = -0.2 + V_{\text{sweep}}$, $V_{G2} = +0.2 + V_{\text{sweep}}$. The biases on the two gates close to the drain are set equal: $V_{G3} = V_{G4} = 0.0$, -0.1, and -0.2V, respectively. All calculations were performed using $V_S = 0.0$, $V_d = 0.3$ mV and $T = 4.2$K.

Fig. 4.5: Spin conductance polarization $\alpha = (G_{\text{up}} - G_{\text{down}})/(G_{\text{up}} + G_{\text{down}})$ versus $V_{\text{sweep}}$ of a four gate QPC with the following parameters: $w_1 = 48$ nm, $l_1 = 80$ nm, $w_2 = 16$ nm, $l_2 = 22$ nm, $d = 4$ nm. The different curves correspond to the biasing conditions $V_{G1} = -0.2 + V_{\text{sweep}}$, $V_{G2} = +0.2 + V_{\text{sweep}}$ for a QPC with a single set of in-plane gates and a length of the narrow portion of the QPC equal to $2l_2 + d = 48$nm. The following parameters were used $V_S = 0.0$, $V_d = 0.3$ mV and $T = 4.2$K.
4.4 Experimental Results

To assess the validity of our NEGF simulations, we performed conductance measurements on the four gate InAs QPC device, as shown in Fig. 4.1, using the following procedure:

1. An asymmetric bias was first applied between the leftmost gates $G_1$ and $G_2$ and an additional voltage $V_{\text{sweep}}$ (frequency : 3 mHz) was applied on both gates. The common gate voltage $V_{\text{sweep}}$ was then varied until a conductance anomaly was found in the conductance with the potential on the two rightmost gates kept constant at 0V. This guarantees that the QPC channel is wide opened between the two gates $G_3$ and $G_4$.

2. Once a strong 0.5 $G_0$ plateau was observed, the collection of the conductance data system was allowed to cycle over several cycles (forward and reverse sweeps) of the common gate voltage $V_{\text{sweep}}$ to make sure that the conductance plateau being observed is robust and reproducible.

3. The potential on the second set of gates was then made more negative to pinch the channel under the right portion of the QPC to electrostatically influence the space-charge effects and fine-tune the importance of the asymmetry in the LSOC in the left portion of the QPC, as demonstrated in our NEGF simulations. In one set of experiments the potential on the two gates $G_3$ and $G_4$ was kept the same. In another set of experiments the potential difference between the two gates was applied. No additional common sweep voltage was superimposed on the two rightmost gates.

Figure 4.6 shows the conductance plots obtained experimentally for an InAs four gate QPC device shown in Fig.4.1 with the width of each of the four gates of the QPC being around 350nm with a 275 nm spacing between the two pairs of gates. The width of the channel was kept same as
that of the single QPC devices i.e. about 300 nm. In Fig. 4.6, the following biasing conditions were used: $V_{G1} = -1.0 + V_{\text{sweep}}$, $V_{G2} = 0.0 + V_{\text{sweep}}$, and the potential on the right most gates was kept the same and varied, progressively, starting with 0V to more and more negative values to pinch the channel on the right side of the QPC.

![Graph showing conductance of four gate InAs QPC device for different sweep voltages.](image)

Fig. 4.6: Conductance of four gate InAs QPC device shown in Fig. 4.1 for $V_{G1} = -1.0 + V_{\text{sweep}}$ and $V_{G2} = 0.0 + V_{\text{sweep}}$ for different values of the same potential applied to gates 3 and 4 as shown in the inset. Measurements were taken at $T = 4.2K$. The voltages $V_{G3}$ and $V_{G4}$ are identical. No common sweep voltage is added to these two gates. The leftmost curves are the actual conductance data for $V_{G3} = V_{G4} = -2.8 \text{ V}$, all the other curves have been shifted to the right for clarity.
Figure 4.6 indicates that the conductance anomaly near $G = 0.5 \ G_0$ can indeed be tuned. The size of the conductance plateau is over a much broader range of $V_{\text{sweep}}$ (about 1 V) for the case of $V_{G3} = V_{G4} = -2.8V$ compared to the case of $V_{G3} = V_{G4} = 0V$. This is in qualitative agreement with the numerical simulations of Fig. 4.5, which shows an increase in the range of $V_{\text{sweep}}$ for which the spin conductance polarization is non-zero as more negative potential is applied to the two rightmost gates. Between the two extreme conductance plots shown in Fig. 4.6, the conductance anomaly is either above or below the $0.5 \ G_0$ value, also in agreement with the results shown in Fig 4.4. The agreement is only qualitative for two reasons:

1. The dimensions of the simulated device are much smaller than the actual device.
2. The NEGF simulations do not take into account the influence of impurity and surface scattering which has been shown to have a profound influence on the shape, number and location of the conductance anomalies [48].

To further investigate the potential for fine tuning the size and location of the conductance anomaly near $0.5 \ G_0$, Figures 4.7 through 4.10 show the conductance plots obtained with a bias applied between the second set of gates. In all measurements depicted in Figures 4.7-4.10, the bias on the leftmost gates was set equal to $V_{G1} = -0.4 + V_{\text{sweep}}$ and $V_{G2} = -0.7 + V_{\text{sweep}}$. Figure 4.7 shows the conductance curves obtained with voltage $V_{G3}$ varied from -0.3V to -1.7V (from left to right) in steps of -0.1V. Figure 4.8 shows the conductance plot with the voltage $V_{G3}$ was varied back from -1.7V to -0.3V (from left to right) in steps of 0.1V to test the robustness of the conductance measurements performed in Fig.4.7. In both Figures 4.7 and 4.8 $V_{G4}$ was held constant at -0.3V.

In Fig.4.7, the potential difference between the two gates is $V_{G1} - V_{G2} = 0.3 \ V$ for all values of $V_{\text{sweep}}$. The different set of conductance plots shown in Fig.4.7 corresponds to values of $V_{G3}$ –
$V_{G4}$ increasing from 0 to -1.4 V, from left to right. The conductance anomaly around near 0.5 $G_0$ is more pronounced when $V_{G3} - V_{G4} = 0$ and is progressively washed out as $V_{G3} - V_{G4}$ becomes more negative. This is also attributed to the proximity effect discussed above. The polarity of $V_{G3} - V_{G4}$ being opposite to $V_{G1} - V_{G2}$, the two rightmost gates have the tendency to balance out the spin imbalance in the LSOC created by the two leftmost gates and weaken the amount of spin polarization through the structures. Because this is a proximity effect only, the effect of the gates 3 and 4 does not completely wipe out the spin polarization due to the asymmetric bias between gates 1 and 2 and evidence of spin polarization (i.e., a plateau around 0.5 $G_0$) can still be seen even when $V_{G3} - V_{G4} = -(V_{G1} - V_{G2}) = -0.3$ V. More negative bias is needed between the two rightmost gates to counteract the effect of the first set of gates.

To test the reliability of the previous results, Fig. 4.8 shows the set of conductance curves as the bias $V_{G3}$ was varied back from -1.7V (leftmost curve) to -0.3V (rightmost curve) in steps of 0.1V with $V_{G4}$ held constant at -0.3V. Figure 4.8 shows that the conductance anomaly near 0.5 $G_0$ becomes progressively more pronounced as the value of $V_{G3} - V_{G4}$ is made less negative and approaches 0V, in agreement with the trend observed in Fig.4.7. A close examination of Figures 4.7 and 4.8 for the same set of bias $V_{G3}$ and $V_{G4}$ shows that the conductance curves are not exactly the same. The possible onset of hysteresis in asymmetrically biased QPC devices with only two SGs in the presence of LSOC has been recently studied by James Charles, working on his senior project with M. Cahay. They have shown that an intrinsic bistability and accompanying hysteresis in the conductance versus common gate voltage applied to the two SGs exists only if the narrow portion of the QPC is long enough. Furthermore, the hysteresis is absent if the effects of electron-electron interaction are neglected but increases with the strength of the electron-electron interaction. The hysteresis appears in the region of conductance anomalies, i.e., less than $2e^2/h$. 
and is due to multistable spin textures in these regions [83]. We believe the hysteresis observed in
the four gate QPC device investigated here is also linked to the presence of multistable spin
textures. The nature of the multistable state in four gate QPC device is further complicated by the
proximity effect discussed above

Fig. 4.7: Conductance of four gate QPC device shown in Fig. 4.1 with $V_{G1} = -0.4 + V_{\text{swep}}$ and $V_{G2} = -0.7 + V_{\text{swep}}$ for different values of the potential applied to gates 3 and 4 as shown in the inset. Measurements were taken at $T = 4.2K$. The voltage $V_{G3}$ is varied from -0.3V to -1.7V (from left to right) in steps of -0.1V. $V_{G4}$ is held constant at -0.3V. The leftmost curves are the actual conductance data for $V_{G3} = V_{G4} = -2.8$ V, all the other curves have been shifted to the right for clarity.
Fig. 4.8: Conductance of four-gate QPC device shown in Fig. 4.1 for $V_{G1} = -0.4 + V_{\text{sweep}}$ and $V_{G2} = -0.7 + V_{\text{sweep}}$ for different values of the potential applied to gates 3 and 4 as shown in the inset. Measurements were taken at $T=4.2\text{K}$. The voltage $V_{G3}$ is varied from $-1.7\text{V}$ to $-0.3\text{V}$ (from left to right) in steps of $0.1\text{V}$. $V_{G4}$ is held constant at $-0.3\text{V}$.

The set of measurements shown in Figures 4.7 and 4.8 was repeated with the biasing conditions on gates 3 and 4 interchanged (the potential on gates 1 and 2 being the same as before). Figure 4.9 corresponds to the case where the voltage $V_{G4}$ was varied from $-0.3\text{V}$ to $-1.7\text{V}$ (from left to right) in steps of $0.1\text{V}$. Figure 4.10 shows the conductance plot with the voltage $V_{G4}$ varied...
back from -1.7V to -0.3V (from left to right) in steps of 0.1V. In both Figures 4.9 and 4.10 $V_{G3}$ was held constant at -0.3V.

The results shown in Figures 4.9 and 4.10 are similar to those observed in Figures 4.7 and 4.8, i.e., the observation of a more pronounced anomaly around 0.5 $G_0$ as $V_{G3} - V_{G4}$ approaches 0V.

Fig. 4.9: Conductance of four-gate QPC device shown in Fig. 4.1 for $V_{G1} = -0.4 + V_{\text{sweep}}$ and $V_{G2} = -0.7 + V_{\text{sweep}}$ for different values of the potential applied to gates 3 and 4 as shown in the inset. Measurements were taken at $T=4.2K$. The voltage $V_{G4}$ was varied from -0.3V to -1.7V (from left to right) in steps of -0.1V. $V_{G3}$ was held constant at -0.3V.
Fig 4.1: Conductance of four-gate QPC device shown in Fig. 4.1 for $V_{G1} = -0.4 + V_{\text{sweep}}$ and $V_{G2} = -0.7 + V_{\text{sweep}}$ for different values of the potential applied to gates 3 and 4 as shown in the inset. Measurements were taken at $T=4.2\,\text{K}$. The voltage $V_{G4}$ was varied from -1.7V to -0.3V (from left to right) in steps of 0.1V. $V_{G3}$ was held constant at -0.3V.

The results discussed in this section show that the four gate QPC device indeed acts as a tunable spin polarizer and that the observation of a well-defined conductance anomaly near 0.5 $G_0$ occurs when the same sufficiently negative bias is applied to the rightmost SGs. This helps pinch the QPC channel near the drain and accentuate the effects of electron-electron interaction in the leftmost part of the QPC. The experimental results are in good qualitative agreement with NEGF simulations based in a Hartree-Fock description of the effects of electron-electron interaction, as described in Appendix I. Next, we consider the effect of a very large negative bias applied to both
gates 3 and 4 which eventually can lead to pinch-off of the QPC channel in that region. As shown in the next section, peaks on the conductance curves appear in that regime of operation which are attributed to the onset of Coulomb/Spin blockade effects in the device.

4.5 Onset of Hysteresis and Negative Resistance Region

Next we analyze the effect of increasing the negative bias on the rightmost SGs. In the set of measurements shown in Figs 4.11(a)-(c), the following biasing conditions were used: $V_{G1} = -0.1 + V_{\text{sweep}}$, $V_{G2} = 0 + V_{\text{sweep}}$, and $V_{G3} = V_{G4}$ was set equal to -3.5V, -4.0V and -4.5V in Figs. 4.11(a), 4.11(b) and 4.11(c), respectively.

![Graph](image)

Fig. 4.11(a): Conductance vs $V_{\text{sweep}}$ for $V_{G1} = -1.0 + V_{\text{sweep}}$ and $V_{G2} = 0.0 + V_{\text{sweep}}$. The second set of gates is biased symmetrically with a negative bias $V_{G3} = V_{G4} = -3.5$ V. No sweep voltage is superimposed on gates 3 and 4. All measurements were taken at $T = 4.2$K.
Fig. 4.11(b): Conductance vs $V_{\text{sweep}}$ for $V_{G1} = -1.0 + V_{\text{sweep}}$ and $V_{G2} = 0.0 + V_{\text{sweep}}$. The second set of gates is biased symmetrically with a high negative bias $V_{G3} = V_{G4} = -4.0$ V. No sweep voltage is superimposed on gates 3 and 4. All measurements were taken at $T = 4.2$ K.

Fig. 4.11(c): Conductance vs $V_{\text{sweep}}$ for $V_{G1} = -1.0 + V_{\text{sweep}}$ and $V_{G2} = 0.0 + V_{\text{sweep}}$. The second set of gates is biased symmetrically with a high negative bias $V_{G3} = V_{G4} = -4.5$ V. No sweep voltage is superimposed on gates 3 and 4. All measurements were taken at $T = 4.2$ K.
The trends observed in Figs. 4.11(a) – (c) are as follows:

1. There is hysteresis observed in the conductance plots which becomes more prominent as the voltage on the gates G3 and G4 is made more and more negative.

2. The conductance plots saturate at a lower value (in units of \(2e^2/h\)) at the maximum applied sweep voltage of 9V.

3. The conductance saturation level is near zero for the largest value of applied voltage to the two rightmost SGs (Fig 4.11(c)).

4. Distinct peaks in the conductance are observed when \(V_{G3} = V_{G4} = -4.5\)V. Figure 4.11(c) shows three sharp peaks nearly equally spaced by about 1V along the \(V_{sweep}\) axis.

5. The conductance peaks are much smaller in magnitude than \(2e^2/h\). The appearance of conductance peaks, their small amplitude and their equal spacing are characteristics of Coulomb blockade transport in nanoscale devices [95].

Referring to Fig.4.12, we offer the following explanation for the data shown in Figs 4.11(a)-(c). In a one electron picture of carrier, the available energy subbands in the narrow portion of the QPC due to the lateral confinement are shown as depicted in Fig. 4.12(b). The locations of the energy subband bottoms are different in the left and the right portions of the QPC because of the different biasing conditions on the left and right SGs. The Fermi level is shown as constant across the entire structure which is a good approximation since the source to drain bias is very small. In the right portion of the figure, a single electron picture of carrier transport is used. The locations of the energy subbands are shifted upwards in energy from \((E_1^R,E_2^R,E_3^R,..)\) to \((E'_1^R,E'_2^R,E'_3^R,..)\) by increasing the negative bias on gates G3 and G4. When the potential on the two rightmost SGs is made more negative, the separation between the energy levels \(E'_1^R,E'_2^R, E'_3^R,..\)
will increase. When the negative bias on gates $G_3$ and $G_4$ approaches threshold for conduction, only one subband will participate in transport until $E_{1R}'$ is more than $2k_BT$ above $E_F$ quenching the conduction through the device. The rightmost part of the device is therefore the bottleneck controlling the transport through the entire QPC structure. By first applying a large negative bias to gates $G_1$ and $G_2$, we can similarly pinch off the left portion of the QPC channel. When superimposing a common positive voltage $V_{sweep}$ on gates $G_1$ and $G_2$, the leftmost part of the QPC channel gradually widens and the conductance through the structure should increases in steps of $2e^2/h$ as the energy levels $E_{1L}, E_{2L}, E_{3L}, \ldots$ progressively line up with the Fermi level and the energy level $E_{1R}$. If an asymmetry is applied between the leftmost SGs, spin polarization will be induced in that region of the QPC channel and conduction steps should be observed in units of $e^2/h$. This is the regime of operation illustrated in Figs. 4.7 – 4.10. The fact that only a step around 0.5 $G_0$ was observed in the conductance plots is attributed to the influence of surface roughness and impurity scattering in the narrow portion of the QPC [48].

For a sufficiently large negative bias on the gates $G_3$ and $G_4$, the electrostatic bottleneck created in that region of the device can be thought of as a potential barrier for the left portion of the QPC and the region located between the two sets of side gates. In this regime of operation, we conjecture that the left region of the QPC acts as a quantum dot in which electrons will accumulate. As a result, the effects of electron-electron become increasingly important and can no longer be modeled with a self-consistent Hartree-Fock approximation of space-charge effects as used in NEGF simulations.

Because of the strong electron-electron interaction, a many body description of carrier transport is needed in the left portion of the QPC. If we adopt a single Coulomb blockade picture of transport in this region, the energy diagram for energy levels available for carrier transport must
now be replaced by the one shown in Fig. 4.12(c). The one electron picture still holds in the right portion of the device and the bottom of the energy levels $E_1^R$, $E_2^R$, $E_3^R$,.. can be tuned with the amount of negative bias on gates $G_3$ and $G_4$. Starting below the threshold for conduction in the left portion of the QPC, the Coulomb blockade energy ladder can be brought down in energy with a positive common gate voltage $V_{\text{sweep}}$ on gates $G_1$ and $G_2$. As the different levels in the Coulomb ladder lined up with the Fermi level and the lowest energy level $E_1^R$ in the right portion of the QPC, peaks will appear in the conductance of the device. The three peaks observed in the conductance plot in Fig. 4.11(c) are attributed to the progressive alignment of the three lowest levels in the Coulomb ladder with $E_1^R$ and $E_F$ as $V_{\text{sweep}}$ increases.

The eventual quenching of the conductance at large value of $V_{\text{sweep}}$ is explained as follows. As more energy levels in the Coulomb ladder fall below the Fermi level, space charge effects in the left portion of the QPC are becoming increasingly important. This influences electrostatically the confinement potential in the right portion of the QPC. As a result, we conjecture that the energy level $E_1^R$ is pushed up in energy, away from $E_F$, causing a sudden drop in conductance at large values of $V_{\text{sweep}}$ as the right portion of the QPC is operated below threshold. As $V_{\text{sweep}}$ is lowered, the electrons that are piled up in the left portion of the QPC cannot escape to the drain and are pushed back towards the source contact. This mechanism offers plausible explanation for the hysteresis seen in the conductance plot of Fig. 4.11(c). At a sufficiently negative voltage, all electrons which had accumulated in the left portion of the QPC have been pushed back into the source and the left portion of the QPC channel is pinched off. We have observed that the conductance peaks and hysteresis loop in Fig 4.11(c) are reproducible by cycling several times through the up and down sweeps of the common gate voltage $V_{\text{sweep}}$.  

97
Fig 4.12 (a): Schematic of QPC with a pair of in-plane SGs with gate contacts $G_1$, $G_2$, $G_3$, and $G_4$. (b) Energy levels corresponding to single electron picture of carrier transport through four gate QPC device. (c) Coulomb blockade picture of carrier transport through the four gate QPC device. $E_F$ is the Fermi level across the entire structure and is assumed to be constant since the source and drain potential is small.
Next, we estimate the separation between the conductance peaks shown in Fig 4.11(c). To estimate the energy spacing $e^2/2C$ in the Coulomb ladder, we model the leftmost portion of the QPC as capacitor whose total capacitance is given by, as shown in Fig.4.12(c),

\[
C_{\text{TOT}} = C_1 + C_2 + C_S + C_R + C_{\text{FF}} \quad 4.1
\]

where $C_1$ and $C_2$ are the coupling capacitances of the central region on the left with the gates $G_1$ and $G_2$, $C_S$ is the coupling capacitance with the source, and $C_R$ is its coupling capacitance with the right portion of the QPC. $C_{\text{FF}}$ accounts for the capacitance due to fringing fields.

The coupling capacitances $C_1$ and $C_2$ are equal and approximated the parallel plate formula

\[
C_1 = C_2 = \frac{\varepsilon A}{d} \quad 4.2
\]

where $A$ is the area of the plates and $d$ is the separation between the QPC channel and the SGs, i.e., equal to the width of the isolation trenches (roughly 300 nm wide). Since the length of left portion of the QPC is approximately 500nm and the width of the 2DEG is taken as the width of the InAs well, i.e. $3.5\text{nm}$ (see Fig. 3.15), the area $A$ in Eq. (4.2) is roughly

\[
A = 500\text{nm} \times 3.5\text{nm} = 1750 \times 10^{-18}m^2 \quad 4.3
\]

Thus the capacitance in eq. 4.1 is be estimated to be

\[
C_1 = C_2 = \frac{\varepsilon A}{d} = 2.3 \text{ aF}
\]

where we have used $\varepsilon_r = 15.15$ for the relative dielectric constant of InAs, and $\varepsilon_0 = 8.85 \times 10^{-12} \text{ F/m}$.
The contributions of the other capacitances $C_s$, $C_r$, $C_{FF}$ are tougher to estimate but are also of the order of an attoFarad. Therefore, if we use $C_{TOT} \sim 5$-10 aF, the energy separation between the energy levels in the Coulomb ladder is estimated to be

$$E_c = \frac{e^2}{2C_{TOT}} \approx 15 - 30 \text{ meV}$$

4.4

Shifting the energy levels in the Coulomb ladder by $E_c$ to progressively aligned them with the Fermi level and energy $E_{1R}$ requires changes in $V_{\text{sweep}}$ which are much larger than 16 mV due to the gaps separating the SGs from the central portion of the QPC. This is similar to the experimental results shown in Fig.1.6 for a QPC with two top contacts where changes in bias of around 100 mV were necessary to shift the bottom of the different subbands through the Fermi level. In this case, the separation through the subbands being only a few meV, a factor of about 50 exists between the shift in the potential on the top gates and the bottom of the conduction band in the narrow portion of the QPC. If we use a similar factor to estimate the shift in the common gate voltage needed on the SGs for our four gate QPC device, a shift of the order of 0.750-1.5 V is needed in the sweep voltage to align the different energy levels in the Coulomb ladder and add an extra electron in the left portion of the QPC. This estimate is in close agreement with the measured separation near 1 V between the three conductance peaks shown in Fig. 4.11 (c). Our simple Coulomb blockade model constitutes a first ballpark satisfactory agreement considering the simple estimate of the contributions of the capacitances given above.

To test the importance of spin in the blockade mode of operation described above, the measurements depicted in Fig. 4.11 were repeated with a symmetric potential applied to the gates 1 and 2, i.e., $V_{G1} = V_{G2} = 0.0 + V_{\text{sweep}}$, for different values of the large negative bias applied to gates 3 and 4. The results are shown in Figures 4.13(a) - (e). Similar features to those observed in
Figures 4.11(a)-(c) can be seen. The shape of the conductance peaks are different in Figures 4.11 and 4.13 indicative that the Coulomb blockade description should actually be improved to account for spin dependence of the energy levels in the left portion of the QPC due to the asymmetric potential on gates 1 and 2 in the presence of LSOC. A more accurate description of carrier transport needs to be based on a spin blockade regime of operation.

![Graph showing conductance versus sweep voltage](image)

Fig. 4.13(a): Conductance vs $V_{\text{sweep}}$ for $V_{G1} = 0.0 + V_{\text{sweep}}$ and $V_{G2} = 0.0 + V_{\text{sweep}}$. The second set of gates is biased symmetrically with a high negative bias $V_{G3} = V_{G4} = -4.1 \text{ V}$. No sweep voltage is superimposed on gates 3 and 4. All measurements were taken at $T = 4.2 \text{K}$. 
Fig. 4.13(b): Conductance vs $V_{\text{sweep}}$ for $V_{G1} = 0.0 + V_{\text{sweep}}$ and $V_{G2} = 0.0 + V_{\text{sweep}}$. The second set of gates is biased symmetrically with a high negative bias $V_{G3} = V_{G4} = -4.2$ V. No sweep voltage is superimposed on gates 3 and 4. All measurements were taken at $T = 4.2$K.

Fig. 4.13(c): Conductance vs $V_{\text{sweep}}$ for $V_{G1} = 0.0 + V_{\text{sweep}}$ and $V_{G2} = 0.0 + V_{\text{sweep}}$. The second set of gates is biased symmetrically with a high negative bias $V_{G3} = V_{G4} = -4.3$ V. No sweep voltage is superimposed on gates 3 and 4. All measurements were taken at $T = 4.2$K.
Fig. 4.13(d): Conductance vs $V_{\text{sweep}}$ for $V_{G1} = 0.0 + V_{\text{sweep}}$ and $V_{G2} = 0.0 + V_{\text{sweep}}$. The second set of gates is biased symmetrically with a high negative bias $V_{G3} = V_{G4} = -4.35$ V. No sweep voltage is superimposed on gates 3 and 4. All measurements were taken at $T = 4.2$K.

Fig. 4.13(e): Conductance vs $V_{\text{sweep}}$ for $V_{G1} = 0.0 + V_{\text{sweep}}$ and $V_{G2} = 0.0 + V_{\text{sweep}}$. The second set of gates is biased symmetrically with a high negative bias $V_{G3} = V_{G4} = -4.4$ V. No sweep voltage is superimposed on gates 3 and 4. All measurements were taken at $T = 4.2$K.
4.6 Conclusions

This chapter has shown that the four gate QPC device studied in this thesis can be used as an all electrical spin polarizer. The leftmost SGs are used to create the spin polarization and the rightmost SGs are used to control current flow through the device and fine tune the electrostatic potential under the leftmost SGs, hence controlling the amount of electron-electron interaction and their influence on the strength of the LSOC in the leftmost portion of the device. We have shown that the size and location of the conductance anomaly near $0.5 \ G_0$ can be tuned over a large range of biases applied to the four SGs. When the rightmost set of gates is not operated close to pinch off, our conductance measurements were shown to be in qualitative agreement with the results of NEGF simulations in which the effects of electron-electron interactions are treated in the Hartree-Fock approximation.

For large negative bias applied on the rightmost SGs for which the narrow portion of the QPC in that region that is close to pinch off, we have argued that the device is operated in a new mode of operation where transport is dominated by Coulomb and Spin blockade effects. The latter are accompanied by large hysteresis loops and negative differential regions in the conductance plots. In this regime of operation, we developed a simple model of carrier transport through the QPC device based on a simple model of Coulomb blockade in the left portion of the QPC. Our simple model gives the correct order of magnitude for the separation of the conductance peaks observed as a function of the common gate signal applied to the two leftmost SGs. A more accurate model of space-charge effects throughout the entire QPC device is needed to fully understand the observed hysteresis curves. Suggestions for future work are outlined in the next chapter.
Chapter 5

Future Work

The work described in the previous chapters offers an alternative for creating and fine tuning the spin-polarization in QPCs by purely electrical means. This work opens a few new avenues for further research as described below.

5.1 All-electric spinvalve

By combining QPCs with a single QD, our approach offers a pathway to an all-electric spin valve. One such spin valve was recently fabricated in our lab and is shown in Fig. 5.1. It consists of two QPCs in series, separated by a channel (the QD) whose length is smaller than the spin coherence length [24, 84]. In Fig. 5.1, the left QPC is the “injector;” it puts spin-polarized electrons into the device’s channel. The right QPC, the “detector,” detects the spin state. The ON condition is defined when the spin orientations of the injector and detector are set parallel by fine tuning the QPC confining potentials with an appropriate asymmetric bias on their respective side gates. Similarly, the OFF condition is when the spin orientations of the injector and detector are antiparallel. The middle gates in Fig. 5.1 are used to perform spin precession in the device via voltage control of the LSOC in the central portion of the structure (as well as to control the size of the QD; see below). This would allow a gradual switching between the ON and OFF conditions described above.
5.2 Studying transport in Coulomb blockade regime

By controlling the dimensions of the central portion of the spin valve in Fig.5.1, i.e. by varying the bias on the middle gates, the device can operate in a regime of transport in which the active channel has a very low capacitance, and a very high junction resistance (i.e., resistance of the left and right QPCs). This can result in a Coulomb Blockade [85, 86] which permits the localization, and possibly, control of individual electrons within the channel. With an asymmetric bias on the gates of the two QPCs, their spin filtering action, when combined with Coulomb blockaded transport through the active channel, should lead to spin-blockaded transport through the spin valve. This would be a new type of blockade effect – LSOC Induced (LSOCI) – similar to spin blockade though it requires a single QD whereas conventional spin blockade requires two QDs in series. The blockade should arise partly from spin filtering effects in each QPC and, through fine tuning of the middle gates, from the lateral spin-orbit interaction in the quantum dot. This will affect the spin-dependent energy levels in the quantum dot. By varying the potential asymmetry on the QPCs, the amount of spin injection into, and extraction from, the dot can be varied over a wide range. This should lead to a highly versatile way to fine tune the spin-blockaded transport through the entire structure and should lead to a plethora of unexplored phenomena in this rapidly expanding field of research. Our investigations should shed some light on the rapidly developing field of spin transport phenomena in nanoscale devices. The appearance of Spin Blockade in these spin valve structures would be additional evidence of the spin filtering effect in the QPCs. Unfortunately, this effect cannot be modeled using NEGF approach shown in appendix I.
Fig 5.1: SEM image of a dual QPC spin valve recently fabricated in our lab. The length of the middle section is roughly 1 micron. Spin precession in the central portion of the spin valve is controlled by LSOC in that region. The central portion of the spin valve must be much smaller than the spin diffusion length in the semiconducting channel.

5.3 Investigating Wigner Crystallization in QPCs

Most studies of the spin-polarization phenomena in QPCs and QDs have focused on cases for which interaction-induced wave-function localization has been less prominent. These studies were performed in the regime of strong geometric confinement and electron densities that are relatively high. More recently, however, the regime of weak confinement and very low electron densities has become accessible experimentally with the important development of high mobility top gate heterostructures and QPCs [86, 87]. At low density, the interaction energy can dominate over the kinetic energy of the electron gas, and electrons are therefore expected to form an ordered state, a Wigner crystal, in order to minimize the total energy [43].
The phenomenon of Wigner crystallization is a new burgeoning emerging area in the field of spintronics. Recent conductance measurements indicate the incipient formation of a Wigner electron lattice and row coupling in such systems. The regime of shallow QPCs has been studied in detail by Hew et al. [85, 86]. They reported robust conductance plateaus at 2G₀ for which they suggested that Coulomb interactions may drive the conducting channel into a two-channel configuration, each channel with a conductance of G₀. On lowering the electron density in each channel the total conductance returns to G₀ because each channel should then spin polarize and contribute 0.5 G₀ to the conductance. Smith and coworkers have also studied electron transport in quasi-one-dimensional wires at relatively weak electrostatic confinement [87]. They have shown that Coulomb interaction distorts the ground state, leading to the bifurcation of the electronic system into two rows.

Several theoretical works predicted Wigner crystallization in low dimensional structures. For instance, Matveev et al. [88, 89] suggested that a Wigner crystal should evolve into a zigzag chain as a function of electron density. The transition to a zigzag pattern occurs when the electron separation becomes less than the characteristic length scale for one-dimensional confinement. Both quantum and classical calculations [89-95] predict that the zigzag will divide as the electron density increases or confinement weakens further, leading to the formation of a lattice of two or more rows of electrons.

In an effort to understand the experimental results of Hew [86] and Smith [87], Yakimenko et al. have studied the occurrence of local magnetization and the effects of electron localization in different models of quantum point contacts (QPCs) using a spin-relaxed density functional theory [96]. For the case of a soft confinement potential, the degree of localization is weak and there is only a partial electron localization in the middle of the QPC. In the pinch-off regime there is a
distinct charge accumulation at the QPC edges. With a strong confinement potential, low-electron density in the leads and top or implant gates favor electron localization.

Referring to the spin valve structure in Fig.5.1, the fine tuning the potential on its middle gates, the device could be operated close to threshold and an adjustment of the length of the middle section and the potential on the QPCs should possibly lead to an all electrical control of Wigner crystallization in these structures. Since phenomena such as Coulomb and Spin Blockades and Wigner Crystallization are many-body effects which cannot be modeled using a one-particle Hamiltonian approach, there is a need of a theoretical framework based on a multi-particle Fock space and steady-state rate equations [43, 85] to calculate the conductance of these spin valves, one that supplements the NEGF approach we have used in the past to model a single QPC. A thorough understanding of the Coulomb and Spin Blockades, and Wigner crystallization in all electric spin valves in the presence of LSOC would be a major milestone in the field of spintronics. A deep understanding of these non-linear effects in strongly correlated systems would contribute crucially toward future theoretical progress in diverse fields where far-out-of-equilibrium dynamics are involved.
List of Publications


Appendix I

Non-Equilibrium Green Function’s approach to spin transport

In chapter 4, we used NEGF results to demonstrate that the use of our new four gate QPC structure helps us realize a tunable all electric spin polarizer. Here, we briefly summarize the details of the NEGF model [32]. Within the NEGF approach, the Green function G(E) associated to the QPC is then a \((2N_x N_y \times 2N_x N_y)\) matrix (where \(N_x\) and \(N_y\) are the number of gridpoints along and perpendicular to the direction of current flow and the factor two is needed to distinguish the contributions from the two spin components. It is is given by explicitly by

\[
G(E) = (E I - H - \sum_S - \sum_D - \sum_{int})^{-1},
\]

(2)

Here \(\sum_S\) and \(\sum_D\) denote the self-energy terms that representing the coupling of the source and drain contacts and \(\sum_{int}\) is the electron-electron interaction self-energy [98]. The Hartree-Fock approximation was used following Lassl et al. [66] to include the effects of Coulomb e-e interaction in the QPC. In this approach, the interaction between two electrons located at \((x, y)\) and \((x', y')\) can also be modeled using the \(\delta\) potential as follows

\[
V_{int}(x, y; x', y') = \gamma \delta(x - x', y - y'),
\]

(3)

Here \(\gamma\) is the interaction strength equal to a few times of \(\hbar^2/2m\)

The interaction self-energy with spin \(\sigma\) is then given by
Here \( n_\sigma(x,y) \) is the density of electrons with spin \( -\sigma \). The interaction self-energy \( \Sigma^\sigma_{\text{int}}(x,y) \) is different for the two spin populations injected from the contacts. A spin-up electron encounters a barrier potential which is proportional to the density of spin-down electrons, and vice versa. This leads to a repulsive interaction between electrons with opposite spin directions. Any external source leading to an imbalance between the density of spin-up and spin-down electrons is amplified by the addition of the self-energy term, \( \Sigma^\sigma_{\text{int}}(x,y) \). In our case, it is the asymmetric LSOC, which causes the initial imbalance.

Once \( H \), \( \Sigma_s \) and \( \Sigma_D \) and \( \Sigma_{\text{int}} \) are known, the Green function (\( G \)) can be calculated from Eq. (2) and all the other quantities of interest can be found out from the following set of equations, i.e.:

The broadening matrices for the source and drain contacts

\[
\Gamma_s(E) = i(\Sigma_s - \Sigma_s^\dagger), \quad \Gamma_D(E) = i(\Sigma_D - \Sigma_D^\dagger).
\]  

(5)

The spectral functions of the source and drain contacts

\[
A_s(E) = GT_s(E)G_s^\dagger, \quad A_D(E) = GT_D(E)G_D^\dagger.
\]  

(6)

The density matrix

\[
\rho = \int_{-\infty}^{\infty} \frac{A_s(E)f_s(E) + A_D(E)f_D(E)}{2\pi} dE.
\]  

(7)

Where \( f_s \) and \( f_D \) are the Fermi-Dirac distributions in the source and drain contacts, respectively;
Using the transmission coefficient

\[ T(E) = \text{Trace} \left[ \Gamma_s G \Gamma_s G^\dagger \right] \] (8)

the current through the QPC under the assumption of ballistic transport

\[ I = \frac{q}{h} \int_{-\infty}^{\infty} T(E) \left[ f_s(E) - f_{d}(E) \right] dE \cdot \] (9)

Based on Eqns.(5-9), the density matrix \( \rho \) can be calculated from the Green function matrix \( G \). The diagonal elements of the density matrix determine the spin-up density \( n_\uparrow \) and spin-down density \( n_\downarrow \) and hence the interaction self-energy \( \sum_{\text{int}} \) from Eq. (4). Since the interaction self-energy depends on the Green function matrix and vice-versa, an iterative procedure is required to obtain the final conductance results.
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