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Student's name: Adam T Zocco

This work and its defense approved by:

Committee chair: Andrew Steckl, Ph.D.

Committee member: Joshua A Hagen, Ph.D

Committee member: Jason Heikenfeld, Ph.D.

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Pentacene-based Organic Thin-film
Transistors on Paper

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Adam T. Zocco

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Committee Chair: Andrew J. Steckl, Ph.D.
Abstract

Pentacene-based organic thin film transistors (OTFTs) have been fabricated on several types of flexible substrates: standard photo paper, ultra-smooth specialty paper and ultra-thin (100 µm) flexible glass. For comparison OTFTs were also fabricated on liquid crystal display (LCD) quality glass rigid substrates. The transistors were fabricated entirely through dry-step processing. The field-effect mobility of OTFTs on photo paper reached values (0.09 cm²/Vs) close to that on LCD glass (0.11 cm²/Vs). Transconductance values for OTFTs on photo paper and LCD glass were also fairly close, with values of 0.52 and 0.82 mS/m, respectively. The comparable characteristics between OTFTs fabricated on widely available, low cost paper and high quality expensive LCD glass indicate the potential importance of cellulose-based electronic devices.
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To My Family...
1. Introduction

The transistor is a fundamental electrical component, endlessly adapting to electronic needs in order to continue next-level technology. The most extensively known form of transistor is fabricated using vast quantities of single crystal silicon. For now, single crystal silicon transistors remain the standard. However, organic based electronics and “green” energy materials are increasingly becoming more common among research and commercial areas. Reasons behind this increase can be attributed to several need-based motives: A) Lowering process and material costs; B) reducing environmental impact; C) maintaining biocompatibility with living life forms. Organic electronics that use semiconductors consisting of organic small molecules or polymers are finding an increasing range of device applications [1-3], including organic light emitting diodes (OLED), organic photovoltaic (OPV) devices, and organic thin-film transistors (OTFT).

To innovatively progress OTFTs, paper substrates are introduced, to completely remove the silicon elements. Most organic electronics are fabricated on rigid glass or silicon substrates. Although, in order to take advantage of the flexible nature of organic materials and of low cost roll-to-roll technology this requires fabrication on flexible substrates. In this context, development of organic electronics on paper is very attractive as it could be extrapolated to the existing high efficiency printing press technology.

Paper materials, in addition to organic thin-film transistors, open new developments into low cost, biologically compatible, and flexible electronic devices[4, 5]. Paper with electronic devices gives rise to Paper Electronics and facilitates organic materials for efficient electronic applications. Considerable progress is being made in the area of
paper electronics with many types of devices being reported[6, 7]. Cellulose based paper substrates were implemented as an electronic substrate as early as 1969 [8] with most advancement occurring in the past decade largely due to technology improvements in thin-film deposition and organic materials. A few notable examples of OTFTs on paper include the report from the Berggren group [9] in 2002 of OTFTs as electrochemical pixels on paper substrates. In 2004, Kim et al. [10] reported OTFT arrays on paper using poly(3-hexylthiophene) as the semiconductor layer and Eder et al. [11] reported paper-based ring oscillators. More recently, the Klauk group [12] reported a novel approach to organics on paper by integration of thin-film transistor circuits on banknotes. It should be pointed out that significant development of paper electronics has also occurred using thin-film *inorganic* semiconductors. Several groups have developed oxide-based semiconductor (such as indium gallium zinc oxide – IGZO) TFTs on paper substrates [8, 13-15].

The objective of the following thesis centralizes around the pursuit of electronics on cellulose-based paper substrates. Particular focus is in development of organic pentacene OTFT fabrication, applying techniques that eliminate liquid elements. The emphasis is to compare the performance of OTFTs on paper with that of identical devices fabricated on standard liquid crystal display (LCD) rigid glass (Corning 1737) and on ultra-thin (100µm) flexible glass (Corning Willow glass). Two paper materials were investigated as OTFT substrates: Hewitt Packard commercially available photo paper (HP), and a specialty ultra-smooth paper (Sappi). This work has evolved from paper substrates used in electro-wetting devices and liqui-FETs [16].
1.2. OTFT background

Similar to field-effect transistor (FET) principles, basic thin-film transistors use three electrodes, usually metallic, and an insulator with an organic semiconducting material acting as the active region. Paul Weimer in the 1960’s [17] showed a useful application of inorganic thin-film transistors and paved the way for the novel development of such devices. The realization of organic semiconductors became practical in the early 1980’s when field effect measurements were done on organic dye films [18]. Thermal evaporation of organic materials also gave rise to a convenient deposition of semiconducting crystalline layers in thin-film transistors. Many different methods can be implemented to obtain these thin layers, especially involving organic thin-film transistors.

1.3. Device Configuration and Operation

As previously mentioned thin-film transistors consist of a substrate, several electrical contacts, an insulator, and a semiconductor. Configuration of thin-film transistors is generally completed in two ways, a bottom-gate or top-gate structure. The bottom-gate, staggered TFT configuration used here, is given in Fig 1. This structure is necessary for field-effect behavior of the insulating layer, creating charge attraction. Transistors in both a bottom and top gate type structure employ three electrode terminals: gate, drain, and source. Depending on the semiconductor being p-type or n-type, a respective negative or positive gate voltage generates an electrical field attracting either holes or electrons to the surface of the dielectric-semiconductor interface. This produces a conducting channel along the interface and regulated by proper biasing of the source-
drain voltage. Voltages applied to the terminals move the charges by biasing either a negative (p-type) or positive (n-type) voltage at the gate and drain. Modulation of the channel current by the source and drain allows the transistor device to behave as a switch and thus be turned on or off. This thesis will focus on p-type pentacene thin-film transistors in a bottom-gate, staggered structure.

![Diagram of a thin-film transistor in a bottom-up (top-contact) staggered configuration.](image)

**Figure 1:** Structure of a thin-film transistor in a bottom-up (top-contact) staggered configuration.

### 1.3.1 Operating Modes

In general, the two key parameters for both inorganic and organic FET operation are the transconductance and the field-effect mobility, even if the actual transport mechanisms are different. FET operation models are useful for extraction of OTFT
electrical parameters. The equations below are derived in literature [19-21] and
calculated for OTFT devices in this work. At low values of drain-source voltage \( V_{DS} \),
the FET drain-source current \( I_{DS} \) increases monotonically with \( V_{DS} \). This is the linear
regime

\[
I_{DS,\text{lin}} = \frac{\mu_{\text{lin}}C_i}{L} (V_{GS} - V_T - \frac{1}{2} V_{DS}) V_{DS}, \quad |V_{DS}| < |V_{GS} - V_{th}| \quad \text{(linear regime)} \tag{1}
\]

where \( V_{GS} \) is the gate-source voltage, \( V_T \) is the threshold value of \( V_{GS} \) for observable \( I_{DS} \)
flow, \( C_i \) is the insulator capacitance per unit area, and \( W/L \) is the transistor channel aspect
ratio. The \( I_{DS} \) saturation regime occurs when \( V_{DS} \) is larger than \( V_{GS} \) minus \( V_T \)

\[
I_{DS,\text{sat}} = \frac{\mu_{\text{sat}}C_iW}{2L} (V_{GS} - V_T)^2, \quad |V_{DS}| > |V_{GS} - V_{th}| \quad \text{(saturation regime).} \tag{2}
\]

\( \mu_{\text{lin}} \) and \( \mu_{\text{sat}} \) are the linear and saturated regime mobilities. Following the notation of
Klauk and Wang and Cheng, the transconductance \( (g_m) \), which describes drain
current modulation through change in gate voltage, is given by

\[
g_m = \frac{\partial I_{DS}}{\partial V_{GS}} \tag{3}
\]

In the linear and saturation regimes, the transconductance varies linearly with voltage
(either \( V_{DS} \) or \( V_{GS} \)) and the corresponding value of mobility

\[
g_{m,\text{lin}} = \frac{\mu_{\text{lin}}C_iW}{L} V_{DS}, \quad |V_{DS}| < |V_{GS} - V_{th}| \quad \text{(linear regime)} \tag{4}
\]

\[
g_{m,\text{sat}} = \frac{\mu_{\text{sat}}C_iW}{L} (V_{GS} - V_T), \quad |V_{DS}| > |V_{GS} - V_{th}| > 0 \quad \text{(saturation regime)} \tag{5}
\]

The mobility in the linear and saturation regimes is given by [20].
\[ \mu_{lin} = \frac{L}{c_V D S W} \left( \frac{\partial I_{DS}}{\partial V_{GS}} \right), |V_{DS}| < |V_{GS} - V_{th}| \ (linear \ regime) \quad (6) \]

\[ \mu_{sat} = \frac{2W}{c_V l_e} \left( \frac{\partial \sqrt{I_S}}{\partial V_{GS}} \right)^2, |V_{DS}| > |V_{GS} - V_{th}| > 0 \ (saturation \ regime) \quad (7) \]

The OTFTs threshold voltage \( V_T \) can be obtained from eq. (2) by extrapolating a linear fit to the steepest slope of the \( I_D \) vs \( V_{GS} \) curve. Finally, another important OTFT characteristic is the ratio of maximum to minimum drain-source current through the device, the so-called On/Off ratio.

**1.3.2. Pentacene Semiconductor**

The organic small molecule pentacene \((C_{22}H_{14})\) pictured in Fig 2. is a polycyclic aromatic hydrocarbon in a \( \pi \)-conjugated system. It is composed of five linear benzene rings with alternating single and double carbon-carbon bonds that enable the molecule to have semiconductor properties. Delocalization of a valence electron caused by the conjugated system allows charge transport to occur linearly across the molecule [20]. When materializing an organic semiconductor layer by thermal sublimation, the molecules form onto the surface with weak intermolecular Van Der Waal forces [22]. Pentacene molecules in particular form polycrystalline structures where grain boundary sites don’t strongly impact carrier transport. This is partially due to the 001 lattice overlap of the HOMO and LUMO frontier orbitals [23].
Figure 2: Structure of an individual pentacene molecule of five linear benzene rings

Pentacene is widely studied as an organic semiconductor due to its fairly large carrier mobility. Carrier mobilities have reached values greater than values of $>10\text{cm}^2/\text{Vs}$ on alumina dielectrics [24, 25]. This information led to the development of pentacene-based OTFT devices on paper and glass substrates.

1.3.3. Dielectric Properties

A 2005 review by Facchetti et al. [26] details the advancement of OTFT in the area of gate dielectrics. The dielectric material can determine both growth characteristics of the organic deposited and the electrical properties of a given device. The dielectric affinity can also determine the performance characteristics of OTFTs developed with polymer dielectrics [27].

1.3.4. Ohmic Contact

The contact between the metal and organic material plays an important role in device performance. That is, the interface between the metal-organic layers and the contact resistance is of great importance in OTFT operation [28, 29]. Usually, a metal with a higher work function is chosen to generate sufficient charge transport in p-type organic semiconductors [30]. Contact barrier height has been shown to influence field-
effect behavior [31]. Lowering the contact resistance can improve the mobility of charge carriers which results in larger field-effect mobilities [32].

### 1.4. Device Fabrication

The pictures of completed OTFT arrays are pictured in Fig 3a-d. Fig 3a. shows devices on HP Advanced photo paper, Fig 3b. devices on Sappi, Fig 3c. on Corning 1737 rigid glass, and in Fig 3d. OTFT devices on Corning Willow glass.

![OTFT arrays on different substrates](image)

**Figure 3:** Completed thin-film transistor arrays on different substrates; (a) OTFT devices on HP advanced photo paper; (b) OTFT devices on Sappi specialty paper being flexed; (c) A set of OTFT devices on Corning 1737 rigid glass; (d) Flexible Corning willow glass OTFT devices being flexed.
1.4.1. General Methods

Fabrication employed for development of OTFTs consisted of a series of steps and no conventional photolithography was utilized. Instead thin-films in all dry-process fabrication method were implemented through shadow masking. The process as an overall method is illustrated in Fig 4a-d. was initiated by sputtering of the a copper gate mask through a laser milled polyimide shadow mask, shown in Fig 4a. Subsequently, in Fig 4b. the dielectric of Parylene C (PC) deposited in a Specialty Coating Systems Labcoater 2. Sublimation of pentacene in a house-made evaporation chamber using a separate mask in Fig 4c. was deposited directly on the PC surface. The following final step in Fig 4d. was thermal evaporation of gold in an Edwards Coating System E306A. Actual thicknesses were verified with a Tencor P10 surface profiler. The final dimensions of the electrode for the gate and source-drain masks were chosen after several iterations of testing with Kapton tape, while simultaneously minimizing alignment issues during masking. Appendix 1 and 2 describes more detail of early device fabrication and electrical characterization.
Figure 4: Method of fabrication steps for dry-process generation of OTFT devices; (a) Copper being sputter deposited through a polyimide shadow mask to create the gate layer; (b) Parylene C monomer chemically vapor deposited on the gate layer as the dielectric material; (c) Pentacene thermally evaporated through a metallic mask along the gate electrode; (d) Source and drain gold electrodes being thermally evaporated through a high resolution metallic shadow mask.

1.4.2. Detailed Method

Fabrication was carried out on pre-cut Corning 1737 LCD (2”×2”) and Corning Willow flexible (1.5”×1”) glass substrates, along with unmodified cellulose based photo paper (HP) and specialty paper (Sappi). As previously mentioned, devices in a bottom-up (top-contact) staggered thin-film transistor structure were configured as illustrated in Fig 5.
Figure 5: Thin-film structure in a bottom-up staggard structure of the completed devices, with given thicknesses, on paper and glass substrates.

The shadow masks utilized for this approach are shown in Fig. 6a-c. In order to minimize variation caused by substrate flexibility, scissor cut paper substrates (1.5”×1.5”) were fixed to a clean glass substrate with double-sided Kapton™ tape.
Figure 6: Pictures of the shadow masked used in the depositions of thin-film materials. (a) Polyimide gate shadow mask; (b) Metallic shadow mask with two rows of 8 openings for pentacene deposition; (c) Milled metallic shadow mask with W:L dimensions of 500µm and 50µm, respectively. (Inset) shows a 50x magnification of a single transistor source-drain channel region.

1.4.2.1. Gate Deposition

Copper electrodes were sputtered through the polyimide shadow mask in Fig 6a. Conditions for copper gates were as follows. Forward power of 175W and reflected power of 23W. A base pressure of 1x10⁻⁷ Torr was achieved before argon gas introduction. Argon plasma was produced with a pressure of 4 microns of mercury.
Typical thickness of copper was ~145nm. The contact pads were then masked with a PDMS stamp before the subsequent deposition of the dielectric film.

1.4.2.2. Parylene Dielectric Deposition

Parylene C (PC) was chosen as the insulator layer for several reasons: it is deposited by an easy chemical vapor dry process, it has good mechanical flexibility, and a dielectric constant \((k>3)\) that is fairly high for vapor-processed polymer dielectrics. Manufacturer specifications give a dielectric constant \((k)\) of 3.1 for PC. This is relatively close to that of typical silicon oxide \(k\) values of 3.9. Moreover, PC is a room temperature, physical process that is fairly conformal across depositions. Importantly since the substrate is heated, PC can withstand short-term temperatures of 100°C. Other properties of PC such as low permeability of moisture, resistance to corrosive gases, and biocompatibility, make it relevant for this application. Wang [33] demonstrated OTFT devices incorporating PC, with mobilities of up to 0.75cm²/Vs.

PC dimer (0.38g) was vapor deposited in a Specialty Coatings System PDS 2010 with a thickness of ~340nm. A furnace and vaporizor temperature of 690°C and 175°C, respectively, were reached at a vacuum pressure of 11mTorr. After PC, the PDMS stamps were carefully removed from the substrate.

1.4.2.3. Pentacene Deposition

A custom, in-house pentacene evaporation system with a crucible shutter was configured for thin film deposition of the semiconductor layer pentacene. The system is equipped with a Pheiffer Hi-Cube turbo molecular pump delivering a consistent base pressure of values in the mid 10⁻⁷ Torr. The shadow mask in Fig 6b. was placed with a
single row of 8 openings along the gate electrode. Samples faced downward, perpendicularly to the crucible z-axis. The crucible cell was slowly increased over a 2 hour period to 140°C by control of a Eurotherm and the shutter was opened after 2 minutes to stabilize. Approximately 47 nm of pentacene (99.995% purity, Sigma Aldrich) was thermally evaporated at a rate of ~0.5-0.9 Å/s directly onto the PC surface through the shadow mask, the shutter closed, and temperatures were allowed to cool to room temperature. Substrate temperature during pentacene deposition was elevated slightly to a stable level in the 31-35°C range. A increase in substrate temperature is reported to lead to better morphological growth and higher molecular ordering [19, 34, 35].

1.4.2.4. Source-Drain Gold Deposition

Finalizing the devices, source and drain patterns were formed by thermal evaporation of 90 nm of gold (99.99%, ESPI) onto the pentacene layer through a second mechanically milled metallic shadow mask pictured in Fig 6c. The transistor had device length ($L$) - width ($W$) dimensions of 50µm and 500µm, respectively. Evaporation temperatures were successfully reached after 20 minutes (~1200°C) at 15 Amps, while maintaining a vacuum pressure in the $10^{-7}$ Torr range (penning gauge). Single tungsten wire baskets coated in a thick layer of aluminum oxide with 4mm inner diameters were filled with 0.6g of several 1/8” pellets. ~100 nm was easily achieved over a 5 minute deposition period as measured by a crystal oscillator with a tooling factor of 0.67 and a density value of 19.30 g/cm$^3$. 


2. Device Characterization

Two initial requirements become immediately apparent when developing OTFTs on paper. The first requirement is a completely smooth surface morphology, allowing homogeneous material deposition and high quality films. The second being thermal capabilities of the paper substrate for compatibility with deposition techniques.

Paper processing is advancing rapidly through improvements of surface morphology and material compatibility permitting transistor development. Common forms of paper are generally composed of interwoven cellulose fiber strands and vary extensively in quality, depending on its purpose. Naturally occurring wood fibers of plant matter passes through several methods of extraction and forming to ultimately create a practical substrate [7]. Much of the time, paper has a rough surface morphology which tends to make it difficult for fabricating thin-films. Additives can be incorporated into the matrix of fibers or applied as an added layer to smooth the main application surface. A familiar example of additives benefiting the refinement of the surface finish, is in photo paper. Still, heat and wet processing steps during device fabrication may have negative effects on paper’s capabilities regardless of surface roughness.

2.1. Thermogravimetric Analysis

Understanding thermal-induced decomposition was of initial importance due to the possibility of paper becoming exposed to maximum temperatures of 100°C. Thermogravimetric Analysis (TGA) was performed on various cellulose-based paper materials, providing an indication of temperature thresholds. A NETZSCH STA 409
PC/PG was used for analyzing samples of Watman P8 filter, standard copy, and three specialty papers composed of cellulose and added constituents.

Samples were hole punched and placed unaltered into clean aluminum weigh pans with metal tweezers. The pans were then heated from 30 to 500°C at 10°C/min in a high purity argon atmosphere. Mass change percentage was simultaneously measured throughout heating. As shown in Fig 7, the onset of cellulose decomposition temperature of around ~250°C is given for each sample, after preliminary moisture is removed (~40°C). This corresponds to a comparative study by Soares et al. [36].

Figure 7: Thermogravimetric analysis of 5 unique papers with closely matching decomposition at ~250°C.
2.2. SEM Analysis of Paper and Pentacene

The papers surface and cross-section structures were analyzed using Scanning Electron Microscopy (SEM) with an Evex Mini-SEM SX-3000. Paper substrates chosen for OTFT fabrication were prepared in surface and cross sectional formats. Samples were placed onto the vacuum stage in Fig 8a. after mounting to a sample stub. The preparation began with a clean 90° mounting stub. Double-sided carbon tape was applied to the 90° portion of the stub, both horizontally and vertically. Surface samples of 1mm x 1mm sections for each paper were scissor cut, carefully placed along the horizontal plane of the carbon tape, gloss side up. Cross section samples required higher precision and delicately press cut with a fine surgeons scalpel. Samples were placed vertically and eye aligned neatly along the top horizontal edge. Each individual sample electrically contacted the carbon tape by silver paste. Completing preparation (Fig 8b.), gold was DC sputtered twice, 25 seconds vertically, then 20 seconds horizontally. Sputtering twice helped minimize well-known charging effects of paper materials.

Figure 8: (a) SEM mounting stage with x-y axis and rotation control; (b) Prepared paper samples on a 90° mounting stub.
The resulting SEM images are pictured in Fig 9a-d. Cross-sectional images in Fig. 9a of Sappi and Fig 9b. of HP reveal a dense calendared bulk with thinner top surface coatings. The surface coatings smooth the underlying bulk cellulose and contribute to higher quality thin-film deposition. Both substrates are ~200µm in thickness. Fig 9c and 9d. both reveal the smooth topology of the surface coatings of the Sappi and HP paper substrates, respectively.

**Figure 9:** SEM images of Sappi paper and HP Advanced photo paper. (a) cross-section images showing the cellulose base material and thick polymer surface coating of Sappi; (b) Cross section of photo paper with a thicker top surface coating; (c) Surface image of Sappi with nearly featureless smooth surface; (d) Top surface image of photo paper with a smooth surface and minor imperfections.
Pentacene films were viewed through SEM to identify clues of film quality and structural properties. The microphotographs in Fig 10a-c. reveal structure rather similar to AFM measurements. There is faint patterning of the film, observing submicron crystallites which the Evex SEM has difficulty focusing. In Fig 10a, a transistor channel region of an operating device has a smooth, nearly featureless surface. The inset of Fig 10a. is the source-drain channel region that was analyzed. Images of Fig 10b and 10c. are pentacene films deposited on Sappi and HP paper with a ~340nm PC layer, respectively. There is patterning seen in Fig 10b, that resembles a grain-like appearance on Sappi. HP has a surface with a better appearance of features, likely the top surface of pentacene grains as shown in Fig 10c.

Figure 10: Scanning Electron Microscopy images of pentacene films. (a) SEM of pentacene surface in channel region; inset – SEM of active area of transistor showing Au source and drain electrodes and pentacene region; (b) Sappi paper with Parylene C showing the pentacene film structure of the surface of grains; (c) Image of photo paper with Parylene C deposited with pentacene, showing patterning of pentacene structure.

2.3. Atomic Force Microscopy

One of the key characteristics of the substrates is the condition (morphology and roughness - Ra) of the surface on which the OTFTs will be fabricated. The bare surfaces
and topology of the glass and paper substrates were analyzed with an Veeco Dimension 3100 Atomic Force Microscope in Tapping Mode. Glass samples were cleaned by an acetone, methanol, deionized water rinse and a 20 minute bake at 150°C. To analyze paper surfaces, a 2” round silicon wafer was mounted with a 50mm×50mm scissor cut paper piece and the four edges taped.

![AFM images of substrates](image)

**Figure 11**: Atomic Force Microscopy images of substrate surfaces. (a) HP photo paper surface morphology with a ~11.1nm surface roughness; (b) Sappi specialty paper surface topology having a surface roughness of ~2nm; (c) The ultra-smooth surface of Corning 1737 LCD glass with a ~0.4nm roughness; (d) Corning Willow glass with a ultra-smooth surface roughness of ~0.4nm.

*Fig. 11* shows 10×10μm image scans of the rigid glass, flexible glass, specialty paper, and photo paper materials. The surfaces of the rigid and flexible glass in *Fig 11a*
and 11b. are ultrasmooth with roughness values ~0.4nm for both substrates. The images in Fig. 11a and 11b covering areas of the Sappi and HP papers yielded surface roughness values of ~2 and ~11.1nm, respectively.

To gain insight in pentacene morphology of the functional transistors, AFM was performed on pentacene thin-films. Pentacene morphologies have been widely studied to understand effects on performance in transistors. A study by Bouchoms et al. [37] indicated the presence of two crystalline phases: a thin-film phase and a bulk phase that is triclinic in nature. Device performance is considered to decrease once the film becomes greater than a critical thickness (~100 nm for room temperature deposition) and enters the bulk phase. Nucleation of the films is also an significant aspect [38] of performance considerations as grain boundaries can be unfavorable to device performance [39]. Many conditions can affect the growth of pentacene layers. Conditions such as temperature, dielectric medium, deposition rate, and purity during deposition of pentacene, are fundamentally related to growth morphologies.

PC and pentacene surface analysis was performed on rigid glass, Sappi, and HP paper substrates to further investigate pentacene morphologies of the deposited films. Fig 12a-c AFM scans are of each substrate and PC. As expected, PC on rigid glass shows exceptionally smooth surfaces of ~2.9nm in Fig 12a. In Fig 12b. Sappi also revealed a smooth surface of ~4.1nm. The slightly more rough surface of PC on HP of ~12.3 are given in Fig 12c. The Figures 12d-f are the same substrate and PC structure with addition to pentacene.
Figure 12: Atomic Force Microscope Images of LCD glass, specialty paper, and photopaper with deposited films. (a) Corning 1737 LCD glass with Parylene C having a surface roughness of ~2.9nm; (b) Sappi specialty paper with Parylene C also having a very smooth surface of ~4.1nm; (c) A surface roughness of ~12.3nm for Hewitt Packard photo paper with Parylene C; (d) Pentacene grain morphology of glass with Parylene C with roughness's of ~7.8nm; (e) Sappi specialty paper with Parylene C showing pentacene grain morphology, yielding a roughness of ~8.5nm; (f) Hewitt Packard photo paper pentacene grain morphology on Parylene C providing a roughness of ~13.2nm.

From the AFM images of ~47nm of pentacene, a high density of submicron grains are apparent on the surface of PC layers (~100-200 nm lateral dimensions). Fig 12d. discovers a uniform and homogeneous film of pentacene grains on a LCD glass substrate with a surface roughness of ~7.8nm. Fig 12e. on Sappi finds the pentacene film closely resembling that of glass, with a roughness of ~8.5nm. Observed in Fig 12f. there appears to be more nucleation of the pentacene film grains on HP and having a roughness of ~13.2nm. The very small grain size may be an indicator to the transistors deficiency in higher mobility values and performance characteristics.
3. Electrical Characterization

Electrical parameters were extracted under room temperature measurements with an HP4140B pA meter with custom LabView software and an Alessi 3200 probe station in a semi-dark box at normal atmosphere. A customized LabView program controlled the voltage sweeps of the drain to source at 0.5V increments, while simultaneously measuring drain to source current on a HP 4140B meter with a three tungsten needle probe system. A DC power supply was manually adjusted for each gate voltage and drain to source voltages were applied from +16V to -60V.

3.1. Capacitance Measurement

Three separate capacitors were electrically measured for gate capacitance with average of 519pF of the three devices (2.25mm×2.25mm). The dielectric constant could then be calculated by eq. 8.

\[ k = \frac{C \cdot t}{\varepsilon_0 \cdot A} \]  \hspace{1cm} (8)

\( C \) is the capacitance (519pF), \( t \) is the dielectric thickness, \( \varepsilon_0 \) is the permittivity of \( 8.85 \times 10^{-12} \), and \( A \) is the area of the active capacitor region. Applying the variables in eq 8, \( k \) is then calculated.

\[ k = \frac{519pF \cdot 340nm}{8.85 \times 10^{-12} N/m^2 \cdot (2.25)^2 mm} = 3.94 \]
The calculated dielectric constant of 3.9 is fairly high for PC, though may be an attribute of averaging across only three capacitors. The gate capacitance per unit area was calculated using the eq 9.

\[ C_i = \frac{\varepsilon_o \varepsilon_r}{t} \]  

where, \( C_i \) is the gate capacitance per unit area, \( \varepsilon_o \) is the permittivity of \( 8.85 \times 10^{-12} \) N/m\(^2\), \( \varepsilon_r \) is the dielectric constant, and \( t \) is the thickness of the dielectric layer (340nm). Calculating the gate capacitance in centimeters yields,

\[ C_i = \frac{8.85 \times 10^{-12} N/m^2 \cdot 3.94}{340 \text{nm}} = 10.2 \text{ nF/cm}^2 \]

The calculated gate capacitance of 10.2nF/cm\(^2\) is then used in the formula for mobility calculations.

### 3.2. I-V Characteristics

Current-voltage (I-V) characteristics are shown in Fig. 13 for OTFTs fabricated on paper and glass substrates. The I-V plots display the drain-to-source current (\( I_{DS} \)) versus drain-source voltage (\( V_{DS} \)) for a series of fixed gate-to-source voltage (\( V_{GS} \)) values. In all cases, the OTFT characteristics follow traditional FET behavior, namely a linear regime at small values of \( V_{DS} \) (compared to \( V_{GS} \), see eq. 1) followed by a saturated regime where \( V_{DS} \) is comparable to or larger than \( V_{GS} \) (see eq. 2). The I-V characteristics indicate comparable saturation drain-source currents at the various gate voltage values for OTFTs on all four substrates. As expected from conventional FET operation, \( V_{GS} \) strongly affects the current flow through the OTFT. This is illustrated in the transfer
characteristics shown in Fig. 14, where the log of $I_{DS}$ is plotted versus $V_{GS}$ at a fixed $V_{DS}$ value of -55V for OTFTs on all four substrates.

**Figure 13**: Current-voltage operating characteristics of OTFTs on (a) Corning 1737 rigid glass; (b) Corning Willow flexible glass; (c) Hewitt Packard commercial photo paper; (d) Sappi specialty paper.
Figure 14: Effect of gate-to-source voltage for OTFTs on the four substrates: (a) drain-to-source current plotted again gate-to-source voltage, showing similar trends as gate voltage is increased.

As expected, all transfer characteristics display a subthreshold regime between the switch-on voltage ($V_{SO}$ – the $V_{GS}$ voltage at which current is first observable) and the threshold voltage. The OTFT on flexible glass has a value of $V_{SO}$ nearly equal to zero, while the OTFTs on the other three substrates have values of $V_{SO}$ larger than +15V. The values of $V_T$ are in the 20 to 30V range for all four OTFT. More accurate $V_T$ values were obtained from $\sqrt{I_{DS}}$ vs $V_{GS}$ curves shown in Fig 15 plotted in the saturation regime (see eq. 2) at $V_{DS}=-55V$. 
Figure 15: Square-root of drain-source current plotted against gate-to-source voltage; Threshold values ($V_T$) is extracted by a linear fit to the curves for each substrate.

The field effect mobility in the saturation regime was obtained using eq. 7. The mobility versus $V_{GS}$ is shown in Fig. 16, at a value of $V_{DS} = -55V$, for OTFTs on all four substrates. Not unexpectedly, the highest saturation mobility is obtained on the LCD glass substrate, with a value of 0.11 cm²/Vs at $V_{GS} = -55V$. Interestingly, the OTFT on HP exhibits the 2nd highest mobility, with a value of 0.09 cm²/Vs. The OTFTs on flexible glass and on Sappi paper yield maximum mobility values of 0.07 and 0.05 cm²/Vs, respectively.
Table 1 lists the key transistor electrical characteristics of the OTFTs on the four substrates in order of the mobility value. The transconductance values in the saturation regime ($V_{DS} = -55V$) calculated using eq. 5 follow the same trend as the mobility, with values of 0.83mS/m for the OTFT on LCD glass and 0.52mS/m on the HP paper OTFT.

The drain current On/Off ratio of the OTFTs was strongly affected by their respective sub-threshold current. The OTFTs on LCD glass and HP, which exhibited significant sub-threshold current, produced On/Off ratios of $10^5$ and $3.75 \times 10^5$, respectively. The OTFT on Sappi paper, which had reduced sub-threshold current, yielded On/Off ratios of $10^6$, while the OTFT on flexible glass which showed the least amount of sub-threshold current exhibited the highest On/Off ratio of $3 \times 10^6$. For comparison, pentacene OTFTs
fabricated on paper by a wet process (photolithography and wet etching) were reported [11] with similar properties, namely a saturated mobility of 0.2 cm$^2$/Vs and an On/Off ratio of $10^6$.

<table>
<thead>
<tr>
<th>Substrate</th>
<th>Mobility (cm$^2$/Vs)</th>
<th>Transconductance (mS/m)</th>
<th>On/Off Current</th>
<th>$V_{SO}$ (V)</th>
<th>$V_T$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LCD Glass</td>
<td>0.11</td>
<td>0.82</td>
<td>$10^5$</td>
<td>16</td>
<td>-20</td>
</tr>
<tr>
<td>HP Paper</td>
<td>0.09</td>
<td>0.52</td>
<td>$10^5$</td>
<td>16</td>
<td>-28</td>
</tr>
<tr>
<td>Flexible Glass</td>
<td>0.07</td>
<td>0.48</td>
<td>$10^6$</td>
<td>0.5</td>
<td>-23</td>
</tr>
<tr>
<td>Sappi Paper</td>
<td>0.05</td>
<td>0.30</td>
<td>$10^6$</td>
<td>16</td>
<td>-26</td>
</tr>
</tbody>
</table>

Table 1: Electrical properties of OTFTs on the two paper substrates and two glass substrates: saturation mobility and Transconductance (at $V_{DS} = -55V$), On/off drain current ration, switch-on voltage and threshold voltage.

It must be pointed out that the results presented here are obtained from a specific set of devices. While the trends between devices on different substrates are reproducible, parameter values do vary. Therefore, one should interpret these results as indicating that OTFTs fabricated on flexible paper substrates can produce characteristics comparable to OTFTs on conventional and flexible glass.
4. Conclusion

Through utilization of a liquid-free, shadow mask method, OTFT arrays were fabricated on multiple substrates of rigid LCD glass, flexible glass, Sappi specialty paper, and HP commercial photo paper. Electrical properties (mobility, transconductance, On/Off current ratio) of the OTFT on HP paper are comparable to those on rigid (LCD) glass. The combination of low cost commercial paper substrate, a simple dry process and useful electrical characteristics indicate that this represents a promising approach for paper electronics.

4.1. Future Work

There is a significant need for future experiments to be performed on paper devices produced in this work.

4.1.1. Pentacene Morphologies and Transistor Performance

A higher degree of understanding is necessary on the growth characteristics of pentacene films and their effect on transistor performance. This includes further development on Parylene C as well as other polymeric dielectric media [40]. It is suggested to analyze pentacene films at larger substrate temperatures, angling of the stage during pentacene growth, and slower deposition. Along with this, self-assembled monolayers (SAM) can be added to dielectric surfaces and/or at the metal-organic interface. The reader is encouraged to begin with reference to Chaudhury’s report on SAM layers on polymer surfaces [41] although there are many reports to consider such as Kim et al.’s [42] Advance Functional Materials report. Also, the use of High- $k$
dielectrics of oxides or polymers could help improve properties of the OTFTs. Modification of the oxide layers through implementation of polymers may also be an area of study [43].

4.1.2. Masking

Another aspect of future work that may impact device performance is improving upon masking methods. Higher resolution stencil masks with smaller features can be created [44, 45] and could advance the function of OTFT.

References:


Appendix 1-Masking and Systems

2.1.1 Mask Development

Acquired through early literature studies on OTFT applications [1-3], the dry-step fabrication method was instigated for the gate, pentacene and source-drain layers. The apprehension with flexible polyimide masks is their ability to lay flat on the substrate surface. An air gap will usually exist between the two surfaces. In the case of the gate layer, polyimide mask edge resolutions were not of great concern and when appropriate, the mask was taped with Kapton as flat as possible. Source-drain electrode tolerances required a higher degree of precision and rigid metallic masks were fabricated instead of polyimide. The interface between the metal-organic layers is of great importance in OTFT operation[4, 5].

The first-generations of gate masks were comprised of kapton tape or film and varied in dimension due to the nature of experimentation. Examples of gate masking is pictured in Fig A1-17.

![Figure A1-17: Taped masking for gate electrodes; (a) large gate pattern; (b) smaller gate dimensions.](image-url)
The gate masking methods needed to be taped along the top and bottom edges of the electrode in order for electrical contact to be made during the testing phase. Normally, Kapton tape was used for this purpose but needed careful removal after pentacene depositions. This posed an issue since removing the tape also removed the metallic layer. Copper, aluminum, and gold do not adhere well to the paper or glass surfaces and thus is easily removed.

To create the gate shadow mask of polyimide film a Universal Laser Systems laser mill (Fig A1-18a.) was administered to cut window patterns in a 5mil thick polyimide film. Fig A1-18b. shows an AutoCAD design of a first generation of gate mask. After prototyping several variations of gate dimensions, as presented in chapter 3, a consistent mask method was established with a second-generation polyimide film mask. The second-generation (G2M) gate mask implemented reduced gate width geometry to lower parasitic capacitances between the gate electrode and the source-drain layers. The overlap of the metallic layers may generate larger capacitances that reduce transistor performance. Additionally, the second-generation mask incorporates two large contact pads that could be masked by tape or PDMS stamps. After removal, in most cases, enough of the metallic film was preserved for proper contact to the gate when using tape. The method for masking the contact pads in final devices utilized PDMS stamps during the deposition of Parylene C. Fig A1-18c. pictures G2M with two contact pads and a thin strip connecting them.
Figure A1-18: Two generations of polyimide gate masks by laser milling; (a) Universal Laser Systems system; (b) First generation gate mask; (c) finalized gate mask for OTFTs.

2.1.2. Microlution 5-axis Mill:

Several metallic masks for the source-drain electrodes were first created in Autocad, and then extensively developed in Mastercam X5 software for milling with the Microlution 5100-S 5-axis Mill system pictured in Fig A1-19a. The internal milling components are pictured in Fig A1-19b and A1-19c.
Figure A1-19: Microlution 5-axis milling system and components; (a) Microlution milling machining; (b) Mounting stage and tool bit arm; (c) Internal view of milling area.

An ultra-flat, 75µm thick test mask was milled out of a standard 2”x 2” stainless steel chuck. The test mask with (2.5mm)$^2$ openings were milled in 16 locations of the metallic plate.

The first-generation source drain (SD-G1) mask was milled using dimensions of the channel of $L=100\mu m$ and $W=1000\mu m$. These dimensions were chosen with the knowledge the Microlution Mill was capable of achieving these resolutions from unrelated milling work. An array of 8 separate TFT devices was milled out of a 6.25mm
thick aluminum puck. SD-G1 is pictured in Fig A1-20a. and a zoomed view of three separate transistor devices is pictured in Fig A1-20b.

![Figure A1-20](image)

**Figure A1-20**: First generation gate mask; (a) full view of metallic mask with \(W=1000\mu m\) and \(L=100\mu m\) dimensions; (b) Magnified view of four transistor window regions.

The second-generation source drain (SD-G2) mask was milled using dimensions of the channel of \(L=50\mu m\) and \(W=500\mu m\). Again, these dimensions were chosen with the knowledge the Microlution Mill was capable of achieving these resolutions after milling SD-G1. SD-G2 also consisted of an 8 transistor array and were milled out of an 6.25mm thick aluminum puck. SD-G2 is pictured in Fig A1-21a. and a 50x view of a transistor channel region is pictured in Fig A1-21b.
Figure A1-21: Final generation gate mask; (a) full view of metallic mask with W=500µm and L=50µm dimensions; (b) 50x magnified view of a transistor window region.

2.1.3. Sputtering system and Gate Deposition

Figure A1-22: Photo of full sputtering system used for gate deposition.
The starting layer in the bottom-up (top-contact) TFT model is deposition of the gate material. A Denton Vacuum DC/RF sputtering system (Fig. A1-22.) deposited the metallic gate film. Test depositions using DC sputtering of aluminum through G1M were done on paper substrates for verification of film quality. Deposition issues arose with G1M when laid flat on the sample stage, with rotation. The system is equipped with a shutter to allow target conditioning before deposition. This shutter required the substrate to lay flat on the sample stage. DC power of 150W was typically used, with the cryogenic pump achieving a base pressure of $7.0 \times 10^{-7}$. Argon pressure was set to 3.1 microns of mercury for proper plasma conditions.

Fig A1-23a. provides an image of low quality aluminum on the paper substrate material over a 26 minute deposition period after a 10 minute target condition time. The polyimide mask was slightly “bowed” because of its flexible nature. The mask sidewall bowing, along with the sample-to-target angle being large caused non-conductive films to deposit on the surface of the paper. Frequently this deposition problem remained and the poor film quality was inadequate for TFT applications. Aluminum showed stress cracks when handling the paper after deposition (Fig A1-23c).
Figure A1-23: Various depositions of gate electrodes; (a) Sputtered aluminum with poor quality deposition through polyimide gate mask, on paper; (b) Angled deposition of aluminum showing a higher quality film on paper; (c) defects of aluminum deposited on a paper substrate; (d) Copper film on paper with high quality deposition by tilting of the sample substrate, incorporating a polyimide mask.

Samples were placed at an angle so the sample surface and target surface were parallel to one another (Fig A1-23b.). The ability to condition the target before deposition on the sample surface was sacrificed since the sample shutter needed to remain open. Conducting films of aluminum were achieved however and angling of the sample to the target was done for all working OTFT devices.

The aluminum issues were countered by switching to radio-frequency (RF) sputtering of copper gates, with samples placed at an angle to the target surface. Fig A1-23d. shows an example of RF sputtered copper electrodes using the angled method.
General sputtering conditions for copper gates were as follows. Forward power of 175W and reflected power of 23W. A base pressure of $5 \times 10^{-7}$ Torr was achieved before argon gas introduction. Argon plasma was produced with a pressure of 4 microns of mercury. Typical thicknesses ranged from 100nm to 850nm of copper. The large range is a product of testing various thicknesses to determine if gate thickness affected the functionality of transistors. Gate thickness likely shouldn’t impact whether OTFTs functioned, resulting in the large thickness range.

### 2.1.4. Specialty coating systems Parylene C Deposition

The step after gate deposition was coating thin-films of the dielectric Parylene C (PC). This was performed with a Specialty Coating Systems LabCoater 2, equipped with a mechanical roughing pump (Fig A1-24a). Pressures of ~8 mTorr with a liquid nitrogen trap were regularly achieved. Typical film thicknesses ranged between 250nm to 700nm. The amount of Parylene dimer (being added if Fig A1-24b.) selected determined film thickness as well as if the sample was placed face side up or face side down. Earlier samples were placed face side up while the later OTFT comparison samples were placed face down. It was recommended by manufacturer technician to place the samples face down to reduce pinhole defects in the films. A 2005 review by Facchetti et al. [6] details advancements made in the area of gate dielectrics for use in OTFT applications.
Figure A1-24: Parylene C coating system; (a) System showing parameter controllers; (b) Adding Parylene C dimer in aluminum foil boat to vaporizer.

It should be mentioned here that prototype devices were difficult to produce working paper devices with Al$_2$O$_3$ proved to be difficult to fabricate and test. The oxide thin-films fractured as the paper substrate was handled. This problem generated the switch to PC so flexibility could be maintained throughout processing and fracturing would not occur.
2.1.5. Pentacene Thermal Sublimation:

![Diagram of the pentacene thermal sublimation system]

**Figure A1-25:** Pentacene thermal sublimation system.

A custom, in-house pentacene sublimation system (Fig A1-25) was configured for thin film deposition of the semiconductor layer pentacene. The system is equipped with a Pfeiffer Hi-Cube turbo molecular pump delivering a consistent base pressure of values in the high $10^{-8}$. Pentacene deposition is apparent on glass substrates when sublimed at temperatures ranging from 120°C to 190°C. Initial results indicated \(\sim 1\text{Å/sec}\) is achieved with a cell temperature range of 125-150°C. **Figures A1-26a and A1-26b** are pictures of the quartz crucible used for pentacene sublimation. The typical amount of fresh pentacene added to the crucible every 4 to 6 runs was \(\sim 85\text{mg}\). This was done after discarding the used pentacene and sonicating the crucible in chloroform, methanol, and
then ethanol. The crucible was then baked at 200°C for 30 minutes. In Fig A1-26c, the substrate stage is shown with a custom carbon-heating element. The sample surface is downward facing perpendicular to the crucible and retaining clips were added to keep the sample in place. A type K thermocouple was placed on the sample surface in each independent run. Temperatures were controlled by a DC power supply directly connected to the electrodes of the carbon-heating element. Sample substrate temperatures ranged from ~30-100°C as it has been shown pentacene and π-conjugated organics generate higher quality films[7-11].

Figure A1-26: Images of crucible and heating stage; (a) Pentacene added to a quartz crucible; (b) Quartz crucible added with pentacene; (c) Sample mounting stage with a carbon heating element and retaining clips for securing the sample.
2.1.6. Thermal Evaporation:

Organic semiconductor sensitivity to light and atmospheric contaminants like oxygen[12] increases the need for reducing time between layer depositions. Thermal evaporation in a diffusion pump based system in Fig A1-27a. functioned as the gold thin-film application method. Evaporation attempts for initial configurations were unsuccessful due to the inability to provide sufficient power for proper temperature values with three strand tungsten baskets to melt 0.4g of several 1/8” pellets. Changing to a single, conically shaped (4mm inner-diameter), tungsten wire basket rectified the temperature insufficiencies. Evaporation temperatures were successfully reached (~1200°C) at 15 Amps, while maintaining a vacuum pressure in the $10^{-7}$ Torr range (penning gauge). After finding single wire baskets allow sufficient gold layer deposition, further film improvements were made through use of a single wire basket coated in a thick layer of aluminum oxide, pictured in Fig A1-27b. This not only concentrates higher levels of gold to the substrate but also increased deposition rates and thicknesses. ~100nm was easily achieved over a 5 minute deposition period as measured by a crystal monitor with a tooling factor of 0.67 and a density value of 19.30g/cm$^3$. 

Figure A1-27: Thermal evaporation system depositing gold; (a) System components and sample holder facing the heated tungsten wire basket; (b) Single tungsten wire coated in a thick alumina layer as the receptacle for gold deposition.
References


Appendix 2- Early Paper Transistors

1. Introduction

Functional prototype devices allowed further investigation into a narrower range of fabrication conditions and electrical parameters. After prototyping the OTFT array, tests were conducted with varying conditions on flexible glass and on paper substrates. This would enable a set of conditions to be selected for comparing different OTFT substrates in chapter 4. The smooth surface and flexible nature of Corning Willow (100µm thick) glass allotted to the understanding of handling a delicate substrate though was still capable of being implemented practically.

1.1. Fabrication of paper devices

Transistors arrays with functional OTFT were produced on Sappi paper through the methods described previously. Final OTFT arrays of each sample are pictured in Fig A2-28a-c. Further fabrication details are described for each device. The fabrication steps taken are different between each array in order to finalize a set of methods that would enable a comparison to be drawn.

PD1

PD1 (Fig A2-28a.) began with a ~850nm copper gate by sputter deposition. The large contact pads were then masked with a polyimide film and taped. 650nm (0.4g) of PC dimer was vapor deposited with the sample faceside up. With the contact pads still masked, pentacene was then thermal evaporated with a substrate temperature of 80°C and
an evaporation temperature of 140°C for a total thickness of ~38nm. The source-drain contacts were deposited at a thickness of ~50nm.

**Figure A2-28:** OTFT arrays on various paper substrates; (a) PD1 sample with eight transistors; (b) PD2 sample with eight transistors; (c) PD3 sample with six devices.

**PD2**

PD2 (Fig A2-28b.) started with a different gate thickness of ~350nm of copper by sputter deposition. The large contact pads were then masked with a Kapton tape. ~650nm (0.4g) of PC dimer was vapor deposited with the sample faceside up. Approximately 75nm of pentacene was then thermally evaporated at a crucible
temperature of 135°C and a substrate temperature of 98°C. The source-drain contacts were deposited at a thickness of ~50nm.

**PD3**

A gate thickness of ~300nm of copper by sputter deposition was first deposited on PD3 (Fig A2-28c). The large contact pads were then masked with a Kapton tape. ~200nm (0.2g) of PC dimer was vapor deposited with the sample faceside up. ~38nm of pentacene was then thermally evaporated at a crucible temperature of 135°C and a substrate temperature of 80°C. The source-drain contacts were deposited at a thickness of ~50nm with 2 of the damaged transistor regions masked.

### 1.2. OTFT Electrical Properties on Paper

The electrical measurements of I-V sweeps are shown in Fig A2-29a-c. The measurements were taken at different electrical parameters to better understand how well the OTFT devices operate across sample changes. PD1 data was collected with a $V_{DS}$ voltage sweep from 0 to -100V and $V_{GS}$ voltages up to -55V. Seen in the I-V curves of Fig A2-29a, $I_{DS}$ doesn’t plateau and fully saturate at the given voltages. This may be attributed to the thickness of the copper gate and PC layers. The thickness of the gate electrode may not allow proper conformal coverage of the 650nm PC layer. This could create defect states that contribute to leakage current and the channel doesn’t fully pinch-off. The there is non-linearity at the lower voltages signifying poor injecting contact[1]. Utilizing the equations, electrical parameters are extracted for the device. The gate capacitance per unit area was first calculated using the eq 8.
\[ C_i = \frac{\varepsilon_o \varepsilon_r}{t} \]  

(8)

Where, \( C_i \) is the gate capacitance per unit area, \( \varepsilon_o \) is the permittivity of \( 8.85 \times 10^{-12} \text{ N/m}^2 \), \( \varepsilon_r \) is the dielectric constant (3.1-manufacturer specifications) of PC, and \( t \) is the thickness of the dielectric layer (650nm). The calculated value of \( C_i = 4.22 \text{nF/cm}^2 \). A transconductance in the saturation regime of \( 2.7 \times 10^{-9} \text{ S} \) at \( V_{GS} = -55 \text{V} \). Field-effect mobility at the same gate voltage shows a mobility of \( \mu_{stat} = 9 \times 10^{-4} \text{ cm}^2/\text{Vs} \) and directs to the low performance of the OTFT of PD1.

\[ \begin{align*}
\text{(a)} & \quad \text{Drain-Source Current (\mu A)} \\
& \quad \text{Drain-Source Voltage (V)} \\
& \quad V_{GS} = -55 \text{V} \\
& \quad V_{GS} = -45 \text{V} \\
& \quad V_{GS} = -35 \text{V} \\
& \quad V_{GS} = -25 \text{V} \\
& \quad V_{GS} = -15 \text{V} \\
\text{(b)} & \quad \text{Drain-Source Current (\mu A)} \\
& \quad \text{Drain-Source Voltage (V)} \\
& \quad V_{GS} = -60 \text{V} \\
& \quad V_{GS} = -45 \text{V} \\
& \quad V_{GS} = -35 \text{V} \\
& \quad V_{GS} = -25 \text{V} \\
& \quad V_{GS} = -15 \text{V} \\
\text{(c)} & \quad \text{Drain-Source Current (\mu A)} \\
& \quad \text{Drain-Source Voltage (V)} \\
& \quad V_{GS} = -55 \text{V} \\
& \quad V_{GS} = -45 \text{V} \\
& \quad V_{GS} = -35 \text{V} \\
& \quad V_{GS} = -25 \text{V} \\
\end{align*} \]

Figure A2-29: I-V characteristic curves of OTFT individual transistors; (a) Curves for PD1; (b) PD2 curves; (c) PD3 curves.
I-V parameters for PD2 in Fig A2-29b. were collected with a $V_{DS}$ voltage sweep from 0 to -50V and $V_{GS}$ voltages up to -60V. The gate voltages to -45V indicate suitable saturation that reaches into the $\mu$A currents. Upon using the same $C_t = 4.22\text{nF/cm}^2$ for PD2, a more respectable saturation mobility $\mu_{sat} = 0.013 \text{ cm}^2/\text{Vs}$ is achieved at a $V_{GS} = -45V$. Transconductance calculated with eq 3. at $V_{GS} = -45V$ is a more accurately represented value of $4.3\times10^{-8} \text{ S}$.

PD3 I-V curves in Fig A2-29c. were taken with a $V_{DS}$ voltage sweep from 0 to -50V and $V_{GS}$ voltages up to -60V. Transistor behavior is moderately well behaved at the gate voltages to -55V and show desirable saturation that reaches into the $\mu$A currents. However, leakage current is apparent at near zero drain-source voltages with $I_{DS} = 7.9\times10^{-10} \text{ A}$ at $V_{GS} = -45V$ and -55V. It is speculated that this reveals dielectric breakdown starting to occur because current was not measured at positive voltages. Gate capacitance is recalculated to $C_t = 0.13\text{nF/cm}^2$ for the thinner dielectric of PD3. Saturation mobility $\mu_{sat} = 1.5\text{cm}^2/\text{Vs}$ is achieved at a $V_{GS} = -55V$. Transconductance calculated at $V_{GS} = -55V$ of $9.8\times10^{-8} \text{ S}$. Both mobility and Transconductance are larger than plausible that could be an artifact of the leakage current seen.

**References**