I, Matthew A Barnes, hereby submit this original work as part of the requirements for the degree of Master of Science in Electrical Engineering.

It is entitled:
Integrating High Temperature Superconducting Yttrium Barium Copper Oxide with Silicon-on-Sapphire Electronics

Student’s name: Matthew A Barnes

This work and its defense approved by:

Committee chair: Altan Ferendeci, PhD
Committee member: Joseph Thomas Boyd, PhD
Committee member: Peter Koesel, PhD

University of Cincinnati
Integrating High Temperature Superconducting Yttrium Barium Copper Oxide with Silicon-on-Sapphire Electronics

A thesis submitted to the Graduate School of the University of Cincinnati in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering in the Department of Electrical and Computer Engineering of the College of Engineering and Applied Sciences by

Matthew Barnes

B.S.E.E. University of Cincinnati
June 2007

Committee Chair: Altan M. Ferendeci, Ph.D
Abstract

High temperature superconductors (HTSC) offer near zero loss performance when operated below the critical temperature which – at this point in the evolution of HTSCs – ranges from 77K to well over 100K, meaning that they can be cooled by readily available and relatively cheap liquid nitrogen.

Silicon-on-insulator (SOI) electronics have proven advantageous with very low parasitics, very low power consumption, and easy integration to high yield CMOS processes [1]. It also enjoys a much lower cost than the more exotic III-V semiconductors that are their best competitors performance-wise.

This research develops and validates processes to develop silicon-on-sapphire (SOS) electronics and YBCO electronics, side-by-side, on the same wafer, without degrading either respective material, or the electrical performance of devices fabricated on either material.
Acknowledgements

First and foremost I thank Dr. Ferendeci, for guidance and advice throughout my graduate work. Without him and his guidance, this document would not exist.

Secondly, I must thank the members of my committee for taking the time to review my thesis project.

Thanks to Dr. Kosel who not only allowed usage of his laboratory facilities, as well as in depth instruction on their operation, but challenged me academically in the classroom.

For advice on all facets of graduate school, Julie Muenchen is an encyclopedia. Her willingness to help and responsiveness to all of my questions was invaluable.

As important as anyone is my family for their continued support and advice on all things, and my lovely fiancé for her unwavering patience.
# Table of Contents

Chapter 1: 
Introduction ........................................................................... 1

1.1 Superconductors (YBCO) ......................................................... 1
1.2 Silicon-on-Sapphire (SOS) ....................................................... 2
1.3 Integration Challenges ........................................................ 3
1.4 Research Goals ...................................................................... 4
1.5 Integration Benefits .............................................................. 4

Chapter 2: High-Temperature Superconductors (HTSCs) ..................... 7

2.1 YBCO Conduction Mechanism ............................................... 7

Chapter 3: State of the Technology .................................................. 10

3.1 State of YBCO Technology .................................................... 10
3.2 State of SOS Technology ...................................................... 13

Chapter 4: Developing the Design Process ........................................ 16

4.1 YBCO Processing Considerations .......................................... 16
4.2 Annealing Considerations ..................................................... 19
4.3 Silicon Processing Considerations ......................................... 21
4.4 Order of Processes .............................................................. 23

Chapter 5: Design ....................................................................... 26

5.1 Resonator Design ................................................................. 26
5.2 Schottky Contact ................................................................. 28
5.3 Ohmic Contact ..................................................................... 31
5.4 Theoretical Schottky Characteristics ...................................... 32

Chapter 6: The Fluid Process of Design ........................................... 35

6.1 Calibration Verifications ......................................................... 35
6.2 Resonator, Jig, and Test Configuration Troubleshooting .............. 47
6.3 Ground Plane ...................................................................... 52
6.4 Probe Contact ..................................................................... 53
6.5 Mask Redesign ................................................................. 56

Chapter 7: Results .................................................................... 64

7.1 Resonator Results – Physical Dimensions .................................. 64
7.2 Resonator Results – Electrical Characteristics ............................ 71
7.3 Schottky Contact – Physical Dimensions ................................ 78
7.4 Schottky Contact – Electrical Characteristics ......................... 82
Chapter 8: Conclusion

8.1 Conclusion

8.2 Future Works
<table>
<thead>
<tr>
<th>Figure reference</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Figure 2.1.1a</td>
<td>Lattice Bending</td>
</tr>
<tr>
<td>Figure 2.1.1b</td>
<td>Travelling Electron</td>
</tr>
<tr>
<td>Figure 3.1.1</td>
<td>SQUID Layout</td>
</tr>
<tr>
<td>Figure 3.1.2</td>
<td>Josephson Junction Layout</td>
</tr>
<tr>
<td>Figure 4.1.1</td>
<td>EDTA Chelation Action</td>
</tr>
<tr>
<td>Figure 4.1.2a</td>
<td>Photoresist Solvent from Chemical Breakdown</td>
</tr>
<tr>
<td>Figure 4.1.2b</td>
<td>Photoresist Binder from Chemical Breakdown</td>
</tr>
<tr>
<td>Figure 4.1.2c</td>
<td>Photoresist Photoactive Compound from Chemical Breakdown</td>
</tr>
<tr>
<td>Figure 4.3.1</td>
<td>Process Flow Chart – Broad Outline</td>
</tr>
<tr>
<td>Figure 4.4.1a</td>
<td>Detailed Process Flow – Part 1</td>
</tr>
<tr>
<td>Figure 4.4.1b</td>
<td>Detailed Process Flow – Part 2</td>
</tr>
<tr>
<td>Figure 5.2.1</td>
<td>Band Diagram for P-Type Silicon Including Relevant Values</td>
</tr>
<tr>
<td>Figure 5.2.2a</td>
<td>Band Diagram of Metal for Schottky Contact Illustration</td>
</tr>
<tr>
<td>Figure 5.2.2b</td>
<td>Bend Bending from Metal Contacting Silicon</td>
</tr>
<tr>
<td>Figure 6.1.1a</td>
<td>Vacuum Pump and Compressor Portion of Test Configuration (photo)</td>
</tr>
<tr>
<td>Figure 6.1.1b</td>
<td>Pressure Gauge and Temperature Control Portion of Test Configuration (photo)</td>
</tr>
<tr>
<td>Figure 6.1.1c</td>
<td>Cold Finger and Test Chamber Portion of Test Configuration (photo)</td>
</tr>
<tr>
<td>Figure 6.1.1d</td>
<td>Top View of Ports into Test Chamber Portion of Test Configuration (photo)</td>
</tr>
<tr>
<td>Figure 6.1.1e</td>
<td>RF Characterization at Cryogenic Temperature Configuration (diagram)</td>
</tr>
<tr>
<td>Figure 6.1.2a</td>
<td>Top View of Resonator Jig</td>
</tr>
<tr>
<td>Figure 6.1.2b</td>
<td>Side View of Resonator Jig</td>
</tr>
<tr>
<td>Figure 6.1.2c</td>
<td>Schematic Drawing of Resonator Jig</td>
</tr>
<tr>
<td>Figure 6.1.3a</td>
<td>Scattering Parameters of Resonator Pre-Jig-Modification (8-12GHz)</td>
</tr>
<tr>
<td>Figure 6.1.3b</td>
<td>Scattering Parameters of Resonator Pre-Jig-Modification (8-10GHz)</td>
</tr>
<tr>
<td>Figure 6.1.3c</td>
<td>Scattering Parameters of Resonator Pre-Jig-Modification (10-12GHz)</td>
</tr>
<tr>
<td>Figure 6.1.4a</td>
<td>Calibration Verification of S11 (Open)</td>
</tr>
<tr>
<td>Figure 6.1.4b</td>
<td>Calibration Verification of S22 (Open)</td>
</tr>
</tbody>
</table>
Figure 6.1.4c…… Calibration Verification of S21 (Open)
Figure 6.1.4d…… Calibration Verification of S12 (Open)
Figure 6.1.5a…… Calibration Verification of S11 (Open)
Figure 6.1.5b…… Calibration Verification of S22 (Open)
Figure 6.1.5c…… Calibration Verification of S21 (Open)
Figure 6.1.5d…… Calibration Verification of S12 (Open)
Figure 6.2.1a…… Magnified Schematic View of Resonator Probe Contact
Figure 6.2.1b…… Magnified Schematic View of Potential Loss of Resonator Probe Contact
Figure 6.2.2……… Problem with Copper Tape used as Ground Plane
Figure 6.2.3a……… Simulation of a Half-Wave Resonator with Perfect Contact Made at the Terminals
Figure 6.2.3b……… Simulation Modeling Losses from Spacing Between Probes and Feed Lines
Figure 6.3.1………. Sketch of Surface Profile Verifying Aluminum Deposition Thickness
Figure 6.4.1………. Probe Bonded to Feed Lines by way of Silver Paint Pen
Figure 6.5.1a…… Original Alignment Marks as Viewed Through the Lens of a Microscope
Figure 6.5.1b…… Original Alignment Mark Progression
Figure 6.5.2a……… Projection of Visible Area under Original Alignment Marks
Figure 6.5.2b……… Mask Centered Over Alignment Marks
Figure 6.5.3………. Layering of Mask Aligning Procedure
Figure 6.5.4………. Original Versus Revised Alignment Marks
Figure 6.5.5……….. Newly Added Rotational Alignment Mark
Figure 7.1.1………. Dimensions of YBCO Resonator
Figure 7.1.2a……… ADS Simulation Showing S11 as Designed
Figure 7.1.2b……… ADS Simulation Showing Negligible shift in S11 for Five Microns of Over-Etching
Figure 7.1.3………. ADS Simulation Showing S11 with Ten Micron Gap
Figure 7.1.4………. Surface Profile of Etched YBCO
Figure 7.2.1a……… S11 VNA Data for Completed Resonator at Room Temperature
Figure 7.2.1b……… S21 VNA Data for Completed Resonator at Room Temperature
Figure 7.2.2a...........Magnitude of S11 Response to Decrease in Temperature
Figure 7.2.2b...........Table of Discrete Values from Figure 7.2.2a
Figure 7.2.3a...........Magnitude of S11 and S22 at 10 Kelvin
Figure 7.2.3b...........Magnitude of S11 and S22 at 10 Kelvin with Focus on Peak
Figure 7.3.1a..........Resolution of Photolithography – Alignment Marks
Figure 7.3.1b..........Resolution of Photolithography – Channel Length
Figure 7.3.2..............Surface Profile of Test Sample Showing Reliable and Expected Photoresist Thickness
Figure 7.3.3..............Illustration of Surface Profile of Aluminum Deposition Sample
Figure 7.4.1..............Collector Supply Setting for Curve Tracer During Schottky Characterization
Figure 7.4.2..............Current-Voltage Characteristic of Schottky Contact
Chapter 1

1.1 Superconductors (YBCO)

Superconductors have the properties of approaching near zero resistance when in an environment whose temperature is below the critical temperature of the superconductor. Until recently, superconductors had critical temperatures ranging from 1-20K [2]. While these conventional superconductors had good resistance characteristics at their respective critical temperatures, they simply lack practicality (at least within Earth’s atmosphere) due to the high cost of cooling. However, the advent of high temperature superconductors (HTSC) opens up new possibilities for practical applications. HTSCs have critical temperatures ranging from 77K to 130K meaning that liquid nitrogen–abundantly available–can be used for cooling while remaining inside the stratosphere and the comfort of a temperate climate.

Interest in superconducting thin film applications truly sparked with the discovery of yttrium-barium-copper-oxide (YBa$_2$Cu$_3$O$_{7-\delta}$, or simply YBCO for the sake of avoiding subscript clutter) in 1987 and moreover, the discovery that this oxide and others like it entered a superconducting state above the boiling point of liquid nitrogen. Specifically, the methods used for fabrication were – and are – of the utmost importance. Some of the first methods of fabrication left researchers pessimistic regarding the potential for microwave applications as some of the early YBCO fabrication methods yielded a bulk material with grain boundaries and high anisotropy – both of which were assumed to be the cause of the poor RF properties [4]. These assumptions were verified by subsequent production techniques such as laser ablation [5] – and pulsed laser deposition [6] – by lessening the production defects joined with an improvement in RF performance and characteristics. With the potential for high quality films the way for microwave devices is paved.

Indeed, many have fabricated and characterized high-temperature-superconducting devices such as cavity resonators, ring oscillators, and phase shifters [7]-[8].
1.2 Silicon-on-Sapphire (SOS)

The second material of interest in this research is silicon. It is a dominant force in the semiconductor industry whose physical, chemical and electrical characteristics have been exhaustively researched and characterized. Additionally, almost every aspect of every mainstream method of processing silicon has been optimized – from CMOS fabrication, to nano-structure fabrication, to photovoltaic fabrication. Of specific relevance to this research is the use of silicon for microwave applications. While materials such as gallium arsenide may have superior characteristics such as higher electron mobility – the characteristic that will ultimately allow gallium arsenide to have a higher cut-off frequency – silicon has the benefit of ease-of-processing, abundance, and more importantly, significant hole mobility, making it much more desirable and practical for CMOS logic. While CMOS logic is not a part of this research, its significance in any work with silicon is undeniable as it was a key reason for silicon dominating the market.

Thanks to the rigorous development of silicon in all of its forms it is well known that for microwave applications, silicon-on-insulator (SOI) technology yields good microwave characteristics. When sapphire is the insulator the microwave characteristics become about as good as possible on a silicon substrate. Peregrine’s silicon on sapphire (SOS) fabrication process is not only established, but it has been used as the basis for the fabrication of microwave devices with great success [9]. In fact, an important side effect of this research is improvement in the practicality of HTSCs so the decision to use Peregrine’s process for the SOS sector of the substrate can likely be attributed to the established and prolific nature of it. Using such a common process is a natural decision based on the goals of this research.
1.3 Integration Challenges

At this juncture, the problem faced by engineers and scientists is integration of superconducting materials with more traditional materials such as silicon, gallium arsenide and germanium. Integration is critical as all of these materials have well established fabrication methods and their manipulation is well researched. In order for HTSCs to have an impact on the performance of a system, the integrity of the material must be maintained through any of the semiconductor processes with the same being true for said semiconductor with respect to HTSC processes. It has been shown that thin films of YBCO and silicon can be fabricated on the same sapphire substrate and is the starting point of this thesis research. The specifics of the process by which the thin-films are created side-by-side on the same wafer are outside the scope of this thesis. However, a brief description is likely helpful. The starting point is a sapphire substrate. Half of the substrate is masked and a buffer layer of cerium dioxide ($\text{CeO}_2$) is deposited – for the purpose of lattice matching – followed by the YBCO deposition. The mask is then removed, leaving half of the substrate as bare sapphire and the other half a thin YBCO film on a ceramic buffer. A second mask is applied over the YBCO this time, and a silicon film is deposited – albeit with many defects, due in part to the lattice mismatch of the sapphire and silicon. Silicon ions are then implanted and the wafer is annealed causing crystallization of the amorphous silicon near the sapphire surface and oxidation at the silicon surface. When the oxide is removed a high quality silicon film remains. The silicon deposition and manipulation follows the Peregrine Process. The mask is then removed and a YBCO film side-by-side with silicon film is what remains.

1.4 Research Goals

Integration of the two materials presents challenges. Primarily, there is a clash of compatibility with the silicon fabrication process and the maximum temperature that YBCO may be exposed
to without prematurely oxygenating or rendering the material non-superconducting. In this work, the cornerstone of microelectronics is used as the component to be fabricated alongside YBCO to determine if such integration is possible. A transistor process will be developed and tested that does not require the exposure of the substrate to temperatures in excess 500°C and protects the YBCO from any moisture during said process. This will allow for simultaneous production of superconducting devices alongside conventional silicon-on-insulator (SOI) transistors.

Additionally, a superconducting resonator will be fabricated in such a way as to not degrade the quality of the silicon with which it shares a substrate.

1.5 Integration Benefits

The appeal of integrating passive, and possibly even active, HTSC components with conventional electronics like silicon-on-sapphire can be primarily summarized by the ideal nature of superconducting components. Zero resistive loss components can have great positive impact outside of just “making the math easier.”

A telling characteristic of many passive components is the quality factor (Q) of said components. Often, the quality factor is surrounded and convoluted with manipulation of inherent values of discrete circuit components towards the goal of finding a value of “Q” that can be paraded on data sheets to tout the quality of the component. However, conceptually, the quality factor is just a ratio of power stored by the device (or component) to the power dissipated over the course of one cycle of operation. Since most power is dissipated by resistive losses and the resistance of a conductor made out of superconducting material is effectively nonexistent, the quality factor of discrete components made out of YBCO (or any superconductor) quickly grows very large. While a large quality factor can allow for very fine tuning of resonant circuits, the low
resistance responsible for the high quality factor is dually responsible for increasing power efficiency – a value chased by electrical engineers of all disciplines.

Specific circuit components that can benefit from high quality factors include two of the usual suspects: inductors and capacitors. Quality factor for both is largely dependent on resistive losses; the quality of an inductor is:

\[ Q_L = \frac{x_L}{R_L} \]  \hspace{1cm} \textbf{[1.5-1a]}

The parasitic resistive component in equation 1.5-1 is represented by RL which is close to zero – especially in planar spiral type inductors. Similarly, the quality factor of a capacitor is

\[ Q_C = \frac{x_C}{R_C} \]  \hspace{1cm} \textbf{[1.5-1b]}

where \( R_C \) is the parasitic resistance of the capacitor. Again, as \( R_C \) goes to zero, the capacitor behaves more and more ideal. With ideal capacitors and resistors, tank circuits can be tuned to a very high degree of accuracy allowing more selective bandwidth.

Using superconducting transmission lines for RF circuitry, the real estate of a layout can be significantly reduced by decreased cross-talk effects [10]. In copper printed circuit boards, keeping lines from running parallel to one-another when possible, keeping transmission lines as short as possible and decreasing spacing between components, are all ways to reduce cross-talk. Additionally, when lines must run parallel to one-another, a good rule is to space the transmission lines by a microstrip line-width to reduce cross-talk. For some circuits, the aforementioned design constraints can be prohibitive, and would be lessened significantly if the lines were cooled and superconducting.

Speaking to the placement of circuit components and reaping benefit from fewer constraints, a specific example of low noise amplifier (LNA) placement for the purpose of amplifying wirelessly
received signals is an obvious beneficiary of said benefits. The very function of an LNA dictates that it be placed as closely to the antenna receiving the signal as possible so as to minimize distortion and losses from line length which may make the integrity of the signal susceptible to the already low signal-to-noise ratio. However, it’s obvious that while this design constraint is normally adhered to, not doing so in many cases could be more convenient, less expensive, and less complex. Again, cooled superconducting transmission lines can alleviate some of the constriction of conventional design constraints.

In this work, a simple half-wave resonator is fabricated. However, HTSCs can be used for a wide array of resonators and filters including more complex filters. Multiple sections of coupled resonators would make a bandpass filter with a nearly ideal passband and sharp drop off; similarly, low pass and high pass filters could be designed to stop or start passing frequencies almost entirely after the cutoff frequency.

Beyond the possible improvements to conventional electronics, devices such as SQUIDs (see Chapter 3) are made possible by the properties inherent in superconductors and specifically Josephson Junctions, namely the sensitivity of a junction being high enough to be affected by a single flux quantum[11].
Chapter 2

2.1 YBCO Conduction Mechanism

The most sound theories developed to describe the mechanism of superconductivity cannot be used to describe YBCO’s conduction mechanism on the microscopic level (or any other HTSC for that matter). The BCS theory posits that the increasing formation of cooper pairs – and their interaction with lattice vibration (phonons) – as the temperature of the HTSC approaches the critical temperature is responsible for the transition from a non-superconducting state to a superconducting, as well as the Meissner effect and other unique thermodynamic properties of superconductors [12].

The basic underpinnings of BCS theory stems from the non-fluid nature of the ions. That is, there is little to no movement due to heat in the lattice. When an electron is injected into the superconducting material, its negative charge attracts the positively charged metal ions as it travels (figure 2.1.1a). The attraction between negatively charged particle A and particles C, D, E, and F causes a bending in the lattice which is important, but the more immediate affect is the concentration of positive charges as they are pulled to the negative charge, A.
Figure 2.1.1a: An exaggerated representation of the “lattice bending” which causes one electron of a Cooper pair to be attracted to the other.

As the negatively charged particle A travels through the lattice the movement of the positively charged particles causes band bending and phonons throughout the lattice.

Figure 2.1.1b: As the electron travels, the higher concentration of positive ions shifts around the position of the traveling electron.
The higher charge concentration creates a stronger attractive force on electrons in the nearby vicinity. The wording in the theory suggests that a second electron is attracted to electron A, but it seems more accurate to say that the second electron is attracted to the position of electron A as it is actually the grouping of metal ions caused by electron A that is responsible for propelling the second electron towards electron A. Unfortunately, there is no theory as sound as that developed by Bardeen, Cooper, and Schrieffer to describe the behavior of high-$T_c$ superconductors on a microscopic level. As such, only well-known and repeatedly measured characteristics can be used as the guidelines for processing and design of the superconducting device.

For instance, typical critical current densities ($J_c$) of YBCO are in the high hundreds-of-thousands to low millions of amperes per square centimeter for thin film samples (bulk samples have much lower $J_c$ due to granularity caused by grain boundaries inherent in the YBCO structure [13]); the transition temperature is assumed to be approximately 92K for a good sample; the upper critical magnetic field ($H_{c2}$) can be as high as 100 Tesla.
Chapter 3

3.1 State of YBCO Technology

The potential uses for a superconductor as well-studied as YBCO, and whose various fabrication and processing procedures are as thoroughly developed, are fairly extensive and promising.

Likely, one of the most prolific – or at least, pedestrian – uses of superconductors is high powered magnets in a magnetic resonance imaging (MRI) device. To be effective, these coiled magnets create fluxes of up to 1.5 T in strength [14] and were it not for superconducting magnets, the amount of energy needed to create such a strong and consistent field would be prohibitive – if not impossible. The stationary and contained nature of the MRI device makes cooling very feasible, and thus, superconducting MRI magnets a practical and effective solution to the requirements of MRI technology.

Japan is developing a magnetically levitating train which uses superconducting magnetic coils aboard the train to interact with stationary guiding coils on the track. Using HTSCs to create electromagnets aboard an electrodynamic suspension (EDS) or electromagnetic suspension (EMS) train allows for strong fields more easily obtained than those in similar systems using conventional electromagnets. The MLX01 is the test train that achieved record speeds of 581 kilometers per hour, and utilizes the Meissner Effect to remain levitating and on course[15]. The superconductors are cooled in the presence of the magnetic field created by the permanent magnets with a gap between the superconductors and the magnetic track. Using an array of alternating poled electromagnets, the train is both attracted to, and repelled by, the guiding system. That is, the system is self-stabilizing as a result of flux pinning. Once again, it is the contained nature of the superconductors that make cooling feasible. If, rather than the rail being
permanent magnets and the car holding superconductors, the rail was a superconductor and the car held permanent magnets, the logistics of cooling the superconductor would be painful.

It’s a lack of the contained nature, that make superconducting power lines – possibly one of the most appealing applications of high temperature superconductors – the most difficult to physically implement. Losses from power transmission lines come primarily from what is referred to as “$i^2R$ losses” (where ‘$i$’ is the magnitude of the alternating current, and ‘$R$’ is the resistance of the alloy used for the power line). The current is kept relatively low by “scaling-up” the voltage via transformer, and the resistance is made as low as possible by choice of alloy while still remaining economically viable. With low current and resistance, $i^2R$ remains small, obviously. However, these losses increase with length and for remote buildings only tens of miles from the generation station, losses in generated power can approach 50%. Only if resistance is reduced to virtually nothing can near lossless lines be achieved. Of course, the logistics of keeping superconducting would be daunting say the least; even assuming underground lines, a practical solution is elusive.

While the aforementioned applications of superconductors are interesting and good for public relations, less trendy and visible applications are more practically implemented and have more viably priced production and development price tags. It is these applications – in the realm of microelectronics – that this work focuses on. Many examples of these uses exploit the discovery of the Josephson junction.

A Josephson junction is essentially two slabs of superconductor separated by an insulator (although a piece of metal will work too, and can be on the order of microns in thickness rather than angstroms) through which, incredibly small currents can flow. A popular use of the Josephson junction effect is in superconducting quantum interference devices, or SQUIDs. The name describes the operation of the device: it is made from superconductors, are sensitive
enough to measure single flux quanta [16], and take measurements by means of the creation of interference [17] with constant currents. The two types of SQUID are DC and RF, with DC being the more sensitive of the two and both can be made with conventional superconductors such as niobium and lead as well as high temperature superconductors such as YBCO and BSCCO (bismuth strontium calcium copper oxide).

Figure 3.1.1: Layout of a SQUID. The magnetic field to be measured passes through the ring and induces a current either clockwise, or counterclockwise, creating a measureable current differential. The two patches of insulating material create Josephson junctions.

In the above device (figure 3.1.1), the Cooper pair electrons are all in phase – or “phase coherent” – and therefore, even after passing through the insulator, the wave functions of the Cooper pairs will be in phase. Since the current is proportional to the phase difference of the wave function of the Cooper pair electrons, an induced current causing a potential differential between either side of the junctions will lead to a measurable difference in oscillations [18].

Another use of the Josephson junction is the superconducting transistor. While different types of transistors have been fabricated, such as single electron transistors [19], the general idea is similar to that of a conventional transistor. Current will flow across the Josephson junction even
without applied voltage on either side of the junction (applied voltage will cause very high frequency oscillations as with the SQUID). To the junction is added a gate that allows for manipulation of said junction (Figure 3.1.2) to a great degree via capacitive coupling.

![General layout of a Josephson junction transistor](image)

**Figure 3.1.2:** General layout of a Josephson junction transistor [20]. Note that in this image, lead is the superconductor being use, but that any superconductor – even HTSCs – can be used.

Less superconductor-specific devices that mimic the operation of conventional microelectronics have been fabricated as well, which include, but are not limited to, microstrip impedance transformers[21], microstrip resonators [22], and even low noise amplifiers[23].

### 3.2 State of SOS Technology

In the realm of microelectronic technology, there are not many categories of device that have not or would not benefit from thin film silicon-on-sapphire electronics. Thin film silicon-on-sapphire is not new, nor is the aspiration to utilize it in an array of microelectronic devices[24].

The qualities of silicon-on-insulator (SOI) substrates – and specifically silicon-on-sapphire (SOS) – include first and foremost high carrier mobility which, among other things, allows for much “faster” transistors. Furthermore, it is possible with a thin-film on an insulator to be fully depleted, meaning that the gate voltage can fully control the channel giving much lower losses and thus very low power consumption devices. The much lower parasitic capacitance from
using an insulator rather than bulk silicon also increases speed by limiting said parasitics, as well as improving isolation among individual components.

Hewlett Packard was perhaps responsible for the first commercial use of SOS technology, the appeal being very low power consumption which was ideal for the calculators they used it in [1]. However, it was not until later when a method to create truly ultra thin-film SOS that the appeal for use in high speed and RF applications peaked. While it still does not compete with some of the more exotic compound semiconductors like indium phosphide when it comes to performance benchmarks such as electron mobility, it is both scalable and compatible with current and prolific CMOS fabrication processes [25], making them an economically viable option for chip manufacturers. For that reason, combined with the very low losses at radio frequencies, that silicon on sapphire substrates are one of the most preferred substrates for high-performance low-power RF applications.

Some specific components that have been integrated into both civilian and military devices are SOS-based phase-locked loops benefiting greatly from very low noise inherent in SOS and RF switches benefiting from high linearity over a large bandwidth [26].

It may happen that the reason for using p-type silicon for this work is born of the UltraCMOS technology reference above, which exists in large part because of the higher mobility experienced by, otherwise lower mobility holes. Obviously, making any field effect transistor on p-type silicon is typically sub-optimal due mostly to the fractional mobility of holes in comparison to electrons. Since the goal of this work is not to create any particular device performing to any particular standard – and certainly not to create the fastest switching transistor or highest quality factor resonator – but rather to prove the thesis that YBCO can be processed side-by-side with SOS electronics, it stands to reason that the terminal goal is to utilize a p-doped substrate in some capacity, possibly one similar to UltraCMOS.
Chapter 4

4.1 YBCO Processing Considerations

In order to determine the precise order of the design process, the effect of each processing material on both YBCO and silicon must be considered, as well as the effect of any given processing material on any residual processing material used before it. This leads to a matrix-like examination of cause and effect. An attempt is made in the following pages to organize the examination into a coherent and logical progression.

The YBCO structure – a microwave resonator – will be etched in a saturated ethylenediaminetetraacetic acid (henceforth referred to as EDTA as it is now in good form to abbreviate, and the whole thing is just a mouthful otherwise). EDTA has been shown to etch YBCO very well without any significant effect on most commonly used YBCO substrates such as SrTiO$_3$, sapphire, and MgO [27]. Additionally, since EDTA is a chelating agent, it selectively bonds to metal ions and leaves the neighboring silicon unaltered.

Other etchants that were considered were nitric acid and hydrochloric acid, both of which have been shown to etch YBCO [28] albeit at potentially very rapid rates (>0.5 μm/minute). The resonator that will be fabricated is gap-coupled with the gap being five microns, and will thus require finer feature sizes than can be achieved at the aforementioned rates.

The mechanism by which EDTA etches YBCO is chelation with EDTA being the chelating agent or chelant. A chelating agent is a ligand that preferentially bonds to a metal ion creating a chelate complex. When an EDTA molecule bonds with a copper (II), or Cu$^{2+}$, ion it creates a very strong complex [29] which insures that once a copper atom is pulled from the YBCO – or specifically the copper-oxide plane – it will have no interaction, undesirable or otherwise, with the rest of the substrate as the acid continues to etch the remainder of the superconducting ceramic.
Figure 4.1.1: “M” denotes the metal ion and the figure shows the way that the EDTA bonds to it, rendering its conductivity very low. In the YBCO etching, the EDTA bonds to a copper atom causing the YBCO to dissociate and etch away in the saturated EDTA solution \[30\].

The benefits to using a chelating agent as the etchant for the YBCO extend beyond its affinity for bonding with copper ions. A chelating ligand bonds preferentially to a central metal atom. As such, the photoresist that will be used to pattern the resonator will be unaffected by the EDTA as it contains no metal ions. As shown in figure 4.1.2, the Shipley 1818 positive photoresist is primarily composed of organic non-metal elements, including solvents, carbogens, and the photoactive compound having the chemical structure $C_{10}H_{6}N_2O$.

Based on surface resistivity measurements, the silicon samples are p-doped at a concentration of roughly $10^{17}/\text{cm}^3$. The p-doping is achieved by boron ion implantation. As such, the interaction between EDTA and boron is of interest on samples containing doped silicon alongside YBCO. As this is a
Figure 4.1.2a: The majority of the photoresist – the solvent…

Figure 4.1.2b: The second most predominant compound, the binder…

Figure 4.1.2c: And the photoactive compound, none of which contain metal ions to be dissociated by the chelating ligand [31].

new area of research, empirical knowledge of EDTA’s interaction with boron is sparse. Using a p-doped silicon sample similar to the sample that will undergo side-by-side processing with YBCO, a surface resistivity measurement was taken following an RCA clean. The sample was then immediately immersed in an EDTA-saturated solution of deionized water and frequently agitated for twenty minutes. After the twenty minutes, the sample was rinsed. Additionally, to
eliminate any possibility of skewed results due to slight wet oxidation, the sample was RCA cleaned once more before re-measuring surface resistivity.

Resistivity was measured by placing copper tape along the edges of a small square silicon sample and applying a constant potential to said tape. Then, assuming that most current flows along the surface of the thin film, the current between the copper tape electrodes is measured, along with the distance between the electrodes and the length of edge of the sample (equivalent to the length of the electrodes).

The difference in surface resistivity after significant exposure to EDTA is approximately 1.1%. That is, the surface resistivity increased from $9.1 \Omega/cm$ to $9.2 \Omega/cm$. This is certainly within acceptable limits. Additionally, with proper mask design, the p-doped silicon’s exposure to the chelating agent should be minimal at most.

While empirical evidence shows that, even though sapphire is made up of aluminum atoms – with a chemical structure of $\text{Al}_2\text{O}_3$ – sapphire is unaffected by chelation (and is rather resilient to buffered oxide etching solutions). Aluminum thin films, however, might be at risk. Theoretically, the native oxide that forms on an aluminum film should protect it, but at only angstroms of thickness, exposure to a chelating agent presents an unnecessary risk. Due to the potential for corrosion on of aluminum by EDTA [32], it was prudent to pursue a process in which the YBCO was fully developed prior to any silicon processing, thus eliminating any contact of aluminum (or titanium) with EDTA.

### 4.2 Annealing Considerations

Pre-oxygenation is the terminal process under which YBCO must go. The process is similar to dry oxidation of silicon by which, with heat as a catalyst creating a controlled environment where silicon dioxide can form. Pre-oxygenation for YBCO is a dry heat process in which pure oxygen is circulated through a previously sealed and evacuated furnace set to $500^\circ C$ for 30 minutes. The empirical formula of the superconductor in this work is actually $\text{YBa}_2\text{Cu}_3\text{O}_7-\delta$, where $\delta$ can
range from zero to one. However, when $\delta$ is greater than 0.8 – and in some cases, 0.2 – [33], the YBCO is not superconducting. That is, when $\delta$ is high, oxygen content in the YBCO is too low for the cuprous oxide to be superconducting. Upon undergoing pre-oxygenation, the structure of the YBCO changes from a tetragonal perovskite to an orthorhombic perovskite and begins reliably superconducting when $\delta$ drops below 0.2, which seems to occur best at a temperature around 450°C to 500°C for the initial pre-oxygenation, but can be achieved at much lower temperatures for re-oxygenation. This seems to suggest that the structure has a “memory” feature [34].

While 500°C is not comparatively high, it warrants thought on the process’s impact on the other materials on the substrate with the YBCO undergoes this critical, terminal process.

As previously mentioned, a dry oxygen environment will oxidize silicon, albeit slowly. Regardless of oxygenation rate, it will be prudent to plan for the source and drain Ohmic contacts to be deposited prior to pre-oxygenation as minor annealing processes have actually been shown to improve the linearity of the current-voltage relationship [35]. However, the silicon side of the wafer should be masked during the process to prevent oxidizing of silicon or titanium and thereby create need for an unnecessary additional etching step.

Furthermore, the aluminum deposition for the gate material – by thermal evaporation or sputtering – is best saved for the final process. During either metal deposition method, heating is not significant. Obviously, all substrate real estate will be covered by photoresist while the aluminum is deposited so no contaminants will reach the source, drain, or superconducting patterning. The reason that gate deposition should be last is that under any annealing process such as pre-oxygenation or even the heat caused by RF sputtering, aluminum might diffuse into silicon which will not only dope the silicon, but make the metal-semiconductor contact less rectifying and more Ohmic – a decidedly bad idea for the gate of a MESFET.
4.3 Silicon Processing Considerations

Having addressed the effects of YBCO processing, including geometric patterning and pre-oxygenation, on the order of processing, the last item that should be considered is any effect that the various silicon processing procedures have on YBCO or sapphire.

First and foremost, it is prudent to choose processes that don’t involve extreme temperatures. For example, it is common for thermal annealing to be used to create Ohmic contacts between titanium and silicon interfaces, where the silicon diffuses upwards into the titanium to create titanium silicide (TiSi$_2$). However, these processes can exceed 700°C and YBCO’s resilience to high temperature treatments may be questionable – it is not a well researched topic. For that reason, using sputtering to deposit TiSi$_2$ directly as an Ohmic contact, rather than pure titanium seems wise.

Obviously, the superconducting portion of the wafer must be masked during any of the silicon processes and it is reasonable to assume that using photoresist to do so should have minimal impact on the YBCO as patterning on successfully fabricated devices has been detailed in [36] and [37] and includes using various photoresists including – but not limited to – the Shipley 1818 which is the resist planned for use in this work.
Another concern should be aggressive chemical use – namely hydrofluoric acid (HF) for wafer cleaning primarily, though potentially needed in removing the native oxide that can form from exposure to regular environmental conditions. Since it is established that both patterning on YBCO via photolithography is harmless to the YBCO, and that Shipley 1818 photoresist is a
resilient mask for HF etching through silicon dioxide for various metal-oxide-semiconductor fabrication technologies, it stands to reason that any HF etching that needs to be done on a substrate occupied by YBCO can safely be executed without risk to the integrity of the superconductor.

4.4 Order of Processes

From the perspective of protecting materials from hostile processes and chemicals, the best approach seems to be to pattern and deposit the rectifying contact last to prevent aluminum diffusion into the channel, and precede it immediately by pre-oxygenation of the YBCO. When patterning the aluminum Schottky contact prior to deposition, a layer of photoresist is applied to the superconducting portion of the wafer and left on during the metal evaporation process.

The first step should be patterning of YBCO by EDTA etching. While it is not a thoroughly researched topic, it seems that – as EDTA is a chelation agent – and as TiSi$_2$ obviously has metal ions, that it (the titanium) might thus be susceptible to becoming the central atom of the chelate complex. That is, the EDTA might undesirably bond to the titanium. Obviously, just as with every process, the source and drain contacts would be protected by a photoresist film; there is just no need to create the potential for a negative interaction.

The last step of course, should be the gate deposition. Any processing after the deposition might lead to diffusion of aluminum atoms and degradation of the efficacy of the Schottky barrier, if said processing involves any intentional or unintentional heat. Prior to gate metal deposition and after drain and source patterning and deposition, resonator patterning and pre-oxygenation must be carried out. The patterning consists of photolithographic covering and etching of the YBCO and pre-oxygenation was described in this chapter in section two.
Figure 4.4.1a: Detailed description of processing steps designed for minimally hostile interaction of patterning chemicals and heat with YBCO and silicon’s respective devices. Bold text indicated silicon based processing, italic indicates YBCO based processing. YBCO is covered in photoresist during initial clean and native oxide removal.

1. Acetone & IPA clean
2. Apply positive resist
3. Pre-bake resist
4. Apply first mask (opens Source and Drain)
5. Develop exposed resist
6. RF sputter TiSi₂
7. Lift-off TiSi₂
8. Apply positive resist
9. Pre-bake resist
10. Apply second mask (patterns High-T, resonator)
11. Develop exposed resist (Silicon remains covered)
12. Etch YBCO
13. Lift-off resist
14. Apply positive resist
15. Pre-bake resist
16. Apply 3rd mask (covers silicon half of wafer)
17. Develop exposed resist
18. Pre-oxygenate YBCO

19. Strip resist
20. Apply positive resist
21. Pre-bake resist
22. Apply 4th mask (opens Gate contact)
23. Develop exposed resist
24. RF Sputter Aluminum

25. Lift-off resist

Figure 4.4.2b: Detailed description of processing steps designed for minimally hostile interaction of patterning chemicals and heat with YBCO and silicon's respective devices.
Chapter 5

5.1 Resonator Design

To prove the processing procedure leaves the YBCO in sound shape, a simple piece of microwave circuitry is designed, fabricated, and characterized to verify performance is acceptably undiminished by processing. To do so, a basic half wave resonator will prove the concept. In the past, resonators using coplanar wave guide transmission lines have yielded good results when only one side of the substrate has a YBCO thin film[38]. To investigate a less reported topology, a microstrip line resonator is designed with a metal ground plane. While aluminum does not superconduct at temperatures above 1-2K, other normal metals have performed well as the ground plane for YBCO transmission lines, such as gold [39] and [40].

For any resonator fabricated from YBCO, since the quality factor is the ratio of stored energy to dissipated power scaled by the frequency or,

$$Q = \frac{\omega W_{\text{stored}}}{P_{\text{dissipated}}}$$  \hspace{1cm} [5.1-1a]

And since $P_{\text{dissipated}}$ is proportional to the resistance (R) of the component, or

$$P_{\text{loss}} = i^2R$$  \hspace{1cm} [5.1-1b]

The quality factor (Q) of the superconducting resonator is expected to be near infinity as R will approach zero at the device’s operating temperature and Q is inversely proportional to R. From [41], for a transmission line resonator,

$$Q = \frac{\beta}{2\alpha}$$  \hspace{1cm} [5.1-2a]

where $\beta$ is the propagation constant and $\alpha$ is the attenuation constant and a sum of the conductor loss ($\alpha_c$) and the dielectric loss ($\alpha_d$).
\[ \alpha = \alpha_c + \alpha_d \]  \[5.1-2b\]

Dielectric losses remain relatively constant, but the conductor losses will decrease with temperature as a function of the decreasing surface resistivity \( R_s \) of the YBCO. With \( R_s \) decreasing to zero and \( \beta \) remaining constant, the trend of the quality factor due to temperature is much like the inverse of the resistivity due to temperature.

Working with 10mmx10mm substrates, the lowest frequency will be somewhere above 4.9GHz from

\[ f_0 = \frac{c}{2L\sqrt{\varepsilon_r}} \]  \[5.1-3\]

For structural purposes, the patch was designed such that plenty of room is available on either side (lateral) of the patch. That is, since the resonator is not being designed for any specific application, the focus may be on geometry that is most conducive to the size and shape of the wafer and characterization fitting to the test configuration. A patch approximately 4.3mm in length works well and corresponds to a resonant frequency of 11.6GHz by equation 5.1-3. Designing for a five micron gap between feed lines and patch to induce good coupling, the feed lines will extend approximately 2.86mm to the edge of the wafer.

Sapphire is anisotropic and while it was fairly certain that the samples obtained were fabricated and cut such that the surface was parallel to the c-axis, the measurements verified it (see Chapter 7). Had the same design been fabricated out of perpendicular c-axis sapphire, the resonant frequency would have occurred closer to 12.8GHz. Since resonant frequency is not dependent on conductivity the same technique used for copper conductors can be – and was – used to design the YBCO resonator. Furthermore, sapphire’s dielectric constant changes very little with drops in temperature occurring below room temperature [42] and remains constant from the kilohertz range up into gigahertz territory [43].
The widths of the feed lines are calculated by equation 7.1-4 to approximately match the 50Ω impedance of the 3.5mm coaxial lines from the vector network analyzer. However, so that the probe contacted the feed lines well, they were made slightly wider, thus lowering the feed line impedance a few Ohms. The reflection caused by the slight intentional mismatch will account for a slightly lower loaded quality factor, calculated and measured in the results section (chapter 7). This design decision does not adversely affect the goal of the resonator, which is simply to prove that the process is effective, the only requirement of which is to produce a well-performing resonator; the goal is not to fabricate and characterize the best resonator possible – otherwise, perfect matching and better geometry would be priority over creating an optimally designed device for characterization.

5.2 Schottky Contact

A transistor design is proposed as a starting point for future work. All of the processing steps are chosen to avoid degradation of the YBCO and the majority of the steps have been proven effective towards transistor creation and compatible with YBCO processing.

The material considerations for a design of a transistor start with determining a suitable metal for a Schottky contact and the deposition method that fits within the constraints of YBCO processing. Since there are a variety of deposition options for most elemental metals, the more important aspect is the work function of the metal (Φm). For n-type substrates with excess electron carriers, the creation of a Schottky contact is straightforward as the requirements is for the work function of the metal to be slightly above that of the doped silicon. However, the metal used for this Schottky contact must have a slightly lower work function than the silicon since it is doped with a p-type material.

Before a metal can be selected, computation for the work function is required:
Figure 5.2.1: Band diagram for p-type semiconductor with values for electron affinity ($\chi_s$), work function of the semiconductor ($\Phi_{p, Si}$), bandgap ($E_g$), conduction and valence bands ($E_c$ & $E_v$), intrinsic Fermi level ($E_{Fi}$) and doped Fermi level ($E_{Fs}$)

From Figure 5.2.1, since the work function is the amount of energy needed to move an electron from the Fermi level ($E_F$) to vacuum, the work function of an arbitrary p-type semiconductor is

$$\Phi_{p, Si} = \chi_s + (E_g - [E_{Fi} - E_{Fs}])$$ \hspace{1cm} [5.2-1]

The electron affinity ($\chi_s$), the band gap ($E_g$), and the intrinsic Fermi level ($E_{Fi}$), can all be found in any solid state electronics text book such as [44]. The doped Fermi level ($E_{Fs}$) is,

$$E_{Fs} = \frac{kT}{q} \ln \left( \frac{N_A}{n_i} \right)$$ \hspace{1cm} [5.2-2]

The approximate concentration of acceptor atoms for the silicon-on-sapphire wafers ($N_A$) is $10^{17}$ cm$^{-3}$ and the intrinsic carrier concentration ($n_i$) is $1.45 \times 10^{10}$ cm$^{-3}$ at room temperature, which gives a doped Fermi energy of about $0.408$ eV at room temperature from equation 5.2-2. Referring back to equation 5.2-1, having solved equation 5.2-2 for the Fermi energy of the
doped silicon, the work function for the p-doped silicon ($\Phi_{p,\text{Si}}$) can be calculated. The electron affinity (4.01eV) is drawn from [44] and the bandgap and intrinsic Fermi value of silicon are ingrained in the mind of every electrical engineer – 1.12eV and 0.56eV respectively – and so the work function is then approximately $4.98\text{eV}$ based on a doping assumption of $10^{17}\text{cm}^{-3}$. This computation agrees well with measured values of 4.91eV from [45].

From [46] the work function of aluminum can range from 4.06eV – 4.26eV. However, most solid state electronics books and references put the value closer to 4.28eV – 4.30eV and so the low end of that range of values is used to estimate the Schottky barrier height. By examination of the band diagrams (figure 5.2.2a-b) the barrier height is approximately

$$\Phi_B = \Phi_M - \chi_S - E_g$$

[5.2-3]
which gives -0.85eV; a negative potential is expected for a Schottky barrier on p-type material. That is, rather than a build-up of elections, a lack of electrons (or build-up of holes if thinking in the abstract) is necessary.

Figure 5.2.2b: When the metal is deposited on the semiconductor, band-bending occurs so that Fermi levels align and thermal equilibrium is reached. \( \Phi_B \) represents the barrier height.

The calculated value of the barrier height is -0.85eV, but empirical data of measured barrier heights indicates values closer to -0.57eV to -0.58eV for very carefully prepared samples [47]. In fact, the same literature suggests that barrier height depends more on sample preparation than it does doping concentration.

Whether the barrier is closer to the theoretical value calculated by equation 5.2-3 or to the empirical data from [47], it suffices for a Schottky contact. In fact, the measured data in chapter 7 is consistent with empirical data.

5.3 Ohmic Contact

Non-rectifying contacts make up the balance of the design considerations and comprise the source and drain of the MESFET. For a p-type substrate, a non-rectifying contact – or Ohmic
contact – requires that resistance to majority carrier flow (holes in this case) not need to overcome large barriers. That is to say that the contact should behave consistently regardless of the polarity of the potential applied to it.

In the literature, one of the most common materials for creating Ohmic contacts on p-type silicon is titanium silicide [48]. In [49], titanium is deposited on silicon and then annealed around 700°C which causes silicon to diffuse into titanium to create a Ti/TiSi₂/Si transition, and a good Ohmic contact. There are similar and well documented processes for creating an Ohmic contact out of titanium silicide using various annealing methods that are more conventional than the lamp anneal from above. While this is an appealing option for the simple ease of the process, it also requires that the substrate be heated to a temperature that might disagree with the YBCO, which can be a finicky companion to silicon for yet another reason – the formation of Ohmic contacts.

However, radio frequency (RF) sputtering technology has progressed to the point that compounds such as titanium silicide and silicon dioxide can be purchased in target form and sputtered directly just as copper, aluminum, or gold would be. As such, the design process laid out in this work includes RF sputtering a masked and patterned substrate with a titanium silicide (TiSi₂) target for the creation of Ohmic contacts. The barrier height for the Ohmic contact created would presumably be low, but data for Ohmic contact barrier height for silicon-silicide contacts is typically empirical and should be measured upon creation of this contact.

5.4 Theoretical Schottky Characteristics

Since the transistor is designed, it is prudent to compute a few operational values to use as markers for success – should the transistor be fabricated in future works. Easily measured operational values are most ideal; those chosen for theoretical determination in this section will
cover some values verifying DC current-voltage relationships. For DC operation, pinch-off voltage \( (V_p) \) would be valuable.

The threshold – or turn-on – voltage for a MESFET is calculated similarly to the threshold voltage for a MOSFET so that the same widely used and accepted formulae may be used for both; also, \( V_{TH} \) relies on some of the gate contact properties computed in Chapter 5, Section 2. Specifically, the doping of the p-type silicon is important, as well as the thickness of the doped region – equivalent to the distance between the Schottky contact and the insulating sapphire material – and the dielectric properties of silicon. The built-in potential is the primary aspect of the aluminum-silicon contact that is important to the threshold voltage. As \( \Phi_B \) is only predictable to a range of values, so too will the threshold voltage be. The aforementioned values relate to each other by the formula:

\[
V_{TH} = \Phi_B - V_p
\]  \[5.3-1a\]

Where \( V_p \) is the pinch-off voltage and described by

\[
V_p = \frac{qN_d d^2}{2\varepsilon_0\varepsilon_r}
\]  \[5.3-1b\]

The pinch-off voltage then is

\[
V_p = \frac{(1.6 \times 10^{-19} C)(1 \times 10^{17} \text{ cm}^{-3})(0.5 \times 10^{-4} \text{ cm})}{2(11.68)(8.85 \times 10^{-14} F/cm)} = 19.3V
\]

Assuming the same thickness of substrate – and the substrate was relatively thick – if the fabricated transistor’s DC voltage limits are tested, pinch-off should occur at the rather large value of 19.3V.
Note that equations 5.1.3a-b are actually technically the equations for pinch-off voltage in MOSFETs, but that, except for very unique situations, can be used perfectly finely to find the theoretical pinch-off voltage of a MESFET as well [50].
6.1 Calibration Verification

As noted, design was actually a fluid process, evolving as a result of external exacerbation inherent in the measurement and characterization configuration. In some instances, the redesign and modification could be said to have happened in parallel with characterization. The superconductor characterizing test bench is configured as follows:

Figure 6.1.1a: A photograph of the compressor and the vacuum pump portion of the test configuration
Figure 6.1.1b: The temperature controller/reader and pressure gauge portion of the test configuration.

Figure 6.1.1c: The cold finger and test chamber portion of the test configuration.
Figure 6.1.1d: The test chamber portion of the configuration with ports 1 and 2 labeled.

Figure 6.1.1e: Diagram of Test Configuration for Characterization of High T_c Superconducting Microwave Devices
Within the cold chamber the spring loaded jig is secured with the sample in place.

Figure 6.1.2a: Top view of jig. The jig is secured in the test chamber in this picture.

Figure 6.1.2b: Side-view of test jig.
Figure 6.1.2c: Schematic drawing of the sample used to hold the jig in place.

The jig is made primarily of brass which has a conductivity on the order of \(10^7\) — and of a similar magnitude of aluminum and copper. As detailed in the design section, the resonator uses distributed element microstrip transmission lines and would thus rely on a ground plane with significantly high conductivity. Due to material constraints the ground plane could not be YBCO and, as such, a smooth piece of copper tape affixed to the jig over the base on which the sample would sit would suffice — in theory. It would not only prevent another processing step, it would make use of one of the most conductive metals used in microelectronics.

However, the HC-4 compressor becomes quite turbulent as the temperature in the cold finger drops below roughly 100 Kelvins. This is due in large part to contaminants that build up in the compressor which is an inevitable part of prolonged operation [51]. Even sans contaminants (which is only common in brand new systems which are no longer made — to the disappointment of vintage compressor enthusiasts everywhere), there are perturbations present which serve as
external and undesirable disturbances in the form of high amplitude vibrations. The resulting characteristic scattering parameter, $S11$, shows no discernable peak at the design frequency as shown in figure 6.1.3a-c.

Figure 6.1.3a: Scattering parameter, $S11$, shows a very small dip (indicates a small quality factor, $Q$), not consistent with expected results of a resonator fabricated from a material that should have near zero resistance.
Figure 6.1.3b: For a different calibration, over a shorter range of frequencies, and at the same substrate temperature, it is obvious that the vibrations cause loss in contact and variation in performance by the discrepancies between the two traces.
Figure 6.1.3c: This plot of S11 shows the same unreliable behavior as that exhibited in 6.1.3b, albeit, at a higher frequency.

While poor results are to be expected with a system having so much parasitic vibration uncompensated for, they were not foreseen. After manually checking calibrations (Figure 6.1.4a-d), verifying continuity through jig ports (Figure 6.1.5a-d), and physically examining the sample, the consensus was that the vibrations in the test set up were making characterization of the resonator impossible. Adjustments were required.
Figure 6.1.4a: S11 is relatively flat at all frequencies over this particular set of calibrated frequencies. The same is true for calibrated frequencies up to 14GHz.

Figure 6.1.4b: The magnitude of S22 also shows good calibration for this set of frequencies, not deviating from 0dB by more than +/- 0.5dB.
Figure 6.1.4c: The magnitude of the scattering parameter, $S_{21}$, is less than $-45\text{dB}$, showing good isolation between port 1 and port 2.

Figure 6.1.4d: $S_{12}$ measures similarly to $S_{21}$ and thus the network shows good reciprocity.
Figure 6.1.5a: With the ports 1 & 2 shorted together, the low magnitude of S11 indicates that there is little reflection – and thus, low return loss – in the calibrated network.

Figure 6.1.5b: Similarly S22’s low magnitude indicates low signal reflection and return loss.
Figure 6.1.5c: The near 0dB value of S21 across this particular set of calibrated frequencies show that a good standard was used when calibrating “thru” signal values, and thus attenuation is minimal due to compensation for line lengths.

Figure 6.1.5d: The signal also shows near zero signal attenuation in the reversed network as well.
6.2 Resonator, Jig, and Test Configuration Troubleshooting

The vibrations inherent in a compressor driven system such as the one in figure 6.1.1a-e cause one of two problems when using a microstrip topology in conjunction with the spring loaded jig in figure 6.1.2a-c.

1) The vibrations cause intermittent separation of the sample from the ground plane on which it was simply “placed.”

2) The contacts to the feed lines might lose contact by way of very slight, yet significant, thermal contraction.

![Diagram](image)

*Figure 6.2.1a: This magnified view of the point at which the probe makes contact shows that contact is only slight, even at room temperature.*
Figure 6.2.1b: The contraction of the probe at very cold temperatures may cause a separation of mere microns – enough to prevent consistent and reliable test results.

While either of the two aforementioned problems would likely cause poor test results, a combination of the two would insure it. The diminished likelihood of good test results is compounded by the fact that an HP8350 signal generator is used, not allowing the control in frequency sweeps of a synthesizer such as the HP83752A.

While it seems that a simple solution to the first problem might be to apply copper tape to the bottom of the substrate rather than the jig-base upon which the substrate is placed, there is error in the idea which fails to regard the non-ideal characteristics of the system. It relies on the surface of the sapphire (or Lanthanum Oxide [LAO] as the case may be), to be an ideally smooth plane. Additionally, even as the purpose of the resonator fabrication is simply to prove a concept in processing, applying copper tape to the sapphire would never pass as a practical process to be used on any scale of fabrication. The lack of practicality of tape application in a processing environment is obvious, but the issue of the surface topology of the sapphire should be addressed.
First and foremost, some of the transistor processing mentioned in prior sections involves the use of hydrofluoric acid (HF), used for its keen preference for etching silicon dioxide (SiO$_2$) over most other materials used in this work. However, it doesn’t show total amnesty to sapphire – it is after all, an oxide (Al$_2$O$_3$). As etching often happens, HF may attack a slight imperfection in the sapphire more aggressively than the rest of the surface, albeit still very mildly in comparison to the SiO$_2$. This tendency may leave a small area of the sapphire substrate slightly thinner than the majority, a small dent in an otherwise smooth surface. As such, it cannot be assumed that the surface is perfectly planar.

The effect of attempting to use a copper tape on an uneven surface is the potential (and likelihood) that a pocket of air would be created between the would-be copper ground plane and the sapphire substrate. Quantitatively, the electric field between the ground and the microstrip line would pass through a dielectric with a permittivity of anywhere between 9 and 11 depending on the orientation of the sapphire, to air, having a permittivity of 1 before reaching the copper ground. The result is potential field reflection or diversion, creating possible perturbation in the current on the microstrip line. Additionally, as the propagation along the microstrip line is limited by the propagation of the electric and magnetic fields – and the field’s propagation is reliant on the dielectric of the medium through which it travels – the signal may suffer further perturbation by random pockets of a low dielectric medium (air) between the sapphire and the would-be-copper-tape-ground.

![Diagram](image_url)

**Figure 6.2.2:** The electric field lines pass through the sapphire to the copper-tape ground plane; any air pockets between the tape and the sapphire will perturb the signal traveling on the YBCO microstrip line.
The second problem of losing contact between the jig and the microstrip feed-lines on the sample may occur due to the coaxial probe lines contracting at low temperatures. That is, copper alloy such as that found in coaxial cable becomes both more rigid and more dense at low temperatures, as too may the dielectric surrounding it. As contact between the feed-line and the coaxial probe is only slight to begin with, a stiffening of the dielectric or shrinkage of the copper would cause the probe to “straighten” or shrink. Even barring this effect which may be too slight to make a difference anyway (though it is not practically measureable) – the vibrations are enough to prevent constant contact at both probes.

The result would be something akin to gap coupling the coaxial probes to the feed-lines, possibly creating some very troubling parasitic. To predict the effect of gap-coupling the coaxial connectors to the microstrip feed lines, a sample resonator was simulated similar in design to the superconducting resonator, with ideal contact made between the coaxial connectors and the feed lines. Then, small gaps at each terminal were introduced and the simulation indicated that adding additional gaps to a resonator of this topology greatly decreased the magnitude of S11 at the center frequency by over 35dB; much worse can be expected in actual measured data. This is a consequence of a versatile test jig: a general lack of permanent contact.
Figure 6.2.3a: The half-wave resonator with perfected contact made at the probes shows very good resonance.

Figure 6.2.3b: Compared to Figure 6.2.3a of a resonator with ideal contacts, the frequency is quite similar (only 20MHz less), but the significantly decreased magnitude (more than 30dB less) suggests a large amount of loss from poor contact.

With two ports, that’s a total of three potential losses of contact in the resonator that must be addressed, as they will be in the next section, in the order in which they were presented.
6.3 Ground Plane

The options for the ground plane constrained by the aforementioned conditions are few; metal deposition is the most effective, feasible, and non-destructive option.

The method of deposition is of significant importance. For compatibility with other processing steps, as well as concern for unintended introduction of oxygen into the YBCO, the temperature must not be too high. Most methods involve an increase in temperature so one that has a high deposition rate is also desirable. Thermal deposition is mild enough in environmental harshness that it can be used for lift-off methods – as well as simple and available. While it lacks the precision of deposition thickness that RF sputtering has, it makes up for in speed and simplicity. Furthermore, for this deposition all that is needed for success is a continuous, unbroken ground plane – easily achieved with thermal deposition. The system used created an aluminum layer approximately 0.6μm thick in a deposition time of less than 20 seconds, during which, the temperature never exceeded 200°C.

![Surface Profile Diagram](image)

*Figure 6.3.1: A rough sketch of the surface profile, copied from a Dektak IIA profile covering the area shadowed during the thermal evaporation deposition of the aluminum ground plane.*

The 10mmx10mm sample was affixed to a non-reactive, non-outgassing piece of quartz glass. For the most accurate measurement of metal thickness, the Dektak IIA was used on the quartz...
stage. The probe was programmed to run 12mm with the start and end point set to 1mm to either side of the “shadow” created by the 10mm substrate. A second probe path was set to scan on a 2mm path with a start and end point immediately before and after the edge of the shadow created by the substrate. In both cases, the thickness was 500-800nm.

As an aside, this same method would be good for creating the gate contact or aluminum layers on top of the TiSi₂, reason being, the metal is of appropriate thickness for lift-off as the photoresist thickness is spun to approximately 1.25µm to 1.50µm. Additionally, the relatively low temperature that the substrate is kept to (less than 200°C) keeps the S1818 photoresist from burning and allows for a clean lift-off process.

6.4 Probe Contact

Having solved the issue of intermittent loss of contact between the ground plane and the sapphire, there remains the issue of probe contact.

There are advantages to the spring loaded contacts, the most significant of which is the ability to quickly swap samples. However, characterization of one sample takes 6-7 hours at minimum, making the appeal of quickly swapping a sample out moot. Additionally, the threat of poor contact or complete loss of contact occurring at any point during the process results in 4-6 hours of evacuation and cooling that is wasted. Also, as the sample is sealed in an airtight chamber and surrounded by a metal shell, it is not possible to observe visually if the sample has lost contact with the probes. If not visually, the only way to tell is to observe S11 over the frequency range containing the resonant frequency (designed to be 10Ghz in this case). However, this is only possible after hours of cooling and pumping, once the sample has dropped below the critical temperature and becomes superconducting, rather than insulating.

The obvious solution is to make the contacts more permanent. A mechanical forcing down of the springs was attempted with no success. Another bane of the test setup – it is known by
examination under a 10x Bausch-Lomb loupe that only slight contact is made between the feedlines and the probe – though testing for electrical continuity is not possible at room temperature. While it is known that physical contact was made at the beginning of the test, it was lost consistently over the course of many tests. Less desirable, though necessary, is some form of semi-permanent adhesive.

At the forefront of conducting electronic adhesives is solder. Solder is desirable for it is known to be conductive down to cryogenic temperatures and becomes superconducting between 6 and 15K depending on the solder. Additionaly, it is easily manipulated. As solder is the optimal solution to another non-optimal test configuration quirk, it is, of course, not an option. Solder only effectively bonds metal to metal. YBCO is a cuprous oxide – a ceramic – and thus not solderable to the brass contacts.

Barring solder, the next most desirable choice is an adhesive paint that is both conductive and easy to manipulate on a small scale. There are a number of conductive paints and a few application mechanisms. Due to availability, nickel and silver paints were considered, though other conductive paints include spray-on carbon based paints and brush-on copper based paints.

The method of delivery of the nickel paint was simply painting it on with a fine tipped probe such as a toothpick or awl. Its conductivity is $3.94 \times 10^6 \text{S/m}$ at room temperature. Conductivity of bulk nickel is approximately $50000 \text{S/m}$ at room temperature (for bulk nickel with a grain boundary of $11 \mu\text{m}$)[52] and approximately $133000 \text{S/m}$ at 77K. By extrapolation:

$$\frac{133333@77K}{50000@298K} = \frac{XX@77K}{39370@298K}$$

So,
\[
XX@77K = \frac{133333@77K \times 39370@298K}{50000@298K}
\]

\[XX@77K = 104986[S/m]\]

The silver paint is in the form of, and uses a delivery method of a fine tipped pen. It has a conductivity of \(1.97 \times 10^7\, S/m\) at 293K. Thin film silver has a conductivity of approximately \(5.5 \times 10^7\, S/m\) at 293K and a conductivity that continues to decrease with temperature past \(5.00 \times 10^8\, S/m\) at 60K [53]. So again, by extrapolation, the silver paint should have a conductivity of roughly:

\[
\frac{5 \times 10^8@60K}{5.5 \times 10^7@293K} = \frac{XX@77K}{1.97 \times 10^7@293K}
\]

So,

\[XX@77K = \frac{5 \times 10^8@60K \times 1.97 \times 10^7@293K}{5.5 \times 10^7@293K}\]

\[XX@77K = 1.79 \times 10^8@60K[S/m]\]

For the better conductivity and the more accurate method of application, the silver pen was chosen.

As with most adhesives, this one can be removed with acetone. Whenever the sample had to be removed from the jig, acetone is applied with a cotton swab to free the sample from the contacts. To remove residual silver paint, the sample is immersed in acetone, rubbed with a swab, and immediately dried with nitrogen to prevent residue from forming and prolonged exposure to superconductivity blunting liquid.
Figure 6.4.1: YBCO resonator bound to the feed lines in the jug creating solid and consistent contact

With contacts secured with conductive silver paint and an aluminum ground plane deposited via thermal evaporation, the resonator is as robust as any similarly designed copper resonator on Alumina or Teflon with wire bonded contacts.

6.5 Mask Redesign

There is simply no better way to learn than doing. In circuit design, there are often techniques learned through experience in working with veterans in the field such as multiple AC grounding capacitors, soldering techniques, and designing to account for fabrication tolerances. Similarly, in power engineering, hardware such as relays and breakers have minimum response times and if higher performance breakers (lower response times) are placed before lower performance breakers (higher response times) in the load line, more outages might occur than needed. In printed circuit board design, traces should have spacing (edge-to-edge) of at least one to two times the trace width to minimize cross-talk – a design consideration that is inconvenient to practice, though necessary for a clean and effective performing finished product.

It is not staggering discovery then, that the first mask design contained some non-optimal features, requiring a redesign. The processing steps remained sound with regards to layering,
etching, developing, and deposition. Primarily, the aligning procedure and contact pad design required adjustment. The original alignment mark design as viewed through a microscope lens is shown in figure 6.5.1a and the (perhaps overly simple) alignment mark progression from one processing step to the next is shown in figure 6.5.1b.

Figure 6.5.1a: The dotted line indicates the approximate amount of mask real estate visible through the microscope lens. The white portion (the crosses) indicates the area of the mask that was transparent, while the black is opaque.
Figure 6.5.1b: The progression scheme for aligning the mask with the wafer from one processing step to the next originally consisted of simply making progressively larger openings in the mask for the cross-shaped alignment marks.

In using the Karl Suss MJ3B mask aligner, it became apparent that there were flaws in the original alignment marks and alignment procedure. In figure 6.5.1a, the marks are created – three crosses on each corner – via photoresist development, but the mask shadows all of the area surrounding the alignment marks and the alignment marks themselves.
Figure 6.5.2a: The wafer has three raised crosses from the development of the S1818 photoresist which should be aligned under the cross openings in the mask. However, only the white area in the figure is visible to the operator, thus it is not possible to know which way to adjust the wafer without trial and error bordering on undue pain and suffering.

Adjusting the stage to arrive at the position shown in figure 6.5.2b, from the position shown in figure 6.5.2a, proved nearly impossible with the original mask design.
Figure 6.5.2b: The positioning of the stage underneath the alignment marks positions the stage to within less than one micron of precision.

Additionally, the mask aligner had limitations. The range of the base in the x, y, and rotational fields was limited when the machine was new and further limited by worn springs which apply force counter to the threaded adjustment knobs.

This meant that the mask’s position in the vacuum driven holder must be carefully approximated such that the proper section of the mask is above the minimally maneuverable base, to which the sample is held in place by a vacuum.
Figure 6.5.3: The vacuum stage is the piece of the configuration that is mobile and the prime adjuster for alignment of the sample under the rigidly placed immobile mask.

So that the approximation of the mask placement can be more accurate, the area around the alignment marks on the mask must be transparent so that the elevated alignment marks are visible behind the mask alignment marks. Using this strategy, not only will the starting point from which the alignment procedure will begin be more desirable and optimal, the actual alignment procedure will be much easier and faster. Since photoresist can be rather temperamental, it is best to move from one process to another, minimizing any intermissions in the processing – and being suctioned onto a stage exposed to the environment while being
moved laterally, longitudinally, rotationally and vertically (which should be minimized as repeatedly mashing only slightly firm photoresist into a chrome plated mask can misshape the resist and make mask clean-up arduous) – makes for a turbulent intermission.

Figure 6.5.4: Following generic explanations of design and use of alignment marks [54], a preposterous degree of estimation was necessary in order to place the small wafer precisely in position for the exposure next in the process. In the figure, the squares on the right depict the alignment marks on the mask, with the shaded area being opaque and the white being transparent.
Essentially, a new window was created around the alignment marks so that the elevated alignments marks (visible after developing the Shipley 1818 photoresist in Microposit 351 developer) can be observed as they are moved and centered around the outlines on the mask.

In addition to the redesign of the alignment marks, a rotational component was included in the revision. The three crosses allow for alignment in the x-y plane to a degree of less than one micron, which is well within the minimum dimensional requirements – the smallest dimension being the 1.5\(\mu\)m gap between the gate and drain/source.

However, with the gate widths ranging from 100\(\mu\)m to 500\(\mu\)m, a slight rotational error in alignment could cause the gate to short with the source or drain. Moreover, a slight rotational error may not register on the cross-shaped alignment marks as even from tip-to-tip the crosses still measure less than 130\(\mu\)m.

For rotational alignment, a simple bar of significant length works brilliantly.

![Progression of bar alignment marks](image)

Figure 6.5.5: Progression of bar alignment marks. The shadowed area indicates an opaque part of the mask, while the white section is transparent.

The bar’s length is around 650\(\mu\)m, which allows for alignment with precision of less than 2° – significantly less if the user has good vision and uses only the slightest amount of finesse.
Chapter 7

7.1 Resonator Results – Physical Dimensions

The design dimensions are shown in figure 7.1.1. The most important dimension is of course, the half wave resonating section on the center of the wafer. The resonating section length 4.275mm corresponds to an 11-12GHz resonating frequency via:

\[
L = \frac{c}{2f\sqrt{\varepsilon_e}} \tag{7.1-1a}
\]

Or, if working from a known length, the resonant frequency can be calculated by rearranging equation 7.1-1 to make the length (L) the independent variable:

\[
f = \frac{c}{2L\sqrt{\varepsilon_e}} \tag{7.1-1b}
\]

Where \( c \) is the speed of light in a vacuum, \( f \) is the desired resonant frequency and \( \varepsilon_e \) is the effective dielectric constant, taking into account the air (\( \varepsilon_r=1.0 \)) above the resonator and the sapphire (\( \varepsilon_r=9.3 \)) below it.

\[
\varepsilon_e = \frac{\varepsilon_r+1}{2} + \frac{\varepsilon_r-1}{2} \frac{1}{\sqrt{1+12d/w}} \tag{7.1-2}
\]

The signal arrives to the resonating section through feed lines on either side of the half wave resonator. They have a width of 580\( \mu \)m which lends itself to a 42\( \Omega \) input impedance from [55].

\[
Z_o = \frac{\eta_0}{2.0\sqrt{2.8\pi(\varepsilon_r+1)^{1/2}}} * \ln \left[1.0 + \frac{4.0h}{w^*} (A + B)^{1/2}\right] \tag{7.1-3a}
\]

Where,

\[
A = \frac{14.0 + 8.0}{11.0} * \frac{4.0h}{w^*} \tag{7.1-3b}
\]
And

\[ B = \left( A^2 + \frac{1.0 + \frac{1.0}{\varepsilon r}}{2.0} \frac{1}{\pi} \right)^{\frac{1}{2}} \]  

[7.1-3c]  

**Dimensions are in microns**

And

\[ B = \left( A^2 + \frac{1.0 + \frac{1.0}{\varepsilon r}}{2.0} \frac{1}{\pi} \right)^{\frac{1}{2}} \]

[7.1-3c]

Figure 7.1.1: Dimensions of the resonator described by equations in this chapter. As noted, all dimensions are in microns. The feed lines on the left and right are symmetrical.

The value \( w' \) is simply the width of the trace plus a factor to account for the trace not having zero thickness. In [56], the correcting factor was necessary; however, in this work, the thickness of the superconducting thin film is less than a quarter of a micron which makes it truly negligible for our purposes.

Equations 7.1-2-7.1-3 calculate impedance to with less than 1% error for impedances ranging from 30Ω to 90Ω [56].

Equations 7.1-3a-7.1-3c also agree well with the formula found in [57] – the holy grail of microwave engineering – when \( A \) and \( B \) are inserted and 7.1-3a is simplified:

\[ Z_o = \frac{120\pi}{\sqrt{\varepsilon r} \frac{w}{2d} + 1.393 + 0.667\ln\left(\frac{w}{2d} + 1.444\right)} \]  

[7.1-4]
The gap is 5\( \mu \text{m} \), which allows for keeping the loaded Q of the resonator high [58] as opposed to a direct coupling which would load the resonator.

With the fabrication process explained in chapter 4, the photolithography was not typical in that a more concentrated solution of developer is used. Typically, a 5:1 ratio of DI water to developer is employed for a gradual etch over the course of 20-60 seconds. For reasons already discussed a higher concentration of Microposit 351 developer is used, and a decreased developing time compensates. Even with decreased development time, over development was an issue. In spite of the minimal time and etch-stop methods, the potential for over-development existed to the tune of 2-5\( \mu \text{m} \).

The variance can cause an increase in characteristic impedance of the input line of between 0.15\( \Omega \) and 0.37\( \Omega \) by:

\[
\Delta Z_{2\mu m} = \frac{120\pi}{\sqrt{7.809} \frac{580}{500} + 1.393 + 0.667 \ln \left( \frac{580}{500} + 1.444 \right)} - \frac{120\pi}{\sqrt{7.809} \frac{576}{500} + 1.393 + 0.667 \ln \left( \frac{576}{500} + 1.444 \right)}
\]

\[= -0.15\Omega\]

And,

\[
\Delta Z_{5\mu m} = \frac{120\pi}{\sqrt{7.809} \frac{580}{500} + 1.393 + 0.667 \ln \left( \frac{580}{500} + 1.444 \right)} - \frac{120\pi}{\sqrt{7.796} \frac{576}{500} + 1.393 + 0.667 \ln \left( \frac{576}{500} + 1.444 \right)}
\]

\[= -0.37\Omega\]

The change in the half-wavelength section can lead to a shift in resonant frequency of between 11.87MHz and 29.71MHz from equation 7.1-1b.

\[
\Delta f_{2\mu m} = \frac{3 \times 10^8}{2 \times 4275 \sqrt{9.131}} - \frac{3 \times 10^8}{2 \times 4271 \sqrt{9.129}}
\]
As designed the resonant frequency is 11.6GHz from equation 7.1-1b.

\[ f = \frac{3 \times 10^8}{2 \times 4275 \sqrt{9.131}} \]

\[ = 11.61GHz \]

In the computations for the change in impedance and the change in resonant frequency due to over-etching, it was assumed that for two microns of over-etching, there is a four micron decrease in trace and patch dimensions. Similarly, for a five micron over-etch, there is a ten micron decrease in overall dimensions. That is, calculations were made assuming uniformity in etching. Also, the effective permittivity for a trace or patch decreases with over-etching, which is also reflected in the calculations and the reason for the varying values of \( \varepsilon_e \).

With over-etching as a distinct possibility, a sample half-wave resonator was simulated in ADS (Figure 7.1.2a). To represent over-etching, various simulations were run, the first of which simulated a simple over etching of five microns in all dimensions by decreasing each dimension's length and width by a total of 10 microns and increasing gaps by 10 microns. In the X-Band, the change in resonant frequency is only in the tens of megahertz and the decrease in magnitude – likely due to the increased impedance of the microstrip lines – is in the neighborhood of 5dB (Figure 7.1.2b).

To verify that the decrease in magnitude was due to increased impedance and not significantly affected by the change in coupling gap, the same sample resonator was simulated with the
original dimensions, but with the gap length increased to ten microns as opposed to five (Figure 7.1.3). The increase in gap length actually increased the magnitude of S11 at the resonant frequency. Larger gaps for gap-coupled resonators will create a more weakly coupled resonator and up to a certain gap length, will help isolate the resonating portion of the circuit and thereby increase the quality factor.

Figure 7.1.2a: S11 for the sample half-wave resonator. As shown, the center frequency is at 10.79GHz and the magnitude is 64.14dB.
Figure 7.1.2b: S11 for the resonator for the case of over-etching by five microns in all dimensions. The center frequency shifted up by 40MHz (10.83GHz) and the magnitude down by 5dB (59.14dB).

Since the resonator has a 5 micron gap in the original design, it is safe to say that the slight amount of over-etching that is possible would only increase the quality factor without being at risk of approaching a gap-width that may prove detrimental to the resonator's performance.

Figure 7.1.3: A ten micron gap doesn't change the resonant frequency a noticeable amount, though it does increase the magnitude by 4.345dB.
Using the pi-model for gap capacitance, the change in capacitance due to over-etching beyond the design gap of 5μm is inconsequential. Working through the following equations [59]

\[ C_p[\mu F] = 500d * e^{(1.86\frac{s}{\pi})} * Q_1 \left(1 + 4.19 \left(1 - e^{-0.785 \sqrt{\frac{d}{W_1}} \left(\frac{W_2}{W_1}\right)}\right)\right) \]  

[7.1-5a]

where \( W_2 \) is the width of the feed line, \( W_1 \) is the width of the patch, \( s \) is the gap length, and \( d \) is the substrate thickness. The variable \( Q_1 \) is calculated by:

\[ Q_1 = 0.04598 \left(0.03 + \left(\frac{W_1}{d}\right)^{Q_5}\right)(0.272 + 0.07 \varepsilon_r) \]  

[7.1-5b]

and \( Q_5 \) is

\[ Q_5 = \frac{1.23}{1+0.12\left(\frac{W_2}{W_1}-1\right)^{0.9}} \]  

[7.1-5c]

the change in capacitance due to variation in gap length is only 4.12fF which is a variation of only 0.25%. Of course, the purpose of the gap is both to provide for weak coupling and allow the loaded Q of the resonator to remain high – not create significant capacitive reactance to affect the performance or center frequency of the resonator [60].

The surface profiles from the Dektak IIIA verify etch characteristics. Figure 7.1.4 is a surface profile from the feed line to the half wavelength resonating section and shows that the gap that was etched was 10μm in length. Other samples had gaps of 8μm and 15μm. The 15μm gap is from a resonator fabricated early in this work before the final photolithography method was developed. Furthermore, the surface profile measures the thickness of thin film to be 0.2-0.25μm. The scattering parameter data in this chapter is from a sample that had the lowest achieved gap length of around 8μm.
7.2 Resonator Results – Electrical Characteristics

The test configuration described in Chapter 6, Section 1 and pictographically represented in figure 6.1.1a through figure 6.1.1e was used for characterization of the resonator as designed according to Chapter 5, Section 1 and modified by the procedures detailed in Chapter 6.

Naturally, data points were gathered in the form of scattering parameters at temperatures ranging from room temperature (which can range from 300K down to perhaps 290K – the wide range presumably depending on a hastily designed HVAC controller), to between 10K and 50K depending on how violently the compressor shook the test bench on the day of testing. At room temperature, as expected the YBCO behaved as an insulator so $S_{11}$ was nearly flat and relatively close to 0dB across the frequency range and $S_{21}$ consisted of large negative values with no coherent increase towards 0dB at any given frequency (figures 7.2.1a-b). The lowest value of $S_{11}$ at room temperature was $-1.82\text{dB}$ and occurred at 10.18GHz while the highest

Figure 7.1.4: The scan over the gap shows that the approximate gap length is 10-15µm and that the thickness of the YBCO thin film is around 2000 angstroms - or 200nm.
magnitude of $S_{21}$ at room was $-32.61 \text{dB}$ and occurred at 10.68GHz. Neither $S_{11}$ nor $S_{21}$ had discernable peaks at room temperature.

Neither the highest $S_{21}$ nor the lowest $S_{11}$ occur close to expected resonance and thus it can be assumed that the YBCO is not conducting sufficiently enough at room temperature to behave even remotely as anything but an insulator – and certainly not a conductor.

Figure 7.2.1a: The scattering parameter $S11$ shows no coherence to any resonator behavior at room temperature, as expected.
Figure 7.2.1b: The magnitude of S21 remains low across the frequency range and has no discernable peak at any frequency.
Figure 7.2.2a: The integer labeled independent axis correspond to temperature ranges over which conductivity does not vary greatly and thus had the S11 values were averaged over the temperature range. For example, data point 2 corresponds to 25-50K.

<table>
<thead>
<tr>
<th>Data Point</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
</tr>
</thead>
<tbody>
<tr>
<td>Corresponding Temperature Range</td>
<td>10-15</td>
<td>25-50</td>
<td>75-80</td>
<td>80-90</td>
<td>100-125</td>
<td>150-200</td>
<td>220-250</td>
<td>273-290</td>
</tr>
</tbody>
</table>

Figure 7.2.2b: Corresponding temperature ranges for Figure 7.2.2a.

As temperature decreases in the chamber housing with the resonator and jig inside, a degree of conductivity becomes apparent. Figure 7.2.2a shows a plot of $S_{11}$ values as temperature progressively lowers, with the highest magnitude occurring at temperatures between 10-15K for
an average of -31.18dB. Each data point in Figure 7.2.2a corresponds to a temperature range detailed in Figure 7.2.2b. The data was extracted from $S_{11}$ measurements from four separate experiments with the same procedure: secure the sample in the jig, secure the jig in the cold chamber, fix the temperature probe to the jig, evacuate the chamber, cool the chamber and measure $S_{11}$ at intervals from 273K down to 10K. The temperature of the lab affects the temperature of the sample regardless of the temperature probe reading inside the cold chamber. The probe reads the temperature of a spot on the jig some millimeters away from the sample and the YBCO is separated from the jig by an insulating layer and while this doesn’t result in an obtuse difference in the probe reading and the actual YBCO temperature, the difference in ambient temperature inside the cold chamber may cause a variance of a Kelvin or two in the YBCO. Additionally, sometimes vibrations in the system would result in a bad measurement so that taking four data points at exactly the same temperature was not feasible, but obtaining data over a small range of temperatures where little change in conductivity occurs yields a more complete characterization of the resonator’s behavior in varying temperatures.

Finally, the $S_{11}$ and the $S_{22}$ plots in figure 7.2.3a-b show peak resonance occurring at 11.58GHz and 11.61GHz with a magnitude of -27.42dB and -28.14dB respectively. There is a slight offset in the two peaks which may indicate lack of symmetry in the resonator; but more likely supports the lack of symmetry – and the results thereof – in the test configuration described in chapter 6.
Figure 7.2.3a: The resonator shows relatively good agreement with the theoretical computations as well as near perfect symmetry.

Figure 7.2.3b: The difference between resonance measurements $S_{11}$ and $S_{22}$ is only 30MHz.
At resonant frequency, both $S_{11}$ and $S_{22}$ show that the resonator has very good frequency selectivity. $S_{11}$ reaches its highest magnitude of $-27.42\,\text{dB}$ at $11.58\,\text{GHz}$ and $S_{22}$ reaches its highest magnitude of $-28.14\,\text{dB}$ at $11.61\,\text{GHz}$. Below -10dB and -18dB, $S_{22}$ and $S_{11}$ respectively have very narrow bandwidths of about 0.25% ($S_{22}$, -10dB) and 0.77% ($S_{11}$, -18dB) by equation 7.2-1, where $f_i$ is frequency of the low end of the passband at the given dB level, $f_h$ is the frequency of the high end of the passband, and $f_c$ is the resonant frequency.

$$\%BW = \frac{f_h-f_i}{f_c} \quad [7.2-1]$$

The very low bandwidths, and very high peaks at resonance suggest that the resonators impedance drops much lower than similar resonators made of conventional materials such as copper.

Using S-Parameter data, the method outlined in [61] allows for the computation of the loaded quality factor from measured results. The loaded $Q$ is found to be 151. Working from [62] the external $Q$ is found to be 165. Furthermore equation 7.2-2 from [41] allows for computation of the unloaded quality factor of 1805.

$$\frac{1}{Q_u} = \frac{1}{Q_L} - \frac{1}{Q_e} \quad [7.2-2]$$

The theoretical estimation of the quality factor is found by calculating the propagation constant $\beta$ and the attenuation constant $\alpha$. The propagation constant is simply

$$\beta = \frac{2\pi}{\lambda_g} \quad [7.2-3a]$$

where $\lambda_g$ is the wavelength in the microstrip line on a particular dielectric and can be found by

$$\lambda_g = \frac{c}{\sqrt{\varepsilon_r} f} \quad [7.2-3b]$$
While **equation 7.2-3** is useful in the design, once the resonance patch has been designed, double the length of the fabricated patch can just be plugged into **equation 7.2-2** to find the propagation constant:

\[
\beta = \frac{2\pi}{8.85 \times 10^{-3}} = 710
\]

The theoretical attenuation constant is the sum of the attenuation from the conductor and the attenuation from the dielectric. Conductor loss is found by:

\[
\alpha_c = \frac{R_S}{Z_0 W}
\]  \[7.2-4a\]

But, conductor loss should be estimated to be zero assuming ideal behavior of YBCO so more important is the dielectric loss:

\[
\alpha_d = \frac{k_o \varepsilon_r (\varepsilon_e - 1) \tan \delta}{2 \sqrt{\varepsilon_e (\varepsilon_r - 1)}}
\]  \[7.2-4b\]

With a loss tangent (\(\tan \delta\)) of 8.61e-5 [63], the losses due to the dielectric are only **0.0309 Np/m** and so the quality factor from **equation 5.1-2a** is **11505**. The theoretical is obviously quite large, but comparing theoretical quality factors to measured quality factors has little merit in this specific case because conductor loss does exist, albeit to a limited extent. To a greater degree, the two are not comparable – other than to say that they’re both very large – because the data points gathered from the network analyzer are discrete and actual resonance might be occurring between two of the discrete frequencies which could serve to further narrow the measured bandwidth and increase the loaded quality factor.

In the measurement of S11 and S22, the frequency response outside of the resonant frequency has showed small peaks and valleys across the calibrated frequency range rather than a flat response that is expected from a standard calibration, which was verified in **figure 6.1.4a**.
Under good calibration with the resonator behaving as it should, the reflection coefficient ($\Gamma$) would, of course, be high as most of the input power doesn’t transmit. Low transmission of power implies that the ratio $V_{in}^+$ and $V_{in}^-$ is close to unity, and therefore, by equation 7.2-5, $S_{11}$ is near zero.

\[ \frac{V_{in}^+}{V_{in}^-} \approx S_{11} \quad [7.2-5] \]

While the magnitude of $S_{11}$ and $S_{22}$ both stay low across the calibrated frequency relative to their magnitude at resonance, they are not perfectly level and they don’t coincide with the flat $S_{11}$ expected outside of resonance. This is more than likely due to the fact that calibration of the VNA was carried out at room temperature. The terminations used for VNA calibrations are very delicate and not rated for low temperature calibration at which YBCO becomes superconducting. Furthermore, there are seven separate changes in port terminations which must be made for a full two port calibrations. With the cryo-chamber being evacuated and sealed, even if the terminations were rated for such low temperatures the act of making a full two port calibration would not be feasible.

7.3 Schottky Contact – Physical Dimensions

Chapter 7, Section 2 conclusively demonstrates that the processing steps outlined in chapter 4, section 4 do not significantly degrade the performance of the YBCO by the results of the characterization of a half-wave gap-coupled patch resonator.

To the end of proving that the processing steps presented in earlier chapters are feasible and conducive to the goals of this work, a transistor is designed (as in chapter 5) and fundamental elements of operation were verified. Complete fabrication however, is outside the scope of this

78
work and is left for future works. The processing steps and mask design however, are both sound and would lead to a functional MESFET SOS transistor.

The Dektak IIA surface profiles in addition to visual examination under a 25X magnification microscope will verify that the photolithography steps are sound, as is thermal evaporation of aluminum – should that be the deposition technique that is used to create the Schottky contacts for the gate of the MESFET.

The procedure to “spin-on” the photoresist is described in chapter 4. Shipley 1818 positive photoresist was used with the spin speeds and times according to both knowledge of the particular spinner and the Microposit data sheet [64], the table from which is reproduced in table 7.3.1. The thickness desired was at least 1.25-1.50μm – thicker than any metal deposition called for in the process so that lift-off is possible. The spin speed of 4000 rotations per minute for a time of 20 seconds corresponds to the desired thickness.

In early stages of this work, the recipe for the photolithography on silicon was developed. It is more traditional than the quick development used for the YBCO samples:

-3000RPM for 30 seconds
-soft bake in oven for 30 minutes at 95°C (yields more even baking than hot plate)
develop in 5:1 solution of deionized water: Microposit 351 Developer
-rinse 10 seconds in deionized water
dry with N₂

After development, the sample is visually inspected. The aforementioned recipe is the result of multiple tweaks and modification made in order to yield resolution of the quality shown in figure 7.3.1a-b. Some of the smallest and most important feature dimensions are marked in the figures and are the yardstick by which success or failure is measured. After visual inspection for resolution, a surface profile can be obtained with the Dektak IIA; scan lengths are typically kept
short which gives higher resolution scans and better indication of how close-to-vertical the walls of the etched valleys are.

Figure 7.3.1a: The resolution of photolithography from the final process as outlined above is high enough for the five micron wide alignment marks in the mask design.

Figure 7.3.1b: The lines and corners are smooth and show no threat of causing shorts between the gate and source or gate and drain.
Figure 7.3.2 is a completed surface profile of the surface of a test sample that has undergone the photolithography steps mentioned earlier. The dotted line shows where the diamond tipped stylus passed over the sample and the two dimensions that have been superimposed were measured using the digital markers on the Dektak IIA. They both show good agreement with the table in the Shipley data sheet. The etch depths of 12420Å (1.242µm) and 12680Å (1.268µm) show not only that the photoresist thickness is within acceptable limits, but that the spinning, baking, exposure, and etch techniques give a nearly perfectly flat surface and uniform valley creation with only a 0.02µm variation in photoresist thickness.

![Graph showing surface profile](image)

Figure 7.3.2: The depth of the valleys represent the thickness of the photoresist measured as the stylus passes over the developed wafer from regions covered by photoresist to regions of bare silicon.

The sketch in figure 7.3.3 is of the surface profile taken on a piece of glass that was proximal to photoresist-coated silicon samples during aluminum deposition via thermal evaporation. Sections of the glass are intentionally “shadowed” from the source of evaporation so that the
Dektak IIA surface profiler can be used to very accurately measure the thickness of the metal deposited on the glass and thus very accurately estimate the thickness of metal evaporated on the silicon samples due to their proximity to the glass. The goal was to deposit 0.60 \( \mu \text{m} \) of aluminum and no more, so that there would be no lift-off issues with the chosen thickness of photoresist.

Figure 7.3.3: A rough sketch of the surface profile taken from the aluminum-on-glass sample. While there was a small peak at the glass-metal transition, the thickness on average is the difference between the plateau at 1.18 \( \mu \text{m} \) and 0.60 \( \mu \text{m} \), or approximately 0.580 \( \mu \text{m} \).

7.4 Schottky Contact – Electrical Characteristics

With the physical characteristics verified, the important electrical characteristics should appreciably verify the efficacy of the process developed for fabricating a silicon-on-sapphire metal-semiconductor field effect transistor (SOS MESFET) alongside YBCO. The most
important of these electrical characteristics is the current-voltage characteristics of the Schottky contact created at the aluminum-silicon interface. In the design section, it was shown that on p-type silicon, aluminum would make a good Schottky contact with said doped silicon, though the actual level of doping of the silicon is of little to no consequence regarding the current-voltage characteristics of the diode-like contact [65]. The computations in the design section (Chapter 5) arrive at a barrier height of $0.57V - 0.58V$.

To examine the Schottky contact created by the aluminum deposited on p-doped silicon, current-voltage characteristics are measured using the classic and reliable Tektronix 370 Curve Tracer. With the collector supply set to 60% of maximum peak voltage (figure 7.4.1) and the scales adjusted as noted on the right side of figure 7.4.2, it is apparent that the 0.5 volt turn-on voltage is accurate. Furthermore, a very high resistance to majority carrier reverse flow is shown with a breakdown potential of more than 20V. These results are indicative of a Schottky barrier that would make a good gate contact for a MESFET, thus proving that the photolithography and metal deposition techniques described thus far are effective for typical microelectronic device fabrication as well as working around YBCO in a non-degradational manner.
Figure 7.4.2: Current-voltage characteristics of Schottky contact.
Chapter 8

8.1 Conclusion

Processes for fabricating microwave microelectronic superconducting devices and thin-film silicon-on-sapphire devices on the same wafer, without causing significant degradation or to either material or performance hindrance to the electronic devices fabricated on said material, have been developed and experimentally verified. Using quick developing techniques for the photolithography steps, a Schottky contact was developed on p-type silicon, and its performance verified on a Tektronix 370B Curve tracer. The same photolithography process was successfully used to fabricate a half-wave resonator on YBCO and its performance was verified on an HP8510 network analyzer.

Some of the key elements that were addressed and resolved were: prevention of prolonged exposure of superconducting material to moisture during photolithographic processes, avoidance of uncertain consequences of high temperature anneals on superconducting material, etching superconducting material without consequence to silicon electronics, creating metal Schottky and Ohmic contacts on silicon without damaging the superconducting material, and bonding superconductor contacts to metal probes.

8.2 Future Work

In this work, a superconducting resonator was fabricated by a process that would not significantly degrade the silicon electronics described in earlier chapters. Additionally, a Schottky contact was fabricated that does not degrade YBCO on the same wafer.

Building on this work and given the necessary fabrication tools, it should be possible to fabricate a MESFET directly, using the mask that was described in chapter 6, and fabricated for this work – sharing the same mask used for the YBCO resonator fabrication. With some modification, it
should also be possible to fabricate a MOSFET as well. The next challenge would be to integrate electronics on the YBCO half of the wafer with electronics on the silicon half of the wafer.
References


