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Robustness Issues of Run-time Leakage Control in Nano-scale Technologies

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Abstract

As CMOS technology scales down, the substantially increased leakage power consumption has made leakage reduction techniques important in VLSI circuit design. Popular techniques such as reverse body bias (RBB) and power gating (PG) are used in current circuit design. However, transient circuit response during mode transitions, especially from sleep mode to active mode, has not been studied thoroughly. Most researchers only analyze the rush current in transition and consider no parasitic inductance. This thesis takes RBB as the target leakage reduction technique and analyzes the circuit response during mode transitions, including ground bounce magnitude and wake up time. An accurate circuit model has been developed where on-chip and package parasitic parameters are added to ensure accuracy. A fast simulation method using Matlab has been provided. The circuit behaviors are discussed in detail. To better understand the modeled circuit behaviors, circuits under RBB with their base connected to the global ground are also analyzed. Such connections cause a positive ground bounce. PG model has been developed to be compared with RBB technique. Finally several optimization methods are proposed to reduce the circuit wake up time.
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Chapter 1

Introduction

1.1 Leakage Current

There are two types of transistor currents: transient and leakage current. Transient current includes dynamic current and short circuit current. Dynamic current is used to charge the circuit capacitance and thus change logic states. Short circuit current exists when both PUN and PDN conduct in a CMOS technology, which is totally useless. Leakage current occurs when the circuit is in the steady state. It is a tiny current flowing through the MOS device.

In the modern VLSI system design, power consumption is a thorny problem. As the transistor feature size continues scaling down and the power supply voltage keeps dropping, the threshold voltage decreases accordingly to maintain the circuit performance. This reduced threshold voltage causes an exponential increase of the leakage current. Especially when more and more transistors are integrated on a single die according to the Moore’s law, the leakage current has become a big problem. Each new technology generation will cause about a 30X increase in the gate leakage and a 5X increase in the subthreshold leakage [1]. When the technology scales down to 45nm, the leakage power may even dominate the dynamic power [2]. Leakage current includes three major components: subthreshold leakage, gate leakage, and band-to-band tunneling (BTBT) leakage. Fig. 1.1 illustrates the leakage current components [3].
The subthreshold leakage current flows between the source and the drain terminal of a transistor which is in the cut off region. It contributes to a large percentage of the total leakage current. The subthreshold leakage current increases exponentially as the threshold voltage scales down. It also increases with temperature. Thus the longer the circuit operates, the higher the circuit temperature, and therefore the larger the subthreshold leakage current. This positive feedback can cause very large subthreshold leakage current. The subthreshold leakage current equation can be expressed as:

\[ I_{\text{subthreshold}} = I_0 \cdot e^{\frac{q(V_{GS} - V_T)}{nKT}} (1 - e^{-\frac{qV_{DS}}{KT}}) \]  \hspace{1cm} (1.1)

where \( I_0 \) and \( n \) are empirical parameters. \( n \) is typically 1.5, \( k \) is the Boltzmann constant, \( q \) is the electronic charge, \( V_T \) is the threshold voltage, and \( T \) is the absolute temperature \([4]\).

The junction BTBT leakage current is caused by the reversed biased PN junction. The BTBT leakage is usually ignored due to its minor contribution to the total leakage power consumption. The BTBT current can be expressed by:

\[ I_{\text{BTBT-side}} = W_{eff} Y_{j-eff} AE_{side} V_{app} \sum_{g}^{1/2} \exp\left(-\frac{B \sum_{g}^{3/2}}{E_{side}}\right) \]  \hspace{1cm} (1.2)

\[ I_{\text{BTBT-btm}} = W_{eff} X_{j-eff} AE_{btm} V_{app} \sum_{g}^{1/2} \exp\left(-\frac{B \sum_{g}^{3/2}}{E_{btm}}\right) \]  \hspace{1cm} (1.3)
where $A = \sqrt{\frac{2m_{q}q}{4\pi \hbar^2}}$, $B = \frac{4\sqrt{2m}}{3qh}$, $V_{app}$ is reverse bias voltage, $\sum_{g}$ is silicon band gap, and $Y_{j-\text{eff}}$ and $X_{\text{eff}}$ are effective height and length of the junction [5].

The gate leakage current draws more attention in recent years since it increases dramatically with transistor dimension scaling. Gate leakage is caused by the direct tunneling of electrons and holes through the insulating layer underneath the gate. Continuous decreasing of the gate-oxide layer thickness leads to the excessive gate leakage current which may surpass the subthreshold leakage current in nano-scale technology [6]. The equation for the gate leakage current is:

$$J_G = J_0 e^{\frac{-8\pi \sqrt{2q}}{3h} (m_{eff} \phi_b)^{0.5} k T_{eqx}}$$ (1.4)

$$J_0 = \frac{q^2 E_{ox}^2}{(8\pi \hbar \phi_b)}$$ (1.5)

where $\phi_b$ is the tunneling potential barrier and $m_{ox}$ is the effective carrier mass in oxide. $E_{ox}^2$ in this equation represents the product of electrical field and inversion charge density across the oxide. Parameter $q$ is the carriers charge, $h$ is Planck's constant over $2\pi$ and $m_{eff}$ is the effective mass of a carrier in the conduction band of silicon [7].

The gate leakage current does not increase with temperature. So in a high temperature, the subthreshold leakage may be much higher than the gate leakage. In January 2007, Intel introduced a new transistor material which combines halfnium-based high-k(Hi-k) gate dielectrics and new metal materials for the transistor gate [8]. With the high-k material to replace the transistor’s silicon dioxide gate dielectric and new metals to substitute the polysilicon gate electrode, the gate leakage can be greatly reduced. So in this thesis, we ignore the gate leakage current, and consider only the subthreshold leakage current.

1.2 Leakage reduction techniques

By considering the subthreshold leakage current equation, the most powerful way to reduce it is to increase the threshold voltage. The threshold voltage can be regulated by
body effect:

$$V_T = V_{T0} + \gamma \sqrt{|(-2)\phi_F + V_{SB}|} - \gamma \sqrt{|2\phi_F|}$$  \hspace{1cm} (1.6)

where $V_{T0}$ is threshold voltage under $V_{SB}=0$, and $\gamma$ and $\phi_F$ are device parameters [4]. So if $V_{SB}$ is larger, the threshold voltage is larger. A small threshold voltage is desired for fast switching speed, but it also causes a larger subthreshold current, which is inversely proportional to the threshold voltage. Obviously, there are trade-offs between the circuit switching speed and the power consumption. In this situation, techniques have been developed to reduce leakage current without affecting circuit performance too much. A leakage reduction technique can be useful only when it renders good performance during normal operation mode, while reducing leakage current in sleep mode. Leakage reduction techniques can be classified into two categories: run-time and design-time techniques.

Design time techniques modify the circuit beforehand, so that it cannot dynamically adjust itself during operation. For example, the dual threshold CMOS is a design time technique. It uses high threshold voltage transistors in non-critical paths and low threshold transistors in critical paths. Variable threshold voltages can be achieved by different fabrication processes such as changing transistor width and length or doping density [8]. But all processes have some performance degradation.

Run-time leakage reduction techniques utilize the short idle time of a circuit and put the circuit into the sleep mode to reduce the power consumption. Several run-time techniques have been listed below:

1. **Natural transistor stacks**

   This technique is based on the stacking effect of transistors. The threshold voltage is reduced if $V_{SB}$ is increase due to body effect, and in turn the subthreshold leakage current reduces when two or more transistors in a series connection are turned off. The leakage of a two-transistor stack is an order of magnitude less than the leakage in a single transistor [9]. Input vectors can be generated to achieve this stack effect. But, sometimes, it is very difficult and may cause higher gate leakage which can surpass the subthreshold leakage reduction [10].

2. **Power Gating (PG)**
Sleep transistors are generally inserted in series with the circuit, and they must be made wide enough to reduce the resistance so that the circuit performance will not be affected too much in the normal operation mode. On the other hand, sleep transistors cannot be too large, since the leakage current is proportional to the transistor size, and large sleep transistors also consume much area. Furthermore large sleep transistors have large capacitances and thus retard the circuit mode transition. Several techniques have been proposed to deal with this problem. [11, 12, 13, 14]

3. Reverse body bias (RBB)

By the RBB technique, each control transistor controls the circuit base voltage and thus the subthreshold leakage current. When the circuit is in active mode, the circuit base is connected to the normal voltage source, either Vdd or Gnd; while the circuit is in stand-by mode, the base is connected to another voltage source to increase the threshold voltage. By the RBB technique, the width of each control transistor does not affect the circuit performance during normal mode.

Currently most run-time techniques aim at reducing the leakage current during the stand-by mode. However run-time active leakage power reduction (RALR), which can reduce the circuit leakage current once it detects sufficient idleness even when the circuit is still in the active mode, has drawn more attention recently [15]. The problem of RALR is that the energy consumed by switching the circuit mode should be less than the energy saved by the leakage reduction technique. Both PG and RBB techniques from an energy view in active run-time circuit operations have been analyzed thoroughly in Paper [15]. PG has higher stabilized leakage reduction ratio but consumes more power than RBB during transition. So RBB is more suitable than PG for short-term idleness leakage reduction [15]. This thesis is focused on the analysis of ground bounce phenomenon caused by the RBB technique, while PG will also be analyzed to be compared with RBB with respect to the wake up time and ground bounce magnitude.
1.3 Ground bounce

In this section, we will introduce the concept of ground bounce. Switching noises include both IR drop and inductive noise which may reduce the circuit noise margin, consume extra energy and even cause circuit malfunction. IR drop is the voltage drop due to resistance. Parasitic inductance may also cause voltage fluctuations. Ground bounce occurs when the circuit is switching, and the ground voltage will go through a fluctuation process before getting stable. In this thesis, the wake up time is defined as the time when the voltage goes below ±1.5% of the nominal voltage. Inductive noise is determined by the product of inductance and transient current values \((L \times \frac{di}{dt})\). Traditionally, capacitive coupling (crosstalk) is the major concern in designing a VLSI circuit, and inductive noise was not a big problem under low working frequency. The complex impedance of inductance under a certain angular frequency \(\omega\) is \(j\omega L\). The higher the angular frequency is, the larger the complex impedance will be. Usually that value is not large enough to be compared with the impedance by resistance and capacitance under low frequency. However, in nano-scale technology, circuit speed is about 1GHz or higher. At this working frequency, parasitic inductance cannot be ignored any more. Inductance may introduce ground bouncing and dramatically reduce circuit performance.

Switching current and parasitic inductance, capacitance and resistance are major contributors to ground bounce. There are two types of parasitics: on-chip and package. Package pins as well as bonding wires have parasitic inductances, and usually circuit package and PCB layout have very large parasitic parameters. Ground bounce was only considered for output driver circuits in the past. When output drivers switch concurrently, the rush current is huge and causes large ground bounce due to package parasitic parameters. Carefully choosing a package which has lower parasitics can improve the circuit performance. As technology advanced in package, the package parasitics have been greatly reduced.

On-chip parasitics of the power and ground wires were ignored compared with the chip-package interface parasitics by many researchers. However, as technology scales down and more transistors are integrated in a single die, ground bounce has become an important issue in VLSI circuit design. Especially in 32nm technology, on-chip self and mutual wire
inductance cannot be ignored due to higher frequency and higher integration intensity.

Both MOS devices and on-chip interconnection have parasitic R, L and C. Transistors have gate overlap capacitance, channel capacitance and diffusion capacitance, and on-off resistance. The values of those parameters vary with the working region and applied voltage. Interconnection wires have distributed parameters of resistance, capacitance and inductance. The wire width is getting smaller and the corresponding resistance becomes larger with each technology scaling down. When considering the device or wire itself, there is IR voltage drop, RC delay and inductive noise. When considering the network, there are coupling inductance and capacitance among conductors. Due to the large coupling effect, the values of parasitic capacitance and inductance are determined by the circuit topology.

1.4 Ground bounce of RBB technique

In a large circuit, there are several different circuit blocks. Some of them go through the mode transition while others remain in one operation mode. Fig. 1.2 shows an example circuits under RBB technique which contains four possible circuit states from left to right:

1. a circuit remains in normal mode (no RBB applied)
2. a circuit remains in normal mode since the circuit base is connected to gnd1
3. a circuit remains in idle mode since the circuit base is biased
4. a circuit switches from idle to normal mode

In the last situation, where the circuit switches from the idle mode to the normal mode will cause the ground and base voltage fluctuation. Other circuits, although remain in either idle or active mode, may go through this fluctuation since they share the same local ground. This may cause performance degradation of circuits in normal mode, and increase leakage current in the idle mode.
1.5 Problem statement

Once a leakage current reduction technique has been applied to the circuit, the major issue is whether the circuit can come back to normal operation mode as soon as possible without affecting other circuits which are in active mode. A complicated circuit may have several logic blocks in different operation modes. Some blocks need to enter energy-saving mode, some need to switch back to normal base voltage, and some will never enter power saving mode. Those blocks experiencing mode transition would probably affect other blocks, since mode transition would cause ground bounce, and affect severely the circuit performance and noise margin of those blocks under normal operation mode.

In this work, the ground bounce of the RBB technique will be thoroughly analyzed. The two aspects of ground bounce, its magnitude and wake up time, will be analyzed according to various environmental settings. The circuit model is composed of three parts: the control circuit, the bench mark circuit, and the parasitic RLC circuit.

When RBB is applied to the circuit, the leakage current can be greatly reduced. However it will go through the ground bouncing process due to the large parasitic parameters, when the circuit switches back to the normal operation mode. The bounce is determined by both parasitic value and energy stored in the circuit, which will be described in detail in following chapters.
Once we have determined the parasitic parameter values in the circuit, we can analyze the circuit response. To understand the complicated circuit behavior, a brief review of a RLC circuit is needed here. Take the simple series RLC circuit in Fig. 1.3 as an example. This is the simplest RLC circuit. A parallel RLC circuit can be transformed to a series circuit easily. For example, Fig. 1.4 shows a parallel RLC circuit which is equivalent to the series RLC circuit shown in Fig. 1.3, as long as they have the same equivalent complex impedance. The equivalent complex impedance of the series RLC circuit is $R_s + jwL_s + \frac{1}{jwC_s}$, and that of the parallel RLC is $\frac{1}{R_p + jwL_p + jwC_p}$. So for different angular frequencies $w$, there must exists a group of values for $R_s, L_s, C_s, R_p, L_p$ and $C_p$ which can make these two complex impedance equations equivalent. So we take the series RLC circuit as an example here without losing generality.

When the circuit in Fig. 1.3 switches with initial energy, it will start to bounce until settling down. It is a damped vibration with resistance. The behaviors of inductance and capacitance can be represented by Equation 1.7 and 1.8:

$$V_L = L \frac{di}{dt} \quad (1.7)$$

$$I_C = C \frac{dv}{dt} \quad (1.8)$$
According to Kirchhoff’s current law, a simple second order differential equation shown below can be used to represent the above circuit behavior.

\[
V = L \frac{d^2v}{dt^2} + CR \frac{dv}{dt} + v
\]  

(1.9)

where \(v\) is the voltage across the capacitor.

There exists an analytic solution for this differential equation when the initial condition is given. However, there is no analytic solution for many complicated circuits, so a numerical solution will be used. In this thesis, Matlab is used to get the numerical solution for each time slot by resolving a set of differential equations, and this will be introduced in Chapter 2 in detail. As we stated above, the equivalent complex impedance of series RLC circuit is \(R + jwL + \frac{1}{jwC}\). We use \(s\) to substitute \(jw\) to get equation \(V = I(R + sL + \frac{1}{sC})\), which is the Ohm’s law in frequency domain. The resonant frequency is defined as the frequency in which the equivalent complex impedance of a circuit is minimum, or in another word, there is only equivalent resistance in the circuit (the effect of \(L\) and \(C\) cancels each other). The magnitude of the complex impedance is \(\sqrt{R^2 + (wL - \frac{1}{wC})^2}\), so the resonant frequency occurs when \(wL = 1/wC\). It takes a long time to simulate a large benchmark circuit by Hspice. Sometimes, Hspice cannot finish simulation due to the huge computational complexity in a reasonable time. To predict the circuit behaviors quickly, other simulation methods must be established to get the fast and acceptable simulation results.

This thesis presents a novel circuit model combined with a Matlab simulation method to predict the circuit behaviors with great easiness and fastness. The procedure of model extraction is illustrated in Fig. 1.5. The simulation results obtained by Matlab are compared with those by Hspice. Little research effort has ever been invested to study all parasitic
parameters to get the accurate circuit behavior analysis. Some researchers only presented package parasitic parameters while some totally ignored the inductance. The results of those studies are not accurate enough and cannot reflect the true story of ground bounce phenomena. On-chip and package parasitic parameters are both considered and added to the circuit model in this thesis. ISCAS85 benchmark circuits have been tested and simulated, and circuit responses are thoroughly analyzed. Simulation results show that the larger the circuit scales, the longer the wake up time is, and the smaller the ground bounce magnitude is.

1.6 Overview of the thesis

The remainder of this thesis is organized as follows.

Chapter 2: An accurate RBB model for inverter circuit is developed. MATLAB solution is given to accomplish fast circuit simulation.

Chapter 3: An accurate RBB model for benchmark circuits is developed. The circuit model is evaluated by comparing simulation results of HSPICE and MATLAB.

Chapter 4: An accurate RBB model for benchmark circuits is developed with base connected to global ground, and the simulation results are compared with the previous experiments.

Chapter 5: A PG model is derived with the same sleep transistor width as RBB, and the circuit responses are compared between RBB and PG.

Chapter 6: Optimizations for RBB technique are presented.

Chapter 7: Conclusion and future research are presented.
Chapter 2

RBB Model

PG (power gating) is a technique that adds sleep transistors to the power supply or ground or both to reduce the circuit leakage power consumption. Normally only one type of sleep transistors is needed. A NMOS transistor has higher mobility than a PMOS, so with the same current sink ability, NMOS needs less area than PMOS and thus becomes a better choice in PG technique. When a circuit is in idle mode, sleep transistors are shut down and thus increase the source voltage of the PDN in the circuit, or decrease that of the PUN. Due to the body effect, the source voltage change will drastically increase the threshold voltage and thus greatly reduce the circuit leakage current. Power gating is an effective and simple way to cut down the leakage power consumption. However, each sleep transistor has to be wide enough to present less resistance when conducting and in turn will not affect the circuit performance too much. On the other hand, if it is too large in size (width), there will be much more leakage current when it is switched off, and thus it cannot reduce the leakage power consumption effectively. Also its capacitance will be so large that it will become a self loaded circuit during mode transition. Furthermore, larger transistor can bring about larger rush current, ground bounce and wake up time during mode transition. All of those pose a limit on PG design.

Reversed body bias (RBB) is another effective technique to reduce leakage current in integrated circuits. RBB also reduces leakage current by increasing the threshold voltage due to the body effect. The control transistor can be made very large to reduce the wake
up time when the circuit switches back to normal operation mode. It can also be made very small to save the area without affecting the circuit performance during normal mode. Technology scaling down calls for more aggressive leakage reduction techniques in order to further reduce power consumption. In this situation, RBB is better than PG because it performs better in short-term idleness energy savings [15]. So, we will study RBB thoroughly in this thesis. The results from PG which has the same sleep transistor width will be compared with RBB.

Firstly, we will study the ground bounce of an inverter circuit under the RBB technique and extract its model. The circuit diagram is shown in Fig. 2.1. In this Figure, the inverter is composed of transistors T3 and T4. The control circuit, which switches the circuit base to normal voltage or lower voltage, is composed of two NMOS transistors T1 and T2. T1 will be turned off and T2 will be turned on when the inverter circuit switches back to normal mode from sleep mode. The parasitic RLC circuit is composed of the on-chip interconnection and package inductance, resistance and capacitance. We can thus split the circuit into three blocks: the inverter circuit, the control circuit, and the parasitic RLC circuit. The block diagram is illustrated in Figure 2.2. Models for every block will be discussed in detail in the following sections.

![Inverter circuit diagram](image)

Figure 2.1: Inverter circuit diagram
2.1 RLC parasitic circuit model

A widely accepted PG model is illustrated in Fig. 2.3 [16, 17, 18]. This figure shows a circuit under the PG technique with an NMOS sleep transistor. R, L, and C are parasitic parameters of the on-chip ground wire and package parasitics. In this PG model, all of those parasitics are lumped together. This model is quite simple and can be used to analyze ground bounce in a fast way. But its accuracy is worthy of discussion.

Firstly, on-chip wire parasitics are distributed parameters, so a lumped model is not accurate to represent it. Secondly, simple addition of on-chip and package parasitics is just a rough estimation. Actually it is not reasonable to add them together directly. In this thesis, we will revise this parasitic RLC circuit model for RBB, so that it can better represent the
real circuit behavior. RBB is only applied to NMOS in this thesis, so we consider the on-chip parasitics from the ground wire only, ignoring Vdd parasitics. To derive the RBB circuit model, we need firstly determine the parasitic RLC values.

2.1.1 RLC parameter values

2.1.1.1 Package parasitic parameters

Paper [19] lists the parasitics of some package technologies, which are shown in Table 2.1. According to this paper, We take the same parasitic parameter values with L=7nh, C=0.5pf and R=0.6Ω for the lumped package parasitics without losing generality [19].

<table>
<thead>
<tr>
<th>Wire bonding Package type</th>
<th>CPGA</th>
<th>PPGA</th>
<th>H-PBGA</th>
<th>TQFP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bondwire/diebumpRₙ(mΩ)</td>
<td>126-165</td>
<td>136-188</td>
<td>114-158</td>
<td>70-150</td>
</tr>
<tr>
<td>Bondwire/diebumpLₙ(nH)</td>
<td>2.3-4.1</td>
<td>2.5-4.6</td>
<td>2.1-4.1</td>
<td>1-4</td>
</tr>
<tr>
<td>Bondwire/diebumpCₙ(pF)</td>
<td>0.2-0.5</td>
<td>0.1-0.3</td>
<td>0.2-0.6</td>
<td>0.1-0.3</td>
</tr>
<tr>
<td>Pin/LandRₙ(mΩ)</td>
<td>20</td>
<td>20</td>
<td>0</td>
<td>90-97</td>
</tr>
<tr>
<td>Pin/LandLₙ(nH)</td>
<td>4.5-7.0</td>
<td>4.5-7.0</td>
<td>4.0-6.0</td>
<td>3-5</td>
</tr>
<tr>
<td>Pin/LandCₙ(pF)</td>
<td>0.1</td>
<td>0.1</td>
<td>0.02</td>
<td>0.1-0.3</td>
</tr>
</tbody>
</table>

2.1.1.2 On-chip interconnection parasitic parameters

On-chip interconnection parasitics are extracted according to 2007 ITRS [20]. Here the global wiring metal is used for the ground signal. For the 32nm technology, the fringe capacitance per unit length for global wires is 1.7-2.0pf/cm, so we take 1.8pf/cm. The minimum global wiring pitch is 96nm. Conductor effective resistivity (µΩ – cm) with minimum pitch Cu global wiring including effect of width-dependent scattering and a conformal barrier of thickness is 3.52 µΩ – cm. Since the wire width is about 1/2 pitch as mentioned in 2007 ITRS [20], we set width=1/2 × 96nm, which is about 50nm. The aspect ratio is 2.5, so the wire height is 50nm × 2.5 = 125nm. Furthermore, We take the length of the power rail as 1mm, its width as 10 times of the minimum wire width, which is 500nm, and the wire height is 125nm. From resistance equation:
\[ R = \frac{\rho l}{WT} \]  

(2.1)

where \( W \) is the width, \( T \) is the height, \( l \) is the length, \( \rho \) is the resistivity, which is 3.52 as stated before. We get the following capacitance and resistance values:

\[ C = 1.8pF/cm \times 1mm \times 10 = 1.8pf \]

\[ R = 3.52 \times 1mm/(500nm \times 125nm) = 563.2\Omega \]

Calculating parasitic inductance without knowing circuit layout is impossible. Here we make several assumptions. Firstly, we calculate the inductance of a single conductor. The equation for the single conductor inductance is,

\[ L = 0.002l \left( \frac{2l}{B + C} + \frac{1}{2} - \log_2 \epsilon \right) \]  

(2.2)

where \( l \) is the conductor length (in centimeters), \( B \) and \( C \) are the width and height of rectangular cross section [21]. The value of \( \log_2 \epsilon \) can be found from Table 2.2 [21].

<table>
<thead>
<tr>
<th>B/C or C/B</th>
<th>( \log_2 \epsilon )</th>
<th>B/C or C/B</th>
<th>( \log_2 \epsilon )</th>
<th>B/C or C/B</th>
<th>( \log_2 \epsilon )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0.25</td>
<td>0.00249</td>
<td>0.55</td>
<td>0.00203</td>
</tr>
<tr>
<td>0.025</td>
<td>0.00089</td>
<td>0.30</td>
<td>0.00244</td>
<td>0.60</td>
<td>0.00197</td>
</tr>
<tr>
<td>0.05</td>
<td>0.00146</td>
<td>0.35</td>
<td>0.00236</td>
<td>0.65</td>
<td>0.00192</td>
</tr>
<tr>
<td>0.10</td>
<td>0.00210</td>
<td>0.40</td>
<td>0.00228</td>
<td>0.70</td>
<td>0.00187</td>
</tr>
<tr>
<td>0.15</td>
<td>0.00239</td>
<td>0.45</td>
<td>0.00219</td>
<td>0.75</td>
<td>0.00184</td>
</tr>
<tr>
<td>0.20</td>
<td>0.00249</td>
<td>0.50</td>
<td>0.00211</td>
<td>0.80</td>
<td>0.00181</td>
</tr>
</tbody>
</table>

According to Equation 2.2, we get the inductance values: \( L1=19.64e-10H \) and \( L2=17.137e-10H \), for interconnection wires which are both 1mm long and 125nm high, but have two different widths: \( 50nm \) and \( 500nm \). The ratio of \( L1/L2 \) is 1.146. According to Table 2.3 [22], the inductance for 50nm technology is \( 18.8nH/mm \) with minimum wire width. Assume \( L=20.4nH/mm \) for the 32nm technology with the minimum wire width, the inductance for a global wire with 10 times of minimum width can be calculated by dividing 1.146, which is \( 20.4nH/mm/1.146 = 17.8nH/mm \).

The on-chip inductance value in this thesis is an estimation. However, the inductance value can be changed in the experiment, so the value of inductance is not vital. Finally the
Table 2.3: On-chip parasitic parameters table

<table>
<thead>
<tr>
<th>Tech.(nm)</th>
<th>180</th>
<th>130</th>
<th>100</th>
<th>70</th>
<th>50</th>
</tr>
</thead>
<tbody>
<tr>
<td>r(kΩ/m)</td>
<td>36.3</td>
<td>3.1</td>
<td>1.9</td>
<td>1.5</td>
<td>1.25</td>
</tr>
<tr>
<td>c(pF/m)</td>
<td>269</td>
<td>240</td>
<td>154</td>
<td>125</td>
<td>106</td>
</tr>
<tr>
<td>l_{max}(nH/mm)</td>
<td>9.2</td>
<td>10.9</td>
<td>13.5</td>
<td>17.9</td>
<td>18.8</td>
</tr>
</tbody>
</table>

On-chip RLC parasitic parameters in this thesis are: C=1.8pf, R=563.2Ω, L=17.8nH.

2.1.2 Revised RLC circuit model

As discussed previously, the widely accepted RLC model is not accurate to describe the real circuit behavior. A revised RLC model is derived to better represent the circuit behavior. An experiment was set up to compare the circuit response of the lumped RLC model (on-chip and package parasitics lumped together), the separate lumped model (on-chip and package parasitics lumped separately), and the T model (which includes T, T2, T3, T4, T5, T6 models as discussed later) for on-chip parasitics with the lumped model for package parasitics. The T model means the resistance and inductance of on-chip parasitics are separated into two parts and placed at each side of the capacitance. In this experiment, the package RLC is represented by the lumped model and the on-chip ground wire is represented by T model with various number of segments. All of those models are illustrated in Fig. 2.4. Based on this concept, we simulate totally eight models. This parasitic RLC circuit is the wire and package parasitics block in the Fig. 2.1. We will compare the circuit response among those models.

In this experiment, the on-chip parasitic parameters are C8=1.8pf, R1=563.2Ω, L1=17.8nH, and package parasitics parameters are L2=7nh, C8=0.5pf and R2=0.6Ω. Fig. 2.5 is the simulation results for different circuit models.

From this experiment, the lumped RLC model will dramatically reduce the ground bounce effect because the capacitance (i.e., C8+C9) acts as a large decoupling capacitance between the global ground and local ground (gnd1). So the lumped RLC model is not suitable to represent the ground bounce effect. It is well known that distributed RLC circuit model is more accurate to represent a global on-chip interconnection. But, due to
the computational complexity, an executable solution is needed to obtain a decent result with less calculation effort. It is obvious that the ground bounce magnitude is similar when we use the T models. To reduce the computation complexity, a T-model for the on-chip wire and a lumped model for the package parasitic parameters are used to represent the RLC parasitic circuit. As illustrated in Figure 2.6, R1, L1 and C8 represent the on-chip wire parasitics, and R2, L2 and C9 are parameters of the package parasitics. It is trivial to calculate the values of R1, C9 and L1, which are 282Ω, 1.8pf, and 8.9nH separately.

Now assume we have a circuit which is composed of 1000 inverters (or equivalent 10 large inverters), and the circuit diagram with the T model for on-chip parasitics and the lumped model for package parasitics is illustrated in Fig. 2.7. T1 and T2 are control transistors for the body bias control of the inverters. T1 is on and T2 is off when the circuit
is in energy-save mode, while T2 is on and T1 is off when circuit is in normal mode. Since we are aiming at the response when the circuit switches back to normal mode, we can rule out the effect of transition of T1, by switching it long off before T2 is switched on.
2.2 Inverter circuit model

An accurate and simple circuit model for the test bench circuit is required to achieve fast simulation and estimation. We start from extracting circuit model for an inverter circuit. As we know, there are two types of capacitances in a transistor, gate and diffusion capacitances. Gate capacitance includes overlap capacitance and channel capacitance. Overlap capacitance is linear and constant, and it can be expressed as [4]:

\[ C_{gso} = C_{gdo} = C_{ox} X_d W = C_o W \]  \hspace{1cm} (2.3)

where \( X_d \) is the overlap width of gate oxide and diffusion. It is determined by the technology used. \( W \) is the channel width; \( C_{ox} \) is the capacitance per unit area; \( C_o \) is the capacitance per unit width.

Channel capacitance includes gate-to-source, gate-to-drain, and gate-to-body capacitances. Those capacitances vary with working regions and voltages. When the circuit is in the cut-off region, there is no channel beneath the gate oxide, so there is only gate-to-body capacitance. When the circuit is in the linear region, there is channel between source and drain, so the capacitance can be considered as two equal capacitances at the source and drain. When the circuit is in the saturation region, pinch-off happens and there is no channel at drain side, so gate-to-drain capacitance does not exist. The values of those capacitances are variables. There is a large fluctuation of channel capacitances especially around the region of \( V_{gs} = V_t \) [4]. From the above analysis, given the transistor state, we can find all transistor capacitance values.

Since the PMOS is conducting in Fig. 2.8, there is no gate-to-body capacitance. Thus, C11 (C12) is the summation of the overlap capacitance and gate-to-source (gate-to-drain) capacitance. The NMOS is off, so there is gate-to-body capacitance. Since the gate and source are connected to the same voltage gnd1, the gate-to-body capacitance can be added with source diffusion capacitance together to get a equivalent lumped capacitance. In Fig. Fig. 2.8, C13 is the drain diffusion capacitance, C14 is the gate capacitance, and C15 is the source diffusion capacitance.
Adding capacitances in Fig. 2.8 together, we have $C_5 = C_{13}$, $C_6 = C_{15}$, $C_7 = C_{14} + C_{12} + C_{11}$. Finally, we have the inverter circuit model which is shown in Fig. 2.9. The on and off resistances of the inverter circuit can ignored because the inputs are not changed (only base is changing). If the input to inverter circuit is logic low, then there is little fluctuation for the output voltage of the inverter during mode transition, and most of time it is absolutely $V_{dd}$. Thus, we assume the drain and source voltages of the PMOS in Fig. 2.8 are both $V_{dd}$, and ignore the tiny current flowing through the PMOS during mode transition. Finally the model of the inverter circuit is composed of three capacitances $C_5$, $C_6$ and $C_7$. This model provides an accurate estimation of the circuit activity and greatly reduces the complexity of calculation.

To determine the value of $C_5$, $C_6$ and $C_7$, Hspice simulations for the above inverter circuit are conducted. According to equation $I = C \times \frac{dv}{dt}$, we need to measure the current and voltage difference with respect to the elapsed time to calculate the capacitance value. In this experiment, the PMOS transistor width is $4\lambda$, and the NMOS transistor width is $2\lambda$. Inputs of the inverters are logic low. To make sure the current value measured is solely the charging current, temperature is set to $-200^\circ C$, in which the subthreshold
leakage of the transistor can be reduced to minimum. In the following part of this thesis, the temperature is always set to $-200\,^\circ C$. Gate leakage is also eliminated due to the assumption of high-k metal gate material.

1. NMOS capacitances

To calculate the gate capacitance of each NMOS transistor, we need to place a current source at the gate, which is shown in Fig. 2.10, and measure the voltage of $V_{gd}$. The gate capacitance is calculated as $C_{14} = 5.1 \times 10^{-18} \text{f}$. 

Figure 2.10: NMOS gate charging

To calculate the diffusion capacitance, we need to give a current source at base, which is shown in Figure 2.11, and measure the voltage of $V_{db}$ and $V_{sb}$ after some time. The diffusion capacitance values are calculated as $C_{13} = 10.9 \times 10^{-18} \text{f}, C_{15} = 22.3 \times 10^{-18} \text{f}$.

2. PMOS capacitances
There is only gate capacitance for the PMOS in an inverter circuit when the input voltage is logic low. By placing a current source at the gate of PMOS, shown in Figure 2.12, we get the gate capacitances $C_{11}=C_{12}=41.7 \times 10^{-18} \text{f}$. According to Figure 2.12, we finally have $C_5=10.9 \times 10^{-18} \text{f}$, $C_6=22.23 \times 10^{-18} \text{f}$, $C_7=88.5 \times 10^{-18} \text{f}$. For a circuit composed of 1000 minimum sized inverters, capacitance values are $C_5=10.9 \times 10^{-15} \text{f}$, $C_6=22.23 \times 10^{-15} \text{f}$, $C_7=88.5 \times 10^{-15} \text{f}$. For other circuits, we developed a tool to calculate these three capacitances.

### 2.3 Control transistor model

To eliminate interference factors, we assume that $T_1$ is off long before $T_2$ is on. An accurate model for $T_2$ is needed to analyze the circuit response. The timing diagram of the gate input signals $V_1$ and $V_2$ of control transistors $T_1$ and $T_2$ are shown in Fig. 2.13. The
transistor model of T2 is illustrated in Fig. 2.14. The current source $I_D$ is the drain current flowing through T2, and the four capacitances are the gate and diffusion capacitances of T2. We ignore the gate-to-body capacitance since most of time the transistor is working at linear and saturation mode. We also ignore transistor resistance to simplify the model. The model of control transistor is thus composed of one current source and four capacitors, gate-to-source (C1), gate-to-drain (C2), base-to-drain (C4), base-to-source (C3). The following sections give the detail of how to obtain those parameters.

![Figure 2.13: Timing of gate voltages of control transistors T1 and T2](image)

![Figure 2.14: Control transistor T2 model](image)

### 2.3.1 Control transistor drain current

A MOSFET transistor is a voltage controlled current source in nature. The drain current will change with working regions and supply voltages. In order to study the drain current, we need to analyze it in different working regions. Here, the bias voltage is set to be -0.26v.

As stated by Payam in [19], an inverter working as an output driver will work in four subintervals: two regions with ramp input, and two regions with constant input. When the transistor starts to switch, it is in cut-off region, and due to the large benchmark circuit capacitances, the output voltage will not change as fast as the input signal voltage. So after
$V_{gs}$ is larger than the threshold voltage, the transistor is working in saturation region. If only $V_{ds}$ is still large enough, which is tested to be 200mv in this experiment, the transistor will remain in saturation region. When $V_{ds}$ is less, the transistor will enter linear region.

In our experiments, the control circuit also has a large load capacitance by the benchmark circuit, so the four working regions can be also applied here. To verify this hypothesis, an inverter circuit shown in Fig. 2.7 has been tested. This circuit contains one thousand equivalent inverters. The control transistor is turned on in 0.01ns. $V_{ds}$ of the control transistor is always larger than 200mv during the entire rising time so that it is in saturation region at ramp input. When the inverter circuit is larger, the time that the circuit remains in saturation region is longer since the output will change more slowly due to the larger circuit load. After the input transition, the output voltage will continue decreasing and make the circuit step out of saturation region and enter into linear region, until the output voltage is zero. So in summary, the control transistor of the RBB technique works in four regions. The four regions are listed below [19]:

A. Ramp input
1. weak-inversion region
2. saturation region

B. Constant input
3. saturation region
4. linear region

The current equations provided by Payam of [19] are relatively complicated, so a set of simple equations have been proposed to reduce the computation complexity in this thesis. When the control transistor transition time $T$ is 0.01ns, we get current equations for four working regions:

$$I_D = \begin{cases} 
0 & (V_{gs} < V_T) \\
A \times (V_{gs} - V_0) & (t < T & V_{gs} \geq V_T) \\
A \times (V_{gs} - V_0) & (t \geq T & V_{ds} \geq V_{DSAT}) \\
B \times V_{ds} & (t \geq T & V_{ds} < V_{DSAT})
\end{cases}$$  \hspace{1cm} (2.4)
where A and B are transconductance in saturation and linear regions. A and B are constants when the working region and circuit bias voltage are determined. $V_T$ is the threshold voltage of the transistor, and $V_{DSAT}$ is the drain-source voltage at which velocity saturation is reached.

Now we discuss in detail about how to get those equations and their parameters. As stated in [4], the current equations for short channel transistor are different from those for the long channel transistor. For long channel transistors, current equations for linear and saturation regions are [4]:

$$I_D = \begin{cases} K_n[(V_{gs} - V_T)V_{ds} - \frac{V_{ds}^2}{2}] & \text{linear region} \\ \frac{k'_n}{2} \frac{W}{L} (V_{gs} - V_T)^2 (1 + \lambda V_{ds}) & \text{saturation region} \end{cases}$$ (2.5)

For short channel transistors, the current equation for linear region remains the same, but the equation for saturation region is different. Due to the velocity saturation phenomena, the current will saturate earlier as long as the saturation voltage is reached. The current equation for short channel transistor is then changed to [4]:

$$I_D = \begin{cases} K_n[(V_{gs} - V_T)V_{ds} - \frac{V_{ds}^2}{2}] & \text{linear region} \\ \upsilon_{sat} C_{ox} W (V_{gs} - V_T - \frac{V_{DSAT}}{2}) & \text{saturation region} \end{cases}$$ (2.6)

From this equation, the short channel transistor’s drain current in saturation region is linear to $V_{gs}$. $V_{ds}$ is so small that $\frac{V_{ds}^2}{2}$ can be ignored when a transistor is in linear region. In our case, $V_{gs}$ is a constant when the circuit is in linear region. So the current in linear region is linear to $V_{ds}$, and can be rewritten as:

$$I_D = \begin{cases} K_n(V_{gs} - V_T)V_{ds} & \text{linear region} \\ \upsilon_{sat} C_{ox} W (V_{gs} - V_T - \frac{V_{DSAT}}{2}) & \text{saturation region} \end{cases}$$ (2.7)

Further simplifying the equations, we have:

$$I_D = \begin{cases} B \times V_{ds} & \text{linear region} \\ A \times (V_{gs} - V_0) & \text{saturation region} \end{cases}$$ (2.8)

where $B = K_n(V_{gs} - V_T)$, $A = \upsilon_{sat} C_{ox} W$, and $V_0 = V_T + \frac{V_{DSAT}}{2}$. 

26
The following experiments are set up to get the coefficients A, B and $V_0$.

1. Saturation region

Experiment setup: A NMOS transistor with $V_{ds}=260\text{mv}$, width=$30\lambda$ is tested. The .DC sweep command is used in Hspice to get the drain current curve with respect to $V_{gs}$. The waveform of drain-source current with respect to $V_{gs}$ is illustrated in Fig. 2.15.

In Fig. 2.15, the drain-source current in saturation region is approximately linear to $V_{gs}$ when $V_{gs}$ is larger than 600mv. So the following function can be used to express the drain current in saturation region, which verify the Eq. 2.8.

$$I_D = A \times (V_{gs} - V_0)$$

(2.9)

where $A$ is the average slope under $V_{gs}$ from 600mv to 900mv. This equation is totally the same as equation 2.8, so we can get the coefficients for Eq. 2.8 from this Figure. We calculate slopes for a transistor with various widths 10, 20, 30, 50, 100, 200, 400$\lambda$, and take the average slope value for different widths as $A$. The result is listed in Table 2.4. If we take transistor width=$10\lambda$ as a reference, then we get the average slope ratio of different transistor widths to it. Table 2.5 shows the ratios. From this table, it can be observed that the slope is almost linear to the width. So we get Eq. 2.10 to calculate the slope for any control transistor width:

$$SLOPE_w = S \times SLOPE_{w0}$$

(2.10)

where we have $S = \frac{\text{width}}{10\lambda}$, and $SLOPE_{w0}$ is the slope when width is $10\lambda$. 

Figure 2.15: $I_D/V_{gs}$
Table 2.4: Slopes for different $V_{gs}$

<table>
<thead>
<tr>
<th>$V_{gs}$ (mv)</th>
<th>W=10($\lambda$)</th>
<th>W=20($\lambda$)</th>
<th>W=30($\lambda$)</th>
<th>W=50($\lambda$)</th>
<th>W=100($\lambda$)</th>
<th>W=200($\lambda$)</th>
<th>W=400($\lambda$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>950</td>
<td>2.74E-04</td>
<td>5.54E-04</td>
<td>8.33E-04</td>
<td>1.39E-03</td>
<td>2.79E-03</td>
<td>5.58E-03</td>
<td>1.12E-02</td>
</tr>
<tr>
<td>900</td>
<td>2.91E-04</td>
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<td>8.86E-04</td>
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<td>5.94E-03</td>
<td>1.19E-02</td>
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<tr>
<td>850</td>
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<td>9.26E-04</td>
<td>1.55E-03</td>
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<tr>
<td>800</td>
<td>3.13E-04</td>
<td>6.35E-04</td>
<td>9.57E-04</td>
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<td>3.21E-03</td>
<td>6.43E-03</td>
<td>1.29E-02</td>
</tr>
<tr>
<td>750</td>
<td>3.20E-04</td>
<td>6.51E-04</td>
<td>9.81E-04</td>
<td>1.64E-03</td>
<td>3.29E-03</td>
<td>6.60E-03</td>
<td>1.32E-02</td>
</tr>
<tr>
<td>700</td>
<td>3.26E-04</td>
<td>6.63E-04</td>
<td>1.00E-03</td>
<td>1.67E-03</td>
<td>3.36E-03</td>
<td>6.73E-03</td>
<td>1.35E-02</td>
</tr>
<tr>
<td>650</td>
<td>3.31E-04</td>
<td>6.73E-04</td>
<td>1.02E-03</td>
<td>1.70E-03</td>
<td>3.41E-03</td>
<td>6.83E-03</td>
<td>1.37E-02</td>
</tr>
<tr>
<td>600</td>
<td>3.30E-04</td>
<td>6.71E-04</td>
<td>1.01E-03</td>
<td>1.70E-03</td>
<td>3.40E-03</td>
<td>6.82E-03</td>
<td>1.36E-02</td>
</tr>
<tr>
<td>Average</td>
<td>3.11E-04</td>
<td>6.31E-04</td>
<td>9.51E-04</td>
<td>1.59E-03</td>
<td>3.19E-03</td>
<td>6.39E-03</td>
<td>1.28E-02</td>
</tr>
</tbody>
</table>

Table 2.5: Ratio of SLOPE with different width to basic width 10$\lambda$

<table>
<thead>
<tr>
<th>width($\lambda$)</th>
<th>W=10</th>
<th>W=20</th>
<th>W=30</th>
<th>W=50</th>
<th>W=100</th>
<th>W=200</th>
<th>W=400</th>
</tr>
</thead>
<tbody>
<tr>
<td>slope</td>
<td>1.00</td>
<td>2.03</td>
<td>3.06</td>
<td>5.12</td>
<td>10.27</td>
<td>20.56</td>
<td>41.15</td>
</tr>
</tbody>
</table>

Table 2.6 lists the value of $V_0$ for different transistor widths. There is no much difference among the values of $V_0$ for those different control transistor widths. So we take $V_0=0.495$ as a constant for any transistor width.

Table 2.6: $V_0$ for all transistor widths

<table>
<thead>
<tr>
<th>width($\lambda$)</th>
<th>W=10</th>
<th>W=20</th>
<th>W=30</th>
<th>W=50</th>
<th>W=100</th>
<th>W=200</th>
<th>W=400</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_0$</td>
<td>0.496</td>
<td>0.4955</td>
<td>0.4953</td>
<td>0.495</td>
<td>0.495</td>
<td>0.495</td>
<td>0.495</td>
</tr>
</tbody>
</table>

2. Linear region

Experiment setup: An NMOS transistor with $V_{gs}$=900mv, width=30$\lambda$ is tested. The .DC sweep command is used in Hspice to get the IV curve with respect to $V_{ds}$. The drain current waveform according to $V_{ds}$ is illustrated in Fig. 2.16.

According to Figure 2.16, when $V_{ds} \leq 200mv$, the current is approximately linear to $V_{ds}$, so we have the equation for the drain-source current when $V_{ds} \leq 200mv$:

$$I_D = B \times V_{ds}$$

(2.11)

where $B$ is the average slope under $V_{gs}$ from 600mv to 900mv. This equation is the same as Eq. 2.8, and therefore verifies it. Hspice simulations are used to get the coefficient $B$. With $V_{gs} = 0.9v$, width=30$\lambda$, and $V_{ds}$ changing from 20mv to 180mv, the slopes for different
widths (10, 20, 50, 100, 200, 400λ) are shown in Table 2.7. We take the average of the values in the table as $B$. In order to get a close-form equation to calculate $B$, we take transistor width equal to 10λ as a reference, and find the average slope ratio of different transistor widths in Table 2.8. From this table, the slope is almost linear to the transistor width. So we get Eq. 2.12 to calculate $B$ according to different transistor widths:

$$SLOPE_w = D \times SLOPE_{w0}$$  \hspace{1cm} (2.12)

where $D = \frac{\text{width}}{10\lambda}$ and $SLOPE_{w0}$ is the slope when the width is 10λ.
Since $V_{gs}$ is about 0.9v for most of the time in linear region, the slope is measured under $V_{gs}=0.9$. Also $V_{ds}$ is small for a large portion of time, so we measure the slope from $V_{ds}=20mv$ to $V_{ds}=100mv$. It is also applicable when the bias voltage is different, such as -0.8v,-0.4v,-0.2v. So we take the same $B$ value for any bias voltage. Now we obtain all coefficients for drain-source current equation.

### 2.3.2 Control transistor capacitances

Fig. 2.17 shows all parasitic capacitances of the control circuit. T1 is turned off and T2 is switched on. Their base are both connected to a bias voltage which is the lowest voltage (-0.26v and -0.8v in this thesis) in this circuit. T1 is off by connecting the gate to the bias voltage. For control transistor T2, there are totally four capacitances as stated before. During the low to high input transition at the gate of T2, two capacitances of transistor T1, C22 and C23 are added.

![Figure 2.17: Control transistor capacitances](image)

From Fig. 2.17 and Fig. 2.14, we have $C1=C24$, $C2=C26$, $C3=C25+C22+C23$, $C4=C27$. C22 and C23 are capacitances of drain-to-gate and drain-to-base of T1. All capacitances are proportional to the transistor width, and T1 and T2 control transistors have the same size. We calculate those capacitances for different control transistor widths and get Table 2.9:

All capacitances are measured in cut-off region, since those capacitances play an im-
Table 2.9: Capacitances for different transistor widths

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>c1(ff)</td>
<td>0.05</td>
<td>0.1</td>
<td>0.15</td>
<td>0.25</td>
<td>0.5</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>c2(ff)</td>
<td>0.063333</td>
<td>0.126667</td>
<td>0.19</td>
<td>0.316667</td>
<td>0.633333</td>
<td>1.26667</td>
<td>2.533333</td>
</tr>
<tr>
<td>c3(ff)</td>
<td>0.178667</td>
<td>0.357333</td>
<td>0.536</td>
<td>0.893333</td>
<td>1.78667</td>
<td>3.57333</td>
<td>7.146667</td>
</tr>
<tr>
<td>c4(ff)</td>
<td>0.094333</td>
<td>0.188667</td>
<td>0.283</td>
<td>0.471667</td>
<td>0.943333</td>
<td>1.886667</td>
<td>3.773333</td>
</tr>
</tbody>
</table>

important role when the control transistor is in cut-off region. Put the inverter circuit model, control circuit model and RLC parasitics model together, we finally get the RBB model for the inverter circuit which is shown in Figure 2.18. This model will be fed into Matlab, so that the circuit response can be calculated fast. The following part will discuss the Matlab solution in detail.

![RBB model for inverter circuit](image)

Figure 2.18: RBB model for inverter circuit

2.4 Matlab solution

Matlab is a powerful and fast tool to do numerical calculations. To resolve the problem in this thesis, a set of differential equations are generated to represent the circuit behaviors. Matlab utilizes ode45 Runge-Kutta to get the numerical solution for complicated second order and higher order differential functions. This method requires simplification of the higher order differential equations to the first order differential equations. Differential
equations for L, C, and R are listed below.

\[ v = L \frac{di}{dt} \quad (2.13) \]

\[ i = C \frac{dv}{dt} \quad (2.14) \]

\[ v = iR \quad (2.15) \]

Fig. 2.19 shows the RBB model with currents labeled. We use Kirchhoff’s current law (KCL) for nodes 2, 4, 6 and 7, and Kirchhoff’s voltage law (KVL) for nodes 2, 4, 6 to get a set of differential equations.

For node 2, KCL:

\[ \frac{v_1 - v_2}{r_1} - \frac{v_3 - v_4}{r_1} = C_8 \frac{dv_2 - dv_4}{dt} \quad (2.16) \]

For node 2, KVL:

\[ v_2 - v_4 = \frac{L_1}{r_1} \frac{dv_3 - dv_4}{dt} + (v_3 - v_4) \quad (2.17) \]

For node 4, KVL:

\[ v_4 = v_5 + \frac{L_2}{r_2} \frac{dv_5}{dt} \quad (2.18) \]

For node 4, KCL:

\[ \frac{v_1 - v_2}{r_1} - \frac{v_5}{r_2} = C_9 \frac{dv_4}{dt} \quad (2.19) \]
For node 6, KVL:
\[ v_6 = v_1 + \frac{L_1}{r_1} \frac{dv_1 - dv_2}{dt} \] (2.20)

For node 6, KCL:
\[ C_6 \left( \frac{dv_7 - dv_6}{dt} \right) - C_7 \frac{dv_6}{dt} + C_2 \left( \frac{dv_{in} - dv_6}{dt} \right) = I_D + C_4 \frac{dv_6}{dt} + \frac{v_1 - v_2}{r_1} \] (2.21)

for node 7, KCL:
\[ C_1 \left( \frac{dv_{in} - dv_7}{dt} \right) + I_D = C_3 \left( \frac{dv_7 - dv_{bias}}{dt} \right) + C_5 \frac{dv_7}{dt} + C_6 \left( \frac{dv_7 - dv_6}{dt} \right) \] (2.22)

Those seven differential functions need to be translated into Matlab-acceptable format. A separate command file in Matlab will set up the plotting environment and initial values. The simulation results by Matlab and Hspice will be compared in the following parts.

2.5 Simulation results

In this experiment, the circuit under test is composed of 1000 inverters (10 equivalent large inverters in Hspice file). Each PMOS transistor’s width is 4\( \lambda \) and each NMOS transistor’s width is 2\( \lambda \). They both have minimum length 2\( \lambda \). Control transistor width is 30\( \lambda \). The bias voltage is -0.26v, and the control transistor transition time is 0.01ns. Table 2.10 shows the ground bounce magnitude and wake up time by Hspice and Matlab. Fig. 2.20 and 2.21 shows the waveforms by Matlab and Hspice. Ground bounce magnitude and wake up time errors are 2% and 5.7% respectively. The waveforms of Matlab and Hspice show high similarity. Notice that in Hspice T1 is switched off 0.1ns before T2 is switched on, so there is 0.1ns before the ground bounce starts in Hspice waveform. But in Matlab, the initial circuit value before switching is directly set, and thus eliminate the 0.1ns setup time. So the ground bounce starts from 0.1ns in Hspice waveform and 0ns in Matlab waveform.

2.5.1 Model verification

The above simulation tests the RBB model when the circuit base is biased to -0.26v and the control transistor width is 30\( \lambda \). In order to verify the RBB model under different
Table 2.10: Simulation results

<table>
<thead>
<tr>
<th>Hspice</th>
<th>Ground bounce magnitude (mv)</th>
<th>Wake up time (e-10s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Matlab</td>
<td>19.25</td>
<td>0.6813</td>
</tr>
<tr>
<td>Error(%)</td>
<td>2</td>
<td>5.7</td>
</tr>
</tbody>
</table>

Figure 2.20: Matlab simulation waveform for $V_{gnd1}$ and $V_{base}$ situations, three groups of simulations are performed and the results obtained by Hspice and Matlab are compared.

a. The first experiment changes the control transistor width. We set the control transistor width to be 200, 100, 50, 20 and 10 λ, and compare the simulation results by Hspice and Matlab.

b. The second experiment changes the bias voltage. We set the bias voltage to be -1.2v, -0.8v, -0.4v, -0.3v, -0.2v, -0.1v, and compare the simulation results by Hspice and Matlab.

c. The third experiment changes the inductance values. Inductances L1 and L2 are shown in Fig 2.18. Initially their values are 8.9nH and 7nH. Table 2.11 shows eight different inductance value pairs which we will use in the simulation. We will simulate the eight groups of the inductance values and then compare the results.

Table 2.11: Different inductance values

<table>
<thead>
<tr>
<th></th>
<th>L1</th>
<th>L2</th>
<th>L1</th>
<th>L2</th>
<th>L1</th>
<th>L2</th>
<th>L1</th>
<th>L2</th>
<th>L1</th>
<th>L2</th>
</tr>
</thead>
<tbody>
<tr>
<td>inductance (nH)</td>
<td>8.9 35</td>
<td>8.9 1.4</td>
<td>44.5 7</td>
<td>44.5 35</td>
<td>44.5 1.4</td>
<td>1.78 7</td>
<td>1.78 35</td>
<td>1.78 1.4</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Tables 2.12, 2.13 and 2.14 show simulation results when we change control transistor
widths, bias voltages and inductance values. From Table 2.12, the RBB model has ground bounce magnitude and wake up time errors under 10% when the control transistor width is less than 200\(\lambda\). The ground bounce magnitude error is 11.7%, if the control transistor width is 200\(\lambda\). Let us trace back to the drain current source of the control transistor. In this model, we assume the transistor is conducting when \(V_{gs}\) is larger than \(v_0\) which is 0.495v. But actually when \(V_{gs}\) is less than \(v_0\), there is current flowing through the device. This current is proportional to the control transistor’s width. Fig. 2.22 shows the drain current with the transistor width equal to 30\(\lambda\) and 200\(\lambda\). The black region shows the current difference when \(V_{gs}\) is less than \(v_0\) between \(w = 30\lambda\) and \(w = 200\lambda\). It is obvious that the current in cut-off region in our definition is large when the control transistor width is large. So when the control transistor’s width is large, the RBB model tends to have larger error.

From Table 2.13, the RBB model is quite accurate when the bias voltage is larger than -1.2v and less than -0.1v. As stated before, the control transistor is considered in cut-off region when \(v_{gs}\) is less than \(v_0\). Parameter \(v_0\) is an approximate value and there exists current when \(v_{gs}\) is less than \(v_0\). Fig. 2.23 shows the drain current with respect to the
different bias voltages: -0.2v and -0.8v. The black region shows a significant difference of the drain currents between $V_{ds} = 0.2v$ and $V_{ds} = 0.8v$ when $V_{gs}$ is less than $v_0$. When $v_{ds}$ is large (i.e., the bias voltage is small, e.g., -1.2v), this current in cut-off region is too large to be ignored. So the result is not accurate if we ignore this large drain-source current when $v_{gs}$ is less than $v_0$. Also if $v_{ds}$ (i.e., the bias voltage is large, e.g., -0.1v) is too small, which means when the transistor is conducting, it will enter linear region directly, then the four section current source model is not accurate. So the RBB model is more suitable for circuits with the bias voltage from about -0.2v to 0.8v.

From Table 2.14, when we change the inductance values, the errors of the RBB model are always within 10%, and do not change too much. So inductance values do not affect the RBB model accuracy. In summary, the RBB model is proved to be accurate for the inverter circuit as long as its control transistor width is not larger than 200\(\lambda\) and its bias voltage is not lower than -0.8v. We will verify the RBB model for benchmark circuits in Chapter 3.
Figure 2.23: Drain current with different bias voltage

Table 2.14: Simulation results with different inductance values

<table>
<thead>
<tr>
<th>L1 L2</th>
<th>$V_{Gnd}$ negative magnitude (mv)</th>
<th>Error%</th>
<th>Wake up time (ns)</th>
<th>Error%</th>
</tr>
</thead>
<tbody>
<tr>
<td>8.9n</td>
<td>19.4 19.1</td>
<td>1.5</td>
<td>0.687 0.719</td>
<td>4.7</td>
</tr>
<tr>
<td>8.9n, 1.4n</td>
<td>19 19.1</td>
<td>0.5</td>
<td>0.675 0.7185</td>
<td>6.4</td>
</tr>
<tr>
<td>44.5n</td>
<td>22 22.4</td>
<td>1.8</td>
<td>1.0185 1.04</td>
<td>2.1</td>
</tr>
<tr>
<td>44.5n, 7n</td>
<td>22.4</td>
<td>2.2</td>
<td>1.0131 1.04</td>
<td>2.66</td>
</tr>
<tr>
<td>44.5n, 1.4n</td>
<td>21.88 22.4</td>
<td>2.4</td>
<td>1.003 1.04</td>
<td>3.7</td>
</tr>
<tr>
<td>1.78n, 7n</td>
<td>15.075 15.3</td>
<td>1.5</td>
<td>0.6176 0.66</td>
<td>6.9</td>
</tr>
<tr>
<td>1.78n, 35n</td>
<td>15.2 15.3</td>
<td>0.7</td>
<td>0.622 0.66</td>
<td>6.1</td>
</tr>
<tr>
<td>1.78n, 1.4n</td>
<td>14.865 15.3</td>
<td>2.9</td>
<td>0.6113 0.66</td>
<td>8</td>
</tr>
</tbody>
</table>
Chapter 3

RBB Model for Benchmark Circuits

In the last chapter, the inverter circuit model is composed of three capacitors: Vdd-to-gnd1, base-to-Vdd and base-to-gnd1, named C7, C5, and C6 respectively in Fig. 2.9. This circuit model for the inverter circuit is accurate. Now we will develop the model for all ISCAS85 benchmark circuits.

In the benchmark circuits, those transistors with global inputs whose voltage is logic low are connected to the global ground, instead of local ground (gnd1). The number of capacitances thus increases by 2: one is local_ground-to-global_ground, while the other is base-to-global_ground. Fig. 3.1 illustrates the capacitances of an NMOS transistor with a global ground input. Global ground and Vdd can be considered as a single point in transient analysis. So finally capacitor local_ground-to-global_ground can be added to capacitor Vdd-to-gnd1 (C7 in Fig. 2.9), and capacitor base-to-global_ground can be added to capacitor base-to-Vdd (C5 in Fig. 2.9). Thus, there are totally three equivalent lumped capacitors in RBB model for benchmark circuits, which is the same as the inverter circuit shown in Fig. 2.9.

The cell library of all benchmark circuits contains a variety of gate types. Some of them have large transistor stacks, so some internal nodes are floating under some input patterns. A NMOS transistor is a good conductor for logic low and a PMOS transistor is a good conductor for logic high, therefore some internal nodes will have voltage values different from the nominal voltages. Capacitances connected to those nodes need to be transformed...
3.1 Capacitances in benchmark circuits

The gate types of the benchmark circuits include AND, NAND, OR, NOR, XOR, INV, BUF. Each NMOS transistor width is assigned $7\lambda$, and each PMOS transistor width equals $14\lambda$ in all gates. The values of those capacitances are dependent on the circuit states, which are determined by the input vectors. Thus the circuit topology and input vectors are both needed to calculate the capacitances. Here the input vectors are randomly generated, and the same vectors will be used in the following part of this thesis. To make this model applicable for fast simulation and design automation, a capacitance table is generated according to all possible transistor states.

3.1.1 Capacitance tables

Transistor capacitances under all possible transistor states are calculated by a set of Hspice simulations. Tables 3.1 and 3.2 show capacitances for every NMOS and PMOS transistor state. In the tables, GDS represents the voltages of the gate, the drain and the source of a transistor. Values 0, 1, 4, 2 are assigned to the terminals (GDS) to represent
the connection to the local ground (gnd1), vdd, global ground (gnd), and the internal points with uncertain voltages respectively. For example, if a transistor’s gate, source and drain are connected to gnd, vdd and gnd1 respectively, then the GDS is 410. If a transistor’s drain or source is floating, then the floating source is called float2 and the floating drain is called float1.

Table 3.1: NMOS transistor capacitance in different states

<table>
<thead>
<tr>
<th>GDS</th>
<th>010</th>
<th>000</th>
<th>100</th>
<th>410</th>
<th>400</th>
<th>112</th>
<th>012</th>
<th>020</th>
<th>022</th>
<th>002</th>
<th>122</th>
<th>412</th>
<th>420</th>
<th>422</th>
<th>402</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cgnd1_vdd(ff)</td>
<td>0.024</td>
<td>0</td>
<td>0.12</td>
<td>0</td>
<td>0</td>
<td>0.024</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Cbase_vdd(ff)</td>
<td>0.038</td>
<td>0</td>
<td>0</td>
<td>0.038</td>
<td>0</td>
<td>0.045</td>
<td>0.038</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0.038</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Cbase_gnd1(ff)</td>
<td>0.077</td>
<td>0.12</td>
<td>0.12</td>
<td>0.067</td>
<td>0.11</td>
<td>0</td>
<td>0.011</td>
<td>0.077</td>
<td>0.01</td>
<td>0.05</td>
<td>0</td>
<td>0</td>
<td>0.067</td>
<td>0</td>
<td>0.04</td>
</tr>
<tr>
<td>Cbase_gnd1(ff)</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0.01</td>
<td>0.01</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0.01</td>
<td>0.01</td>
<td>0.01</td>
<td>0.01</td>
<td></td>
</tr>
<tr>
<td>Cgnd1_gnd1(ff)</td>
<td>0</td>
<td>0</td>
<td>0.04</td>
<td>0.08</td>
<td>0</td>
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<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0.037</td>
<td>0</td>
<td>0.037</td>
<td></td>
</tr>
<tr>
<td>Cvdd_float1(ff)</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0.0495</td>
<td>0</td>
<td>0.0495</td>
</tr>
<tr>
<td>Cvdd_float2(ff)</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0.05</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0.0495</td>
<td>0</td>
<td>0.0495</td>
<td></td>
</tr>
<tr>
<td>Cgnd1_float1(ff)</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0.027</td>
<td>0.027</td>
<td>0.027</td>
<td>0</td>
<td>0</td>
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<td>0</td>
</tr>
<tr>
<td>Cgnd1_float2(ff)</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0.039</td>
<td>0.039</td>
<td>0.039</td>
<td>0</td>
<td>0</td>
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<td>0.039</td>
</tr>
<tr>
<td>Cbase_float1(ff)</td>
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<td>0</td>
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<td>0</td>
<td>0</td>
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<td>0</td>
<td>0.039</td>
<td>0.039</td>
<td>0.039</td>
</tr>
<tr>
<td>Cbase_float2(ff)</td>
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<td>0</td>
<td>0</td>
<td>0</td>
<td>0.063</td>
<td>0.063</td>
<td>0</td>
<td>0.039</td>
<td>0.039</td>
<td>0.039</td>
<td>0.039</td>
<td>0</td>
<td>0</td>
<td>0.039</td>
<td>0.039</td>
</tr>
<tr>
<td>Cgnd_float1(ff)</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0.027</td>
<td>0.027</td>
<td>0</td>
</tr>
<tr>
<td>Cgnd_float2(ff)</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
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<td>0</td>
<td>0</td>
<td>0</td>
<td>0.027</td>
<td>0.027</td>
<td>0.027</td>
</tr>
</tbody>
</table>

Table 3.2: PMOS transistor capacitance in different states

| GDS   | 101 | 111 | 011 | 411 | 002 | 012 | 020 | 022 | 122 | 412 | 420 | 422 | 402 |
|-------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Cvdd_gnd1(ff) | 0.13 | 0.0279 | 0 | 0.13 | 0.13 | 0 | 0 | 0 | 0 | 0 | 0.078 | 0 |
| Cgnd_gnd1(ff) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0.08 | 0 |
| Cvdd_float1(ff) | 0 | 0 | 0 | 0 | 0 | 0.127 | 0.18 | 0.18 | 0 | 0.127 | 0.127 | 0.127 |
| Cvdd_float2(ff) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0.138 | 0.14 | 0.0825 | 0 | 0.08 |
| Cgnd1_float1(ff) | 0 | 0 | 0 | 0 | 0 | 0.096 | 0 | 0 | 0 | 0 | 0 | 0.098 | 0 | 0 |
| Cgnd1_float2(ff) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0.098 | 0 | 0 |
| Cgnd_float1(ff) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0.096 | 0.098 |
| Cgnd_float2(ff) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0.098 |

Let us take GDS=010, 000 and 420 in Table 3.1 as examples to explain how to get those data. The NMOS transistor capacitance diagram is illustrated in Figure 3.2. For GDS=010, the gate and source of the NMOS transistor are both connected to gnd1, so there are totally three capacitors: base-to-Vdd, base-to-gnd1 and gnd1-to-vdd. For GDS=000, transistor gate, source and drain are all connected to gnd1, so there are three base-to-gnd1 capacitors.
and these three capacitors can be lumped together as one capacitor. For GDS=420, there are five capacitors: base-to-float1, base-to-gnd1, base-to-Gnd, gnd1-to-Gnd and float1-to-Gnd. The values of those capacitors can be obtained by looking up the above capacitance table.

As discussed previously, the benchmark circuit model is also composed of three capacitances, which are the same as the inverter-only circuit. Once we have the capacitance table, we can do logic simulation for benchmark circuits and get the three capacitances. Note that the three capacitances of each benchmark circuit can be obtained by summing the corresponding capacitances of each transistor. We use the same input vectors as previous experiment and get the circuit capacitances for every benchmark circuit by Perl program. The capacitances of every benchmark circuit are shown in Fig. 3.3. In the following discussion, we will verify the capacitance table by simulating benchmark circuits using Hspice and Matlab.
3.2 Simulation results

In this experiment, the bias voltage is set to be -0.26v and control transistor widths are all 30\(\lambda\) for every benchmark circuit. Input vectors are the same as the above. Simulation results from Hspice and Matlab are listed in Table 3.3. In this experiment, the maximum and average ground bounce magnitude errors are 9.52% and 3.48% respectively, and the maximum and average wake up time errors are 17.60% and 4.87% respectively. This experiment proves the accuracy of capacitance table.

Table 3.3: Simulation results with bias voltage equal to -0.26v

<table>
<thead>
<tr>
<th>Benchmark circuit</th>
<th>Cap. C5(\text{ff})</th>
<th>Cap. C6(\text{ff})</th>
<th>Cap. C7(\text{ff})</th>
<th>Hspice time(ns)</th>
<th>Hspice magnitude (-mv)</th>
<th>Matlab time(ns)</th>
<th>Matlab magnitude(-mv)</th>
<th>Error(%)</th>
<th>Time error(%)</th>
<th>Hspice Matlab Simulation time(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>c432</td>
<td>5.33</td>
<td>39.21</td>
<td>77.90</td>
<td>0.06786</td>
<td>8.775</td>
<td>0.073</td>
<td>9.131</td>
<td>4.06</td>
<td>7.60</td>
<td>19.6 0.094</td>
</tr>
<tr>
<td>c499</td>
<td>18.08</td>
<td>82.58</td>
<td>184.37</td>
<td>0.13849</td>
<td>12.497</td>
<td>0.163</td>
<td>12.482</td>
<td>0.12</td>
<td>17.60</td>
<td>47.2 0.084</td>
</tr>
<tr>
<td>c880</td>
<td>17.49</td>
<td>76.95</td>
<td>173.16</td>
<td>0.15155</td>
<td>13.627</td>
<td>0.155</td>
<td>12.958</td>
<td>4.91</td>
<td>2.27</td>
<td>89 0.071</td>
</tr>
<tr>
<td>c1355</td>
<td>25.5</td>
<td>88.77</td>
<td>207.47</td>
<td>0.18021</td>
<td>14.009</td>
<td>0.195</td>
<td>15.342</td>
<td>9.52</td>
<td>8.20</td>
<td>79.2 0.073</td>
</tr>
<tr>
<td>c1908</td>
<td>27.01</td>
<td>139.17</td>
<td>361.68</td>
<td>0.2606</td>
<td>10.318</td>
<td>0.26</td>
<td>9.703</td>
<td>5.96</td>
<td>0.23</td>
<td>251.9 0.081</td>
</tr>
<tr>
<td>c2670</td>
<td>46.95</td>
<td>230.89</td>
<td>587.79</td>
<td>0.42746</td>
<td>10.184</td>
<td>0.425</td>
<td>10.179</td>
<td>0.05</td>
<td>0.58</td>
<td>492.4 0.12</td>
</tr>
<tr>
<td>c3540</td>
<td>64.52</td>
<td>323.74</td>
<td>825.90</td>
<td>0.59665</td>
<td>9.6767</td>
<td>0.605</td>
<td>10.012</td>
<td>3.47</td>
<td>1.40</td>
<td>1395.4 0.053</td>
</tr>
<tr>
<td>c5315</td>
<td>94.38</td>
<td>477.03</td>
<td>1188.15</td>
<td>0.86851</td>
<td>10.155</td>
<td>0.907</td>
<td>9.8543</td>
<td>2.96</td>
<td>4.43</td>
<td>1450.4 0.062</td>
</tr>
<tr>
<td>c6288</td>
<td>73.05</td>
<td>465.44</td>
<td>1062.62</td>
<td>0.79734</td>
<td>8.2109</td>
<td>0.82</td>
<td>8.464</td>
<td>3.08</td>
<td>2.84</td>
<td>1608.4 0.068</td>
</tr>
<tr>
<td>c7552</td>
<td>129.08</td>
<td>645.26</td>
<td>1667.80</td>
<td>1.2026</td>
<td>9.6569</td>
<td>1.245</td>
<td>9.5907</td>
<td>0.69</td>
<td>3.53</td>
<td>2385.5 0.126</td>
</tr>
</tbody>
</table>

In order to further verify its correctness, we conduct another experiment where the bias voltage is set to be -0.8v, and the control transistor width to be 200\(\lambda\). The same input vectors are used as the above. The experiment results of ten benchmark circuits are listed in Table 3.4. In this experiment, the maximum and average ground bounce magnitude errors are 9.73% and 5.17% respectively, and the maximum and average wake up time errors are 17.3% and 9.03% respectively. Most of the simulation results show that the error percentage between Hspice and Matlab is below 10%. From the simulation results, we can draw the conclusion that this RBB model can represent benchmark circuits well. It can be used to simulate circuits with bias voltage ranging from -0.26v to -0.8v. The Hspice simulation time is huge, especially when circuit size is large. It may take more than one hour to simulate benchmark C7552 by Hspice. However the simulation time by Matlab is
just a few seconds. Simulations based on this RBB model can greatly reduce the execution time. A few more experiments in the following part will be conducted to analyze the circuit behaviors.

Table 3.4: Simulation results with bias voltage equal to -0.8v

<table>
<thead>
<tr>
<th>test bench</th>
<th>Gate number</th>
<th>Hspice Wakeup time(ns)</th>
<th>Hspice magnitude(-mv)</th>
<th>Matlab Wakeup time(ns)</th>
<th>Matlab magnitude(-mv)</th>
<th>Magnitude error(%)</th>
<th>Time error(%)</th>
<th>Simulation time(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>c432</td>
<td>159</td>
<td>0.06357</td>
<td>54.672</td>
<td>0.068165</td>
<td>54.526</td>
<td>0.27</td>
<td>7.23</td>
<td>18.8</td>
</tr>
<tr>
<td>c499</td>
<td>170</td>
<td>0.1834</td>
<td>56.898</td>
<td>0.162</td>
<td>59.523</td>
<td>4.61</td>
<td>17.10</td>
<td>33.2</td>
</tr>
<tr>
<td>c880</td>
<td>382</td>
<td>0.15967</td>
<td>65.953</td>
<td>0.152</td>
<td>62.618</td>
<td>5.06</td>
<td>4.80</td>
<td>55.9</td>
</tr>
<tr>
<td>c1355</td>
<td>514</td>
<td>0.58714</td>
<td>69.4</td>
<td>0.58</td>
<td>75.334</td>
<td>8.55</td>
<td>1.22</td>
<td>61.6</td>
</tr>
<tr>
<td>c1908</td>
<td>879</td>
<td>0.2165</td>
<td>49.802</td>
<td>0.248</td>
<td>48.032</td>
<td>3.55</td>
<td>11.95</td>
<td>190.2</td>
</tr>
<tr>
<td>c2670</td>
<td>1267</td>
<td>0.41135</td>
<td>49.486</td>
<td>0.355</td>
<td>50.402</td>
<td>1.85</td>
<td>13.70</td>
<td>404.8</td>
</tr>
<tr>
<td>c3540</td>
<td>1668</td>
<td>0.8558</td>
<td>46.933</td>
<td>0.72</td>
<td>48.783</td>
<td>3.94</td>
<td>15.87</td>
<td>1088</td>
</tr>
<tr>
<td>c5315</td>
<td>2305</td>
<td>1.2288</td>
<td>47.941</td>
<td>1.11</td>
<td>52.6</td>
<td>9.72</td>
<td>9.67</td>
<td>1297.5</td>
</tr>
<tr>
<td>c6288</td>
<td>2177</td>
<td>0.9068</td>
<td>39.579</td>
<td>0.885</td>
<td>43.432</td>
<td>9.73</td>
<td>2.40</td>
<td>1208.4</td>
</tr>
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<td>c7552</td>
<td>3511</td>
<td>1.7088</td>
<td>50.095</td>
<td>1.6</td>
<td>47.896</td>
<td>4.39</td>
<td>6.37</td>
<td>2254.1</td>
</tr>
</tbody>
</table>

3.3 Ground bounce with different inductance values

Take benchmark circuit c7552 as an example, and set inductance values of L1 and L2 to: 8.9/7nH, 44.5/35nH, 222.5/175nH, and 1112.5/875nH. The bias voltage is -0.26v, and the control transistor width is 200λ. Experiment results are illustrated in Fig. 3.4.

![Simulation results for different inductance values](image)

Figure 3.4: Simulation results of C7552 with different inductance values

It is a misconception that larger inductance values will cause larger bouncing and thus
longer wake up time. While the ground bounce magnitude and wake up time do increase with larger inductance in this circuit, the effect is not so distinct. Inductance does not play a key role in this circuit.

Most of the current generated by the control transistor when the inverter base is switched to normal voltage is consumed by benchmark circuit capacitances: C5, C6 and C7, as we can see from the following analysis. The parasitic RLC circuit only gets a small portion of the total current. Now we label the currents flowing through the control transistor, three capacitances and the parasitic circuit as I1, I2, I3, I4, I5 separately, as shown in Fig. 3.5. Fig. 3.6 illustrates the total charge (from the very beginning to the wake up time) on all components in the circuit.

![RBB model with currents labeled](image1)

![Total charge with different inductances of C7552](image2)

It is obvious that the current which can flow outside of the benchmark circuit is quite
small. Current flowing into the RLC parasitic circuit is only about 1 percent of that flowing into the benchmark circuit. Fig. 3.7 illustrates the current on inductance L1 for circuit c7552.

![C7552 current on L1 with different inductance values](image)

Figure 3.7: Current on L1 with different inductances of C7552

It shows that the current flowing into the inductance L1 is small, whose maximum value is 3.5e-5A. The product of the inductance value and the rate of the current change ($L \times \frac{di}{dt}$) can only make a small voltage vibration (less than 1 mv). It is obvious that in this case the inductance value does not affect ground bounce magnitude too much due to the small current change rate. When the inductance value continues increasing, the maximum ground bounce magnitude will increase too. Firstly, when the inductance value is larger, its complex impedance is larger, and less current can pass through the inductance at the very beginning of the current change. According to Fig. 3.7, although the rate of the current change is larger when the inductance value is small, their product is still smaller than that of large inductances. Also capacitance between Vdd and gnd1 draws more current when the inductance value is larger. Fig. 3.8 illustrates the total charge ($I \times \Delta t$) on Cvdd_gnd1 (C7) when Vgnd1 is changing from 0 down to the maximum negative magnitude for different inductance values. According to equation $I \times \Delta t = C \times \Delta v$, when the current is larger, the voltage change will be larger. So the ground bounce negative magnitude will increase when inductance L1 is larger.

After some time, the fluctuation of the drain current of the control transistor tends to cease and cannot charge up the circuit. Finally the parasitic RLC circuit starts to charge up gnd1 and the base. Due to the large parasitics in this RLC circuit, the charging process is
slow. It takes more time to charge the local ground (gnd1) back to nominal voltage if we increase the inductance value, 

3.4 Ground bounce with different bias voltage and control transistor width

We take benchmark circuit c7552 as an example. The bias voltage is set to -0.26v, -0.4v, and -0.8v respectively. The control transistor width is assigned to 30, 200, 400, 800λ. The input vector is the same as the above. Ground bounce magnitude and wake up time are shown in Fig. 3.9 and Fig. 3.10.

The ground bounce will increase initially with increasing control transistor width. However when the control transistor width is larger than 200λ, it is affected little by the control
transistor width. The wake up time will decrease with the increase of the control transistor width at first, and is affected little when the control transistor width is larger than 200\(\lambda\). A larger control transistor width introduces a larger drain current, and this larger current may cause the drain (gnd1) voltage of control transistor to be pulled down rapidly by its source voltage (base). But as we stated before, the increase of drain current does not guarantee the larger voltage drop in vgn\(d\)1. According to Fig. 3.9 and 3.10, we have observed that when the control transistor width is large enough, the local ground voltage cannot be pulled down any more. Usually, if the bias voltage is smaller, the wake up time is larger, and the ground bounce magnitude is larger. Since when the bias voltage is larger in magnitude, the local ground voltage (vgn\(d\)1) will be pulled down more and thus the magnitude will be larger and the circuit need more time to charge the local ground voltage back to zero.
Chapter 4

Positive Ground Bounce by RBB

As we can see from Chapter 2 and Chapter 3, the ground bounce in RBB is a negative value. However in most published papers for PG, the ground bounce is positive [23, 17, 18]. In this chapter, we analyze the positive ground bounce phenomenon. Let us first take a look at an inverter circuit with the RBB technique whose base is connected to the global ground (Gnd), instead of a local ground, as shown in Fig. 4.1. Just take the same analysis procedure as in the previous chapters, we get the RBB model for this circuit, illustrated in Fig. 4.2. The parasitic RLC for the global ground is ignored. In Fig. 4.2, C1 is the capacitance between the gate (V2) and the drain (Gnd), C2 is the one between the gate (V2) and the source (Base), and C3 is the one between the control transistor base (Bias) and the source (Base). There is no capacitance between the control transistor base (Bias) and the drain (Gnd), since both of the two points have the constant voltages. The capacitance between the gate (V2) and the control transistor base (Bias) is ignored since the control transistor works in saturation and linear regions for most of time.

4.1 Matlab model

According to the circuit model above, we use the Kirchhoff’s current law (KCL) for nodes 2, 4, 6 and 7, and the Kirchhoff’s voltage law (KVL) for nodes 2, 4, 6 to get a set of differential equations, which is used in the Matlab simulation.
for node 2, KCL:

\[
\frac{v_1 - v_2}{r_1} - \frac{v_3 - v_4}{r_1} = C_8 \frac{dv_2 - dv_4}{dt}
\]  

(4.1)

for node 2, KVL:

\[
v_2 - v_4 = \frac{L_1}{r_1} \frac{dv_3 - dv_4}{dt} + (v_3 - v_4)
\]  

(4.2)

for node 4, KVL:

\[
v_4 = v_5 + \frac{L_2}{r_2} \frac{dv_5}{dt}
\]  

(4.3)
for node 4, KCL:

\[
v_1 - \frac{v_2}{r_1} - \frac{v_5}{r_2} = C_9 \frac{dv_4}{dt}
\] (4.4)

for node 6, KVL:

\[
v_6 = v_1 + \frac{L_1}{r_1} \frac{dv_1 - dv_2}{dt}
\] (4.5)

for node 6, KCL:

\[
C_2 \frac{dv_{in} - dv_7}{dt} + I - C_3 \frac{dv_7}{dt} - C_5 \frac{dv_7}{dt} - C_6 \frac{dv_7 - dv_6}{dt}
\] (4.6)

for node 7, KCL:

\[
C_6 \frac{dv_7 - dv_6}{dt} - C_7 \frac{dv_6}{dt} - \frac{v_1 - v_2}{r_1}
\] (4.7)

### 4.2 Simulation results

In this experiment, the control transistor width is set to 200λ, and the bias voltage is -0.8v. Fig. 4.3 and Fig. 4.4 show the simulation waveforms of c432 by Hspice and Matlab. The ground bounce is positive. According to Fig. 4.1 and Fig. 4.2, when T2 is switched on, the base voltage will be pulled up by Gnd. As we know, the voltage on the capacitance cannot change abruptly. So gnd1 will increase with the base due to capacitance C6. In consequence there is a positive ground bounce. The simulation results are shown in Table 4.1. The maximum error is 17.2%. The simulation time of Matlab is substantially smaller than that of Hspice, especially when the benchmark circuit is large. This Matlab model is good for fast simulation, and can be implemented as a CAD tool to get the circuit response quickly.

### 4.3 Ground bounce with different inductance values

We now test the ground bounce for benchmark circuit c7552 with different parasitic inductance values. The inductance values of L1 and L2 are: 8.9/7nH, 44.5/35nH, 222.5/175nH, and 1112.5/875nH. The bias voltage is -0.26v, the control transistor width is 30λ. Experiment result is illustrated in Fig. 4.5. In this experiment, ground bounce magnitude increases
Figure 4.3: Simulation waveforms of c432 by Hspice

Figure 4.4: Simulation waveforms of c432 by Matlab

Table 4.1: Simulation results for ten benchmark circuits

<table>
<thead>
<tr>
<th>benchmark circuit</th>
<th>$V_{gnd1}$ Magnitude(mv)</th>
<th>Error%</th>
<th>Wake up time (ns)</th>
<th>Error%</th>
<th>Simulation time (s)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Hspice</td>
<td>Matlab</td>
<td>Hspice</td>
<td>Matlab</td>
<td>Hspice</td>
</tr>
<tr>
<td>c432</td>
<td>241.36</td>
<td>246.69</td>
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<td>1.5279</td>
<td>1.7272</td>
</tr>
<tr>
<td>c499</td>
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<td>5.56</td>
<td>1.1335</td>
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</tr>
<tr>
<td>c880</td>
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<td>227</td>
<td>6.5</td>
<td>1.1362</td>
<td>1.23</td>
</tr>
<tr>
<td>c1355</td>
<td>208.6</td>
<td>218.57</td>
<td>4.76</td>
<td>1.179</td>
<td>1.02</td>
</tr>
<tr>
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<td>183.95</td>
<td>200.72</td>
<td>9.12</td>
<td>1.3527</td>
<td>1.12</td>
</tr>
<tr>
<td>c2670</td>
<td>191.25</td>
<td>199</td>
<td>4.05</td>
<td>1.9796</td>
<td>1.72</td>
</tr>
<tr>
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<td>4.70</td>
<td>2.5341</td>
<td>2.28</td>
</tr>
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<td>197.73</td>
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</tr>
<tr>
<td>c6288</td>
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<td>210.31</td>
<td>1.60</td>
<td>3.289</td>
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</tr>
<tr>
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<td>183.36</td>
<td>192.52</td>
<td>5.00</td>
<td>4.588</td>
<td>4.2</td>
</tr>
</tbody>
</table>

with the inductance value. According to the Eq. $v = L \frac{di}{dt}$, a larger inductance value will cause a larger voltage drop, so the ground bounce magnitude is larger. Furthermore, a larger ground bounce needs more time to settle down. When the inductance values are 8.9/7nH, 44.5/35nH, 222.5/175nH respectively, there is no much difference in wake up time. How-
ever when inductance value is 1112.5/875nH, the wake up time increases dramatically.

Figure 4.5: Simulation results for c7552 with different inductance values

4.4 Ground bounce with different bias voltage and control transistor width

We take benchmark circuit c7552 as an example. The bias voltage is assumed to be -0.26v, -0.4v, and -0.8v, and the control transistor width is 30, 200, 400, 800λ respectively. The ground bounce magnitude and the wake up time are shown in Fig. 4.6 and Fig. 4.7.

Figure 4.6: Ground bounce magnitude of c7552

Compared to the simulation results in Chapter 3, the circuit has similar responses to different inductance values, bias voltages and control transistor widths. The only difference is that the ground bounce value here is positive, while in Chapter 3, the ground bounce value is negative. In the real chip design, the circuit base would probably be connected
Figure 4.7: Wakeup time of c7552

to a local ground, and the corresponding negative ground bounce would not affect circuit too much. So optimization will be applied only to circuits with its base connected to the global ground. In Chapter 6, optimization techniques will be discussed in detail for the RBB circuit.
Chapter 5

PG Model

In this chapter, we will discuss the ground bounce behavior of the PG technique and compare it with the RBB technique. A PG model is developed to get fast simulation of circuit behaviors. Once we have both PG model and RBB model, the ground bounce magnitudes and wake up times of PG and RBB can be compared quickly such that we can make design decisions easily. Same as the development of the RBB model, we firstly analyze an inverter circuit with the PG technique. In order to simplify the analysis, the PG technique is only applied to the ground, the same as the RBB technique. For consistency, we will try to maintain the terminal labeling using the same sequence as in the RBB model. The inverter circuit is shown in Fig. 5.1. The benchmark circuit enters the sleep mode when the sleep transistor is switched off, and the normal mode when the sleep transistor is switched on. According to the circuit diagram, the circuit can be split into three blocks as shown in Fig. 5.2, just like in the RBB technique. According to this diagram, we get the model for every block.

5.1 PG model for inverter circuit

Taking the same parasitic circuit model as in the RBB model, we get the PG model shown in Fig. 5.3 for the inverter circuit. Assume the input of the inverter is logic low, we analyze all of the capacitances of the inverter, which is the same as the case of RBB and
From the capacitance diagram of the inverter circuit, we can derive the inverter circuit model by lumping the same capacitances together, as shown in Fig. 2.9. For inverters which have logic high input voltage, the same inverter model can be used too.

The sleep transistor in PG is slightly different from the control transistor in the RBB technique. Its base and source terminals are connected to one point, named Base in our design. So there are totally three capacitances in the sleep transistor model as shown in Fig. 5.4, where $I_D$ is the drain current of the sleep transistor, C1 and C2 are the gate capacitances.
capacitances and C3 is the diffusion capacitance of the sleep transistor. The method to calculate those capacitance values is the same as in RBB, so the detailed calculation will be omitted here.

The current source of the sleep transistor needs to be carefully modeled. The four section current source that we discussed in Chapter 2 is no longer accurate for the PG technique. Firstly, PG will cause a larger ground bounce than RBB as we can see in the following part. Even when the sleep transistor is only 30λ wide, it can cause more than 100mv of ground bounce. In RBB, the four section current model gives four different current equations according to different $V_{gs}$ and $V_{ds}$ values. In each equation, we assume either $V_{ds}$ or $V_{gs}$
remains constant. However in PG, this assumption is not acceptable since both $V_{ds}$ and $V_{gs}$ fluctuate severely. In order to resolve this problem, we provide a better piecewise model to express the current source of the sleep transistor. Now assume the sleep transistor width is $30\lambda$. The drain current of the NMOS transistor with different $V_{gs}$ and $V_{ds}$ is shown in Fig. 5.5.

![Figure 5.5: I/V curves of sleep transistor](image)

From this chart, the drain current is quite small when $V_{gs}$ is less than 0.5v, so we assume there is no drain current when $V_{gs}$ is less than 0.45v. When $V_{gs}$ is larger than 0.45v, we split transistor states into five regions according to $V_{gs}$: 0.45v-0.55v, 0.55v-0.65v, 0.65v-0.75v, 0.75v-0.85v, 0.85v-0.9v. We then use $V_{gs}$ equals 0.5v, 0.6v, 0.7v, 0.8v, 0.9v to derive the parameters for the current equations in those different regions. Now we take $V_{gs}$ equals 0.9v as an example to illustrate the calculation process, and the I/V curve is shown in Fig. 5.6.

![Figure 5.6: Drain current of sleep transistor with vgs=0.9v](image)

Two straight lines are used to represent the currents in linear and saturation regions. The
largest error of this model occurs when the transistor is working between saturation region and linear region. Other than that, these two lines can express the current accurately. The equation for the drain current under \( V_{gs} \) equals 0.9v is:

\[
I_D = \begin{cases} 
A \times (V_{ds}) & \text{linear region} \\
B \times (V_{ds}) + V_0 & \text{saturation region}
\end{cases}
\]  

(5.1)

where A is equal to 2.5e-3, B is equal to 3e-4, and \( V_0 \) is equal to 3.17e-4. Following this method, we calculate the parameter values for all \( V_{gs} \) regions. But for \( V_{gs} = 0.5v \), the situation is slightly different. Since \( V_{gs} \) is small, it is easy to enter the saturation region even with a small \( V_{ds} \). We assume when \( V_{gs} \) is around 0.5v, the circuit will enter saturation region once there is a small voltage difference between the drain and source terminals. Fig. 5.7 shows a straight line which can express the I/V curve when \( V_{gs} \) is 0.5v. Table 5.1 shows all the parameter values.

![Figure 5.7: Drain current of sleep transistor with vgs=0.5v](image)

<table>
<thead>
<tr>
<th>( V_{gs} ) (v)</th>
<th>A</th>
<th>B</th>
<th>( V_0 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.9</td>
<td>2.513E-3</td>
<td>3E-04</td>
<td>3.17E-04</td>
</tr>
<tr>
<td>0.8</td>
<td>2.575E-03</td>
<td>2.81E-04</td>
<td>2.277E-04</td>
</tr>
<tr>
<td>0.7</td>
<td>2.15E-03</td>
<td>2.68E-04</td>
<td>1.316E-04</td>
</tr>
<tr>
<td>0.6</td>
<td>1.38E-03</td>
<td>2.58E-04</td>
<td>0.326E-04</td>
</tr>
<tr>
<td>0.5</td>
<td>1.5E-4</td>
<td>/</td>
<td>/</td>
</tr>
</tbody>
</table>

Table 5.1: Parameters for current equations with different \( V_{gs} \).

According to the discussion above, we can get the model for the inverter circuit with the PG technique. Fig. 5.8 shows the circuit model for PG, which looks similar to the one in
the RBB model. Once we get all of the capacitance values for this model, we can compare
the simulation results by Hspice and Matlab.

![Figure 5.8: PG model](image)

**5.2 Matlab solution**

Similar to the case in RBB, a set of differential equations are derived to represent the
circuit behavior of Fig. 5.8. We use the Kirchhoff’s current law (KCL) for nodes 2, 4, 6
and 7, and the Kirchhoff’s voltage law (KVL) for nodes 2, 4, 6 in Fig. 5.8, and get the
differential equations for the PG model.

for node 2, KCL:

\[ \frac{v_1 - v_2}{r_1} - \frac{v_3 - v_4}{r_1} = C_8 \frac{dv_2 - dv_4}{dt} \]  \hspace{1cm} (5.2)

for node 2, KVL:

\[ v_2 - v_4 = L_1 \frac{dv_3}{r_1 dt} + (v_3 - v_4) \]  \hspace{1cm} (5.3)

for node 4, KVL:

\[ v_4 = v_5 + L_2 \frac{dv_5}{r_2 dt} \]  \hspace{1cm} (5.4)

for node 4, KCL:

\[ \frac{v_1 - v_2}{r_1} - \frac{v_5}{r_2} = C_9 \frac{dv_4}{dt} \]  \hspace{1cm} (5.5)
for node 6, KCL:
\[ C_1 \left( \frac{dv_{in} - dv_6}{dt} \right) - I_D - C_3 \left( \frac{dv_6 - dv_7}{dt} \right) - C_5 \frac{dv_6}{dt} = C_6 \left( \frac{dv_6 - dv_7}{dt} \right) \] (5.6)

for node 7, KVL:
\[ v_7 = v_1 + \frac{L_1}{r_1} \frac{dv_1 - dv_2}{dt} \] (5.7)

for node 7, KCL:
\[ C_6 \left( \frac{dv_6 - dv_7}{dt} \right) - C_7 \frac{dv_7}{dt} + C_2 \left( \frac{dv_{in} - dv_7}{dt} \right) + I_D + C_3 \left( \frac{dv_6 - dv_7}{dt} \right) = \frac{v_1 - v_2}{r_1} \] (5.8)

Those seven differential functions can be translated to a matlab-acceptable format. A separate command file will set up the plotting environment and initial values. Now we have the Matlab solution for the inverter circuit PG model, so we can conduct an experiment to compare this PG model with Hspice simulation.

### 5.3 Inverter circuit experiment results

Now assume we have a circuit composed of 1000 inverters which use PG to reduce leakage power consumption. The circuit will wake up from sleep mode, and the input of those inverters are assigned logic high. Fig. 5.9 and Fig. 5.10 show the ground and base bounce magnitudes calculated by Hspice and Matlab respectively. In these two charts, the simulation waveforms obtained from Hspice and Matlab are quite similar to each other. Table 5.2 shows the simulation results and errors represented by percentage. From Table 5.2, the simulation results of Matlab is within 10% error with respect to Hspice results.

<table>
<thead>
<tr>
<th>( V_{gnd} ) magnitude (v)</th>
<th>Error%</th>
<th>( V_{base} ) magnitude (v)</th>
<th>Error%</th>
<th>Wake up time (ns)</th>
<th>Error%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hspice</td>
<td>Matlab</td>
<td>Hspice</td>
<td>Matlab</td>
<td>Hspice</td>
<td>Matlab</td>
</tr>
<tr>
<td>0.2944</td>
<td>0.29576</td>
<td>0.46</td>
<td>0.11928</td>
<td>0.12885</td>
<td>8</td>
</tr>
</tbody>
</table>
5.4 Benchmark circuits

In the ISCAS85 benchmark circuits, all transistors have three possible gate inputs: $V_{dd}$, local ground (gnd1), or global ground (Gnd), which is the same as RBB. Since $V_{dd}$ and Gnd can be considered as one single point in transient analysis, there are totally three capacitances in the PG model for every benchmark circuit. This is the same as the inverter circuit model. From the above analysis, for each benchmark circuit, the circuit model for PG is the same as that for RBB.

Applied the same input vectors, each of the ten benchmark circuits has the same capacitance (i.e., C5, C6, and C7) as listed in Table 3.3. As stated in Chapter 1, the sleep transistor width of the PG technique should be large enough so that it will not affect the circuit speed in normal operation mode. But this thesis is aimed at comparing the circuit responses between RBB and PG, so we assign $200\lambda$ as the sleep transistor width in the experiment. The input transition time of the sleep transistor is also set to be 0.01ns. The
The maximum error occurred in the wake up time of the benchmark circuit c432. Since c432 has small capacitances, inductances play a very important role, and induce a significant ground bouncing. The simulation waveforms of c432 and c499 are shown in Fig. 5.11. It shows that c432 has more voltage fluctuation than c499 as time elapses. The wake up time is defined as when the local ground voltage is within $\pm 13\text{mv}$ to be consistent with RBB, which is too small compared with its bounce magnitude of PG. In most published papers focused on the ground bounce of PG take $\pm 45\text{mv}$, which is the 5\% of the nominal voltage of Vdd, as the criterion for the wake up time. For other circuits which have larger capacitances, the errors are relatively small.

Compare simulation results of RBB and PG in Table 3.4 and Table 5.3, we observe that when we use the same sized transistor to activate the same benchmark circuit, the ground bounce magnitude of RBB is just about one fourth of that of PG, and the wake up time of RBB is much less than that of PG, especially benchmark circuit c432 whose wake up time of RBB is less than 0.2\% of that of PG. When we need to determine which low power technique, RBB or PG, should be applied to a certain circuit, we can use the two models to predict the circuit response. When considering jointly with the switching power consumption and power reduction effectiveness of RBB and PG, we can then derive a good solution for a specific circuit, and is very useful in design automation.
Figure 5.11: Simulation waveform of c432 and c499
Chapter 6

Optimization for RBB

6.1 Optimization for RBB with base connected to local ground

The wake up time of a large circuit switching back to normal mode under RBB is usually quite large. In benchmark circuit c7552, it is around 1.8ns with -0.8v bias voltage and 200$\lambda$ control transistor width. In order to reduce the wake up time, some optimization methods are provided in this chapter.

Firstly, let us take a look at the simulation waveform of benchmark circuit c7552, shown in Fig. 6.1. The ground bounce waveform can be split in to two phases, decrease phase and increase phase. There is no inductance-induced voltage bounce in this circuit since

Figure 6.1: Ground bounce waveform of c7552
the circuit capacitances are too large and dominate. The voltage drops sharply at the very beginning and then increases slowly until it reaches voltage zero. During the voltage drop phase, the drain (local ground) and source (base) voltages of the control transistor are pulled toward each other. It thus causes the local ground (gnd1) voltage to drop and the base voltage to increase. When the drain-source voltage of the control transistor is small enough, there is no much drain current flowing in the transistor, and the local ground voltage will stop decreasing and both of the source and the drain voltages will be charged back to zero slowly. Fig. 6.2 shows the gnd1 and base voltages: the red line represents the gnd1 voltage and the black line represents the base voltage. Fig. 6.3 shows part of the curves between magnitude [-50mv, 0v], so that we can see clearly that the gnd1 voltage and the base voltage are similar to each other after 0.3ns. Table 6.1 shows the voltage of gnd1 and base after 0.2831ns, and the voltage difference is within 3mv after 0.3039ns.

![Figure 6.2: Base and gnd1 waveforms](image)

Fig. 6.4 shows the circuit diagram. We assume the gnd1 and the base are a single point after 0.3039ns since the voltage difference between them is quite small (less than 3mv). Then the control transistor and C6 are ignored. The capacitances of c7552 (C5 and C7)
can be considered as a large capacitance between gnd1 and Vdd as shown in Fig. 6.5. The value of $C_L$ is 1797fF. Since inductances do not play an important role in c7552, we ignore them in the following analysis. The circuit diagram can be revised to Fig. 6.6. We derive a set of differential equations for the circuit:

for node 6, KCL:

$$-C_L \frac{dv_6}{dt} = \frac{v_6 - v_2}{r_1}$$ (6.1)

for node 2, KCL:

$$\frac{v_6 - v_2}{r_1} = \frac{v_2 - v_4}{r_1} + C_8 \frac{dv_2 - dv_4}{dt}$$ (6.2)

for node 4, KCL:

$$\frac{v_4}{r_2} + C_9 \frac{dv_4}{dt} = \frac{v_6 - v_2}{r_1}$$ (6.3)

We put differential equations into Matlab and get the simulation waveform of gnd1 starting from 0.3039ns. The initial conditions of the differential equations will be taken from the Matlab simulation result of the RBB model at 0.3039ns. At that time, $V_{gnd1}$ is -44.89mv, $V_2$ is -48.15mv and $V_4$ is 7.85mv. The gnd1 waveform shown in the red line in
Fig. 6.7 is compared to the waveform by our previous RBB model shown in the black line. We can see that there is only limited difference in the simulation waveforms, so it verifies our assumption. Actually the model can be further simplified by eliminating C8 and C9, since these two capacitances are small under the frequency of the increase phase and can be considered as open.

Since the value of $C_L$ is very large, the wake up time is quite large. According to the previous analysis, the wake up time is mainly determined by the benchmark circuit and parasitic capacitances and parasitic resistance. So the optimization of wake up time
becomes the problem of:

1. Reducing $C_L$

2. Reducing R, including on-chip and package parasitic resistance

3. Adding an extra voltage source

Splitting a circuit into several blocks can reduce $C_L$ only when each block has a separate local ground. Enlarging on-chip wire width will help reduce the resistance, but due to the limited chip area, this method may not be applicable. Adding an extra voltage source to speed up the charging process may introduce more power consumption and thus can only be used when power consumption is not a key issue in circuit design. As we discussed in Chapter 3, a circuit will not be affected too much by small negative ground bouncing, so we will discuss the optimization methods for RBB with circuit base connected to global ground.

### 6.2 Optimization for circuits with base connected to global ground

As we discussed in Chapter 4, the ground bounce is a positive value when the circuit base is connected to the global ground. A positive ground bounce will bring about smaller
noise margin and transition speed. The circuit is considered to be settled down when the local ground bouncing magnitude is within $\pm 13\text{mv}$ in this thesis. To reduce the effect of ground bouncing, the ground bounce magnitude and wake up time should both be reduced as much as possible.

The ground bounce of benchmark circuit c7552 is shown in Fig. 6.8. The local ground voltage increases first and then decreases, and the increasing slope is much steeper than the decreasing slope. According to Fig. 4.2, when the control transistor is conducted, the base voltage will be pulled up, and the local ground voltage will also increase due to the capacitance between the local ground and the base. If the base voltage increases fast, the local ground voltage will also increase fast and bring about a large local ground bounce. Unfortunately, a large ground bounce magnitude will cause long wake up time, so we need to reduce the magnitude in increase phase in order to reduce the wake up time. In the decrease phase, the local ground voltage discharges so slowly and takes up a large percentage of total wake up time.

Fig. 6.8: Ground bounce waveform of c7552

Fig. 6.9 shows the circuit diagram. According to Fig. 6.10, the base is pulled to zero rapidly, which means that the base can be considered as the same point as Gnd in the decrease phase. So we can ignore the control transistor in the decrease phase. Also the capacitance $C_5$ can be ignored since Vdd and Gnd can be considered as a single point in the transient analysis. We then have a equivalent capacitance between gnd1 and Vdd which is the equal to the summation of $C_7$ and $C_6$, as shown in Fig 6.11. Finally we have a
simplified model for the circuit under RBB in the decrease phase as shown in Fig. 6.12. Obviously circuit connected to the global ground has the same equivalent circuit during charging back to zero as the circuit connected to the local ground. We put differential equations into Matlab and get the simulation waveform of gnd1 starting from 0.2736ns. The gnd1 waveform shown in the red line in Fig. 6.13 is compared to the waveform by our previous RBB model shown in the black line. We can see that there is only limited difference in the simulation waveforms, so it verifies our assumption. So according to Fig. 6.12, we also have three methods to reduce the wake up time.

Figure 6.9: Circuit diagram of c7552

Figure 6.10: Base and gnd1 waveforms
1. Reducing $C_L$

Since benchmark circuit c432 only takes 1.5ns to wake up while c7552 needs 5ns, and the only difference between benchmark circuit c7552 and c432 is the value of $C_L$, we will try to reduce $C_L$. In the previous simulations, the circuit base is connected to one single point and uses one control transistor to connect to the global ground. Here we divide the circuit base into several points and connect them to different control transistors. The idea is that we can divide the big $C_L$ into several small $C$, so the wake up time will be reduced.

The base of benchmark circuit C7552 has been divided into 2-6 parts as shown in Table 6.2, and every base point is connected to a separate control transistor. Every control transistor has width equal to 30 $\lambda$. Table 6.2 shows the simulation results. As we can see from the table, the wake up time of ground bounce does not change too much. In another word, partitioning the circuit into several base points does not result in much improvement in the wake up time. Let us discuss the partitioned circuit diagram in Fig. 6.14. Here we ignore the control transistors which connect the bias and base, since they remain switched off during circuit mode transition. Although we tried to partition the circuit into several parts, the capacitance between gnd1 and Vdd remains constant. That is, those subcircuits are still connected together. Especially when the base has its voltage charged back to zero, there is no voltage difference between each control transistor’s drain and source terminals.
So there is no driving current flowing through this control transistor any more, and the control transistor provides no benefit when discharging local ground back to zero. So in decrease phase, there is no difference between partitioned and unpartitioned circuits. As we stated before, the decrease phase time is dominant in the total wake up time, so this partition method is not suitable for RBB.

Table 6.2: Simulation results by different partitions

<table>
<thead>
<tr>
<th>partition</th>
<th>total transistor width</th>
<th>Ground bounce magnitude</th>
<th>Wake up time</th>
</tr>
</thead>
<tbody>
<tr>
<td>none</td>
<td>30λ</td>
<td>115.87mv</td>
<td>5.03ns</td>
</tr>
<tr>
<td>2</td>
<td>60λ</td>
<td>144.14mv</td>
<td>4.86ns</td>
</tr>
<tr>
<td>3</td>
<td>90λ</td>
<td>160.99mv</td>
<td>4.77ns</td>
</tr>
<tr>
<td>4</td>
<td>120λ</td>
<td>169.40mv</td>
<td>4.73ns</td>
</tr>
<tr>
<td>5</td>
<td>150λ</td>
<td>176.61mv</td>
<td>4.71ns</td>
</tr>
<tr>
<td>6</td>
<td>180λ</td>
<td>180.19mv</td>
<td>4.69ns</td>
</tr>
</tbody>
</table>

2. Reducing R

Assume the on-chip parasitic resistance (R1) is reduced to 56 ohms. The ground bounce waveform is shown in Fig. 6.15. As we can see from this figure, the local ground bounce decreases sharply followed by a bunch of bouncing caused by inductances, and the circuit settles down within 2ns which is quite fast. So decreasing the parasitic resistance is an applicable method to reduce the wake up time. However, the most efficient way to reduce
resistance is to widen the wire, which will greatly enlarge the circuit area and thus become unrealistic in most situations.

3. Adding control transistors between local ground and base.

Since discharging the local ground voltage back to zero takes long time, reducing decrease time becomes the most efficient way to reduce the wake up time. In the decrease phase, the control transistor does not provide enough discharge current, since there is no voltage difference between the source and drain. The circuit will discharge the large capacitance $C_L$ slowly. If the local ground and base are connected by a extra transistor, then the...
local ground voltage will be pulled down sharply by the base. By taking an inverter circuit as an example, the circuit diagram is shown in Fig. 6.16. V1 and V2 and V3 are switched on (or off) in sequence. When V1 is switched off, the circuit base is separated from the bias voltage source; when V2 is switched on, the circuit base is pulled up by the global ground; when V3 is switched on, the local ground voltage is pulled down by the base. In this way, the decrease time can be greatly reduced.

![Circuit diagram of C7552 with extra control transistor](image)

**Figure 6.16: Circuit diagram of C7552 with extra control transistor**

The timing diagram of V1, V2 and V3 are shown in the Fig. 6.17. In this experiment, V2 is switched on followed by V3 after 0.01ns. The rising time of V2 and V3 are both 0.01ns. All of the control transistor widths are assigned 30 $\lambda$, and the bias voltage is set to -0.8v in two simulations. The simulation waveform of c7552 is shown in Fig. 6.18, while (a) is the waveforms without the extra control transistor connecting the base and gnd1 while (b) is the waveforms of adding an extra control transistor. It is obvious that the local ground in (b) has a much faster drop compared to (a). The simulation result is shown in Table 6.3. The wake up time is reduced by 50%. Adding an extra voltage source is thus a good method to reduce the wake up time for large benchmark circuits.
Figure 6.17: Timing diagram of v1v2v3

Figure 6.18: Simulation results of c7552 with an extra control transistor

Table 6.3: Simulation results

<table>
<thead>
<tr>
<th></th>
<th>Ground bounce magnitude</th>
<th>Wake up time</th>
</tr>
</thead>
<tbody>
<tr>
<td>without extra transistor</td>
<td>115.87mv</td>
<td>5.03ns</td>
</tr>
<tr>
<td>with extra transistor</td>
<td>117.16mv</td>
<td>2.61ns</td>
</tr>
</tbody>
</table>
Chapter 7

Conclusions and future work

7.1 Thesis Conclusions

This thesis presents a RBB model which can predict circuit behaviors during mode transition (from sleep mode to normal mode) under the RBB technique. The model is composed of three parts: the benchmark circuit, the control transistor, and the parasitic RLC circuit which includes both on-chip and package parasitics. This thesis gives a novel model of the parasitic RLC circuit which is more accurate than the traditional lumped model. The benchmark circuit can be represented by three equivalent capacitances. The control transistor is modeled as four capacitances and a current source. The circuit model can be applied with the bias voltage ranging from -0.2v to -0.8v, and the control transistor width ranging from 30λ to 200λ. The simulation waveforms of the local ground and base voltages for ISCAS85 benchmark circuits show high similarity between the Matlab and Hspice results. The simulation results including the ground bounce magnitude and settle down time show high accuracy, which is with 20% error range compared with Hspice.

The ground bounce of RBB is negative when the base of a benchmark circuit is connected to the local ground (gnd1). This thesis also shows the situation where the base is connected to the global ground, which causes positive ground bounce. It is not very applicable in real circuit design since for the latter case we usually connected the base to the local ground. But this gives us in-depth understanding of the RBB technique, and shows
that the circuit behavior can be totally different due to a small change. A small negative ground bounce will not affect the circuit performance and the circuit robustness. In fact, it can improve the circuit performance since the voltage difference between Vdd and Gnd is even larger. Also it causes larger noise margin. But it has negative effect in dynamic power consumption due to the larger voltage difference of Vdd and Gnd. As we know, there are four metrics for digital circuit design, which include area, robustness, power and performance. The RBB technique connecting the circuit to the appropriate voltage source during mode transition shows improvement in two of them: robustness and performance. Since the maximum negative ground bounce in this thesis is around -60mv, which will not cause punch through of a MOSFET transistor, the RBB technique is thus quite safe.

PG causes a large positive ground bounce which will dramatically reduce the circuit performance and robustness. A model for PG is developed and the circuit responses under the PG technique is also studied to be compared with those of RBB. As stated in Chapter 5, RBB causes only a quarter of the ground bounce magnitude of PG under the same control transistor width. PG is more effective in leakage reduction, however it consumes more power during mode transition and takes longer time to wake up [15].

This thesis also analyzes the factors which contribute to the long settle down time during mode transition. For a large benchmark circuit such as c7552, which has large settle down time and has relatively no inductive ground bounce due to the large capacitive load, a concise circuit model (similar to a RC ladder) which contains only capacitances and resistances helps us to fully understand the circuit behavior. This model shows that we can reduce the circuit settle down time by reducing the resistance, capacitance or adding additional intermediate voltage source to speed up the capacitance charging, and in turn reduce the settle down time.

### 7.2 Future work

The RBB model presented in this thesis shows high accuracy. However, the calculation of three equivalent capacitances of some circuits such as c499 still can be further improved. According to the simulation result, the largest error occurs in the case of benchmark cir-
circuit c499, which includes many XOR gates. Since an XOR gate contains floating internal points, it is hard to calculate the equivalent capacitances. There should be a better implementation method to deal with gates with many floating points. An alternative way to get the three capacitances is to charge the whole circuit and get the capacitance values.

By using this model, we can predict the circuit behavior in a short time. So we can use it to adjust the bias voltage as well as the wake up strategy. For example, we can determine the bias voltage according to the trade-off between leakage reduction and settle down time during waking up. There is also trade-off between the power consumption during mode transition and the leakage power reduction. To develop a solid system to determine the appropriate circuit bias voltage for different applications is critical for future circuit design. Also we can determine whether a certain circuit should use PG or RBB based on their advantages and disadvantages.

The RBB technique with base connected to the local ground does not need to be optimized, since it generates a small negative ground bounce. The PG model can be used to optimize the wake up strategy of PG circuits. Commonly used PG optimization strategies such as circuit partition and gradually waking up can be tested using the PG model in this thesis, but the control transistor model needs to be changed according to different strategies.
Bibliography


Appendices
.1 Input vectors for ISCAS85 benchmark circuits

c432:
0 1 0 1 1 0 0 0 0 0 0 1 1 1 1 0 1 1 0 0 1 1 1 1 0 0 1 0 1 0 0 1 1 1 0

c499:
0 1 1 0 1 1 1 1 1 0 1 1 1 1 1 1 1 0 1 1 0 1 1 0 0 0 0 0 0 1 0 1 0 1 1 1 0 0 0 0 1 1

c880:
0 0 0 0 1 0 0 0 1 1 0 1 0 0 1 0 1 1 0 1 1 1 0 0 1 0 0 1 1 0 0 1 1 0 0 1 1 1 0 0
0 0 1 0 0 1 0 1 1 1 0 0 0 1

c1355:
0 0 0 0 1 1 1 0 1 1 0 0 0 0 0 0 0 1 0 0 1 1 1 1 1 0 1 1 1 0 0 1 0 0 1 0 1 1 1 0

c1908:
0 0 0 1 0 0 1 1 1 1 1 0 1 1 1 1 1 1 0 0 0 0 1 0 1 1 1

c2670:
0 1 1 1 0 0 1 1 0 1 1 0 0 1 0 1 0 0 1 1 1 1 1 0 1 0 1 0 0 0 0 1 0 1 0 1 1 1 1 1 1 1 0 0
1 1 1 1 0 1 0 0 0 1 1 1 0 1 1 1 1 0 1 1 1 0 0 1 0 0 1 0 1 1 1 1 1 1 1 1 0 0 1 0 1 1 1 1 1 0
1 1 1 0 0 1 0 1 0 1 1 1 0 0 1 0 0 0 0 0 0 1 1 0 1 1 0 0 0 1 0 1 1 0 1 1 1 1 1 0 0 1 0 0 0 0 0
0 1 0 1 1 0 0 0 1 1 0 1 0 0 0 0 1 0 1 0 1 1 1 1 0 1 1 0 1 1 0 1 1 0 0 0 0 0 1 1 1 1 0 0 0 1 0 0 1
1 0 1 0 0 1 0 0 1 0 0 1 0 1 1 1 1 0 0 0 1 1 0 1 0 1 1 1 1 1 0 1 0 0 0 1 1 1 1 1 1 0 1 1 0 1 0 1
1 0 1 1 0 0 0 0 1 0 1 1 1 1 1 0 0 0 1 0 1 1 1 1 0 0 1 1 1 0 1 1 1 0 1 1 1 0 1 1 0 0 0 1 1 0 0 1 1
0 0 1 1 0 0 1 0 1 0 1 1 1 1 1 0 0 0 0 1 0 1 1 1 1 1 0 1 0 1 1 1 1 0 1 1 0 1 0 1 1 0 0 0 0 0 1
0 1 1 0

c3540:
0 0 1 1 0 1 1 0 0 1 0 1 0 0 1 0 1 0 1 0 1 1 0 0 1 0 0 1 0 1 0 1 1 0 1 0 0 0 0 1
0 1 1 0

c5315:
0 1 1 0 1 1 0 0 1 1 0 0 0 0 0 0 1 0 0 0 0 0 1 1 1 1 1 1 0 1 0 0 1 0 1 0 1 1 0 1 1 0 1 1 0 1 1 0 0 1
0 1 0 1 0 1 1 1 0 0 0 1 0 0 1 0 0 0 0 1 0 1 1 1 1 0 1 1 1 1 0 1 1 0 0 0 0 1 0 1 1 1 0 1 1 1
c6288:
010001101101001100101100000010001

c7552:
01111101101100110011110001001001011110000001
11110010111011001100010001110101010111000100100
1011001100011111101100011001010000001101011110
010111000100111011001101000101101100011101000010
10100111000010