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ABSTRACT

As device dimensions continue to shrink into the nanometer length regime, conventional complementary metal-oxide semiconductor (CMOS) technology will approach its fundamental physical limits. Further miniaturization based on conventional scaling appears neither technically nor economically feasible. New strategies, including the use of novel materials and one-dimensional device concepts, innovative device architectures, and smart integration schemes need to be explored. They are crucial to extending current capabilities and maintaining momentum beyond the end of the technology roadmap. Semiconducting nanowires are an attractive and viable option for channel structures. By virtue of their potential one-dimensionality, such nanoscale structures introduce quantum confinement effects, thus enabling new functionalities and device concepts. In this thesis we study performance limits of Indium Arsenide nanowire Field Effect Transistors (InAs NWFETs) in a Gate All Around (GAA) structure and examine its upper limits of performance. InAs in particular is an attractive candidate for NW-based electronic devices because of its very high electron mobility at room temperature of 30,000 cm²/Vs in comparison to silicon’s mobility of 1480 cm²/Vs.

The device simulations were carried out using MultiGate Nanowire (Nanowire MG) simulator made available at NanoHUB (www.nanohub.org) by Network for Computational Nanotechnology (NCN). The InAs NWFET was simulated for variations in channel diameter, channel length, oxide thickness and the corresponding I_d – V_g characteristics were analyzed. Short Channel Effects (SCEs) namely Drain Induced Barrier Lowering (DIBL) and threshold voltage roll off were studied. Sub-threshold slope and ON/OFF current variations were analyzed for variations in device dimensions. Finally the device characteristics of Silicon Nanowire Field
Effect Transistors (Si NWFETs) were simulated for the same variations in channel diameter, channel length and oxide thickness and a comparative study of the device performance between InAs NWFET and Si NWFET was carried out to assess the effect of varying the channel material system. It was concluded that Silicon NWFET showed higher immunity towards threshold voltage roll off with scaling in channel length and exhibited better sub-threshold slopes for the same device structure in comparison to the InAs NWFET. Also it was observed that Silicon NWFET operated with lower leakage currents compared to InAs NWFET. Overall it was concluded that SiNWFET exhibited higher immunity towards short channel effects while InAs NWFET showed higher drive currents in the order of $0.10 \times 10^{-3}$ A/μm compared to $8.4 \times 10^{-6}$ A/μm which would translate to higher switching speeds.
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Chapter 1

1. Introduction

As device dimensions continue to shrink into the nanometer length regime, conventional complementary metal-oxide semiconductor (CMOS) technology will approach its fundamental physical limits. Further miniaturization based on conventional scaling appears neither technically nor economically feasible. New strategies, including the use of novel materials and one-dimensional device concepts, innovative device architectures, and smart integration schemes need to be explored. They are crucial to extending current capabilities and maintaining momentum beyond the end of the technology roadmap.

Nanowires, measuring typically 2 to 100 nm in diameter, can have significantly different electrical properties compared with those for the bulk materials. By virtue of their potential one-dimensionality, such nanoscale structures introduce quantum confinement effects, thus enabling new functionalities and device concepts. The subject of this thesis is the study of InAs nanowire MOSFETs (NWFET) and an examination of its upper limit performance levels. InAs in particular is an attractive candidate for NW-based electronic devices because of its very high electron mobility at room temperature of 30,000 cm²/Vs in comparison to silicon’s mobility of 1480 cm²/Vs [1]. In addition, its surface Fermi level pinning in the conduction band [2] leads to the formation of an electron surface accumulation layer [3] and allows straightforward formation of low-resistance ohmic contacts [4]. In recent years new technologies have been developed to fabricate excellent quality InAs nanowires. A very high degree of control and homogeneity in terms of the nanowire’s diameter, length, and the crystal quality has been made possible by the Vapor-Liquid-Solid (VLS) mechanism and Selective Area-Metal Organic Vapor Phase Epitaxy (SA-MOVPE) methods [5]. Using these InAs nanowires, scientists have recently succeeded in fabricating nanowire MOSFETs which have demonstrated promising performance for high gain and high frequency operation [6]. Currently prototype devices are being tested to investigate their potential as an
eventual replacement for Si MOSFETs. To better understand the relevance of this study and its simulation results, we begin by looking back at the evolution of Si MOSFETs and the limitations that now hinder their further development.

1.1 Moore’s Law and Silicon MOSFET downscaling

Historically, for more than four decades, the electronics industry has thrived on steadily reducing the size of the Silicon MOSFET. The reasons for this is that, not only does it increase the transistor speed and transconductance (gain), but it also helps pack in more functionality into a single chip thereby decreasing the cost per function. This trend has been quantified and is popularly known as Moore’s Law (See Fig 1.1). Gordon E. Moore observed in 1965 that “The complexity for minimum component costs has increased at a rate of roughly a factor of two per year. Certainly over the short term this rate can be expected to continue, if not to increase. Over the longer term, the rate of increase is a bit more uncertain, although there is no reason to believe it will not remain constant for at least 10 years” [7]. This observation has since continued to be true for decades and in fact the Moore’s law is used as the baseline assumption in the semiconductor industry’s strategic road map, International Technology Roadmap for Semiconductors (ITRS) [8] for the future and also has become an almost universal predictor of the entire industry’s growth

Figure 1.1 Timeline of transistor count per die with each line of processor [6]
1.2 Silicon MOSFET Evolution and Short Channel Effects

MOSFET’s have come a long way from the time they were first theoretically conceptualized in Dr. Lilienfelds patent application of 1928 to the first operating transistor in 1947 at the Bell Laboratories by William Shockley and his group [9]. Dawon Khang at Bell Labs later on successfully overcame the surface states problem [10] that troubled other researchers and fabricated the first operational planar MOSFET in 1960. Since then, there has been a flood of research in developing better and more efficient Field Effect Transistors (FET) for an increasing variety of applications. An integral part of the MOSFET’s evolution has been a steady reduction in its size. Researchers are continuously working on finding ways to further scale down the transistor size by overcoming the problems associated in doing so. Initially, scaling was not as difficult as it is now because the limitations were in the fabrication technology. But as the device size entered the micrometer and sub-micrometer regime for the gate length, scaling has become increasingly more complicated due Short Channel Effects (SCE) that degrade the Electrostatic Integrity (EI) of the device. In the next section we briefly describe these effects since they will be used in our subsequent description and analysis of the performance of the InAs NWFT.

1.2.1 Short Channel Effects (SCEs) in Silicon MOSFETs

Short channel effects (SCEs) are phenomena associated with the degradation in MOSFET device performance that arises as the device is scaled down in size. These SCEs include the effects of scaling on the threshold voltage, transconductance and subthreshold current of the MOSFET [11]. SCEs arise when control of the channel region by the gate is degraded by the electric field lines from the source to drain. As the channel length is scaled down, the distance between the source and drain depletion regions is reduced. As a result, they begin to influence the electric potential in the channel region. This reduces the net effective charge controlled by the gate and so results in a lowering of the threshold voltage as shown in Fig.1.2. Hence, one of the SCEs is that the threshold voltage decreases as the channel length decreases, whereas it is independent of the channel length for a long channel MOSFET. Fig 1.2(a) shows the subthreshold characteristics for MOSFETs of 2.0μm, 0.35μm, and 0.2μm [12] if the threshold voltage is
defined as the gate voltage needed for a specific current level, e.g. $10^6$ A/µm, then it can be seen from the figure that the threshold voltage becomes smaller as the gate length is reduced. Fig. 1.2(b) shows the extent of this roll off in threshold voltage for different transistor structures each with a different source/drain doping gradient [13].

![Figure 1.2](image)

(a) Subthreshold characteristics of long and short channel devices at low and high drain biases [12] (b) Short channel threshold voltage roll off with three different lateral Source-drain doping gradients. Each point on the curve corresponds to metallurgical lengths ($L_{met}$) of 0.05, 0.07, 0.10, 0.15, 0.25 and 0.50 µm respectively [13].

Another SCE is the effect the drain voltage has on the subthreshold current. At gate voltages below the threshold voltage, an increase in the drain voltage effectively reduces the energy barrier height at the source end of the channel allowing electrons to flow from source to drain. This increased subthreshold conduction of electrons due to an increase in the drain voltage influence further reduces the threshold voltage of the device as seen in Fig. 1.3 by ~ 50mV and is what is called Drain Induced Barrier Lowering (DIBL). In summary, the device achieves a particular drain current value ($10^{10}$ A) at a smaller gate voltage thereby corresponding to a lowering of the threshold voltage. This is usually expressed in terms of mV of threshold voltage shift per volt of drain voltage increase.
Figure 1.3 Threshold Voltage lowering as a result of variation in the drain bias (DIBL) [14]

As the channel length is reduced, the effects of DIBL in the subthreshold region (weak inversion) show up initially as a simple translation of the subthreshold current vs. gate bias curve with a change in drain-voltage as seen in Fig.1.3. However, at shorter lengths the slope of the drain current vs. gate bias curve is reduced (as shown in Fig.1.2(a)), that is, a larger change in gate bias is needed to effect the same change in drain current. At extremely short channel lengths, the gate can almost entirely fail to turn the device off. To counter these effects and ensure the gate voltage retains the dominant role in controlling charge carrier flow in the channel, doping concentrations can be increased in the channel to reduce the width of the depletion region associated with the source drain p-n junctions formed with the substrates. The reason for reducing this depletion depth is because the field lines from source to drain propagate through these depletion regions to end up in the channel and interfere with the gate’s control over the channel. But this increase in channel doping unfortunately also leads to a change in threshold voltage, a degradation of the carrier mobility due to increased impurity scattering, which degrades the transistor transconductance, and also causes junction edge leakage due to tunneling [15]. For modern devices with channel lengths currently in the nanometer regime at 50nm, the doping factor puts additional pressure on the fabrication process technologies because controlling the doping profile in terms of depth and steepness within the channel now becomes much more difficult. Additionally the gate dielectric thickness needs to be scaled down to ensure good gate field control. Since the gate oxide is already down to a few
atomic layers, further scaling not only puts increased process strain but also results in gate leakage above acceptable levels.

As seen in Fig.1.2(a), at shorter channel lengths there is a clear degradation of the sub-threshold characteristics. This slope of the plot of the drain current versus the gate voltage is quantified using the sub-threshold slope ‘S’, which is defined as the change in gate voltage in mV required to change the drain current by an order of magnitude. As a result S has units of mV/dec and is typically of the order 100 mv/dec where 60 mV/dec is the theoretical lower limit. A smaller value of S is desired since it corresponds to a steeper $I_d$-$V_g$ plot and enables a smaller off current for a given gate voltage swing, e.g. 1V, between the on and off states of the transistor. One approach to improving ‘S’ and minimizing SCEs is to employ a high-K gate dielectric which will provide better electrostatic control of the channel at a thicker gate dimension and also reduce the gate tunneling leakage current which is a significant portion of the overall leakage current in the device.

Another approach to contain the SCE and ensure better gate control over the channel has been achieved by the use of additional gates on other sides of the channel, such as a second gate which is directly below the top gate. This helps in cutting down the subthreshold leakage current effectively because there are now two gates that control the same channel region resulting in better electrostatic integrity and smaller SCEs. This avoids the problems of increased channel doping and lessens the need for down scaling of gate dielectric thickness that were described above to retain the gate control over the channel. Although this double gate device structure functionally is efficient, in practice it is difficult to fabricate due to process integration issues [16]. More recently, MOSFETs with the gate on three or four sides of the channel have also been explored and shown promising results [17][18], though fabrication process issues remain. For the Nanowire MOSFETs considered here, they correspond to a Wrap Around Gate (WAG) that ensures excellent gate control of charge throughout the channel, i.e. suppression of short channel effects. Recently, Nanowire silicon MOSFETs have been fabricated and have shown excellent charge mobility and very low off state currents [17], which will be discussed in the following section.
1.3 Nanowire MOSFETs

Nanowire silicon FETs have the inherent advantage of being extremely small in device dimensions and have shown to possess excellent immunity towards Short Channel Effects [17]. The Silicon Nanowire FETs (SNWFETs) have been fabricated (see Fig 1.5) with good reproducibility and excellent device characteristics that quite comfortably outperform the planar Silicon On Insulator (SOI) MOSFET. Shown in Fig 1.5 is an example of a SNWFET and its performance characteristics.

![Figure 1.5](image)

Figure 1.5 a) Shows an SEM image of the SNWT fabricated with a channel diameter of 10nm and gate length 30nm, b) SNWT Id-Vg characteristics showing the subthreshold slope and DIBL and c) Output transistor characteristics [18]

For a SNWFET with a channel diameter of 15nm and a gate length 50 nm and a gate oxide thickness of 1.5nm, it has been demonstrated by the Lieber group at Harvard that the average transconductance in SNWFET is up to ten times larger at 2700-7500 µS/µm when compared to 650µS/µm for the planar SOI FET with the same gate length [17]. The SNWFET also showed a very impressive $I_{on}$ / $I_{off}$ ratio of 5600µA/45nA, i.e. an $I_{on}$ that’s nearly 12 million times the $I_{off}$ current. By comparison, the planar SOI FET had an $I_{on}$ / $I_{off}$ ratio of 650µA/ 9nA, which
corresponds to an $I_{on}$ that’s 70000 times its $I_{off}$ [17]. Clearly, it can be seen that the SNWFET shows a better current drive capability with superior transconductance curves and on/off characteristics.

Research is also currently underway in developing NW FETs with different semiconducting materials to utilize the advantages, e.g. higher mobility, that are specific to other semiconductors. Silicon has always been the work horse of the semiconductor industry and so Si NWFETs were the first to be fabricated and tested, but newer and better materials are attracting increasing interest within the semiconductor world with the advent of new nanowire fabrication techniques. For example, Ge, GaAs, GaN, InAs and ZnO are some of the materials being explored for future use in NWFETs. Ge nanowires have the intrinsic advantage of superior electron and hole mobilities of 3900 cm$^2$ V$^{-1}$ S$^{-1}$ and 1900 cm$^2$ V$^{-1}$ S$^{-1}$, respectively [1], resulting in faster switching speeds. GaAs on the other hand would be an excellent option for n-type devices considering this semiconductor has one of the highest electron mobilities of 8500 cm$^2$ V$^{-1}$ S$^{-1}$ [1]. GaN has a very high bandgap of 3.2eV, so it can be used in high power and high temperature applications, such as satellite communications and radar.

InAs is yet another very attractive material for Nanowire FETs. It has an extremely high electron mobility of the order of 40,000 cm$^2$ V$^{-1}$ S$^{-1}$ with a very small energy band gap of 0.36eV making it an ideal material for high speed, low power applications such as portable electronic devices. The research group of Q.T Do et al. [19] have successfully demonstrated some of the first n-InAs NWFETs (see Fig. 1.6) with a channel diameter of 50nm using a silicon nitride gate dielectric. The device exhibited an excellent drain saturation behavior with a maximum normalized drain current of 3 A/mm and a very high transconductance of 2 S/mm at a gate dielectric thickness of 30nm and a gate length of 2μm or less [19]. These results are higher than any reported for Silicon based Nanowire FETs with comparable gate lengths.
Figure 1.6 a) Omega shaped Gate InAs NWFET b) Output transconductance for the device versus gate voltage [19].

Figure 1.7 a) SEM image of vertical warp around InAs NWFET array with a threshold voltage of -0.15V at Vds= 0.4V and its I_d – V_ds characteristics [6].

Vertically oriented wrap around gate InAs nanowire FETs have also been demonstrated by Brylert et al., at Lund University [6] as shown in Fig.1.7 with low threshold voltages of -0.15V and a current saturation at V_ds = 0.15V for V_g = 0V [6]. With further optimization of the device structure in terms of the channel doping, the gate length, the nanowire diameter and employing High-K dielectrics with metal gates, it is possible to further enhance the device drive current and reduce the off state leakage current providing an excellent option for devices for High Performance (HP) as well as Low Operating Power (LOP) applications. Heterostructure nanowires have also been fabricated based on InP/InAs/InP by the group of Premila Mohan at Hokkaido University in Japan, which would have an inherent relaxed strain in the InAs section.
due to lattice mismatch [20]. These heterostructure nanowires shown in Fig.1.8 could further enhance the mobility of the electrons within the channel. In summary, it can be seen that nanowire MOSFETs are proving to be a promising candidate for furthering Moore’s law and InAs, in particular, is an attractive and viable material for high speed, low power applications.

Figure 1.8. Schematic illustration of a core-multishell InP/InAs/InP nanowire

1.4 Purpose of the Thesis

In this thesis we investigate using state of the art computer modeling to examine the performance potential and limitations of the InAs Nanowire MOSFETs. The purpose of this thesis is to use device simulations to examine the upper limit to device performance of a Gate All Around (GAA) InAs Nanowire MOSFET and compare it with the limited available experimentally published results. The tools used to simulate our device are the Multigate Nanowire and FETtoy software programs that were developed and made available by the NanoHub at Purdue University [21]. The aim is to simulate the devices for different physical parameters, such as varying gate lengths, channel doping, channel diameter, gate dielectric thickness, and examine their effects on the device performance. The results are expected to be useful in optimizing the transistor’s design and for comparison to future experimental results. In addition, the extent of short channel effects in the InAs MOSFET will be investigated. The threshold voltage, subthreshold characteristics, DIBL and other key parameters will be obtained from the simulations. Finally, an optimization of the device is planned to obtain the best possible
performance in terms of drive current, transconductance, subthreshold slope and minimum off state leakage current, i.e. minimum short channel effects.

1.5 Organization of the Thesis

This thesis is organized into five chapters. Chapter 1 has discussed the long term trend of down scaling conventional silicon MOSFETs and the various approaches being taken to curtail the SCEs and retain the electrostatic integrity of the device. The concept of the nanowire FETs has been introduced using silicon NWFETs with their performance results being briefly discussed and the promise of InAs nanowire MOSFETs for the future has been introduced. Chapter 2 will deal with the material properties of InAs and its advantages over other semiconductors including silicon. Growth techniques for InAs nanowires will also be discussed followed by an overview of the software tools used for simulating the device. Chapter 3 describes the results of experimental work on the development of InAs nanowire MOSFETs reported in the literature and the results of our initial modeling of the InAs NWFET performed in this study for a particular device structure. Chapter 4 analyzes the effects on device performance for varying the device structure, e.g. nanowire diameter, and presents the understanding of the physics behind the variation in its performance followed by a comparative study between the device performances of InAs Nanowire FET and Si Nanowire FET. Chapter 5 provides the conclusion and some suggestions for future work.
References


[14] [http://www.iue.tuwien.ac.at/phd/stockinger/node15.html](http://www.iue.tuwien.ac.at/phd/stockinger/node15.html)


[21] Nanohub, Purdue University, www.nanohub.org
Chapter 2

2. InAs Nanowire as channel material and growth techniques

2.1 Properties of Indium Arsenide

Many III-V materials such as GaAs, InP and GaN have been and will continue to be researched for exploring the possibilities of extracting the maximum benefits out of these materials for electronic devices, transistors particularly. Yet another III-V semiconductor that is attracting quite a bit of attention is Indium arsenide (InAs). InAs has excellent material properties from an electrical point of view. Since the carrier effective mass is strongly correlated with the carrier mobility, it is known to be one of the most important device parameters.

Every electron has a constant free electron mass of $9.1 \times 10^{-31}$ Kg. But when an electron travels within a medium (InAs in this case), its mass is no longer considered as a constant. Rather it varies based on the material it propagates in and is called the electron effective mass. InAs being a direct band gap material, has an electron effective mass ($m_c^\Gamma / m_0$) of 0.024 in the $\Gamma$ valley of the conduction band. This is very low compared to silicon’s longitudinal electron effective mass ($m_l^\Gamma / m_0$) of 0.98 and a transverse effective mass ($m_t^\Gamma / m_0$) of 0.19 in the X valley of the conduction band [1]. The lighter the electron’s mass, the faster it can travel ‘$v$’ in an electric field ‘$E$’ and hence higher the mobility ‘$\mu$’ that can be achieved as given by the expression [2]

$$v = \mu . E \quad \text{Where,} \quad \mu = \frac{q \tau}{m^*} \quad (2.1)$$

where $\tau$ is the electron’s time between collision and $m^*$ is the electron effective mass.
It is for this reason that InAs has one of the highest low-field electron mobilities in the order of $3 \times 10^4 \text{ cm}^2/\text{Vs}$ in comparison to electron mobilities of $9.34 \times 10^3 \text{ cm}^2/\text{Vs}$, $6.46 \times 10^3 \text{ cm}^2/\text{Vs}$ and $1254 \text{ cm}^2/\text{Vs}$ for GaAs, InP and GaN, respectively [1]. This mobility is roughly a factor of three larger than what GaAs has. This directly translates to the possibility of having FETs with InAs as their transport channel that operates at three times the switching speeds of the current GaAs based FETs. The reason electron mobilities in semiconductors is stressed a lot is because it directly translates to the speeds at which a device can operate at particular supply voltage.

The transconductance ‘$g_m$’ of a MOSFET is directly proportional to its mobility $\mu$, and is given by the expression [3]

$$g_m = \frac{\mu C V_{ds}}{L} \quad (2.2)$$

where $V_{ds}$ is the applied drain to source voltage, $C$ is the total gate capacitance and $L$ is the effective channel length. A device channel with high mobility will yield high transconductance ensuring high output drive current for a given input voltage. The transit time ‘$\tau_t$’ for electrons from the source to the drain is given by

$$\tau_t \propto \frac{L}{v} \quad (2.3)$$

where $v$ is the electron velocity given by $v = \mu E$

As it can be seen from equation (2.3), a large mobility ‘$\mu$’ results in a smaller transit time for the electrons in the channel from the source to the drain and so a faster device.
InAs has a very narrow band gap of 0.36eV relative to other semiconductors as shown in Fig. 2.1 [1]. The result of this very narrow bandgap is that we don’t need a relatively large energy to excite charge carriers from the valence band into the conduction band. As a result of this, we can avalanche breakdown in the material at very low voltages. This requires that we operate at very low voltage and power, which serves as an attractive feature for their use in portable devices where battery time is a critical measure of performance. Fortunately, the high mobility of electrons in InAs enables high speed device operation at low voltages. So InAs FETs are more useful for low power, high speed operations and not high power, high speed operations.

Figure 2.1 Bandgap energy versus lattice constant for various III-V semiconductors at 300K [4]

Figure 2.2 Energy band diagram of InAs [5]
Fig. 2.2 shows the Energy (E) - Wave vector (K) diagram for InAs. As it can be seen from the diagram, the lower most conduction band valley in InAs is the Γ valley. Since electrons have the inherent tendancy to fill up the bottom most energy bands, the energy bands in the Γ valley get filled with electrons. With the application of an electric field these electrons begin to flow with a drift velocity (which is dependent on the strength of the applied field and the material of propagation) that constitute the current. So conduction will predominantly occur in the Γ valley region of the conduction band at lower voltages of operation. But as the voltage is increased, above a particular limit, the electrons acquire sufficient energy to jump into higher valleys, namely the L and the X valleys. But the density of these electrons contributing towards current conduction in these higher valleys is relatively small when compared to the electron density in the Γ valley. It is for this reason that we consider conduction only in the Γ valley for our simulation study.

Another advantage with InAs is that it has a higher overshoot velocity when compared to GaAs. With device dimensions being scaled down more aggressively when compared to their supply voltages, the fields within the device keep getting larger. This results in devices reaching their saturation currents very quickly reducing their current gain. Devices with high saturation currents are preferred for the reasons of higher current gain and transconductance. Overshoot velocity occurs when the average velocity of carriers in semiconductor exceeds saturation velocity which is possible during ballistic transport. So as the devices are scaled further and further approaching the ballistic regime, there will eventually come a time when overshoot velocity gains significance in the device performance. InAs also has a very high saturation velocity of $0.9 \times 10^7$ cm/s for an electric field of kV/cm in the Γ valley compared to $0.72 \times 10^7$ cm/sec for GaAs [6]. The advantage of having high saturation velocity is that a higher current gain and transconductance can be achieved. Higher gain-bandwidth product $f_T$ can be achieved due to higher current gains thereby increasing the upper limit to the FET operation [7].
Figure 2.3 Velocity-Field relationship for electrons and holes in InAs at 300K [8].

Fig. 2.3 shows the electron drift velocity versus electric field in InAs obtained from the work of Y.Hori et al. in NEC Corporation. In their work, a mobility of 17800 cm$^2$/v.s was obtained for InAs at 300K and peak drift velocities of $3.65 \times 10^7$ cm/sec was observed.

All these above mentioned advantages make InAs quite an attractive material system for pursuing device modeling to study the upper limits of MOSFET device performance. One additional fact worth mentioning is that, although InAs is a very attractive material for N-type devices, it is not so for the p-type devices. The reason for this being that the hole mobilities in InAs is nearly the same as that for silicon at 450 cm$^2$/V-sec [1]. So p-channel InAs FETs will be no better or faster than silicon p-channel MOSFETs. Germanium on the other hand is a better material for p-type devices since it has a hole mobility in the order of 2400 cm$^2$/V-sec [1].

In summary, for this InAs nanowire FET modeling study the key InAs material parameters used in the simulations are given in table 2.2.
Table 2.1 InAs material parameters used in nanowire FET modelling [1].

<table>
<thead>
<tr>
<th>Properties</th>
<th>Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Energy Band gap</td>
<td>0.36 eV</td>
</tr>
<tr>
<td>Low field electron mobility</td>
<td>$3 \times 10^4$ cm$^2$/V-s</td>
</tr>
<tr>
<td>Electron effective mass in $\Gamma$ Valley</td>
<td>0.024</td>
</tr>
<tr>
<td>Work function</td>
<td>5.06</td>
</tr>
<tr>
<td>Static Dielectric constant ($\varepsilon_s$)</td>
<td>14.3</td>
</tr>
</tbody>
</table>

2.2 InAs Nanowire Growth Techniques

A number of fundamental issues in the growth of nanowires for their application in practical and integrated devices are the control of their growth and reproducibility in their position, composition, size and shape, because they determine their electrical properties and their feasibility of their high density integration. Over the years a number of methods have been developed to selectively grow uniform InAs nanowires. Nanowire growth in general is achieved by the Vapor-Liquid-Solid (VLS) mechanism [9]. Different growth methods based on this underlying mechanism are the Metal Organic Vapor Phase Epitaxy (MOVPE) [9] and laser ablation [10]. They both use nanoscale metallic seeds such as gold as catalysts to form an initial eutectic alloy with the growth elements at an elevated growth temperature from which the nanowire subsequently grows.
2.2.1 Vapor-Liquid-Solid Mechanism

In the VLS mechanism the growth material for the nanowire formation is fed from the vapor phase with gas molecules absorbed into the molten liquid metallic seed formed at a high temperature. Once the eutectic liquid alloy seed gets supersaturated with the growth material, further influx of the growth material results in crystallization of the semiconductor from the seed forming the nanowire which represents the solid phase of the VLS mechanism [9]. Supersaturation and continued vertical growth of the seed is maintained by the continued flow of the gaseous source material and its absorption into the eutectic alloy. Metallic seed particles, e.g. gold, are typically used and dispersed using an aerosol technology over a substrate. As shown in Fig.2.4(a), The aerosol technology allows diameter selection of the catalytic gold particles by virtue of their size, which is inversely proportional to their mobilities in an electric field [9]. So selectively tuning out certain sizes with an appropriate electric field helps to select gold particles with the required diameters. Since the size of these gold particles determine the diameter of the nanowire, this provides a reasonable amount of control over diameter selection for the nanowires.

Figure 2.4 a) Schematic setup for Gold assisted VLS growth of NWs [11] b) SEM image of 20nm diameter InAs NW, Where the inset shows the Gold cap on the Nanowire from the gold catalyst used [12].
Another method employing laser ablation and vapor-liquid-solid (VLS) growth has been developed for the synthesis of semiconductor nanowires [10]. In this process, laser ablation was used to prepare nanometer-diameter metallic catalyst particles that define the size of the nanowires subsequently produced by VLS growth. This approach has been used to prepare bulk quantities of uniform single-crystal semiconductor nanowires as shown in Fig. 2.5 for silicon nanowires [13].

![Figure 2.5 SEM image of Silicon nanowire array with a uniform lengths of 750nm [12]](image)

However, there is a considerable interest in the electronics industry to integrate high-performance nanomaterials with Si using methods compatible with existing Si processing technology. Gold, however, is not a material that is well accepted within the silicon processing industry because it poisons Silicon since gold atoms act as impurities trapping electrons and holes in deep-level recombination centers [13]. So NWs grown using catalytic gold seeds in a V-L-S mechanism invariably contain trace amounts of gold in them or end up on process equipments which could potentially damage a silicon integrated system and so these silicon nanowires are not compatible with the CMOS processing. For InAs nanowires, this may also be a concern. NW growth without foreign metal catalyst particles would offer an attractive alternative to the VLS method. Selective-area MOVPE is one such growth technique.


2.2.2 Selective-Area Metal Organic Vapor Phase Epitaxy (SA-MOVPE)

This technique serves two advantages. Not only does it eliminate the use of catalysts but it also provides control of the positions of the nanowires on a substrate which is otherwise hard to achieve. In SA-MOVPE, amorphous films are used to partially mask the substrates and the crystal grows epitaxially only in the mask openings (holes) formed with lithographic and etching technique [14].

Figure 2.6 (a) Experimental procedure for growth of InAs nanowire array using SA-MOVPE with 100nm mask openings [14]. (b) SEM image of InAs NWs grown at 540°C having 100nm diameter and 1.5µm length, where the Inset shows the top view of the nanowire [14].

The periodic openings in the masking material are made by electron beam lithography and wet chemical etching based on buffered hydrofluoric acid for SiO₂. The growth of the nanowires are carried out using horizontal MOVPE system [14]. The results are shown in Fig. 2.7. It was observed that the nanowires grow with diameters equal to the mask openingS as long as the
growth temperature was maintained within a range of 540-560°C. At temperatures below 540°C the nanowire showed later growth and thickening while nanowire growth was suppressed at a temperature of 600°C [14]. The grown InAs nanowires had a diameter of 100nm and about 1.5µm in length although there were random nanowires with much lesser diameters of around 50nm and longer lengths of 5µm. It was also observed that with increased height of the nanowires the diameters reduced and the height was inversely proportional to the square of the diameter and was independent of the pressure as it can be seen in in Fig 2.7 (b). The growth rate of the nanowires increased with an increase in the pressure.

![Figure 2.7 (a)InAs nanowire diameter dependence on growth temperature and a variation of the InAs nanowires with the diameter of the mask of the openings [14].](image)

**2.3 Fabrication of InAs Nanowire FET**

A number of research groups have successfully fabricated and demonstrated working InAs NW FETs with impressive performances. The nanowire FETs that have been fabricated are
principally of two types, the first one being the Planar NW FET and the other being the vertically standing wrap around gate configuration as shown in Fig. 2.8. While the first device structure offers the advantage of less fabrication complexity, the second configuration provides superior gate electrostatic control due to gate being all around the channel. But this comes at the cost of increased process complexity and lesser mechanical stability of the device.

The group of E.T.Yu et al. at UCSD have fabricated the top gated, planar version of the InAs NWFET and have obtained very high current densities in the order of $10^6 – 10^7$ A/cm$^2$ at $V_{DS} = 0.5$V and $V_{GS} = 0$V [15]. The InAs NW used in this case had a diameter range of 30-75nm and were 20-30µm in length and were grown by Metal Organic-Chemical Vapor Deposition (MOCVD) at temperatures of 395°C. Electron-beam lithography was used to pattern the Au/Ti Source and drain electrodes and Au/SiO$_x$ top gated electrode. Al metallization and a standard lift off process were used to create ohmic contacts to the nanowires. The n-Si substrate served as a global back gate. From Fig. 2.9(a) it can be seen that the top gated InAs Nanowire FET shows low ohmic contact resistance and is highly conductive. From the linear region of the $I_d – V_{gs}$ characteristics shown in Fig. 2.9(b), the transconductance was calculated to be 3μs. From this
transconductance value, a mobility of 6580 cm²V⁻¹s⁻¹ was deduced using equation 2.2. This is by far the highest mobility achieved at room temperature in a nanowire FET.

![Graph](image1)

Figure 2.9 a) $I_{ds} - V_{ds}$ for gate voltages of -2V, 0V, and +2V and the $I_d - V_{gs}$ at $V_{ds} = 0.5V$ for the top gated nanowire FET with a gate length of 1.3 μm and nanowire diameter of 68nm [15].

The group of Tomas Bryllert at Lund University is working on the vertical Gate all around structure [16]. They have reported using Chemical-Beam-Epitaxy (CBE) with the diameter being controlled by the size of the gold particles being used, where the metal seeds were lithographically defined. In their approach they report using a novel architecture for their drain terminal. An air bridge made of Gold with a thin layer of Titanium was used to form low-resistance ohmic contact with drain and wraps around the top of the nanowire as shown in Fig 2.8(b). In the fabricated device array as seen below in Fig. 2.10, a transconductance of 6mS was obtained and a drive current of 6mA at 0 V gate voltage which translates to a current density of 50µA per nanowire [16]. A Very low leakage current of 1nA is reporte in their study.
Figure 2.10 $I_{ds} - V_{ds}$ characteristics for varying gate voltages from 0.8V to -2V in steps of 0.2V for 120 nanowire channel array \[16\].

There are few more groups that have reported impressive device characteristics with the InAs NWFET. The research group headed by Q.T.Do of University Duisburg-Essen, Germany have fabricated InAs Nanowire FETs with very high transconductance of 4800 cm$^2$ V$^{-1}$s$^{-1}$. Current density of 7.9*10$^5$ A/cm$^2$ have been reported in a single InAs nanowire resulting in transconductance of upto 895 ms/mm \[17\]. Another group, headed by Q.Hang and D.B.Janes of Purdue University have fabricated InAs NWFET having on-off ratios of 10$^4$ at room temperature\[18\].

Figure 2.11 a) $I_{ds} - V_{ds}$ characteristics for InAs NWFET with a channel diameter of 120nm and a channel length of 3.8µm reported by Q.T.Do et al. \[17\] b) $I_{ds} - V_{ds}$ characteristics for a Zinc doped InAs NWFET with channel length of 3µm and 20 nm channel diameter reported by Q.Hang and D.B. Janes \[18\].
In summary, encouraging progress is being made with the InAs NWFET and a handful of research groups around the world are very actively working on the optimization of the InAs NWFET. While InAs has definitely proved to be a worthier candidate over its other material counterparts such as Si and Ge in terms of device performance, efforts are currently on to optimize the device design and further improve the InAs NWFET performance.
References


Chapter 3

3. Multi Gate Nanowire FET Simulator Numerical Approach and Validation

3.1 Multi Gate Nanowire FET Simulator

Over the last twenty years there has been extensive work done in understanding the transport mechanism of charge carriers as the dimensions of the conducting medium (channel of the MOSFET in this case) is scaled down to a few nanometers. Conventionally, the charge transport mechanism in the channel has been governed by the drift-diffusion model wherein the electrons travel in channel lengths in the order of few micrometers. In such a case, the electrons undergo scattering a number of times in their journey from the source to the drain. But with down scaling of devices into the nanometer regime (few atomic layers), electrons get scattered only a few times or not at all because their mean free path is greater than the channel length. In the case of the electron undergoing no collision, it is said to have ballistically travelled through the channel. Under these conditions the conventional semi-classical approaches based on Boltzmann transport equation for modeling of the charge transport in the MOSFET channel model breaks down. In addition, due to complications arising from quantum mechanical effects at the mesoscopic level, the wave nature of the electrons begin to play a more significant role in its transport through the channel medium, giving rise to what is known as the quantum transport model [1]. The drift-diffusion model and Boltzmann equations do not include these quantum effects that are becoming increasingly important in the modeling of the transistor in the nanometer regime. It is for this reason that more sophisticated analysis of the device’s physics is needed, such as the Non Equilibrium Green’s Function (NEGF) approach, to model devices all the way down to the ballistic limits. The NEGF transport model is the most rigorous approach among existing quantum transport models and is the approach that is used in the software being used for our simulation study of InAs nanowire MOSFETs.
As a brief introduction to the numerical approach implemented in the NanowireMG software, in the next section we briefly describe the Effective Mass Theory (EMT) and the Non-Equilibrium Green’s Function (NEGF) formalism. The simulation consists of solutions of the three dimensional Poisson’s equation, using a product-space method to solve the two-dimensional Schrödinger equations self consistently in the nanowire cross-sectional planes and one dimensional transport equation [2].

### 3.1.1 Numerical Approach of the Simulator

The simulation software used here (NanowireMG) is based on the work done by Mincheol Shin at the Information and Communications University in the Republic of Korea [2]. The device that is simulated in this software is viewed as a three-dimensional, rectangular nanowire FET with Source/Drain, channel and multiple gates as in shown in Fig. 3.1.

![Nanowire FET model](image)

Figure 3.1 Nanowire FET model that is considered in the simulator [3]
For the quantum mechanical analysis, the effective mass 3-D Hamiltonian of the device is written as follows [2],

\[ H^{3D}(x, y, z) = \mathbf{E} \Psi(x, y, z) \]  

(3.1)

For the 3-D Hamiltonian of a device, what it means here is that when we consider quantum transport, we replace the Newtonian dynamics with quantum dynamics as described by Schrödinger equations where ‘H’ describes the quantum state of the physical system (MOSFET channel in this case) and how it varies with time. Here \( H^{3D} \) is given by,

\[
H^{3D} = -\frac{\hbar^2}{2m_x^*} \frac{\partial^2}{\partial x^2} - \frac{\hbar^2}{2} \frac{\partial}{\partial y} \left( \frac{1}{m_y^*} \frac{\partial}{\partial y} \right) - \frac{\hbar^2}{2} \frac{\partial}{\partial z} \left( \frac{1}{m_z^*} \frac{\partial}{\partial z} \right) + V(x, y, z)
\]  

(3.2)

where, \( m_x^* \), \( m_y^* \), \( m_z^* \) are the effective masses of the electrons in the x, y, z directions, respectively. \( V(x, y, z) \) is the conduction band-edge profile, given by

\[
V(x, y, z) = E_c^0(y, z) - \Phi(x, y, z)
\]  

(3.3)

where \( E_c^0(y, z) \) is half of the band gap of silicon or oxide depending upon whether the location \((y, z)\) lies in the silicon region or the oxide region and \( \Phi(x, y, z) \) is the vacuum level potential. Electron transport occurs in the x direction and \( m_x^* \) is therefore the channel effective mass while \( m_y^*(y,z) \) and \( m_z^*(y,z) \) can be either channel or oxide effective mass depending on the position of \((y,z)\). As a result the wave function penetration into the oxide region is also taken into account.
In general the wave function can be expanded as

$$\Psi(x, y, z) = \sum_{m} \varphi_m(x) \psi_m(y, z; x)$$

(3.4)

where $\psi_m(y, z; x)$ is the $m$th mode eigenfunction of the 2-D Schrödinger equation given by

$$H^{2D} \psi_m(y, z; x) = E_m(x) \psi_m(y, z; x)$$

(3.5)

where

$$H^{2D} = -\frac{\hbar^2}{2} \frac{\partial^2}{\partial y^2} \left( \frac{1}{m_y^*(y, z)} \right) \frac{\partial}{\partial y} - \frac{\hbar^2}{2} \frac{\partial^2}{\partial z^2} \left( \frac{1}{m_z^*(y, z)} \right) + V(y, z; x)$$

(3.6)

This simulation model approaches the original 3-D model by splitting it into a 2-D Schrödinger equation in the cross sectional planes of the nanowire and a 1-D Schrödinger equation along the transport direction.

The 1-D transport problem equation in the Uncoupled Modes Space (UMS) approach [2] is given by

$$\left\{ -\frac{\hbar^2}{2m_x^*} \frac{d^2}{dx^2} + E_m(x) \right\} \varphi_m(x) = E \varphi_m(x)$$

(3.7)

where the shape of the channel body is assumed to be uniform along its length (x direction) (rectangular quantum well). The conduction band-edge profile $V(x, y, z)$ has the same shape along the channel but has different values for different values of ‘x’ due to the potential drop along the channel due to source-drain bias. So the eigenfunctions $\xi(y, z; x)$ are almost the same along the channel length although the eigen values $E_{sub}^m(x)$ are different.
The 1-D transport equation (Eqn. 3.7) is solved by the Non-Equilibrium Green’s Function method in the following manner. The one dimensional Green’s function $G_m$ for a sub-band $m$ is given by

$$G_m = \left[ E - H_{m}^{1D} - \Sigma_{S,m} - \Sigma_{D,m} \right]^{-1} \tag{3.8}$$

where

$$H_{m}^{1D} = -\frac{\hbar^2}{2m^*_x} \frac{d^2}{dx^2} + E_m(x) \tag{3.9}$$

where $E_m$ are the eigen value energies for the ‘m’ sub-bands separately and $\Sigma_{S,m}$ and $\Sigma_{D,m}$ are the source and drain self energies of sub-band ‘m’ and are given by,

$$\Sigma_{S}(E) = \frac{1}{2} \left( E - 2t - E_m(1) - i\sqrt{(4t+E_m(1)-E)(E-E_m(1))} \right) \tag{3.10}$$

$$\Sigma_{D}(E) = \frac{1}{2} \left( E - 2t - E_m(N_x) - i\sqrt{(4t+E_m(N_x)-E)(E-E_m(N_x))} \right) \tag{3.11}$$

The one dimensional charge density is given by,

$$n_{m}^{1D}(x) = \frac{1}{2\pi \Delta x} \int dE \left( f_S G_m \Gamma_{S,m} G_m^\dagger + f_D G_m \Gamma_{D,m} G_m^\dagger \right) \tag{3.12}$$

where, $\Delta x$ in Eqn. (3.12) represents the 1D lattice spacing and $\Gamma_{S,m}$ and $\Gamma_{D,m}$ are defined by

$$\Gamma_{S,m} = i \left( \Sigma_{S,m} - \Sigma_{S,m}^\dagger \right) \tag{3.13}$$

$$\Gamma_{D,m} = i \left( \Sigma_{D,m} - \Sigma_{D,m}^\dagger \right) \tag{3.14}$$
The Fermi distribution functions at the source and drain ends are given by

\[
 f_{S(D)}(E) = \frac{1}{1 + e^{\frac{E - E_{F}^{S(D)}}{k_{B}T}}}
\]  

(3.15)

where \(E_{F}^{S(D)}\) are the Fermi energies at the source and drain regions, respectively.

This 1D NEGF equation (3.8) is obtained by inverting the matrix:

\[
 G_{m}^{-1}(E) = \begin{bmatrix}
 d_{1,1}(E) & t & 0 & \cdots \\
 t & d_{2,2}(E) & t & 0 \\
 \vdots & \vdots & \vdots & \vdots \\
 0 & t & d_{N_{x}-1, N_{x}-1}(E) & t \\
 \cdots & 0 & t & d_{N_{x}, N_{x}}(E)
\end{bmatrix}
\]

(3.16)

where,

\[
 d_{n,n}(E) = \begin{cases}
 E - (2t + E_{m}(1) + \Sigma_{S}(E)), & \text{if } n = 1 \\
 E - (2t + E_{m}(n)), & \text{if } n = 2, \ldots, N_{x} - 1 \\
 E - (2t + E_{m}(N_{x}) + \Sigma_{D}(E)), & \text{if } n = N_{x}
\end{cases}
\]

(3.17)

here \(N_{x}\) is the number of mesh elements in the x direction and it is defined as

\[
 t = \frac{\hbar^{2}}{2m^{*}_{x}\Delta x}
\]

(3.18)

Once the 1D charge density is calculated from Eqn. (3.12), the next step in calculation is calculating the 3D quantum charge density from equation Eqn.(3.19) using

\[
 n^{3D}(x, y, z) = \sum_{m} n_{m}^{1D}(x)|\psi_{m}(y, z, x)|^{2}
\]

(3.19)
where the summation is over the number of sub-bands that are occupied in the 2D quantum well at each value of ‘x’. This three dimensional quantum charge density is used then to calculate for the potential \( \Phi(x,y,z) \) at each point along the channel using the Poisson’s equation given by

\[
\nabla^2 \phi(x, y, z) = -\frac{q}{\epsilon} \left( N_D(x, y, z) - n^{3D}(x, y, z) \right)
\]

(3.20)

where \( N_D(x,y,z) \) in Eqn.(3.20) is the doping profile in the channel. The Poisson’s equations and Schrödinger equation are solved iteratively for electron density and self consistent potential, until a self-consistent potential and charge distribution that varies very minimally is determined at the end of the iteration. Once this condition is reached, the drain current is calculated using the Landauer-Büttiker formula

\[
I_d = \frac{2q}{h} \sum_m \int dE T_m(E)(f_S(E) - f_D(E))
\]

(3.21)

The term \( T_m(E) \) in the above equation represents the transmission probability of a particular sub-band ‘m’ at energy ‘E’ and is given by the formula

\[
T_m(E) = Tr(\Gamma \Sigma_{\omega} G_m \Gamma_{D,m} G_m^\dagger)
\]

(3.22)

The model implemented is based on the effective mass theory and so the effective masses in x, y, z directions of the charge carriers are provided externally by the user.
The rectangular cross section of the transistor’s channel perpendicular to the current flow along the ‘x’ direction is shown in Fig. 3.2

![Figure 3.2 Schematic cross sectional view of the NWFET being modeled](image)

The ‘y’ component of the effective mass \( m_y^* \) is given by

\[
    m_y^*(y, z) = \begin{cases} 
        m_y^*(y) & \text{if } z_\alpha \leq z \leq z_\beta \\
        m_{ox}^* & \text{if } z < z_\alpha \text{ or } z > z_\beta 
    \end{cases}
\]

(3.23)

where

\[
    m_y^*(y) = \begin{cases} 
        m_{si,y}^* & \text{if } y_\alpha \leq y \leq y_\beta \\
        m_{ox}^* & \text{if } y < y_\alpha \text{ or } y > y_\beta 
    \end{cases}
\]

(3.24)

and \( m_{si,y}^* \) and \( m_{ox}^* \) are the effective mass of electrons in silicon and oxide region, respectively.

As a good approximation we may write it as

\[
    m_y^*(y, z) = m_y^*(y), \text{ for } 0 \leq z \leq L_z
\]

(3.25)

Similarly, in the z direction we have

\[
    m_z^*(y, z) = m_z^*(z), \text{ for } 0 \leq y \leq L_y
\]

(3.26)
The reason for this is that the Schrödinger equation in the ‘y’ direction only will result in wave functions that penetrate into the oxide region left and right of the silicon channel which is

\[ Y_a < Y < Y_b \]. But the amplitude of the wave function is very small in these oxide regions because of the larger band gap in the oxide than in the silicon region. As a result, the effective mass in oxide regions is not considered to play a significant role in the model and can be disregarded. In summary we may write the 2D Schrödinger equation as

\[
H^{2D} = -\frac{\hbar^2}{2}\frac{\partial}{\partial y} \left( \frac{1}{m_y^*(y)} \frac{\partial}{\partial y} \right) - \frac{\hbar^2}{2}\frac{\partial}{\partial z} \left( \frac{1}{m_z^*(z)} \frac{\partial}{\partial z} \right) + V(y, z)
\]  

(3.27)

The overall operation of this simulator can be summed up as depicted in the flowchart below.

---

Figure 3.3 Flowchart of the numerical approach used in the software [4]
3.2 Preview of the Simulator

The initial window of the NanowireMG software is shown in Fig. 3.4 provides us with options to describe the dimensions of the device structure which include the channel length, channel body thickness and gate dielectric thickness.

![Screen shot of the software Nanowire MG simulator showing the various parameters of the device structure that can be controlled](image)

Figure 3.4 Screen shot of the software Nanowire MG simulator showing the various parameters of the device structure that can be controlled [5]

The software can simulate nanowire channels with a minimum diameter of 3 nm and can go up to a maximum channel diameter of 50 nm. The source/drain lengths, channel length and gate length have the same range of 3 nm up to 50 nm. The dielectric thickness can be varied within the range of 1 nm up to 30 nm. This tool also allows one to simulate the nanowire
transistor in different gate configurations, namely gate all around, double gate, tri gate, omega and pi-gate configuration as seen in Fig. 3.5. For our simulation study, we will be using the Gate All Around (GAA) configuration, since it provides the best Short Channel Effects (SCEs) suppression enabling us to investigate the upper limits of performance for the InAs NWFET.

nanowireMG

Figure 3.5 Screen shot showing the different gate configurations that can be simulated using this software [5].

Although the NanowireMG software was initially configured for modelling the silicon material system, it is also flexible so that it can be used for other moderate bandgap materials such as InAs, Ge and GaAs. The software has options to change the material properties such as the semiconductor bandgap, dielectric constant, effective mass and work function, effectively giving us the option of simulating a different material for the NWFET channel. As shown in Fig.
3.6, The effective masses of electrons in the $x$, $y$, $z$ directions in each of the three valley bands $\Gamma$, $X$, $L$ for the channel, can be specified providing accurate device modeling for a particular material system based on the Effective Mass theory.

The same flexibility is available for the gate dielectric material, where the $\text{SiO}_2$ gate dielectric can be replaced with a nitride for example, based on use of its dielectric constant, work function and material bandgap. Figure 3.4 and 3.6 shows the setup for inputting of these parameters in the software.

Figure 3.6 Screen shot of the software window that enables changing the semiconductor material parameters for the nanowire [5].
As discussed in the previous chapter, electrons in InAs have a symmetrical effective mass in $x, y, z$ directions. This can be explained as follows. The most important semiconductor properties are determined by regions in the first Brillouin zone corresponding to lines and points of symmetry. The first Brillouin zone for the face-centered cubic, diamond, and zinc blende (III-V semiconductors) structures is the same and the electron energy within the first Brillouin zone varies as a function of wave vectors $K_x, K_y, K_z$ in the $x, y, z$ directions respectively. For materials such as silicon, Germanium, GaAs, InAs and compound III-V and II-VI compounds, the $\Gamma$ valley lies at the center of the first Brillouin zone, $\Gamma (000)$ while the $X$ and $L$ satellite valleys are displaced away from the center by a factor $X (2\pi/a) (100)$ and $L (2\pi/a) (111)$. From the energy band diagram of InAs (see Fig. 2.2), it can be seen that the conduction band minimum coincides with the $\Gamma$ valley. As a result the electrons in the InAs conduction band will have a constant energy surface in the first Brillouin zone which is spherical (symmetrical in $x, y, z$ directions). It is the same case in GaAs as well with its conduction band minimum coinciding with the $\Gamma$ valley and so InAs and GaAs are called direct band gap materials. On the other hand in silicon and germanium, the conduction band minimum is at the $X$ and $L$ valley, respectively, which is displaced away from the center of the first Brillouin zone, so these are indirect gap semiconductors. As a result the constant energy surface is no longer symmetrical for silicon and is ellipsoidal resulting in a longitudinal and transverse effective mass for the electrons.

The software also gives us the option of controlling the doping density both in the channel and in the Source-Drain (Shown in Fig. 3.7). For the most part in our simulation study we keep the channel doping to be 0, resulting in an intrinsic semiconducting channel. This is typically the case for nanowire FETs in order to reduce the detrimental effects of statistical variations in doping. The source-drain doping was kept fixed at $1 \times 10^{20}/\text{cm}^3$. 
The software simulates the device model for a fixed gate voltage while the drain voltage is swept across a range that can be user specified (see Fig. 3.9) giving us the $I_d - V_d$ characteristics shown later. Similarly the $I_d - V_g$ characteristics can be obtained for a set value of drain voltage (see Fig. 3.8). The user also has the option of setting the voltage increments during the voltage sweep. Smaller increments produce smooth characteristics and are more accurate in values; this however takes a longer run time for the simulation. The software by default maintains the device operating temperature at 300K, though it can be changed as per user specification.
3.3 Multigate Nanowire FET Simulator validation Results

The InAs NWFET is simulated for a channel diameter of 50nm and gate length of 50nm and gate dielectric thickness of 10nm was used to simulate the same device structure as studied by Thelander et al [6]. The above mentioned device structure was simulated to operate as an enhancement mode MOSFET, with a positive threshold voltage of $V_T = 0.083\text{V}$ as seen in Fig.3.9. Fig.3.9(a) shows the experimental results of Thelander et al [6] while Fig.3.9(b) shows the simulation result for the same device. This was obtained by converting the logarithmic graph of $I_{ds} - V_g$ into a linear graph (Fig. 3.9) by taking the square root of the drain current values and plotting it against the gate voltage. The resulting graph has a region of linear transconductance $dI_{ds} / dV_g$. It is conventional to linearly extrapolate a straight line along this region at the point of maximum slope; the intercept on the gate voltage axis is taken as the threshold voltage as shown in Fig.(3.10). The resulting gate voltage intercept denotes the threshold voltage of the device which is 0.083V in the case of our above simulated device (Fig.3.10b) versus 0.09V reported experimentally by Thelander et al [6]. Figure 3.10 (a) and (b) show the corresponding and very similar experimental and simulation results at a drain voltage of 1.0V. These plots give a threshold voltage of 0.0V (experimental) and 0.0V (Simulation).
Figure 3.9 (a) Experimental $I_{ds} - V_g$ characteristics on a linear scale at $V_{DS} = 0.5V$ reported by Thelander et al which gives a threshold voltage of $V_T = 0.09V$ [6] and (b) Simulated $I_{ds} - V_g$ characteristics using Nanowire MG at the same $V_{DS} = 0.5V$ which gives $V_T = 0.083V$. 
Figure 3.10 (a) $I_{ds} - V_g$ characteristics on a linear scale at $V_{DS} = 1V$ experimentally reported by Thelander and group [6] and (b) Simulated $I_{ds} - V_g$ characteristics using NanowireMG at $V_{DS} = 1V$.

It can be seen from these results both in the simulated and experimental work that by increasing the drain voltage, the threshold voltage shifts to a lower voltage i.e from 0.083V at $V_{DS} = 0.5V$ to 0.0V at $V_{DS} = 1V$ for our simulation results. The primary reason for this lowering of the threshold voltage is Drain Induces Barrier Lowering. At very short channel lengths the fields at the source and drain ends penetrate deeper into the channel thereby lowering the energy barrier between them independent of the gate’s role. When the drain voltage is increased, the resulting increase in the drain field further lowers the barrier resulting in lowering of the Threshold voltage as can be seen above by comparing Fig. 3.9 and 3.10.
The lowering of the threshold voltage is accompanied by an increase in the sub-threshold current as seen below in Fig. 3.11 where the experimental results are shown in Fig 3.11 (a) and the simulation results in Fig 3.11 (b).

![Figure 3.11](image)

Figure 3.11 (a) $I_{ds} - V_g$ characteristics on a logarithmic scale at $V_{DS} = 1V$ and $V_{DS} = 0.5V$ experimentally reported by Thelander and group [6] and (b) Simulated $I_{ds} - V_g$ characteristics at $V_{DS} = 1V$ and $V_{DS} = 0.5V$.

In comparing the results of our simulations with the work done by Thelander et al [6], we find a striking difference in the magnitude of the drain currents. From our simulation results we obtained a maximum drain current value of $17.6\mu A$ at a drain voltage of $V_d = 0.5V$ and $18.7 \mu A$ for $V_d = 1V$, whereas a peak drain current value of $2 mA$ at $V_d = 0.5V$ and $2.5 mA$ at $V_d = 1V$ were reported by Thelander et al as can be seen in Fig. 3.12 (a) and 3.12 (b). This is due to the reason that in their experimental work, an array of 61 InAs nanowires were considered, which resulted collectively in a higher drain current. However, as a reasonable approximation, to
calculate the maximum drain current obtained from a single InAs nanowire in their experimental work, when the experimental current values are divided by 61, a drain current value of 16.4µA is obtained at $V_d = 0.5V$ and 32.7 µA at $V_d = 1V$, which are close to the simulated values of 17.6 µA and 18.9 µA respectively, that we obtained. A second reason that our simulated result yielded a higher drain current over the experimental result is probably due to the fact that the Multi Gate Nanowire simulator simulates the device for a perfectly cylindrical nanowire free of defects, which in a practical case is quite difficult and would generally have surface irregularities (defects) that would cause scattering of charge carriers during their transport through the channel resulting in reduction in drain current. Another reason that would help explain the higher drain current in our simulated device is that the Multi Gate Nanowire simulator assumes that the NWFET is operating in the ballistic limit eliminating any losses of charges carrier momentum due to collision during transport along the channel. This, however is, not likely so in the experimental case wherein not all the nanowires have their lengths less than the ballistic limits and as a result scattering of charge carriers is likely occurring. From the experimentally reported results by Thelander et al [6] sub-threshold slopes of 88mV/dec and 103mV/dec were obtained for drain voltages of $V_d = 0.5V$ and $V_d = 1V$ respectively. From our simulation results we obtained sub-threshold slopes of 110mV/dec and 125mV/dec for drain voltages of $V_d = 0.5V$ and $V_d = 1V$ respectively. This shows that the experimentally fabricated device clearly had a better sub-threshold ON-OFF swing compared to our simulated device. It is not clear why this is the case; usually the opposite situation is seen when comparing the experimental and simulation results. One final important observation from our $I_{ds} - V_g$ simulation is that, the device characteristics match reasonably closely to the experimental results providing us confidence in the simulation results.

The $I_d-V_d$ characteristics of the experimental and simulated devices are shown in Fig.3.12, The nearly steady state saturated drain current condition in the simulated results as opposed to the continually increasing drain current seen in the experimental results, emphasizes the ideal wrap around condition of the gate over the channel that has been assumed in the simulation.
software. Another reason for the continuously increasing drain currents in the experimental results as opposed to the flat saturated condition in the simulated device is because of the effects of high series resistance the experimental device may have from the source/drain - Channel contacts (Fig 3.13a). Since series resistance has not been included in the simulation results we see a more ideal flat saturated condition in Fig. 3.13 (b).

Figure 3.12(a) Experimentally reported output characteristics at $V_G = -0.25V, 0V, 0.25V, 0.5V$ [6]  
(b) Simulated output characteristics for $V_G = 0V, 0.25V, 0.5V$.

The ON/OFF current ratio for a FET is an important performance measure. A high ON/OFF current ratio is preferred to maintain sufficient noise margins and reliability in switching states above and below the threshold voltages. Fig. 3.13 (a) and (b) show the experimental plots obtained by Thelander et al [6] and our simulated result respectively for the device structure as described above for a drain voltage of $V_d = 0.5V$. From the plots, we can calculate the ON/OFF current ratio and compare with the experimental results as follows.
The ON and OFF currents were calculated based on the metrics defined in [7].

ON current ($I_{ON}$)  =>  current at $V_g = V_t + (2/3) V_d$  \hspace{1cm} (3.19)

OFF current ($I_{OFF}$)  =>  current at $V_g = V_t - (1/3) V_d$  \hspace{1cm} (3.20)

The experimental results yield an $I_{ON} / I_{OFF}$ ratio of around $10^3$ where the ON current was $\sim 1 \times 10^{-3} A$ and OFF current was $\sim 1 \times 10^{-6} A$. A $I_{ON}$ current of 13.9 $\mu A$ was obtained in our simulation for $V_g = V_t + (2/3) V_d$ where $V_t$ was 0.08V. For the OFF current determination, for a gate voltage swing of 0.5V at a drain voltage of $V_{DS} = 0.5V$,

we get, $V_g = 0.09 - (1/3) 0.5 = -0.076V$. However, since the NanowireMG simulator allows us to simulate only for positive voltages we will take $I_{OFF} = 0.121 \mu A$ for $V_g = 0V$. As a result nd so is an underestimation. from our simulation results we get $I_{ON}/I_{OFF} = 10^2$. This is lower than the $10^3$ reported experimentally, but clearly our ratio was obtained for a smaller gate voltage swing.
The transconductance of a MOSFET is another electrical parameter that is an important measure of performance. It is a measure of the change in drain current for a change in gate voltage. It is always preferred to have high values of transconductance to achieve higher drive current and faster switching of the transistor. Fig. 3.14(a) and (b) are the experimental and simulated transconductances obtained, respectively, for the InAs NWFET.

The above transconductance plots (Fig.3.14 (a) and (b)) have been normalized with the nanowire diameters, which is 50nm in our simulations. We see that both the experimentally obtained transconductance plot and the simulated transconductance plot show similar device behavior with increase in gate voltage from 0 to 1V. A peak transconductance value of 0.045 S/mm was obtained for the simulated device, while the experimental data reported by Thelander et al is 0.8S/mm. However this
transconductance was achieved by an array of 61 nanowires. So this gives an individual nanowire FET transconductance of approximately 0.013 S/mm. We see that the simulated transconductance value for an individual Nanowire FET to be much higher than the experimental data by a factor of 3.5. This can be because, the simulator simulates the device under ballistic conditions and assuming perfect geometry for the nanowire. In practice there would be a degree of imperfection in nanowire geometry that would reduce the overall performance of the device causing carrier scattering and wouldn’t be purely ballistic. In addition, the experimental transistor undoubtedly has some series resistance at the source and drain contacts, which will also reduce the transconductance.

In summary, the results we obtained for the InAs NWFET, through simulation using Multi Gate Nanowire simulator were in close agreement with the experimental values and device characteristics reported by Thelander et al [6]. A maximum drain current of $I_d = 17.6\mu A$ at $V_d = 0.5 V$ was obtained for the simulated device compared to a maximum experimental drain current of $I_d = 16.4\mu A$. An $I_{ON}/I_{OFF} = 10^2$ was obtained from our simulation results for a reduced gate voltage swing (0.0V – 0.5V), while a $I_{ON}/I_{OFF} = 10^3$ was obtained experimentally for a much larger gate voltage swing of -0.15V – 0.45V. A higher normalized transconductance value of $g_m = 0.045 \text{ S/mm}$ was obtained in our simulated results, while a transconductance of $g_m = 0.013 \text{ S/mm}$ was reported experimentally bt Thelander et al [6]. The higher transconductance for the simulated device was attributed to the ballistic nature of the simulated device in contrast to experimental device which was likely not a ballistic device. In all, the Multi Gate Nanowire simulator [5] used for our study, showed good agreement with the experimental device behavior and characteristics giving us the confidence to proceed with our study on InAs Nanowire Field Effect Transistor (InAs NWFET) and the effects of scaling on the device characteristics.
References


Chapter 4

4. Scaling Effects in InAs NW-FET and Performance Comparison to Simulated Si NW-FET

4.1 Effects of Scaling in InAs Nanowire FET

Device structural parameters of the NW-FET such as dielectric thickness, channel diameter, source-drain doping, channel length and channel doping play a significant role in determining the performance of the transistor. In this chapter we vary these device structural parameters and study the corresponding effects of each of these parameters on the device performance to better understand the physics behind the device’s performance. We subsequently compare the performance of the InAs nanowire FET with that of a Si nanowire FET with exactly the same dimensions to study the device’s relative performance. This will also give us a good understanding of the effect the channel material has on the device performance and Short Channel Effects (SCE) such as DIBL, threshold voltage rolloff, Sub-threshold slope and ON/OFF current ratios. The device structure chosen as the baseline device is an n-channel NW-FET of channel length $L_{ch} = 30\text{nm}$, channel thickness $T_{ch} = 10\text{nm}$ with a silicon dioxide gate dielectric thickness of $T_{ox} = 2\text{nm}$. The gate work function was set at 5.3eV to obtain a good threshold voltage value and low OFF currents of the order of $1 \times 10^{-12} \text{A/um}$. The Multi Gate Nanowire [1] simulator gives us options to vary the nanowire channel length, channel thickness, gate dielectric thickness and doping concentration in the channel. The source and drain doping concentrations are set at a default doping concentration of $2 \times 10^{20}\text{cm}^{-3}$. The channel was simulated for an intrinsic condition, with an intrinsic doping concentration of $N_{ch} = 1 \times 10^{15}\text{cm}^{-3}$, which is typically done for NW-FETs in order to avoid effects of random dopant fluctuations. For all our simulations, a gate voltage corresponding to a drain current of $1 \times 10^{-7} \text{A/um}$ was taken to be the threshold voltage of the device.
4.1.1 Variation in the Channel Length

The channel length was varied while keeping the channel diameter and gate dielectric thickness constant. In this case we simulated the InAs NWFET for channel lengths of 20nm, 25nm, 30nm, 35nm, 40nm, 45nm, 50nm. The channel diameter for the square cross-sectional nanowire was kept at 10nm and the dielectric thickness was set at 2nm. Figure 4.1 below shows the $I_d-V_g$ characteristics obtained for the device with varying channel lengths for a $V_d = 0.5V$. The current values have been normalized by dividing it by the nanowire diameter.

(a)

(b)
(c)

Figure 4.1 (a) $I_d-V_g$ characteristics at a drain voltage of $V_d = 0.5V$ for variation in channel length.  
(b) Marginal increase in drain current near saturation as the channel length is decreased

From the above characteristics seen in Fig. 4.1(a) and (b) it is seen that there is a monotonic increase in the ON current from a value of $I_d = 0.1354 \text{ A/μm}$ for a 50nm channel length to $I_d = 0.151 \text{ A/μm}$ for channel length of 20nm. This increase in monotonic increase in ON current can be understood from the expression for ON current below [2].

$$I_d = \frac{\mu_{eff}C_{ox}W}{L} \cdot (m - 1) \cdot e^{\frac{q(V_g-V_T)}{mKT}}$$  \hspace{1cm} (4.1)

With the decrease in channel length, the drain current increases due to their inverse relationship. Qualitatively, it can be said that since the electrons travel a shorter distance from source to the drain, they experience lesser scattering events leading to an increase in drain current. This is the case for conventional MOSFETs where the channel length is long, i.e larger than the mean free path.
However, in this work we are assuming ballistic transport so the likely origin of the increase in drain current is the effect of the drain bias in reducing the barrier height at the source end of the channel as shown in Fig 4.1 (c).

The OFF currents increase dramatically with a decrease in channel length varying from a minimum of $0.12 \times 10^{-12} \ A/\mu m$ at 50nm channel length to over 3.5 nA/μm at 20nm. This change in OFF currents in the order of $10^3$ can be attributed to Drain Induced Barrier Lowering (DIBL) which plays a significant role at such short channel lengths. It was observed that for channel lengths above 25nm, near ideal sub-threshold slopes were obtained with values of 67mv/dec at 30nm channel length and 62mv/dec at 35nm channel length. However, the sub-threshold slope increases rapidly with a decrease in channel length below 25nm, where a sub-threshold slope 102mv/dec was obtained for channel length of 20nm. This degradation in sub-threshold slope is a typical short channel phenomenon that play a significant role at these short channel lengths. Fig.4.2 shows the trend of increasing sub-threshold slope as the channel length is reduced.

![Subthreshold Slope Vs Channel length](image)

Figure 4.2 Simulation results for variation of sub-threshold slope with channel length.

The sub-threshold slope values were obtained by calculating the amount of gate voltage swing needed to obtain a decade change in the drain current from the $I_D-V_G$ characteristics shown in
From the plot in Fig.4.2, a sub-threshold slope variation from 102 mV/dec for channel length of 20 nm to 60.5 mV/dec for channel length of 50 nm were observed. A near ideal sub-threshold slope of 60.8 mV/dec and 60.5 mV/dec was obtained at the longer channel lengths of 45 and 50 nm due to almost complete suppression of short channel effects and excellent gate control over the channel due to the wrap around structure. We would like to have the sub-threshold slope value as low as possible since this helps the MOSFET to switch efficiently from the OFF state to the high conduction ON state and vice versa. Ideally the theoretical lower limit for the sub-threshold slope is set at 60 mV/dec [2], which is due to the overall physics involved in the process of an electron crossing over an energy barrier. Where the probability of an electron crossing over an energy barrier is given by the exponential dependence of the barrier height over the thermal energy.

The DIBL for each device structure was calculated by plotting the $I_D$-$V_G$ characteristics of the device for maximum and minimum values of drain voltages, which are 0.05 V and 0.8 V, respectively, in the simulations as shown in Fig.4.3, then the change in threshold voltage (Gate voltage corresponding to a drain current of $1 \times 10^{-7} A/\mu m$) divided by the difference in the applied drain voltages (0.75 V in this case). It is seen from Fig.(4.4) that the DIBL increases rapidly to a value of 134 mV/V for a 20 nm long channel length compared to 65 mV/V for a 25 nm channel length. This effect is more clearly plotted in Fig.4.1(c) that shows the lowering of the barrier in the source side as the channel length is reduced from 50 nm to 20 nm.
Figure 4.3 $I_D-V_G$ characteristics for drain voltages of $V_d = 0.05V$ and 0.8V.

Figure 4.4 Drain induced barrier lowering effects with reduction in channel lengths.
Another well known short channel effect is the variation in the threshold voltage with variation in channel length. This effect was examined for the InAs NWFET and the results are shown in Fig4.6 where the threshold voltage was taken as the gate voltage when the drain current reaches $10^{-7} A/\mu m$

![Threshold Voltage Roll-off](image)

Figure 4.6. Threshold voltage roll off with channel length at drain voltages of $V_d = 0.5V$ and $V_d = 0.8V$

A net threshold voltage change of 0.21V was observed (0.36V- 0.15V) for variation in channel length from 50nm to 20nm at a drain voltage of $V_d = 0.5V$. A higher threshold voltage change of 0.24V was observed (0.36V - 0.12V) at a higher drain voltage $V_d = 0.8V$ due to the increased field at the drain side corresponding to a 18.5% drop in threshold voltage for an increase in drain voltage from 0.5V to 0.8V at the 20nm channel length. However, at larger channel lengths (above 40nm) we see that the threshold voltage change with drain voltage is very small due to very low short channel effects. So significant fluctuations in threshold voltage of devices due to process variations will be seen when the channel length becomes less than 40nm.
The ON-OFF currents are also dependant on the channel length of the device. Throughout our simulations the ON current was taken as the drain current at 0.8V gate voltage for a maximum drain voltage of 0.8V. The OFF current was obtained as the sub-threshold drain current at 0V gate voltage for the same drain voltage of 0.8V. The ON and OFF currents are shown in Figures 4.7 and 4.8 respectively as a function of channel length. Note the linear current scale for the ON current variation, but the logarithmic scale for the OFF current change. The dramatic increase in the OFF current as the channel length is reduced is due to increased electron tunneling from the source to the drain through the potential energy barrier at the source end of the channel. Fig 4.1 (c) shows the thinning of the potential energy barrier as the channel length is reduced.

![Graph showing ON current variation for channel lengths at V_d = 0.8V](image)

Figure 4.7 ON current variation for with channel lengths at V_d = 0.8V
Figure 4.8 OFF current variation with channel lengths at $V_d = 0.8V$.

From Fig.4.7 and Fig.4.8 we observe that the ON current increases monotonically for a decrease in channel length while the OFF current increases approximately exponentially. A very low OFF current of 0.1pA was observed for a channel length of 50nm, but increases to 6nA (a factor of $6 \times 10^3$ times higher) for a channel length of 20nm. Meanwhile ON current of $0.1\mu A/\mu m$ was observed for the 20nm channel length versus $7.4 \times 10^{-5}mA/\mu m$ for a 50nm channel length (a factor of 1.38X). It is to be noted that the drain currents have been normalized by dividing by the channel diameter, which is 10nm in this case so the units are $\mu A/\mu m$. Fig (4.9) below shows the simulated results for variation of ON/OFF current ratio with channel length. A high ON/OFF current ratio is desirable to have good noise margin to avoid unwanted switching, low off state leakage currents and good transconductance for the device. A very high ON/OFF current ratios in the order of $6 \times 10^9$ was obtained at a channel length of 50nm, but this degrades to $\sim 10^4$ at 20nm. The change in OFF currents mainly determine the difference in the ON/OFF ratio considering that the ON currents vary relatively little with channel length while the OFF currents vary nearly exponentially as seen in Fig.4.7 and 4.8, respectively.
Figure 4.9 Simulation results for drain current ON/OFF ratio variation with channel length

Shown below in Fig.4.10 is the variation in the transconductance of the device with channel length. A peak transconductance value of $g_m = 0.286$ S/mm and $g_m = 0.283$ S/mm were observed for drain voltages of $V_d = 0.8V$ and $0.5V$, respectively. As expected the transconductance drops at shorter channel lengths due to increased electron tunneling, i.e decreasing gate control of the charge in the channel and the flow of electrons through the potential energy barrier in the channel near the source.
Figure 4.9 Simulation results for transconductance variation with channel length for drain voltages of $V_d = 0.8V$ and $0.5V$
4.1.2 Variation in Channel Diameter

Channel thickness or diameter also has a strong influence over the transport properties of the nanowire and the performance of the NWFET. In our simulations we simulated the nanowire for diameters of 8-15nm at a constant channel length of 30nm and oxide thickness of 2nm. The results are shown in Fig. 4.11.

Figure 4.11 $I_d$-$V_g$ characteristics of the InAs NWFET for increasing channel thicknesses at $V_d = 0.5$V

As the channel thickness is increased, it is observed that the saturation drain current increases, but there is a much larger increase in the OFF current resulting in increased sub-threshold slope as seen in Fig.4.12
Since the gate bias has its strongest control of the charge in the channel closest to the gate, the gate’s control weakens as the channel diameter increases. This allows a larger leakage current or OFF current to flow, hence the degradation in the sub-threshold characteristics seen in Fig. 4.10 and quantified in Fig.4.12. Near ideal sub-threshold slopes with values of 62.6, 64, 65.5 and 67mV/dec were obtained for channel thickness of 8, 9, 10 and 11nm, respectively. Comparing the effects of channel length and channel thickness on sub-threshold slope, we observe that channel length plays a more significant role in the control of this short channel effect than the channel thickness.
The DIBL was also investigated as a function of the channel diameter; the results are shown in Fig.4.13

![DIBL variation with channel thickness of the InAs NWFET.](image)

The immunity towards DIBL for a constant channel length of 30nm is reduced as the channel thickness is increased from 8nm to 15nm. This can be explained on the basis of degradation in the gate’s control over the channel. As discussed above, as the channel thickness is increased, the channel volume increases while the oxide thickness is maintained constant at 2nm. As a result, the gate capacitance per unit area reduces and so the effective gate control is diminished with increasing channel thickness. This reduced gate control makes the DIBL more prominent as the channel thickness is increased as shown in the plot of the simulated results in Fig4.12. A DIBL of 93mV/V was obtained for a channel thickness of 15nm while 22mV/V at 8nm channel thickness which corresponds to a 76% improvement in DIBL suppression over a channel thickness range of 8nm – 15nm.

The threshold voltage variation with channel diameter was also examined. The simulated results for the nanowire transistor showed that the threshold voltage is significantly dependant on the
channel thickness. The threshold voltage is seen to increase rapidly with a decrease in channel thickness as shown in Fig 4.14. Unlike the effect of channel length where the threshold voltage decreases as the channel length was decreased, here we see that the threshold voltage increases as the channel diameter is decreased.

Figure 4.14 Simulated threshold voltage variation with channel thickness for the InAs NWFET.

As the channel thickness is reduced, the gate has better control of the charge carriers in the channel, resulting in reduced short channel effects and increased threshold voltage. In particular, as the nanowire thickness is reduced to very small dimensions quantum effects begin to play a major role in the way charges are present within the nanowire and the quantum confinement effects start to have a very significant effect on the threshold voltage [2]. Since the electrons are confined in a potential well formed by the oxide barrier and silicon conduction band for both directions perpendicular to the direction of current flow, and their motion is limited to a direction along the channel. At high normal fields these electrons are grouped into discrete energy levels that are grouped into sub-bands. The lowest energy level is some finite energy higher than the bottom of the conduction band and this increases as the nanowire diameter is reduced. As a result more band
bending is required to populate the lowest band that translates to a higher threshold voltage. The simulated results showed an increase in threshold voltage from 0.09V to 0.46V within a channel thickness variation of 8nm-15nm. This is 5X increase in the threshold voltage value.

The effect of channel diameter on the NWFET ON-OFF currents was also examined. From Fig(4.15) it can be seen that, as the channel thickness is increased, the ON currents increases almost linearly. This is because as the channel diameter is increased there are more number of modes available for the electrons to populate in the channel. Also in practice though not simulated here, by increasing the channel diameter the electrons have more volume to travel in, thereby reducing the surface scattering effects that the nanowires otherwise posses due to their very large surface to volume ratio. A maximum ON current of 0.18mA/μm was obtained at a channel thickness of 15nm. This corresponds to an increase of 0.14mA/μm in drain current (344% increase) for a channel thickness varying from 8nm to 15nm.

![ON Current Vs Channel Thickness](image)

Figure 4.15 Simulated ON current variation with channel thickness at $V_d=0.5V$ for the InAsNWFET
However, the OFF currents increased more dramatically with channel thickness increase due to reduced gate control as seen in Fig.4.16. The OFF current versus channel thickness graph has been plotted in a logarithmic scale to clearly show the OFF currents.

![Graph showing variation of OFF current with channel thickness at V_d = 0.5V](image)

Figure 4.16 Variation of OFF current with channel thickness at V_d = 0.5V

The OFF current varied from \(8.9 \times 10^{-15}\) A/\(\mu\)m at 8nm to 13.5 nA/\(\mu\)m at 15nm, which corresponds to an OFF current that is \(~10^6\) times higher. Such a large increase in OFF current is undesirable and so significant control over maintaining the nanowire thickness constant throughout the fabrication process is extremely critical to avoid large variations in OFF currents. Extremely low OFF currents of the order of \(~10^{-15}\) and \(10^{-13}\) A/\(\mu\)m were obtained at small channel thicknesses of 8 and 9nm, respectively, which are excellent values compared to existing OFF current values for nano-scale, planar silicon MOSFETs of 70nA/\(\mu\)m (65nm technology node) and 100nA/\(\mu\)m (45nm technology node) [4].
Finally, using the above results we obtained and plotted the ON/OFF current ratio versus channel diameter as shown in Fig.4.17. A maximum ON/OFF current ratio of $\sim 10^9$ for a channel thickness of 8nm was obtained. We see that the ON/OFF current ratio decreases significantly with an increase in channel thickness due to the exponential increase in OFF currents with increasing channel thickness.

![Figure 4.17 Simulation results for ON/OFF current ratio variation with respect to channel thickness](image)

The transconductance with variation in channel diameters were studied and plotted as seen in Fig.4.17. The normalized transconductance values were observed to increase with increase in channel diameters. A normalized transconductance value of 0.52 S/mm was obtained for a channel diameter of 15nm while a lower transconductance value of 0.22 S/mm was obtained for 8nm channel diameter. This corresponds to a 58% decrease in the device transconductance for channel diameter variation from 15nm to 8nm, indicating that the device transconductance has a reasonably strong dependence on the channel diameter.
4.1.3 Variation in Gate Dielectric Thickness

In this set of simulations we kept the channel length and channel thickness constant and varied the gate capacitance per unit area by varying the gate dielectric thickness. In these simulations, as previously, Silicon dioxide (SiO$_2$) was used as the gate dielectric with a dielectric constant value of 3.9 and a oxide bandgap of 9eV. The channel length was set at 30nm and the channel thickness at 10nm. The gate oxide was varied from 1 to 5nm. Shown in Fig. 4.18 are the $I_d$ – $V_g$ characteristics of the InAs NWFET as the gate oxide thickness was varied.
From the $I_d-V_g$ characteristics above it is seen that as the dielectric thickness is reduced from 5nm to 1nm, the drain saturation current increases relatively little, but there is significant effect on sub-threshold slope of the device. The sub-threshold slope was studied with change in gate oxide thickness from 1nm to 5nm shown in Fig.4.19. It was seen that the sub-threshold slope increases with increase in oxide thickness due to the reduced gate control and gate oxide capacitance. But this increase is not very severe compared to the effects of channel length or channel diameter variation seen previously. Sub-threshold slope values varied from 64mV/dec – 74.6mV/dec obtained for oxide thickness variations from 1 to 5nm. The role of the oxide thickness can be understood from the expression for the sub-threshold slope [2]
where

\[ m = 1 + \frac{C_{dm}}{C_{ox}} \]  

(4.3)

So by decreasing the gate oxide thickness we increase the gate oxide capacitance per unit area ‘\( C_{ox} \)’, which results in reducing the factor ‘\( m \)’ and so the sub-threshold slope to lower values towards ideal value of 60mV/dec.

\[ S = \frac{(2.3) m k T}{q} \]  

(4.2)

Figure 4.19 Sub-threshold slope variation with change in gate dielectric thickness

The plot for DIBL with respect to oxide thickness is shown below in Fig. (4.20). The DIBL is seen to increase nearly linearly with an increase in gate oxide thickness. As the oxide thickness is increased, the capacitance per unit area decreases.

\[ C_g = \frac{\varepsilon_0 \varepsilon_r A}{T_{OX}} \]  

(4.4)

This results in reduction of gate control over the channel charge allowing the effects of the drain bias to become more important and leads to an increase in DIBL.
A DIBL value of 76mV/V at 5nm oxide thickness was obtained. Scaling down the oxide thickness to 1nm resulted in improved DIBL suppression with a value of 21mV/V. But at such low oxide thicknesses, device reliability is a major concern due to electron tunneling through the oxide to the gate. This problem can be overcome by replacing the SiO$_2$ dielectric with another gate dielectric with a higher dielectric constant such as hafnium oxide (25). This allows us to use a thicker gate dielectric that would still give us the same equivalent oxide capacitance as seen in eqn 4.5.

$$T_{HK} = T_{EOT} \frac{\varepsilon_{HK}}{\varepsilon_{SiO_2}}$$ (4.5)

An increase in threshold voltage was observed as the gate oxide thickness was reduced as seen in Fig 4.21. This is similar to the increase in $V_{th}$ that was observed as the channel thickness was reduced. Improved gate control over the channel resulted in better suppression of DIBL as seen in Fig 4.20 resulting in lesser threshold voltage roll off and higher threshold voltage values.
A threshold voltage increase of 1.3X was observed from a variation of threshold voltage from 0.25V at 5nm oxide thickness to 0.34V at 1nm.

![Threshold Voltage Vs 1/Tox](image)

Figure 4.21 Simulated results for the threshold voltage change with variation in gate oxide thickness

The OFF currents were also examined as shown in Fig.4.22 and found to increase with increase in oxide thickness due to a decrease in gate capacitance per unit area. The OFF currents increased by a factor of $\sim 10^2$ for an oxide thickness increase from 1 to 5nm. This corresponds to $\sim 40A/\mu m$ increase in OFF current for every 1nm increase in gate oxide thickness.
Similarly, the ON currents were examined as seen in Fig.4.23. The ON currents increased relatively little with decrease in gate dielectric thickness. A 9% increase in ON current was obtained by reducing the gate dielectric thickness from 5nm to 1nm. By combining the results for ON and OFF currents, the ON/OFF current ratio was calculated for each gate oxide thickness and the results are shown in Fig.4.24. A maximum ON/OFF current ratio of $2 \times 10^8$ was obtained for an oxide thickness of 1nm while a value of $9 \times 10^5$ was seen for an oxide thickness of 5nm with most of the change due to the change in OFF currents.
Figure 4.23 Simulated ON current variation for oxide thicknesses of 1, 2, 3, 4, 5nm

The transconductance of the device with variation in gate oxide thickness variation was examined as shown in Figure 4.25. It was observed that the normalized transconductance weakly reduced with increase in the gate oxide thickness. A transconductance value of 0.316S/mm for a gate oxide thickness of 1nm in comparison to a transconductance value of 0.2461S/mm for a
5nm gate oxide thickness. This corresponds to a 22% decrease in transconductance value for an increase in gate oxide thickness in the range of 1nm to 5nm, roughly about .014S/mm decrease in transconductance for every 1 nm increase in gate oxide thickness. This decrease in device transconductance with thicker gate oxide is due to decrease in gate capacitance resulting in reduced control of the gate over the mobile charges in the channel.

Figure 4.25 Normalized transconductance with variation in Gate oxide thickness at V_d = 0.5V
4.2 Comparison of InAs NWFET with Si NWFET

In this section, for comparison Si NWFETs are simulated for the exact device structure parameters as the InAs NWFET. The channel thickness, channel doping and gate oxide thickness were maintained the same and the channel length was varied to study the behavior of the Si NWFET in comparison to that of the InAs NWFET to see the effects of material parameters on Short Channel Effects. Table 4.1 provides a comparison of the material properties of Silicon and Indium Arsenide.

Table 4.1 Comparison of Silicon and Indium Arsenide Material Properties [5]

<table>
<thead>
<tr>
<th>Material Properties</th>
<th>Silicon (Si)</th>
<th>Indium Arsenide (InAs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electron Mobility (cm$^2$/V-s)</td>
<td>1480</td>
<td>34000</td>
</tr>
<tr>
<td>Hole Mobility (cm$^2$/V-s)</td>
<td>540</td>
<td>530</td>
</tr>
<tr>
<td>Electron Effective Mass</td>
<td>m$_e$ = 0.98m$_0$</td>
<td>m = 0.024m$_0$</td>
</tr>
<tr>
<td></td>
<td>m$_h$ = 0.19m$_0$</td>
<td></td>
</tr>
<tr>
<td>Band Gap Energy (eV)</td>
<td>1.12</td>
<td>0.36</td>
</tr>
<tr>
<td>Dielectric Constant</td>
<td>11.9</td>
<td>14.3</td>
</tr>
<tr>
<td>Work Function</td>
<td>4.05</td>
<td>5.06</td>
</tr>
<tr>
<td>Intrinsic carrier concentration (cm$^{-3}$)</td>
<td>1.4×10$^{10}$</td>
<td>1×10$^{15}$</td>
</tr>
</tbody>
</table>
4.2.1 $I_d-V_g$ characteristics

Initially, the $I_d-V_g$ characteristics of the Si and InAs NWFETs were examined. Shown in Fig. 4.24 (a) and (b) are the characteristics for both the Si and InAs NWFET, respectively.

![Id-Vg variation with channel length](image)

(a)  

Figure 4.26 (a) $I_d-V_g$ characteristics for Simulated Si NWFET for variation in channel lengths  
(b) $I_d-V_g$ characteristics for Simulated InAs NWFET for variation in channel lengths.

From the above $I_d-V_g$ characteristics one aspect that can be clearly stated is that InAs NWFET gives a higher drain current of 0.102 mA/μm compared to Si NWFET with 8.36μA/μm at a channel length of 20nm. It can also be seen that from the sub-threshold slope variation is larger for InAs NWFET, which would most likely contribute to a higher threshold voltage roll-off compared to the Si NWFET characteristics, which would be analyzed more in detail in section 4.2.4. However, This high drive current with acceptable levels of OFF current in InAs NWFET could play a major role in High Performance (HP) logic technologies at very short channel lengths.
From the simulated $I_d$-$V_g$ characteristics for Si NWFET and InAs NWFET in Fig. 4.26 (a) and (b), respectively, we calculate the Sub-threshold slope variation, DIBL, threshold voltage roll-off and ON-OFF current ratio for various channel lengths. The DIBL is calculated from $I_d$-$V_g$ characteristics obtained for drain voltages of 0.05V and 0.8V. The ON-OFF currents were calculated from $I_d$-$V_g$ characteristics at maximum drain voltage of $V_d = 0.8V$. They are then compared for performance with those for the simulated InAs NWFET.

### 4.2.2 Comparison of Sub-Threshold slope variation

From Fig.4.25, the sub-threshold slopes were calculated for both InAs and Si NWFET as a function of channel length as shown in Fig.4.27. InAs NWFET shows higher sub-threshold slopes for all simulated channel lengths in comparison to the Si NWFET. A sub-threshold slope of 102mV/dec at a channel length of 20nm was observed in the InAs NWFET while the Si NWFET had a sub-threshold slope of 73mV/dec which is a 39% decrease in the sub-threshold slope value.

![Sub-Threshold Slope Vs Channel length](image)

**Figure 4.27** Comparison between InAs NWFET and SiNWFT for simulated sub-threshold slope values with varying channel lengths
The difference in sub-threshold slopes can be explained through the difference in the dielectric constants of Si and InAs. The sub-threshold slope expression is given by [2]

\[
S = \frac{(2.3)m k T}{q}
\]  \hspace{1cm} (4.3)

where, ‘m’ is the body effect coefficient given by the expression

\[
m = 1 + \frac{c_{dm}}{c_{ox}}
\]  \hspace{1cm} (4.4)

where \(c_{dm}\) is the depletion capacitance given by

\[
c_{dm} = \frac{\varepsilon_S}{w_{dm}}
\]  \hspace{1cm} (4.5)

where \(\varepsilon_S\) is the dielectric constant of the semiconductor channel. Since InAs has a higher dielectric constant of 14.3 compared to the dielectric constant of Si 11.9, a higher body effect coefficient value \(m\) is seen for InAs which results in increased sub-threshold slope value. This does not explain all the differences between the InAs and Si results since this sub-threshold slope expression is only an approximate one that is accurate for the long channel transistors.

4.2.3 Comparison of DIBL Effects

From the simulated results of both the InAs NWFET and Si NWFET, the Drain Induced Barrier Lowering (DIBL) effects with varying channel lengths were obtained and plotted as shown in Fig (4.28). It is seen that Silicon Nanowire FET offers superior DIBL suppression for exactly the same device structure as compared to the Indium Arsenide Nanowire FET. At a short channel length of 20nm the InAs NWFET had a DIBL of 134mV/V while the Si NWFET had a DIBL value that was nearly half of InAs NWFET (DIBL = 60.2mV/V).
Figure 4.28 Comparison between InAs NWFET and Si NWFET for the simulated DIBL values with varying channel lengths.

This increase in DIBL in InAs in comparison to Si can be attributed to the smaller transverse electron effective mass of InAs which is nearly 8 times smaller than the electron effective mass of Si. This can be explained as follows, The energy eigenvalue of an electron determines the energy levels an electron can occupy in the conduction band. An electron with a higher energy eigenvalue can occupy higher energy levels. Since the energy eigenvalue of an electron is inversely proportional to its effective mass, a lighter electron will have a higher energy eigenvalue allowing it to occupy higher energy levels within the conduction band. As a result, for an applied drain voltage, electrons occupying the higher energy levels would be able to overcome the barrier much more easily than those electrons that are at the base of the conduction band occupying the lower energy levels. As a result in InAs NWFET, whose electrons are at the higher energy levels enter the channel from the source more easily for an applied drain voltage. Whereas for Si a higher drain voltage would be necessary to lower the source-channel barrier to get the same amount of DIBL value. As the channel length is increased it can be seen that the
difference in the DIBL values between the two devices reduce due to enhanced gate control of
the wrap around gate structure and the sufficient large distance between the source and the drain
regions.

4.2.4 Comparison of Threshold Voltage Roll-off

Also examined were the threshold voltage for the InAs and Si NWFET devices and their
variation with channel length as shown in Fig.4.29. From the simulations carried out, we see that
not only does InAs NWFET show a lower threshold voltages for any given channel length, but it
also is more susceptible to threshold voltage rolloff, i.e. its rolloff is more rapid with decreasing
channel length.

Figure 4.29 Comparison between InAs NWFET and Si NWFET for threshold voltage roll off
with channel lengths
From Fig 4.29 we see that InAs NWFET shows a threshold voltage rolloff 0.21 V at $V_d = 0.5V$ and 0.24 V at $V_d = 0.8V$. By comparison we find that in Si NWFET has a threshold voltage rolloff of only 0.07 V at $V_d = 0.5V$ and 0.08 V at $V_d = 0.8V$. This corresponds to a 66% roll off of threshold voltage in InAs NWFET compared to a 17% rolloff in the Si NWFET at the maximum drain voltage of $V_d = 0.8V$. This can be explained as follows using the expression for threshold voltage roll off as shown below [2]

$$\Delta V_T = \theta(m - 1) \sqrt{\frac{\psi_{bi} (\psi_{bi} + V_{ds})}{e^2 m^2 W}}$$

(4.6)

Because of the higher dielectric constant of InAs (14.3), the ‘m’ value obtained from equation (4.4) and (4.5) is higher than that for Silicon. Substituting this value of body coefficient in equation (4.6), which is both exponentially dependant on the ‘m’, value results in an increased threshold voltage roll off.

**4.2.5 Comparison of ON-OFF Current Variation**

The ON-OFF currents in InAs and Si devices were investigated and plotted as shown in Fig.4.30. The ON-OFF currents are significantly dependant on the device’s physical parameters including namely gate length, channel thickness, doping concentration and gate dielectric thickness. They are also dependant on the material of the channel through which the charge carriers travel from the source to the drain. The reason the ON-OFF currents are dependent on the channel material is predominantly due to concept of electron effective mass, which is the mass of the electrons in a specific material relative to the mass of a free electron. The electrons in Indium arsenide have a very low symmetrical effective mass of $0.024m_0$ compared to the transverse effective mass of $0.19m_0$ in silicon. This very low effective mass translates to very high electron mobility. For a given magnitude of electric field, the electrons in InAs having a lower effective mass would be accelerated much faster compared to the Si electrons. This higher
mobility results in higher ON currents and as a result higher switching speeds for the transistor. Shown below is a plot showing the comparison of ON currents in InAs NWFET and Si NWFET varying with channel lengths. The small change in ON current with channel length is due to the assumption of ballistic transport in the modeling of the device.

Figure 4.30 Comparison between InAs NWFET and Si NWFET for ON currents with variation in channel lengths.

The ON currents in the simulation were obtained as the drain current at 0.8V gate voltage for a maximum drain voltage of 0.8V. The OFF currents similarly were obtained as the sub-threshold drain current at 0V gate voltage for a maximum drain voltage of 0.8V. It can be seen that InAs has an ON current which is higher by a magnitude of 10 compared to Silicon. A maximum ON current of 0.10mA/μm was obtained in the simulation at a channel length of 20nm. Correspondingly an ON current of 8.4μA/μm was obtained in the SiNWFET. This is approximately 12X higher in magnitude compared to the ON current in the Si NWFET. This is important since the circuit delay is given by the simplified equation [2] shown below in equation (4.7)

$$\tau = \frac{C.V_{dd}}{I_d}$$  \hspace{1cm} (4.7)
The 12X increase in drain current in InAs NWFET results in 12X reduction in circuit delay time making circuit operations 12 times faster.

Figure 4.31 shows the plot for variation of OFF currents with change in channel lengths for both InAs and Si NWFET. The increased OFF currents for any given channel length in InAs NWFET compared to Si NWFET is because InAs has a very small bandgap of 0.36eV compared to a bandgap of 1.12eV of silicon. So electrons are able to more easily tunnel through the potential energy barrier at the source end of the channel at room temperatures at zero gate voltage, contributing to increased OFF currents. The leakage currents are increased due to the very low electron effective mass, making it easier for the electrons to jump over the source channel junction barrier as explained earlier. OFF currents of magnitude $10^4$ times higher were observed in our simulations for channel length of 20nm.

Figure 4.31 Comparison between InAs NWFET and Si NWFET for OFF currents with variation in channel lengths

The plots for ON/OFF current ratios with variation in channel length are shown in Fig.4.32 and shows higher ON/OFF ratios in Si NWFET by a factor of $10^3$ compared to the InAs NWFET at a channel length of 20nm. This factor gradually reduces to a factor of 10X as the channel length is increased towards 50nm. The primary reason for higher ON/OFF ratios in Si NWFET is
due to the better sub-threshold characteristics that were observed, namely lower OFF currents and lower sub-threshold slopes for the Si NWFET, when compared to the InAs NWFET.

Figure 4.32 Comparison between InAs NWFET and Si NWFET for ON/OFF current ratio with variation in channel lengths

Finally the transconductance curves were plotted for InAs NWFET and Si NWFET and examined at a drain voltage $V_d = 0.5V$ as shown in Fig.4.33.
4.2.6 Summary of InAs NWFET Comparison with Si NWFET

Table 4.2 Summary of Comparison of InAs NWFET and Si NWFET Device Performance for Channel Length of 20nm.

<table>
<thead>
<tr>
<th>Device Performance Parameter</th>
<th>Indium Arsenide (InAs)</th>
<th>Silicon (Si)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain Induced Barrier Lowering (mV/V)</td>
<td>134</td>
<td>60.2</td>
</tr>
<tr>
<td>Sub-threshold slope (mV/dec)</td>
<td>102</td>
<td>73</td>
</tr>
<tr>
<td>Threshold Voltage, Vd = 0.5V (V)</td>
<td>0.15</td>
<td>0.386</td>
</tr>
<tr>
<td>ON Current, Vd = 0.8V (A/μm)</td>
<td>0.10 × 10⁻³</td>
<td>8.4 × 10⁻⁶</td>
</tr>
<tr>
<td>OFF current, Vd = 0.8V (A/μm)</td>
<td>7.1 × 10⁻⁹</td>
<td>9.5 × 10⁻¹³</td>
</tr>
<tr>
<td>ON/OFF Ratio</td>
<td>1.4 × 10⁴</td>
<td>8.8 × 10⁶</td>
</tr>
</tbody>
</table>

In summary, it can be said that the Si NWFET shows better immunity towards short channel effects compared to InAs NWFET with OFF currents 10⁴ times lower, 39% lower sub-threshold slopes, very low threshold voltage roll off of 17% with channel length in comparison to 66% in InAs NWFET and ON/OFF ratios varying from 10⁷-10⁹ compared to ON/OFF current ratio of 10⁴-10⁸. For the InAs NWFET however, InAs NWFET has the advantage of higher ON currents that are 12X higher than the Si NWFET which would lead to increased switching speeds by a factor of 12X. Because of the very low bandgap of InAs (0.36eV), InAs NWFET would also require much lower active power to switch resulting in lower active power dissipation. Additionally, the InAs NWFET has the advantage of being able to scale down the threshold voltage of the device to much lower values due to its very small band gap further improving the
switching speeds. However schemes to control the OFF currents would need to be developed to achieve a leakage current under acceptable levels of 100nA/μm. So, in conclusion, Si NWFETs with low OFF currents and good immunity to short channel effects, prove to be a good candidate for Low Operating Power applications (LOP) while InAs with its high ON currents and switching speeds prove to be a good candidate for High Performance applications (HP) where reasonably high OFF currents are acceptable as a trade off for increased operating speeds.
References


Chapter 6
Conclusion and Future Work

In this study we have investigated the electrical properties of an n-channel enhancement mode InAs nanowire MOSFET using the quantum-ballistic transport model implemented in the simulator Multigate Nanowire. We started the study by initially validating the simulator against experimentally reported data for InAs nanowire FET by Thelander et al [1]. A very good agreement in device performance and characteristics was observed between the experimental and our simulated results. Although our simulated results had a higher drain current of 17.6\(\mu\)A at \(V_d = 0.5\)V compared to a drain current of 16.4\(\mu\)A. Consequently a higher transconductance value of 0.045S/mV was obtained for our simulated device compared to a lower transconductance value of 0.013S/mV. This can be explained by the ballistic transport model implemented in the NanowireMG simulator. The good agreement of our simulated results with the experimentally reported results gave us the confidence to proceed with our simulation study on InAs Nanowire FET.

The effects of scaling on InAs NWFET were then examined for change in channel length, channel diameter and gate oxide thickness. The sub-threshold slope, Drain Induced Barrier Lowering (DIBL), threshold voltage rolloff, ON-OFF currents and transconductance were studied for each case. The short channel effects were qualitatively and quantitatively discussed to explain the behavior of the device. Finally the Simulated InAs NWFET was compared with a simulated Si NWFET for varying channel length to further examine the effects of material properties on short channel effects. It was observed that an ideal sub-threshold slope of 60mV/dec and 61mV/dec were observed in Si NWFET and InAs NWFET, respectively, for a channel length of 50nm. However InAs consistently yielded higher values of sub-threshold slope with \(S = 102\)mV/dec at 20nm channel length in comparison to 73mV/dec for Si NWFET. Over all it was observed that InAs NWFET showed lesser immunity to
short channel effects, namely, sub-threshold slope degradation, Drain Induced Barrier Lowering and threshold voltage rolloff compared to the Si NWFET for exactly the same device structure and dimensions.

The current transport model used for simulations in the NanowireMG [2] simulator assumes a ballistic transport, i.e. carrier transport without any scattering in the channel. A more accurate transport model could be used bringing into account the surface scattering effects through methods such as the buttiker probes, which start to dominate at very small diameters (<5 nm). Another improvement that could be made to the simulator to provide a more realistic simulation would be to include the source-drain contact resistances. This would further enhance the accuracy of the transconductance values and ON currents due to its effects on the injection velocity of charge carriers from the source into the channel. Finally, the simulation software assumes an ideal wrap around gate for the nanowire FET. Since this ideal structure is not possible in practice, changes can be incorporated into the device structure to more faithfully reproduce the actual device structure.
Reference
