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Design of Current Sensors to measure small current signals of pico-amperes to nano-amperes in magnitude

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ABSTRACT

The primary goal of this research work is to amperometrically measure small current signals, in the range of pico-ampere to nano-ampere that are produced by electrolytic reactions of micro-electrode sensors. Two circuit designs viz. Type-I and Type-II have been described, which are capable of measuring such small current signals. Simulation results obtained from this thesis work predict the behavior of these circuits for three different technologies viz. AMI 1.5 micron, AMI 0.5 micron and TSMC 0.3 micron. These circuits were laid and fabricated through the MOSIS foundry service using the AMI 1.5 micron technology. The circuits were tested after fabrication and experimental results were reported illustrating the performance of these circuits in measuring small current signals. Type-I circuit was found to produce appreciable change in output voltage to detect currents of magnitude as low as 1nA. The sensitivity of the circuit for input currents varying from 1nA to 1uA was found to be reasonably high. The amperometric circuits described in this work occupy low area and also consume low power in the range of tens of milli-watts. The ability of these amperometric circuits to measure small signal currents coupled with low area and power consumption make them an integral part of any analog system with wide applications in medical and biological field as well as in optical sensor areas.
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1 INTRODUCTION

Measurement of toxicants or pollutants in water, bio-film and others is a vital study in environmental engineering as it serves as a direct indication of the amount of environmental pollution. Similarly, the dissolved in physiological and environmental systems is an indication of the physical, chemical and biochemical oxygen (DO) activity [1]. Continuous and more importantly in-situ monitoring of these toxicants, pollutants and DO have major applications in the medical science and environmental engineering [1]. Monitoring devices based on microelectrode sensors are presently leading the way in several research areas including: medical science, limnology, microbial ecology and environmental engineering. A system that includes these sensors along with some signal processing circuitry to output the concentration in a readable digital format is mandatory for in-situ measurements in many emerging applications. The development of enabling technology for such a system is the focus of this thesis.

1.1 PREVIOUS WORK IN CURRENT SENSOR DESIGN

The mandate provided by the low currents generated by the microelectrodes used for chemical, biological and optical measurements have triggered off a serious research in the area of designing circuits for precise measurements of these low currents.

Previously, a group under the direction of Dr. Beyette in the department of Electrical and Computer Engineering at the University of Cincinnati, worked on the first generation current sensors. They reported on the design, fabrication and testing of two amperometric circuits [2]. These circuits were designed to measure the currents generated by amperometric microelectrodes. Their Type I circuit was based on a fixed gain provided by the current mirror to
Figure 1-1: Type II Amperiometric circuit [2]

the input current, followed by a sample and hold circuit to produce a corresponding voltage level of the amplified current. The Type I circuit was found to be unsuitable during real time testing of the circuit owing to the limitations of the gain of the current mirror in different current ranges [2]. The Type II circuit is as shown in Figure 1-1.

As shown in the above Figure 1-1, the current from the reference electrode is fed to the input terminal of an opamp (Transimpedance amplifier). As the opamp has very high input impedance, the current is unable to enter it and hence follows the path through the resistor. This results in the development of a voltage \( V = iR \) at the output of the opamp (node 2). Hence, an I-V conversion is achieved. A differential instrumentation amplifier is used to further amplify the signal produced by the transimpedance amplifier. Finally, a unity gain inverting buffer is used to obtain desired output voltages polarity and insure sufficient electrical driving capability. Unfortunately, it was found that this circuit was not suitable for measuring currents in the range of nano-amperes and pico-amperes [2]. The gain provided by the transimpedance and transconductance amplifiers was limited and offset by the geometry of the transistors and the complexity of the circuit respectively.
Beyond the work of Dr. Beyette et al. there are a number of other methods that have been utilized to detect the signal from current based sensors. Charge accumulation is one of the pervasive methods employed for measurement of the input current [3]. This method relies on the fact that if the time of the charge accumulation is made variable then one can achieve a variable gain. This variable gain would allow appreciable output for different low values of input current [3]. However, it is to be noted that these circuits involve a linear capacitor and sometimes additional complex circuitry that make them less attractive.

Another frequently used approach involves converting the current to an appropriate voltage using the logarithmic behavior of a MOS transistor. If the current through a MOS channel and the gate to source voltage are allowed to vary with the input current then the drain to source voltage will be logarithmically proportional to the input current [4][5]. Unfortunately, these circuits generally suffer from low sensitivity.

1.2 PROBLEM STATEMENT

As shown in Figure 1-2 the microelectrode sensors developed and fabricated by the research team under the direction of Dr. Papautsky at the University of Cincinnati contain four different probes on a single wafer [6].

These probes are enveloped using different materials to measure different analyte concentrations in a solution. The basic principle of the microelectrode sensors is reduction oxidation (redox) reactions, which produce a current/voltage. This output current/voltage is proportional to the concentration of the pollutants or DO in the solution. In general, the operating current range of such microelectrodes is nano-amperes or pico-amperes.
As discussed earlier, the previous generation current sensor design failed to work properly in the desired operating range of nano-amperes to pico-amperes. This motivates a need for the design of a circuit that produces appreciable difference in output voltage for input currents in the pico-ampere and nano-ampere range. While the desired operating current range for the microelectrodes of interest varies from 1-10 nA [1], failed microelectrodes output current in the range of hundreds of nanoamperes to tens of microamperes. Hence the current sensor should be able to produce different voltage levels for a wide range of input current magnitudes. This defines the primary problem statement of this research.

It is also important to note that noise parameters due to the interface between the current sensors and microelectrodes are unknown. Hence, performance due to the interference of noise owing to the microelectrodes and the interface cannot be modeled for the current sensor designs are discussed. The ADC that shall follow the Type-I circuit is assumed to have a bit resolution of 10-bits. For a 5 volt range, this results in 1-bit change for every 5mV change in the input. So in a worst case scenario the current sensors should be able to convert every nano-ampere step change in the input to a 5mV variation in the output, resulting in a resolution of 5mV/nA.

Figure 1-2: MEMS sensors with four probes on a single wafer [6]
The present thesis work reports the design, test results and performance of current sensor that is part of a system that allows in-situ measurements of the solution being tested. The overall system is beyond the scope of this thesis work. However, it is beneficial to briefly discuss the overall system in order to appreciate certain changes that are made in the padframe and layout of the circuits.

The overall system aims at integrating the microelectrode sensors with the signal processing circuitry which shall allow in-situ measurements. The signal processing circuitry would be able to convert the sensed current/voltage generated by the microelectrode sensors to a digital output format using a microcontroller based hardware platform. Subsequently, a calibration between the concentrations of the solute in the solution and the digital output from the signal processing circuitry can be built.

The four probes of the microelectrode sensors are capable of measuring concentrations of four different entities in the solution (e.g. pH, dissolved oxygen (DO) etc.). Hence, the overall system shall have the capability to perform time multiplexing among the concentrations being measured by the four probes simultaneously.

The capability of the system to measure four different entities of the solution puts forth a secondary requirement on the current sensor design which is low area consumption. Compactness of design shall allow four replications of the design within a conventional padframe and for the targeted AMI 1.5 micron technology. These replications would provide the necessary resource to enable time multiplexing for the overall system.

The process of measuring current produced by an electrochemical reaction in general is termed as amperometry. The current sensor designed to measure these low magnitude currents could be
an integral part of any analog system. Other than having application in medical and biological fields they are also useful in areas of optical sensors to measure photo currents which range from pico-amperes to nano-amperes.

1.3 CHAPTER SUMMARIES

Following this introduction, Chapter 2 describes the principle and design of the current sensor developed for this thesis work. This chapter also discusses the simulation results obtained from the proposed circuits. The padframe and layout of the current sensor designs along with a discussion about the portability of design to different technologies is covered in Chapter 3. Chapter 4 presents the test set up and discusses the real time test results. Finally, Chapter 5 summarizes this thesis work and makes suggestion for future work.
2 CURRENT SENSOR DESIGN

Chapter 1 introduced the limitations of the work previously done in the area of low current signal detection. These limitations motivated the present thesis work for design of a current sensor for measuring currents in the range of nano-amperes and pico-amperes. The present chapter illustrates the principle, design and simulation results for the two current sensors designed in this thesis work. The two circuits presented here are referred to as the Type I and Type II circuits.

2.1 PRINCIPLE AND DESCRIPTION OF TYPE I CIRCUIT

The following schematic diagram Figure 2-1 illustrates the transistor level design of the Type I circuit which is an improvement on the principle of detecting weak input current signals using a current to voltage converter that has an adaptive gain described by Chunyan Wang [3]. The circuit works as a current to voltage converter and aims at an adaptive gain for the entire range of input currents. While high conversion gain makes the circuit highly sensitive to weak currents, it adaptively adjusts its conversion gain down for stronger input currents. The variable conversion gain is obtained by exploiting the non-linear features of MOS transistors.

2.1.1 CIRCUIT DESCRIPTION

The circuit as shown in Figure 2-1 consists of eight transistors. The PMOS transistors (M1, M2, M5 and M6) have identical width = 120 micron and length = 8 micron while all NMOS transistors (M3, M4, M7 and M8) have identical width = 40 micron and length = 8 micron as well.
The input current $I_{in}$ that is fed in at node 1 can either be a current source (into the circuit) or a current sink (out of the circuit) and hence can be positive or negative. When the input current is zero, the voltage at the three nodes 1, 2 and Out are equal, i.e. $V_1 = V_2 = V_{out}$, owing to the fact that the PMOS transistors and NMOS transistors are identical in the pull up network and pull
down network respectively. For the case in which the input current is not zero there is a corresponding voltage developed at Node 2, which we refer to as $V_{\text{change}}$. This change of voltage at Node 2 will cause the voltage at node 1 to be equal to the difference of $V_2$ and $V_{\text{change}}$ i.e. $V_1 = V_2 - V_{\text{change}}$, therefore bringing about a change in the currents $I_{\text{in1}}$ and $I_{\text{in2}}$. Consequently, the currents $I_{\text{out1}}$ and $I_{\text{out2}}$ flowing in the output branch will be altered, ultimately causing a change in the output voltage $V_{\text{out}}$. Hence, the output voltage will be modulated according to the input current based on an adaptive gain, which we will discuss shortly. First each of the various operating regions is discussed based on the magnitude/strength of the input current.

**REGION 1: Small input current**

When the input current is small, in the nano-amperes or pico-amperes range the voltage change $V_{\text{change}}$ at node 2 is small and typically not strong enough to disturb the original states of the transistors. Hence, the output transistors M5, M6, M7 and M8 stay in saturation. However, the input current that is injected at node 1 produces a change in the currents $I_{\text{in1}}$ and $I_{\text{in2}}$ as this is the only path that it can flow through. As the PMOS transistors (M1, M2, M5 and M6) and NMOS transistors (M3, M4, M7 and M8) are in current mirror configurations, the change in the branches $I_{\text{in1}}$ and $I_{\text{in2}}$ induced by the input current are reflected in the output branch currents $I_{\text{out1}}$ and $I_{\text{out2}}$, respectively. It should be noted that the difference of the output branch currents is equal to the magnitude of the input current ($I_{\text{out1}} - I_{\text{out2}} = I_{\text{in}}$). As the output current has no path to flow out, it causes a change in the drain to source voltages ($V_{ds}$) of the output transistors (M5, M6, M7 and M8). The drain to source resistance ($R_{ds}$) of the output transistors is finite and hence the output voltage $V_{\text{out}}$ is changed from $V_2$ to $V_2 - V_{\text{out,change}}$. The output voltage variation can be equated to the product of the input current and the drain to source resistances of the output transistors.
\[ V_{\text{out,change}} = I_{\text{in}} \times R_{\text{eq}} \]

where \( R_{\text{eq}} = R_{\text{dsp}} \parallel R_{\text{dsn}} \) and \( R_{\text{dsp}} \) and \( R_{\text{dsn}} \) are the drain to source resistance of the PMOS transistors and NMOS transistors respectively.

As the output transistors are in saturation their drain to source resistance is large in magnitude ranging from tens to hundreds of Mega ohms. As a result the value of \( V_{\text{out,change}} \) for different input currents in this range will be appreciable enough to be discerned as different voltage levels by an analog to digital converter. Thus, we see that a current of small magnitude is converted to a voltage with a very high gain factor. It is also noted that the behavior of this circuit is quite linear for small input currents.

The following simulation result Figure 2-2 illustrates the HSPICE simulations of the Type-I circuit for small input currents.

The resolution obtained for this input current range was 200 mV/nA. An interesting property of the circuit is the cascode transistors (M1, M4, M5 and M8) which provide higher gain and hence greater difference in output voltage for various current levels over the entire range of interest. In the absence of the cascode transistors the source to drain resistance of the output transistors would be \( r_0 \), which is the saturation resistance of a MOS transistor. The presence of the cascode transistors allows the output resistance to be \( r_0^2 \) and hence provide a greater variation in the output voltage for corresponding levels of input current. However, cascading comes at the cost of an additional voltage drop of \( V_{\text{dsat}} \) for the output voltage. Ultimately, this reduces the dynamic range of the output voltage.
Figure 2-2: Simulation results illustrating the variation of output voltage with input current for current ranging from 0 to 1 nA. The output voltage varies from 2.05V to 1.87V.

Triple cascoding is not employed due to the subsequent loss of output dynamic range with each increasing stages of cascode.

REGION 2: Strong input current

The earlier discussion gives a good understanding of the basic principle on which the circuit is based. The behavior of the output transistors in different regions of operation (saturation or linear) governs the gain and voltage variation that is observed for various values of input current. Now let us analyze the behavior of the circuit for strong input currents. By strong input currents we mean currents in the range of hundreds of nano-amperes to microamperes.
If the input current is strong, the voltage variation at node 2, \( V_{\text{change}} \) will be greater. This variation is typically strong enough to disturb the states of the output transistors. If the current is positive the PMOS transistors (M5 and M6) will be operating in the linear region while the NMOS transistors (M7 and M8) remain in saturation.

Alternately, if the current is negative NMOS transistors will be in linear region of operation while the PMOS transistors remain in saturation. As explained earlier the difference of currents in the two output branches would be equal to the input current and the output voltage variation \( V_{\text{out,change}} \) is the product of the input current and the output resistance. The transistors of one of the output branches being in linear region of operation will exhibit much lesser output resistance than a transistor in saturation region. Thus, as we had seen earlier the output resistance is the parallel combination of the two branches, which results in a lower resistance value than the case in which both the output branches are in saturation. Ultimately this results in lower output
voltage variation. If we compare the case of a small input current to the case of a strong input current we find that the conversion gain is much less in the strong current case.

The HSPICE simulation shown in Figure 2-3 concurs with the theoretical explanation given above for this region of operation.

For current ranges in the medium range, tens of nano-amperes, the transistors make a transition between the saturation and linear mode. Hence the variation $\frac{dv_{ds}}{di_{ds}}$ is a continuous function of $v_{ds}$ and the gain is a continuous function of the input current $I_{in}$.

The HSPICE simulation (Figure 2-4) illustrates the output voltage as a function of the input current for these medium range values.

![Figure 2-4: Simulation results illustrating the variation of output voltage against input current for current ranging from 10 to 100 nA. The output voltage varies from 1.31V to 950mV](image-url)
Figure 2-5: Simulation results illustrating the variation of output voltage against input current for current ranging from 1nA to 10 nA. The output voltage varies from 1.87V to 1.31V.

It is also interesting to observe the simulation results for the Type I circuit in desired range of operation (1nA – 10nA) for the microelectrode sensors as shown by the HSpice simulation in Figure 2-5. The Type-I circuit has a resolution of 65mV/nA in this region of input current which surpasses the worst case scenario by a factor greater than 10. This head room is sufficient to accommodate noise issues that may originate due to the current sensors or the overall system which is unknown during this thesis work.

The following Hspice simulation Figure 2-6 result summarizes the behavior of the Type I circuit over all regions of operation by sweeping the input current from 0 to 1 micro amperes.
The Type I circuit utilizes an operational amplifier [7] used in the source follower configuration. The operational amplifier in this configuration serves as an output buffer. If the output node, is taken directly to the bonding pad of the pad frame, the output signal would be susceptible to noise generated by the measuring instruments like multi-meters, oscilloscopes etc. and the cabling used to connect them to the chip under test. An output buffer shields this susceptible node by providing signal isolation and impedance matching.

2.2 PRINCIPLE AND DESCRIPTION OF TYPE II CIRCUIT

The Type II circuit is based on the principle of converting the input current signal to time that was highlighted by Narula and Harris [8]. Unlike the Type I circuit, the Type II circuit is not
Figure 2-7: Schematic symbol of a current conveyor

based on amplifying the input current to appropriate voltage levels. Instead it aims at converting the various strengths of input current into the time domain, thereby eliminating matching problems and increasing the dynamic range. Prior to explaining the working of the Type II circuit let us first take a moment to understand the principle of a current conveyor. Figure 2-7 shows a schematic symbol of a current conveyor.

If a voltage $V_y$ is applied on the terminal $Y$ of the current conveyor, then an equal voltage appears at terminal $X$ independent of the current supplied to $X$. The circuit has the behavior of a virtual short circuit at $X$. Another important aspect is that the current flowing through terminal $Y$ is equal to the current supplied to $X$ independent of the voltage $V_y$. Hence, there exists a virtual open circuit at the terminal $Y$. Also, the current supplied to the terminal $X$ is conveyed to the output terminal $Z$. [9].

An ideal current conveyor can be built by placing a MOS transistor in the negative feedback loop of an op amp. A schematic diagram of this is shown in Figure 2-8. In the figure, the PMOS transistor following the op amp in the negative loop is referred to as the super transistor, which allows the current to be restricted to flow into the terminal $X$. As explained previously, the current forced into the terminal $X$ shall be conveyed to the terminal $Z$. Also, a reference voltage can be applied to the terminal $Y$ and this shall not affect the current forced into $X$. 
DESCRIPTION OF THE CIRCUIT

The following Figure 2-9 shows the schematic of Type II circuit using Cadence Virtuoso while Table 2-1 summarizes the sizes of the transistors used in the design.

The reference voltage for the electrochemical reaction of the microelectrodes is applied at the terminal Y and the current produced by the reduction/oxidation reaction is supplied to the terminal X. The op amp [7] followed by the PMOS, as explained above acts as a current conveyor and an equal current is observed at the terminal Z ($I_z = I_x$).

The capacitor C shown in the diagram is charged in accordance with the current flowing through the terminal Z, which in turn is equal to the input current. The Schmitt trigger, following the
capacitor restricts the range of the voltages to which the capacitor is charged/discharged. This range in other words is the difference between the Upper threshold point (UTP) and Lower threshold points (LTP) voltages of the Schmitt trigger. We shall shortly, discuss the design of the Schmitt trigger.

The capacitor C is initially discharged through the NMOS transistor M3 by the application of an external reset pulse at the pin named RESET. This external pulse is applied only initially to make sure that the capacitor C is completely discharged prior to the circuit behaving in its expected fashion. Thereafter, the capacitor is charged to the UTP of the Schmitt trigger in accordance with the magnitude of the input current I, produced by the redox reactions. The time taken by the capacitor to charge up is given by the equation:

\[ T = \frac{C \cdot V_{\text{diff}}}{I} \]  \hspace{1cm} (2.1)

Where T is the time taken by the capacitor to charge up,

\begin{table}[h]
\centering
\begin{tabular}{|c|c|c|}
\hline
\textbf{Transistor} & \textbf{Width (in microns)} & \textbf{Length (in microns)} \\
\hline
M1 & 1.8 & 41.6 \\
\hline
M2 & 1.6 & 128 \\
\hline
M3 & 4.8 & 1.6 \\
\hline
M4 & 4.8 & 1.6 \\
\hline
M5 & 14.4 & 1.6 \\
\hline
\end{tabular}
\caption{Width and length of the transistors used in Type II circuit}
\end{table}
$V_{\text{diff}}$ is the voltage difference between the UTP and LTP of the Schmitt trigger and $I$ is the input current.

Upon reaching the UTP of the Schmitt trigger, a reset pulse is generated which turns on the NMOS (M2). Once again the capacitor starts discharging through the transistor M2, till the LTP of Schmitt trigger. As the voltage on the capacitor reaches the LTP of the Schmitt trigger, the reset pulse goes low which turns off the discharge path for the capacitor. The capacitor starts charging up again through the PMOS transistor M1, and the time taken to charge up to the UTP is in accordance with the equation 2.1. The reset pulse generated by the circuit is obtained by feeding the Schmitt trigger output to an inverter which controls the gate of the NMOS transistor M2. The inverter provides the phase inversion and some time delay as well which aids in overcoming any race condition.

The key parameter here is the time taken for the capacitor to charge up to the UTP. As we have seen this epoch depends on the strength of the input current. Hence, as we vary the input current ($I$), the time

![Figure 2-9: Schematics of the Type II circuit](image-url)
taken to charge the capacitor (T) will vary. According to the proportionality between the two parameters, it is easy to understand that a weaker signal will take more time to charge up the capacitor as compared to a stronger signal. This also gives the advantage of a greater dynamic range, as the input current is directly converted to time. The value of the capacitor C was chosen to be 1 pF. A larger capacitor would aid in reducing the noise, however it would also slow down the overall system as shown by the equation 2.1.
As governed by the equation 2.1, in the small input current range (10pA – 1nA) the time taken to charge up capacitor is the longest compared to the medium input current range (1nA – 100nA) and strong input current range (100nA – 1uA). This result is supported by Figure 2-10 through Figure 2-12 which show the response to various small, medium and strong current inputs.
Figure 2-10 shows the simulation result for a small input current of 10pA. The time taken to charge up the capacitor between the UTP and LTP of the Schmitt trigger was 0.234 seconds.

Figure 2-11 simulates the Type-II design for a small input current of 500pA.

Figure 2-11 illustrates the response of the circuit for a small-medium input current of 1nA.

In Figure 2-13 the input current is increased to 100nA and it is observed that the time taken to charge the capacitor is in the micro-seconds range.

Figure 2-11: HSpice simulation result for a weak-medium input current of 1nA takes 2.30 milli seconds to charge up the capacitor between the UTP and LTP of the Schmitt trigger
Figure 2-12: HSpice simulation result for a medium input current of 100nA takes $2.29 \times 10^{-5}$ seconds to charge up the capacitor between the UTP and LTP of the Schmitt trigger.

Increasing the current further to 500nA leads to lesser time taken for the charging of the capacitor and was observed to be 4.67 micro-seconds as shown in Figure 2-12.

Conforming to the equation 2.1, the simulation results indicate that for small input currents the time taken for the capacitor to charge up is in the range of hundreds of milli-seconds to seconds. In contrast, for strong input currents, the charging time is in the range of tens of milliseconds to microseconds for stronger input currents.

Figure 2-14 shows the behavior of the circuit over the desired input current range from 1nA to 10nA.

**SCHMITT TRIGGER DESIGN AND APPLICATION**

Schmitt trigger is a well-known circuit that is widely used for its unique hysteresis property. The prime application of a Schmitt trigger is generating clean pulses from a noisy input signal.
The circuit shows two steep transitions at $V_{U TP}$ and $V_{L TP}$ in opposite directions. At $V_{L TP}$ the transition is from high to low while at $V_{U TP}$ the transition is from low to high. We use this to our advantage in two cases. Firstly, we use the UTP and LTP voltages to define the voltages to which the capacitor $C$ should charge and discharge to respectively. This helps in keeping the
simulation and real time testing times under constraint as a complete charge up of the capacitor from ground to Vdd would take time in the range of tens to hundreds of seconds for small input currents. This might prove prohibitive in terms of measurements and simulation time. Secondly, the two steep transitions at different voltages are used to produce the reset pulse for the NMOS (M2) and hence the discharge path for the capacitor. When the capacitor is charged up to the UTP, the Schmitt trigger’s output goes from low to high. As the Schmitt trigger’s output is fed to the gate of the N1 transistor, it turns it on. The capacitor finds a discharge path and discharges through the transistor N1. This discharge time is much faster than the charge up time as it does not have any dependence on the input current. Once, the capacitor is discharged to the LTP, the Schmitt trigger’s output makes a transition from high to low. As a result the transistor N1 is turned off, and the discharge path to the capacitor is cut-off. Once again the charge up of the capacitor resumes until it is charged up to the UTP, where the cycle repeats itself as shown in the simulation results.

There are various ways of designing a Schmitt trigger. The one adopted in this design is based on the principle explained by Baker, Li and Boyce [10]. Figure 2-15 depicts the transistor level diagram of the Schmitt trigger.

Let us look into the working of this circuit. If we assume that initially that the output is high, and the input is low. Transistors M1, M2 and M3 aid in defining the UTP of the Schmitt trigger, while M4, M5 and M6 define the LTP. As the input V_{in} is low, the transistors M1 and M2 are off while M3 is on. The source for M3 is held at V_{x}, which is an intermediate voltage. Now as V_{in} is increased the transistors M1 and M2 start to turn on and the intermediate voltage V_{x} starts to decrease towards ground. The UTP is defined when:
\[ V_{in} = V_{UTP} = V_{thn2} + V_x. \]

As M2 starts to turn on, the output voltage \( V_{out} \) starts decrease towards ground. As the source of M2 and M3 are tied they experience the same body effect. This transition continues until M1 and M2 are completely turned on and M3 is turned off. This transition is shown to be steep in the following simulation results. To determine the UTP voltage we can equate the currents flowing through M1 and M3 as follows:

Solving equations 2 and 3 we get

\[ \frac{\beta_1}{2} (V_{UTP} - V_{THN})^2 = \frac{\beta_3}{2} (V_{dd} - V_X - V_{THN3}) \] …………………..(2.2)

which when rearranged can be written as

\[ \beta_1/\beta_3 = \left[ (V_{dd} - V_{UTP})/(V_{SPH} - V_{THN}) \right]^2 \] …………………..(2.3)
A similar analysis can be applied to define the LTP of the Schmitt trigger. We will come to the following equation to define the LTP:

\[ \frac{\beta_5}{\beta_6} = \frac{[V_{LTP}/V_{dd} - V_{LTP} - V_{THP}]}{\sqrt{2}} \]  

where \( \beta_1, \beta_3, \beta_5 \) and \( \beta_6 \) are the transconductances of the transistors M1, M3, M5 and M6

\( V_{UTP} \) is the upper threshold point voltage,

\( V_{LTP} \) is the lower threshold point voltage,

and \( V_{THN} \) and \( V_{THP} \) are the threshold voltages for the NMOS and PMOS respectively

Governed by the above equations we can derive the widths and lengths of the transistors that comprise the Schmitt trigger circuit.

The width and length of the transistors, for the present Schmitt trigger design is listed in Table 2-2

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Length (in microns)</th>
<th>Width (in microns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>3.2</td>
<td>4.8</td>
</tr>
<tr>
<td>M2</td>
<td>9.6</td>
<td>4.8</td>
</tr>
<tr>
<td>M3</td>
<td>38.4</td>
<td>4.8</td>
</tr>
<tr>
<td>M4</td>
<td>44</td>
<td>4.8</td>
</tr>
<tr>
<td>M5</td>
<td>8.8</td>
<td>4.8</td>
</tr>
<tr>
<td>M6</td>
<td>3.2</td>
<td>4.8</td>
</tr>
</tbody>
</table>
Table 2-2: Length and Width of the transistors used in the Schmitt trigger

Detailed analysis of the Schmitt trigger in various transition regions and alternate designs are explained by Filanovsky and Baltes [11].
3 LAYOUT AND PORTABILITY OF DESIGN TO SUB-MICRON TECHNOLOGIES

Previous chapter explained the Type I and Type II designs for the current sensor and also illustrated the behavior and performance of the designs through HSPICE simulations. In this chapter, the layout styles for the Type I and Type II designs is presented and the portability of the two designs to two different sub-micron technologies is illustrated.

3.1 PADFRAME

A conventional 40 pin padframe (Tiny Padframe [12]) consists of power pads and I/O pads. The Tiny Padframe by MOSIS has two power pads, 34 I/O pads which are designed for analog applications and four corner pads which supply $V_{dd}$ and $V_{ss}$ to the I/O pads. The total pin count for the padframe is 40. The padframe used in this work was altered to satisfy certain requirements of the overall system as explained in Chapter 1. The overall system design was expected to have the provision of both amperometric and potentiometric [7] measurements. To satisfy this requirement the padframe contains the potentiometric circuits [7] in addition to the Type I and Type II amperometric circuits explained in the previous chapter. The potentiometric circuits require 2.5V, -2.5V and 0V as the power supplies for their operation, while the Type I and Type II amperometric circuits operate on 5V and 0V as their power supplies. To accommodate all these power supplies on a single padframe two additional power pads (P2 and P4) were added on the Tiny Padframe by replacing the analog I/O pads. Figure 3-1 shows the conventional Tiny Padframe while Figure 3-2 shows the padframe used in the work presented.
here. The power pads are placed symmetrically and evenly on the padframe to minimize any power distribution problems.

**Figure 3-1:** Magic layout of a conventional Tiny Padframe

**Figure 3-2:** Altered padframe with extra power pads P2 and P4. Corner pads have also been swapped.
A schematic of an analog I/O pad is as shown in the Figure 3-3. The Electrostatic discharge (ESD) protection diodes are present to prevent any ESD hazard, as the gate voltage of a transistor is sensitive and can be permanently damaged by high voltage. Hence these diodes are of prime importance in Input pads as the gate of the transistor is connected to the outside of the chip. D1 and D2 are referenced to the V_{dd} and V_{ss} supplies respectively. The resistor shown in the figure is laid out using p/n diffusion layer and serves to limit current caused by voltage spikes.

During normal operation the diodes D1 and D2 are reverse biased and do not play any active role. However, in the case when a voltage higher than the Vdd value is applied to the node In the diode 1 gets forward biased and hence clamps the node Int to Vdd, thereby, preventing any surge (ESD hazard) in the positive direction to harm the circuitry inside. A similar analysis can be applied to the diode D2 which prevents any surge in the negative direction to propagate to the internal circuitry by clamping the Int node to Vss. To make sure that the ESD diodes of the analog I/O pads of the amperometric circuits and potentiometric circuits were tied to their respective supply voltages, the padframe was divided into upper and lower half. The corner pads
Figure 3-4: Disconnect between the upper and lower half emphasized

(C1, C2, C3 and C4) were swapped to make sure that each half had a positive and negative corner pad. Figure 3-2 illustrates this alteration when compared to the conventional padframe shown in Figure 3-1. The supply rings that run around the periphery of the padframe and connects each pad to the positive and negative corner pad was carefully disconnected at the points which demarcate the upper half from the lower half so that no short circuit exists between the power supplies of the two halves. Figure 3-4 emphasizes the disconnection in red. A similar disconnect can be found on the opposite side of the padframe. This makes sure that the upper and lower half are disconnected from each other and the potentiometric and amperometric circuits operate on their respective power supplies without any interference.

This concept can be extended to constructing padframes that require different power pads for digital and analog circuitry in the same padframe. The isolation of the two halves from each other would ensure that the analog and digital circuitry do not interfere with each other.

3.2 LAYOUT OF TYPE I AND TYPE II CIRCUITS

The layout of Type-I and Type-II circuits has been performed using Magic 7.0. The layouts of the two circuits follow good practice guidelines for analog circuit layout/design. A short discussion of some of the analog design techniques follows.
Multi-fingered transistors

Analog designs often necessitate the use of wide transistors. One of the conventional techniques to reduce the source drain area and the gate resistance is to fold the transistor. However, often a simple folded structure proves to be inadequate for very wide devices. Another technique which can overcome the shortcoming of folded structure is to layout the wide transistor with multiple fingers. There exists a tradeoff between the gate resistance and the capacitance associated with the perimeter of the source/drain area while choosing the number of fingers that the transistor should be divided into. If more parallel fingers are used for the transistor the gate resistance can be reduced. This would however, result in an increase in the source/drain area capacitance. Therefore, as a rule of thumb the width of each finger is selected such that the resistance of the finger is less than the inverse transconductance associated with the finger. A lower gate resistance is desired in low noise applications.

Multi-finger transistors can be laid out using an alternate technique in the case when a transistor (M1) and its associated cascode transistor (M2) having the same size. This case is observed in Type I circuits where the PMOS and NMOS transistors and their respective cascode transistors have the same size. The drain of transistor M1 can share the same junction as the source of transistor M2. This layout technique often proves to be more compact. Further this layout technique also reduces the capacitance of the drain of M1 substantially, hence improving the high frequency performance of the cascade pair.

A detailed description of this analog layout technique can be found in “Design of Analog CMOS circuits”, by Behzad Razavi [13].
Length of the transistors

Due to the dependence of various secondary effects like channel length and mobility modulation on the length of the transistors, transistor length is of prime importance in analog design. Of particular interest is the channel length modulation factor ($\lambda$) which is proportional to $1/L$, where $L$ is the length of the transistor. Greater channel length also results in higher gain as gain is dependent more strongly (inversely) on $\lambda$ than the transconductance of the transistor [8]. Flicker noise and mismatches are also inversely proportional to the length of the transistor. Hence, a greater length of the transistor results in reducing the undesired effects of transistor mismatches and noise in the circuitry. A general rule of thumb in analog design is to have the length of the MOSFET to be two to five times the minimum length allowed by the technology. Type I circuit maintains the length of the transistors in accordance with the thumb rule mentioned above while Type-II circuit emphasizes on using greater channel lengths to reduce various components of noise.

Well contacts

One of the undesired phenomenon observable in CMOS circuits is latch up. As shown in Figure 3-5 the parasitic bipolar transistors formed by the well and substrate gives rise to this effect. [14]

The latch up process is based on positive feedback resulting as the base of each bipolar transistor being driven by the collector of the other. With only a small signal induced on to either base (through either well or substrate resistances), the positive feedback can be catastrophic to the normal operation of the circuit.
A VLSI designer can take precautions during the layout of analog circuits to minimize the chances for a latch up to occur. One of the design techniques to curtail CMOS latch up is to decrease the well ($R_{well}$) and substrate ($R_{sub}$) resistances. This can be achieved by having

**Figure 3-5**: Schematic diagram illustrating CMOS latch up

**Figure 3-5**: Magic layout of Type I circuit
numerous small well and substrate contacts which aid in reducing the resistance. Both Type-I and Type-II circuits follow this design technique as illustrated in their layouts.

3.2.1 TYPE-I CIRCUIT

The Type-I circuit was laid out keeping in mind the analog design techniques discussed above. Figure 3-5 shows the Magic layout of the Type-I circuit. The PMOS transistors have four fingers with each finger having a width of 20 lambda and length of 6 lambda. The NMOS transistors have two fingers with each finger having a width of 10 lambda and length of 6 lambda. Lambda for the AMI 1.5 technology is 0.8 microns. An alternate method for laying out the transistors is to use the folded cascode formation discussed above. A version of the Type-I circuit laid out in a folded cascode fashion is shown in Figure 3-6. Unfortunately, the simulation of the Hspice file extracted from this layout did not produce the desired simulation results. On the other hand, simulation results for the layout shown in Figure 3-5 closely matched with the simulation results.

Figure 3-6: Folded cascode layout of Type I circuit
Figure 3-7: Padframe with four replications of the Type I circuit results obtained from simulating the HSpice file extracted from the schematics of the Type I circuit.

As discussed in Chapter 1, the microelectrode sensors are capable of making four different measurements as each probe can be enveloped by a different membrane. In order to make the overall system capable of multiplexing among the four probes the Type-I circuit has been replicated four times inside the padframe as shown in Figure 3-7. The Type-I circuit occupied an area of 106833 \( \lambda^2 \) where \( \lambda = 0.8 \) micron for the AMI 1.5 micron technology. Hspice simulation results of Type-I circuits showed the average power consumption to be 6.698 mW.

3.2.2 TYPE-II CIRCUIT

The Type-II circuit has been laid out keeping in mind the analog design techniques discussed above. Unlike the transistors in Type-I circuit, the transistors in Type-II circuit have greater length than width. This aids in further reducing various components of noise like flicker noise. The Schmitt trigger contains multi-fingered NMOS and PMOS transistors as well. The Magic layout of the Type-II circuit is shown in Figure 3-8. The Type-II circuit occupied an area of 112500 \( \lambda^2 \) where \( \lambda = 0.8 \) micron for the AMI 1.5 micron technology.
3.3 PORTABILITY TO AMI 0.5 TECHNOLOGY

This section illustrates the portability of the Type-I and Type-II designs to AMI 0.5 technology and the behavior of the circuits in AMI 0.5 technology. The motive behind this study is to observe the deviations in the behavior of the circuits in a different technology. This also serves in simulating the designs for some corner cases.

3.3.1 TYPE-I CIRCUIT

The Type-I circuit was simulated with the model parameters for the AMI 0.5 technology [12] using HSpice. The simulation results for the same range of input current as the simulations presented in Chapter 2 are illustrated below. This enables a comparison between the behaviors of the circuit in the two technologies.
Figure 3-10: Hspice simulation of Type I circuit in AMI 0.5 technology for input current ranging from 0 to 1 nA. The output voltage swings from 2.06V to 1.83V.

Figure 3-10 through Figure 3-11 illustrate the behavior of the Type-I circuit when simulated using the AMI 0.5 micron technology.

Figure 3-11: Hspice simulation of Type I circuit in AMI 0.5 technology for input current ranging from 100nA to 1 uA. The output voltage swings from 0.97V to 0.421V
Figure 3-9: Hspice simulation of Type I circuit in AMI 0.5 technology for input current ranging from 10nA to 100 nA. The output voltage swings from 1.26V to 0.97V.

Figure 3-10 illustrates the simulation of Type-I circuit using the AMI 0.5 micron technology for an input current ranging from 0 to 1nA. The behavior of the output voltage for this input current range is found to be quite linear.

A non-linear behavior of the output voltage commences when the applied input current is increase to tens of nano-amperes to micro-amperes. Figure 3-11 and Figure 3-9 illustrate this behavior of the Type-I circuit.

Figure 3-10 illustrates the behavior of the Type-I circuit for the desired range of input current ranging from 1nA-10nA using the AMI 0.5 micron technology. The dynamic range of output voltage over this input current range was found to vary from 1.83V to 1.26V.
Figure 3-10: Hspice simulation of Type I circuit in AMI 0.5 technology for input current ranging from 1nA to 10 nA. The output voltage swings from 1.83V to 1.26V.

Finally, Figure 3-11 illustrates the behavior of the Type-I circuit over the entire input current range from 0 to 1 micro-amperes.

Figure 3-11: Hspice simulation of Type I circuit in AMI 0.5 technology for input current ranging from 0 to 1 uA. The output voltage swings from 2.06V to 0.421V.
Figure 3-12: HSpice simulation of Type II circuit in AMI 0.5 technology. For a small input current of 10pA it takes 0.374 seconds to charge up the capacitor between the UTP and LTP of the Schmitt trigger.

1.1.1 TYPE-II CIRCUIT

The Type-II circuit was simulated with the model parameters for the AMI 0.5 technology [12] using HSpice. The simulation results for the same range of input current as the simulations

Figure 3-13: HSpice simulation of Type II circuit in AMI 0.5 technology. For a weak input current of 500pA it takes 7.82 milli-seconds to charge up the capacitor between the UTP and LTP of the Schmitt trigger.
Figure 3-14: HSpice simulation of Type II circuit in AMI 0.5 technology. For a weak-medium input current of 1nA it takes 3.93 milli-seconds to charge up the capacitor between the UTP and LTP of the Schmitt trigger presented in Chapter 2 are illustrated below. This enables a comparison between the behaviors of the circuit in the two technologies.

Figure 3-12 illustrates the transient response of Type-II circuit for a small input current of 10pA using the AMI 0.5 micron technology. It takes 0.374 seconds to charge the output capacitor between the UTP and LTP defined by the Schmitt trigger. An increase in the input current magnitude to 500pA causes the charging time for the output capacitor to reduce to 7.82 milli-seconds. This is illustrated in Figure 3-13.

Figure 3-14 illustrates the simulation result of Type-II circuit using the AMI 0.5 micron technology for an input current of 1nA. The time taken to charge the output capacitor was observed to be 3.93 milli-seconds.

Further increase in the magnitude of the input current causes the output capacitor charging time to reduce further, as the signal is now in the medium-strong region. As shown in Figure 3-15, the
Figure 3-15: HSpice simulation of Type II circuit in AMI 0.5 technology. For a medium input current of 100nA it takes 38.9 micro-seconds to charge up the capacitor between the UTP and LTP of the Schmitt trigger. The time taken to charge the output capacitor was 38.9 micro-seconds for a medium-strong input current.

Figure 3-16 illustrates the transient response of the Type-II circuit for a strong input current of...
Figure 3-17: HSpice simulation of Type II circuit in AMI 0.5 micron technology over the desired range of operation from 1-10nA

magnitude 500nA. The time taken to charge the output capacitor was observed to be 7.93 microseconds.

Finally, Figure 3-17 illustrates the time response for charging the output capacitor for an input current range varying over the desired current range varying from 1nA to 10nA.

3.4 PORTABILITY TO TSMC 0.3 MICRON TECHNOLOGY

This section discusses the portability of the Type-I and Type-II designs to TSMC 0.3 micron technology and illustrates the behavior of the circuits in TSMC 0.3 micron technology. The motive behind this study is to observe the deviations in the behavior of the circuits in a different technology. This also serves in simulating the designs for some corner cases.
Figure 3-18: Hspice simulation of Type I circuit in TSMC 0.3 micron technology for input current ranging from 0 to 1 nA. The output voltage swings from 2.245V to 2.19V

3.4.1 TYPE-I CIRCUIT

The Type-I circuit was simulated with the model parameters for the TSMC 0.3 micron technology [12] using HSpice. The simulation results for the same range of input current as the simulations presented in Chapter 2 are illustrated below. This enables a comparison between the behaviors of the circuit in the two technologies.

Figure 3-18 through Figure 3-20 illustrate the behavior of the Type-I circuit when simulated using the TSMC 0.3 micron technology.

Figure 3-18 illustrates the simulation of Type-I circuit using the AMI 0.5 micron technology for an input current ranging from 0 to 1nA. The behavior of the output voltage for this input current range is found to be quite linear.

A non-linear behavior of the output voltage commences when the applied input current is increase to tens of nano-amperes to micro-amperes. Figure 3-19 and Figure 3-23 illustrate this behavior of the Type-I circuit.
Figure 3-19: Hspice simulation of Type I circuit in TSMC 0.3 micron technology for input current ranging from 10nA to 100nA. The output voltage swings from 1.81V to 1.43V.

Figure 3-23: Hspice simulation of Type I circuit in TSMC 0.3 micron technology for input current ranging from 100nA to 1000nA. The output voltage swings from 1.43V to 0.937V.

Figure 3-24 illustrates the behavior of the Type-I circuit for the desired range of input current ranging from 1nA-10nA using the TSMC 0.3 micron technology. The dynamic range of output voltage over this input current range was found to vary from 2.19V to 1.81V.
Figure 3-24: Hspice simulation of Type I circuit in TSMC 0.3 micron technology for input current ranging from 1nA to 10 nA. The output voltage swings from 2.19V to 1.81V.

Finally, Figure 3-20 illustrates the behavior of the Type-I circuit over the entire input current range from 0 to 1 micro-amperes.

Figure 3-20: Hspice simulation of Type I circuit in TSMC 0.3 micron technology for input current ranging from 0 to 1 uA. The output voltage swings from 2.24V to 0.937V.
3.4.2 TYPE-II CIRCUIT

The Type-II circuit was simulated with the model parameters for the TSMC 0.3 micron technology [MOSIS] using HSpice. The simulation results for the same range of input current as
Figure 3-21: HSpice simulation of Type II circuit in TSMC 0.3 micron technology. For a weak-medium input current of 1nA it takes 5.46 milli-seconds to charge up the capacitor between the UTP and LTP of the Schmitt trigger. The simulations presented in Chapter 2 are illustrated below. This enables a comparison between the behaviors of the circuit in the two technologies.

Figure 3-26 illustrates the transient response of Type-II circuit for a small input current of 10pA using the AMI 0.5 micron technology. It takes 0.509 seconds to charge the output capacitor between the UTP and LTP defined by the Schmitt trigger. An increase in the input current magnitude to 500pA causes the charging time for the output capacitor to reduce to 0.109 milli-seconds. This is illustrated in Figure 3-27.

Figure 3-21 illustrates the simulation result of Type-II circuit using the AMI 0.5 micron technology for an input current of 1nA. The time taken to charge the output capacitor was observed to be 5.46 milli-seconds.
Further increase in the magnitude of the input current causes the output capacitor charging time to reduce further, as the signal is now in the medium-strong region. As shown in Figure 3-29, the

Figure 3-29: HSpice simulation of Type II circuit in TSMC 0.3 micron technology. For a medium input current of 100nA it takes 55.5 micro-seconds to charge up the capacitor between the UTP and LTP of the Schmitt trigger.

Figure 3-30: HSpice simulation of Type II circuit in TSMC 0.3 micron technology. For a strong input current of 500nA it takes 11.3 micro-seconds to charge up the capacitor between the UTP and LTP of the Schmitt trigger.
Figure 3-22: HSpice simulation of Type II circuit in TSMC 0.3 micron technology over the desired range of operation from 1-10nA. The time taken to charge the output capacitor was 55.3 micro-seconds for a medium-strong input current.

Figure 3-30 illustrates the transient response of the Type-II circuit for a strong input current of magnitude 500nA. The time taken to charge the output capacitor was observed to be 11.3 micro-seconds.

Finally, Figure 3-22 illustrates the time response for charging the output capacitor for an input current range varying over the desired current range varying from 1nA to 10nA.
### 3.5 PERFORMANCE COMPARISON

#### Table 3-1

<table>
<thead>
<tr>
<th>Input current range</th>
<th>Output voltage swing (in volts)</th>
<th>Output voltage swing (in volts)</th>
<th>Output voltage swing (in volts)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>AMI 1.5</td>
<td>AMI 0.5</td>
<td>TSMC 0.3</td>
</tr>
<tr>
<td>0 - 1nA</td>
<td>0.18</td>
<td>0.227</td>
<td>51.5 mV</td>
</tr>
<tr>
<td>1nA − 10nA</td>
<td>0.56</td>
<td>0.565</td>
<td>0.378</td>
</tr>
<tr>
<td>10nA − 100nA</td>
<td>0.36</td>
<td>0.294</td>
<td>0.495</td>
</tr>
<tr>
<td>100nA − 1uA</td>
<td>0.47</td>
<td>0.549</td>
<td>0.363</td>
</tr>
<tr>
<td>0 − 1uA</td>
<td>1.57</td>
<td>1.63</td>
<td>0.937</td>
</tr>
</tbody>
</table>

Table 3-1 summarizes the output voltage swing of Type I circuit over the various input current range. It also draws a comparison among the performance of the Type-I circuit for the three technologies. It can be inferred from Table 3-1 that the performance of Type-I circuit is similar in AMI 1.5 micron and AMI 0.5 micron technology. However, porting of this design to TSMC 0.3 micron technology does not produce any enhancement in performance. Moreover, the performance of Type-I circuit, in terms of output voltage swing for various input current ranges is worsened when using TSMC 0.3 micron technology.
Figure 3-23 illustrates the behavior of the Type II circuit over the desired range of input current (1nA-10nA). It also draws a comparison among the performance of the Type-II circuit for the three technologies. Simulation results of the Type-II circuits in the three technologies illustrate that the charging time for the output capacitance with varying input current is lowest for AMI 1.5 micron technology, followed by AMI 0.5 micron and TSMC 0.3 in that order. Hence, porting of this design to smaller technology does not provide any benefit. Rather, the increase in charging time for the output capacitor puts further limitation on the simulation times for the circuit.

Table 3-1: Table illustrating the output voltage swing of Type-I circuit for various input current ranges over the three technologies

Figure 3-23: Chart illustrating the performance of Type-II circuit over an input current range of 1nA-10nA over the three technologies
4 TEST SET UP AND RESULTS

This chapter discusses the post silicon testing of the Type-I and Type-II amperometric sensing circuits and reports the real time results that were obtained. It also discusses the results and draws a comparison between the simulation and real time results.

The circuit design of Type-I and Type-II circuits discussed in the previous chapter were fabricated through the MOSIS foundry service using the AMI 1.5 micron technology. The fabricated design was packaged in Leadless Chip Carrier (LCC) packaging. As the name suggests LCC packaging does not have leads. Instead it has rounded pins at the edges, which makes the packaging smaller and more compact. The ceramic package had 44 pins, out of which 40 pins were connected to the bonding pads of the padframe discussed in Chapter 3. The remaining 4 pins were not connected. A snapshot of the LCC packaging is shown in Figure 4-1 [15]

![Figure 4-1: Picture illustrating the difference between an LCC packaging and conventional DIP packaging](image)
The pin out of the package is as shown in Figure 4-2.

As described in the previous chapter the padframe was divided into upper and lower halves. The upper half contained the Type-I and Type-II amperometric circuits described in this thesis work.

### 4.1 TEST SET UP FOR TYPE-I CIRCUITS

The laboratory test set up for performing the post silicon testing is as shown in Figure 4-3. As shown by the figure the test setup includes a current source, a 5 volt power supply and a multi-meter. The test components are all connected to breadboard that holds a special socket that...
can hold the LCC packaged chip. The specification for each of these components is described in the following sub-section.

### 4.1.1 APPRATUS DISCUSSION

**Current Source:**

The current source used to provide the input current for the amperometric circuits was Keithley 220 Programmable Current source. It is a programmable DC current source with high accuracy and low noise. It has an LED display for displaying the current being sourced and has the ability to source current in the range of 1pA to 1uA.

**Socket:**

The LCC packaging though compact has a drawback that the IC cannot be directly soldered onto a breadboard or fitted on a conventional testing board for testing and debugging purposes. The absence of leads required that the IC be mounted on a socket. The socket was then soldered onto a general purpose board for further testing. The socket used for the LCC packaging in this thesis work was procured from Emulation Technologies (Part number SKT2292). The ease of press
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Figure 4-5: Figure describing the pin out of the IC for the amperometric circuits

fitting the IC into the socket proves to be convenient during testing and was one of the reasons for its selection. Figure 4-4 shows the footprint of the SKT2292 socket that was used in this thesis work.

**Multi-meter:**

Multi-meter used to measure the output voltages was a HP 34401A Multi-meter. Some of the features of this multi-meter that aided in recording precise measurements were to measure with a
resolution of 6 1/2 digits and a dc accuracy of 0.0015%. The readings taken on the multi-meter also had the option of being stored on the internal memory which had a capacity of 512 readings. This feature coupled with the programmable current source provides the avenue to automate the bench top testing of the current sensor.

The pin out of the for the upper half of the padframe is described in Figure 4-5

4.1.2 TEST PROCEDURE

The IC was initially tested for possible short circuits or other fault by measuring the resistance between adjacent pins and other critical paths e.g. between supplies. During this phase no voltage or current was injected into the circuitry. The next step was to provide the ground voltage (0V) at pin 12 and to check the output voltage at the corner pin 7. As the corner pad provides the supply to all other I/O pads, this serves in testing if there is any discontinuity between the power pad and the ground rail running to all other pads. The output voltage measured at pin 7 was 0V. Similar test was done for the V_{dd} supply. The V_{dd} supply (5V) was applied at pin 23 and the output voltage was measured at pin 18. The output voltage measured at pin 23 was 4.99V.

After this initial testing of continuity and insuring that the supply voltages were being provided to the I/O pads, the functional testing of Type-I circuit followed. The current source described above was initially set to a known value and connected to a pico-ammeter to gauge the loss due to the probes and leads. To test the first replication of the Type-I circuit input current was sourced into the circuitry by connecting the positive probe from the current source to pin 19. The intermediate output voltage from the first stage of the Type-I circuit was measured at pin 16 using the positive probe of the multi-meter. The negative/ground probes of the multi-meter and
current source was connected to the common ground of the IC. The output voltage reading obtained from the multi-meter was recorded for each step decrement of the input current. The input current was decremented starting from 1uA in steps until 90 pA after which the Type-I circuit was found to make no appreciable change in the output voltage. This methodology was adopted based on the rationale that the lower magnitude currents prove to be the limiting factor for the Type-I circuit. The steps in which the input current was decremented was also based in this rationale. Figure 4-3 illustrates this set up.

4.1.3 TEST RESULT DISCUSSION

The real time test results were observed to follow a trend similar to the simulation results and in conformance with the explanation of the expected behavior of the Type-I circuits in Chapter 2.

The following inferences were derived from the output voltage observed during the post fabrication testing of the Type-I circuit
Firstly, the circuit does not produce an appreciable change in output voltage when the magnitude of the input current is lowered below 1 nA. The output voltage stays almost constant for input currents in the range of 860 pA or lower. This proves to be a limitation for the Type-I circuits. Secondly, Type-I circuit provides a greater output swing for the input current ranging from 90 pA till 1uA when compared to the simulation results. Thirdly, the output node drawn from the op-amp does not follow the input (intermediate node) voltage as expected. The op-amp is configured in the voltage follower configuration and was expected to serve as a buffer hence providing signal isolation and noise immunity. On the contrary, the op-amp follows the input voltage for lower ranges until 0.798V. Thereafter, the op-amp’s output voltage gradually rises to be clamped at 4.99V. Fourthly, fabrication errors/misalignments and presence of parasitic elements (like diodes, bipolar transistors) are possible reasons for this incongruous behavior. Fifthly, gain for the desired region of operation (1nA – 10nA) is lower than the expected value with respect to the simulation results. Finally, the real-time output voltage swing for the region of operation (1nA – 10nA) has a more linear trend when compared to the simulation result for the same range of input current as shown in Chapter 2. Figure 4-6 illustrates the close to linear behavior of the Type-I circuit for the input current range of 1nA – 10nA.

4.1.4 REAL TIME VERSUS SIMULATION RESULTS

The results obtained from real-time testing of the Type-I circuit deviated from the expected behavior predicted by the Hspice simulations in a few aspects.

The output voltage swing obtained from the real-time testing was greater for the same input current ranges when compared to simulation results. The gain for lower input current ranges (nano-amperes and pico-amperes) was higher in simulation results resulting in greater difference in voltages for successive increments of input current. Figure 4-7 illustrates a comparison
between the results obtained from real-time testing and HSpice simulations for an input current range varying from 90pA – 1uA.

Figure 4-8 illustrates the comparison between the real-time test results and simulation results in the desired range of operation (1nA – 10nA). It is evident from this chart that, the real-time test results have a diminished output voltage swing of 80mV over an input current variation from 1nA – 10nA. Simulation results presented in Chapter 2 had predicted the output voltage swing to be 555mV. However, it is also to be noted that the real-time results are more linear in trend than the simulation results for this input current range.
4.2 TEST SET UP FOR TYPE-II CIRCUITS

Figure 4-9 shows the test set up used for testing the Type-II circuits. The test apparatus used for the testing of Type-II circuits was the same as Type-I circuits mentioned in 4.1.1.

4.2.1 TEST PROCEDURE

The test set up for the functional testing of the Type-II circuit is as shown in Figure 4-9. The circuit initially requires a reset pulse which is a step input to be applied at pin 14. Simultaneously, the input current is injected at pin 22. The circuit behaves to the applied magnitude of input current as discussed in Chapter 2. Outputs are drawn at two points from the Type-II circuit as shown in Figure 4-9. The output being read by the multi-meter is drawn from pin 3. The multi-meter records the voltage on the capacitor discussed in Chapter 2. The other
Figure 4-9: Test set up for Type-II circuits

output is drawn from pin 4. The signal from pin 4 is fed to an external counter. The counter counts till the time the Schmitt trigger output enables it. Once the Schmitt trigger of Type-II circuit changes voltage levels the counter is disabled and the value is read on either an LED display or a Logic analyzer.

The output value of the counter directly indicates the time taken to charge the capacitor. A calibration of the time taken to charge the capacitor against the input current injected can be derived from the measurements recorded. This calibration can be further extended to the calibration of the time taken to charge the capacitor against the concentration of the analyte being measured.

4.2.2 TEST RESULTS DISCUSSION

As mentioned in 4.1.3, the operational amplifier [7] used in Type-I circuit did not behave as expected in its configuration. The possible reasons for the anomaly could be fabrication errors/misalignments or the presence of parasitic elements (like bipolar transistors, diodes etc.). This unexpected behavior is also associated with the op-amp used to form the current conveyor
of the Type-II circuit. As a result the vital part of Type-II circuit viz. current conveyor could not be realized and hence no appreciable test results could be obtained. Hence, this thesis works only reports the simulation results of the Type-II circuit in Chapter 2. A discussion about the possible reasons for the incongruous behavior is presented in Divjyot Bhan’s thesis work [7].
5 CONCLUSION

This chapter provides a summary of the work done in this thesis and evaluates the success of the designs that have been introduced, as per the requirements and problem statement that was discussed in Chapter 1. A future work section suggests the work that needs to be accomplished to overcome the limitations of the Type-I and Type-II circuits.

5.1 SUMMARY

This thesis work presented a solution to the problem that arose from the limitations encountered in a previous generation current sensor design i.e. problems in detecting low magnitude currents especially in the desired operating range (1nA – 10nA). Extensive simulation results of the Type-I and Type-II circuits for various ranges of input current were presented. These simulation results provided evidence to support the theoretical explanation of the behavior anticipated for these circuits.

The Type-I circuit, which is an improvement on the principle described by Chunyan Wang [3] primarily functions as a current to voltage converter which allows adaptive gain for different strengths of input current. This adaptive gain permits a high gain for the low magnitude input currents, thus producing higher voltage difference between successive increments in input current.

The Type-II circuit was based on the design described by Harpreet Narula and John Harris [8] which followed a time based approach for the low current signal detection. The Type-II circuit aimed at converting the input current into time differential. This time based conversion
eliminated the requirement of any current amplifying circuitry. At the same time it also enhanced the dynamic range of the output signal and reduced matching problems [8].

This thesis work accomplished schematic entry of the Type-I and Type-II circuits using Cadence Virtuoso and performed layout using Magic layout editor. The absence of certain rule and design files did not permit performing layout of these circuits using Cadence Virtuoso. The layouts were completed with good analog design layout techniques that were presented in Chapter 3. This chapter also presented the simulation results of the Type-I and Type-II circuits using two technologies other than AMI 1.5 micron viz. AMI 0.5 micron and TSMC 0.3 micron. The simulation results aid in providing an insight to any future work that may be performed using a technology other than AMI 1.5. It also predicts the behavior of the circuits in different technologies and serves as a corner case parameter.

The laid out designs were fabricated by MOSIS foundry service using the AMI 1.5 micron technology and packaged in LCC packaging. Chapter 4 provided detailed description of the bench top test set up used to test the Type-I and Type-II circuits. It also discussed the test results obtained from these circuits and compared them against the simulation results presented in earlier chapters. This comparison illustrated the conformance and deviations of the fabricated circuits with respect to the theoretical explanation of the behavior of these circuits.

5.2 EVALUATION OF THE DESIGN

The primary requirement for this thesis work was the detection of low current input signals especially in the desired range of operation (1nA – 10nA). A secondary requirement was low area consumption. This requirement arose keeping in mind the overall system (beyond the scope of this work) of which this current sensor would be a part of. Lower area consumption would
allow replications of the circuit within the padframe providing the necessary resource for performing time-multiplexing in the overall system.

The real time results of Type-I circuit presented in Chapter 4 show that in the desired range of operation (1nA – 10nA) the difference in output voltage for every step increase of 1 nA within this range was 5 mV. This change of output voltage is enough to produce 1-bit change in an analog to digital converter (ADC) with 10-bit resolution. Hence, an ADC with 10-bit resolution following the Type-I circuit shall be able to indicate every nano-ampere change in input current. Therefore, the Type-I circuit is found to be successful in fulfilling the requirement of detecting low current input signal in the desired range of operation (1nA – 10nA). Failure of the micro-electrode sensors, introduced in Chapter 1, would produce an output current in the range of hundreds of nano-amperes to a micro-ampere. Type-I circuits are capable of measuring currents in this range as well. The test results for Type-I circuit show that there is a difference of 0.83V between the correct region of operation and failure of the micro-electrode sensors. This voltage range is enough to indicate the state of the micro-electrodes through several bits of the ADC. Hence, the Type-I circuit is successful in indicating whether the micro-electrode sensors are working as expected. Finally, the output voltage of the Type-I circuit can be fed to the ADC and a direct calibration between the digital output and the concentration of the analyte being tested can be derived. This aspect would prove to be vital in the overall system, as discussed in Chapter 1.

The Type-I circuit occupied an area of $106833 \lambda^2$ where $\lambda=0.8$ micron for the AMI 1.5 micron technology. The layout of Type-I circuit was compact enough for four replications of the circuit within the padframe as shown in Chapter 3. Compact area of Type-I circuit fulfilled the secondary requirement discussed earlier. Hspice simulation results of Type-I circuits showed the
average power consumption to be 6.698 mW. This is reasonably low power consumption and
opens the avenue for the use of these circuits in low power applications as well. Input current
signals lower than 1nA proved to be a limitation for the Type-I circuits.

Type-II circuits as explained in Chapter 3 could not be tested due to anomalies in the behavior of
the op-amp configured for a current conveyor. Hence, this thesis work presents no rationales that
prove the fulfillment of the requirements by Type-II circuits.

In a conclusion, this thesis work proposed and proved, through simulation results and real-time
test results, an amperometric circuit that is capable of measuring low current input signals and
can produce the required change in the output to indicate the sensing of these currents for the
worst case scenario as mentioned in Chapter 1. However, a higher gain (maybe by a factor of 10)
would be desirable for this operating current range in order to accommodate any noise issues that
may originate from the microelectrode sensors or overall system. These noise issues are
unknown at this point. Type-I circuit fulfills the requirements put forth for this thesis work and
presents a current sensing solution that can be incorporated in the overall system for in-situ
measurements of toxicants or pollutants in water, bio-film and others.

5.3 FUTURE WORK

Limitation of the Type-I circuit for input currents lower than 1nA triggers off scope for future
work. The prime challenge in future work would be to increase the gain of the circuit for input
currents lower than 1nA. Alteration of the length and width of the transistors used in Type-I
circuits with respect to the current equations for the transistors in different regions of operation
viz. saturation and linear, could prove to be one possible solution to this problem.
Design of an operational amplifier for proper functioning in the voltage follower configuration (Type-I circuit) and current conveyor (Type-II circuit) would be yet another challenge in future work. Prior work done in this area [16] would be a good reference to achieve the design of an operational amplifier for the requirements put forth.
REFERENCES


