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I, ________________________________, hereby submit this work as part of the requirements for the degree of:
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It is entitled:
Imaging Sensors with Data Communications Capabilities

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Imaging Sensors with Data Communications Capabilities

A Thesis Submitted to
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Master of Science
Department of Electrical & Computer Engineering & Computer Science, College of Engineering
by

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Bachelor of Science in Computer Engineering
Bachelor of Science in Electrical Engineering

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Dedicated to my wife Maren, my parents, sister, and grandparents for their support, encouragement, and confidence in me.
Abstract

Currently radio frequencies are employed in wireless internet and cellular telephones. Radio frequencies, however, are partially regulated and can interfere with surrounding devices. In contrast, optical communication offers a non-regulated/cost-effective interface that can be implemented with human safe light sources such as LEDs. Furthermore, the combination of imaging with optical communication makes communication with multiple optical data sources within a scene possible.

This thesis explores the design of data communicating imaging sensors that store video and data information from a scene within an array of light-sensitive pixels. Applications of these sensors include: security monitoring, optical-based asset tracking, or vehicle-to-vehicle communication.

Four data communicating sensor designs are explored, concluding with two key designs: Beta and Gamma. The Beta sensor stores video and data within each pixel. The Gamma sensor stores video in every pixel but distributes data storage among a cluster of pixels.
Acknowledgements

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Chapter 1 Introduction

“Ubiquitous computing” is a frequently-used cliché describing the goal of placing small computers in every facet of daily life. While this goal contains certain privacy, social, and intellectual concerns, there are some tangible benefits inherent in the goal. A key piece of this goal is wireless communication. Currently, radio frequency (RF) communication is popular for cell phones and wireless Internet connections. RF is also being rapidly adopted to replace bar codes and Wal-Mart has recently required all its distributors to use radio frequency identification (RFID) tags. This will allow Wal-Mart’s store shelves and warehouses to automatically monitor how much of a given product has been sold and which products need replenished within the store or warehouse.

In this goal of ubiquitous computing interfaces are extremely important. RFID enables products on the shelf to give information to their surroundings. Stores also frequently use surveillance cameras to monitor their inventory and the patrons within the store. A combination of video surveillance with RF ID tags on merchandise can provide additional security information. The combination of video and wireless communication can be used to augment the overall system’s capabilities. In short, the combination of wireless communication integrated with video has potentially interesting applications worth exploration.

RF has many benefits including distance communication, the ability to go through common structures (most buildings), and being omni-directional. However, RF is not perfect for every situation. RF is regulated, requires multiple antennas for finding location, and is
omni-directional. Optical communication by nature is directional (television remote control) and is un-regulated. Furthermore, within the context of a picture, an optical source’s location in a 2 dimensional space is easily determined. The choice between optical and radio frequency communication is one of application and environment.

This thesis investigates the design of a data-integrated video imager. This chip integrates a video array with the ability to communicate with multiple optical data sources in the same field of view. The integration of communication and imaging allows for a simple system to track a scene with multiple moving data sources within it.

To clarify, the goal of the Photonic Communication Imager (PHOCI™) is to communicate with multiple optical sources at the same time. In addition, the chip has the ability to capture a video image of a scene. The system driving this chip produces a video image and can identify, track, and receive communications from data sources within that picture. There are several benefits of optical communication in this area. Antennas are not required to track the source; the optical spectrum is not regulated; and there is no interaction between nearby electronics and an optical data source. The broad goal of the chip designs explored in this thesis is to capture a video image, locate data sources within that image, and then receive communication from those sources.

**1.2 Motivation for Research**

As previously mentioned, the drive to “Ubiquitous Computing” creates a need for new ways to interact with electronic devices. The design of these chips investigates the
capabilities of a system based around a data communicating imager. The system can
track items with optical tags on them in a warehouse. It is also feasible to attach an optical
source to the system for two way communication. With the ability to track multiple data
sources, ad hoc optical networks can be created. The motivation in designing the sensors
themselves is to provide flexible imaging and communication capabilities without limiting
the final application space.

1.3 Objective of Research

The objective of this research is to explore the design space of a data integrated imager.
There will be system, optical, and electrical metrics. These goals are organized as follows.

The chip must be able to record video and receive data independently and simultaneously.
This is key to meeting the goals of the system augmenting an image with data from
multiple sources within the image.

The video portion of the system must run at least 30 fps. This is common video rate as
produced by many off the shelf cameras. The operation of the system is to constantly
scan video, while finding and capturing data sources.

The data side must be able to receive transmissions from many sources simultaneously.
Each implementation has a different number of sources it can support. More than 10 is
expected. Each communication channel must also support data transmission in at least
the kilo-bit range.
1.4 Thesis Overview

The remainder of this thesis is organized as follows.

Chapter 2: Background and Related Work

This chapter places the research in a field of research of optical communication. This includes free-space optical communication, communication with LEDs, and RF communication with video.

Chapter 3: Requirements, Performance, and Design Issues

The chapter outlines the performance metrics used to direct designs and evaluate implementations.

Chapter 4: Prototype

The prototype chip was the first PHOCI™ chip. This chip sets the design direction for the rest of the project and creates a baseline performance analysis.

Chapter 5: Alpha

The alpha chip expands the prototype functionality to a much larger array. The alpha pixel is much smaller because of reduced circuitry and a change of manufacturing technology.
Chapter 6: Beta

The Beta chip addresses some major performance issues encountered in the alpha design. The circuitry is further reduced from the alpha chip and the photodetector size is increased to provide better optical performance.

Chapter 7: Gamma

The Gamma architecture extends the Beta chip’s architecture by introducing the notion of clustering. Clustering assigns groups of video pixels to each specific data communication link. This produces a coarser data resolution capability, but it further reduces power consumption and allows for much large mega-pixel designs to be achieved.

Chapter 8: Chip Comparison

This chapter compares the benchmarks reached with each chip and discusses benefits and drawbacks from each approach.

Chapter 9: Conclusion

This chapter summarizes results of the work and provides direction for the use of this work in future implementations.
Chapter 2 Background and Related Work

The concept of a data communicating imager is related to several common areas of research. Free space optical communication has found applications where high speed and line of sight are required. Digital cameras have reached performance levels at and above film cameras and have become so popular that Nikon™ has chosen to begin phasing out their film camera line\(^7\).

2.1 Imaging

Digital Imaging chips are frequently created using CCD technology. These use a specialized process capable of transferring charge from one pixel to another in a highly efficient manner. However, because of their manufacturing, these chips are not practical for use if processing circuitry is to be included along with a photodetector. CMOS imagers are created using the common and inexpensive CMOS processes used to manufacture standard VLSI chips. These imagers are not as efficient as CCD imagers, but they consume less power and can contain circuitry within the pixel and on the chip in general\(^7\). The PHOCI™ imager falls into a category of chips using Smart Pixels\(^3\). These pixels contain an amount of circuitry associated with every photodetector. This ensures a very high degree of parallel operation.
2.2 Wireless Communication

Wireless communication is becoming increasingly common. Wireless standards like IEEE 802.11x, Bluetooth™, RFID, and the various cell phone standards each enjoy wide adoption. With coming standards such as ZigBee (IEEE 802.15.4) and Ultra-Wideband this trend would seem only to be increasing. In fact, Intel CEO Craig Barrett predicted wireless technology will be the most important technology of the current decade. Each of these standards make products possible that bring modern life closer and closer to that goal of “Ubiquitous Computing.” Optical communications are frequently used both in lower and higher end systems. Home audio/video remote controls as well as the IRDA standard use wireless free space communication for low speed transactions.

The Visible Light Communication Consortium (VLCC) is a group of companies and universities located in Japan. The VLCC has established itself to research using LED lights for ubiquitous computing. The VLCC is studying how communications using visible light can be used in lighting, ubiquitous computing and intelligent transportation systems. The VLCC concept complements the PHOCI™ concept. This organization is studying the use of human safe and visible light produced by LEDs for data communication. One of PHOCI™’s stated goals is to allow for flexible communication with data sources of varying optical powers. Both endeavors seek to create flexible optical communication link using low light level LEDs.
2.3 Related Work

FoxSports™ developed a system for tracking a hockey puck within a hockey game\textsuperscript{12}. This enabled FoxSports™ to hi-lite the puck so that television viewers could more easily see where the puck was located. The FoxTrax™ system modifies the hockey puck with an infrared (IR) beacon. Multiple IR sensors were then placed around the hockey rink to track the puck.

Another system creates a “High-Precision, High-Speed” camera system by combining two cameras\textsuperscript{13}. One camera is low resolution and high speed, while the other camera is high resolution and low speed. The combination of these cameras is able to track high speed motion with an interpolated high resolution. This system, however, requires much work in up-scaling the low resolution image and combining the resulting images.

Another similar system from Pixim™ allows for 1000 video samples to be taken each second enabling several sample periods to be attained\textsuperscript{14}. This is very high speed for a video sensor. This system would not be suitable for data communication because even at 1000 frames/second, the peak data rate would be limited to 1 kilobit per second. This sensor is aimed at low light level security cameras.

Another company named LightPointe™ produces the necessary equipment for transmission and reception of network data optically, over long distances. This technology uses Si receivers receiving infrared light (850 nm). These networks are used over long distances between buildings, and across stadiums where stringing a wire or optical fiber is
impractical and radio frequencies would be slower and less secure\textsuperscript{15}. This system provides no imaging capability.

Setting up multiple autonomous information sources with the capability of communicating with all other sources simultaneous would be very useful for applications like SmartDust\textsuperscript{TM}, made by Dust Incorporated. Currently, theses systems use RF communications along with their imaging capabilities. Providing this company with an optical alternative to RF could extend the benefits of their product and potentially reduce chip count in their system\textsuperscript{16}.

There has been some research for tracking an object optically that has an RFID tag attached to it\textsuperscript{17}. This system is based on CAD models of the object being tracked and much image analysis. This system requires models of the objects to be tracked in advance of tracking them. The model is required to perform image analysis to detect movement. The PHOCI\textsuperscript{TM} concept does not aim at tracking specific objects as much as data sources. A PHOCI\textsuperscript{TM} can replace both the camera and RFID tag reader in this situation with a single chip, thus reducing the system complexity.

Another paper explores the application of a camera with sub-window readout capability to free space optical data communication\textsuperscript{18}. Sub-window readout is the ability to capture only some regions of a video array, rather than the entire video array. This setup is extremely close to the data integrated video imager, but does not possess digital conversion within the pixel. This leads to a complex system design as their system solely outputs an intensity value. The system explored uses an analog to digital converter and digital signal processing to extract data sources from the video data output by the chip.
The approach explored in this thesis simplifies this by implementing the digital conversion within the pixel.
Chapter 3 Requirements, Design, and Performance Issues

The design of the PHOCI™ chips involved many factors playing against each other. This chapter explores what factors were considered and the potential benefits and pitfalls of each design factor.

3.1 Basic operation

The PHOCI™ sensors’ goals can be classified by their intended operation. The sensor is a video camera chip that can be constantly scanned to produce black and white analog values for a pixelated view of the imaged area. This video scanning operates in the 30 fps region that has become a standard for video. While producing video, the sensor will also mark pixels that might contain data sources. A data source is a digital, optical signal that is brighter than the general scene in the field of view. This optical signal’s “1” value is an optical intensity brighter than the scene the camera is focused on. There may be bright spots in the scene, but a data source will transmit information by modulating the optical signal. When the system driving the PHOCI™ sensor sees that there is potentially a data source at a specific pixel, the system will address that individual pixel. The pixel will then respond by providing data sampled from the optical input. If this data is judged to be valid, that pixel is designated as an active channel. Data communication from active channels occurs at much faster speeds than the video communication. For example, 30 fps video produces a frame 1 every 33 milliseconds. Supporting a data rate in the khz range would
require a scanning operation in the microsecond range. Once a data source is identified, the active channel is active until no more data is sent.

3.2 Pixel architecture

To accomplish the intended operation of the sensor, certain traits are required of the chip. The PHOCI™ sensors are an interpretation of these requirements. The defining trait of a PHOCI™ chip is that data and video are stored in the array. In addition the data and video stored within the array are independently addressable and captured at vastly different rates. This ensures that the data side can run at significantly faster speeds, and not address the entire array, as is common for video.

Early in the design cycle a basic signaling scheme was chosen. As the PHOCI™ sensors are camera chips, the pixels are arranged in an array. To control this array, a basic data flow was chosen. Pixels are addressed by row. The outputs of the pixels are routed vertically by column. The data from each pixel is then routed off chip by control circuitry at the bottom of each column of pixels. This basic mode of operation was not changed through any of the chip designs. With this basic understanding of the sensor and its function, the pixel is the unique feature of these sensors and, as such, is the most interesting. Figure 3.1 shows the basic block architecture of a PHOCI™ pixel that is shared by all the sensor designs explored in this thesis.
The Photoreceiver block contains the photodetector and support circuitry to produce electric signals for the Data and Video paths. A goal of the PHOCI™ sensor is to be easily adaptable to many situations. Integrating video and data makes a simple system that does not require image analysis or multiple cameras. Another trait of being easily adaptable is to use common, non-harmful light sources for data transmission. LED light sources are now used in everything from flashlights to status lights and do not produce harmful light levels as lasers can. LED communication is also advantageous because it helps keep the total system costs low.
The Video Sampling block contains circuitry for sampling the Photoreceiver block and clearing the Data Storage. This block controls how long the video is sampled. This is analogous to a film camera's exposure time.

The Video Storage block stores an analog video value. It also has the capability to route this analog value out of the array to the control circuitry. This storage is addressed separately from the data storage.

The Digital Conversion block converts the optical intensity incident on the photodetector to a digital value. This block receives a value of light from the control system to accept as a data source. This allows the data sources to operate in many environments and with many different data sources.

The Data Storage block stores data from the Digital Conversion and routes the data out of the array. The amount of storage and signaling of the storage are implementation issues in each chip.

The remaining block is the Data Flag. The Data Flag is a digital bit read by the system during video readout. The Data Flag indicates data may be contained in the currently addressed pixel.
3.3 Pixel implementation

These chips went through an iterative design process. Concepts are proved in small prototype chips and then applied to larger chips to build a fully functional sensor. The aspects of this implementation are as follows.

3.3.1 Optical Implementation

A digital imaging sensor has an arrayed set of pixels each containing a photodetector and its supporting electronics. The photodetector and supporting electronics must occupy separate and non-overlapping areas of each pixel. In addition, the electronics must be optically shielded such that the optical signal incident on the entire sensor does not influence the electrical operation of the circuitry. Only the photodetector itself responds to the optical light incident on the pixel. The electronics contained in each pixel do not respond to the light. This creates a so called “dead spot” in the array.
Figure 3.2 shows a scene from the photodetector’s reference view. This is an exaggerated view of the pixelation introduced by a smart pixel design. This is not a picture produced by a PHOCI$^\text{TM}$ sensor, but rather a representation of what the camera “sees.” In this example, the picture is subdivided into a 5x5 array of pixels. The shaded areas of the picture represent where electronics are located. The light spots represent where a photodetector would be. All of the picture that is shaded is not seen by the camera, because it does not fall on a photodetector. The PHOCI$^\text{TM}$ chips are looking for data in addition to the video.

The circles in Figure 3.2 represent possible data sources. It can be seen that the larger circle covers some shaded area and some photodetector area. Assuming the data source is bright enough, this data source will be seen by the sensor. The smaller circle falls solely in the shaded portion of the picture. This data source will not be seen at all, no matter how
bright it is. The shading highlights what will be referred to as “dead spot.” This is further explained below.

Figure 3.3 shows the measurements for quantifying the effect integrated electronics have on the pixel. This pixel is similar to that which is portrayed in Figure 3.2. The dead spot is defined as the largest distance between two photodetectors within the array, as shown in Equation 3.1. After lensing is chosen, the array along with dead spot is projected onto a scene. This dead spot computed against the size of the field of view defines the minimum data source size that can be guaranteed to be detectable in a field of view.
Another metric of pixel quality is fill factor, as defined in Equation 3.2. This equation describes the how much of the image is sampled. A higher fill factor aids a picture’s clarity.

The remaining portion of the optical system is the lensing system and the total pixel count in the array. These two factors determine the amount of the space that is projected on a pixel. With the same lensing, more pixels in the array allow the scene to be broken into more individual pieces. A photodetector averages all light incident on it. An array with more pixels reduces the physical space being projected onto a single pixel, as compared to a smaller array. Less averaging of the seen occurs with a larger and larger array. Lensing makes distance from the sensor a tricky situation to address at the sensor level. There is a difference between distance and field of view. Distance from the lens is a simple one dimensional unit. Field of view is the total area seen by the lens at the focused distance. The design of the sensor concerns the image that is projected onto the sensor. Inversely, the sensor array can be thought of as being projected onto the image (as illustrated in Figure 3.2). Lensing can project either an image closeup (macro lens) onto the sensor or it can project a distant scene (zoom lens) onto the sensor. In both cases, the same array of photodetectors and dead spots are projected onto the scene. For instance, if a 128x128 array is used and the field of view is 128 inches (~11 feet) square, each pixel will contain about a square inch of the scene. If the focus is on a scene that is 128 feet square (~43 yards), then each pixel will contain a square foot of the actual scene.
3.3.1 Electrical Implementation

There are certain electrical considerations to take into account as well as the optical considerations. The photodetector is obviously the basic element of each PHOCi™ sensor. The PHOCi™ sensors use an nwell-to-psubstrate diode because it produces a significant amount of current for incident light (for low light situations) and requires only a small guard ring around it (aiding fill factor). The only decision about the photodetector to be made in the study of this thesis is its geometry and size. There could be several shapes imaginable for the photodetector. Each of the photodetectors designed for these chips is rectangular in shape. This was for ease of layout and to save space. There was a minimal exploration concerning the adjustment of the corners of the pixel and photodetector to reduce the size of the dead spot. This ended up requiring larger amounts of space because of spacing rules associated with the materials used to create the photodetector. This exploration can be applied to the pixel as well, with some minor exceptions (due to well spacings, to be explained in the implementations). This means that the photodetector will be close to rectangular, allowing the pixel surrounding it to be close to square. With this specific geometry in mind, circuitry and layout can be easily turned into fill factor and dead spot calculations.

Data communication has several influencing factors. The ability to distinguish a bright tag from its background is important. This is the idea of thresholding. A given environment has a certain brightness that is commonly measured by traditional photographic light meters. This general brightness incident on a photodetector produces an electrical current relative to the brightness of the scene. A data source must be brighter than the
environment it is in. The data source produces a current that is greater than the current produced by the general environment. The circuitry most likely will be faster than the chosen photodetector. The chip’s bandwidth issues come with getting data from many pixels off the chip before the data starts getting overwritten. This is the determination of active pixels.

Once the determination of photodetector size is made, the rest of the pixel can be designed. In the PHOCI™ investigations this is left to the remaining pixel components; the bus and circuitry. There are a discrete number of vertical metal layers which can be used for bringing signals from outside the array into the pixels and from within the pixel to outside the array. If enough layers exist bus lines can be stacked vertically. In any organized standard cell or pixel-lated design, it is most useful to assign rules to the metal layers. For example, in a process with 5 metal layers, metal 1 may be used for power and ground, metals 2 and 3 could go vertically, and metals 4/5 can go horizontally. By making these rules, the designer is able to break the total pixel bus into vertical and horizontal buses. This begins the process of assigning signals to certain wires in certain metal layers.

There is an amount of space that can be saved by laying out circuitry in an intelligent manor. However, the area that circuitry takes up is more related to how many components are in the design, and how large those components are.

Bus layout is similar. Fewer wires take up less space. The stacking of wires, however, has much more of an impact on the space taken up by the bus than creative layout has on component layout. A bus wire in this chip is most likely to have one connection per pixel.
Transistors have three connections. As the PHOCI™ chip design moved from one generation to the next, there were tradeoffs between building smaller circuitry against building smaller buses. To make smaller circuitry, transistors must be eliminated; to make smaller buses, creative ways of overlapping wires, and even wire reuse must be considered.

While physical constraints are of obvious importance to an optical chip, power constraints are also important to an arrayed design. The prototype pixel was used in a 7x7 array. This means the power consumed by a pixel was multiplied by 49 for the array. The alpha and gamma chips were 128x128, meaning the power consumed by each pixel was multiplied by 16,384. This means that the alpha pixel should consume ~334 times less power than the prototype pixel for the array to use the same amount of power.

Bandwidth tends to stress circuit design rather than issues relating to arraying the circuits. The circuits need to be designed to input and output data at speeds capable of supporting the speed of the photodetector. The only major issue that needs addressed in order to support a large array is driving a signal from within the pixel across the large bus line capacitance to the control circuitry.
Chapter 4 Prototype

The PHOCI™ prototype sensor was designed with the sole purpose of providing a sensor for the demonstration and analysis of a data integrated video imager. This sensor was actually the fourth in a series of test sensors. The first of these sensors was functionally inoperative and the second and third sensors used a fixed data thresholding mechanism that made these sensors operate only in narrow ranges of optical power illumination. The fourth sensor had a variable thresholding circuit that controls what light power is accepted as a data source. It functioned adequately for experimentation and demonstration of the data communicating imager concept.

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*Figure 4.1 Prototype Sensor Characteristics*
The physical characteristics of the fourth prototype sensor and its implementation are summarized in Figure 4.1. The circuit architecture of the sensor was derived from the third prototype sensor with the main modification being the addition of a variable thresholding circuit. After extensive simulation based testing of the circuit, a CMOS implementation was created and fabricated. In the remainder of this chapter, a detailed review of the sensor architecture and its implementation is presented. The chapter concludes with a review of the performance characteristics of this sensor. In the remainder of this thesis, we will use the term “prototype sensor” to refer to this fourth implementation.

4.1 Architecture

The goal of the chip architecture is to provide minimal functionality, while still enabling the creation an array of pixels. This sensor contains a 7x7 array of identical pixels. The video and data paths are accessed separately using on chip decoders. The video and data values are routed to the pins of the chip for storage and processing. The chip’s optical thresholding capability is controlled by an off-chip voltage applied to a pin. All control, video and data capture, data source validation and tracking are performed off sensor.

With the processing kept off-chip, the principle challenge of the sensor is the architecture of the pixel. Clearly the pixel's main functions are receiving light, and producing a video and data signal from that light. However, the location of new data sources within a scene is the key design feature. It may be possible to scan the entire array for data on a small array. However, as the design scales to larger array sizes, scanning the entire array for data would impede the system speed. As previously discussed, the video rate and data
rates are vastly different. This is because the data speed is relative only to a single pixel, while the video frame rate is relative to the entire array.

To achieve separate data and video functionality, the PHOCI™ concept has been subdivided into certain blocks common across all PHOCI™ chips, namely: Photoreceiver, Video Sampling, Video Storage, Digital Conversion, Data Storage and Data Flag, as seen in Figure 3.1. The Photoreceiver block takes the light incident on the pixel and begins both the video and data paths. The Video Sampling block controls the storage of an analog video value. The Video Storage block stores that value and routes the value out of the array. The Digital Conversion block produces a digital value based on the incident light intensity. The Data Storage block saves the data produced by the Digital Conversion block. Finally the Data Flag block notifies the video readout system that there may be data in the currently sampled pixel.

The prototype sensor architecture implements each of these blocks. Within the Photoreceiver block, incident light is converted to an electrical signal. The representation and magnitude of this electrical signal must be determined. The Video Sampling block must allow for variable sampling times and the ability to clear the previous video sample. The Video Storage block must store the value and be able to drive that value to the outside of the array. The Digital Conversion block must take in an analog electrical signal in addition to a variable threshold and produce a digital representation of that signal. The Data Storage block must take the digital signal from the Digital Conversion block and hold that value until readout by the controlling system. Lastly, the Data Flag block produces a signal available on video readout that tells the controlling system if data may be present.
4.1.1 Pixel Architecture

The prototype pixel architecture is presented in Figure 4.2. The blocks are labeled as expected from the previous introduction of the specific blocks: Photoreceiver, Video Sampling, Video Storage, Digital Conversion, Data Storage, and Data Flag.

The prototype Photoreceiver block shown in Figure 4.2 is where light hits the pixel and is turned into an electrical signal. The detector is a photodiode that is kept in a reverse bias state to function as desired. A current mirror is used to bias the photodetector and capture the current running through the photodetector. The current mirror creates an
analog current for the Video Sampling block. The prototype also uses the current mirror to create an analog voltage. This voltage is converted to a digital value in the Digital Conversion block.

The Video Sampling block receives an analog current from the Photoreceiver block. The Video Sampling block takes in a Video Sample signal and Video Clear signal and controls when the light input is sampled and when the stored value is cleared. These two signals have no physical directionality to conform to the stated flow of data.

The prototype Video Storage block stores the current controlled by the Video Sampling block. This capacitor's analog value is then applied to the line capacitance on a readout when the pixel is addressed with the Video Row Select signal. The Video Row Select signal is a horizontal signal, as rows are defined as horizontal groups of pixels.

The Digital Conversion block takes in an analog voltage from the Photoreceiver block and produces a digital value. The voltage on the photodiode node decreases as incident light intensity increases. This voltage is then amplified and routed into a differential amplifier. The differential amplifier compares the voltage representing light intensity to a voltage chosen exterior to the array. If the light input voltage is higher than the threshold voltage, the differential amplifier outputs a '1'. If the light input voltage is less than the threshold, the differential amplifier outputs a '0'. The last step in the Digital Conversion block is a D flip-flop. This flip flop holds an incoming bit for input into the data storage. The Digital Conversion block contains 3 incoming signals. The differential amplifier takes the
Threshold input and a Current Bias voltage for controlling how much current flows through the differential amplifier. The D flip flop uses a Clock signal to store data.

The prototype Data Storage block stores the bits provided serially from the Digital Conversion block for routing out of the pixel in parallel. The unique feature of a PHOCi™ sensor is the pixel’s ability to store digital data in addition to an analog video signal. The prototype chip contains 4 bits of storage, each implemented using a standard cell latch. The latch outputs are routed through pass gates to the outside of the array and eventually off the chip. Writing to each latch is controlled by 4 write enable signals. These write enable signals occur in sequential order to store sequentially received bits from the photodiode. When the pixel’s row is selected using Data Row Select, the values stored in these 4 latches are routed to the outside of the array, and then off chip.

The Data Flag block is the only interaction between the video path and the data path. The data flag is a simple “OR-ing” together of each of the data bits. As soon as a ‘1’ is received by the pixel, and stored in the Data Storage block, the data flag will be read as true. The data flag is output when the Video Row Select signal is enabled. The intended operation of the chip is to constantly scan the video output. While scanning each pixel’s video path, the data flag is examined to determine if that pixel possibly contains data. If the data flag is set to true, then a data source may be located in that pixel’s area.
4.1.2 Bus architecture

The prototype sensor is implemented using AMI 1.5 μm technology. This technology provides only 2 metal layers, so bus structure is not so important. Metal 1 is used for inter-circuit wiring and horizontal signals. Metal 2 is used for vertical busing.

4.2 Implementation

The goal of the layout is to place all the functional blocks in a manner that aligns the signals from pixel to pixel. Figure 4.3 shows the final layout of the prototype pixel. A mostly square layout was chosen to accommodate arraying of the pixel and a logical optical
layout. As previously described, the general data flow is that rows are selected (using

**Video Row Select** and **Data Row Select**) horizontally, and video and data are
passed vertically. The row select signals are generated by decoders. Once the data and
video have been propagated to the bottom of the array, column select signals choose
which column to read out of the chip.

The layout begins with the Photoreceiver block, as shown in Figure 4.3. The first element
in the current mirror is a diode connected p-type transistor. This allows three conditions to
be met. The diode node is pulled near **Vdd** such that the photodiode is kept in reverse
bias condition. In addition, the photodiode's node voltage is able to fluctuate in
relationship to the current being pulled by the photodiode. This is the same as a current
being pulled across a resistor. Third, the current from the photodiode is mirrored in a
second transistor for video sampling into a capacitor. This transistor was made quite long
to increase its resistivity in order to have a reasonable voltage swing for the data path. This
sets up the separate paths for video (with mirrored current) and data (with a voltage). As
will be discussed in the storage portion of this chapter, the layout space of this chip is
dominated by using standard cells. Standard cells not only have standard circuits and
transistor sizes, but also standard layout geometries. The standard cell layout geometry
dictates the layout of the p and n wells. This in turn sets the guide for laying out the
custom circuitry within the pixel.
The Video Sampling circuit samples the photodetector current when \text{Video Sample} turned on, and clears the video storage capacitor when \text{Video Clear} is turned on. It is shown in the “Video Sampling” block of Figure 4.3.

The Video Storage block holds an analog video value from the Video Sampling circuit, and outputs that value to the bottom of the array. The current is sampled into a capacitor, and then read out on the video out line. The capacitor in this design is sized to share its charge with the line capacitance when \text{Video Row Select} is turned on. In later designs it is not possible to use such a large capacitor in the pixel and create larger arrays. The sampling transistor’s size is made slightly wider than a standard cell to allow better current flow. The clear transistor is sized to clear the capacitor quickly.

The Digital Conversion and Data Storage blocks constitute the novel addition to a typical video pixel. As such, their layout comes to define the pixel’s main characteristics. As previously mentioned the data path begins with a voltage drawn off of the video-path’s current-sourcing transistor. In the first stage, this voltage is amplified from a millivolt signal to a \text{Gnd} to \text{Vdd} signal. This is accomplished using an active load configured amplifier. As the current source is an inverting structure, so is this amplifier. This leads to a positive logic analog voltage being fed into the differential amplifier. This means that the brighter the light is, the higher this voltage will be. This is seen in block “Digital conversion” in Figure 4.3.

A differential amplifier is used to decide when a light value is accepted as a data source. This differential amp compares the output of the first stage amplifier to a reference voltage.
The reference voltage is a way of setting a light threshold. The brighter the data source is, the higher the voltage is coming out of the first stage amplifier. The transfer function of the first stage amplifier can be used to correlate voltage with input light intensity. This transfer function can also apply to the reference voltage, such that the system designer can set a threshold for light with a corresponding analog voltage. The differential amplifier is also an inverting structure. The signal coming from the differential amplifier is a digital signal. If the input light intensity is higher than the set threshold, then a '0' is output. If the input light intensity is less than the set threshold, a '1' is output. This value is then made into a positive logic by going through an inverter.

A D flip flop is used to stabilize the digital value from the threshold circuit and hold that value until it is stored in the Data Storage block. The D flip flop is the first circuit in the data path that is clocked. This controls the data flow between the Photoreceiver and data storage. The D flip flop is implemented using two standard latches in master slave configuration.

The Data Storage block is able to store 4 bits of data from the Digital Conversion block until the bits are read out of the pixel. These storage bits are located in the “Data Storage” block of Figure 4.3. The bit storage in the prototype is implemented with standard latches. The storage of serialized bits is accomplished using 4 Write Enable signals. There is one Write Enable signal for each latch. The control of these signals is such that each bit is written to in sequential order in relationship to the clock signal.
The Data Flag “ORs” together the 4 bits from the Data Storage block to signal if data may be present. This flag is available on the video readout, and is reset on data readout. The intended operation of the chip is to be constantly scanning video at a slow rate (compared to data). Initially, there are no data channels assigned to any pixels. When a data flag is read during the course of regular video scanning, the system assigns a channel to that pixel. With a channel assigned, the system knows to address that pixel and check its data bits. Addressing the data bits resets the data flag, so that it can be reset re-evaluated in the next video read cycle. This, however, is not as important once the system assigns an active channel to a data-receiving pixel. Once a data transmission is complete, the flag is left unset. The data flag can be seen in Figure 4.3 alongside the data storage.

The bus structure connects the pixel to the outside of the array. The AMI 1.5 μm CMOS process provides only 2 metal layers. This limits any type of creative bus structuring. However, using standard cells created a large pixel with adequate horizontal and vertical space for busing. With only two metal layers, it is obvious to route one metal layer vertically and the other horizontally. The standard cells follow a few structuring rules also. Metal 1 is used for power and ground and inter-cell wire routing. Metal 2 is used for connecting between cells. With this in mind, there is not much more focus on the busing structure. Outside of the pixel electronics, metal 2 is used for routing vertically and metal 1 is routed horizontally.

The support circuitry for this pixel design is similarly designed using standard cells. Because this is a simple 7x7 array, a decoder tree can easily be created using standard
gates. In order to buffer the analog voltage being driven outside the chip a standard cell operational amplifier was placed in the video path.

AMI 1.5 μm technology has several influences on the design of this chip. First and foremost, it has a relatively large feature size. In laying out photodetectors and circuits in an active pixel design, feature size has an interesting influence on design decisions. A photodetector’s performance is based on its physical size, regardless of feature size. This holds for all technologies and feature sizes. There is some dependence of the performance on the junction depths of the wells. This, however, is not a design decision and does not affect the performance nearly as much as photodetector area.

Circuitry area changes with feature sizes. Digital circuits specifically attempt to swing their voltage from power to ground, ideally with no voltage levels in between. This allows them to scale fairly easily with feature size. Although analog circuits may not scale as readily as digital circuits, they too scale with feature sizes. The photodetectors scaling issues are different than the circuit scaling issues. With the same incident light power and same photodetector structure, smaller and smaller photodetectors produce less current. This can be addressed by altering the design of amplifiers, capacitors, and timing requirements. In general, smaller feature sizes allow the sensor chips to have a better fill factor and smaller dead spot.
4.4 Functionality and Performance

Extensive simulations and verifications have been performed on the prototype chip. Each signal diagram in this chapter and subsequent chapters is a simulation waveform. Video has been shown to work at 30 fps, and data has been shown to function near 20kbps. The video and data channels have been shown to operate independently at these speeds. The threshold circuit has been simulated to operate in the 15-670 nW range. Simulations will now be discussed and explained.
The signaling control of the video path is shown in Figure 4.4. **Optical Signal Input** is kept at a constant to show the charging of the capacitor. The storage capacitor is cleared with the **Video Clear** signal. When the current is sampled with the **Video Sample** signal, the storage capacitor charges as shown in the **video storage capacitor** wavelength. The **video storage capacitor** is an internal node, and not the voltage routed out of the pixel. The **Video Row Select** signal shares charge from **video storage capacitor** with the line capacitance for reading for the video signal. **Video Out** shows the analog voltage stored on the storage capacitor being routed out of the pixel.

![Prototype Data Signal Diagram](image-url)
An example of data path control is shown in Figure 4.5. The optical input signal is now a pulse to show digital operation. The Clock is shown here oversampling the data signal by 4 times. All four Write Enable signals are placed in the same viewing area. The Write Enable signals have been spaced out to read every fourth bit that is sampled by the Clock. The next wavelengths show the data storage bits collecting data when their write enable signal is held high. The last wavelength shows the Data Flag staying high for the duration of data being stored in any of the bits, and going low when all the data has been written over by zeros.

The control of the optical input power vs. Threshold voltage is shown in Figure 4.6. This graph shows what optical input value of power is accepted as a data ‘1’. The optical characteristics of a PHOCI™ sensor set certain limits on its operation. The detector size sets the target optical power for both the tag and the amplifier circuitry. As the threshold
voltage is increased (shown on the X axis), the optical power required to register a data source is raised (shown on the y-axis).

![Graph showing optical input signal, threshold, and data output](image)

*Figure 4.7 Prototype Threshold signaling*

Figure 4.7 shows the signaling control of the thresholding circuit. The optical input signal increases linearly in power. The threshold is set at a constant voltage. The data signal produced by the threshold circuit goes high once there is enough optical power to register as a '1'.

Because of its small size, power consumption in the prototype is not a significant issue. There are only 49 pixels within the chip. The prototype pixel consumes .4 mW. This power consumption can be broken down by the main components of the design. The current mirror consumes a current relative to the optical current generated by the photodetector. This current is relatively small as compared to the current drawn by a static CMOS circuit or an amplifier. The circuitry size dictates a pixel size. The pixel size dictates the array size. Once there is a target array size, a power budget can be established. The
total chip power dissipation is dictated by what the package can dissipate. It is true that high power consumption brings problems such as power fluctuations and voltage drop across bus lines. These, however, can be dealt with by design using wide lines and extra capacitance. The absolute power limit is dictated by the packaging. A Kyocera Dip40 is the standard package for tiny chips. This package can dissipate 2.2 W of continuous power without a heat sink. Generously, 10% of that could be allocated to the control circuitry. This leaves almost 2W for the array. With a target of a 7x7 array, this creates a power budget of 41 mW. This is the highest power consumption the pixel can use and still have a chip that does not overheat. The prototype pixel is well within this limit.

Figure 4.8 shows the distribution of power consumption in the prototype pixel. It can be seen that the latches draw the most current under worst-case optical conditions. Because these are digital circuits, each circuit’s power consumption is related to the clock frequency driving the circuit. Each chip has been simulated at 100khz. This requires
certain optical powers for each chip, but allows a consistent electrical comparison for each circuit.

The bandwidth of this chip is dictated by the photodetector. This photodetector structure has been shown to operate near 500 khz using a strong laser. Using an LED at varying distances the chip was shown to operate at 15-20 khz.

![Image: Test Pattern and Picture of Test Pattern taken with Prototype Chip](image)

**Figure 4.9 Test Pattern and Picture of Test Pattern taken with Prototype Chip**

A test system was created using an FPGA card with RGB output. This system controlled the addressing of the video and data paths, and output a picture of the array to a monitor. Figure 4.9 shows an image test pattern on the left, and a picture of that test pattern taken with the Prototype chip on the right. The pattern was intentionally made to be 7x7 pixels for this chip.
Chapter 5 Alpha

The PHOCi™ alpha chip is the second design in the series of four. It is designed to migrate the concepts learned in the prototype series of chips to a larger array. The characteristics of the alpha chip are shown in Figure 5.1. In order to take the prototype design to a larger array, several broad goals must be reached. The pixel must be made smaller. The pixel must also use less power. Both of these goals can be accomplished using a smaller technology and fewer transistors. The prototype’s emphasis is on the pixel architecture, as it was the first in the series of chips. With an architecture in place, the emphasis of the alpha chip is on adaptation of the prototype architecture to a much smaller pixel. This chapter explores the details of that adaptation and how well the stated goals were met. The term “alpha sensor” refers to this second chip design.

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<tr>
<td>Packaging</td>
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<tr>
<td>Pixel Power Consumption (μW)</td>
<td>252.45</td>
</tr>
<tr>
<td>Transistor Count</td>
<td>47</td>
</tr>
</tbody>
</table>

*Figure 5.1 Alpha Sensor Characteristics*
5.1 Architecture

The alpha sensor is a 128x128 array of pixels. Each pixel contains 4 bits of storage and the ability to output an analog video signal. This pixel was designed to be substantially smaller than the prototype chip. This pixel has nearly the same architecture as the prototype, with a much different implementation. Analysis of the prototype pixel shows several circuits that could be implemented differently to save space. The latches used for data storage and the capacitor used for video storage both present large circuits that need reduced in size.

The standard PHOCITM blocks will now be discussed as they are applied to the alpha architecture. The strength of this approach is that while the blocks have the same function from chip to chip, they have vastly different implementations.

The Photoreceiver block seen in Figure 5.2 outputs a current for the Video Sampling block and a voltage for the Digital Conversion block. In order to create a smaller pixel, however,
the photodetector must be made smaller. This means there will be less generated current to sample and a smaller voltage swing to amplify for the Digital Conversion block.

The Video Sampling block has an identical architecture as the prototype in this chip. It samples the current from the Photoreceiver block into the Video Storage block. The Video Sampling block also takes in a Video Sample and Video Clear signal. These signals have no directionality.

The Video Storage block inputs a sampled current and produces a voltage. However, in migrating to the alpha chip, there are new implementation issues to address. In particular, the line capacitance in relationship to the video storage capacitor is much larger. Consequently, the analog stored voltage needs actively driven onto the bus using an amplifier. This block receives only the Video Row Select signal, which is a horizontal signal. The Video Out signal must be vertical to match the corresponding data flow.

The Digital Conversion block creates a digital value from a voltage generated by the Photoreceiver block. The thresholding capability is controlled by a voltage pin. To address the smaller voltage swing from the Photoreceiver block, two amplifiers are now used before the differential amplifier. The differential amplifier is the same structure as in the prototype. The D flip-flop is implemented using two pass transistors and two inverters. This circuit now takes in Threshold, Current Bias, and two non-overlapping clock signals Clock 1 and Clock 2. None of these signals have specific directionality.
The data storage path contains 4 bits of storage controlled by Write Enable signals and read out on Data Row Select. The prototype used latches for each of these bits. In the alpha chip, data storage is implemented with a much more space efficient DRAM circuit utilizing the same signaling. The Data Storage block receives 4 Write Enable signals and outputs 4 Data Bits. The Data Bits must be vertical signals in keeping with the previously stated data flow. The write enables have no directionality.

A static CMOS latch has been added for the Data Flag. This is connected to the unlatched data signal seen in Figure 5.2. This changes the algorithm of the data flag in a subtle way. The data flag will become true anytime a ‘1’ is accepted by the Digital Conversion block. This is slightly different than the prototype's 'OR-ing' together of the four data bits. This data flag will remain true, even if data is passed through the data storage bits. The data flag is reset when the pixel's Data Storage block is addressed. This requires the data flag to take in Data Row Select and Data Column Select. Data Row Select is a horizontal signal, while Data Column Select is a vertical signal. The Data Flag is addressed using Video Row Select.
5.2 Implementation

The implementation of the alpha chip, shown in Figure 5.3, varied greatly from the prototype pixel. The circuits in the alpha chip are all full custom design. A critical objective for this layout was the minimization of the non-photosensitive circuits in the pixel. As the alpha architecture did not change substantially from the prototype chip, the main focus of the alpha chip is on the pixel implementation.

The layout of the Photoreceiver block begins with a small photodetector size. Assuming quasi-uniform illumination across the field of view, the smaller photodetector creates a much smaller current. Because of the smaller current, a second gate-drain connected transistor was placed in cascode configuration with the current source connected to the
photodiode. This can be seen in the Photoreceiver block of Figure 5.2. This configuration increases the effective resistance seen by the photodiode and creates a larger voltage drop for a smaller current draw. Correspondingly, these transistors were made larger to increase their effective resistance.

The video sampling circuit is completely unchanged from the prototype chip. There is a sampling transistor and a clear transistor. Each of these transistors have now been minimally sized for space concerns. This circuit is nested close to the large Photoreceiver block circuit.

The video storage circuit of the alpha chip has changed significantly. The alpha pixel is much smaller to enable a larger array. This means the video storage circuit has less room for a large storage capacitor and a larger capacitance line to drive the video value out of the array. To correct this, an active load amplifier has been added in between the video storage node and the output from the pixel.

The Digital Conversion block had to be modified in order to save space and account for the smaller current draw of the photodetector. Even with the larger resistances mentioned in the Photoreceiver block section, there is a smaller voltage to amplify in this pixel. Because of this, a second amplifier has been added. The first amplifier is a pmos transistor with nmos active load. This provides some amplification while separating the photodiode from the larger amplifier. The larger, second amplifier is a common push-pull type with a larger gate capacitance. This capacitance was found to dampen the signal coming from the photodiode. The differential amplifier was kept largely the same from the
prototype chip. The D flip-flop, however, was implemented dynamically rather than statically. The first stage of the flip flop is comprised of a pass transistor connected to the input of an inverter. The data input to the flip flop is switched through the pass transistor controlled by Clock 1. This value is then input to an inverter. The second stage of the flip flop is identical to the first, with the exception that the pass transistor is controlled by Clock 2. To avoid race conditions, it is vital that Clock 1 and Clock 2 do not overlap. The output of this flip flop then goes to the Data storage.

The Data Storage has been transitioned from standard cell latches to fully custom DRAM circuits. The latches used in the prototype design contained 14 transistors each. The latches used both N and P type transistors which are sized for standard static CMOS operation. A DRAM circuit is comprised of 3 minimum sized nmos transistors. Their write signals correspond to PHOCI™'s write enable signal, while their read signal corresponds to PHOCI™'s Data Row Select signal. These circuits have a patterned layout as seen in the Data Storage block of Figure 5.3.

The Data Flag is a total redesign from its original definition in the prototype chip. The data flag is now implemented as a static CMOS latch. This is not a standard cell latch, but it has the common 3/1 pmos/nmos transistor sizes. This latch goes high when a data bit goes through the D flip flop. The latch then resets when the pixel's data path is accessed with both Data Row Select and Data Column Select. This circuit is placed in the lower right hand side of the layout as seen in Figure 5.3.
The bus of the alpha chip is just as important as the circuits within the pixel. The bus structure of this chip lead to a square pixel approach. To make the layout as regular as possible, the bus structure was chosen to have a similar number of vertical and horizontal signals. This created a mostly square layout. This is seen in Figure 5.3. The upper left corner is where the photodetector is placed. The contiguous block consisting of the bottom left and right corners is where the bulk of the circuitry is contained. The upper right corner contains the DRAM circuitry. This layout accommodates two long n and p wells in the bottom of the circuit. It also allows the many vertical and horizontal wires. There are 11 vertical wires, and 8 horizontal wires. The vertical wires consist of four write enables, four data outs, video out, data column select, and the data flag. The horizontal wires consist of Threshold, Comparator Bias, Data Row Select, Video Row Select, Clock 1, Clock 2, Video Sample, and Video Clear. TSMC .25 provides 5 metal layers. The metal layer assignments for this pixel are shown in Figure 5.4.

Metal 1  Vdd, Gnd, Local Wiring  
Metal 2  Intra-circuit Wiring  
Metal 3  Bus Connections  
Metal 4  Optical Shielding and Horizontal Bus  
Metal 5  Vertical Bus  

*Figure 5.4 Alpha Metal layer assignment*

Using metal 1 for Vdd and ground is sensible as it is the closest metal layer to the device connections in poly and diffusion. Using metal 2 for connections within the pixel also makes sense so as to reduce the amount of vias used. These connections are from poly, diffusion, or metal 1. With so many bus wires and transistors in the circuit, it made sense to leave a metal layer (metal 3) just for connecting from the circuitry to the bus.
The remaining layout was heavily influenced by contact spacings and data flow. Incident light is gathered as a current at the left of the pixel circuitry and flows to the bottom of the circuit. The signal goes through both the Video Sampling and the Digital Conversion circuits in the bottom of the pixel. The bits are then stored in the upper right corner, while the analog signal is held for output in the same area. Much of the circuitry is hidden under the power rails to save space. This pixel was also designed with considerations made that it would serve as a replicated component in a large array. Overlapping wells, power rails, and even some circuitry placement was aided by placing the pixel in an array.

### 5.3 Functionality and Performance

The Alpha pixel and its control circuitry was simulated and verified. Simulations were arranged similar to those performed for the prototype chip. This circuit was simulated to work in the 580-750 pW range at similar data and video rates as the prototype circuit.
4.3.1 Functionality

Figure 5.5 shows the clocking of the video circuitry. The optical input signal is at a constant value while being sampled. **Video Clear** is asserted to ensure the storage capacitor is cleared. During the **Video Sample** period, the **video storage capacitor** can be seen charging. Once again, the **video storage capacitor** node is not external to the pixel. When **Video Row Select** is raised, an amplified value from the video storage capacitor is placed on the bus, as seen in the **Video Out** signal.
Just as the video path is very similar to the prototype, the data path is also closely related to the prototype graph (as seen in Figure 5.6). The **Optical Input Signal** in this example is shown pulsing to mimic an actual digital data source. **Clock 1** and **Clock 2** are shown clocking when the **Optical Input Signal** is evaluated and clocked through the D flip flop. The Write Enable signals are aligned with the Clock signals such that each storage bit is written to in order. The Data Bits are shown in the next 4 waveforms of Figure 5.6. The largest architectural difference between the prototype chip and the alpha chip is shown in the remaining two waveforms. **Data Flag** goes high when data is clocked through the D flip flop in the Digital Conversion block. This flag stays
high for reading out with Video Row Select. It is cleared, however, when the pixel’s data
path is addressed using both Data Row Select and Data Column Select. In this example
Data Column select is shown clearing the Data Flag.

![Figure 5.7 Alpha Threshold Control](image)

The thresholding circuit operation is shown in Figure 5.7. There are several important
pieces of information in this graph. First, the addition of a second amplifier has inverted
the control of the circuit. Increasing voltage now corresponds to lowering the optical
threshold. Second, the scale is now in pW, highlighting the ability of this circuit to scale to a
smaller photo current. Third, the control of the threshold is not linear. This is due to the
high amplification of the signal using small transistors. These features will be important to
the control of the chip when it is placed in its operational framework.
4.3.2 Power Consumption

This pixel's power consumption analysis is much like the prototype's power analysis. The circuits in the alpha chip are either the same or dynamic representations of the same circuitry in the prototype chip. This saved space and some power.

![Pie chart showing power consumption](attachment:image.png)

**Figure 5.8 Alpha Power Consumption**

The total power consumption of the pixel has been simulated at 244 uW. The distribution of power is shown in Figure 5.8. It can be noted from this analysis that Amplifiers 1 and 2, located in the Digital Conversion block, are the largest consumers of power.
Chapter 6 Beta

The PHOCI™ Beta chip addresses the power and optical deficiencies of the alpha chip. The alpha chip succeeded in creating a smaller pixel capable of physically scaling to a large array. However, it did have problems with power, fill factor, and dead spot. Some basic conclusions can be drawn from these issues with the alpha chip. Most of the transistors in the alpha chip were minimum sized. In order to aid fill factor, either the photodetector must be made larger or there must be fewer transistors. The same can be said to aid in reducing the size of the dead spot. Power is a more complex issue. There is not such a clear relationship between the number of transistors in a circuit and the power drawn by that circuit. To decrease the power draw and increase fill-factor, it would seem that reducing the number of transistors in this pixel design was a main goal. In order to
make an intelligent decision on this chip, the areas of improvement for alpha must be understood.

6.1 Motivation

The alpha chip presented several areas for improvement. Its fill factor and dead spot must be vastly improved. The alpha’s peak power consumption under full illumination limits its maximum array size and is not applicable in portable applications. In attempting to make the most useful chip that can be applied in many situations these issues must be addressed.

From the picture of the alpha pixel, shown in Figure 5.3, it can be seen that the dead spot is decided as much by the bus structure as it is the circuitry. The alpha vertical bus consists of write enables, video out, data outs, data column select, and the data flag. The vertical bus creates a dead spot of 14.04 μm between two side by side photo detectors. The horizontal bus consists of data row select, video samples, data threshold, VRS, clock 1, current bias, clock 2, and video clear. The horizontal bus creates a dead spot of 12.36 μm between two photo detectors on top of each other. In terms of dead space, this creates a fill factor of 8%. Two conclusions can be reached on how to deal with the bus to fix these optical problems.

A simple conclusion might be to keep the same signals, but use the 5 metal layers available in a more aggressive fashion. This would include distributing the signals equally
between the horizontal and vertical buses. The write enable signals are placed on top of where the storage bits are floor-planned. There could also be a more creative way to allow some write enable bits to come in on the horizontal bus. There are 11 wires in the vertical bus and 8 wires in the horizontal bus. Moving a wire from the vertical bus to the horizontal bus would add space to the horizontal bus, but shorten the vertical bus, and thus shorten the effective dead spot. This, however, would not affect fill factor. In order to keep all the same lines, and help fill factor, the buses must become stacked. By reassigning some of these layers, it is conceivable that some signals could be stacked.

The second method of dealing with a large bus would be to reduce the number of signals. The first group of wires in the bus that attract attention are the write enable signals. These could be interpreted from the clock one and clock two signals. These previously existed in order to drive standard cell latches. With a fully custom and dynamic pixel, these are not entirely necessary. Reduction of the other signals requires more in depth circuit analysis that can be determined from a more detailed analysis of power consumption by the various sub-blocks of each pixel.

With such large power consumption of the alpha chip an in depth analysis had to be performed to see where all this power was consumed. Figure 5.8 shows how much power each section of the alpha pixel draws. The amplifiers take up the majority of power in the pixel. The first amplifier simply separates the current mirror input from the rest of the data path. Using a small pmos transistor keeps the parasitic capacitance from being too large. With larger capacitances on the current source node, the voltage response being
measured was largely dissipated. The second amplifier in the circuit performs most of the amplification.

The threshold circuit’s power consumption is essentially dictated by the current biasing transistor at the bottom of the circuit. This current is chosen globally by the external biasing resistor. This circuit does not draw as much current as the amplifiers, but is still a significant source to the overall current draw of the pixel.

In contrast to the data circuit, the video circuit pulls very little current. The only connection to vdd in the video circuit is the original current source. The current generated by this circuit is in proportion to the light intensity incident on the pixel. This is generally in the range between pico-watts and nano-watts. The current generated by the incident light is a fraction of the incident power. This means that current is also in the pico-amperes to nano-amperes. This is compared to the micro-amperes drawn by several parts on the data side.

Two realizations happened between the design of the alpha chip and the beta chip. There was considerable difficulty in designing the amplifiers so that they would operate in the proper incident optical power range. That is, if the light intensity incident on the pixel was not in the expected range, the amplifiers would be in either a low or high saturation range and not in the amplification range. The second issue at hand was the power consumption. This lead to the notion of using a sample and hold circuit for data thresholding. The video path samples an analog current and outputs an analog voltage. The amplifiers in the data path measure a voltage created from an analog current and produce an analog voltage for comparison to a threshold. A data storage capacitor replaces the amplifiers for building
voltage. A new data sample signal’s pulse width is used for thresholding. An inverter can be used with a static switch point to digitize the voltage on the capacitor. This circuit is now discussed in detail.

### 6.2 Architecture

The Beta architecture was changed significantly from the alpha and prototype architectures. The basic boxes that help define a PHOCI™ chip are common with the alpha and prototype designs. The way these boxes interact is much different, however. In addition to capturing data by a sample and hold circuit, significant signaling changes were made.

As shown in Figure 6.2, the Photoreceiver Block of the beta pixel highlights the first major change between the alpha and beta designs. In particular, the beta pixel uses a data

*Figure 6.2 Beta Pixel Schematic*
sample and hold circuit. A current source is still used to bias the photodiode, but instead of amplifying the voltage drop across the current source, a separate transistor is used to source current to the Digital Conversion block. In this design, the analog current is used for both video and data. The benefit of this can be seen in the digital conversion block (described below).

The Video Sampling block is once again unchanged and contains only the Video sampling transistor and Video Clear transistor. It still takes in the Video Sampling and Video Clear signals.

The Video Storage block is changed only slightly. It contains a small storage capacitor, similar to the alpha chip. The value of this capacitor controls the gate of an nmos transistor that controls an amount of current drawn from the video line when the pixel is addressed. This current is then turned back into a voltage for output from the chip by a trans-impedance amplifier located on the periphery of the sensor array. This block requires the Video Row Select signal and produces the Video Out signal.

The Digital Conversion block is where most of the power and space savings occurs. Instead of having two amplifiers, a differential amplifier and a D flip flop, the block now contains a sampling transistor, storage capacitor, and single inverter. The sampling time pulse width replaces the threshold signal in the alpha design. The current is sampled into the capacitor, creating an analog voltage. When that analog voltage is higher than the switch-point of the following inverter, the light input level is accepted as a '1'. With no
need for a differential amplifier, there is no need for the current bias line. The Digital Conversion block now inputs a **Data Sample, Clock 1** and **Clock 2** signal. **Clock 1** acts as an evaluate signal, and passes the sampled value into the first stage of the Data Storage block. **Clock 2** clears the storage capacitor in the Digital Conversion block. **Data Sample** controls how long the photocurrent is sampled into the capacitor. This functions as threshold previously functioned.

The Data Storage block is now also substantially changed from the alpha chip. The alpha chip controls the storing of bits using 4 write enable lines. These write enable lines are timed with **Clock 1** and **Clock 2** which were also present in the alpha design. This means there are 6 clock lines going into the alpha pixel. The beta chip’s storage is now a shift register. Previously the write enable lines were controlled to create a shift register. In the beta design, the shift register only requires 2 non-overlapping clock signals.

The data flag was also changed significantly. In brainstorming about a data source within a pixel and how that affected the video signal, a new implementation was designed. That is, a data source within a pixel most likely means that pixel’s video will be saturated. A data source must be brighter than the scene the camera is pointing at to be differentiated. With this in mind, a separate digital value for a data flag is unnecessary. A simple high voltage on the video signal could be defined as a data flag ‘true’. To accomplish this, a gate was designed to pull the video signal high when data passes through the Data Storage block. The data flag block only takes in the **Video Clear** signal, for implementation issues. There is no longer a separate line for Data Flag. This saves another bus line.
6.2 Implementation

The circuit design of the Beta pixel focused on reducing transistors in the design to minimize power consumption and increase fill factor. In the implementation, transistor sizes are chosen to minimize power and careful layout is critical to gaining the optical benefits of the circuit. With this pixel the circuit has been made smaller and the photodetector itself has been enlarged significantly. The general layout for this pixel is now a large photodetector located above the circuitry that drives it (Figure 6.3). To minimize
the distance between photodetectors side by side, the buses are aggressively stacked on top of the photodetector guard rails.

This Photoreceiver block begins a very different layout from the alpha and prototype pixels. From those previous designs, it is quickly realized that the p-transistor to n-transistor spacing is the largest spacing requirement inherent in this circuit. To minimize this effect on the pixel size, it is desirable to have a single n-well for the p-transistors. In this fairly linear layout, an n-well has spacing requirements to the left and right of the well. If there were two wells in the design, there would be 4 n-transistor to p-transistor spacing requirements. If there is only one n-well, this spacing penalty is cut to two n-transistor to p-transistor spacings. P-transistors are used in the current source of the Photoreceiver block, the Data Flag and the Data Storage block. From a circuit flow perspective, however, the Photoreceiver and the Data Storage are at opposite ends of the circuit. To enable a single well, the Photoreceiver and Data Flag are placed on one side of the pixel to mate with the Data Storage block in an adjacent pixel.

The Video Sampling block consists of two minimally sized transistors. These transistors are placed immediately next to the Photoreceiver transistors. Because the Video Sample and Video Clear signals have been chosen to run horizontally over the circuit, the routing of these signals to the circuit is a small issue.

The Video Storage block has changed somewhat from the alpha chip. The capacitor has been implemented using a transistor with source and drain connected to ground. The gate of the transistor is then the storage node. This was used because the spacing
requirements associated with the explicit capacitor in TSMC .25 were much too restrictive for use in an arrayed optical pixel design. The routing of the video signal has also changed. Instead of amplifying an analog voltage onto the bus line, an analog current is drawn across the bus line. This is accomplished by connecting the storage node of the capacitor to the gate of a capacitor. The capacitor is then routed through a pass transistor connected to Video Row Select. When the pixel is addressed this current is transformed into a voltage by a trans impedance amplifier located on the outside of the array.

The Digital Conversion block consists of a sample transistor, clear transistor, storage capacitor, and inverter. The sample and clear transistors have been minimally sized for space. The switch point of the inverter has been lowered from a common $\frac{V_{dd}}{2}$ (1.65 V) to a little less than $\frac{V_{dd}}{3}$ (1 V). The combination of sample time, inverter switch point, and incident optical light dictate how fast this sampling circuit can be run as a digital conversion circuit. The capacitor has been implemented exactly the same as the video storage capacitor, using a transistor. The data capacitor's size is also exactly the same as the video capacitor. This could be a future optimization of the chip.

The Data Storage block looks like an extended D flip-flop from the alpha chip. The data storage is now a shift register comprised of pass transistors connecting inverters. To further save space, there are also only 2 bits of storage within this pixel. The output of the last two inverters in the chain are the data bits. These are routed out of the chip by two pass transistors controlled by Data Row Select. This chain is an inverting chain. Thus,
Data bit 0 is output from the pixel as the inverse of Data 0. Data 1 is standard logic.

Data bit 0 is inverted outside the array, while Data bit 1 is simply buffered.

The data flag has now been implemented as a high (3.3) voltage on the video side. The video storage capacitor only charges up to about 90% of Vdd. Using transistors to pull the node to \texttt{Vdd} as a logic gate would. The main transistor is controlled by one of the Data bits, signifying that the Digital Conversion block had accepted a data bit. To pull the node high a pmos transistor is used. Because PMOS transistors are inverse logic, the Data bit controlling this transistor is taken from a negative logic point in the scan chain.

This can be seen in Figure 6.2. The second transistor in this “gate” is controlled by Video Clear. This transistor prevents a short from \texttt{Vdd} to \texttt{Gnd}, as the clear transistor is also connected to the video storage node.

<table>
<thead>
<tr>
<th>Metal 1</th>
<th>Gnd, Local Wiring</th>
</tr>
</thead>
<tbody>
<tr>
<td>Metal 2</td>
<td>Vertical Bus, Local Wiring</td>
</tr>
<tr>
<td>Metal 3</td>
<td>Vertical Bus, Local Wiring</td>
</tr>
<tr>
<td>Metal 4</td>
<td>Horizontal Bus</td>
</tr>
<tr>
<td>Metal 5</td>
<td>Vdd, Optical Shielding</td>
</tr>
</tbody>
</table>

*Figure 6.4 Beta Metal layer assignment*

Reducing the space taken by busing is just as important as reducing circuit size in the pixel. The Beta pixel used 2 stacked vertical buses to make the photodetectors as close as possible to each other horizontally. As the data flow into and out of the array has not changed, there are only three vertical signals: Data Bit 0, Data Bit 1, and Video Out. To make use of all the vertical spacing, Data Sample was also included in this
vertical group. This leaves **Data Row Select, Clock 1, Clock 2, Video Row Select, Video Sample, and Video Clear** to run horizontally. The metal layer assignments are shown in Figure 6.4. The grounded guard rings around the photo detectors require metal 1. To fully utilize each metal layer available, **Vdd** was run on top of the entire array using metal 5, which doubles as an optical shield. This brings up concerns with the resistance of vias going from metal 5 to the circuits just below metal 1. Fortunately, this design has very few connections to **Vdd** and those connections do not use much power, so the effect of this added resistance between **Vdd** and the circuits drawing power is minimized.

### 6.3 Functionality and Performance

The Beta chip has been shown to operate up at up to 20 khz with an LED at a distance of 20 feet. This speed is limited by the optical system consisting of the optical power produced by LED and the lensing in front of the sensor. The primary performance factor of the beta chip is power consumption. The most significant changes to the PHOCI™ architecture occurred in the beta chip. The following simulation waveforms highlight the differences from the previous chips and show the new operation.

#### 6.3.1 Functionality
Figure 6.5 shows the Beta Video signals. These are largely the same as in the previous chips. As such, the video control signals are still largely the same. A constant optical input is shown. The capacitor is first cleared with Video Clear. The optical input signal is then sampled with the Video Sample signal. The capacitor can be seen charging up in the video storage capacitor signal (which is not visible outside the pixel).

The Video Row Select propagates the signal from within the pixel to outside the array. The Video Out signal is produced by converting the current produced by the pixel into a voltage. This is accomplished with a trans-impedance amplifier on the outside edge of the sensor array.
Figure 6.6 Beta Data Signal Diagram

The Beta Data path, shown in Figure 6.6, is where the most significant control signal changes occur. The **Optical Input signal** is a pulse to illustrate data communication. There is now a **Data Sample** pulse that is aligned with the two clock pulses. The **Data Sample** pulse samples the light input. **Clock 1** clocks the sample through the first stage in the data storage block. Intended operation is for two bits to be clocked into the storage bits in between data readout. This means there are two bits received serially by the photodetector. As the data storage is a shift register, **Bit 0** first
appears in Bit 1, before it is clocked to its readout position at Bit 0. This explains why Bit 1 is shown going high first. In this example Data Row Select is kept high (not shown) in order to show the operation of the new circuit. Also in this example, Video Sample is turned off (not shown) to show that the data flag is operating separately from the video signal. In this simulation the video output is connected through a resistor to Vdd. This appears in Figure 6.6 as Video Out is pulled to Gnd when current is flowing, meaning the Data Flag is true. No current flows when Data is not present because Video Sample is turned off.

Thresholding of the Beta chip is the main difference between the beta and alpha chip. The signaling of the beta thresholding circuit is shown in Figure 6.7. A constant Optical Power Signal is shown. The data storage capacitor is first cleared with Clock
While **Data Sample** is kept high, the capacitor stores current and builds a voltage. Once this voltage is higher than the first inverter’s switch point, a data source is accepted and the inverter outputs a '0', as seen in the **thresholded data signal**. This signal is internal to the pixel, but illustrates when a bit is accepted as a potential data source. Figure 6.8 illustrates the control of the Beta sensor's thresholding control. This graph shows a slow turn on of a transistor used as a capacitor for low light levels. This area corresponds to the “Depletion” region of transistor operation when used as a capacitor.

**Figure 6.8 Beta Thresholding Control**

6.3.2 Power

Power consumption of this chip is much different than the previous chips. The power hungry amplifiers and static circuits have all been replaced with more dynamic circuits. In addition, the inverters that remain have been resized to consume much less power when switching. The remaining power consumption is detailed in Figure 6.9. With this power
savings, the beta sensor consumes 38 times less power than the alpha chip. This can translate into an array with 38 times more pixels than an alpha array at the same power levels.

![Pie chart showing beta power consumption](image)

**Figure 6.9 Beta Power Consumption**

6.3.3 System Results

![Image of test pattern taken with beta chip](image)

**Figure 6.10 Picture of test pattern taken with Beta chip**

The beta chip was integrated into a test system. Figure 6.10 shows a picture taken with the beta chip system. The same pattern taken with the prototype chip (seen in Figure 4.9)
is shown. The prototype contained only a 7x7 array which was only able to show the pattern. A scene much larger than the pattern can be seen with the beta sensor’s 80x72 array.
Chapter 7 Gamma

The gamma chip augments the PHOCI™ architecture by further reducing the dead spot and power consumption by spreading data circuitry among several pixels. Each previous chip has combined both video and data storage within a single pixel. The gamma pixel contains video storage in each pixel while data storage is contained within a group of pixels. Thus, while each pixel is sensitive to both data and video signals, data processing is performed by a group (or cluster) of pixels. The gamma sensor has been implemented as a 4x4 data cluster (Figure 7.1). This results in a video resolution of 128x128 and data resolution of 32x32.
7.1 Motivation

The Beta chip succeeded in finding a promising circuit design that allows the necessary functionality as well as a higher fill factor than the alpha chip. However, power consumption is still an issue when the beta chip is scaled to megapixel resolutions. For the final (gamma) chip an architecture capable of supporting larger arrays is explored. Optical and electrical considerations directed the design of the cluster and its size.

Clustering allows for a smaller dead spot at the expense of requiring a greater distance between two separate data sources. A cluster is a group of pixels that have separate video pixels, but act as one data pixel. Using spreadsheets, several different clustering geometries were developed. The relationship between pixels in the array to the field of view it is projected upon is held constant. The only difference from the previous non-clustered designs is that the minimum space between data sources is several pixel-widths rather than a single pixel width. A portion of the spreadsheet showing this relationship is shown in Figure 7.2. This figure shows a comparison of a 128x128 array with a 256x256 array for clustering configurations of 16x16 pixels, 8x8 pixels, and 4x4 pixels. These schemes are then projected onto 9 different fields of view. The spreadsheet shows the video resolution (which is constant across each clustering configuration) and the data resolution. Distances between data sources are computed and can be used to support design considerations for various applications.
There are several electrical considerations to implementing the cluster. The benefits of clustering are a reduction in power consumption per pixel and a reduction in dead spot achieved by distributing the data circuitry among several pixels rather than one. Clustering must have little to no effect on the optical requirements of single data sources.

One simple way of combining the data intensities from a cluster of photodetectors is to gather the current generated by each photodetector in one common sampling capacitor.

**Figure 7.2 Gamma Resolution Exploration**
Unfortunately, this has a signal to noise problem. More precisely, each photodetector produces a dark current (not related to optical light incident on the photodetector) due to thermal generation of electron hole pairs\(^{18}\). Assuming a square design, clustering can introduce a squared relationship between the size of the cluster and the dark current. For example, if a 4x4 array were created and each photo detector simply tied together the dark current being sampled would now be 16 dark currents. The goal of the cluster is to maintain the ability to track data communication even when it falls incident on a single pixel. Consequently, the increased dark current noise generated by simply tying the photodetectors together makes this solution unacceptable. Thus, a different solution must be discovered where the current generated by the data source’s intensity incident on a single pixel is larger than the dark currents of the cluster. The solution used is to only tie together photodetectors of a common column in the cluster and “OR” the results of the columns together. The additional dark currents across the column are sufficiently low that the ability to detect a low light level data source is kept. This also produces a solution where the dark current scales linearly with cluster size, so that larger clusterings may also be possible.

### 7.2 Architecture

The architecture of the gamma chip is closely related to the architecture of the beta chip. It is only the data portion of the chip that has been spread out within the cluster. The Photoreceiver block, Video Sampling block, and Video Storage block are all exactly the same as in the beta chip and common to every pixel in the gamma chip. This preserves the high video resolution of the chip. The data circuitry is spread out among the pixels to
improve fill factor and dead spot, as well as further reduce power consumption of the entire array.

The Photoreceiver block in the gamma chip is the same as the Beta chip. The current provided by the Photoreceiver block to the digital conversion block is common to a column within the cluster. This block requires no external bus signals. The data current line, however, is an internal cluster bus line. This means that the data current line must be placed on a bus internal to the cluster to be routed to another pixel within the cluster. This
allows the data circuitry to be spread throughout the cluster to enhance functionality and save space.

The Gamma Video Sampling block is common to every pixel in the array. This block samples the current coming from the Photoreceiver block and clears the Video Storage. This block requires the signals Video Sample and Video Clear. These have no directionality.

The Video Storage block contains a storage capacitor and circuitry to read out an analog value. This block takes in sampled current from the Video Sampling block and outputs a Video Out signal. By design, this signal is a vertical signal. This block also takes in the horizontal signal Video Row Select to address the pixel.

The Digital Conversion block is where the clustering takes place. There are several issues that must be addressed for the cluster approach to scale and not suffer too many penalties. First, as several photodetectors' outputs are combined, their dark currents add together. This dark current is noise in the electrical signal. When multiple detectors are combined, this noise increases, thus decreasing the signal to noise ratio. Another issue with clustering is to keep the optical metrics on the scale of the pixel and not the cluster. The dead spot and required optical power for a single data source should be detectable by one pixel and not require illumination of multiple photodetectors in the cluster. The only influence the cluster should have on the performance of the system is in defining the minimum separation distance required between two adjacent data signals in the field of view. The
size of each individual data source must still be compared to the dead spot and fill factor
defined by the measurements of a single pixel and not the cluster.

To avoid vastly increasing dark current’s effect on a clustered data pixel, the gamma chip
pipelines the digital conversion block. Instead of summing the currents from all
photodetectors within a cluster, the gamma chip sums the currents from a column of
photodetectors. At the column level, this sampled data is thresholded with an inverter as
is done in the beta sensor. The results of the column sums are then “OR-ed” together. To
recount, the optical outputs of the photodetectors are summed by column, producing a
digital value determining if the column has data or not. The Data Storage then reads the
“OR-ed” combination of these digital values. This circuit requires Data Sample, Clock
1, and Clock 2. This signals have no directionality. The circuit also receives the internal
summation of photodetector current from the Photoreceiver block. The Digital Conversion
block produces an internal cluster signal for the data to go into the Data Storage block.
Additionally, The digital conversion block is broken up among several pixels within the
cluster. The implementation will take into account how the circuit is subdivided and which
additional internal signals will be routed from pixel to pixel.

The Data Storage block is a shift register now spread among the pixels in the cluster.
Once a 4x4 cluster was chosen it was logical for the layout to have 4 storage bits. This
circuit takes Clock 1 and Clock 2, which have no specified directionality, and Data
Row Select which is a horizontal signal. The Data Storage block produces 4 Data Bits
which are vertical signals. The Data Storage block takes the internal cluster signal digital
output from the Digital Conversion block. The Data Storage block also produces an inverse data bit for the Data Flag block. This is a signal that is kept internal to the cluster. In addition to these external signals, the Data Bits are distributed among the cluster pixels. This means there will be internal signals connecting the data storage bits. These signals will be specified during implementation.

Because the data is stored in the cluster and not the pixel, the Data Flag of the cluster is only necessary in a single pixel within the cluster. This means the data flag signifies the possibility of data within the cluster. The data flag operates on the video signal of a pixel, in a manner similar to its implementation in the beta sensor. The Data Flag takes Video Clear, which has no directionality, and produces Video Out which is a vertical signal. The data flag also takes an inverse data bit from the Data Storage block which is an internal cluster signal.

7.3 Implementation

The gamma implementation contains a significantly different set of problems from any of the previous chips. The previous chips have a specific circuit to be laid out in the smallest, contiguous area possible. For the implementation of the gamma chip the circuit must first be partitioned into pieces that will go in each pixel. For example, some of the circuit is in every pixel, while other portions of the circuit are only in a few pixels within the cluster. The actual layout of each transistor and circuit becomes quite simple once the partitioning scheme is decided upon.
7.3.1 Busing scheme

With the extra partitioning of circuits across the cluster, the importance of bus design is magnified. The circuits cannot be distributed if there is no way to connect them. The gamma bus design motivation is again to minimize the horizontal space between adjacent photodetectors and focus on placing the majority of the bus and circuitry beneath the photodetector. Stacked vertical wires are used to minimize horizontal space between photodetectors.

In the beta design, Video Sample and Data Bit Out are the only required vertical signals. Video Row Select and Data Row Select are the only horizontal signals. The remaining global signals are Video Sample, Video Clear, Data Sample, Clock 1 and Clock 2. In addition to these signals, there are now requirements for internal cluster wiring. Because the photodetectors' current is summed by the column, another vertical line for combining these currents (called the Column Capacitor Signal) is required. In addition to the current Column Capacitor Signal, a generic Inter-Cluster Wiring pathway is required. This is not a wire with a single definition; it is a re-useable wire space for single signals traveling between adjacent pixels in the cluster. Horizontal wiring has the same approach, but is less complicated. As mentioned previously, there are only two required horizontal signals and 5 remaining signals with no specific directionality. As an intermediate step these 5 signals would all be made horizontal to continue decreasing the horizontal space between photodetectors. The layout of the Video Storage
block, however, makes Video Clear and Video Sample vertical signals. This will be discussed in the following section. The final busing scheme is shown in Figure 7.4.

<table>
<thead>
<tr>
<th>Metal 1</th>
<th>Gnd, Local Wiring</th>
</tr>
</thead>
<tbody>
<tr>
<td>Metal 2</td>
<td>Vertical Bus, Local Wiring</td>
</tr>
<tr>
<td>Metal 3</td>
<td>Vertical Bus, Local Wiring</td>
</tr>
<tr>
<td>Metal 4</td>
<td>Horizontal Bus</td>
</tr>
<tr>
<td>Metal 5</td>
<td>Vdd, Optical Shielding</td>
</tr>
</tbody>
</table>

*Figure 7.4 Gamma Bus Structure*

7.3.2 Partitioning Scheme and Layout

With the bus design mostly complete, a circuit partitioning scheme needs to be determined. Logical breaks in the circuit are required to distribute the electronics in a way that minimizes unused space and preserves functionality. Partitioning of this circuit is determined by the circuit function and the exact connections that necessary.

The Photoreceiver block is common to every pixel. This block begins the Video Sampling and Video Storage blocks. The only signal external to the pixel that the Photoreceiver block takes in or produces is the **Column Capacitor Signal**. The Photoreceiver block uses PMOS transistors for its current source. These require an n-well. Likewise, the photodetector guard ring requires a p-well. This creates an n-well-p-well-n-well spacing requirement per the rules associated with TSMC .25 μm. The current source transistors have been sized longer than wide to accommodate the smallest possible n-well. This minimum space between detectors that includes the guard ring width around two
detectors' boundaries and the n-well in between them is 40 lambda (lambda =0.12 μm for TSMC 0.25 μm process). With spacing requirements around a wire and using minimum wire widths, 5 wires fit in 41 lambda. As previously mentioned there were 2 required horizontal wires and 5 wires with no direction. This means there is space for 5 horizontal wires with 2 of those spaces taken up by required horizontal signals and leaving 3 spaces for the 5 wires with no specific direction. This suggests moving 2 wires to a vertical bus. The vertical bus is stacked with each wire space stacking two wires on top of each other. Thus, it makes sense to add to the vertical bus in multiples of 2.

The Video Sampling block is also common to every pixel in the array. This block consists of a sampling transistor and clear transistor which are controlled by Video Sample and Video Clear respectively. The contact spacings dominate the layout of this block because the transistors are minimally sized.

*Figure 7.5 Base Gamma Pixel*
The Video Storage block completes the layout of the base pixel for the gamma chip. The Photoreceiver, Video sampling and Video Storage are common to every pixel. This is essential to keep the video resolution at the maximum while only reducing the data resolution. The Video Storage block contains a large capacitor implemented with a transistor, a current sinking transistor, and a select transistor connected to Video Row Select. The large capacitor in the Video storage block can be seen placed vertically to the right of the photodetector in Figure 7.5. Placing the capacitor in this space creates more space for digital circuitry under the Busing wires. The video storage capacitor has few connections and can simply be placed under the vertical bus with no worries of bus connections or vias complicating its placement. This also makes room for the 2 wires that have been suggested for vertical layout. Because the Video Sample block and Video Storage blocks are so close to the vertical bus Video Clear and Video Sample were chosen to be the two additional vertical wires.
The Digital Conversion block contains circuitry that can be distributed among the pixels within the cluster. Figure 7.6 shows the cluster layout with a grid for discussion of the circuit distribution.
Figure 7.7 shows the full Digital Conversion block circuit for the cluster. There are 16 photodetectors arranged in groups of four for the four columns. The output from these photodetectors is collected in the data storage capacitors. There is one data storage capacitor per column. These capacitors are located in row D shown in Figure 7.6. The thresholding inverter for each data storage capacitor is located in row C. This thresholding inverter is connected to a current-sourcing PMOS transistor. The currents controlled by the thresholding inverters are collected in a single capacitor located in pixel B3. The output from this circuit begins the Data Storage block.

The photodetectors are connected to their column’s data storage capacitor vertical line. The data storage capacitor stores and then clocks the stored voltage for evaluation in the thresholding transistors in row C. This is accomplished using the inter cluster wiring channel. A horizontal channel is needed to sum the currents from the thresholding circuits. **Data Row Select** is only used in the Data Storage Block located in row A of Figure
7.6. This allows that channel to be used for the sum of currents in row C. The intercluster wiring is then used to move this signal to the summing capacitor located in pixel B3. The result of pixel B3 is then propagated to the start of the Data Storage in row A using the intercluster wiring.

The Data Storage block occupies row A, as seen in Figure 7.6. There is one bit per pixel. Data Sample is not used in this row. This makes a channel for the data bits to be connected in a shift register style.

The Data Flag is only necessary in one pixel of the cluster. As data is common to the entire array, there is no need to essentially overwrite the valid video samples throughout the cluster with redundant data flags. The Data flag block is located in pixel B2. The Data flag requires the signals Video Clear and an inverse data bit from the Data Storage. Pixel B2 is near an inverse logic node of the Data Storage and is therefore a logical choice for data flag placement. Inter-cluster wiring is used to route the inverse data bit from the data storage to the data flag.

7.4 Performance and Functionality

The gamma chip’s functionality and control is similar to the beta chip. Preliminary testing shows the gamma chip to work in a beta system with minor changes.
Figure 7.8 shows the clocking of the video. The **Optical Input Signal** shown is increasing in optical power. The **Video Clear** clears the video storage capacitor. The **Video Sample** samples the incoming current. **Video Row Select** routes the current produced by the pixel through a trans-impedance amplifier located on the outside of the array.
Figure 7.9 illustrates the clocking of data through the cluster. The Optical Data Signal shown is incident on a single pixel. No other pixels are contributing current to the data transmission. The Data Sample, Clock 1, and Clock 2 signals are the same as in the beta chip. The four data column storage capacitors are shown to illustrate that only one column is receiving data. The cluster storage capacitor is the “OR-ing” together of all the column capacitors. The first data bit shows the first stage in the shift register. The Data Bits go high as each accepted bit is clocked in. Video Row Select has been left high for this simulation, while Video Clear clears the video storage
capacitor node and shows when data is going through the pipeline. When there is no data, a standard video signal of lesser proportions can be seen on the Video Out.

Figure 7.10 shows the thresholding of the data signal. The data storage capacitor is first cleared with Clock 2. The Optical Input Signal is kept constant and Clock 1 and Data Sample are kept high to show when the sampled current is accepted as data. The thresholded data shows when the inverter switches; signifying an accepted data source.
Figure 7.11 shows the threshold control of the gamma chip. The overall graph appears exponential, but this is skewed by the readings in the low optical power region. This is still a transistor being used as a capacitor and reflects the issues as seen in the Beta design at low light levels. The graph is linear in the 50-500 nW range. This mirrors the charging of a capacitor.

7.8 uW

Figure 7.12 Gamma Power Consumption
The power savings of the gamma chip is shown in Figure 7.12. This is a misleading graph when compared to previous graphs. All components of the cluster are shown as opposed to a single pixel. This is necessary as each pixel is different and consumes a different amount of current. This graph is the accumulation of power consumption of one of each circuit. The decision circuit is replicated 4 times in the cluster. The current mirrors are replicated in each of the 16 pixels in a cluster. The graph shows a comparison of power consumption from one circuit to another. The design of the gamma chip was meant to be scalable to various array sizes. This graph can be used to locate potential issues as the cluster and array are scaled.
Chapter 8 Comparison of chips

Each chip explored in this project stresses different goals. The prototype sensor is designed to create a baseline of functionality and performance for a data integrated imager. The alpha sensor the same architecture as the prototype but a different implementation to attain a larger array size. The beta sensor addresses both optical and power concerns of the alpha chip with the introduction of a data sample and hold circuit. The gamma sensor furthers the beta architecture by implementing a data cluster.

For all explored simulations and scenarios, the beta and gamma chips are superior to the prototype and alpha designs. Optical and electrical features are vastly improved because of the use of a data sample and hold circuit. These two designs allow for scaling of the array much further than the arrays that were manufactured.

The impact of the data sample and hold circuit can be measured in several comparisons. Optically, each chip can be compared with dead spot and fill factor, as well as supported pixel array sizes. Electrically speaking, each chip can be compared with transistor counts and power consumption. System performance can be compared with supported pixel array sizes, maximum communication speed, and supported active pixels. By leveraging each of these specific benchmarks against each other, it could be seen that the PHOCI™ technology has a number of implementations and applications.
Figure 8.2 and Figure 8.3 show the comparison of fill factor and dead spot across each chip. The stark difference in fill factors of the beta and gamma chips is from the use of the data sample and hold circuitry as well as using larger photodetectors.
Figure 8.4 shows the comparison of each chip’s power consumption. Power has been reduced so significantly that in order to graph the comparison, the power consumption scale must be made logarithmic.

The main goal of the progression of chips has been to support larger and larger arrays. To accomplish this goal each chip required a large reduction in power consumption and decrease in dead spot. The PHOCI\textsuperscript{TM} concept is characterized by storing data within the array. The progress from one chip to the next is characterized by the use of a data sample and hold circuit.
Chapter 9 Conclusions

This thesis has reviewed the investigation of designs and implementations of a series of data communicating imaging chips. To incorporate data storage with video storage, several different circuits were explored. Over the course of the project, optics dominated the goals of the chips. Our studies focused on the design problems of fill factor, dead spot, and array size instead of data bandwidth or active channels. Power consumption, fill factor, and dead spot have been identified as key metrics in evaluating each chip.

Within the investigations reported in this thesis, four sensor designs were studied. The first series of chips were fabricated as tiny chips (called Prototype sensors) to evaluate our basic ideas for building a data communicating imager. The next three sensor designs (the Alpha, Beta, and Gamma sensors) were all larger chips planned to prove the data communicating imager concept at larger scaling factors. The prototype and alpha sensors captured data communication information from the photodetector by voltage amplification. Unfortunately as the design moved from the prototype to the alpha sensor the photodetector size was substantially reduced which required an increased application step. Unfortunately the resulting alpha sensor design could consume too much power if a major portion of the chip was illuminated. Consequently, this design solution is not scalable to large arrays. The beta and gamma chips modify the data capture circuit to use a sample and hold model. These sensors prove that using a sample and hold circuit for capturing data transmission is a valid design solution to support megapixel sized sensors. The data sample and hold circuitry also presents a finer control of the threshold needed to
recognize an optical data signal. The alpha chip threshold control is related to the amplifier’s amplification function; the data sample and hold is related to the linear charging of a capacitor. In light levels outside the amplifiers range, the alpha chip simply will not work, as the amplifier will be saturated either on or off. The data sample and hold circuit allows the system to continue holding the sample pulse open for low level situations, or clocking more quickly for high light levels.

Another conclusion is that data source size is strictly related to dead spot and that data communication is not substantially affected by fill factor. Fill factor is a common measurement of the quality of a video camera. The dead spot dictates when data sources can become lost in the space created by electronics between adjacent photodetectors. These data communicating imagers track data sources while also capturing image data. Thus, both fill factor and dead spot size are important metrics in their design.

The notion of clustering has also been proven feasible by the gamma sensor design. Clustering reduces data resolution and the total number of active data communications that can be simultaneously occurring. However, these reductions allow the design of sensors with an increased fill factor and reduced dead spot and power consumption. The gamma design illustrates clustering with a 4x4 cluster of video pixels to create a “virtual” data pixel. The concept of clustering, however, can be applied to other cluster sizes such as 2x2, 8x8, or 16x16. While clustering is also possible in irregular cluster configurations like 16x9 or 3x2, these geometries were not explored.
9.1 Future Work

There are many possibilities for the future of the designs discussed within this thesis. Aside from common timing and performance enhancements, the architectures described within can be further explored and adapted.

The beta chip could have several improvements. It can be implemented with more storage as it is the only design described within this thesis that has only 2 bits of storage per pixel. There could also be individual thresholding values held for each pixel. With this ability to store a state the array could adapt to a wider range of intensities across the array.

The gamma chip has many possibilities for advancement. An array based on gamma clusters can be scaled into the megapixel region. Increasing the size of the cluster allows for even larger arrays to be created. As the gamma chip is designed now there is one bit of storage per row in the cluster. In this design scaling the cluster also scales the size of the buffer per data cluster. As larger clusters are created, more rows become available. This could lead to even more storage in the cluster. This would significantly increase the number of supported active channels while providing a high quality image. The extra space in the cluster could also be used to add more data analysis to the array. Oversampling could be performed at the cluster level, thereby making better use of the stored bits in the cluster.
References


[8] Frenzel, Louis, “ZigBee Zooms To Market,” Electronic Design, Jan 12 06, pg 64A


   Http://www.vlcc.net/e


